AN2645
Application note

Migration and compatibility guidelines for STM8S microcontroller applications

Introduction

For designers of STM8S microcontroller applications, it's important to be able to easily replace one microcontroller type by another one in the same product family. Migrating an application to a different microcontroller is often needed, when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may force you to switch to smaller components and shrink the PCB area. This application note is written to help you and analyze the steps you need to migrate from an existing STM8S-based design to any one of the 20+ other microcontroller types in the fast-growing STM8S family.

To save your time, this application note groups together all the most important information and lists the vital aspects that you need to address.

All the information included here can also be extremely worthwhile in your first STM8 design, not immediately concerned by a migration project. Studying the issues now will help you tackle any future requirement by designing for compatibility from the beginning. To use this application note fully, general STM8S knowledge is required, you can learn it from the STM8S family reference manual (RM0016), the STM8S datasheets, and the STM8S Flash program memory / data EEPROM programming manual (PM0051).

This document is divided into three main sections:

● **Section 1: STM8S family compatibility**: This section presents a first level view of the different aspects of the STM8S family architecture that are important to consider when planning a new design or migrating. The microcontroller blocks and peripherals are grouped and identified either as compatible or compatible with minor limitations.

● **Section 2: Planning for migration:** This section gives an overview of common migration cases. It provides a checklist of items which are potentially impacted by each case to allow you to quickly analyze which subjects you need to anticipate.

● **Section 3: Block-by-block compatibility:** This section lists all the topics for each block, focussing on the compatibility aspects in more detail.

Contents

List of tables

List of figures

1 STM8S family compatibility

1.1 Family concept

The STM8S family is one of a growing number of different STM8 microcontroller families.

All these STM8 microcontroller families are based on common robust and low cost 8-bit high performance core with rich set of enhanced peripherals. This ensures high level of compatibility within the STM8 'world', especially in terms of software development, compilers, debugging environment, programming tools and driver libraries.

The STM8S product family offers a wide choice of memory sizes and package types to fit different application requirements as closely as possible. So when there are new requirements on the application side, it can make sense to switch to another STM8S type with different memory capacity or package size.

The STM8S family is divided into two product lines, and within each product line there are two main sub-families:

- **STM8S Performance line** includes STM8S208 and STM8S207 sub-families
- **STM8S Access line** includes STM8S105 and STM8S103 sub-families

The STM8S family also includes some application-specific microcontrollers (ASSM) like the STM8S903 which is derived from the STM8S103 sub-family and which has extra features.

Both main product lines provide a complete set of essential peripherals. **STM8S Access line** targets applications requiring reduced cost, lower memory capacity, fewer GPIOs and less advanced features.

The wide range of available pin-counts and package sizes is discussed in *Chapter 3.1: Package pinout*.

All STM8S family microcontrollers use the same application development tools:

● Embedded single wire interface module (SWIM)

● Software integrated development environment (IDE) tools including assembler, simulator, debugger, programmer:

– ST Visual Develop (ST)

– Ride (Raisonance)

● In-circuit debugging and programming tools

– STIce from ST (full hardware emulator)

– RLink from Raisonance (low cost debug/programming tool)

● Starter kits and evaluation boards

● C compiler and assembler tool chains (Cosmic, Raisonance)

● Firmware libraries (peripheral control examples, MISRA or class B compliance, touch sensing)

● Application notes

By using a common development environment, you significantly reduce code maintenance effort and shorten the time-to-market, especially in cases when an application has to be migrated from one STM8 microcontroller to another.

By using the drivers provided in the STM8S firmware library to interface with the hardware, it becomes reasonably straightforward to move the application firmware from one STM8

product to another. The principle job is analyzing the details on the hardware side, taking care of the placement and availability of the peripheral I/O functions in the pinout. Details about this can be obtained in the STM8S datasheet and further in this document in *Section 3.1: Package pinout*.

Figure 1: STM8S family block diagram gives an overview of the STM8S blocks and their compatibility level, as discussed further in the next sections.

1.2 Fully compatible blocks

The STM8S family embeds a set of system blocks which are by definition common to all products. Those blocks are identical, so they have the same structure, registers and control bits. There is no need to perform any software change to keep the same functionality at the application level after migration. When external components are needed (e.g. Vcap capacitor) no change is required from one product to an other. All the features and behavior remain the same. These blocks are printed in green in *Figure 1*.

Fully compatible parts and peripherals are:

● STM8 core
● Debug / SWIM module
● Power on Reset and Brownout reset (POR & BOR)
● Voltage regulator
● Low speed internal RC (LSI)
● Independent watchdog, Window watchdog
● Auto wakeup timer (AWU) and Beeper unit

1.3 Blocks that are compatible with minor exceptions

Some of the peripherals or functional blocks can have differences in their electrical parameters, structure, registers, control bits or other minor aspects but not in their main functionality. The CAN peripheral is not available in all STM8S devices, so this aspect can be considered as an incompatibility, too.

The following functional blocks can be considered as compatible with only a few negligible differences:

● Interrupt management (interrupt vectors)
● Power control (wake up from low power mode)
● GPIO (I/O capabilities)
● SPI (max speed)
● I2C (true open drain)
● CAN (available only in STM8S208x subfamily)
● Clock controller with internal RC oscillators (accuracy, calibration)
● Internal memories (FLASH, SRAM, EEPROM, boot ROM - size & organization)

You can find more details about these blocks in *Chapter 3: Block-by-block compatibility analysis*. They are shown in yellow in *Figure 1*.

1.4 Blocks that are compatible with significant exceptions

A few peripherals have additional features or lack important functionality compared to the same peripheral in other STM8S sub-families. For these particular peripherals you have to adapt the software drivers and check all possible hardware dependencies.

The peripheral and functional blocks in the following list are compatible with significant exceptions. The package pinout is high on the list, as this aspect requires special attention:

● Package pinout

● ADC

● UART

● Timers

You can find more details in *Section 3: Block-by-block compatibility analysis*. These blocks are shown in red in *Figure 1*.

Figure 1.   STM8S family block diagram
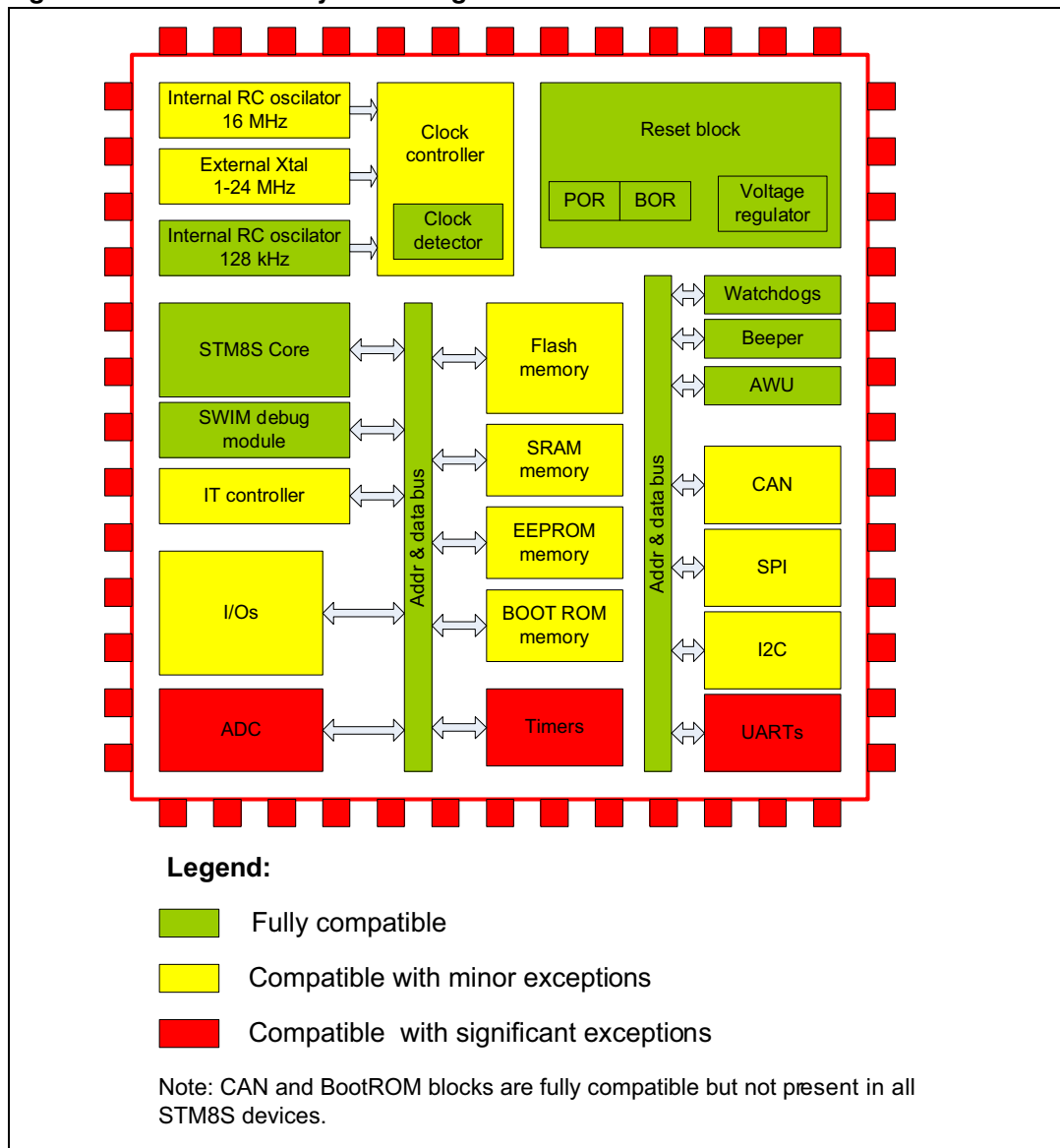
2 Planning for migration

You can use *Table 1: STM8S family compatibility quick reference table* as a starting point for planning any migration from one STM8S microcontroller to another. This table shows the available migration choices and indicates the features that need special attention in each case.

The table is intended to be used as follows:

● Sub-families are listed in rows. Moving between the rows means changing the sub-family.

● Available package sizes are listed in columns. Moving between columns means changing the pin-count.

● The gray fields represent the migration between each column or row and give the impacted features.

The impact of moves between two subfamilies is common for all available package pairs. Therefore all gray cells in rows are merged into common fields. The text in these common fields is divided into two lines:

● When migrating upward: the upper line lists the impact of added features and the lower line lists the features that are lost due to the migration.

● When migrating downward, the lower line lists the added features and the upper lines lists the features that are lost.

A move to the right towards smaller packages mainly leads to a loss of I/O pins and their related alternate functions. So the content of these cells is a simple list of impacted items only.

This section mainly discusses cases of migration between neighboring pairs. However your project may be a migration over several rows or columns in *Table 1* or even in a diagonal direction. In this case, you should check the differences indicated in each step passed by the vertical and horizontal moves through the table.

Getting started:

1. Specify the migration pair and the direction of the migration, with reference to *Table 1*.

2. In *Table 1*, find the gray cell between the selected migration pair.

3. Check here the list of items impacted by any difference in given direction.

4. Check the corresponding paragraph of *Chapter 3: Block-by-block compatibility analysis* for each of items listed there.

5. Check appropriate datasheets and reference manual for more details.

Table 1.   **STM8S family compatibility quick reference table**

		Pin-count									
		80-pin		**64-pin**		**48-pin**		**44-pin**		**32-pin**		**20-pin**
	STM8S208x	GPIO (PH,PI) TIM1 (CH1-3N) ADC (ETR)										
		CAN No feature added									
	STM8S207x	GPIO (PH,PI) TIM1 (CH1-3N) ADC (ETR)		GPIO (PF,PG) ADC (AIN10-15) ADC VRef				GPIO ADC (AIN8) TIM1		I/O Supply ADC UART I2C		
		ADC2 ADC1	HSE 24 MHz HSE 16 MHz	HSI calibrated +/-2% HSI calibrated +/-1%		UART1 & UART3 UART2	SPI 10 Mbit SPI 8 Mbit				
Functionality	STM8S105x					ADC TIMERS		I/O supply ADC I2C			
						ADC supply ADC inputs I/O supply UART2 TIM3 IO Boot ROM RWW GPIO UART1 True open drain at I2C					
	STM8S103x									ADC TIMERS SPI UART		
									GPIO TIM2 TIM4 ADC inputs Internal ref. TIM5 TIM6		
	STM8S903x										

3 Block-by-block compatibility analysis

3.1 Package pinout

Migration within the STM8S implies small changes in the pin layout and related changes in the device functionality. The migration requirements are analyzed here under two main aspects, depending on whether the migration is horizontal or vertical in *Table 2: Overview of packages in each sub-family*.

● Vertical moves are described in *Section 3.1.1* and represent migration from one sub-family to another. No package change is assumed at this point.

● Horizontal moves are detailed in *Section 3.1.2* which covers migration between different packages inside the same sub-family.

The same syntax as in the STM8S datasheets is used here:

pin name (pin type) / alternate functions [optional functions]

Functions affected by migration are printed in bold.

Special groups of pins like power supply, alternate and optional outputs or system pins are discussed separately.

See also *Figure 2: STM8S pinout compatibility guide from 80-pin to 20-pin packages on page 19*.

Table 2. Overview of packages in each sub-family

		Pin-count					
		80-pin (xxxM)	**64-pin (xxxR)**	**48-pin (xxxC)**	**44-pin (xxxS)**	**32-pin (xxxK)**	**20-pin (xxxF)**
Sub-family	**STM8S208x**	LQFP	LQFP				
	STM8S207x	LQFP	LQFP	LQFP	LQFP	LQFP	
	STM8S105x			LQFP	LQFP	LQFP VFQFN	
	STM8S103x					LQFP VFQFN	TSSOP WFQFPN
	STM8S903x					LQFP VFQFPN	

3.1.1 Migration from one sub-family to another one

Migration between sub-families highlights the basic differences between their peripherals, features and capabilities. When the pin-count remains unchanged, the peripheral I/Os often stay on the same pins, but their properties can differ slightly (e.g. UART2 x UART1, ADC2 x ADC1, I2C etc.).

Note: *In Table 3 to Table 15 the differences are shown in **bold**.*

Refer to the migration checklist described in *Chapter 2: Planning for migration* and the next sections for more details about all the differences mentioned here.

Table 3.   **Migration between STM8S208 and STM8S207 80-pin or 64-pin packages**

STM8S208M, 208R	STM8S207M, 207R
PG1 / **CAN_RX**	Not available
PG0 / **CAN_TX**	Not available

Table 4.   **Migration between STM8S207 and STM8S105 48-pin or 44-pin packages**

STM8S207C, 207S	STM8S105C, 105S
PA4 / **UART1_RX** PD6 / **UART3_RX**	PD6 / **UART2_RX**
PA5 / **UART1_TX** PD5 / **UART3_TX**	PD5 / **UART2_TX**
PA6 / **UART1_CK**	PC1 (HS) / TIM1_CH1 / **UART2_CK**

Table 5.   **Migration between STM8S207 and STM8S105 32-pin packages**

STM8S207K	STM8S105K
PD6 / **UART3_RX**	PD6 / **UART2_RX**
PD5 / **UART3_TX**	PD5 / **UART2_TX**
Not available	PC1 (HS) / TIM1_CH1 / **UART2_CK**

Table 6. **Migration between STM8S105 and STM8S103 32-pin packages**

STM8S105K	STM8S103K
VDDIO	Connected internally to VDD
VDDA	Connected internally to VDD
VSSA	Connected internally to VSS
Not available	**PA3 (HS) /** TIM2_CH3 [SPI_NSS]
Not available	**PB7**
Not available	**PB6**
PF4 / **AIN12**	Not available
PB4 / **AIN4** [I2C_SCL]	Not available
PB5 / **AIN5** [I2C_SDA]	Not available
PB4 / AIN4 [**I2C_SCL**]	PB4 (**T**) / **I2C_SCL** (True open drain)
PB5 / AIN5 [**I2C_SDA**]	PB5 (**T**) / **I2C_SDA** (True open drain)
PD6 / **UART2_RX**	PD6 (HS) / **UART1_RX**
PD5 / **UART2_TX**	PD5 (HS) / **UART1_TX**
PC1 (HS) / TIM1_CH1 / **UART2_CK**	PC1 (HS) / TIM1_CH1 / **UART1_CK**
PD2 (HS) / **TIM3_CH1** [TIM2_CH3]	Not available
PD0 (HS) / **TIM3_CH2** [TIM1_BKIN][CLK_CCO]	Not available

Table 7. **Migration between STM8S105 and STM8S903 32-pin packages**

STM8S105K	STM8S903K
VDDIO	Connected internally to VDD
VDDA	Connected internally to VDD
VSSA	Connected internally to VSS
Not available	**PA3 (HS) /** TIM5_CH3 [SPI_NSS]
Not available	**PB7**
Not available	**PB6**
PF4 / **AIN12**	PD6 (HS) / **AIN6** / UART1_TX
PB4 / AIN4 [**I2C_SCL**]	PB4 (**T**) / **I2C_SCL** (True open drain)
PB5 / AIN5 [**I2C_SDA**]	PB5 (**T**) / **I2C_SDA** (True open drain)
PD6 / **UART2_RX**	PD6 (HS) / **UART1_RX**
PD5 / **UART2_TX**	PD5 (HS) / **UART1_TX**
PC1 (HS) / TIM1_CH1 / **UART2_CK**	PC1 (HS) / TIM1_CH1 / **UART1_CK**
PD2 (HS) / **TIM3_CH1** [TIM2_CH3]	Not available
PD0 (HS) / **TIM3_CH2** [TIM1_BKIN][CLK_CCO]	Not available
PD4 (HS) / **TIM2_CH1** [BEEP]	PD4 (HS) / BEEP / **TIM5_CH1** / ADC_ETR
PD3 (HS) / **TIM2_CH2** [ADC_ETR]	PD3 (HS) / AIN4 / **TIM5_CH2** [UART1_CK]

Table 8.   Migration between STM8S903 and STM8S103 32-pin packages

STM8S903K	STM8S103K
PD3 (HS) / **AIN4** / TIM5_CH2 / ADC_ETR	Not available
PD4 (HS) / **AIN5** / UART1_TX	Not available
PD6 (HS) / **AIN6** / UART1_RX	Not available
PD4 (HS) / BEEP / **TIM5_CH1** [UART1_CK]	PD4 (HS) / BEEP / **TIM2_CH1**
PD3 (HS) / AIN4 / **TIM5_CH2** / ADC_ETR	PD3 (HS) / **TIM2_CH2** / ADC_ETR

When migrating from one 32-pin device to another one within the Access line family, there are additional differences besides those listed in *Table 6*, *Table 7* and *Table 8*:

● A difference in the number of high-sink capable pins

● Some I/O alternate functions are default alternate functions in one case and remappable options in the other case. Some alternate functions are assigned to different pins. Compare the pinouts in the datasheets for more details.

More information about CAN, UART, I2C, ADC, Timer and power supply system compatibility is given in *Section 3: Block-by-block compatibility analysis*.

3.1.2   Migration to a package with different pin-count within the same sub-family

Change of pin-count leads to a gain or loss of some I/Os and functions. In this case, you may have to find a replacement solution for lost functionality. These cases are highlighted in the following tables. The available replacements by default or remapped alternate functions present on another pin are shown in bold.

Migration within the STM8S208 & 207 sub-families

The STM8S208x sub-family is available in 80-pin and 64-pin packages only. Migration constraints are listed in *Table 9*. They also apply to the STM8S207x sub-family.

Table 9.   STM8S20xx migration between 80-pin and 64-pin packages

STM8S208M, 207M	STM8S208R, 207R
PC0 / ADC_ETR	PD3 / TIM_CH2 **[ADC_ETR]**
PH0	Not available
PH1	Not available
PH2	Not available
PH3	Not available
PH4 / TIM1_ETR	PB3 / AIN3 **[TIM1_ETR]**
PH5 / TIM1_CH3N	PB2 / AIN2 **[TIM1_CH3N]**
PH6 / TIM1_CH2N	PB1 / AIN1 **[TIM1_CH2N]**
PH7 / TIM1_CH1N	PB0 / AIN0 **[TIM1_CH1N]**
PI1	Not available
PI2	Not available
PI3	Not available

Table 9. **STM8S20xx migration between 80-pin and 64-pin packages**

STM8S208M, 207M	STM8S208R, 207R
PI4	Not available
PI5	Not available
PI6	Not available
PI7	Not available

Table 10. **STM8S207x migration between 64-pin and 48-pin packages**

STM8S207R	STM8S207C
PF7 / AIN15	Not available
PF6 / AIN14	Not available
PF5 / AIN13	Not available
PF4 / AIN12	Not available
PF3 / AIN11	Not available
PF0 / AIN10	Not available
VREF+	Not available
VREF-	Not available
PG2	Not available
PG3	Not available
PG4	Not available
PG5	Not available
PG6	Not available
PG7	Not available
PI0	Not available
PE4	Not available

Table 11. **STM8S207x migration between 48-pin and 44-pin packages**

STM8S207C	STM8S207S
PA3 / TIM2_CH3 [TIM3_CH1]	PD2 / TIM3_CH1 **[TIM2_CH3]**
PE7 / AIN8	Not available
PC4 / TIM1_CH4	PD7 / TLI **[TIM1_CH4]**
PE3 / TIM1_BKIN	PD0 / TIM3_CH2 **[TIM1_BKIN** / CLK_CCO]

Table 12. **STM8S207x migration between 44-pin and 32-pin packages**

STM8S207S	STM8S207K
VSSIO_1	Not available
PA4 / UART1_RX	Not available
PA5 / UART1_TX	Not available

Table 12. STM8S207x migration between 44-pin and 32-pin packages (continued)

STM8S207S	STM8S207K
PA6 / UART1_CK	Not available
PB7 / AIN7	Not available
PB6 / AIN6	Not available
PE6 / AIN9	Not available
VSSIO_2	Not available
VDDIO_2	Not available
PE2 / I2C_SDA	PB5 / AIN5 **[I2C_SDA]**[1]
PE1 / I2C_SCL	PB4 / AIN4 **[I2C_SCL]**[1]
PE0 / CLK_CCO	PD0 (HS) / TIM3_CH2 [TIM1_BKIN]**[CLK_CCO]**
PG0	Not available
PG1	Not available
Not available	PF4 / AIN12
PD7 / TLI / **[TIM1_CH4]**	PC4 / TIM1_CH4

1. I2C pins without true open drain capability

Migration within the STM8S105x sub-family

Table 13. STM8105x migration between 48-pin and 44-pin packages

STM8S105C	STM8S105S
PA3 / TIM2_CH3 [TIM3_CH1]	PD2 / TIM3_CH1 **[TIM2_CH3]**
PE7 / AIN8	Not available
PC4 / TIM1_CH4	PD7 / TLI **[TIM1_CH4]**
PE3 / TIM_BKIN	PD0 / TIM3_CH2 **[TIM1_BKIN** / CLK_CCO]

Table 14. STM8S105x migration between 44-pin and 32-pin packages

STM8S105S	STM8S105K
VSSIO_1	Not available
PA4	Not available
PA5	Not available
PA6	Not available
PB7 / AIN7	Not available
PB6 / AIN6	Not available
PE6 / AIN9	Not available
VSSIO_2	Not available
VDDIO_2	Not available
PE2 / I2C_SDA	PB5 / AIN5 **[I2C_SDA]**[1]

Table 14. STM8S105x migration between 44-pin and 32-pin packages

STM8S105S	STM8S105K
PE1 / I2C_SCL	PB4 / AIN4 **[I2C_SCL]**[1]
PE0 / CLK_CCO	PD0 (HS) / TIM3_CH2 [TIM1_BKIN / **CLK_CCO**]
PG0	Not available
PG1	Not available
Not available	PF4 / AIN12
PD7 / TLI / **[TIM1_CH4]**	PC4 / TIM1_CH4

1. I2C pins without true open drain capability

Migration within the STM8S103x sub-family

Table 15. STM8S103x migration between 32-pin and 20-pin packages

STM8S103K	STM8S103F
PF4	Not available
PB6	Not available
PB7	Not available
PB3 / AIN3 / TIM1_ETR	PD2(HS) / **AIN3** [TIM2_CH3][1]
PB2 / AIN2 / TIM1_CH3N	PD6 (HS) / **AIN6** / UART1_RX[1]
PB1 / AIN1 / TIM1-CH2N	PD5 (HS) / **AIN5** / UART1_TX PC4(HS)/AIN2/TIM1_CH4/CLK_CCO **[TIM1_CH2N]**
PB0 / AIN0 / TIM1_CH1N	PD3(HS) / **AIN4** / TIM2_CH2 / ADC_ETR PC3(HS)/TIM1_CH3 [TLI] **[TIM1_CH1N]**
PE5 / SPI_NSS	PA3 (HS) / TIM5_CH3 **[SPI_NSS]**
PC1 (HS) / TIM1_CH1 / UART1_CK	PC6 (HS) / SPI_MOSI **[TIM1_CH1]** PD4 (HS) / BEEP / TIM2_CH1 / **UART1_CK**
PC2 (HS) / TIM1_CH2	PC7 (HS) / SPI_MISO **[TIM1_CH2]**
PD0 (HS) / TIM1_BKIN [CLK_CCO]	PB5 / I2C_SDA/ **[TIM1_BKIN]** PC4 (HS) / AIN2 / TIM1_CH4 / **CLK_CCO** [TIM1_CH2N]
PD7 / TLI [TIM1_CH4]	Not available

1. No replacement for TIM1_ETR and TIM1_CH3N pins

Migration within the STM8S903x sub-family

Migration within this sub-family does not apply because it has only a 32-pin package.

3.1.3 System pins and package pinout

To ensure the fundamental compatibility of all members of the STM8S family, the key system pins are all present and perform the same functions in all packages. This includes the NRST, OSCIN, OSCOUT and PD1/SWIM pins.

Figure 2.　STM8S pinout compatibility guide from 80-pin to 20-pin packages

3.1.4 Digital power supply and package pinout

The digital power supply design includes two supply sources. The purpose is to distribute the current flowing through the I/O logic separately from the rest of the digital microcontroller circuits. Up to two V_{DDIO} / V_{SSIO} pin pairs are used as well as the main V_{DD} / V_{SS} digital supply pair, depending on the pin-count:

● Both V_{DDIO} pairs are present in all larger packages, from the 80-pin package down to the 44 pin package.

● The 32-pin package has only one V_{DDIO} pin for supplying power to the I/Os in the STM8S207x and STM8S105x sub-families.

● The STM8S103x and STM8S903x sub-families have no particular pins dedicated to supplying I/Os. All their I/Os are supplied by the main V_{DD}/V_{SS} pin pair.

The total output current is limited by the number of supply pins. The total output current capability declines for smaller packages, regardless of the number of I/Os with high-sink capability.

The V_{CAP} pin for connecting the external decoupling capacitor for the internal 1.8V regulator is present on all packages.

Table 16. Overview of power supply pins used in all packages

STM8S	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)	LQFP20 (xxxF)
VDD / VSS / VCAP	•	•	•	•	•	•
VDDIO1 / VSSIO1 VDDIO2 / VSSIO2	•	•	•	•	•[(1)]	

1. The 32-pin package has an incomplete I/O supply pair consisting of a single V_{DDIO} pin. This pin is not available for STM8S103x & STM8S903x sub-family devices.

3.1.5 ADC power supply and voltage reference in package pinout

The analog power supply design includes an extra power supply for the analog parts of the microcontroller and an external reference voltage connected via an extra pin pair.

● The V_{DDA}/V_{SSA} analog supply pin pair is present on all larger packages, from the 80-pin package down to the 32-pin package, except in the STM8S103x and STM8S903x sub-families.

● The STM8S103x and STM8S903x sub-families take the analog supply from the main digital supply V_{DD}/V_{SS} pin pair.

● The external ADC voltage reference pair V_{REF+}/V_{REF-} is present in the 80 and 64 pin packages used by the Performance line family only. Without these pins, it is not possible to use the ADC zooming function feature (see *Section 3.4: Analog-to-digital converter* for more details).

● For the rest of the family the ADC reference is taken from the main analog supply V_{DDA}.

Table 17.   Overview of ADC supply and ADC reference pins used in all packages

STM8S	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)	LQFP20 (xxxF)
VDDA / VSSA	●	●	●	●	●(1)	
VREF+ / VREF-	●	●				

1. Not present on STM8S103x and STM8S903x sub-families

3.1.6 Alternate functions and package pinout

The main purpose of the alternate feature concept is to keep the microcontroller configurable for different user and application needs. This is especially important and useful in low pin-count packages.

Default alternate functions can be enabled on dedicated pins by settings in the peripheral registers. A large number alternate functions can be remapped to other pins by programming the option bytes in data EEPROM memory. So many functions that would otherwise be lost by migrating to a smaller package size are preserved by remapping alternate functions to the remaining pins.

The pin layout remapping is controlled by setting the AFRi bits in option byte OPT2. There are differences in the settings between STM8S sub-families. In the STM8S103x sub-family there are even differences in the settings between the pin-counts used. In this sub-family some AFR bits have different meanings for "K" and "F" packages. Refer to the relevant datasheet to check the correct control and all the differences.

3.2 Digital I/O

This section describes the different aspects of compatibility related to digital I/Os:

● GPIO ports

● High-sink capability

● External interrupts

More information related to digital I/O can be found in section *3.3: Timers*.

3.2.1 GPIO

The basic GPIO structure consists of nine ports named from PA to PI with a maximum number of 68 GPIO pins in the 80-pin package (refer to *Table 18*). When migrating to packages with lower pin-count, the number of GPIO pins is reduced in consequence.

STM8S103K and STM8S903K have three additional GPIO pins compared to other sub-families with the same 32-pin package. This is because they have I/Os instead of VDDIO, VDDA and VSSA.

Table 18. Total number of GPIOs in each package

I/O port	Package size						
	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)[1]	LQFP32 (STM8S103 & STM8S903)	LQFP20 (xxxF)
PA	6	6	6	5	2	3	3
PB	8	8	8	8	6	8	2
PC	8	7	7	6	7	7	5
PD	8	8	8	8	8	8	6
PE	8	8	7	5	1	1	
PF	6	6			1	1	
PG	8	8	2	2			
PH	8						
PI	8	1					
Total	68	52	38	34	25	28	16

1. Except STM8S103x and STM8S903x sub-families

3.2.2 High-sink capability

Most of the I/Os with high sink capability are in Ports C and D. The Access line family (STM8S10xx) has a greater number of high sink pins, which are also spread out in the other ports. See *Table 19*.

Table 19. **Total number of high sink I/Os in each package**

Product family	Package size						
	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)[1]	LQFP32 (STM8S103 & STM8S903)	LQFP20 (xxxF)
STM8S20xx	18	16	16	15	12		
STM8S10xx			16	15	12	21	12

1. Except STM8S103x and STM8S903x sub-families

3.2.3 External interrupts

In general only five ports (PA to PE) have external interrupts capability. However in the STM8S903x sub-family external interrupt capability with a dedicated interrupt vector for port PF is added.

Table 20. **Total number of external interrupt pins in each package**

LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)[1]	LQFP32 (STM8S103 & STM8S903)	LQFP20 (xxxF)
37	36	36	31	23	27/26[2]	16

1. Except STM8S103x and STM8S903x sub-families

2. PF4 interrupt is available at STM8S903x sub-family only

3.3 Timers

All STM8S Performance Line and Access Line sub-families are equipped with the following timers:

● TIM1 advanced control timer: 16-bit up/down auto reload counter with 16-bit prescaler, wide range of modes, 4x16-bit CAPCOM channels, 3 of them have a complementary output)

● TIM2 general purpose timer (3x16-bit CAPCOM channels)

● TIM3 general purpose timers (2x16-bit CAPCOM channels)

● TIM4 basic timer: (1x8bit, no CAPCOM channel, no output)

This means a total of up to 9x16-bit CAPCOM channels, 9 inputs/outputs and 3 complementary outputs.

TIM1 is an up/down counter, the others are up counters only. Timer pins, mainly from TIM1, can be remapped to other pins. You have to check the options in the datasheet pinout description and program the option byte settings accordingly.

TIM1 can be triggered externally by the ETR pin or by its TI1 and TI2 inputs or receive an external break signal from the BKIN pin. The ETR, BKIN and all of TIM1 pins are present on all packages except in STM8S103x 20-pin devices which lack the ETR and CH3N signals.

In the STM8S903x sub-family, TIM1 can also be synchronized internally with TIM5 and TIM6. The TIM5 and TIM6 are enhanced timers which are present only in the STM8S903x sub-family only. They have an added synchronization circuit which lets you control them with external signals and interconnect several timers.

Table 21. Total number of timer channels (direct I/Os + complementary outputs) in each package

Sub-family	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)	LQFP20 (xxxF)
STM8S208x	9 (9+3)	9 (9+3)				
STM8S207x	9 (9+3)	9 (9+3)	9 (9+3)	7 (7+3)	8 (8+3)	
STM8S105x			9 (9+3)	7 (7+3)	8 (8+3)	
STM8S103x					7 (7+3)	7 (7+2)
STM8S903x					7 (7+3)	

3.4 Analog-to-digital converter

All STM8S sub-families use the same 10-bit analog-to-digital successive approximation conversion unit. Most of the ADC functions are the same but there are some differences between sub-families.

3.4.1 ADC inputs

The number of ADC inputs depends on the sub-family and package size.

Analog input channels are in continuous sequence, except in the STM8S105x subfamily where:

● AIN8 is missing In the 44-pin package (AIN9 is used instead).

– AIN9 can be converted in scan mode if the AIN8 converted value is discarded.

● AIN12 is present in the 32-pin package instead of AIN6.

– AIN12 cannot be used as part of a conversion channel sequence in scan continuous mode and cannot be used in analog watchdog mode.

Table 22.   Total number of analog inputs in each package

Sub-family	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)	LQFP20 (xxxF)
STM8S208x	16	16				
STM8S207x	16	16	10	9	7	
STM8S105x			10	9	7	
STM8S103x					4	5
STM8S903x					7+1[1]	

1. Reference voltage can be measured on AIN7

3.4.2 ADC supply and reference pins

All migration impacts related to the ADC supply and reference pins depend on the available pins in the actual package and are fully described in *Section 3.1.5: ADC power supply and voltage reference in package pinout*.

3.4.3 ADC modes

Table 23 gives a selected list of ADC modes showing only those where there are differences between STM8S sub-families.

The differences are mainly related to analog zooming, continuous conversion buffering, scanning capability and analog watchdog.

Table 23. Overview of ADC mode differences

ADC Mode	STM8S207x, 208x	STM8S105x	STM8S103x
	ADC2	ADC1	
Analog zooming	YES[1]	NO	NO
Conversion modes	– Single – Continuous	– Single – Continuous – Continuous buffered (10 sample buffers) – Single scan – Continuous scan	– Single – Continuous – Continuous buffered (8 sample buffers) – Single scan – Continuous scan
Analog watchdog	NO	YES	YES
Interrupts	– EOC	– EOC – analog watchdog	– EOC – analog watchdog

1. For devices with V_{REF+}/V_{REF-} pin pair only (80-pin and 64-pin packages)

3.5 Communication peripherals

3.5.1 SPI

This peripheral is present in all STM8S sub-families. The only difference is the maximum communication speed:

- 8 Mbit/s ($f_{MASTER}/2$) in Access line
- 10 Mbit/s in Performance line.

3.5.2 I2C

This peripheral is present in all STM8S sub-families. If true open drain lines are required, you have to take this into account when selecting the I/O pins to use for I2C. In the default mapping, the SDA & SCL alternate functions are generally mapped to pins with true open drain capability. This is not the case when the SDA & SCL function are remapped to other pins.

I/Os with true open drain capability are available for I2C in all STM8S with one important exception mentioned in the note below.

Note: *STM8S105x 32-pin devices do not have true open drain I/Os available for I2C. The I/Os where the I2C functions can be mapped are configurable as pseudo open drain only.*

3.5.3 CAN

The CAN peripheral present only in the STM8S208x sub-family. When migrating within this sub-family there are no compatibility concerns for this block.

3.5.4 UART

UART1, UART2 and UART3 are three different UART types used in the STM8S sub-families. All the UARTs include common basic functions, but differ in the special features they provide.

UART1 is present in the STM8S208x, STM8S207x and STM8S103x sub-families and it offers the complete set of all UART features except LIN slave mode.

The LIN slave mode feature is present in UART2 and UART3. As the STM8S Performance line devices (except the 32-pin device) include both UART1 and UART3 they are able to cover all UART features.

UART2 is present in the STM8S105x sub-family only and it covers all features except single wire half duplex mode.

Refer to the STM8S family reference manual (RM0016) and STM8S datasheets for more detailed information.

Table 24. UART special features

Feature	STM8S207x, 208x		STM8S105x	STM8S103x
	UART1[1]	UART3	UART2	UART1
Synchronous communication	●		●	●
Smart card mode	●		●	●
IrDA mode	●		●	●
Single wire half duplex mode	●			●
LIN slave mode		●	●	

1. Not present in STM8S207K (32-pin device)

3.6 Clock controller

The clock controller is broadly compatible across the whole STM8S family range. There are some small differences which concern the maximum frequency of the high speed external clock (HSE clock) and the calibration and trimming of the high speed internal clock frequency (HSI clock).

3.6.1 HSE clock frequency

Depending on the STM8S family, there is a difference in the maximum speed of the HSE external oscillator clock.

● In STM8S Performance line, the HSE clock can be used at up to 24 MHz.

● In STM8S Access line, the HSE clock is limited to 16 MHz.

If the core runs at a frequency higher than 16 MHz one wait state must be inserted for reading the Flash/EEPROM memory. This is configured by an option byte setting.

The stabilization delay for the HSE oscillator can be configured by the Option byte setting. The Performance line family supports double the delay duration of the Access line family.

3.6.2 HSI clock frequency

In all STM8S sub-families, the HSI internal oscillator is factory calibrated in intervals of +/-2% of the range 5/25°C. This value can be trimmed by the user within an interval of +3/-4% of the range in eight steps using 3 trimming register bits. This permits calibration in steps of about 1% of the range.

In addition, in access line products only, it is optionally possible to trim the HSI in the same interval but in 16 steps using 4 calibration bits. This allows you to trim the frequency more finely, in steps of about 0.5% of the range.

3.7 Memory

3.7.1 Flash program memory

The Flash program memory organization differs slightly in each sub-family. There are three different Flash densities:

● High density in the STM8S208x and STM8S207x sub-families

● Medium density in the STM8S105x subfamily

● Low density in the STM8S103x and STM8S903x sub-families

The memory is organized in pages:

● High density and medium density Flash memory are organized in up to 256 pages of 512 bytes each. Each page is divided into 4 blocks of 128 bytes each. A block is the maximum amount of memory that can be programmed in a single programming cycle.

● Low density Flash memory is organized in up to 128 pages of 64 bytes. A page consists of a single block of 64 bytes.

The page size defines the granularity of the User Boot Code area. Refer to the STM8S datasheets for more details.

Table 25.   Flash program memory size in bytes for each package/sub-family

Sub-family	Memory density	LQFP80 (xxxM)	LQFP64 (xxxR)	LQFP48 (xxxC)	LQFP44 (xxxS)	LQFP32 (xxxK)	LQFP20 (xxxF)
STM8S208x	High	128K	128K				
STM8S207x	High	128K	128K 64K 32K	128K 64K	64K	32K	
STM8S105x	Medium			32K 16K	32K 16K	32K 16K	
STM8S103x	Low					8K	8K 4K
STM8S903x	Low					8K	

Table 26.   Flash program memory granularity in each sub-family

Sub-family	Number of pages	Page size [bytes]	Blocks per page	Block size [bytes]
STM8S20xx	up to 256	512	4	128
STM8S105x	up to 64	512	4	128
STM8S103x	up to 128	64	1	64
STM8S903x	up to 128	64	1	64

3.7.2   EEPROM data memory

The data EEPROM memory organization differs slightly in each sub-family. There are three different data EPROM densities:

● High density in the STM8S208x and STM8S207x sub-families

● Medium density in the STM8S105x subfamily

● Low density in the STM8S103x and STM8S903x sub-families

The data EEPROM is organized in pages:

● High density and medium density data EEPROM are organized in up to 4 pages of 512 bytes each. Each page is divided into 4 blocks of 128 bytes each. A block is the maximum amount of memory that can be programmed in a single programming cycle.

● Low density data EEPROM is organized in up to 10 pages of 64 bytes. A page consists of a single block of 64 bytes.

The start address of data EEPROM is always 0x4000. Refer to the STM8S datasheets for more details.

Table 27.   Data EEPROM memory size in bytes for each sub-family/Flash size

Sub-family	Flash Program memory size (bytes)					
	128K	**64K**	**32K**	**16K**	**8K**	**4K**
STM8S208x	2048					
STM8S207x	2048	1536	1024			
STM8S105x			1024	1024		
STM8S103x					640[(1)]	640[(1)]
STM8S903x					640[(1)]	

1. No read-while-write (RWW) capability

Table 28.   Data EEPROM memory granularity in each sub-family

Sub-family	Number of pages	Page size [bytes]	Blocks per page	Block size [bytes]
STM8S20xx	up to 4	512	4	128
STM8S105x	up to 2	512	4	128
STM8S103x	10	64	1	64
STM8S903x	10	64	1	64

3.7.3   BootROM memory

The BootROM memory, containing the bootloader code, is present in the STM8S20xx and STM8S105x sub-families. It is not present in the STM8S103x sub-family. The BootROM size is 2KB and its start address is always 0x6000.

3.7.4   RAM memory

The RAM memory always starts from address 0. The first 256 bytes make up the zero page.

Table 29.   RAM memory size (bytes) for each sub-family/Flash size

Sub-family	Flash Program memory size (bytes)					
	128K	**64K**	**32K**	**16K**	**8K**	**4K**
STM8S208x	6K					
STM8S207x	6K	4K	2K			
STM8S105x			2K	2K		
STM8S103x					1K	1K
STM8S903x					1K	

3.7.5   Stack

The space for the stack is always located at the end of the SRAM memory. So its position in the address space varies depending on the SRAM memory size. The stack pointer value is initialized to the upper address at reset and it is decremented each time a byte is pushed in. The stack size is 1024 bytes in Performance line devices and 512 bytes in other STM8S

devices. So both the stack pointer initialization value and the stack length is product dependent.

3.7.6 GPIO and peripheral registers

The space for the GPIO and peripheral registers is mapped in the memory area between addresses 0x5000 and 0x57FF. The register block start addresses for each peripheral are the same across in all sub-families. The names of the registers are the same but their position in the register structure differs slightly in some sub-families. That's why you can use the same drivers by referring to the register names, but you must be careful to include the correct library map file into your project and replace this file by the proper one if you are migrating to another family member.

3.7.7 Interrupt mapping

The interrupt vector mapping is compatible for all the sub-families except STM8S103x and STM8S903x. These sub-families have an added vector for the external interrupt from the GPIO PF4 pin. The PF4 pin is present only in the 32-pin device. This vector is mapped in the same location as the CAN Rx interrupt which is not used in this sub-family. TIM5 and TIM2 share the same interrupt vector, as do TIM6 and TIM4, UART2 and UART3, ADC1 and ADC2. Refer to *Table 30*.

Table 30. Interrupt vector table differences

Priority	Source block	Interrupt vector address	STM8S208x STM8S207x	STM8S105x	STM8S103x	STM8S903x
8	CAN	0x8028	CAN Rx interrupts	Reserved	Reserved	Port F external interrupts
9	CAN	0x802C	CAN TX/ER/SC interrupts	Reserved	Reserved	Reserved
13	TIM2/TIM5	0x803C	TIM2 Update/Overflow	TIM2 Update/Overflow	TIM2 Update/Overflow	TIM5 Update/Overflow/ Trigger
14	TIM2/TIM5	0x8040	TIM2 Capture/Compare	TIM2 Capture/Compare	TIM2 Update/Overflow	TIM5 Capture/Compare
15	TIM3	0x8044	TIM3 Update/Overflow	TIM3 Update/Overflow	Reserved	Reserved
16	TIM3	0x8048	TIM3 Capture/Compare	TIM3 Capture/Compare	Reserved	Reserved
17	UART1	0x804C	UART1 Transmit interrupts	Reserved	UART1 Transmit interrupts	UART1 Transmit interrupts
18	UART1	0x8050	UART1 Receive Interrupts	Reserved	UART1 Receive Interrupts	UART1 Receive Interrupts
20	UART2/ UART3	0x8058	UART3 Transmit interrupts	UART2 Transmit interrupts	Reserved	Reserved
21	UART2/ UART3	0x805C	UART3 Receive Interrupts	UART2 Receive Interrupts	Reserved	Reserved

Table 30.   Interrupt vector table differences (continued)

Priority	Source block	Interrupt vector address	STM8S208x STM8S207x	STM8S105x	STM8S103x	STM8S903x
22	ADC1/ADC2	0x8060	ADC2 End of conversion interrupt	ADC1 End of conversion/Analog watchdog interrupts	ADC1 End of conversion/Analog watchdog interrupts	ADC1 End of conversion/Analog watchdog interrupts
23	TIM4/TIM6	0x8064	TIM4 Update/Overflow	TIM4 Update/Overflow	TIM4 Update/Overflow	TIM6 Update/Overflow/Trigger

3.7.8   Option bytes

As the block of option bytes is placed in the last page of EEPROM data memory its position varies in address space.

The basic structure of the option byte area is compatible across the family. There are some differences in the actual settings and option bit meanings between sub-families.

The first difference is in the OPT1 option bits setting which controls the User Boot Code (UBC) protected area. The settings differ due to the different page sizes in each sub-family which are described in *Section 3.7.1: Flash program memory on page 30*. Some settings are reserved depending on the size the FLASH program memory and in some cases the same code can correspond to a different number of pages in some sub-families.

The next difference is in the OPT2 option bits settings which enable the alternate option functions for the GPIOs. The option bits of this register have the same meaning for the STM8S208x, 207x and 105x sub-families, but they differ for the STM8S103x sub-family and differ again for the STM8S903x sub-family. For STM8S103x these bits are divided into two groups. Bits 6,5,1 and 0 are for the STM8S103K (32-pin device) and bits 7,5,4 and 3 are for STM8S103F (20-pin device).

In the OPT3 option, the HSITRIM bit is present in Access line but not in Performance line devices. This bit controls the number of calibration steps when the HSI clock frequency is trimmed (see *Section 3.6.2: HSI clock frequency*).

The OPT5 register settings differ between Access and Performance line. Optional HSE oscillator stabilization time has two times higher numbers of clock periods for Performance line.

The OPT7 register (FLASH memory access wait states) settings is used only in the STM8S Performance line family.

The OPTBL optional switching the reset vector to the boot loader area is not available for the 103x sub-family where any boot loader area memory is not present.

4 Revision history

Table 31.   Document revision history

Date	Revision	Changes
06-Mar-2009	1	Initial release

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