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**Information Technology -  
AT Attachment  
with Packet Interface - 5  
(ATA/ATAPI-5)**

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- D97150R2 Power-up in Standby as amended at the 8/18/98 plenary.
- D98101R2 State diagram proposal as amended at the 8/18/98 plenary.
- D98102R2 Set multiple proposal as requested at the 4/14-16/98 plenary.
- D98104R0 Master password revision as requested at the 6/16-18/98 plenary.
- D98105R2 Clarification of nIEN and pending interrupt as amended at the 8/18/98 plenary.
- D98111R0 Editorial changes requested at the 4/14-16/98 plenary.
- D98112R2 New identify word as requested at the 8/18/98 plenary.
- D98121R0 Proposed ATA/ATAPI-4 amendment as requested at the 8/18/98 plenary.
- D98122R0 Cable, mechanical, and connector proposal as amended at the 8/18/98 plenary.
- Replaced "should" with "shall" in 6.8.2 and removed parenthetical phrase per 8/18/98 plenary.
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- D99101R0 Cache flush mandatory proposal
- D99105R0 Self-test log modification
- D99107R0 Checksum definition
- D99108R0 Optional pointer on self-test log

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- D98133R4 Ultra DMA 66 timing
- D98144R2 CFA SET FEATURES codes
- D99104R1 Error log depth extension
- D99112R1 Multiword DMA description

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American National Standard  
for Information Systems —

**AT Attachment  
with Packet Interface - 5 — (ATA/ATAPI-5)**

Secretariat  
**Information Technology Industry Council**

Approved mm dd yy

**American National Standards Institute, Inc.**

**Abstract**

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices. It includes the Packet Command feature set implemented by devices commonly known as ATAPI devices.

This standard maintains a high degree of compatibility with the AT Attachment Interface with Packet Interface Extensions (ATA/ATAPI-4), NCITS 317-1998, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

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## Foreword

(This foreward is not part of American National Standard X3.\*\*\*-199\*.)

This AT Attachment with Packet Interface -5 (ATA/ATAPI-5) standard is designed to maintain a high degree of compatibility with the AT Attachment with Packet Interface (ATA/ATAPI-4) standard.

This standard was developed by the ATA ad hoc working group of Accredited Standards Committee NCITS during 1998-99. The standards approval process started in 199n. This document includes annexes that are informative and are not considered part of the standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the NCITS Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, NCITS. Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, the NCITS Committee had the following members:

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Subcommittee T13 on ATA Interfaces, that reviewed this standard, had the following members:

- Gene Milligan, Chairman
- Pete McLean, Vice-Chairman
- Dan Colegrove, Secretary

ATA/ATAPI ad hoc Working Group, that developed this standard, had the following additional participants:

## **Introduction**

This standard encompasses the following:

Clause 1 describes the scope.

Clause 2 provides normative references.

Clause 3 provides definitions, abbreviations, and conventions used within this document.

Clause 4 contains the electrical and mechanical characteristics; covering the interface cabling requirements of the interface and DC cables and connectors.

Clause 5 contains the signal descriptions of the AT Attachment Interface.

Clause 6 describes the general operating requirements of the AT Attachment Interface.

Clause 7 contains descriptions of the registers of the AT Attachment Interface.

Clause 8 contains descriptions of the commands of the AT Attachment Interface.

Clause 9 contains the protocol of the AT Attachment Interface.

Clause 10 contains the interface timing diagrams.

American National Standard  
for Information Systems —

**Information Technology—  
AT Attachment with Packet Interface ~~–5~~ (ATA/ATAPI-5)**

## **1 Scope**

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

The application environment for the AT Attachment Interface is any host system that has storage devices contained within the processor enclosure.

This standard defines the connectors and cables for physical interconnection between host and storage device, as well as, the electrical and logical characteristics of the interconnecting signals. It also defines the operational registers within the storage device, and the commands and protocols for the operation of the storage device.

This standard maintains a high degree of compatibility with the AT Attachment with Packet Interface Extensions standard (ATA/ATAPI-4), NCITS 317-1998, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

## **2 Normative references**

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents can be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax) or via the World Wide Web at <http://www.ansi.org>.

Additional availability contact information is provided below as needed.

### **2.1 Approved references**

The following approved ANSI standards, approved international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), may be obtained from the international and regional organizations who control them.

SCSI-3 Primary Commands (SPC) [NCITS 301:1997] (PACKET command feature set device types)  
SCSI-3 Multimedia Commands (MMC) [NCITS 304:1997] (PACKET command feature set sense codes)

To obtain copies of these documents, contact Global Engineering or NCITS.

## 2.2 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

SCSI Primary Commands - 2 (SPI-2) [T10/1236-D]  
Multimedia Commands - 2 (MMC-2) [T10/1228-D] (PACKET command feature set commands)

For more information on the current status of the above documents, contact NCITS. To obtain copies of these documents, contact Global Engineering or NCITS.

## 2.3 Other references

The following standard and specifications were also referenced.

PC Card Standard , February 1995, PCMCIA (68-pin Connector)

For the PC Card Standard published by the Personal Computer Memory Card International Association, contact PCMCIA at 408-433-2273.

## 3 Definitions, abbreviations, and conventions

### 3.1 Definitions and abbreviations

For the purposes of this standard, the following definitions apply:

**3.1.1 ATA (AT Attachment):** ATA defines the physical, electrical, transport, and command protocols for the internal attachment of storage devices.

**3.1.2 ATA-1 device:** A device that complies with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives. ANSI X3.221-1994 has been withdrawn.

**3.1.3 ATA-2 device:** A device that complies with ANSI X3.279-1996, the AT Attachment Interface with Extensions.

**3.1.4 ATA-3 device:** A device that complies with ANSI X3.298-1997, the AT Attachment-3 Interface.

**3.1.5 ATA/ATAPI-4 device:** A device that complies with ANSI NCITS 317-1998, AT Attachment Interface with Packet Interface Extensions.

**3.1.6 ATA/ATAPI-5 device:** A device that complies with this standard.

**3.1.7 ATAPI (AT Attachment Packet Interface) device:** A device implementing the Packet Command feature set.

**3.1.8 bus release:** For devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed to allow the host to select the other device.



- 3.1.9 byte count:** The value placed in the Byte Count register by the device to indicate the number of bytes to be transferred under this DRQ assertion when executing a PACKET command.
- 3.1.10 byte count limit:** The value placed in the Byte Count register by the host as input to a PACKET command to indicate the maximum byte count that may be transferred under a single DRQ assertion.
- 3.1.11 CFA:** The CompactFlash Association that created the specification for compact flash memory that uses the ATA interface.
- 3.1.12 check condition:** For devices implementing the PACKET Command feature set, this indicates an exception condition has occurred that needs to be reported to the host.
- 3.1.13 CHS (cylinder-head-sector):** This term defines the addressing of the device as being by cylinder number, head number, and sector number.
- 3.1.14 command aborted:** Command completion with ABRT set to one in the Error register and ERR set to one in the Status register.
- 3.1.15 command acceptance:** A command is considered accepted whenever the currently selected device has the BSY bit equal to zero in the Status register and the host writes to the Command register. An exception exists for the EXECUTE DEVICE DIAGNOSTIC (see 8.9) and DEVICE RESET command (see 8.7).
- 3.1.16 Command Block registers:** Interface registers used for delivering commands to the device or posting status from the device.
- 3.1.17 command completion:** Command completion is the completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the Error register, the placing of the appropriate status bits in the Status register, the clearing of both BSY and DRQ to zero, and the asserting of INTRQ if nIEN is cleared to zero and the command protocol specifies that INTRQ be asserted.
- 3.1.18 command packet:** A command packet is a data structure transmitted to the device by a PACKET command that includes the command and command parameters.
- 3.1.19 Control Block registers:** Interface registers used for device control and to post alternate status.
- 3.1.20 CRC:** Cyclical Redundancy Check used for the Ultra DMA protocol to check the validity of each Ultra DMA burst transferred.
- 3.1.21 data block:** This term describes a unit of data words transferred using PIO data transfer. A data block is transferred between the host and the device as a complete unit. A data block is a sector, except for data blocks of a READ MULTIPLE and WRITE MULTIPLE commands. In the cases of READ MULTIPLE and WRITE MULTIPLE commands, the size of the data block may be changed in multiples of sectors by the SET MULTIPLE MODE command.
- 3.1.22 device:** Device is a storage peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.
- 3.1.23 device selection:** A device is selected when the DEV bit of the Device/Head register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal.
- 3.1.24 DMA (direct memory access):** A means of data transfer between device and host memory without host processor intervention.

- 3.1.25 don't care:** A term to indicate that a value is irrelevant.
- 3.1.26 interrupt pending:** Interrupt pending is an internal state of a device that exists when the device has need to notify the host of an event.
- 3.1.27 LBA (logical block address):** This term defines the addressing of the device as being by the linear mapping of sectors.
- 3.1.28 master:** In ATA-1, Device 0 has also been referred to as the master. Throughout this document the term Device 0 is used.
- 3.1.29 native max address:** The highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command. The capacity defined by native max address may be different in CHS and LBA translations.
- 3.1.30 overlap:** Overlap is a protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device on the bus.
- 3.1.31 packet delivered command:** A command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters.
- 3.1.32 PIO (programmed input/output):** A means of accessing device registers. PIO is also used to describe one form of data transfers. PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.
- 3.1.33 queued:** Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred but command completion has not occurred.
- 3.1.34 register delivered command:** A command that is delivered to the device by placing the command and all of the parameters for the command in the device Command Block registers.
- 3.1.35 released:** Indicates that a signal is not being driven. For tri-state drivers, this means that the driver is in the high impedance state. For open-collector drivers, the driver is not asserted.
- 3.1.36 sector:** A uniquely addressable set of 256 words (512 bytes).
- 3.1.37 signature:** A unique set of values placed in the Command Block registers by the device to allow the host to distinguish between register delivered command devices and packet delivered command devices.
- 3.1.38 slave:** In ATA-1, Device 1 has also been referred to as the slave. Throughout this document the term Device 1 is used.
- 3.1.39 SMART:** Self-Monitoring, Analysis, and Reporting Technology for prediction of device degradation and/or faults. Throughout this document this is noted as SMART.
- 3.1.40 Ultra DMA burst:** An Ultra DMA burst is defined as the period from an assertion of DMACK- to the subsequent negation of DMACK- when Ultra DMA has been enabled by the host.
- 3.1.41 unit attention condition:** A state that a device implementing the PACKET Command feature set maintains while the device has asynchronous status information to report to the host.
- 3.1.42 unrecoverable error:** An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one in the Status register at command completion.

**3.1.43 VS (vendor specific):** This term is used to describe bits, bytes, fields, and code values that are reserved for vendor specific purposes. These bits, bytes, fields, and code values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE – Industry practice could result in conversion of a Vendor Specific bit, byte, field, or code value into a defined standard value in a future standard.

## 3.2 Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (see 3.2.6 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., Cylinder Low register).

### 3.2.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, then text.

### 3.2.2 Lists

Ordered lists, those lists describing a sequence, are of the form:

- a)
- b)
  - 1)
  - 2)
- c)

Unordered list are of the form:

- 1)
- 2)
  - a)
  - b)
- 3)

### 3.2.3 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

**3.2.2.1 expected:** A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

**3.2.2.2 mandatory:** A keyword indicating items to be implemented as defined by this standard.

**3.2.2.3 may:** A keyword that indicates flexibility of choice with no implied preference.

**3.2.2.4 obsolete:** A keyword used to describe bits, bytes, fields, and code values that no longer have consistent meaning or functionality from one implementation to another. However, some degree of functionality may be required for items designated as "obsolete" to provide for backward

compatibility. An obsolete bit, byte, field, or command shall never be reclaimed for any other use in any future standard.

Obsolete commands should not be used by the host. Commands defined as obsolete in previous standards may be command aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

**3.2.2.5 optional:** A keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

**3.2.2.6 retired:** A keyword indicating that the designated bits, bytes, fields, and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, fields, or code values are utilized before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

**3.2.2.7 reserved:** A keyword indicating reserved bits, bytes, words, fields, and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be set to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

**3.2.2.8 shall:** A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other standard conformant products.

**3.2.2.9 should:** A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase "it is recommended".

### 3.2.4 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

### 3.2.5 Signal conventions

Signal names are shown in all uppercase letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates the signal is a low active signal. A low active signal is true when the signal is below  $V_{iL}$ , and is false when the signal is above  $V_{iH}$ . No dash at the end of a signal name indicates the signal is a high active signal. A high active signal is true when the signal is above  $V_{iH}$ , and is false when the signal is below  $V_{iL}$ .

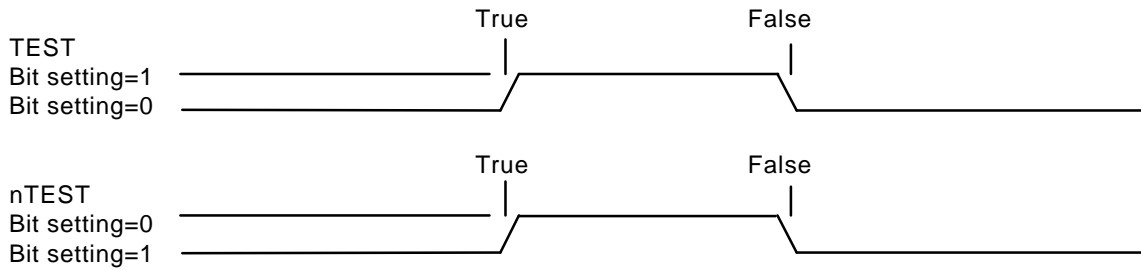
Asserted means that the signal is driven by an active circuit to the true state. Negated means that the signal is driven by an active circuit to the false state. Released means that the signal is not actively driven to any state (see 4.2.1). Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal.

Control signals that may be used for more than one mutually exclusive functions are identified with their function names separated by a colon (e.g., DIOW-:STOP).

### 3.2.6 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true, and when BIT is cleared to zero the

meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero the meaning of the bit is true and when nBIT is set to one the meaning of the bit is false.



### 3.2.7 State diagram conventions

State diagrams shall be as shown in Figure 1.

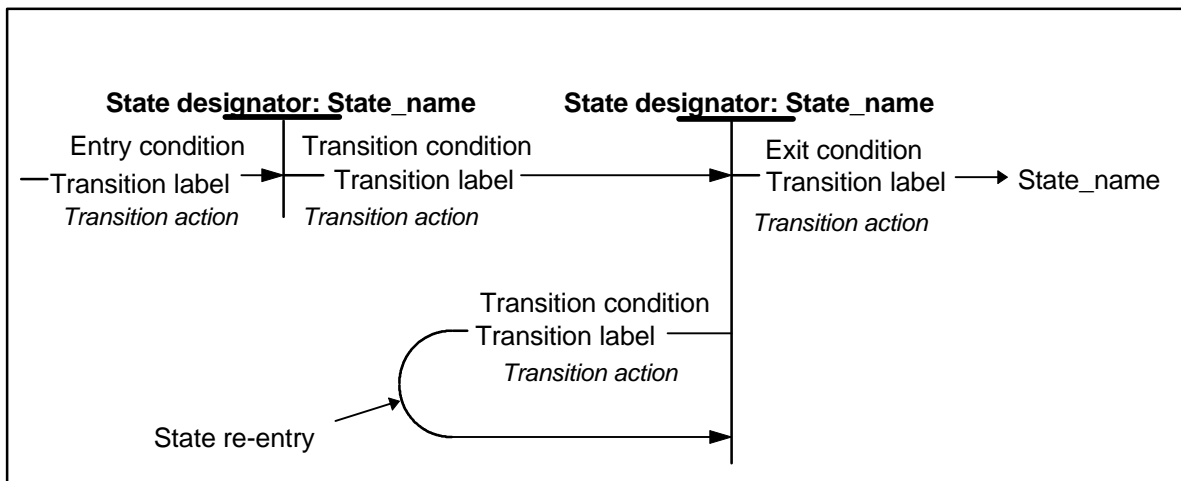


Figure 1 – State diagram convention

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized in the title of the figure containing the state diagram followed by a unique number. The state name is a brief description of the primary action taken during the state, and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

In device state diagrams, the state of bits and signals that change state during the execution of this state diagram are shown under the state designator:state\_label, and a table is included that show the state of all bits and signals throughout the state diagram as shown below.

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	v	v	v	v	v	v	v	v

where the value indicates:

- v = bit value changes.
- 1 = bit set to one.
- 0 = bit cleared to zero.
- x = bit is don't care.
- V = signal changes.
- A = signal is asserted.
- N = signal is negated.

R = signal is released.  
 X = signal is don't care.

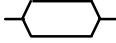

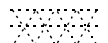
Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made followed by the state designator of the state to which the transition is being made. In some cases, the transition to enter or exit a state diagram may come from or go to a number of state diagrams, depending on the command being executed. In this case, the state designator is labeled xx. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action, indicated in italics, that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

It is assumed that all actions defined in a state are executed within the state and that transitions from state to state are instantaneous.

### 3.2.8 Timing conventions

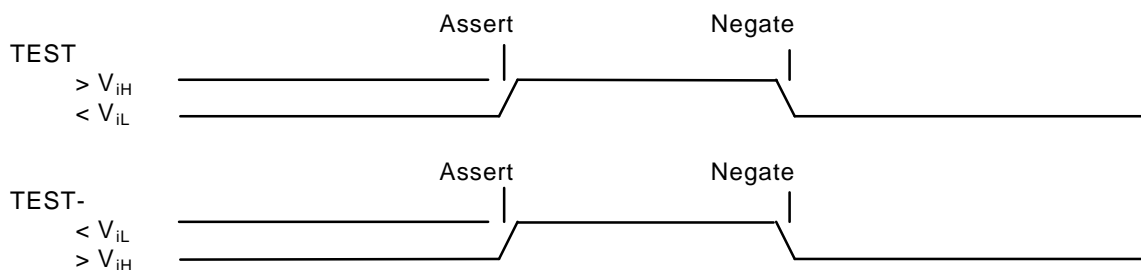
Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.

- $/$  or  $\backslash$  - signal transition (asserted or negated)
- $\langle$  or  $\rangle$  - data transition (asserted or negated)
-  - data valid
-  - undefined but not necessarily released
-  - asserted, negated or released
- ..... - released
- - the "other" condition if a signal is shown with no change

All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



### 3.2.9 Byte ordering for data transfers

Assuming a block of data contains "n" bytes of information, the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block, and Byte(n-1) is the last byte of the block. Table 1 shows the order the bytes shall be presented in when such a block of data is transferred on the interface (see 8.12.8 and 8.13.8).

**Table 1 – Byte order**

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (n-1)								Byte (n-2)							

NOTE – The above description is for data on the interface. Host systems and/or host adapters may cause the order of data, as seen in the memory of the host, to be different.

## 4 Interface physical and electrical requirements

Connectors [and cables](#) are documented in annex A.

### 4.1 Cable configuration

This standard defines an interface containing a single host or host adapter and one or two devices. One device is configured as Device 0 and the other device as Device 1.

The designation of a device as Device 0 or Device 1 may be made in a number of ways including but not limited to:

- a switch or a jumper on the device;
- use of the Cable Select (CSEL) pin.

The host shall be placed at one end of the cable. [It is recommended that for a single device configuration the device be placed at the end of the cable. If a single device configuration is implemented with the device in the middle, a cable stub results that may cause degradation of signals. Single device configurations with the device in the middle of the cable shall not be used with Ultra DMA modes using 80-conductor cable assemblies.](#)

### 4.2 Electrical characteristics

Table 2 defines the DC characteristics of the interface signals. Table 3 defines the AC characteristics.

**Table 2 – DC characteristics**

Description		Min	Max
$I_{OL}$	Driver sink current (see note 1)	4 mA	
$I_{OLDASP}$	Driver sink current for DASP (see note 1)	12 mA	
$I_{OH}$	Driver source current (see note 2)	400 $\mu$ A	
$I_{OHDMARQ}$	Driver source current for DMARQ (see note 2)	xx $\mu$ A	
$I_Z$	Device pull up current on DD (15:0) and STROBE when high Z	-10 $\mu$ A	200 $\mu$ A
$V_{IH}$	Voltage input high	2.0 VDC	
$V_{IL}$	Voltage input low		0.8 VDC
$V_{OH}$	Voltage output high at $I_{OH}$ min	2.4 VDC	
$V_{OL}$	Voltage output low at $I_{OL}$ min		0.5 VDC
<p><b>NOTES –</b></p> <p>1 <math>I_{OLDASP}</math> shall be 12 mA minimum to meet legacy timing and signal integrity.</p> <p>2 <math>I_{OH}</math> value at 400 <math>\mu</math>A is insufficient in the case of DMARQ that is pulled low by a 5.6 k<math>\Omega</math> resistor.</p>			

**Table 3 – AC characteristics**

Description		Min	Max
$S_{RISE}$	Rising edge slew rate for any signal on AT interface (see note)		1.25 V/ns
$S_{FALL}$	Falling edge slew rate for any signal on AT interface (see note)		1.25 V/ns
$C_{host}$	Host I/O capacitance		25 pf
$C_{device}$	Device I/O capacitance		20 pf
<p><b>NOTE –</b> <math>S_{RISE}</math> and <math>S_{FALL}</math> shall meet this requirement when measured at the sender's connector from 10-90% of full signal amplitude with all capacitive loads from 15 pf through 40 pf where all signals have the same capacitive load value.</p>			



#### 4.2.1 Driver types and required termination

**Table 4 – Driver types and required termination**

Signal	Source	Driver type (see note 1)	Host (see note 2)	Device (see note 2)	Notes
RESET-	Host	TP			
DD (15:0)	Bidir	TS			3
DMARQ	Device	TS	5.6 kΩ PD		
DIOR-:HDMARDY- :HSTROBE	Host	TS			
DIOW-:STOP	Host	TS			
IORDY:DDMARDY- :DSTROBE	Device	TS	1.0 kΩ PU		6,10
CSEL	Host		Ground	10 kΩ PU	4, 6
DMACK-	Host	TP			
INTRQ	Device	TS	10 kΩ		5
DA (2:0)	Host	TP			
PDIAG-:CBLID-	Device	TS		10 kΩ PU	2,6,7,8
CS0- CS1-	Host	TP			
DASP-	Device	OC		10 kΩ PU	6,9

**NOTES –**

1 TS=Tri-state; OC=Open Collector; TP=Totem-pole; PU=Pull-up; PD=Pull-down.

2 All resistor values are the minimum (lowest allowed) except for the 10K Ω PU on PDIAG-:CBLID- which shall have a tolerance of ±5% or less.

3 Devices shall not have a pull-up resistor on DD7. The host shall have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up so that a host shall detect BSY as being cleared when attempting to read the Status register of a device that is not present.

4 When used as CSEL, this line is grounded at the Host and a 10 kΩ pull-up is required at both devices.

5 A 10 kΩ pull-down or pull-up, depending upon the level sensed, should be implemented at the host.

6 Pull-up values are based on +5 v Vcc.

7 Hosts that do not support Ultra DMA modes greater than mode 2 shall not connect to the PDIAG-:CBLID- signal.

8 The 80-conductor cable assembly shall meet the following requirements: the PDIAG-:CBLID- signal shall be connected to ground in the host connector of the cable assembly; the PDIAG-:CBLID- signal shall not be connected between the host and the devices; and, the PDIAG-:CBLID- signal shall be connected between the devices.

9 The host shall not drive DASP-. If the host connects to DASP- for any purpose, the host shall ensure that the signal level detected on the interface for DASP- shall maintain V<sub>oH</sub> and V<sub>oL</sub> compatibility, given the I<sub>oH</sub> and I<sub>oL</sub> requirements of the DASP- device drivers.

10 Values greater than 1 kΩ may improve noise margin.

#### 4.2.2 Electrical characteristics for Ultra DMA

Hosts that support Ultra DMA transfer modes greater than mode 2 shall not share signals between primary and secondary I/O ports. They shall provide separate drivers and separate receivers for each cable.

#### 4.2.2.1 Cable configuration

The following table defines the host transceiver configurations for a dual cable system configuration for all transfer modes.

Transfer mode	Optional host transceiver configuration	Recommended host transceiver configuration	Mandatory host transceiver configuration
All PIO and Multiword DMA	One transceiver may be used for signals to both ports	DIOR-, DIOW- and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW- and IORDY or CS0- and CS1- shall have a separate transceiver for each port.
Ultra DMA 0, 1, 2	One transceiver may be used for signals to both ports except DMACK-	DIOR-, DIOW- and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW- and IORDY or CS0- and CS1- shall have a separate transceiver for each port. DMACK- shall have a separate transceiver for each port
Ultra DMA 3, 4	One transceiver may be used for signals to both ports for RESET-, INTRQ, DA(2:0), CS0-, CS1-, and DASP-		All signals shall have a separate transceiver for each port except for RESET-, INTRQ, DA(2:0), CS0-, CS1-, and DASP-

The following table defines the system configuration for connection between devices and systems for all transfer modes.

Transfer mode	Single device direct connection configuration (see note 1)	40-conductor cable connection configuration (see note 2)	80-conductor cable connection configuration (see note 2)
All PIO and Multiword DMA	May be used.	May be used.	May be used (see note 3)
Ultra DMA 0, 1, 2	May be used.	May be used.	May be used (see note 3)
Ultra DMA 3, 4	May be used (see note 4).	Shall not be used.	May be used (see note 4).
<b>NOTES –</b> 1 Direct connection is a direct point-to-point connection between the host and device connectors. 2 The 40-conductor cable assembly and the 80-conductor cable assembly are defined in Annex A. 3 80-conductor cable assemblies may be used in place of 40-conductor cable assemblies to improve signal quality for data transfer modes that do not require an 80-conductor cable assembly. 4 Either a single device direct connection configuration or an 80-conductor cable connection configuration shall be used for systems operating with Ultra DMA modes greater than 2.			

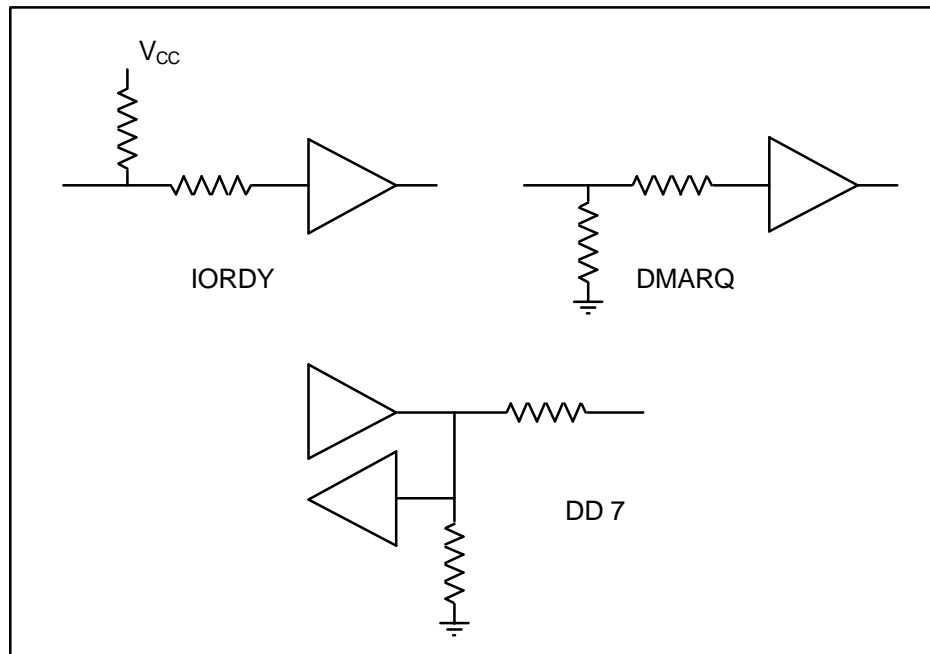
#### 4.2.2.2 Series termination required for Ultra DMA

Series termination resistors are required at both the host and the device for operation in any of the Ultra DMA modes. Table 5 describes typical values for series termination at the host and the device.

**Table 5 – Typical series termination for Ultra DMA**

Signal	Host Termination	Device Termination
DIOR-:HDMARDY- :HSTROBE	22 ohm	82 ohm
DIOW-:STOP	22 ohm	82 ohm
CS0-, CS1-	33 ohm	82 ohm
DA0, DA1, DA2	33 ohm	82 ohm
DMACK-	22 ohm	82 ohm
DD15 through DD0	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY:DDMARDY- :DSTROBE	82 ohm	22 ohm
RESET-	33 ohm	82 ohm

NOTE – Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Figure 2 shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.

**Figure 2 – Ultra DMA termination with pull-up or pull-down**

## 5 Interface signal assignments and descriptions

### 5.1 Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Table 6 defines the signal names. For connector descriptions see annex A. For driver and termination definition see 4.2.1. For signal protocol and timing see clause 9 and clause 10.

**Table 6 – Interface signal name assignments**

<b>Description</b>	<b>Host</b>	<b>Dir</b>	<b>Dev</b>	<b>Acronym</b>
Cable select		(see note)		CSEL
Chip select 0			→	CS0-
Chip select 1			→	CS1-
Data bus bit 0		↔		DD0
Data bus bit 1		↔		DD1
Data bus bit 2		↔		DD2
Data bus bit 3		↔		DD3
Data bus bit 4		↔		DD4
Data bus bit 5		↔		DD5
Data bus bit 6		↔		DD6
Data bus bit 7		↔		DD7
Data bus bit 8		↔		DD8
Data bus bit 9		↔		DD9
Data bus bit 10		↔		DD10
Data bus bit 11		↔		DD11
Data bus bit 12		↔		DD12
Data bus bit 13		↔		DD13
Data bus bit 14		↔		DD14
Data bus bit 15		↔		DD15
Device active or slave (Device 1) present		(see note)		DASP-
Device address bit 0			→	DA0
Device address bit 1			→	DA1
Device address bit 2			→	DA2
DMA acknowledge			→	DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read DMA ready during Ultra DMA data-in bursts Data strobe during Ultra DMA data-out bursts			→ → →	DIOR- HDMARDY- HSTROBE
I/O ready DMA ready during Ultra DMA data-out bursts Data strobe during Ultra DMA data-in bursts	← ← ←			IORDY DDMARDY- DSTROBE
I/O write Stop during Ultra DMA data bursts			→ →	DIOW- STOP
Passed diagnostics Cable assembly type identifier		(see note) (see note)		PDIAG- CBLID-
Reset			→	RESET-
NOTE – See signal descriptions and annex A for information on source of these signals				

## 5.2 Signal descriptions

### 5.2.1 CS (1:0)- (Chip select)

These are the chip select signals from the host used to select the Command Block registers (see 7.2). When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16-bits wide.

### 5.2.2 DA (2:0) (Device address)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device (see 7.2).

### 5.2.3 DASP- (Device active, device 1 present)

This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present.

NOTE – The indication that the device is active may be unsynchronized with the execution of the command.

### 5.2.4 DD (15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16-bits wide.

### 5.2.5 DIOR-:HDMARDY-:HSTROBE (Device I/O read:Ultra DMA ready:Ultra DMA data strobe)

DIOR- is the strobe signal asserted by the host to read device registers or the data port.

HDMARDY- is a flow control signal for Ultra DMA data-in bursts. This signal is asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY- to pause an Ultra DMA data-in burst.

HSTROBE is the data-out strobe signal from the host for an Ultra DMA data-out burst. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

### 5.2.6 DIOW-:STOP (Device I/O write:Stop Ultra DMA burst)

DIOW- is the strobe signal asserted by the host to write device registers or the data port

DIOW- shall be negated by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.

### 5.2.7 DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

### 5.2.8 DMARQ (DMA request)

This signal, used for DMA data transfers between host and device, shall be asserted by the device when the device is ready to transfer data to or from the host. For Multitword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK-, i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

This signal shall be released when the device is not selected.

### 5.2.9 INTRQ (Device interrupt)

This signal is used by the selected device to interrupt the host system when interrupt pending is set. When the nIEN bit is cleared to zero and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is set to one or the device is not selected, the INTRQ signal shall be released.

When asserted, this signal shall be negated by the device within 400 ns of the negation of DIOR- that reads the Status register to clear interrupt pending. When asserted, this signal shall be negated by the device within 400 ns of the negation of DIOW- that writes the Command register to clear interrupt pending.

When the device is selected by writing to the Device/Head register while interrupt pending is set, INTRQ shall be asserted within 400 ns of the negation of DIOW- that writes the Device/Head register. When the device is deselected by writing to the Device/Head register while interrupt pending is set, INTRQ shall be released within 400 ns of the negation of DIOW- that writes the Device/Head register.

For devices implementing the Overlapped feature set, if INTRQ assertion is being disabled using nIEN at the same instant that the device asserts INTRQ, the minimum pulse width shall be at least 40 ns.

This signal shall be released when the device is not selected.

### 5.2.10 IORDY:DDMARDY-:DSTROBE (I/O channel ready:Ultra DMA ready:Ultra DMA data strobe)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

If the device requires to extend the host transfer cycle time at PIO modes 3 and above, the device shall utilize IORDY. Hosts that use PIO modes 3 and above shall support IORDY.

DDMARDY- is a flow control signal for Ultra DMA data-out bursts. This signal is asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY- to pause an Ultra DMA data-out burst.

DSTROBE is the data-in strobe signal from the device for an Ultra DMA data-in burst. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.

This signal shall be released when the device is not selected.

### 5.2.11 PDIAG-:CBLID- (Passed diagnostics:Cable assembly type identifier)

PDIAG- shall be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics (see clause 9).

The host may sample CBLID- after a power-on or hardware reset in order to detect the presence or absence of an 80-conductor cable assembly by performing the following steps:

- a) The host shall wait until the power on or hardware reset sequence is complete for all devices on the cable;
- b) If Device 1 is present, the host should issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE and use the returned data to determine that Device 1 is compliant with ATA-3 or subsequent standards. Any device compliant with ATA-3 or subsequent standards releases PDIAG- no later than after the first command following a power on or hardware reset sequence.

NOTE – Older devices not in compliance with ATA-3 or subsequent standards may continue to assert this signal providing a false indication of the cable type. Issuing IDENTIFY DEVICE or IDENTIFY PACKET DEVICE not only provides the host with the information required to verify that the devices are compliant with these standards, but also provides a command resulting in the release of this signal.

If the host detects that CBLID- is connected to ground, an 80-conductor cable assembly is installed in the system. If the host detects that this signal is not connected to ground, an 80-conductor cable assembly is not installed in the system. See Annex D for a description of the non-standard device determination of cable type.

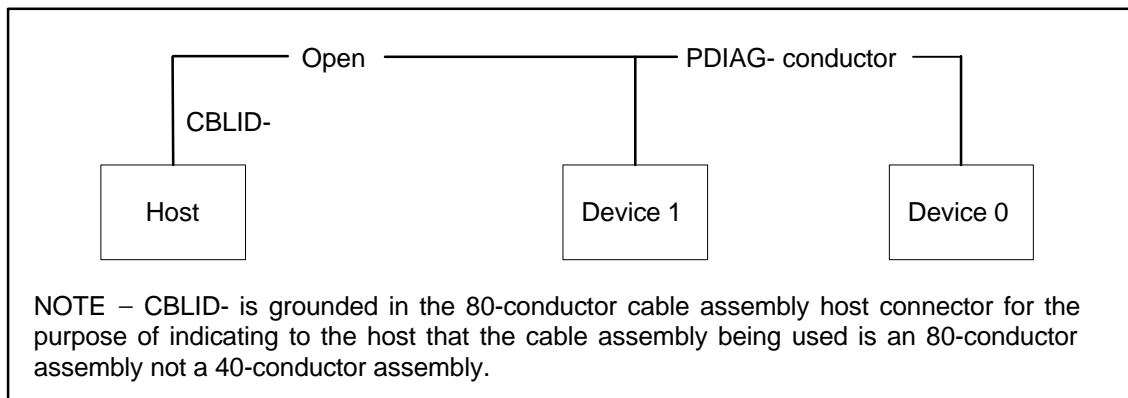


Figure 3 – PDIAG- example using an 80-conductor cable assembly

### 5.2.12 RESET- (Hardware reset)

This signal, referred to as hardware reset, shall be used by the host to reset the device (see 9.1).

### 5.2.13 CSEL (Cable select)

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL:

- If CSEL is negated, the device number is 0;
- If CSEL is asserted, the device number is 1.

#### 5.2.13.1 CSEL with 40 conductor cable

Special cabling may be used to selectively ground CSEL e.g., CSEL of Device 0 is connected to the CSEL conductor in the cable, and is grounded, thus allowing the device to recognize itself as Device 0. CSEL of Device 1 is not connected to CSEL because the conductor is removed, thus the device recognizes itself as

Device 1. It should be recognized that if a single device is configured at the end of the cable using CSEL, a device 1 only configuration results.

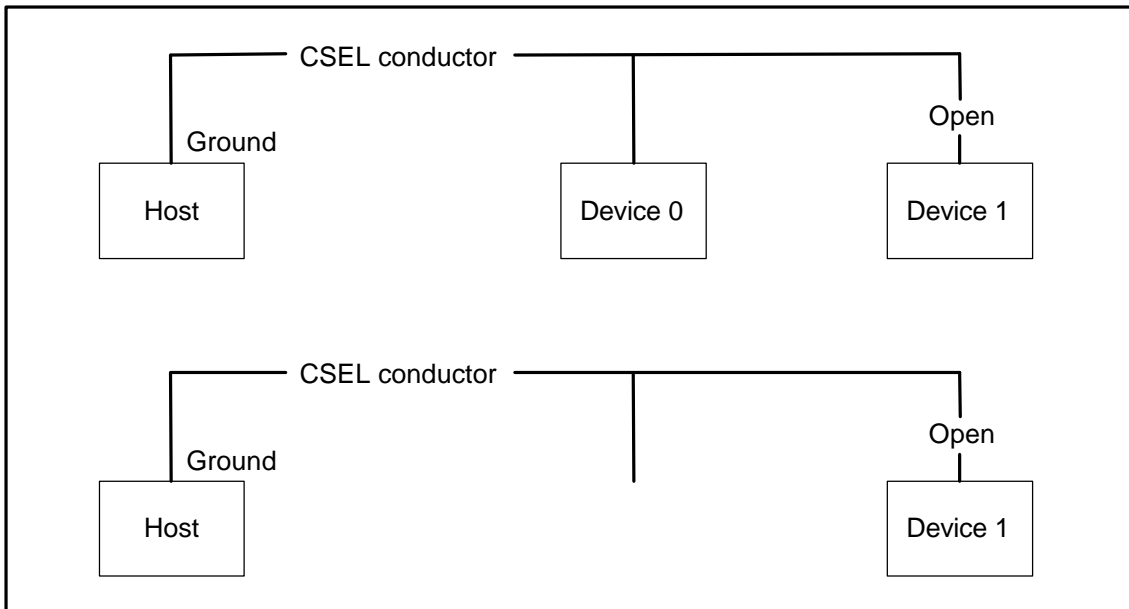


Figure 4 – Cable select example

**5.2.13.2 CSEL with 80 conductor cable**

For designated cable assemblies (including all 80-conductor cable assemblies): these assemblies are constructed so that CSEL is connected from the host connector to the connector at the opposite end of the cable from the host. Therefore, Device 0 shall be at the opposite end of the cable from the host. It should be recognized that if a single device is configured at the connector not at the end of the cable, a Device 1 only configuration results.

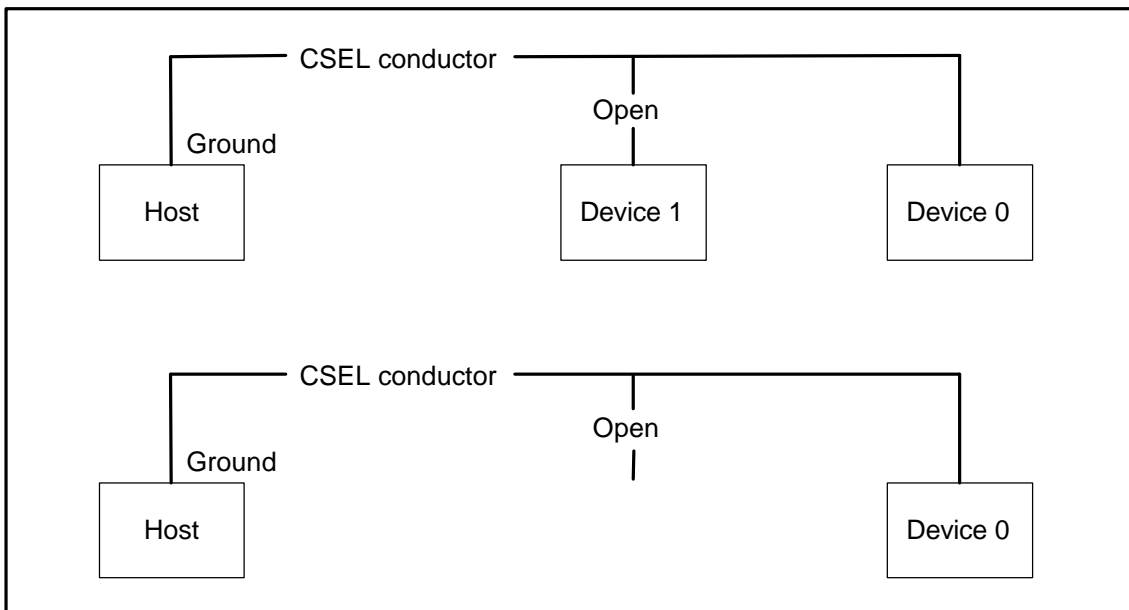


Figure 5 – Alternate cable select example



## 6 General operational requirements

### 6.1 Command delivery

Commands may be delivered in two forms. For devices that do not implement the PACKET Command feature set, all commands and command parameters are delivered by writing the device Command Block registers. Such commands are defined as register delivered commands.

Devices that implement the PACKET Command feature set utilize packet delivered commands as well as some register delivered commands.

All register delivered commands and the PACKET command are described in clause 8.

NOTE – The content of command packets delivered by the PACKET command are not described in this specification.

### 6.2 Register delivered data transfer command sector addressing

For register delivered data transfer commands all addressing of data sectors recorded on the device's media is by a logical sector address. There is no implied relationship between logical sector addresses and the actual physical location of the data sector on the media.

Devices shall support translations as described below:

- All devices shall support LBA translation.
- If the device's capacity is greater than or equal to one sector and less than or equal to 16,514,064 sectors, then the device shall support CHS translation.
- If the device's capacity is greater than 16,514,064 sectors, the device may support CHS translation.
- If a device supports CHS translation, then, following a power-on or hardware reset, the CHS translation enabled by the device shall be known as the default translation.
- If a device supports CHS translation, a device may allow a host to use the INITIALIZE DEVICE PARAMETERS command to select other CHS translations.
- If a device supports CHS translation, IDENTIFY DEVICE words 1,3, and 6 shall describe the default translation, and words 53-58 shall describe the current translation.

A CHS address is made up of three fields: the sector number, the head number, and the cylinder number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation but shall not exceed 255. Heads are numbered from 0 to the maximum value allowed by the current CHS translation but shall not exceed 15. Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation but shall not exceed 65,535.

When the host selects a CHS translation using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in the requested translation.

A device shall not change the addressing method specified by the command and shall return status information utilizing the addressing method specified for the command.

- 1) The host may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the LBA bit in the Device/Head register;
- 2) The device shall support LBA addressing for all media access commands.;

- 3) Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation currently in effect, the LBA address of a given logical sector does not change. The following is always true for LBA numbers less than or equal to 16,514,064 for devices supporting the current CHS translation:

$$\text{LBA} = (((\text{cylinder} * \text{heads\_per\_cylinder}) + \text{heads}) * \text{sectors\_per\_track}) + \text{sector} - 1$$

where heads\_per\_cylinder and sectors\_per\_track are the current translation values.

### 6.2.1 Definitions and value ranges of IDENTIFY DEVICE words (see 8.12)

- 1) Word 1 shall contain the number of user-addressable logical cylinders in the default CHS translation. If the content of words (61:60) is less than 16,514,064 then the content of word 1 shall be greater than or equal to one and less than or equal to 65,535. If the content of words (61:60) is greater than or equal to 16,514,064 then the content of word 1 shall be equal to 16,383.
- 2) Word 3 shall contain the number of user-addressable logical heads in the default CHS translation. The content of word 3 shall be greater than or equal to one and less than or equal to 16. For compatibility with some BIOSs, the content of word 3 may be equal to 15 if the content of word 1 is greater than 8192.
- 3) Word 6 shall contain the number of user-addressable logical sectors in the default CHS translation. The content of word 6 shall be greater than or equal to one and less than or equal to 63.
- 4) [(The content of word 1) \* (the content of word 3) \* (the content of word 6)] shall be less than or equal to 16,514,064.
- 5) Word 54 shall contain the number of user-addressable logical cylinders in the current CHS translation. The content of word 54 shall be greater than or equal to one and less than or equal to 65,535. After power-on or after a hardware reset the content of word 54 shall be equal to the content of word 1.
- 6) Word 55 shall contain the number of user-addressable logical heads in the current CHS translation. The content of word 55 shall be greater than or equal to one and less than or equal to 16. After power-on or after a hardware reset the content of word 55 shall be equal to the content of word 3.
- 7) Word 56 shall contain the number of user-addressable logical sectors in the current CHS translation. The content of word 56 should be equal to 63 for compatibility with all BIOSs. However, the content of word 56 may be greater than or equal to one and less than or equal to 255. At power-on or after a hardware reset the content of word 56 shall equal the content of word 6.
- 8) Words (58:57) shall contain the user-addressable capacity in sectors for the current CHS translation. The content of words (58:57) shall equal [(the content of word 54) \* (the content of word 55) \* (the content of word 56)]. The content of words (58:57) shall be less than or equal to 16,514,064. The content of words (58:57) shall be less than or equal to the content of words (61:60).
- 9) The content of words 54, 55, 56, and (58:57) may be affected by the host issuing an INITIALIZE DEVICE PARAMETERS command (see 8.16).
- 10) If the content of words (61:60) is greater than 16,514,064 and if the device does not support CHS addressing, then the content of words 1, 3, 6, 54, 55, 56, and (58:57) shall equal zero. If the content of word 1, word 3, or word 6 equals zero, then the content of words 1, 3, 6, 54, 55, 56, and (58:57) shall equal zero.
- 11) Words (61:60) shall contain the total number of user-addressable sectors. The content of words (61:60) shall be greater than or equal to one and less than or equal to 268,435,456.
- 12) The content of words 1, 54, (58:57), and (61:60) may be affected by the host issuing a SET MAX ADDRESS command (see 8.38).

### 6.2.2 Addressing constraints and error reporting

- 1) Devices may access any address in the current CHS translation if [(the requested cylinder + 1) \* (the requested head + 1) \* (the requested sector)] is less than or equal to the content of words (61:60).
- 2) Devices may respond with an "ID NOT FOUND" or a command aborted error to any command with a CHS address request where one or more of the following are true:
  - a) The requested cylinder value is greater than [(the content of word 54) - 1]
  - b) The requested head value is greater than [(the content of word 55) - 1]

- c) The requested sector value is zero or greater than the content of word 56
- 3) Devices shall respond with an "ID NOT FOUND" or a command aborted error to any command with an LBA address request where the requested LBA number is greater than or equal to the content of words (61:60).

### 6.3 Interrupts

INTRQ is used by the selected device to notify the host of an event. The device internal interrupt pending state is set when such an event occurs. If nIEN is cleared to zero, INTRQ is asserted (see 5.2.9).

The device shall enter the interrupt pending state when:

- 1) any command except a PIO data-in command reaches command completion successfully;
- 2) any command reaches command completion with error;
- 3) the device is ready to send a data block during a PIO data-in command;
- 4) the device is ready to accept a data block after the first data block during a PIO data-out command;
- 5) a device implementing the PACKET Command feature set is ready to receive the command packet and bits 6-5 in word 0 of the IDENTIFY PACKET DEVICE response have the value 01b;
- 6) a device implementing the PACKET Command feature set is ready to transfer a DRQ data block during a PIO transfer;
- 7) a device implementing the Overlap feature set performs a bus release if the Bus release interrupt is enabled;
- 8) a device implementing the Overlap feature set has performed a Bus release and is now ready to continue the command execution;
- 9) a device implementing the Overlap feature set is ready to transfer data after a SERVICE command if the Service interrupt is enabled;
- 10) Device 0 completes an EXECUTE DEVICE DIAGNOSTIC command. Device 1 does not enter the interrupt pending state when completing an EXECUTE DEVICE DIAGNOSTIC command.

The device shall not exit the interrupt pending state when the device is deselected.

The device shall exit the interrupt pending state when:

- 1) the device is selected, BSY is cleared to zero, and the Status register is read;
- 2) the device is selected, both BSY and DRQ are cleared to zero, and the Command register is written;
- 3) the RESET- signal is asserted;
- 4) the SRST bit is set to one.

### 6.4 General feature set

The General feature set defines the common commands implemented by devices.

#### 6.4.1 General feature set for devices not implementing the PACKET command feature set

The following General feature set commands are mandatory for all devices not implementing the PACKET command feature set:

- EXECUTE DEVICE DIAGNOSTIC
- IDENTIFY DEVICE
- INITIALIZE DEVICE PARAMETERS
- READ DMA
- READ MULTIPLE
- READ SECTOR(S)
- READ VERIFY SECTOR(S)
- SEEK
- SET FEATURES

- SET MULTIPLE MODE
- WRITE DMA
- WRITE MULTIPLE
- WRITE SECTOR(S)

The following General feature set commands are optional for devices not implementing the PACKET command feature set:

- DOWNLOAD MICROCODE
- FLUSH CACHE
- NOP
- READ BUFFER
- WRITE BUFFER

Read only devices shall return command aborted in response to write commands.

The following General feature set command is prohibited for use by devices not implementing the PACKET command feature set:

- DEVICE RESET

The following resets are mandatory for devices not implementing the PACKET command feature set:

- Power On Reset: Executed at power on, the device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parameters, and sets default values (see 9.1).
- Hardware Reset: Executed in response to the assertion of the RESET- signal the device executes a series of electrical circuitry diagnostics, and resets to default values (see 9.1).
- Software Reset: Executed in response to the setting of the SRST bit in the Device Control register the device resets the interface circuitry (see 9.2).

#### **6.4.2 General feature set for devices implementing the PACKET command feature set**

The following General feature set commands are mandatory for all devices implementing the PACKET command feature set:

- DEVICE RESET
- EXECUTE DEVICE DIAGNOSTIC
- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- NOP
- READ SECTOR(S)
- SET FEATURES

The following General command set commands are optional for devices implementing the PACKET command feature set:

- FLUSH CACHE

The following General command set commands are prohibited for use by devices implementing the PACKET command feature set.

- DOWNLOAD MICROCODE
- INITIALIZE DEVICE PARAMETERS
- READ BUFFER
- READ DMA
- READ MULTIPLE
- READ VERIFY
- SEEK
- SET MULTIPLE MODE
- WRITE BUFFER

- WRITE DMA
- WRITE MULTIPLE
- WRITE SECTOR(S)

The following resets are mandatory for devices implementing the PACKET command feature set:

- Power On Reset: Executed at power on, the device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametrics, and sets default values (see 9.1).
- Hardware Reset: Executed in response to the assertion of the RESET- signal the device executes a series of electrical circuitry diagnostics, and resets to default values (see 9.1).
- Software Reset: Executed in response to the setting of the SRST bit in the Device Control register the device resets the interface circuitry (see 9.2).
- Device Reset: Executed in response to the DEVICE RESET command the device resets the interface circuitry (see 8.7).

## 6.5 Multiword DMA

Multiword DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED, and PACKET commands. When a Multiword DMA transfer mode has been set via the SET FEATURES 03h subcommand, this data transfer protocol shall be used for the data transfers associated with these commands. Signal timing for this protocol is described in 10.2.3.

The DMARQ and DMACK- signals are used to signify when a Multiword DMA transfer is to be executed. The DMARQ and DMACK- signals are also used control the data flow of a Multiword DMA data transfer.

When a device is ready to transfer data associated with a Multiword DMA transfer, the device shall assert DMARQ. The host shall then respond by negating CS0- and CS1-, asserting DMACK-, and begin the data transfer by asserting, then negating, DIOW- or DIOR- for each word transferred. CS0- and CS1- shall remain negated as long as DMACK- is asserted. The host shall not assert DMACK- until DMARQ has been asserted by the device shall transfer data only when both DMARQ and DMACK- are asserted. Having asserted DMARQ and DMACK-, these signals shall remain asserted until at least one word of data has been transferred.

The device may pause the transfer for flow control purposes by negating DMARQ. The host shall negate DMACK- in response to the negation of DMARQ. The device may then reassert DMARQ to continue the data transfer when the device ready to transfer more data and DMACK- has been negated by the host.

The host may pause the transfer for flow control purposes by either pausing the assertion of DIOW- or DIOR- pulses or by negating DMACK-. The device may leave DMARQ asserted if DMACK- is negated. The host may then reassert DMACK- when DMARQ is asserted and begin asserting DIOW- or DIOR- pulses to continue the data transfer.

When the Multiword DMA data transfer is complete, the device shall negate DMARQ and the host shall negate DMACK- in response.

DMARQ shall be driven from the first assertion at the beginning of a DMA transfer until the negation after the last word is transferred. This signal shall be released at all other times.

## 6.6 Ultra DMA feature set

### 6.6.1 Overview

Ultra DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED, and PACKET commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).

Several signal lines are redefined to provide new functions during an Ultra DMA burst. These lines assume these definitions when:

- 1) an Ultra DMA mode is selected, and
- 2) a host issues a READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED, or a PACKET command requiring data transfer, and
- 3) the host asserts DMACK-.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of DMACK- by the host at the termination of an Ultra DMA burst. All of the control signals are unidirectional. DMARQ and DMACK- retain their standard definitions.

With the Ultra DMA protocol, the control signal (STROBE) that latches data from DD(15:0) is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of DD(15:0) and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the maximum frequency of the data. The highest fundamental frequency on the cable shall be 16.67 MHz which equates to 33.33 million transitions per second .

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting Ultra DMA mode 4 shall also support Ultra DMA modes 3, 2, 1, and 0. Devices supporting Ultra DMA mode 3 shall also support ultra DMA modes 2, 1, and 0. Devices supporting Ultra DMA mode 2 shall also support Ultra DMA modes 0 and 1. Devices supporting Ultra DMA mode 1 shall also support Ultra DMA mode 0. Hosts supporting Ultra DMA may support any combination of modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a Software reset sequence or the sequence caused by receipt of a DEVICE RESET command. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a Power on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

## 6.6.2 Phases of operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see 9.13 and 9.14 for the detailed protocol descriptions for each of these phases, 10.2.4 defines the specific timing requirements). In the following rules DMARDY- is used in cases that could apply to either DDMARDY- or HDMARDY-, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

- 1) An Ultra DMA burst is defined as the period from an assertion of DMACK- by the host to the subsequent negation of DMACK-.
- 2) When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused. When operating in Ultra DMA modes 4 or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA burst is paused.

### 6.6.2.1 Ultra DMA burst initiation phase rules

- 1) An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.
- 2) An Ultra DMA burst shall always be requested by a device asserting DMARQ.
- 3) When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting DMACK-.
- 4) A host shall never assert DMACK- without first detecting that DMARQ is asserted.
- 5) For Ultra DMA data-in bursts: a device may begin driving DD(15:0) after detecting that DMACK- is asserted, STOP negated, and HDMARDY- is asserted.
- 6) After asserting DMARQ or asserting DDMARDY- for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.
- 7) After negating STOP or asserting HDMARDY- for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

### 6.6.2.2 Data transfer phase rules

- 1) The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.
- 2) A recipient pauses an Ultra DMA burst by negating DMARDY- and resumes an Ultra DMA burst by reasserting DMARDY-.
- 3) A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
- 4) A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate DMARDY- and wait the required period before signaling a termination request.
- 5) A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

### 6.6.2.3 Ultra DMA burst termination phase rules

- 1) Either a sender or a recipient may terminate an Ultra DMA burst.
- 2) Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset to the device.
- 3) An Ultra DMA burst shall be paused before a recipient requests a termination.
- 4) A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
- 5) A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.

- 6) Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
- 7) A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.
- 8) Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
- 9) A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

## 6.7 Host determination of cable type

In a system using a cable, hosts shall determine that an 80-conductor cable is installed in a system before operating with transfer modes faster than Ultra DMA mode 2. Hosts shall detect that CBLID- is connected to ground to determine the cable type.

For detecting that CBLID- is connected to ground, the host shall test to see if CBLID- is below  $V_{IL}$  or above  $V_{IH}$ . If the signal is below  $V_{IL}$ , then an 80-conductor cable assembly is installed in the system because this signal is grounded in the 80-conductor cable assembly's host connector. If the signal is above  $V_{IH}$ , then a 40-conductor cable assembly is installed because this signal is connected to the device(s) and is pulled up through a 10 kΩ resistor at each device.

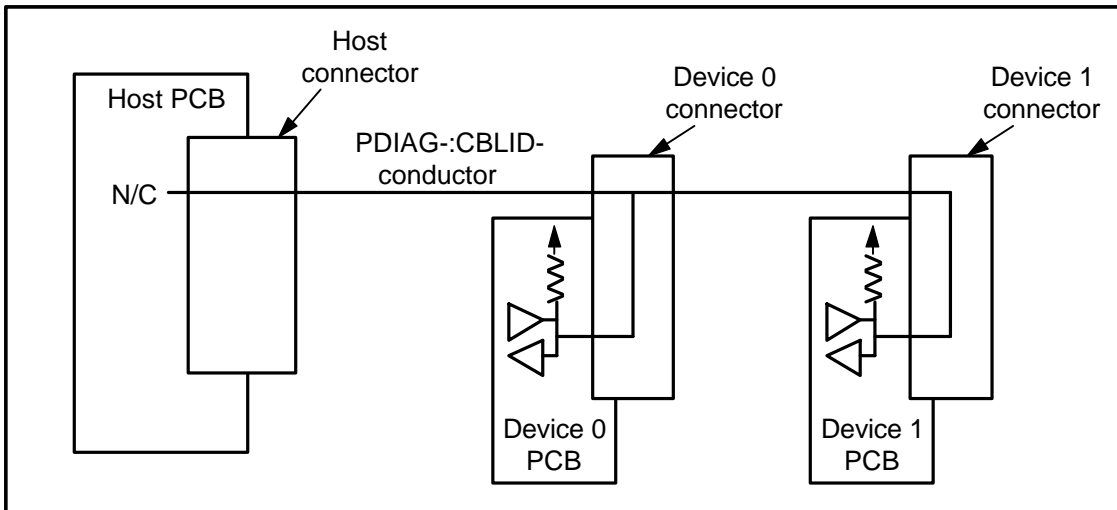


Figure 6 – Example configuration of a system with a 40-conductor cable

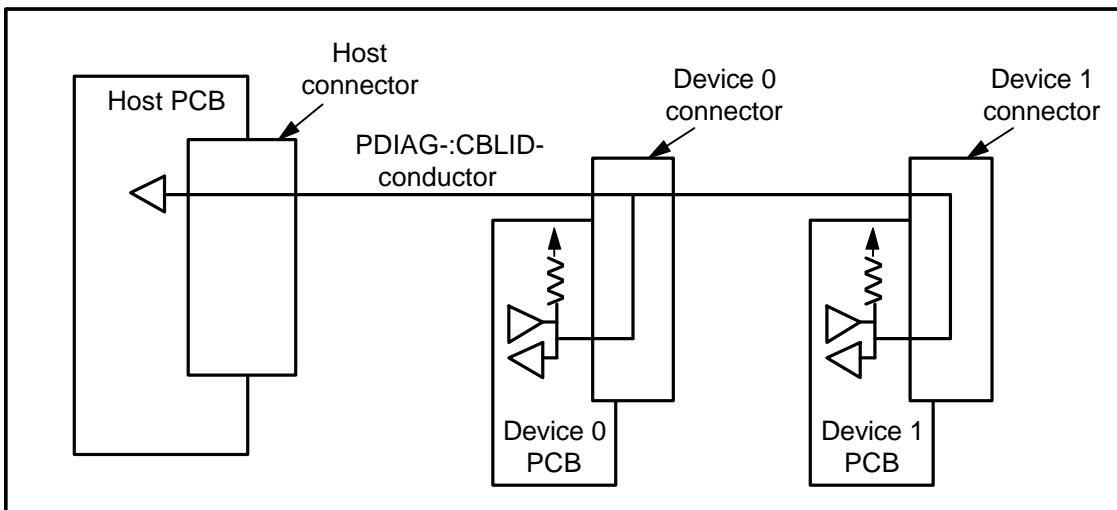


Figure 7 – Example configuration of a system where the host detects a 40-conductor cable



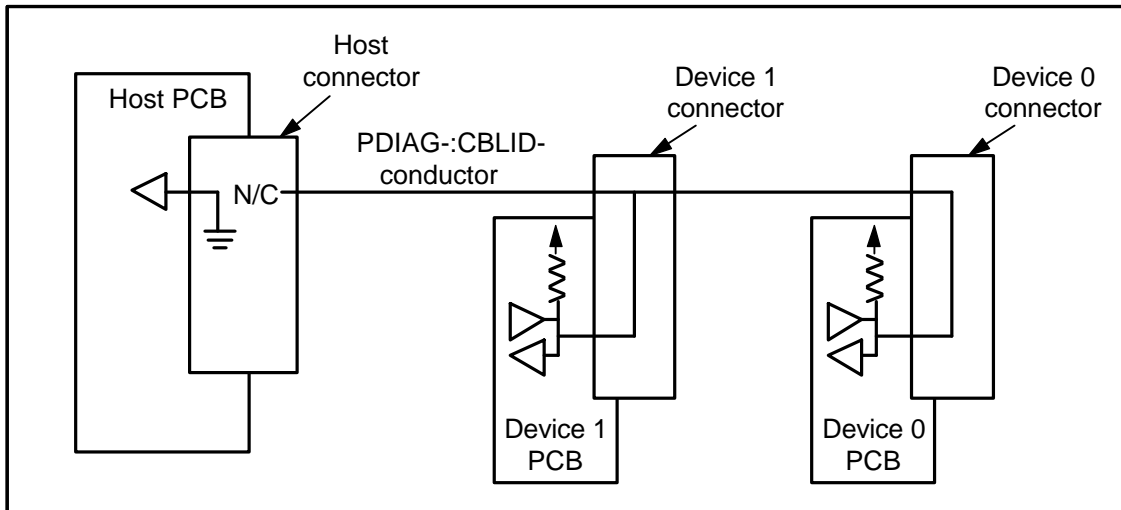


Figure 8 – Example configuration of a system where the host detects an 80-conductor cable

Table 7 – Host detection of CBLID-

Cable assembly type	Device 1 releases PDIAG-	Electrical state of CBLID- at host	Host-determined cable type	Determination correct?
40-conductor	Yes	1	40-conductor	Yes
80-conductor	Yes	0	80-conductor	Yes
40-conductor	No	0	80-conductor	No (see note)
80-conductor	No	0	80-conductor	Yes

NOTE – Ultra DMA mode 3 or 4 may be set incorrectly resulting in ICRC errors.

## 6.8 PACKET Command feature set

The PACKET Command feature set provides for devices that require command parameters that are too extensive to be expressed in the Command Block registers. Devices implementing the PACKET Command feature set exhibit responses different from those exhibited by devices not implementing this feature set.

The commands unique to the PACKET Command feature set are:

- PACKET
- IDENTIFY PACKET DEVICE

### 6.8.1 Identification of PACKET Command feature set devices

When executing a power on, hardware, DEVICE RESET, or software reset, a device implementing the PACKET Command feature set performs the same reset protocol as other devices but leaves the registers with a signature unique to PACKET Command feature set devices (see 9.12).

In addition, the IDENTIFY DEVICE command shall not be executed but shall be command aborted and shall return a signature unique to devices implementing the PACKET Command feature set. The IDENTIFY PACKET DEVICE command is used by the host to get identifying parameter information for a device implementing the PACKET Command feature set (see 8.12.5.2 and 8.13).

### 6.8.2 PACKET Command feature set resets

Devices implementing the PACKET Command feature set respond to power-on, hardware, and software resets as any other device except for the resulting contents in the device registers as described above. However, software reset should not be issued while a PACKET command is in progress. PACKET commands utilized by some devices do not terminate if a software reset is issued.

The DEVICE RESET command is provided to allow the device to be reset without affecting the other device on the bus.

### 6.8.3 The PACKET command

The PACKET command allows a host to send a command to the device via a command packet. The command packet contains the command and command parameters that the device is to execute.

Upon receipt of the PACKET command the device sets BSY to one and prepares to receive the command packet. When ready, the device sets DRQ to one and clears BSY to zero. The command packet is then transferred to the device by PIO transfer. When the last word of the command packet is transferred, the device sets BSY to one, and clears DRQ to zero (see 8.21 and 9.8).

## 6.9 Overlapped feature set

Overlap allows devices that require extended command time to perform a bus release so that the other device on the bus may be used. To perform a bus release the device shall clear both DRQ and BSY to zero. When selecting the other device during overlapped operations, the host shall disable interrupts via the nIEN bit on the currently selected device before writing the Device/Head register to select the other device.

The only commands that may be overlapped are:

- NOP (with a subcommand code other than 00h)
- PACKET
- READ DMA QUEUED
- SERVICE
- WRITE DMA QUEUED

For the PACKET command, overlap is indicated by the OVL bit in the Features register when the PACKET command is issued.

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been enabled via the SET FEATURES command, then the device shall perform a bus release when the command packet has been received. This allows the host to select the other device to execute commands. When the device is ready to continue the command, the device sets SERV to one, and asserts INTRQ if selected and interrupts are enabled. The host then issues the SERVICE command to continue the execution of the command

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, then the device may or may not perform a bus release. If the device is ready to complete execution of the command, the device may complete the command immediately as described in the non-overlap case. If the device is not ready to complete execution of the command, the device may perform a bus release and complete the command as described in the previous paragraph.

For the READ DMA QUEUED and WRITE DMA QUEUED commands, the device may or may not perform a bus release. If the device is ready to complete execution of the command, the device may complete the command immediately. If the device is not ready to complete execution of the command, the device may perform a bus release and complete the command via a service request.

If a device has an outstanding command that has been released, the device can only indicate that service is required when the device is selected. This implies that the host has to poll each device to determine if a device is requesting service. The polling can be performed at the host either by hardware or by a software routine. The latter implies a considerable host processor overhead. Hardware polling is initiated by the NOP Auto Poll command.

The NOP Auto Poll command is a host adapter function and is ignored by the device. The host software can test for the support of this feature by issuing the NOP Auto Poll command and examining the Status

register. If the host adapter does not support this feature, the response received by the host will be from the device with the ERR bit set to one. If the host adapter does support the command, the response will be from the host adapter with the ERR bit cleared to zero. The only action taken by a device supporting the Overlapped feature set will be to return the error indication in the Status register and to not abort any outstanding commands.

## 6.10 Queued feature set

Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the overlapped feature set may be queued. The queue contains all commands for which command acceptance has occurred but command completion has not occurred. If a queue exists when a non-queued command is received, the non-queued command shall be command aborted and the commands in the queue shall be discarded. The ending status shall be command aborted and the results are indeterminate.

The maximum queue depth supported by a device shall be indicated in word 75 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

A queued command shall have a Tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this Tag shall be restored so that the host may identify the command for which status is being presented. A Tag value may be any value between 0 and 31, regardless of the queue depth supported. If a queued command is issued with a Tag value that is identical to the Tag value for a command already in the queue, the entire queue shall be aborted including the new command. The ending status shall be command aborted and the results are indeterminate. If any error occurs, the command queue shall be aborted.

When the device is ready to continue the processing of a bus released command and BSY and DRQ are both cleared to zero, the device requests service by setting SERV to one, setting a pending interrupt, and asserting INTRQ if selected and if nIEN is cleared to zero. SERV shall remain set until all commands ready for service have been serviced. The pending interrupt shall be cleared and INTRQ negated by a Status register read or a write to the Command register.

When the device is ready to continue the processing of a bus released command and BSY or DRQ is set to one (i.e., the device is processing another command on the bus), the device requests service by setting SERV to one. SERV shall remain set until all commands ready for service have been serviced. At command completion of the current command processing (i.e., when both BSY and DRQ are cleared to zero), the device shall process interrupt pending and INTRQ per the protocol for the command being completed. No additional interrupt shall occur due to other commands ready for service until after the device's SERV bit has been cleared to zero.

When the device receives a new command while queued commands are ready for service, the device shall execute the new command and process interrupt pending and INTRQ per the protocol for the new command. If the queued commands ready for service still exist at command completion of this command, SERV remains set to one but no additional interrupt shall occur due to commands ready for service.

When queuing commands, the host shall disable interrupts via the nIEN bit before writing a new command to the Command register and may re-enable interrupts after writing the command. When reading status at command completion of a command, the host shall check the SERV bit since the SERV bit may be set because the device is ready for service associated with another command. The host receives no additional interrupt to indicate that a queued command is ready for service.

## 6.11 Power Management feature set

A device shall implement power management. A device implementing the PACKET Command feature set may implement the power management as defined by the packet command set implemented by the device. Otherwise, the device shall implement the Power Management feature set as described in this standard.

The Power Management feature set permits a host to modify the behavior of a device in a manner that reduces the power required to operate. The Power Management feature set provides a set of commands and a timer that enable a device to implement low power consumption modes. A register delivered command device that implements the Power Management feature set shall implement the following minimum set of functions:

- A Standby timer
- CHECK POWER MODE command
- IDLE command
- IDLE IMMEDIATE command
- SLEEP command
- STANDBY command
- STANDBY IMMEDIATE command

A device that implements the PACKET Command feature set and implements the Power Management feature set shall implement the following minimum set of functions:

- CHECK POWER MODE command
- IDLE IMMEDIATE command
- SLEEP command
- STANDBY IMMEDIATE command

### **6.11.1 Power management commands**

The CHECK POWER MODE command allows a host to determine if a device is currently in, going to or leaving Standby or Idle mode. The CHECK POWER MODE command shall not change the power mode or affect the operation of the Standby timer.

The IDLE and IDLE IMMEDIATE commands move a device to Idle mode immediately from the Active or Standby modes. The IDLE command also sets the Standby timer count and enables or disables the Standby timer.

The STANDBY and STANDBY IMMEDIATE commands move a device to Standby mode immediately from the Active or Idle modes. The STANDBY command also sets the Standby timer count and enables or disables the Standby timer.

The SLEEP command moves a device to Sleep mode. The device's interface becomes inactive at command completion of the SLEEP command. A hardware or software reset or DEVICE RESET command is required to move a device out of Sleep mode.

### **6.11.2 Standby timer**

The Standby timer provides a method for the device to automatically enter Standby mode from either Active or Idle mode following a host programmed period of inactivity. If the Standby timer is enabled and if the device is in the Active or Idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the Standby mode.

If the Standby timer is disabled, the device may not automatically enter Standby mode.

### **6.11.3 Power modes**

Figure 9 shows the minimum set of mode transitions that shall be implemented.

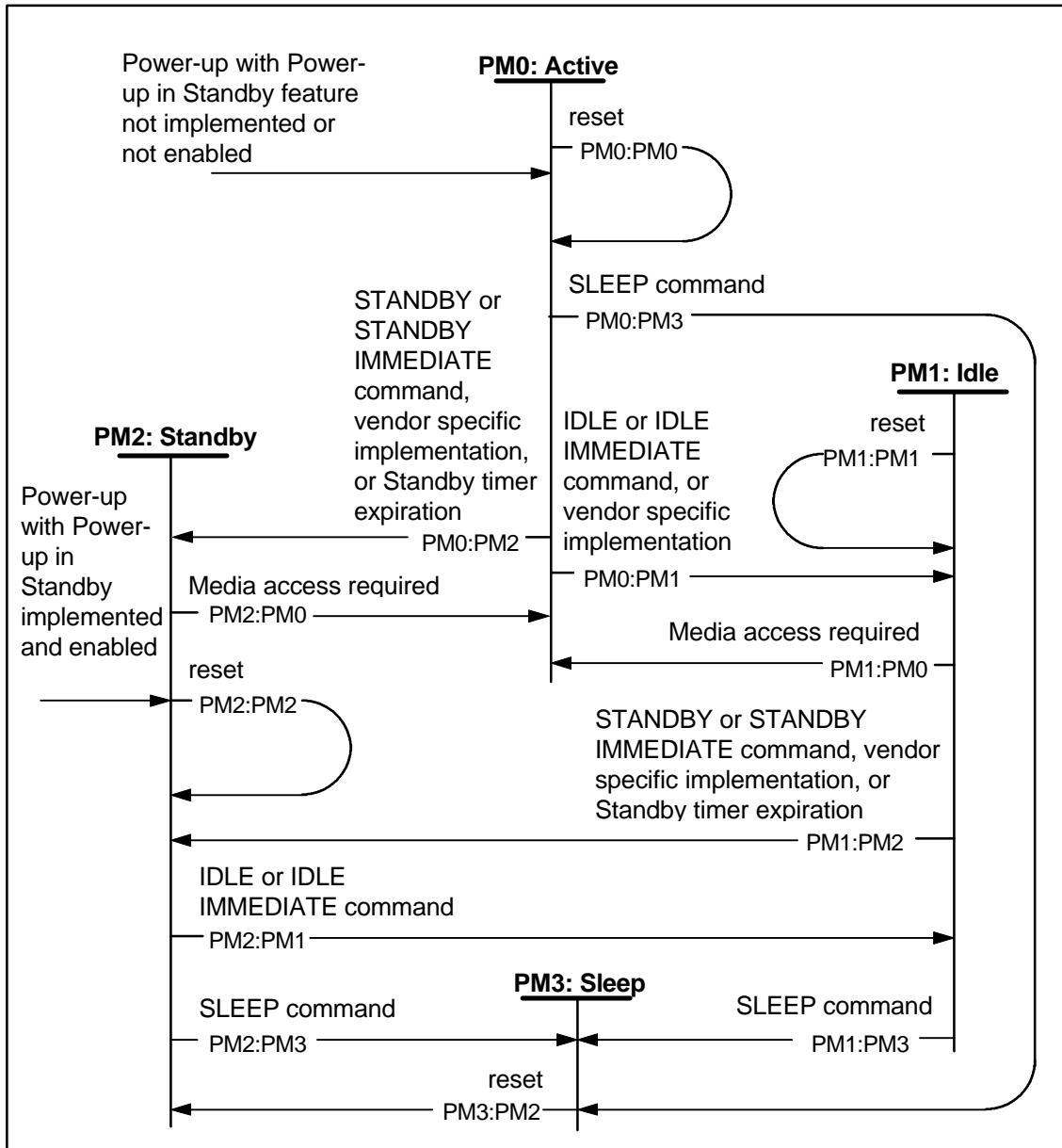


Figure 9 – Power management state diagram

**PM0: Active:** This mode shall be entered when the device receives a media access command while in Idle or Standby mode. This mode shall also be entered when the device is powered-up with the Power-Up In Standby feature not implemented or not enabled (see 6.18).

In Active mode the device is capable of responding to commands. During the execution of a media access command a device shall be in Active mode. Power consumption is greatest in this mode.

**Transition PM0:PM0:** When hardware reset, software rest, or DEVICE RESET command is received, the device shall transition to the PM0: Active mode when the reset protocol is completed.

**Transition PM0:PM1:** When an IDLE or IDLE IMMEDIATE command is received or when a vendor specific implementation determines a transition is required, then the device shall transition to the PM1:Idle mode.

**Transition PM0:PM2:** When a STANDBY or STANDBY IMMEDIATE command is received, the Standby timer expires, or a vendor specific implementation determines a transition is required, then the device shall transition to the PM2:Standby mode.

**Transition PM0:PM3:** When a SLEEP command is received, the device shall transition to the PM3:Sleep mode.

**PM1: Idle:** This mode shall be entered when the device receives an IDLE or IDLE IMMEDIATE command. Some devices may perform vendor specific internal power management and transition to the Idle mode without host intervention.

In Idle mode the device is capable of responding to commands but the device may take longer to complete commands than when in the Active mode. Power consumption may be reduced from that of Active mode.

**Transition PM1:PM0:** When a media access is required, the device shall transition to the PM0:Active mode.

**Transition PM1:PM1:** When hardware reset, software rest, or DEVICE RESET command is received, the device shall transition to the PM1:Idle mode when the reset protocol is completed.

**Transition PM1:PM2:** When a STANDBY or STANDBY IMMEDIATE command is received, the Standby timer expires, or a vendor specific implementation determines a transition is required, then the device shall transition to the PM2:Standby mode.

**Transition PM1:PM3:** When a SLEEP command is received, the device shall transition to the PM3:Sleep mode.

**PM2: Standby:** This mode shall be entered when the device receives a STANDBY command, a STANDBY IMMEDIATE command, or the Standby timer expires. Some devices may perform vendor specific internal power management and transition to the Standby mode without host intervention. This mode shall also be entered when the device is powered-up with the Power-Up In Standby feature implemented and enabled.

In Standby mode the device is capable of responding to commands but the device may take longer to complete commands than in the Idle mode. The time to respond could be as long as 30 s. Power consumption may be reduced from that of Idle mode.

**Transition PM2:PM0:** When a media access is required, the device shall transition to the PM0:Active mode.

**Transition PM2:PM1:** When an IDLE or IDLE IMMEDIATE command is received, or a vendor specific implementation determines a transition is required, then the device shall transition to the PM1:Idle mode.

**Transition PM2:PM2:** When hardware reset, software rest, or DEVICE RESET command is received, the device shall transition to the PM2:Standby mode when the reset protocol is completed.

**Transition PM2:PM3:** When a SLEEP command is received, the device shall transition to the PM3:Sleep mode.

**PM3: Sleep:** This mode shall be entered when the device receives a SLEEP command.

In Sleep mode the device requires a hardware or software reset or a DEVICE RESET command to be activated. The time to respond could be as long as 30 s. Sleep mode provides the lowest power consumption of any mode.

In Sleep mode, the device's interface is not active. The content of the Status register is invalid in this mode.

**Transition PM3:PM2:**, When hardware reset, software rest, or DEVICE RESET command is received the device shall transition to the PM2:Standby mode.

## 6.12 Advanced Power Management feature set

The Advanced Power Management feature set is an optional feature set that allows the host to select a power management level. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. [A device may implement one power management method for two or more contiguous power management levels.](#) For example, a device may implement one power management method from level 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

The Advanced Power Management feature set uses the following functions:

- A SET FEATURES subcommand to enable Advanced Power Management
- A SET FEATURES subcommand to disable Advanced Power Management

Advanced Power Management is independent of the Standby timer setting. If both Advanced Power Management and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that the Standby state should be entered.

The IDENTIFY DEVICE indicates that Advanced Power Management is supported, if Advanced Power Management is enabled, and the current advanced power management level if Advanced Power Management is enabled.

## 6.13 Security Mode feature set

The Security Mode feature set is a password system that restricts access to user data stored on a device. The system has two passwords, User and Master and two security levels, High and Maximum. The security system is enabled by sending a user password to the device with the SECURITY SET PASSWORD command. When the security system is enabled, access to user data on the device is denied after a power cycle until the User password is sent to the device with the SECURITY UNLOCK command.

A Master password may be set in a addition to the User password. The purpose of the Master password is to allow an administrator to establish a password that is kept secret from the user, and which may be used to unlock the device if the User password is lost. Setting the Master password does not enable the password system.

The security level is set to High or Maximum with the SECURITY SET PASSWORD command. The security level determines device behavior when the Master password is used to unlock the device. When the security level is set to High the device requires the SECURITY UNLOCK command and the Master password to unlock. When the security level is set to Maximum the device requires a SECURITY ERASE PREPARE command and a SECURITY ERASE UNIT command with the master password to unlock.

The SECURITY FREEZE LOCK command prevents changes to passwords until a following power cycle. The purpose of the SECURITY FREEZE LOCK command is to prevent password setting attacks on the security system.

A device that implements the Security Mode feature set shall implement the following minimum set of commands:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

Support of the Security Mode feature set is indicated in IDENTIFY DEVICE word 128.

### **6.13.1 Security mode default setting**

The Master password shall be set to a vendor specific value during manufacturing and the password system disabled.

If the Master Password Revision Code feature set is supported, the Master Password Revision Code shall be set to FFFEh by the manufacturer.

### **6.13.2 User password lost**

If the User password sent to the device with the SECURITY UNLOCK command does not match the user password previously set with the SECURITY SET PASSWORD command and the device shall not allow the user to access data.

If the Security Level was set to High during the last SECURITY SET PASSWORD command the device shall be unlocked using the Master password.

If the Security Level was set to Maximum during the last SECURITY SET PASSWORD command the device shall not be unlocked using the Master password. The SECURITY ERASE UNIT command shall erase all user data and unlock the device if the Master password matches the last Master password previously set with the SECURITY SET PASSWORD command .

### **6.13.3 Attempt limit for SECURITY UNLOCK command**

The device shall have an attempt limit counter. The purpose of this counter is to defeat repeated trial attacks. After each failed User or Master password SECURITY UNLOCK command, the counter is decremented. When the counter value reaches zero the EXPIRE bit (bit 4) of word 128 in the IDENTIFY DEVICE information is set to one, and the SECURITY UNLOCK and SECURITY UNIT ERASE commands are command aborted until the device is powered off or hardware reset. The EXPIRE bit shall be cleared to zero after power on or hardware reset. The counter shall be set to five after a power on or hardware reset.

### **6.13.4 Security mode states**

Figure 8 describes security mode states and state transitions.



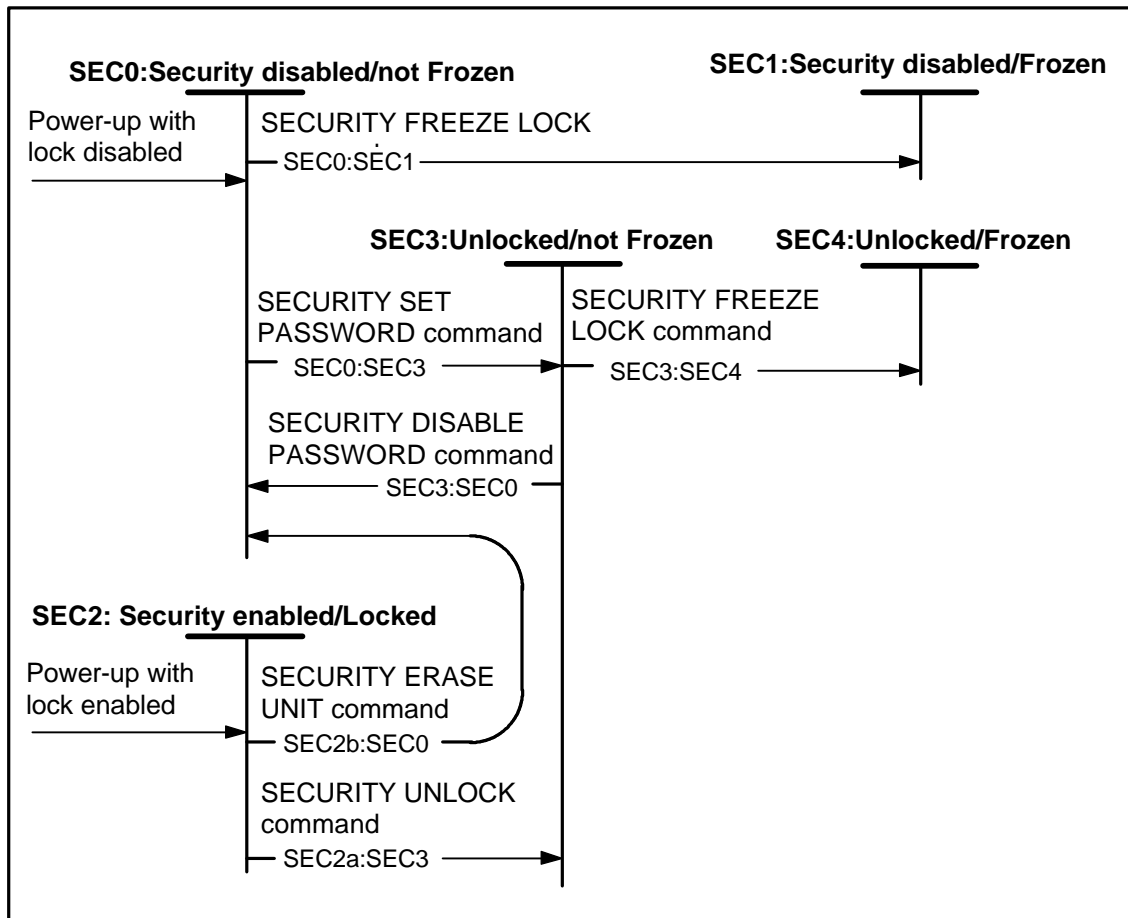


Figure 10 – Security mode state diagram

**SEC0: Security disabled/not Frozen:** This mode shall be entered when the device is powered-up with the Security Mode feature set disabled or when the Security Mode feature set is disabled by a SECURITY DISABLE PASSWORD command.

In this state, the device is capable of responding to all commands (see Table 8 Unlocked column).

**Transition SEC0:SEC1:** When a SECURITY FREEZE LOCK command is received, the device shall transition to the SEC1: Security disabled/Frozen state.

**Transition SEC0:SEC3:** When a SECURITY SET PASSWORD command is received, the device shall transition to the SEC3: Unlocked/not frozen state

**SEC1: Security disabled/ Frozen:** This mode shall be entered when the receives a SECURITY FREEZE LOCK command while in Security disabled/not Frozen state.

In this state, the device is capable of responding to all commands except those indicated in Table 8 Frozen column . The device shall remain in this state until the device is powered-down.

**SEC2: Security enabled/locked:** This mode shall be entered when the device is powered-up with the Security Mode feature set enabled.

In this state, the device shall only respond to commands that do not access data in the user data area of the media (see Table 8 Locked column).

**Transition SEC2a:SEC3:** When a valid SECURITY UNLOCK command is received, the device shall transition to the SEC3: Unlocked/not Frozen state.

**Transition SEC2b:SEC0:** When a SECURITY ERASE PREPARE command is received and is followed by a SECURITY ERASE UNIT command, the device shall transition to the SEC0: Security disabled/not Frozen state.

**SEC3: Unlocked/not Frozen:** This mode shall be entered when the device receives a SECURITY SET PASSWORD command to enable the lock, a SECURITY UNLOCK command, or a SECURITY ERASE UNIT command.

In this state, the device shall respond to all commands (see Table 8 Unlocked column).

**Transition SEC3:SEC0:** When a valid SECURITY DISABLE PASSWORD command is received, the device shall transition to the SEC0: Security disabled/not Frozen state.

**Transition SEC3:SEC4:** When a SECURITY FREEZE LOCK command is received, the device shall transition to the SEC4: Unlocked/Frozen state.

**SEC4: Unlocked/ Frozen:** This mode shall be entered when the receives a SECURITY FREEZE LOCK command while in Unlocked/not Frozen state.

In this state, the device is capable of responding to all commands except those indicated in Table 8 Frozen column. The device shall remain in this state until the device is powered-down.

**Table 8 – Security mode command actions**

<b>Command</b>	<b>Locked</b>	<b>Unlocked</b>	<b>Frozen</b>
CHECK POWER MODE	Executable	Executable	Executable
CFA REQUEST EXTENDED ERROR CODE	Executable	Executable	Executable
CFA ERASE SECTORS	Command aborted	Executable	Executable
CFA TRANSLATE SECTOR	Executable	Executable	Executable
CFA WRITE MULTIPLE WITHOUT ERASE	Command aborted	Executable	Executable
CFA WRITE SECTORS WITHOUT ERASE	Command aborted	Executable	Executable
DEVICE RESET	Executable	Executable	Executable
DOWNLOAD MICROCODE	Executable	Executable	Executable
EXECUTE DEVICE DIAGNOSTIC	Executable	Executable	Executable
FLUSH CACHE	Command aborted	Executable	Executable
GET MEDIA STATUS	Command aborted	Executable	Executable
IDENTIFY DEVICE	Executable	Executable	Executable
IDENTIFY PACKET DEVICE	Executable	Executable	Executable
IDLE	Executable	Executable	Executable
IDLE IMMEDIATE	Executable	Executable	Executable
INITIALIZE DEVICE PARAMETERS	Executable	Executable	Executable
MEDIA EJECT	Command aborted	Executable	Executable
MEDIA LOCK	Command aborted	Executable	Executable
MEDIA UNLOCK	Command aborted	Executable	Executable
NOP	Executable	Executable	Executable
PACKET	Command aborted	Executable	Executable
READ BUFFER	Executable	Executable	Executable
READ DMA	Command aborted	Executable	Executable
READ DMA QUEUED	Command aborted	Executable	Executable
READ MULTIPLE	Command aborted	Executable	Executable
READ NATIVE MAX ADDRESS	Executable	Executable	Executable
READ SECTORS	Command aborted	Executable	Executable
READ VERIFY SECTORS	Command aborted	Executable	Executable
SECURITY DISABLE PASSWORD	Command aborted	Executable	Command aborted
SECURITY ERASE PREPARE	Executable	Executable	Executable
SECURITY ERASE UNIT	Executable	Executable	Command aborted
SECURITY FREEZE LOCK	Command aborted	Executable	Executable
SECURITY SET PASSWORD	Command aborted	Executable	Command aborted
SECURITY UNLOCK	Executable	Executable	Command aborted
SEEK	Executable	Executable	Executable
SERVICE	Command aborted	Executable	Executable
SET FEATURES	Executable	Executable	Executable
SET MAX ADDRESS	Command aborted	Executable	Executable
SET MULTIPLE MODE	Executable	Executable	Executable
SLEEP	Executable	Executable	Executable
SMART DISABLE OPERATIONS	Executable	Executable	Executable
SMART ENABLE/DISABLE AUTOSAVE	Executable	Executable	Executable
SMART ENABLE OPERATIONS	Executable	Executable	Executable
SMART EXECUTE OFF-LINE IMMEDIATE	Executable	Executable	Executable
SMART READ DATA	Executable	Executable	Executable
SMART READ LOG SECTOR	Executable	Executable	Executable
SMART RETURN STATUS	Executable	Executable	Executable
SMART SAVE ATTRIBUTE VALUES	Executable	Executable	Executable
SMART WRITE LOG SECTOR	Executable	Executable	Executable
STANDBY	Executable	Executable	Executable
STANDBY IMMEDIATE	Executable	Executable	Executable
WRITE BUFFER	Executable	Executable	Executable
WRITE DMA	Command aborted	Executable	Executable
WRITE DMA QUEUED	Command aborted	Executable	Executable
WRITE MULTIPLE	Command aborted	Executable	Executable
WRITE SECTORS	Command aborted	Executable	Executable

## **6.14 Self-monitoring, analysis, and reporting technology feature set**

The intent of self-monitoring, analysis, and reporting technology (the SMART feature set) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in the IDENTIFY DEVICE response.

Devices that implement the PACKET Command feature set shall not implement the SMART feature set as described in this subclause. Devices that implement the PACKET Command feature set and SMART shall implement SMART as defined by the command packet set implemented by the device.

### **6.14.1 Device SMART data structure**

SMART feature set capability and status information for the device are stored in the device SMART data structure. The off-line data collection capability and status data stored herein may be useful to the host if the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented (see 8.41.4).

### **6.14.2 On-line data collection**

Collection of SMART data in an “on-line” mode shall have no impact on device performance. The SMART data that is collected or the methods by which data is collected in this mode may be different than those in the off-line data collection mode for any particular device and may vary from one device to another.

### **6.14.3 Off-line data collection**

The device shall use off-line mode for data collection and self-test routines that have an impact on performance if the device is required to respond to commands from the host while performing that data collection. This impact on performance may vary from device to device. The data that is collected or the methods by which the data is collected in this mode may be different than those in the on-line data collection mode for any particular device and may vary from one device to another.

### **6.14.4 Threshold exceeded condition**

This condition occurs when the device’s SMART reliability status indicates an impending degrading or fault condition.

### **6.14.5 SMART feature set commands**

These commands use a single command code and are differentiated from one another by the value placed in the Features register (see 8.41).

If the SMART feature set is implemented, the following commands shall be implemented.

- SMART DISABLE OPERATIONS
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATIONS
- SMART RETURN STATUS

If the SMART feature set is implemented, the following commands may be implemented.

- SMART EXECUTE OFF-LINE IMMEDIATE
- SMART READ DATA
- SMART READ LOG SECTOR
- SMART WRITE LOG SECTOR

#### **6.14.6 SMART operation with power management modes**

When used with a host that has implemented the Power Management feature set, a SMART enabled device should automatically save the device accumulated SMART data upon receipt of an IDLE IMMEDIATE, STANDBY IMMEDIATE, or SLEEP command or upon return to an Active or Idle mode from a Standby mode (see 8.41.5).

If a SMART feature set enabled device has been set to utilize the Standby timer, the device should automatically save the device accumulated SMART data prior to going from an Idle mode to the Standby mode or upon return to an Active or Idle mode from a Standby mode.

A device shall not execute any routine to automatically save the device accumulated SMART data while the device is in a Standby or Sleep mode.

#### **6.14.7 SMART device error log reporting**

Logging of reported errors is an optional SMART feature. If error logging is supported by a device, it is indicated in byte 370 of the SMART READ DATA command response. If error logging is supported, the device shall provide information on the last five errors that the device reported as described in the SMART READ LOG SECTOR command (see 8.41.6). The device may also provide additional vendor specific information on these reported errors.

If error logging is supported, it shall not be disabled when SMART is disabled. Error log information shall be gathered at all times the device is powered on except that logging of errors when in a reduced power mode is optional. If errors are logged when in a reduced power mode, the reduced power mode shall not change. Disabling SMART shall disable the delivering of error log information via the SMART READ LOG SECTOR command.

If a device receives a firmware modification, all error log data shall be discarded and the device error count for the life of the device shall be reset to zero.

### **6.15 Host Protected Area feature set**

A reserved area for data storage outside the normal operating system file system is required for several specialized applications. Systems may wish to store configuration data or save memory to the device in a location that the operating systems cannot change. The Host Protected Area feature set allows a portion of the device to be reserved for such an area when the device is initially configured. A device that implements the Host Protected Area feature set shall implement the following minimum set of commands:

- READ NATIVE MAX ADDRESS
- SET MAX ADDRESS

If the Host Protected Area feature set is supported, the device shall indicate so in the IDENTIFY DEVICE response.

The READ NATIVE MAX ADDRESS command allows the host to determine the maximum native address space of the device even when a protected area has been allocated.

The SET MAX ADDRESS command allows the host to redefine the maximum address of the user accessible address space. That is, when the SET MAX ADDRESS command is issued with a maximum

address less than the native maximum address, the device reduces the user accessible address space to the maximum set, providing a protected area above that maximum address. The SET MAX ADDRESS command shall be immediately preceded by a READ NATIVE MAX ADDRESS command. After the SET MAX ADDRESS command has been issued, the device shall report only the reduced user address space in response to an IDENTIFY DEVICE command in words 1, 54, 57, 58, 60, and 61. Any read or write command to an address above the maximum address specified by the SET MAX ADDRESS command shall cause command completion with the IDNF bit set to one and ERR set to one, or command aborted. A volatility bit in the Sector Count register allows the host to specify if the maximum address set is preserved across power-up or hardware reset cycles. On power up or hardware reset the device maximum address returns to the last non-volatile address setting regardless of subsequent volatile SET MAX ADDRESS commands. If the SET MAX ADDRESS command is issued with a value that exceeds the native maximum address command aborted shall be returned.

Typical use of these commands would be:

#### On Reset

- a) BIOS receives control after a system reset;
- b) BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
- c) BIOS issues a SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
- d) BIOS reads configuration data from the highest area on the disk;
- e) BIOS issues a READ NATIVE MAX ADDRESS command followed by a SET MAX ADDRESS command to reset the device to the size of the file system.

#### On Save to Disk

- a) BIOS receives control prior to shut down;
- b) BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
- c) BIOS issues a volatile SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
- d) Memory is copied to the reserved area;
- e) Shut down completes;
- f) On power on or hardware reset the device max address returns to the last non-volatile setting.

These commands are intended for use only by system BIOS or other low level boot time process. The process should select a single addressing translation, CHS or LBA, for all SET MAX ADDRESS and READ NATIVE MAX ADDRESS commands. Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device. Devices should command aborted a second non-volatile SET MAX ADDRESS command after a power on or hardware reset

### 6.15.1 Host protected area orphan sectors

Issuing a SET MAX ADDRESS command with an LBA value may create orphan sectors just as an INITIALIZE DEVICE PARAMETERS command may create such sectors (see B.3). If the SET MAX ADDRESS LBA value does not correspond to a cylinder boundary, orphan sectors are created. The device shall report the CHS boundary just below the requested LBA value in word 1. Sectors above this cylinder boundary are orphan sectors and the device may or may not allow access to them in CHS translation.

## 6.16 CFA feature set

The CompactFlash Association (CFA) feature set provides support for solid state memory devices. The commands provided for the CFA feature set are:

- CFA REQUEST EXTENDED ERROR CODE
- CFA WRITE SECTORS WITHOUT ERASE
- CFA ERASE SECTORS
- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA TRANSLATE SECTOR

Devices reporting the value 848Ah in IDENTIFY DEVICE data word 0 or devices having bit 2 of IDENTIFY DEVICE data word 83 set to one shall support the CFA feature Set. If the CFA feature set is implemented, all five commands shall be implemented.

Support of DMA commands is optional for devices that support the CFA feature set.

The CFA ERASE SECTORS command preconditions the sector for a subsequent CFA WRITE SECTORS WITHOUT ERASE or CFA WRITE MULTIPLE WITHOUT ERASE command to achieve higher performance during the write operation. The CFA TRANSLATE SECTOR command provides information about a sector such as the number of write cycles performed on that sector and an indication of the sector's erased precondition. The CFA REQUEST EXTENDED ERROR CODE command provides more detailed error information.

## 6.17 Removable Media Status Notification and Removable Media feature sets

This section describes two feature sets that secure the media in removable media storage devices using the ATA/ATAPI interface protocols. First, the Removable Media Status Notification feature set is intended for use in both devices implementing the PACKET command feature set and those not implementing the PACKET command feature set. Second, the Removable Media feature set is intended for use only in devices not implementing the PACKET command feature set. Only one of these feature sets is enabled at any time. If the Removable Media Status Notification feature set is in use then the Removable Media feature set is disabled and vice versa.

The reasons for implementing the Removable Media Status Notification feature Set or the Removable Media feature set are:

- to prevent data loss caused by writing to new media while still referencing the previous media's information.
- to prevent data loss by locking the media until completion of a cached write.
- to prevent removal of the media by unauthorized persons.

### 6.17.1 Removable Media Status Notification feature set

The Removable Media Status Notification feature set is the preferred feature set for securing the media in removable media storage devices. This feature set uses the SET FEATURES command to enable Removable Media Status Notification. Removable Media Status Notification gives the host system maximum control of the media. The host system determines media status by issuing the GET MEDIA STATUS command and controls the device eject mechanism via the MEDIA EJECT command (for devices not implementing the PACKET command feature set) or the START/STOP UNIT command (for devices implementing the PACKET command feature set, [see SCSI Primary Commands, NCITS 301-1997](#)). While Removable Media Status Notification is enabled devices not implementing the PACKET command feature set execute MEDIA LOCK and MEDIA UNLOCK commands without changing the media lock state (no-operation). While Removable Media Status Notification is enabled the eject button does not eject the media.

Removable Media Status Notification is persistent through medium removal and insertion and is only disabled via the SET FEATURES command, hardware reset, software reset, the DEVICE RESET

command, the EXECUTE DEVICE DIAGNOSTIC command, or power on reset. Removable Media Status Notification shall be re-enabled after any of the previous reset conditions occur. All media status is reset when Removable Media Status Notification is disabled because a reset condition occurred. Any pending media change or media change request is cleared when the Removable Media Status Notification reset condition occurs.

The following task file commands are defined to implement the Removable Media Status Notification feature set.

- GET MEDIA STATUS
- MEDIA EJECT
- SET FEATURES (Enable media status notification)
- SET FEATURES (Disable media status notification)

NOTE – Devices implementing the PACKET command feature set control the media eject mechanism via the START/STOP UNIT packet command.

The preferred sequence of events to use the Removable Media Status Notification feature set is as follows:

- a) Host system checks whether or not the device implements the PACKET command feature set via the device signature in the task file registers.
- b) Host system issues the IDENTIFY DEVICE command or the IDENTIFY PACKET DEVICE command and checks that the device is a removable media device and that the Removable Media Status Notification feature set is supported.
- c) Host system uses the SET FEATURES command to enable Media Status Notification that gives control of the media to the host. At this time the host system checks the Cylinder High register to determine if :
  - the device is capable of locking the media.
  - the device is capable of power ejecting the media.
  - Media Status Notification was enabled prior to this command.
- d) Host system periodically checks media status using the GET MEDIA STATUS command to determine if any of the following events occurred:
  - no media is present in the device (NM).
  - media was changed since the last command (MC).
  - a media change request has occurred (MCR).
  - media is write protected (WP).

### 6.17.2 Removable Media feature set

The Removable Media feature set is intended only for devices not implementing the PACKET command feature set. This feature set operates with Media Status Notification disabled. The MEDIA LOCK and MEDIA UNLOCK commands are used to secure the media and the MEDIA EJECT command is used to remove the media. While the media is locked the eject button does not eject the disk. Media status is determined by checking the media status bits returned by the MEDIA LOCK and MEDIA UNLOCK commands.

Power up reset, hardware reset, and the EXECUTE DEVICE DIAGNOSTIC command clear the Media Lock (LOCK) state and the Media Change Request (MCR) state. Software reset clears the Media Lock (LOCK) state, clears the Media Change Request (MCR) state, and preserves the Media Change (MC) state.

The following commands are defined to implement the Removable Media feature set.

- MEDIA EJECT
- MEDIA LOCK
- MEDIA UNLOCK

The preferred sequence of events to use the Removable Media feature set is as follows:



- a) Host system checks whether or not the device implements the PACKET command feature set via the device signature in the task file registers.
- b) Host system issues the IDENTIFY DEVICE command and checks that the device is a removable media device and that the Removable Media feature set is supported.
- c) Host system periodically issues MEDIA LOCK commands to determine if:
  - no media is present in the device (NM) - media is locked if present.
  - a media change request has occurred (MCR).

## 6.18 Power-Up In Standby feature set

The optional Power-Up In Standby feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices. This optional feature set may be enabled or disabled via the SET FEATURES command or may be enabled by use of a jumper or similar means, or both. When enabled by a jumper, the feature set shall not be disabled via the SET FEATURES command. The IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response indicates whether this feature set is implemented and/or enabled.

The enabling of this feature set shall be persistent after power-down and power-up. When this feature set is enabled, the device shall power-up into Standby.

A device may implement a SET FEATURES subcommand that notifies the device to spin-up to the Active state when the device has powered-up into Standby. If the device implements this SET FEATURES subcommand and power-up into Standby is enabled, the device shall remain in Standby until the SET FEATURES subcommand is received. If the device implements this SET FEATURES subcommand, the fact that the feature is implemented is reported in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If the device implements this SET FEATURES subcommand and power-up into Standby is enabled, when an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is received while the device is in Standby as a result of powering up into Standby, the device shall respond to the command remaining in Standby (without spinning-up). If the device has IDENTIFY DEVICE or IDENTIFY PACKET DEVICE that requires access to the media, the device shall set word 0 bit 2 to one to indicate that the response is incomplete. At a minimum, words 0 and 2 shall be correctly reported. Those fields that cannot be provided shall be filled with zero. Once the full IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response data has been accessed, a full response shall be returned until the next power-down/power-up sequence has taken place.

If the device does not implement the SET FEATURES subcommand to spin-up the device after power-up and power-up into Standby is enabled, the device shall spin-up upon receipt of the first command that requires the device to access the media.

## 7 Interface register definitions and descriptions

### 7.1 Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, when a register is written the value is written to the register of both devices. The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are connected on the cable, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTIC command, only the selected device executes the command. Both devices shall execute an EXECUTE

DEVICE DIAGNOSTIC command regardless of which device is selected, and Device 1 shall post status to Device 0 via PDIAG-.

When the Device Control register is written, both devices respond to the write regardless of which device is selected (see 7.9.5).

Devices are selected by the DEV bit in the Device/Head register (see 7.10). When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When **two** devices are **connected to the cable**, one shall be set as Device 0 and the other as Device 1.

For register access protocols and timing see clauses 9 and 10.

When the host initiates a register or Data port read or write cycle by asserting then negating either DIOW- or DIOR-, the device(s) on the ATA interface shall determine how to respond and what action(s), if any, are to be taken. The following text and tables describe this decision process.

The device response begins with these steps:

- 1) For a device that is not in Sleep mode, see Table 9.
- 2) If DMACK- is asserted, a device in Sleep mode shall ignore all DIOW-/DIOR- activity. If DMACK- is not asserted, a device in Sleep mode shall respond as described in Table 14 if the device does not implement the **PACKET Command feature set** or Table 15 if the device does implement the **PACKET Command feature set**.

**Table 9 – Device response to DIOW-/DIOR-**

Is the device selected? (see note 1)	Is DMACK- asserted?	Action/Response
No	No	See Table 10
No	Yes	DIOW-/DIOR- cycle is ignored (possible DMA transfer with the other device)
Yes	No	See Table 11
Yes	Yes	See Table 12 (see note 2)
Device 1 is selected but there is no device 1, Device 0 will respond for device 1.	No	See Table 13 and 9.16.1
Device 1 is selected but there is no device 1, Device 0 will respond for device 1.	Yes	DIOW-/DIOR- cycle is ignored (possible malfunction of the host)
NOTES –		
1 Device selected means that the DEV bit in the Device/Head register matches the logical <b>device number</b> of the device.		
2 Applicable only to Multiword DMA, not applicable to Ultra DMA.		

**Table 10 – Device is not selected, DMACK- is not asserted**

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
N	N	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	Z	X	X	
N	A	A	N	X	X	Z	X	X	
N	A	A	A	N	W	Z	X	X	Place new data into the Device Control register and respond to the new values of the nIEN and SRST bits.
N	A	A	A	N	R	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	A	A	A	X	Z	X	X	
A	N	N	N	N	X	Z	X	X	
A	N	N	N	A	W	Z	0	X	Place new data into the Feature register.
A	N	N	N	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	N	N	A	R	Z	X	X	
A	N	N	A	N	W	Z	0	X	Place new data into the Sector Count register.
A	N	N	A	N	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	N	A	N	R	Z	X	X	
A	N	N	A	A	W	Z	0	X	Place new data into the Sector Number register.
A	N	N	A	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	N	A	A	R	Z	X	X	
A	N	A	N	N	W	Z	0	X	Place new data into the Cylinder Low register.
A	N	A	N	N	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	N	N	R	Z	X	X	
A	N	A	N	A	W	Z	0	X	Place new data into the Cylinder High register.
A	N	A	N	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	N	A	R	Z	X	X	
A	N	A	A	N	W	Z	0	X	Place new data into the Device/Head register. Respond to the new value of the DEV bit.
A	N	A	A	N	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	A	N	R	Z	X	X	
A	N	A	A	A	W	Z	0	X	Place new data into the Command register. Do not respond unless the command is EXECUTE DEVICE DIAGNOSTICS.
A	N	A	A	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	A	A	R	Z	X	X	
A	A	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.

NOTE – 1. Except in the DIOx- column, A = asserted, N = negated, X = don't care.

2. In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

3. Device selected means that the DEV bit in the Device/Head register matches the logical **device number** of the device.

Table 11 – Device is selected, DMACK- is not asserted

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
N	N	X	X	X	X	X	X	X	DIOw-/DIOr- cycle is ignored.
N	A	N	X	X	X	X	X	X	
N	A	A	N	X	X	X	X	X	
N	A	A	A	N	W	X	X	X	Place new data into the Device Control register and respond to the new values of the nIEN and SRST bits.
N	A	A	A	N	R	X	X	X	Place Status register contents on the data bus (do not change the Interrupt Pending state).
N	A	A	A	A	X	X	X	X	DIOw-/DIOr- cycle is ignored.
A	N	N	N	N	X	X	0	0	
A	N	N	N	N	X	X	0	1	PIO data transfer for this device, a 16-bit data word is transferred via the Data register.
A	N	N	N	N	X	X	1	X	DIOw-/DIOr- cycle is ignored.
A	N	N	N	A	W	X	0	0	Place new data into the Features register.
A	N	N	N	A	W	X	0	1	DIOw- is ignored, this is a malfunction of the host.
A	N	N	N	A	W	X	1	X	DIOw- is ignored.
A	N	N	N	A	R	X	0	X	Place the contents of the Error register on the data bus.
A	N	N	N	A	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	N	A	N	W	X	0	0	Place new data into the Sector Count register.
A	N	N	A	N	W	X	0	1	DIOw- is ignored, this is a malfunction of the host.
A	N	N	A	N	W	X	1	X	DIOw- is ignored.
A	N	N	A	N	R	X	0	X	Place the contents of the Sector Count register on the data bus.
A	N	N	A	N	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	N	A	A	W	X	0	0	Place new data into the Sector Number register.
A	N	N	A	A	W	X	0	1	DIOw- is ignored, this is a malfunction of the host.
A	N	N	A	A	W	X	1	X	DIOw- is ignored.
A	N	N	A	A	R	X	0	X	Place the contents of the Sector Number register on the data bus.
A	N	N	A	A	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	N	N	W	X	0	0	Place new data into the Cylinder Low register.
A	N	A	N	N	W	X	0	1	DIOw- is ignored, this is a malfunction of the host.
A	N	A	N	N	W	X	1	X	DIOw- is ignored.
A	N	A	N	N	R	X	0	X	Place the contents of the Cylinder Low register on the data bus.
A	N	A	N	N	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	N	A	W	X	0	0	Place new data into the Cylinder High register.
A	N	A	N	A	W	X	0	1	DIOw- is ignored, this is a malfunction of the host.

(continued)

**Table 11 – Device is selected, DMACK- is not asserted(continued)**

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
A	N	A	N	A	W	X	1	X	DIOW- is ignored.
A	N	A	N	A	R	X	0	X	Place the contents of the Cylinder High register on the data bus.
A	N	A	N	A	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	A	N	W	X	0	0	Place new data into the Device/Head register. Respond to the new value of the DEV bit.
A	N	A	A	N	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	A	A	N	W	X	1	X	DIOW- is ignored.
A	N	A	A	N	R	X	0	X	Place the contents of the Device/Head register on the data bus.
A	N	A	A	N	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	A	A	W	X	0	0	Place new data into the Command register and respond to the new command (exit the Interrupt Pending State).
A	N	A	A	A	W	X	0	1	DIOW- is ignored, unless the device supports DEVICE RESET. If the device supports the DEVICE RESET command, exit the Interrupt Pending state.
A	N	A	A	A	W	X	1	X	
A	N	A	A	A	R	X	X	X	Place contents of Status register on the data bus and exit the Interrupt Pending state.
A	A	X	X	X	X	X	X	X	DIOW-/DIOR- cycle is ignored.

NOTE – 1. Except in the DIOx- column, A = asserted, N = negated, X = don't care.  
 2. In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.  
 3. Device selected means that the DEV bit in the Device/Head register matches the logical **device number** of the device.

(concluded)

**Table 12 – Device is selected, DMACK- is asserted (for Multiword DMA only)**

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
X	X	X	X	X	X	Z	0	0	DIOW-/DIOR- cycle is ignored(possible malfunction of the host).
X	X	X	X	X	X	Z	1	X	
X	X	X	X	X	X	Z	0	1	
X	X	X	X	X	X	N	0	0	
N	N	X	X	X	X	N	1	X	This could be the final DIOW-/DIOR- of a Multiword DMA transfer burst, or a possible malfunction of the host that is ignored.
N	N	X	X	X	X	N	0	X	
N	N	X	X	X	X	A	1	X	DMA transfer for this device, a 16-bit word of data is transferred via the Data Port.
N	N	X	X	X	X	A	0	1	
X	A	X	X	X	X	X	X	X	DIOW-/DIOR- cycle is ignored(possible Malfunction of the host).
A	X	X	X	X	X	X	X	X	

NOTE – 1. Except in the DIOx- column, A = asserted, N = negated, X = don't care.  
 2. In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.  
 3. Device selected means that the DEV bit in the Device/Head register matches the logical **device number** of the device.

**Table 13 –Device 1 is selected and Device 0 is responding for Device 1**

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
N	N	X	X	X	X	Z	0	0	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	Z	0	0	
N	A	A	N	X	X	X	0	0	
N	A	A	A	N	W	X	0	0	Place new data into the Device 0 Device Control register and respond to the new values of the nIEN and SRST bits.
N	A	A	A	N	R	X	0	0	Place 00H on the data bus.
N	A	A	A	A	X	X	0	0	DIOW-/DIOR- cycle is ignored.
A	N	N	N	N	X	X	0	0	
A	N	N	N	A	W	X	0	0	Place new data into the Device 0 Feature register.
A	N	N	N	A	R	X	0	0	Place the contents of the Device 0 Error register on the data bus.
A	N	N	A	N	W	X	0	0	Place new data into Device 0 Sector Count register.
A	N	N	A	N	R	X	0	0	Place the contents of the Device 0 Sector Count register on the data bus.
A	N	N	A	A	W	X	0	0	Place new data into Device 0 Sector Number register.
A	N	N	A	A	R	X	0	0	Place the contents of the Device 0 Sector Number register on the data bus.
A	N	A	N	N	W	X	0	0	Place new data into Device 0 Cylinder Low register.
A	N	A	N	N	R	X	0	0	Place the contents of the Device 0 Cylinder Low register on the data bus.
A	N	A	N	A	W	X	0	0	Place new data into Device 0 Cylinder High register.
A	N	A	N	A	R	X	0	0	Place the contents of the Device 0 Cylinder High register on the data bus.
A	N	A	A	N	W	X	0	0	Place new data into the Device 0 Device/Head register. Respond to the new value of the DEV bit.
A	N	A	A	N	R	X	0	0	Place the contents of the Device 0 Device/Head register, with DEV bit set to 1, on the data bus.
A	N	A	A	A	W	X	0	0	Place new data into the Command register of Device 0. Do not respond unless the command is EXECUTE DEVICE DIAGNOSTICS.
A	N	A	A	A	R	X	0	0	Place 00H on the data bus.
A	A	X	X	X	X	X	0	0	DIOW-/DIOR- cycle is ignored.

NOTE – 1. Except in the DIOx- column, A = asserted, N = negated, X = don't care.  
2. In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.  
3. Device selected means that the DEV bit in the Device/Head register matches the logical **device number** of the device.

**Table 14 – Device is in Sleep mode, DEVICE RESET is not implemented, DMACK- is not asserted**

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
N	N	X	X	X	X	Z	X	X	DIOw-/DIOr- cycle is ignored.
N	A	N	X	X	X	Z	X	X	
N	A	A	N	X	X	Z	X	X	
N	A	A	A	N	W	Z	X	X	Place new data into the Device Control register SRST bit and respond only if SRST bit is 1.
N	A	A	A	N	R	Z	X	X	DIOw-/DIOr- cycle is ignored.
N	A	A	A	A	X	Z	X	X	
A	N	X	X	X	X	Z	X	X	
A	A	X	X	X	X	Z	X	X	

NOTE – 1. Except in the DIOx- column, A = asserted, N = negated, X = don't care.  
2. In the DIOx- column, R = DIOR- asserted, W = DIOw- asserted, X = either DIOR- or DIOw- is asserted.  
3. Device selected means that the DEV bit in the Device/Head register matches the logical **device number** of the device.

**Table 15 – Device is in Sleep mode, DEVICE RESET is implemented, DMACK- is not asserted**

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
N	N	X	X	X	X	Z	X	X	DIOw-/DIOr- cycle is ignored.
N	A	N	X	X	X	Z	X	X	
N	A	A	N	X	X	Z	X	X	
N	A	A	A	N	W	Z	X	X	Place new data into the Device Control register SRST bit and respond only if SRST bit is 1.
N	A	A	A	N	R	Z	X	X	DIOw-/DIOr- cycle is ignored.
N	A	A	A	A	X	Z	X	X	
A	N	N	X	X	X	Z	X	X	
A	N	A	N	X	X	Z	X	X	
A	N	A	A	N	W	Z	X	X	Place new data into the Device/Head register DEV bit.
A	N	A	A	N	R	Z	X	X	DIOR- cycle is ignored.
A	N	A	A	A	W	Z	X	X	DIOw- cycle is ignored unless the device is selected and the command is DEVICE RESET.
A	N	A	A	A	R	Z	X	X	DIOR- cycle is ignored.
A	A	X	X	X	X	Z	X	X	DIOw-/DIOr- cycle is ignored

NOTE – 1. Except in the DIOx- column, A = asserted, N = negated, X = don't care.  
2. In the DIOx- column, R = DIOR- asserted, W = DIOw- asserted, X = either DIOR- or DIOw- is asserted.  
3. Device selected means that the DEV bit in the Device/Head register matches the logical **device number** of the device.

## 7.2 I/O register descriptions

Communication to or from the device is through registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR-, and DIOw-). CS0- and CS1- both asserted or negated is an invalid (not used) address except when both are negated during a DMA data transfer. When CS0- and CS1- are both asserted or both negated and a DMA transfer is not in progress, the device shall hold DD (15:0) in the released state and ignore transitions on DIOR- and DIOw-. When CS0- is negated and CS1- is asserted only DA (2:0) with a value of 6h is valid. During invalid combinations of assertion and negation of CS0-, CS1-, DA0, DA1, and DA2, a device shall keep DD(15:0) in the high impedance state and ignore transitions on DIOR- and DIOw-. Valid register addresses are described in the clauses defining the registers.

The Command Block registers are used for sending commands to the device or posting status from the device. These registers include the Cylinder High, Cylinder Low, Device/Head, Sector Count, Sector Number, Command, Status, Features, Error, and Data registers. The Control Block registers are used for device control and to post alternate status. These registers include the Device Control and Alternate Status registers.

Each register description in the following clauses contain the following format:

Address - the CS and DA address of the register.

Direction - indicates if the register is read/write, read only, or write only from the host.

Access restrictions - indicates when the register may be accessed.

Effect - indicates the effect of accessing the register.

Functional description - describes the function of the register.

Field/bit description - describes the content of the register.

## 7.3 Alternate Status register

### 7.3.1 Address

CS1	CS0	DA2	DA1	DA0
A	N	A	A	N
A = asserted, N = negated				

### 7.3.2 Direction

This register is read only. If this address is written to by the host, the Device Control register is written.

### 7.3.3 Access restrictions

When the BSY bit is set to one, the other bits in this register shall not be used. The entire contents of this register are not valid while the device is in Sleep mode.

### 7.3.4 Effect

Reading this register shall not clear a pending interrupt.

### 7.3.5 Functional description

This register contains the same information as the Status register in the command block.

See 7.15 for definitions of the bits in this register.

## 7.4 Command register

### 7.4.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	A	A
A = asserted, N = negated				

### 7.4.2 Direction

This register is write only. If this address is read by the host, the Status register is read.



### 7.4.3 Access restrictions

For all commands except DEVICE RESET, this register shall only be written when BSY and DRQ are both equal to zero and DMACK- is not asserted. The contents of this register when read may not be valid while a device is in the Sleep mode. If written when BSY or DRQ is set to one, the results of writing the Command register are indeterminate except for the DEVICE RESET command.

### 7.4.4 Effect

Command processing begins when this register is written. The content of the Command Block registers become parameters of the command when this register is written. Writing this register clears any pending interrupt condition.

### 7.4.5 Functional description

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are summarized in the tables in informative annex E.

### 7.4.6 Field/bit description

7	6	5	4	3	2	1	0
Command Code							

## 7.5 Cylinder High register

### 7.5.1 Address

<b>CS1</b>	<b>CS0</b>	<b>DA2</b>	<b>DA1</b>	<b>DA0</b>
N	A	A	N	A
A = asserted, N = negated				

### 7.5.2 Direction

This register is read/write.

### 7.5.3 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

### 7.5.4 Effect

The content of this register becomes a command parameter when the Command register is written.

### 7.5.5 Functional description

The content of this register is command dependent (see clause 8).

## 7.6 Cylinder Low register

### 7.6.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	N	N
A = asserted, N = negated				

### 7.6.2 Direction

This register is read/write.

### 7.6.3 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of the this register are not valid while a device is in the Sleep mode.

### 7.6.4 Effect

The content of this register becomes a command parameter when the Command register is written.

### 7.6.5 Functional description

The content of this register is command dependent (see clause 8).

## 7.7 Data port

### 7.7.1 Address

When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16-bits wide.

CS1	CS0	DA2	DA1	DA0
N	N	X	X	X
A = asserted, N = negated, X = don't care				

### 7.7.2 Direction

This port is read/write.

### 7.7.3 Access restrictions

This port shall be accessed for host DMA data transfers only when DMACK- and DMARQ are asserted.

### 7.7.4 Effect

DMA out data transfers are processed by a series of reads to this port, each read transferring the data that follows the previous read. DMA in data transfers are processed by a series of writes to this port, each write transferring the data that follows the previous write. The results of a read during a DMA in or a write during a DMA out are indeterminate.

### 7.7.5 Functional description

The data port is 16-bits in width.

### 7.7.6 Field/bit description

15	14	13	12	11	10	9	8
Data(15:8)							
7	6	5	4	3	2	1	0
Data(7:0)							

## 7.8 Data register

### 7.8.1 Address

<b>CS1</b>	<b>CS0</b>	<b>DA2</b>	<b>DA1</b>	<b>DA0</b>
N	A	N	N	N
A = asserted, N = negated				

### 7.8.2 Direction

This register is read/write.

### 7.8.3 Access restrictions

This register shall be accessed for host PIO data transfer only when DRQ is set to one and DMACK- is not asserted. The contents of this register are not valid while a device is in the Sleep mode.

### 7.8.4 Effect

PIO out data transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO in data transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a PIO in or a write during a PIO out are indeterminate.

### 7.8.5 Functional description

The data register is 16-bits wide.

### 7.8.6 Field/bit description

15	14	13	12	11	10	9	8
Data(15:8)							
7	6	5	4	3	2	1	0
Data(7:0)							

## 7.9 Device Control register

### 7.9.1 Address

<b>CS1</b>	<b>CS0</b>	<b>DA2</b>	<b>DA1</b>	<b>DA0</b>
A	N	A	A	N
A = asserted, N = negated				

## 7.9.2 Direction

This register is write only. If this address is read by the host, the Alternate Status register is read.

## 7.9.3 Access restrictions

This register shall only be written when DMACK- is not asserted.

## 7.9.4 Effectiveness

The content of this register shall take effect when written.

## 7.9.5 Functional description

This register allows a host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When the Device Control register is written, both devices respond to the write regardless of which device is selected. When the SRST bit is set to one, both devices shall perform the software reset protocol. **The device shall respond to the SRST bit when in the SLEEP mode.** When the nIEN bit is set or cleared, both devices shall disable or enable assertion of the INTRQ signal.

## 7.9.6 Field/bit description

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved.
- SRST is the host software reset bit (see 9.2).
- nIEN is the enable bit for the device interrupt to the host. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer and shall be asserted or negated by the device as appropriate. When the nIEN bit is set to one, or the device is not selected, the INTRQ signal shall be in a high impedance state.
- Bit 0 shall be cleared to zero.

## 7.10 Device/Head register

### 7.10.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	A	N
A = asserted, N = negated				

### 7.10.2 Direction

This register is read/write.

### 7.10.3 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. For devices not implementing the **PACKET Command feature set**, the contents of this register are not valid while a device is in the Sleep mode. For devices implementing the **PACKET Command feature set**, the contents of this register are valid while the device is in Sleep mode.

#### 7.10.4 Effect

The DEV bit becomes effective when this register is written by the host or the signature is set by the device. All other bits in this register become a command parameter when the Command register is written.

#### 7.10.5 Functional description

Bit 4, DEV, in this register selects the device. Other bits in this register are command dependent (see clause 8).

#### 7.10.6 Field/bit description

7	6	5	4	3	2	1	0
obsolete	#	obsolete	DEV	#	#	#	#

- obsolete - These bits are obsolete.

NOTE – Some hosts set these bits to one. Devices shall ignore these bits.

- # - The content of these bits is command dependent (see clause 8).
- DEV - Device select. Cleared to zero selects Device 0. Set to one selects Device 1.

### 7.11 Error register

#### 7.11.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	N	A
A = asserted, N = negated				

#### 7.11.2 Direction

This register is read only. If this address is written to, the Features register is written.

#### 7.11.3 Access restrictions

The contents of this register shall be valid when BSY and DRQ equal zero and ERR equals one. The contents of this register shall be valid upon completion of power on, or after a hardware or software reset, or after command completion of an EXECUTE DEVICE DIAGNOSTICS or DEVICE RESET command. The contents of this register are not valid while a device is in the Sleep mode.

#### 7.11.4 Effect

None.

#### 7.11.5 Functional description

This register contains status for the current command.

Following a power on, a hardware or software reset (see 9.1), or command completion of an EXECUTE DEVICE DIAGNOSTIC (see 8.9) or DEVICE RESET command (see 8.7), this register contains a diagnostic code .

At command completion of any command except EXECUTE DEVICE DIAGNOSTIC, the contents of this register are valid when the ERR bit is equal to one in the Status register.

### 7.11.6 Field/bit description

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
#	#	#	#	#	ABRT	#	#

- Bit 2 - ABRT (command aborted) is set to one to indicate the requested command has been command aborted because the command code or a command parameter is invalid or some other error has occurred.
- # -The content of this bit is command dependent (see clause 8).

## 7.12 Features register

### 7.12.1 Address

<b>CS1</b>	<b>CS0</b>	<b>DA2</b>	<b>DA1</b>	<b>DA0</b>
N	A	N	N	A
A = asserted, N = negated				

### 7.12.2 Direction

This register is write only. If this address is read by the host, the Error register is read.

### 7.12.3 Access restrictions

This register shall be written only when BSY and DRQ equal zero and DMACK- is not asserted. If this register is written when BSY or DRQ is set to one, the result is indeterminate.

### 7.12.4 Effect

The content of this register becomes a command parameter when the Command register is written.

### 7.12.5 Functional description

The content of this register is command dependent (see clause 8).

## 7.13 Sector Count register

### 7.13.1 Address

<b>CS1</b>	<b>CS0</b>	<b>DA2</b>	<b>DA1</b>	<b>DA0</b>
N	A	N	A	N
A = asserted, N = negated				

### 7.13.2 Direction

This register is read/write.

### 7.13.3 Access restrictions

This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of the this register are not valid while a device is in the Sleep mode.

#### 7.13.4 Effect

The content of this register becomes a command parameter when the Command register is written.

#### 7.13.5 Functional description

The content of this register is command dependent (see clause 8).

### 7.14 Sector Number register

#### 7.14.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	A	A
A = asserted, N = negated				

#### 7.14.2 Direction

This register is read/write.

#### 7.14.3 Access restrictions

This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

#### 7.14.4 Effect

The content of this register becomes a command parameter when the Command register is written.

#### 7.14.5 Functional description

The content of this register is command dependent (see clause 8).

### 7.15 Status register

#### 7.15.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	A	A
A = asserted, N = negated				

#### 7.15.2 Direction

This register is read only. If this address is written to by the host, the Command register is written.

#### 7.15.3 Access restrictions

The contents of this register, except for BSY, shall be ignored when BSY is set equal to one. BSY is valid at all times. The contents of this register are not valid while a device is in the Sleep mode.

### 7.15.4 Effect

Reading this register when an interrupt is pending causes the interrupt to be cleared (see 5.2.9). The host should not read the Status register when an interrupt is expected as this may clear the interrupt before the interrupt can be recognized by the host.

### 7.15.5 Functional description

This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device.

### 7.15.6 Field/bit description

7	6	5	4	3	2	1	0
BSY	DRDY	#	#	DRQ	obsolete	obsolete	ERR

#### 7.15.6.1 BSY (Busy)

BSY is set to one to indicate that the device is busy. After the host has written the Command register the device shall have either the BSY bit set to one, or the DRQ bit set to one, until command completion or the device has performed a bus release for an overlapped command.

The BSY bit shall be set to one by the device:

- 1) after either the negation of RESET- or the setting of the SRST bit to one in the Device Control register;
- 2) after writing the Command register if the DRQ bit is not set to one;
- 3) between blocks of a data transfer during PIO data-in commands before the DRQ bit is cleared to zero;
- 4) after the transfer of a data block during PIO data-out commands before the DRQ bit is cleared to zero;
- 5) during the data transfer of DMA commands either the BSY bit, the DRQ bit, or both shall be set to one;
- 6) after the command packet is received during the execution of a PACKET command.

NOTE – The BSY bit may be set to one and then cleared to zero so quickly, that host detection of the BSY bit being set to one is not certain.

When BSY is set to one, the device has control of the Command Block Registers and:

- 1) a write to a Command Block register by the host shall be ignored by the device except for writing DEVICE RESET command;
- 2) a read from a Command Block register by the host will most likely yield invalid contents except for the BSY bit itself.

The BSY bit shall be cleared to zero by the device:

- 1) after setting DRQ to one to indicate the device is ready to transfer data;
- 2) at command completion;
- 3) upon releasing the bus for an overlapped command;
- 4) when the device is ready to accept commands that do not require DRDY during a power-on, hardware or software reset.

When BSY is cleared to zero, the host has control of the Command Block registers, the device shall:

- 1) not set DRQ to one;
- 2) not change ERR bit;
- 3) not change the content of any other Command Block register;
- 4) set the SERV bit to one when ready to continue an overlapped command that has been bus released.



### 7.15.6.2 DRDY (Device ready)

The DRDY bit shall be cleared to zero by the device:

- 1) when power-on, hardware, or software reset or DEVICE RESET or EXECUTE DEVICE DIAGNOSTIC commands for devices implementing the PACKET command feature set.

When the DRDY bit is cleared to zero, the device shall accept and attempt to execute as described in clause 8

The DRDY bit shall be set to one by the device:

- 1) when the device is capable of accepting all commands for devices not implementing the PACKET command feature set;
- 2) prior to command completion except the DEVICE RESET or EXECUTE DEVICE DIAGNOSTIC command for devices implementing the PACKET feature set.

When the DRDY bit is set to one:

- 1) the device shall accept and attempt to execute all implemented commands;
- 2) devices that implement the Power Management feature set shall maintain the DRDY bit equal to one when they are in the Idle or Standby modes.

### 7.15.6.3 Command dependent

The use of bits marked with # are command dependent (see clause 8). Bit 4 was formerly the DSC (Device Seek Complete) bit.

### 7.15.6.4 DRQ (Data request)

DRQ indicates that the device is ready to transfer a word of data between the host and the device. After the host has written the Command register the device shall either set the BSY bit to one or the DRQ bit to one, until command completion or the device has performed a bus release for an overlapped command.

The DRQ bit shall be set to one by the device:

- 1) when BSY is set to one and data is ready for PIO transfer;
- 2) during the data transfer of DMA commands either the BSY bit , the DRQ bit, or both shall be set to one.

When the DRQ bit is set to one, the host may:

- 1) transfer data via PIO mode;
- 2) transfer data via DMA mode if DMARQ and DMACK- are asserted.

The DRQ bit shall be cleared to zero by the device:

- 1) when the last word of the data transfer occurs;
- 2) when the last word of the command packet transfer occurs for a PACKET command.

When the DRQ bit is cleared to zero, the host may:

- 1) transfer data via DMA mode if DMARQ and DMACK- are asserted and BSY is set to one.

### 7.15.6.5 Obsolete bits

Some bits in this register were defined in previous ATA standards but have been declared obsolete in this standard. These bits are labeled "obsolete".

**7.15.6.6 ERR (Error)**

ERR indicates that an error occurred during execution of the previous command. For the PACKET and SERVICE commands, this bit is defined as CHK and indicates that an exception conditions exists.

The ERR bit shall be set to one by the device:

- 1) when BSY or DRQ is set to one and an error occurs in the executing command.

When the ERR bit is set to one:

- 1) the bits in the Error register shall be valid;
- 2) the device shall not change the contents of the following registers until a new command has been accepted, the SRST bit is set to one or RESET- is asserted:
  - Error register;
  - Cylinder High/Low registers;
  - Sector Count register;
  - Sector Number register;
  - Device/Head register.

The ERR bit shall be cleared to zero by the device:

- 1) when a new command is written to the Command register;
- 2) when the SRST bit is set to one;
- 3) when the RESET- signal is asserted.

When the ERR bit is cleared to zero at the end of a command:

- 1) the content of the Error register shall be ignored by the host.

**8 Command descriptions**

Commands are issued to the device by loading the required registers in the command block with the needed parameters and then writing the command code to the Command register. Required registers are those indicated by a specific content in the Inputs table for the command, i.e., not noted as na or obs.

Each command description in the following clauses contains the following subclauses:

Command code - Indicates the command code for this command.

Feature set - Indicates feature set and if the command is:

- Mandatory - Required to be implemented by devices as specified.
- Optional - Implementation is optional but if implemented shall be implemented as specified.

Protocol - Indicates which protocol is used by the command (see clause 9).

Inputs - Describes the Command Block register data that the host shall supply.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Command	Command Code							
NOTE – na indicates the content of a bit or field is not applicable to the particular command. obs indicates that the use of this bit is obsolete.								

Normal outputs - Describes the Command Block register data returned by the device at the end of a command.

Register	7	6	5	4	3	2	1	0
Error								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Status								
NOTE – na indicates the content of a bit or field is not applicable to the particular command. obs indicates that the use of this bit is obsolete.								

Error outputs - Describes the Command Block register data that shall be returned by the device at command completion with an unrecoverable error.

Register	7	6	5	4	3	2	1	0
Error								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Status								
NOTE – na indicates the content of a bit or field is not applicable to the particular command. obs indicates that the use of this bit is obsolete.								

Prerequisites - Any prerequisite commands or conditions that shall be met before the command is issued.

Description - The description of the command function(s).

## 8.1 CFA ERASE SECTORS

### 8.1.1 Command code

C0h

### 8.1.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

This command code is Vendor Specific for devices not implementing the CFA feature Set.

### 8.1.3 Protocol

Non-data command (see 9.4).

### 8.1.4 Inputs

The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be erased. The Sector Count register specifies the number of sectors to be erased.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	C0h							

**Sector Count -**

number of sectors to be erased. A value of 00h indicates that 256 sectors are to be erased.

**Sector Number -**

starting sector number or LBA address bits (7:0).

**Cylinder Low -**

starting cylinder number bits (7:0) or LBA address bits (15:8).

**Cylinder High -**

starting cylinder number bits (15:8) or LBA address bits (23:16).

**Device/Head -**

bit 6 set to one if LBA address, cleared to zero if CHS address starting head number or LBA address bits (27:24).

**8.1.5 Normal outputs**

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

**Status register**

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.

**8.1.6 Error outputs**

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	MED
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	na	na	na	ERR

**Error Register -**

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established

(see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

MED shall be set to one if a media error is detected.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

ERR shall be set to one if an Error register bit is set to one.

**8.1.7 Prerequisites**

DRDY set equal to one.

**8.1.8 Description**

This command pre-erases and conditions from 1 to 256 sectors as specified in the Sector Count register. This command should be issued in advance of a CFA WRITE SECTORS WITHOUT ERASE or a CFA WRITE MULTIPLE WITHOUT ERASE command to increase the execution speed of the write operation.

**8.2 CFA REQUEST EXTENDED ERROR CODE**

**8.2.1 Command code**

03h

**8.2.2 Feature set**

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

**8.2.3 Protocol**

Non-data command (see 9.4).

**8.2.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Command	03h							

**8.2.5 Normal outputs**

The extended error code written into the Error register is an 8-bit code. Table 16 defines these values.

Register	7	6	5	4	3	2	1	0
Error	Extended error code							
Sector Count	Vendor specific							
Sector Number	Vendor specific							
Cylinder Low	Vendor specific							
Cylinder High	Vendor specific							
Device/Head	obs	na	obs	DEV	Vendor specific			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register -

Extended error code.

Sector Number, Cylinder Low, Cylinder High, Device/Head -

May contain additional information.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.

**Table 16 – Extended error codes**

Extended error code	Description
00h	No error detected / no additional information
01h	Self-test passed
03h	Write / Erase failed
05h	Self-test or diagnostic failed
09h	Miscellaneous error
0Bh	Vendor specific
0Ch	Corrupted media format
0D-0Fh	Vendor specific
10h	ID Not Found / ID Error
11h	Uncorrectable ECC error
14h	ID Not Found
18h	Corrected ECC error
1Dh, 1Eh	Vendor specific
1Fh	Data transfer error / command aborted
20h	Invalid command
21h	Invalid address
22-23h	Vendor specific
27h	Write protect violation
2Fh	Address overflow (address too large)
30-34h	Self-test or diagnostic failed
35h, 36h	Supply or generated voltage out of tolerance
37h, 3Eh	Self-test or diagnostic failed
38h	Corrupted media format
39h	Vendor specific
3Ah	Spare sectors exhausted
3Bh 3Ch, 3Fh	Corrupted media format
3Dh	Vendor specific
All other values	Reserved

## 8.2.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	na	na	na	ERR

Error Register -

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

ERR shall be set to one if an Error register bit is set to one.

## 8.2.7 Prerequisites

DRDY set equal to one.

## 8.2.8 Description

This command provides an extended error code which identifies the cause of an error condition in more detail than is available with Status and Error register values. If the CFA REQUEST EXTENDED ERROR CODE command is the next command issued to the device following the command which ended with an error condition the device shall provide valid extended error code information.

## 8.3 CFA TRANSLATE SECTOR

### 8.3.1 Command code

87h

### 8.3.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

This command code is Vendor Specific for devices not implementing the CFA feature Set.

### 8.3.3 Protocol

PIO data-in command (see 9.5).

### 8.3.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	87h							

Sector Number -

sector number or LBA address bits (7:0).

Cylinder Low -

cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address head number or LBA address bits (27:24).

### 8.3.5 Normal outputs

A 512 byte information table is transferred to the host. Table 17 defines these values.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.



**Table 17 – CFA TRANSLATE SECTOR Information**

Byte	Description
00h	Cylinder number MSB
01h	Cylinder number LSB
02h	Head number
03h	Sector number
04h	LBA bits (23:16)
05h	LBA bits (15:8)
06h	LBA bits (7:0)
07-12h	Reserved
13h	Sector erased flag (FFh = erased; 00h = not erased)
14-17h	Reserved
18h	Sector write cycles count bits (23:16)
19h	Sector write cycles count bits (15:8)
1Ah	Sector write cycles count bits (7:0)
1B-FFh	Reserved

### 8.3.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	na	na	na	ERR

#### Error Register -

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

ERR shall be set to one if an Error register bit is set to one.

### 8.3.7 Prerequisites

DRDY set equal to one.

### 8.3.8 Description

This command provides information related to a specific sector. The data indicates the erased or not erased status of the sector, and the number of erase and write cycles performed on that sector. Devices may return zero in fields that do not apply or that are not supported by the device.

## 8.4 CFA WRITE MULTIPLE WITHOUT ERASE

### 8.4.1 Command code

CDh

### 8.4.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

### 8.4.3 Protocol

PIO data-out command (see 9.6).

### 8.4.4 Inputs

The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	CDh							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address starting head number or LBA address bits (27:24).

### 8.4.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.

### 8.4.6 Error outputs

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command

block registers contain the address of the sector where the first unrecovered error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	MED
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error Register -

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

MED shall be set to one if a media error is detected

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.4.7 Prerequisites

DRDY set equal to one. If bit 8 of IDENTIFY DEVICE word 59 is equal to zero, a successful SET MULTIPLE MODE command shall precede a CFA WRITE MULTIPLE WITHOUT ERASE command.

### 8.4.8 Description

This command is similar to the WRITE MULTIPLE command. Interrupts are not generated on every sector, but on the transfer of a block that contains the number of sectors defined by the SET MULTIPLE MODE.

Command execution is identical to the WRITE MULTIPLE operation except that the sectors are written without an implied erase operation. The sectors should be pre-erased by a preceding CFA ERASE SECTORS command.

## 8.5 CFA WRITE SECTORS WITHOUT ERASE

### 8.5.1 Command code

38h

### 8.5.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

### 8.5.3 Protocol

PIO data-out command (see 9.6).

### 8.5.4 Inputs

The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	38h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address starting head number or LBA address bits (27:24).

### 8.5.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.

### 8.5.6 Error outputs

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	MED
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error Register -

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

MED shall be set to one if a media error is detected

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.5.7 Prerequisites

DRDY set equal to one.

### 8.5.8 Description

This command is similar to the WRITE SECTORS command. Command execution is identical to the WRITE SECTORS operation except that the sectors are written without an implied erase operation. The sectors should be pre-erased by a preceding CFA ERASE SECTORS command.

## 8.6 CHECK POWER MODE

### 8.6.1 Command code

E5h

### 8.6.2 Feature set

Power Management feature set.

- Power Management feature set is mandatory when power management is not implemented by a PACKET power management feature set.
- This command is mandatory when the Power Management feature set is implemented.

### 8.6.3 Protocol

Non-data command (see 9.4).

### 8.6.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E5h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.6.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Result value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

Device/Head register -  
DEV shall indicate the selected device.

Sector Count result value -  
00h - device is in Standby mode.  
80h - device is in Idle mode.  
FFh - device is in Active mode or Idle mode.

### 8.6.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

**Error register -**

ABRT shall be set to one if Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

**Device/Head register -**

DEV shall indicate the selected device.

**Status register -**

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

**8.6.7 Prerequisites**

DRDY set equal to one.

**8.6.8 Description**

The CHECK POWER MODE command allows the host to determine the current power mode of the device. The CHECK POWER MODE command shall not cause the device to change power or affect the operation of the Standby timer.

**8.7 DEVICE RESET**

**8.7.1 Command code**

08h

**8.7.2 Feature set**

General feature set

- Use prohibited when the PACKET Command feature set is not implemented.
- Mandatory when the PACKET Command feature set is implemented.

**8.7.3 Protocol**

Device reset (see 9.11).

**8.7.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	08h							

**Device/Head register -**

DEV shall indicate the selected device.

### 8.7.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	Diagnostic results							
Sector Count	signature							
Sector Number	signature							
Cylinder Low	signature							
Cylinder High	signature							
Device/Head	0	0	0	DEV	0	0	0	0
Status	see 9.11							

Error register -

The diagnostic code as described in 8.9 is placed in this register.

Sector Count, Sector Number, Cylinder low, Cylinder High -

Signature (see 9.12).

Device/Head register -

DEV shall indicate the selected device.

Status register -

see 9.11.

### 8.7.6 Error outputs

If supported, this command cannot end in an error condition. If this command is not supported and the device has the BSY bit or the DRQ bit set to one when the command is written, the results of this command are indeterminate. If this command is not supported and the device has the BSY bit and the DRQ bit cleared to zero when the command is written, the device shall respond command aborted.

### 8.7.7 Prerequisites

This command shall be accepted when BSY or DRQ is set to one, DRDY is cleared to zero, or DMARQ is asserted. This command shall be accepted when in Sleep mode.

### 8.7.8 Description

The DEVICE RESET command enables the host to reset an individual device without affecting the other device.

## 8.8 DOWNLOAD MICROCODE

### 8.8.1 Command code

92h

### 8.8.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.8.3 Protocol

PIO data-out (see 9.6).



### 8.8.4 Inputs

The head bits of the Device/Head register shall always be cleared to zero. The Cylinder High and Low registers shall be cleared to zero. The Sector Number and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Sector count (low order)							
Sector Number	Sector count (high order)							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	obs	na	obs	DEV	0	0	0	0
Command	92h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.8.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

### 8.8.6 Error outputs

The device shall return command aborted if the device does not support this command or did not accept the microcode data. The device shall return command aborted if subcommand code is not a supported value.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the device does not support this command or did not accept the microcode data. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.8.7 Prerequisites

DRDY set equal to one.

### 8.8.8 Description

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number Register and the Sector Count register. The Sector Number Register shall be used to extend the Sector Count register to create a sixteen bit sector count value. The Sector Number Register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number Register and the Sector Count register shall indicate no data is to be transferred. This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Feature Register are:

- 01h - download is for immediate, temporary use.
- 07h - save downloaded code for immediate and future use.

Either or both values may be supported. All other values are reserved.

## 8.9 EXECUTE DEVICE DIAGNOSTIC

### 8.9.1 Command code

90h

### 8.9.2 Feature set

General feature set

- Mandatory for all devices.

### 8.9.3 Protocol

Device diagnostic (see 9.10).

### 8.9.4 Inputs

None. The device selection bit in the Device/Head register is ignored.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	na	na	na	na	na
Command	90h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.9.5 Normal outputs

The diagnostic code written into the Error register is an 8-bit code. Table 18 defines these values. The values of the bits in the Error register are not as defined in 7.11.6.

Register	7	6	5	4	3	2	1	0
Error	Diagnostic code							
Sector Count	Signature							
Sector Number	Signature							
Cylinder Low	Signature							
Cylinder High	Signature							
Device/Head	Signature							
Status	see 9.10							

Error register -

Diagnostic code.

Sector Count, Sector number, Cylinder Low, Cylinder High, Device/Head registers -  
device signature (see 9.12).

Device/Head register -

DEV shall indicate the selected device.

Status register -

see 9.10.

**Table 18 – Diagnostic codes**

Code (see note 1)	Description
<b>When this code is in the Device 0 Error register</b>	
01h	Device 0 passed, Device 1 passed or not present
00h, 02h-7Fh	Device 0 failed, Device 1 passed or not present
81h	Device 0 passed, Device 1 failed
80h, 82h-FFh	Device 0 failed, Device 1 failed
<b>When this code is in the Device 1 Error register</b>	
01h	Device 1 passed (see note 2)
00h,02h-7Fh	Device 1 failed (see note 2)
NOTE –	
1 Codes other than 01h and 81h may indicate additional information about the failure(s).	
2 If Device 1 is not present, the host may see the information from Device 0 even though Device 1 is selected.	

### 8.9.6 Error outputs

Table 18 shows the error information that is returned as a diagnostic code in the Error register.

### 8.9.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

### 8.9.8 Description

This command shall perform the internal diagnostic tests implemented by the device. The DEV bit in the Device/Head register is ignored. Both devices, if present, shall execute this command regardless of which device is selected.

If the host issues an EXECUTE DEVICE DIAGNOSTIC command while a device is in or going to a power management mode except Sleep, then the device shall execute the EXECUTE DEVICE DIAGNOSTIC sequence.

## 8.10 FLUSH CACHE

### 8.10.1 Command code

E7h

### 8.10.2 Feature set

General feature set

- Mandatory for all devices.

### 8.10.3 Protocol

Non-data command (see 9.4).

### 8.10.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E7h							

Device/Head register -

DEV shall indicate the selected device.

### 8.10.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.  
 DRDY shall be set to one.  
 DF (Device Fault) shall be cleared to zero.  
 DRQ shall be cleared to zero.  
 ERR shall be cleared to zero.

### 8.10.6 Error outputs

An unrecoverable error encountered during execution of writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The sector is removed from the cache. Subsequent FLUSH CACHE commands continue the process of flushing the cache.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT may be set to one if the device is not able to complete the action requested by the command.

Sector Number, Cylinder Low, Cylinder High, Device/Head -

shall be written with the address of the first unrecoverable error.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.10.7 Prerequisites

DRDY set equal to one.

### 8.10.8 Description

This command is used by the host to request the device to flush the write cache. If the write cache is to be flushed, all data cached shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs. The device should use all error recovery methods available to ensure the data is written successfully. The flushing of write cache may take several seconds to complete depending upon the amount of data to be flushed and the success of the operation.

NOTE – This command may take longer than 30 s to complete.

## 8.11 GET MEDIA STATUS

### 8.11.1 Command code

DAh

### 8.11.2 Feature set

Removable Media Status Notification feature set

- Mandatory for devices implementing the Removable Media Status Notification feature set.

Removable Media feature set

- Optional for devices implementing the Removable Media feature set.

### 8.11.3 Protocol

Non-data command (see 9.4).

### 8.11.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	DAh							

Device/Head register -

DEV shall indicate the selected device.

### 8.11.5 Normal outputs

Normal outputs are returned if Media Status Notification is disabled or if no bits are set to one in the Error register.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.11.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	WP	MC	na	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error register -

ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.

NM (No Media) shall be set to one if no media is present in the device. This bit shall be set to one for each execution of GET MEDIA STATUS until media is inserted into the device.

MCR (Media Change Request) shall be set to one if the eject button is pressed by the user and detected by the device. The device shall reset this bit after each execution of the GET MEDIA STATUS command and only set the bit again for subsequent eject button presses.

MC (Media Change) shall be set to one when the device detects media has been inserted. The device shall reset this bit after each execution of the GET MEDIA STATUS command and only set the bit again for subsequent media insertions.

WP (Write Protect) shall be set to one for each execution of GET MEDIA STATUS while the media is write protected.

#### Device/Head register -

DEV shall indicate the selected device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.11.7 Prerequisites

DRDY set equal to one.

### 8.11.8 Description

This command returns media status bits WP, MC, MCR, and NM, as defined above. When Media Status Notification is disabled this command returns zeros in the WP, MC, MCR, and NM bits.

## 8.12 IDENTIFY DEVICE

### 8.12.1 Command code

ECh

### 8.12.2 Feature set

General feature set

- Mandatory for all devices.
- Devices implementing the PACKET Command feature set (see 8.12.5.2).

### 8.12.3 Protocol

PIO data-in (see 9.5).

### 8.12.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	ECh							

Device/Head register -  
DEV shall indicate the selected device.

### 8.12.5 Outputs

#### 8.12.5.1 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

#### 8.12.5.2 Outputs for PACKET Command feature set devices

In response to this command, devices that implement the PACKET Command feature set shall post command aborted and place the PACKET Command feature set signature in the Command Block registers (see 9.12).

### 8.12.6 Error outputs

Devices not implementing the PACKET Command feature set shall not report an error.

### 8.12.7 Prerequisites

DRDY set equal to one.

### 8.12.8 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

Some devices may have to read the media in order to complete this command.



When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 19 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32-bit values (e.g., words 57 and 58). Such fields are transferred using two successive word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD (15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD (15:0) respectively.

Some parameters are defined as a string of ASCII characters. ASCII data fields shall contain only graphic codes (i.e., code values 20h through 7Eh). For the string "Copyright", the character "C" is the first byte, the character "o" is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character ("C") is on bits DD (15:8) of the first word,  
 the 2nd character ("o") is on bits DD (7:0) of the first word,  
 the 3rd character ("p") is on bits DD (15:8) of the second word,  
 the 4th character ("y") is on bits DD (7:0) of the second word,  
 the 5th character ("r") is on bits DD (15:8) of the third word,  
 the 6th character ("i") is on bits DD (7:0) of the third word,  
 the 7th character ("g") is on bits DD (15:8) of the fourth word,  
 the 8th character ("h") is on bits DD (7:0) of the fourth word,  
 the 9th character ("t") is on bits DD (15:8) of the fifth word,  
 the 10th character ("space") is on bits DD (7:0) of the fifth word,

**Table 19 – IDENTIFY DEVICE information**

Word	F/V	
0	F	General configuration bit-significant information: 15 0=ATA device
	F	14-8 retired
	F	7 1=removable media device
	F	6 1=not removable controller and/or device
	F	5-1 retired
	F	0 Reserved
1	V	Number of logical cylinders
2	V	Specific configuration
3	F	Number of logical heads
4-5	X	retired
6	F	Number of logical sectors per logical track
7-9	X	retired
10-19	F	Serial number (20 ASCII characters)
20-21	X	retired
22	F	obsolete
23-26	F	Firmware revision (8 ASCII characters)
27-46	F	Model number (40 ASCII characters)
47	X	15-8 80h
	R F	7-0 00h =Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands
48	R	Reserved
49	R	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command.
	F	13 1=Standby timer values as specified in this standard are supported 0=Standby timer values shall be managed by the device
	R	12 Reserved for the IDENTIFY PACKET DEVICE command.
	F	11 1=IORDY supported 0=IORDY may be supported
	F	10 1=IORDY may be disabled
	R	9 Shall be set to one. Utilized by IDENTIFY PACKET DEVICE command.
	R	8 Shall be set to one. Utilized by IDENTIFY PACKET DEVICE command.
X	7-0 retired	
50	F	Capabilities 15 Shall be cleared to zero.
		14 Shall be set to one.
		13-1 Reserved.
		0 Shall be set to one to indicate a device specific Standby timer value minimum.
51	X	15-0 <b>retired</b>
52	R	retired
53	R	15-3 Reserved
	F	2 1=the fields reported in word 88 are valid 0=the fields reported in word 88 are not valid
	F	1 1=the fields reported in words 64-70 are valid 0=the fields reported in words 64-70 are not valid
	V	0 1=the fields reported in words 54-58 are valid 0=the fields reported in words 54-58 may be valid
54	V	Number of current logical cylinders

*(continued)*

**Table 19 – IDENTIFY DEVICE information**(continued)

Word	F/V	
55	V	Number of current logical heads
56	V	Number of current logical sectors per track
57-58	V	Current capacity in sectors
59	R	15-9 Reserved
	V	8 1=Multiple sector setting is valid
	V	7-0 xxh=Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	F	Total number of user addressable sectors (LBA mode only)
62	R	retired
63	R	15-11 Reserved
	V	10 1= Multiword DMA mode 2 is selected 0= Multiword DMA mode 2 is not selected
	V	9 1= Multiword DMA mode 1 is selected 0= Multiword DMA mode 1 is not selected
	V	8 1= Multiword DMA mode 0 is selected 0= Multiword DMA mode 0 is not selected
	R	7-3 Reserved
	F	2 1= Multiword DMA mode 2 and below are supported
	F	1 1= Multiword DMA mode 1 and below are supported
	F	0 1= Multiword DMA mode 0 is supported
64	R	15-8 Reserved
	F	7-0 Advanced PIO modes supported
65	F	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds
66	F	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds
67	F	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds
68	F	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds
69-70	R	Reserved (for future command overlap and queuing)
71-74	R	Reserved for IDENTIFY PACKET DEVICE command.
75	F	Queue depth 15-5 Reserved 4-0 Maximum queue depth - 1
76-79	R	Reserved

(continued)

**Table 19 – IDENTIFY DEVICE information***(continued)*

Word	F/V	
80	F	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 Reserved for ATA/ATAPI-7 6 Reserved for ATA/ATAPI-6 5 1=supports ATA/ATAPI-5 4 1=supports ATA/ATAPI-4 3 1=supports ATA-3 2 1=supports ATA-2 1 Obsolete 0 Reserved
81	F	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = see 8.12.43
82	F	Command set supported. If words 82 and 83 = 0000h or FFFFh command set notification not supported. 15 Obsolete 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 Obsolete 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt supported 7 1=release interrupt supported 6 1=look-ahead supported 5 1=write cache supported 4 1=supports PACKET Command feature set 3 1=supports Power Management feature set 2 1=supports Removable Media feature set 1 1=supports Security Mode feature set 0 1=supports SMART feature set
83	F	Command sets supported. If words 82 and 83 = 0000h or FFFFh command set notification not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-7 Reserved 6 1=SET FEATURES subcommand required to spinup after power-up 5 1=Power-Up In Standby feature set supported 4 1=Removable Media Status Notification feature set supported 3 1=Advanced Power Management feature set supported 2 1=CFA feature set supported 1 1=READ/WRITE DMA QUEUED supported 0 1=DOWNLOAD MICROCODE command supported

*(continued)*

**Table 19 – IDENTIFY DEVICE information**(continued)

Word	F/V	
84	F	Command set/feature supported extension. If words 82, 83, and 84 = 0000h or FFFFh command set notification extension is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
85	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15 Obsolete 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 Obsolete 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt enabled 7 1=release interrupt enabled 6 1=look-ahead enabled 5 1=write cache enabled 4 1=supports PACKET Command feature set 3 1=supports Power Management feature set 2 1=supports Removable Media feature set 1 1= Security Mode feature set enabled 0 1= SMART feature set enabled
86	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15-7 Reserved 6 1=SET FEATURES subcommand required to spin-up after power-up 5 1=Power-Up In Standby feature set enabled 4 1=Removable Media Status Notification feature set enabled 3 1=Advanced Power Management feature set enabled 2 1=CFA feature set supported 1 1=READ/WRITE DMA QUEUED command supported 0 1=DOWNLOAD MICROCODE command supported
87	V	Command set/feature default. If words 85, 86, and 87 = 0000h or FFFFh command set default notification is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
88	R V V V V V R F F F F F	15-13 Reserved 12 1=Ultra DMA mode 4 is selected 0=Ultra DMA mode 4 is not selected 11 1=Ultra DMA mode 3 is selected 0=Ultra DMA mode 3 is not selected 10 1=Ultra DMA mode 2 is selected 0=Ultra DMA mode 2 is not selected 9 1=Ultra DMA mode 1 is selected 0=Ultra DMA mode 1 is not selected 8 1=Ultra DMA mode 0 is selected 0=Ultra DMA mode 0 is not selected 7-5 Reserved 4 1=Ultra DMA mode 4 and below are supported 3 1=Ultra DMA mode 3 and below are supported 2 1=Ultra DMA mode 2 and below are supported 1 1=Ultra DMA mode 1 and below are supported 0 1=Ultra DMA mode 0 is supported

(continued)



**Table 19 – IDENTIFY DEVICE information**(continued)

Word	F/V	
89	F	Time required for security erase unit completion
90	F	Time required for Enhanced security erase completion
91	V	Current advanced power management value
92	V	Master Password Revision Code
93	V	<p>Hardware reset result. The contents of bits 12-0 of this word shall change only during the execution of a hardware reset.</p> <p>15 Shall be cleared to zero.</p> <p>14 Shall be set to one.</p> <p>13 1=device detected CBLID- above <math>V_{IH}</math> 0=device detected CBLID- below <math>V_{IL}</math></p> <p>12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:</p> <p>12 Reserved.</p> <p>11 0= Device 1 did not assert PDIAG-. 1= Device 1 asserted PDIAG-.</p> <p>10-9 These bits indicate how Device 1 determined the device number: 00=Reserved. 01=a jumper was used. 10=the CSEL signal was used. 11=some other method was used or the method is unknown.</p> <p>8 Shall be set to one.</p> <p>7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:</p> <p>7 Reserved.</p> <p>6 0= Device 0 does not respond when Device 1 is selected. 1= Device 0 responds when Device 1 is selected.</p> <p>5 0= Device 0 did not detect the assertion of DASP-. 1= Device 0 detected the assertion of DASP-.</p> <p>4 0= Device 0 did not detect the assertion of PDIAG-. 1= Device 0 detected the assertion of PDIAG-.</p> <p>3 0= Device 0 failed diagnostics. 1= Device 0 passed diagnostics.</p> <p>2-1 These bits indicate how Device 0 determined the device number: 00=Reserved. 01=a jumper was used. 10=the CSEL signal was used. 11=some other method was used or the method is unknown.</p> <p>0 Shall be set to one.</p>
94-126	R	Reserved
127	F	<p>Removable Media Status Notification feature set support</p> <p>15-2 Reserved</p> <p>1-0 00=Removable Media Status Notification feature set not supported 01=Removable Media Status Notification feature supported 10=Reserved 11=Reserved</p>

(continued)

**Table 19 – IDENTIFY DEVICE information**(concluded)

Word	F/V	
128	V	Security status 15-9 Reserved 8 Security level 0=High, 1=Maximum 7-6 Reserved 5 1=Enhanced security erase supported 4 1=Security count expired 3 1=Security frozen 2 1=Security locked 1 1=Security enabled 0 1=Security supported
129-159	X	Vendor specific
160	V	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma
161-254	R	Reserved
255	F/V	Integrity word 15-8 Checksum 7-0 Signature
<p>Key:</p> <p>F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.</p> <p>V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.</p> <p>X = the content of the word is vendor specific and may be fixed or variable.</p> <p>R = the content of the word is reserved and shall be zero.</p>		

**8.12.9 Word 0: General configuration**

Devices that conform to this standard shall clear bit 15 to zero.

Devices reporting a value of 848Ah in this word shall support the CFA feature set.

**8.12.10 Word 1: Number of cylinders**

This word contains the number of user-addressable logical cylinders in the default CHS translation (see 6.2).

**8.12.11 Word 2: Specific configuration.**

Word 2 shall be set as follows:



Value	Description
37C8h	Device requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is incomplete (see 6.18).
738Ch	Device requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is complete (see 6.18).
8C73h	Device does not require SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is incomplete (see 6.18).
C837h	Device does not require SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is complete (see 6.18).
All other values	Reserved.

#### 8.12.12 Word 3: Number of logical heads

This word contains the number of user-addressable logical heads per logical cylinder in the default CHS translation (see 6.2).

#### 8.12.13 Word 4-5: Retired.

#### 8.12.14 Word 6: Number of logical sectors per logical track

This word contains the number of user-addressable logical sectors per logical track in the default CHS translation (see 6.2).

#### 8.12.15 Words 7-9: Retired.

#### 8.12.16 Words 10-19: Serial number

This field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (words 10-19) and Model number (words 27-46) shall be unique for a given manufacturer.

#### 8.12.17 Word 20-21: Retired.

#### 8.12.18 Word 22: Obsolete.

#### 8.12.19 Word 23-26: Firmware revision

This field contains the firmware revision number of the device. The contents of this field is an ASCII character string of eight bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

#### 8.12.20 Words 27-46: Model number

This field contains the model number of the device. The contents of this field is an ASCII character string of forty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (words 10-19) and Model number (words 27-46) shall be unique for a given manufacturer.

#### 8.12.21 Word 47: READ/WRITE MULTIPLE support.

Bits 7-0 of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands.

#### 8.12.22 Word 48: Reserved.

### 8.12.23 Word 49-50: Capabilities

Bits 15 and 14 of word 49 are reserved for use in the IDENTIFY PACKET DEVICE command response.

Bit 13 of word 49 is used to determine whether a device utilizes the Standby timer values as defined in this standard. Table 22 specifies the Standby timer values utilized by the device if bit 13 is set to one. If bit 13 is cleared to zero, the timer values shall be vendor specific.

Bit 12 of word 49 is reserved for use in the IDENTIFY PACKET DEVICE command response.

Bit 11 of word 49 is used to determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This ensures backward compatibility. If a device supports PIO mode 3 or higher, then this bit shall be set to one.

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command.

Bits 9 and 8 of word 49 shall be set to one for backward compatibility. These bits are defined for use in the IDENTIFY PACKET DEVICE command response.

Bits 7 through 0 of word 49 are retired.

Bit 15 of word 50 shall be cleared to zero to indicate that the contents of word 50 are valid.

Bit 14 of word 50 shall be set to one to indicate that the contents of word 50 are valid.

Bits 13 through 1 of word 50 are reserved.

Bit 0 of word 50 set to one indicates that the device has a minimum Standby timer value that is device specific.

### 8.12.24 Words 51 and 52: Retired

### 8.12.25 Word 53: Field validity

If bit 0 of word 53 is set to one, the values reported in words 54 through 58 are valid. If this bit is cleared to zero, the values reported in words 54 through 58 may be valid. If bit 1 of word 53 is set to one, the values reported in words 64 through 70 are valid. If this bit is cleared to zero, the values reported in words 64-70 are not valid. Any device that supports PIO mode 3 or above, or supports Multiword DMA mode 1 or above, shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70. If the device supports Ultra DMA and the values reported in word 88 are valid, then bit 2 of word 53 shall be set to one. If the device does not support Ultra DMA and the values reported in word 88 are not valid, then this bit is cleared to zero.

### 8.12.26 Word 54: Number of current logical cylinders

This field contains the number of user-addressable logical cylinders in the current CHS translation (see 6.2).

### 8.12.27 Word 55: Number of current logical heads

This field contains the number of user-addressable logical heads per logical cylinder in the current CHS translation (see 6.2).

**8.12.28 Word 56: Number of current logical sectors per logical track**

This field contains the number of user-addressable logical sectors per logical track in the current CHS translation (see 6.2).

**8.12.29 Word (58:57): Current capacity in sectors**

This field contains the current capacity in sectors in the current CHS translation (see 6.2).

**8.12.30 Word 59: Multiple sector setting**

If bit 8 is set to one, bits 7-0 reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. This field may default to the preferred value for the device.

**8.12.31 Word (61:60): Total number of user addressable sectors**

This field contains the total number of user addressable sectors (see 6.2).

**8.12.32 Word 62: Retired****8.12.33 Word 63: Multiword DMA transfer**

Word 63 identifies the Multiword DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is enabled, then no Multiword DMA mode shall be enabled. If a Multiword DMA mode is enabled then no Ultra DMA mode shall be enabled.

**8.12.33.1 Reserved**

Bits 15 through 11 of word 63 are reserved.

**8.12.33.2 Multiword DMA mode 2 selected**

If bit 10 of word 63 is set to one, then Multiword DMA mode 2 is selected. If this bit is cleared to zero, then Multiword DMA mode 2 is not selected. If bit 9 is set to one or if bit 8 is set to one, then this bit shall be cleared to zero.

**8.12.33.3 Multiword DMA mode 1 selected**

If bit 9 of word 63 is set to one, then Multiword DMA mode 1 is selected. If this bit is cleared to zero then Multiword DMA mode 1 is not selected. If bit 10 is set to one or if bit 8 is set to one, then this bit shall be cleared to zero.

**8.12.33.4 Multiword DMA mode 0 selected**

If bit 8 of word 63 is set to one, then Multiword DMA mode 0 is selected. If this bit is cleared to zero then Multiword DMA mode 0 is not selected. If bit 10 is set to one or if bit 9 is set to one, then this bit shall be cleared to zero.

**8.12.33.5 Reserved**

Bits 7 through 3 of word 63 are reserved.

**8.12.33.6 Multiword DMA mode 2 supported**

If bit 2 of word 63 is set to one, then Multiword DMA modes 2 and below are supported. If this bit is cleared to zero, then Multiword DMA mode 2 is not supported. If Multiword DMA mode 2 is supported, then

Multiword DMA modes 1 and 0 shall also be supported. If this bit is set to one, bits 1 and 0 shall be set to one.

#### **8.12.33.7 Multiword DMA mode 1 supported**

If bit 1 of word 63 is set to one, then Multiword DMA modes 1 and below are supported. If this bit is cleared to zero, then Multiword DMA mode 1 is not supported. If Multiword DMA mode 1 is supported, then Multiword DMA mode 0 shall also be supported. If this bit is set to one, bit 0 shall be set to one.

#### **8.12.33.8 Multiword DMA mode 0 supported**

If bit 0 of word 63 is set to one, then Multiword DMA mode 0 is supported.

#### **8.12.34 Word 64: PIO transfer modes supported**

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the advanced PIO modes the device is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future advanced PIO modes. Bit 0, if set to one, indicates that the device supports PIO mode 3. Bit 1, if set to one, indicates that the device supports PIO mode 4.

#### **8.12.35 Word 65: Minimum Multiword DMA transfer cycle time per word**

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the device supports when performing Multiword DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

#### **8.12.36 Word 66: Device recommended Multiword DMA cycle time**

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the device recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result.

If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

**8.12.37 Word 67: Minimum PIO transfer cycle time without flow control**

Word 67 of the parameter information of the IDENTIFY DEVICE command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

**8.12.38 Word 68: Minimum PIO transfer cycle time with IORDY**

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

**8.12.39 Words 69-74: Reserved****8.12.40 Word 75: Queue depth**

Bits 4 through 0 of word 75 indicate the maximum queue depth supported by the device. The queue depth includes all commands for which command acceptance has occurred and command completion has not occurred. The value in this field is the maximum queue depth - 1, e.g., a value of 0 indicates a queue depth of 1, a value of 31 indicates a queue depth of 32. If bit 1 of word 83 is cleared to zero indicating that the device does not support READ/WRITE DMA QUEUED commands, the value in this field shall be 0. A device may support READ/WRITE DMA QUEUED commands to provide overlap only (i.e., queuing not supported), in this case, bit 1 of word 83 shall be set to one and the queue depth shall be set to 0.

**8.12.41 Words 76-79: Reserved****8.12.42 Word 80: Major version number**

If not 0000h or FFFFh, the device claims compliance with the major version(s) as indicated by bits 2 through 5 being equal to one. Values other than 0000h and FFFFh are bit significant. Since ATA standards maintain downward compatibility, a device may set more than one bit.

**8.12.43 Word 81: Minor version number**

If an implementor claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 shall be 0000h or FFFFh.

Table 20 defines the value that may optionally be reported in word 81 to indicate the revision of the standard that guided the implementation.

**Table 20 – Minor version number**

<b>Value</b>	<b>Minor revision</b>
0001h	Obsolete
0002h	Obsolete
0003h	Obsolete
0004h	ATA-2 published, ANSI X3.279-1996
0005h	ATA-2 X3T10 948D prior to revision 2k
0006h	ATA-3 X3T10 2008D revision 1
0007h	ATA-2 X3T10 948D revision 2k
0008h	ATA-3 X3T10 2008D revision 0
0009h	ATA-2 X3T10 948D revision 3
000Ah	ATA-3 published, ANSI X3.298-199x
000Bh	ATA-3 X3T10 2008D revision 6
000Ch	ATA-3 X3T13 2008D revision 7 and 7a
000Dh	ATA/ATAPI-4 X3T13 1153D revision 6
000Eh	ATA/ATAPI-4 T13 1153D revision 13
000Fh	ATA/ATAPI-4 X3T13 1153D revision 7
0010h	ATA/ATAPI-4 T13 1153D revision 18
0011h	ATA/ATAPI-4 T13 1153D revision 15
0012h	ATA/ATAPI-4 published, ANSI NCITS 317-1998
0013h	Reserved
0014h	ATA/ATAPI-4 T13 1153D revision 14
0015h	ATA/ATAPI-5 T13 1321D revision 1
0016h	Reserved
0017h	ATA/ATAPI-4 T13 1153D revision 17
0018h-FFFFh	Reserved

**8.12.44 Words 82-84: Features/command sets supported**

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by devices prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid.

If bit 0 of word 82 is set to one, the SMART feature set is supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

If bit 2 of word 82 is set to one, the Removable Media feature set is supported.

If bit 3 of word 82 is set to one, the Power Management feature set is supported.

If bit 4 of word 82 is set to one, the PACKET Command feature set is supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

If bit 7 of word 82 is set to one, release interrupt is supported.

If bit 8 of word 82 is set to one, SERVICE interrupt is supported.

If bit 9 of word 82 is set to one, the DEVICE RESET command is supported.

If bit 10 of word 82 is set to one, the Host Protected Area feature set is supported.

Bit 11 of word 82 is obsolete.

If bit 12 of word 82 is set to one, the device supports the WRITE BUFFER command.

If bit 13 of word 82 is set to one, the device supports the READ BUFFER command.

If bit 14 of word 82 is set to one, the device supports the NOP command.

Bit 15 of word 82 is obsolete.

If bit 0 of word 83 is set to one, the device supports the DOWNLOAD MICROCODE command.

If bit 1 of word 83 is set to one, the device supports the READ DMA QUEUED and WRITE DMA QUEUED commands.

If bit 2 of word 83 is set to one, the device supports the CFA feature set.

If bit 3 of word 83 is set to one, the device supports the Advanced Power Management feature set.

If bit 4 of word 83 is set to one, the device supports the Removable Media Status feature set.

If bit 5 of word 83 is set to one, the device supports the Power-Up In Standby feature set.

If bit 6 of word 83 is set to one, the device requires the SET FEATURES subcommand to spin-up after power-up if the Power-Up In Standby feature set is enabled (see 8.37.14).

#### **8.12.45 Words 85-87: Features/command sets enabled**

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by devices prior to ATA/ATAPI-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid.

If bit 0 of word 85 is set to one, the SMART feature set has been enabled via the SMART ENABLE OPERATIONS command.

If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the SECURITY SET PASSWORD command.

If bit 2 of word 85 is set to one, the Removable Media feature set is supported.

If bit 3 of word 85 is set to one, the Power Management feature set is supported.

If bit 4 of word 85 is set to one, the PACKET Command feature set is supported.

If bit 5 of word 85 is set to one, write cache has been enabled via the SET FEATURES command (see 8.37.9).

If bit 6 of word 85 is set to one, look-ahead has been enabled via the SET FEATURES command (see 8.37.16).

If bit 7 of word 85 is set to one, release interrupt has been enabled via the SET FEATURES command (see 8.37.17).

If bit 8 of word 85 is set to one, SERVICE interrupt has been enabled via the SET FEATURES command (see 8.37.18).

If bit 9 of word 85 is set to one, the DEVICE RESET command is supported.

If bit 10 of word 85 is set to one, the Host Protected Area feature set is supported.

Bit 11 of word 85 is obsolete.

If bit 12 of word 85 is set to one, the device supports the WRITE BUFFER command.

If bit 13 of word 85 is set to one, the device supports the READ BUFFER command.

If bit 14 of word 85 is set to one, the device supports the NOP command.

Bit 15 of word 85 is obsolete.

If bit 0 of word 86 is set to one, the device supports the DOWNLOAD MICROCODE command.

If bit 1 of word 86 is set to one, the device supports the READ DMA QUEUED and WRITE DMA QUEUED commands.

If bit 2 of word 86 is set to one, the device supports the CFA feature set.

If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the SET FEATURES command.

If bit 4 of word 86 is set to one, the Removable Media Status feature set has been enabled via the SET FEATURES command.

If bit 5 of word 86 is set to one, the Power-Up In Standby feature set has been enabled via the SET FEATURES command (see 8.37.12).

If bit 6 of word 86 is set to one, the device requires the SET FEATURES subcommand to spin-up after power-up (see 8.37.14).

#### **8.12.46 Word 88: Ultra DMA modes**

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is enabled, then no Multiword DMA mode shall be enabled. If a Multiword DMA mode is enabled then no Ultra DMA mode shall be enabled.

##### **8.12.46.1 Reserved**

Bits 15 through 13 of word 88 are reserved.

##### **8.12.46.2 Ultra DMA mode 4 selected**

If bit 12 of word 88 is set to one, then Ultra DMA mode 4 is selected. If this bit is cleared to zero, then Ultra DMA mode 4 is not selected. If bit 11 or bit 10 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

##### **8.12.46.3 Ultra DMA mode 3 selected**

If bit 11 of word 88 is set to one, then Ultra DMA mode 3 is selected. If this bit is cleared to zero, then Ultra DMA mode 3 is not selected. If bit 12 or bit 10 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.



**8.12.46.4 Ultra DMA mode 2 selected**

If bit 10 of word 88 is set to one, then Ultra DMA mode 2 is selected. If this bit is cleared to zero, then Ultra DMA mode 2 is not selected. If bit 12 or bit 11 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

**8.12.46.5 Ultra DMA mode 1 selected**

If bit 9 of word 88 is set to one, then Ultra DMA mode 1 is selected. If this bit is cleared to zero then Ultra DMA mode 1 is not selected. If bit 12 or bit 11 or bit 10 or bit 8 is set to one, then this bit shall be cleared to zero.

**8.12.46.6 Ultra DMA mode 0 selected**

If bit 8 of word 88 is set to one, then Ultra DMA mode 0 is selected. If this bit is cleared to zero then Ultra DMA mode 0 is not selected. If bit 12 or bit 11 or bit 10 or bit 9 is set to one, then this bit shall be cleared to zero.

**8.12.46.7 Reserved**

Bits 7 through 5 of word 88 are reserved.

**8.12.46.8 Ultra DMA mode 4 supported**

If bit 4 of word 88 is set to one, then Ultra DMA modes 4 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 4 is not supported. If Ultra DMA mode 4 is supported, then Ultra DMA modes 3, 2, 1 and 0 shall also be supported. If this bit is set to one, then bits 3, 2, 1 and 0 shall be set to one.

**8.12.46.9 Ultra DMA mode 3 supported**

If bit 3 of word 88 is set to one, then Ultra DMA modes 3 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 3 is not supported. If Ultra DMA mode 3 is supported, then Ultra DMA modes 2, 1 and 0 shall also be supported. If this bit is set to one, then bits 2, 1 and 0 shall be set to one.

**8.12.46.10 Ultra DMA mode 2 supported**

If bit 2 of word 88 is set to one, then Ultra DMA modes 2 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 2 is not supported. If Ultra DMA mode 2 is supported, then Ultra DMA modes 1 and 0 shall also be supported. If this bit is set to one, bits 1 and 0 shall be set to one.

**8.12.46.11 Ultra DMA mode 1 supported**

If bit 1 of word 88 is set to one, then Ultra DMA modes 1 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 1 is not supported. If Ultra DMA mode 1 is supported, then Ultra DMA mode 0 shall also be supported. If this bit is set to one, bit 0 shall be set to one.

**8.12.46.12 Ultra DMA mode 0 supported**

If bit 0 of word 88 is set to one, then Ultra DMA mode 0 is supported. If this bit is cleared to zero, then Ultra DMA is not supported.

**8.12.47 Word 89: Time required for Security erase unit completion**

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

#### 8.12.48 Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the ENHANCED SECURITY ERASE UNIT command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

#### 8.12.49 Word 91: Advanced power management level value

Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

#### 8.12.50 Word 92: Master Password Revision Code

Word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed.

#### 8.12.51 Word 93: Hardware configuration test results

During hardware reset execution, Device 0 shall clear bits 13-8 of this word to zero and shall set bits 7-0 of the word as indicated to show the result of the hardware reset execution. During hardware reset execution, Device 1 shall clear bits 7-0 of this word to zero and shall set bits 13-8 as indicated to show the result of the hardware reset execution.

Bit 13 shall be set or cleared by the selected device to indicate whether the device detected CBLID- above  $V_{IH}$  or below  $V_{IL}$  at any time during execution of each IDENTIFY DEVICE routine after receiving the command from the host but before returning data to the host. This test may be repeated as desired by the device during command execution (see Annex D).

#### 8.12.52 Words 94-126: Reserved

#### 8.12.53 Word 127: Removable Media Status Notification feature set support

If bit 0 of word 127 is set to one and bit 1 of word 127 is cleared to zero, the device supports the Removable Media Status Notification feature set. Bits 15 through 2 shall be cleared to zero.

#### 8.12.54 Word 128: Security status

Bit 8 of word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.

Bit 5 of word 128 indicates the Enhanced security erase unit feature is supported. If bit 5 is set to one, the Enhanced security erase unit feature set is supported.

Bit 4 of word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hard reset.

Bit 3 of word 128 indicates security Frozen. If bit 3 is set to one, the security is Frozen.

Bit 2 of word 128 indicates security locked. If bit 2 is set to one, the security is locked.

Bit 1 of word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.

Bit 0 of word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

#### 8.12.55 Words 129-159: Vendor specific.

#### 8.12.56 Word 160: CFA power mode

Word 160 indicates the presence and status of a CFA feature set device that supports CFA Power Mode 1.

If bit 13 of word 160 is set to one then the device must be in CFA Power Mode 1 to perform one or more commands implemented by the device.

If bit 12 of word 160 is set to one the device is in CFA Power Mode 0 (see 8.37.13).

Bits 11-0 indicate the maximum average RMS current in Milliamperes required during 3.3V or 5V device operation in CFA Power Mode 1.

#### 8.12.57 Words 161-254: Reserved.

#### 8.12.58 Word 255: Integrity word

The use of this word is optional. If bits 7:0 of this word contain the signature A5h, bits 15:8 contain the data structure checksum. The data structure checksum is the two's complement of the sum of all bytes in words 0 through 254 and the byte consisting of bits 7:0 in word 255. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct.

### 8.13 IDENTIFY PACKET DEVICE

#### 8.13.1 Command code

A1h

#### 8.13.2 Feature set

PACKET Command feature set

- Use prohibited for devices not implementing the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.

#### 8.13.3 Protocol

PIO data-in (see 9.5).

#### 8.13.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	A1h							

Device/Head register -

DEV shall indicate the selected device.

### 8.13.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.13.6 Error outputs

The device shall return command aborted if the device does not implement this command, otherwise, the device shall not report an error.

### 8.13.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

### 8.13.8 Description

The IDENTIFY PACKET DEVICE command enables the host to receive parameter information from a device that implements the PACKET Command feature set.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 21 defines the arrangement and meanings of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a group of bits. A word that is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32-bit values (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD (15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD (15:0) respectively.

Some parameters are defined as a string of ASCII characters. For the string "Copyright", the character "C" is the first byte, the character "o" is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character ("C") is on bits DD (15:8) of the first word,  
the 2nd character ("o") is on bits DD (7:0) of the first word,  
the 3rd character ("p") is on bits DD (15:8) of the second word,  
the 4th character ("y") is on bits DD (7:0) of the second word,  
the 5th character ("r") is on bits DD (15:8) of the third word,  
the 6th character ("i") is on bits DD (7:0) of the third word,  
the 7th character ("g") is on bits DD (15:8) of the fourth word,  
the 8th character ("h") is on bits DD (7:0) of the fourth word,  
the 9th character ("t") is on bits DD (15:8) of the fifth word,  
the 10th character ("space") is on bits DD (7:0) of the fifth word,

**Table 21 – IDENTIFY PACKET DEVICE information(continued)**

Word	F/V	
0	F	General configuration bit-significant information: 15-14 10=ATAPI device 11=reserved
	R	13 reserved
	F	12-8 Field indicates command packet set used by device
	F	7 1=removable media device
	F	6-5 00=Device shall set DRQ to one within 3 ms of receiving PACKET command. 01=obsolete. 10=Device shall set DRQ to one within 50 $\mu$ s of receiving PACKET command. 11=reserved
	R	4-2 reserved
	F	1-0 00=12 byte command packet 01=16 byte command packet 1x=reserved
1	R	Reserved
2	V	Unique configuration
3-9	R	Reserved
10-19	F	Serial number (20 ASCII characters)
20-22	R	Reserved
23-26	F	Firmware revision (8 ASCII characters)
27-46	F	Model number (40 ASCII characters)
47-48	R	Reserved
49		Capabilities
	F	15 1=interleaved DMA supported
	F	14 1=command queuing supported
	F	13 1=overlap operation supported
	F	12 1=ATA software reset required (obsolete)
	F	11 1=IORDY supported
	F	10 1=IORDY may be disabled
	F	9 1=LBA supported
	F	8 1=DMA supported
	X	7-0 Vendor specific
50	R	Reserved
51	X	15-8 Retired
	X	7-0 Vendor specific
52	R	Reserved
53	R	15-3 Reserved
	F	2 1=the fields reported in word 88 are valid 0=the fields reported in word 88 are not valid
	F	1 1=the fields reported in words 64-70 are valid 0=the fields reported in words 64-70 are not valid
	V	0 1=the fields reported in words 54-58 are valid 0=the fields reported in words 54-58 may be valid
54-62	R	Reserved

(continued)

**Table 21 – IDENTIFY PACKET DEVICE information**(continued)

Word	F/V	
63	R	15-11 Reserved
	V	10 1= Multiword DMA mode 2 is selected 0= Multiword DMA mode 2 is not selected
	V	9 1= Multiword DMA mode 1 is selected 0= Multiword DMA mode 1 is not selected
	V	8 1= Multiword DMA mode 0 is selected 0= Multiword DMA mode 0 is not selected
	R	7-3 Reserved
	F	2 1= Multiword DMA mode 2 and below are supported
	F	1 1= Multiword DMA mode 1 and below are supported
	F	0 1= Multiword DMA mode 0 is supported Multiword DMA mode selected
64	R	15-8 Reserved
	F	7-0 Advanced PIO transfer modes supported
65	F	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds
66	F	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds
67	F	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds
68	F	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds
69-70	R	Reserved (for future command overlap and queuing)
71	F	Typical time in ns from receipt of PACKET command to bus release.
72	F	Typical time in ns from receipt of SERVICE command to BSY cleared to zero
73-74	R	Reserved
75	F	Queue depth
		15-5 Reserved
		4-0 Maximum queue depth supported - 1
76-79	R	Reserved
80	F	Major version number 0000h or FFFFh = device does not report version
		15 Reserved
		14 Reserved for ATA/ATAPI-14
		13 Reserved for ATA/ATAPI-13
		12 Reserved for ATA/ATAPI-12
		11 Reserved for ATA/ATAPI-11
		10 Reserved for ATA/ATAPI-10
		9 Reserved for ATA/ATAPI-9
		8 Reserved for ATA/ATAPI-8
		7 Reserved for ATA/ATAPI-7
		6 Reserved for ATA/ATAPI-6
		5 1=supports ATA/ATAPI-5
		4 1=supports ATA/ATAPI-4
3 1=supports ATA-3		
2 1=supports ATA-2		
1 Obsolete		
0 Reserved		
81	F	Minor version number 0000h or FFFFh=device does not report version 0001h-FFFEh=see 8.12.43

(continued)

**Table 21 – IDENTIFY PACKET DEVICE information(continued)**

Word	F/V	
82	F	<p>Command set supported. If words 82 and 83 =0000h or FFFFh command set notification not supported.</p> <p>15 Obsolete</p> <p>14 1=NOP command supported</p> <p>13 1=READ BUFFER command supported</p> <p>12 1=WRITE BUFFER command supported</p> <p>11 Obsolete</p> <p>10 1=Host Protected Area feature set supported</p> <p>9 1=DEVICE RESET command supported</p> <p>8 1=SERVICE interrupt supported</p> <p>7 1=release interrupt supported</p> <p>6 1=look-ahead supported</p> <p>5 1=write cache supported</p> <p>4 1=supports PACKET Command feature set</p> <p>3 1=supports Power Management feature set</p> <p>2 1=supports Removable Media feature set</p> <p>1 1=supports Security Mode feature set</p> <p>0 1=supports SMART feature set</p>
83	F	<p>Command sets supported. If words 82 and 83 =0000h or FFFFh command set notification not supported.</p> <p>15 Shall be cleared to zero</p> <p>14 Shall be set to one</p> <p>13-6 Reserved</p> <p>5 1=Power-Up In Standby feature set supported</p> <p>4 1=Removable Media Status Notification feature set supported</p> <p>3-1 Reserved</p> <p>0 1=DOWNLOAD MICROCODE command supported</p>
84	F	<p>Command set/feature supported extension. If words 82, 83, and 84 = 0000h or FFFFh command set notification extension is not supported.</p> <p>15 Shall be cleared to zero</p> <p>14 Shall be set to one</p> <p>13-0 Reserved</p>
85	V	<p>Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported.</p> <p>15 Obsolete</p> <p>14 1=NOP command supported</p> <p>13 1=READ BUFFER command supported</p> <p>12 1=WRITE BUFFER command supported</p> <p>11 Obsolete</p> <p>10 1=Host Protected Area feature set supported</p> <p>9 1=DEVICE RESET command supported</p> <p>8 1=SERVICE interrupt enabled</p> <p>7 1=release interrupt enabled</p> <p>6 1=look-ahead enabled</p> <p>5 1=write cache enabled</p> <p>4 1=supports PACKET Command feature set</p> <p>3 1=supports Power Management feature set</p> <p>2 1=supports Removable Media feature set</p> <p>1 1= Security Mode feature set enabled</p> <p>0 1= SMART feature set enabled</p>

(continued)



**Table 21 – IDENTIFY PACKET DEVICE information***(continued)*

Word	F/V	
86	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15-6 Reserved 5 1=Power-Up In Standby feature set enabled 4 1=Removable Media Status Notification feature set enabled via the SET FEATURES command. 3-1 Reserved 0 1=DOWNLOAD MICROCODE command supported
87	V	Command set/feature default. If words 85, 86, and 87 = 0000h or FFFFh command set default notification is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
88	R	15-13 Reserved
	V	12 1=Ultra DMA mode 4 is selected 0=Ultra DMA mode 4 is not selected
	V	11 1=Ultra DMA mode 3 is selected 0=Ultra DMA mode 3 is not selected
	V	10 1=Ultra DMA mode 2 is selected 0=Ultra DMA mode 2 is not selected
	V	9 1=Ultra DMA mode 1 is selected 0=Ultra DMA mode 1 is not selected
	V	8 1=Ultra DMA mode 0 is selected 0=Ultra DMA mode 0 is not selected
	R	7-5 Reserved
	F	4 1=Ultra DMA mode 4 and below are supported
	F	3 1=Ultra DMA mode 3 and below are supported
	F	2 1=Ultra DMA mode 2 and below are supported
	F	1 1=Ultra DMA mode 1 and below are supported
	F	0 1=Ultra DMA mode 0 is supported
89-92	R	Reserved

*(continued)*

**Table 21 – IDENTIFY PACKET DEVICE information**(continued)

Word	F/V	
93	V	<p>Hardware reset result. The contents of bits 12-0 of this word shall change only during the execution of a hardware reset.</p> <p>15 Shall be cleared to zero.</p> <p>14 Shall be set to one.</p> <p>13 1=device detected CBLID- above <math>V_{iH}</math> 0=device detected CBLID- below <math>V_{iL}</math></p> <p>12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:</p> <p>12 Reserved.</p> <p>11 0= Device 1 did not assert PDIAG-. 1= Device 1 asserted PDIAG-.</p> <p>10-9 These bits indicate how Device 1 determined the device number: 00=Reserved. 01=a jumper was used. 10=the CSEL signal was used. 11=some other method was used or the method is unknown.</p> <p>8 Shall be set to one.</p> <p>7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:</p> <p>7 Reserved.</p> <p>6 0= Device 0 does not respond when Device 1 is selected. 1= Device 0 responds when Device 1 is selected.</p> <p>5 0= Device 0 did not detect the assertion of DASP-. 1= Device 0 detected the assertion of DASP-.</p> <p>4 0= Device 0 did not detect the assertion of PDIAG-. 1= Device 0 detected the assertion of PDIAG-.</p> <p>3 0= Device 0 failed diagnostics. 1= Device 0 passed diagnostics.</p> <p>2-1 These bits indicate how Device 0 determined the device number: 00=Reserved. 01=a jumper was used. 10=the CSEL signal was used. 11=some other method was used or the method is unknown.</p> <p>0 Shall be set to one.</p>
94-126	R	Reserved
127	F	<p>Removable Media Status Notification feature set support</p> <p>15-2 Reserved</p> <p>1-0 00=Removable Media Status Notification feature set not supported 01=Removable Media Status Notification feature set supported 10=Reserved 11=Reserved</p>

(continued)

**Table 21 – IDENTIFY PACKET DEVICE information**(concluded)

Word	F/V	
128	V	Security status 15-9 Reserved 8 Security level 0=High, 1=Maximum 7-6 Reserved 5 1=Enhanced security erase supported 4 1=Security count expired 3 1=Security frozen 2 1=Security locked 1 1=Security enabled 0 1=Security supported
129-159	X	Vendor specific
160-254	R	Reserved
255	F/V	Integrity word 15-8 Checksum 7-0 Signature
<p>Key:</p> <p>F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.</p> <p>V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.</p> <p>X = the content of the word is vendor specific and may be fixed or variable.</p> <p>R = the content of the word is reserved and shall be zero.</p>		

### 8.13.9 Word 0: General configuration

Bits 15 and 14 of word 0 indicate the type of device. If bit 15 is cleared to zero the device does not implement the PACKET Command feature set. If bit 15 is set to one and bit 14 is cleared to zero, the device implements the PACKET Command feature set. The value bit 15 and bit 14 both set to one is reserved.

Bits 12 through 8 of word 0 indicate the command packet set implemented by the device. This value follows the peripheral device type value as defined in SCSI Primary Commands - 2 (SPC-2) T10/1236D.

Value	Description
00h	Direct-access device
01h	Sequential-access device
02h	Printer device
03h	Processor device
04h	Write-once device
05h	CD-ROM device
06h	Scanner device
07h	Optical memory device
08h	Medium changer device
09h	Communications device
0A-0Bh	Reserved for ACS IT8 (Graphic arts pre-press devices)
0Ch	Array controller device
0Dh	Enclosure services device
0Eh	Reduced block command devices
0Fh	Optical card reader/writer device
10-1Eh	Reserved
1Fh	Unknown or no device type

Bit 7 if set to one indicates that the device has removable media.

Bits 6 and 5 of word 0 indicates the DRQ response time when a PACKET command is received. A value of 00b indicates a maximum time of 3 ms from receipt of PACKET to the setting of DRQ to one. A value of 10b indicates a maximum time of 50  $\mu$ s from the receipt of PACKET to the setting of DRQ to one. The value 11b is reserved.

Bits 1 and 0 of word 0 indicate the packet size the device supports. A value of 00b indicates that a 12 byte packet is supported; a value of 01b indicates a 16 byte packet. The values 10b and 11b are reserved.

#### **8.13.10 Word 1: Reserved**

#### **8.13.11 Word 2: Specific configuration**

Word 2 shall have the same content described for word 2 of the IDENTIFY DEVICE command.

#### **8.13.12 Words 3-9: Reserved**

#### **8.13.13 Words 10-19: Serial number**

The use of these words is optional. If not implemented, the content shall be zeros. If implemented, the content shall be as described in words 10-19 of the IDENTIFY DEVICE command (see 8.12).

#### **8.13.14 Words 20-22: Reserved**

#### **8.13.15 Words 23-26: Firmware revision**

Words 23 through 26 shall have the content described for words 23 through 26 of the IDENTIFY DEVICE command.

#### **8.13.16 Words 27-46: Model number**

Words 27 through 46 shall have the content described for words 27 through 46 of the IDENTIFY DEVICE command.

#### **8.13.17 Words 47-48: Reserved**

#### **8.13.18 Word 49: Capabilities**

Bit 15 of word 49 is used to indicated that the device supports interleaved DMA data transfer for overlapped DMA commands.

Bit 14 of word 49 is used to indicated that the device supports command queuing for overlapped commands. If bit 14 is set to one, bit 13 shall be set to one.

Bit 13 of word 49 is used to indicated that the device supports command overlap operation.

Bit 12 of word 49 indicates that the device requires a software reset to reset the device when BSY is set to one. Some devices produced before this standard are unable to process a DEVICE RESET when the BSY bit is set to one. The use of this bit is obsolete.

Bit 11 of word 49 is used to determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This ensures backward compatibility. If a device supports PIO mode 3 or higher, then this bit shall be set to one.

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command.

Bit 9 of word 49 indicates that an LBA translation is supported

Bits 8 of word 49 indicates that DMA is supported.

**8.13.19 Word 50: Reserved**

**8.13.20 Word 51: Retired**

**8.13.21 Word 52: Reserved**

**8.13.22 Word 53: Field validity**

Word 53 shall have the content described for word 53 of the IDENTIFY DEVICE command.

**8.13.23 Words 54-62: Reserved**

**8.13.24 Word 63: Multiword DMA transfer**

Word 63 shall have the content described for word 63 of the IDENTIFY DEVICE command.

**8.13.25 Word 64: PIO transfer mode supported**

Word 64 shall have the content described for word 64 of the IDENTIFY DEVICE command.

**8.13.26 Word 65: Minimum multiword DMA transfer cycle time per word**

Word 65 shall have the content described for word 65 of the IDENTIFY DEVICE command.

**8.13.27 Word 66: Device recommended multiword DMA cycle time**

Word 66 shall have the content described for word 66 of the IDENTIFY DEVICE command.

**8.13.28 Word 67: Minimum PIO transfer cycle time without flow control**

Word 67 shall have the content described for word 67 of the IDENTIFY DEVICE command.

**8.13.29 Word 68: Minimum PIO transfer cycle time with IORDY**

Word 68 shall have the content described for word 68 of the IDENTIFY DEVICE command.

**8.13.30 Word 69-70: Reserved**

**8.13.31 Word 71: PACKET to bus release time**

Word 71 shall contain the time (for 99.7 % of the occurrences) in microseconds from the receipt of a PACKET command until the device performs a bus release.

**8.13.32 Word 72: SERVICE to bus release time**

Word 72 shall contain the time (for 99.7% of the occurrences) in microseconds from the receipt of a SERVICE command until the device performs a bus release.

**8.13.33 Word 73-74: Reserved**

**8.13.34 Word 75: Queue depth**

Bits 4 through 0 of word 75 shall have the content described for word 75 of the IDENTIFY DEVICE command.

**8.13.35 Words 76-79: Reserved**

**8.13.36 Word 80: Major revision number**

Word 80 shall have the content described for word 80 of the IDENTIFY DEVICE command.

**8.13.37 Word 81: Minor revision number**

Word 81 shall have the content described for word 81 of the IDENTIFY DEVICE command.

**8.13.38 Words 82-84: Features/command sets supported**

Words 82, 83, and 84 shall have the content described for words 82, 83, and 84 of the IDENTIFY DEVICE command.

**8.13.39 Words 85-87: Features/command sets enabled**

Words 85, 86, and 87 shall have the content described for words 85, 86, and 87 of the IDENTIFY DEVICE command.

**8.13.40 Word 88: Ultra DMA modes**

Word 88 shall have the content described for word 88 of the IDENTIFY DEVICE command.

**8.13.41 Word 89: Time required for Security erase unit completion**

Word 89 shall have the content described for word 89 of the IDENTIFY DEVICE command.

**8.13.42 Word 90: Time required for Enhanced security erase unit completion**

Word 90 shall have the content described for word 90 of the IDENTIFY DEVICE command.

**8.13.43 Word 91-92: Reserved**

**8.13.44 Word 93: Hardware reset results**

Word 93 shall have the content described for word 93 of the IDENTIFY DEVICE command.

**8.13.45 Word 94-126: Reserved**

**8.13.46 Word 127: Removable Media Status Notification feature set support**

Word 127 shall have the content described for word 127 of the IDENTIFY DEVICE command.

**8.13.47 Word 128: Security status**

Word 128 shall have the content described for word 128 of the IDENTIFY DEVICE command.

**8.13.48 Words 129-254: Reserved**

**8.13.49 Word 255: Integrity Word**

Word 255 shall have the content described for word 255 of the IDENTIFY DEVICE command.

## 8.14 IDLE

### 8.14.1 Command code

E3h

### 8.14.2 Feature set

Power Management feature set.

- Power Management feature set is mandatory when power management is not implemented by a PACKET power management feature set.
- This command is mandatory when the Power Management feature set is implemented and the **PACKET Command feature set is not implemented**.

### 8.14.3 Protocol

Non-data command (see 9.4).

### 8.14.4 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer. Table 22 defines these values.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E3h							

Device/Head register -

DEV shall indicate the selected device.

**Table 22 – Automatic Standby timer periods**

Sector Count register contents	Corresponding timeout period
0 (00h)	Timeout disabled
1-240 (01h-F0h)	(value * 5) s
241-251 (F1h-FBh)	((value - 240) * 30) min
252 (FCh)	21 min
253 (FDh)	Period between 8 and 12 hrs
254 (FEh)	Reserved
255 (FFh)	21 min 15 s

NOTE – Times are approximate.

### 8.14.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.14.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.14.7 Prerequisites

DRDY set equal to one.

### 8.14.8 Description

The IDLE command allows the host to place the device in the Idle mode using the Standby timer. INTRQ may be asserted even though the device may not have fully transitioned to Idle mode.



If the Sector Count register is non-zero then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer (see 6.11). If the Sector Count register is zero then the Standby timer is disabled.

## 8.15 IDLE IMMEDIATE

### 8.15.1 Command code

E1h

### 8.15.2 Feature set

Power Management feature set.

- Power Management feature set is mandatory when power management is not implemented by a PACKET power management feature set.
- This command is mandatory when the Power Management feature set is implemented.

### 8.15.3 Protocol

Non-data command (see 9.4).

### 8.15.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E1h							

Device/Head register -

DEV shall indicate the selected device.

### 8.15.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.15.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.15.7 Prerequisites

DRDY set equal to one.

### 8.15.8 Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the Idle mode. INTRQ may be asserted even though the device may not have fully transitioned to Idle mode (see 6.11).

## 8.16 INITIALIZE DEVICE PARAMETERS

### 8.16.1 Command code

91h

### 8.16.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set if a CHS translation is supported.
- Not mandatory for devices not implementing the PACKET command feature set if the device capacity is greater than 8 Gbytes and only LBA translation is supported.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.16.3 Protocol

Non-data (see 9.4).

### 8.16.4 Inputs

The Sector Count register specifies the number of logical sectors per logical track, and the Device/Head register specifies the maximum head number.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Logical sectors per logical track							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	Max head			
Command	91h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.16.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	na	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

### 8.16.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	na	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if the device does not support the requested CHS translation. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DF (Device Fault) shall be set to one if a device fault has occurred.  
DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.16.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

### 8.16.8 Description

This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

If the capacity of the device is less than 16,514,064 sectors, a device shall support the CHS translation described in words 1, 3, and, 6 of the IDENTIFY DEVICE information. Support of other CHS translations is optional.

If the host requests a CHS translation that is not supported by the device, the device shall return command aborted. The device shall also clear bit 0 of word 53 in the IDENTIFY DEVICE data to zero, and the content of words 54, 55, 56, and, (58:57) may be zero until a supported translation is requested by the host.

If the requested CHS translation is not supported, the device shall fail all media access commands with an ID Not Found error until a valid CHS translation is established.

After a successful INITIALIZE DEVICE PARAMETERS command the content of all IDENTIFY DEVICE words shall comply with 6.2.1 in addition to the following:

- 1) The content of words 1, 3, 6, and (61:60) shall be unchanged.
- 2) The content of word 55 shall equal (Max head value requested by the host + 1).
- 3) The content of word 56 shall equal (Logical sectors per logical track value requested by the host).
- 4) If the content of word (61:60) is less than or equal to 16,514,064, then word 54 shall equal the whole number result of  $[(\text{content of words (61:60)}) \div [(\text{new content of word 55 as determined by the successful INITIALIZE DEVICE PARAMETERS command}) * (\text{new content of word 56 as determined by the successful INITIALIZE DEVICE PARAMETERS command})]]$ , or 65,535 whichever is less.
- 5) If the content of word (61:60) is greater than 16,514,064, then word 54 shall equal the whole number result of  $[(16,514,064) \div [(\text{new content of word 55 as determined by the successful INITIALIZE DEVICE PARAMETERS command}) * (\text{new content of word 56 as determined by the successful INITIALIZE DEVICE PARAMETERS command})]]$  or 65,535 whichever is less.
- 6) Words (58:57) shall equal  $[(\text{new content of word 54}) * (\text{new content of word 55}) * (\text{new content of word 56})]$ .

## 8.17 MEDIA EJECT

### 8.17.1 Command code

EDh

### 8.17.2 Feature set

Removable Media Status Notification feature set

- Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media Status Notification feature set.
- Prohibited for devices implementing the PACKET command feature set.

Removable Media feature set

- Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media feature set.
- Prohibited for devices implementing the PACKET command feature set.

### 8.17.3 Protocol

Non-data command (see 9.4).

### 8.17.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	EDh							

Device/Head register -  
DEV shall indicate the selected device.

### 8.17.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

### 8.17.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	NM	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.  
NM (No Media) shall be set to one if no media is present in the device.  
Device/Head register -

DEV shall indicate the selected device.

Status register -

- BSY shall be cleared to zero indicating command completion.
- DRDY shall be set to one.
- DF (Device Fault) shall be set to one if a device fault has occurred.
- DRQ shall be cleared to zero.
- ERR shall be set to one if an Error register bit is set to one.

**8.17.7 Prerequisites**

DRDY set equal to one.

**8.17.8 Description**

This command causes any pending operations to complete, spins down the device if needed, unlocks the media if locked, and ejects the media. The device keeps track of only one level of media lock.

**8.18 MEDIA LOCK**

**8.18.1 Command code**

DEh

**8.18.2 Feature set**

Removable Media Status Notification feature set

- Optional for devices not implementing the PACKET command feature set and implementing the Removable Media Status Notification feature set.
- Prohibited for device implementing the PACKET command feature set.

Removable Media feature set

- Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media feature set.
- Prohibited for devices implementing the PACKET command feature set.

**8.18.3 Protocol**

Non-data command (see 9.4).

**8.18.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	DEh							

Device/Head register -

DEV shall indicate the selected device.

### 8.18.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.18.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.

NM (No Media) shall be set to one if no media is present in the device.

MCR (Media Change Request) shall be set to one if the device is locked and a media change request has been detected by the device.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.18.7 Prerequisites

DRDY set equal to one.

### 8.18.8 Description

This command can be used to lock the media, if Media Status Notification is disabled. If Media Status Notification is enabled, this command will return good status (no ERR bit in the Status register) and perform no action.

If the media is unlocked and media is present, the media shall be set to the LOCKED state and no Error register bit shall be set to one. The device keeps track of only one level of media lock. Subsequent MEDIA LOCK commands, while the media is in the LOCKED state, do not set additional levels of media locks.

If the media is locked, the status returned shall indicate whether a media change request has been detected by the device. If a media change request has been detected, the MCR bit in the Error register and the ERR bit in the Status register shall be set to one.

When media is in the LOCKED state, the device shall respond to the media change request button, by setting the MCR bit in the Error register and the ERR bit in the Status register to one, until the media LOCKED condition is cleared.

## 8.19 MEDIA UNLOCK

### 8.19.1 Command code

DFh

### 8.19.2 Feature set

Removable Media Status Notification feature set

- Optional for devices not implementing the PACKET command feature set and implementing the Removable Media Status Notification feature set.
- Prohibited for devices implementing the PACKET command feature set.

Removable Media feature set

- Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media feature set.
- Prohibited for devices implementing the PACKET command feature set.

### 8.19.3 Protocol

Non-data command (see 9.4).

### 8.19.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	DFh							

Device/Head register -

DEV shall indicate the selected device.



### 8.19.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.19.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	NM	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.

NM (No Media) shall be set to one if no media is present in the device.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.19.7 Prerequisites

DRDY set equal to one.

### 8.19.8 Description

This command can be used to unlock the device, if Media Status Notification is disabled. If Media Status Notification is enabled, this command will return good status (no ERR bit in the Status register) and perform no action.

If the media is present, the media shall be set to the UNLOCKED state and no Error register bit shall be set to one. The device keeps track of only one level of media lock. A single MEDIA UNLOCK command unlocks the media.

If a media change request has been detected by the device prior to the issuance of this command, the media shall be ejected at MEDIA UNLOCK command completion.

## 8.20 NOP

### 8.20.1 Command code

00h

### 8.20.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.
- Mandatory for devices implementing the Overlapped feature set.

### 8.20.3 Protocol

Non-data (see 9.4).

### 8.20.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	00h							

Features register -

Subcommand code	Description	Action
00h	NOP	Return command aborted and abort any outstanding queued <b>commands</b> .
01h	NOP Auto Poll	Return command aborted and do not abort any outstanding queued <b>commands</b> .
02h-FFh	Reserved	Return command aborted and do not abort any outstanding queued <b>commands</b> .

Device/Head register -

DEV shall indicate the selected device.

### 8.20.5 Normal outputs

This command always fails with an error.

## 8.20.6 Error outputs

The Command Block registers, other than the Error and Status registers, are not changed by this command. This command always fails with the device returning command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	Initial value							
Sector Number	Initial value							
Cylinder Low	Initial value							
Cylinder High	Initial value							
Device/Head	Initial value							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one.

Sector Count, Sector Number, Cylinder Low, Cylinder High, Device/Head - value set by host is not changed.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one.

## 8.20.7 Prerequisites

DRDY set equal to one.

## 8.20.8 Description

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

## 8.21 PACKET

### 8.21.1 Command code

A0h

### 8.21.2 Feature set

PACKET Command feature set

- Use prohibited for devices not implementing the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.

### 8.21.3 Protocol

Packet (see 9.8).

## 8.21.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na	na	na	na	na	na	OVL	DMA
Sector Count	Tag					na		
Sector Number	na							
Byte count low (Cylinder Low)	Byte count limit (7-0)							
Byte count high (Cylinder High)	Byte count limit (15-8)							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	A0h							

Features register -

OVL - This bit is set to one to inform the device that the PACKET command is to be overlapped.

DMA - This bit is set to one to inform the device that the data transfer (not the command packet transfer) associated with this command is via DMA or Ultra DMA mode.

Sector Count register -

Tag - If the device supports command queuing, this field contains the command Tag for the command being delivered. A Tag may have any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this field is not applicable.

Byte count low and Byte count high registers -

These registers are written by the host with the maximum byte count that is to be transferred in any single DRQ assertion for PIO transfers. The byte count does not apply to the command PACKET transfer. If the PACKET command does not transfer data, the byte count is ignored.

If the PACKET command results in a data transfer:

- 1) the host shall not set the byte count limit to zero. If the host sets the byte count limit to zero the device shall return command aborted;
- 2) the value set into the byte count limit shall be even if the total requested data transfer length is greater than the byte count limit;
- 3) the value set into the byte count limit may be odd if the total requested data transfer length is equal to or less than the byte count limit;
- 4) the value FFFFh is interpreted by the device as though the value were FFFEh.

Device/Head register -

DEV shall indicate the selected device.

## 8.21.5 Normal outputs

### 8.21.5.1 Awaiting command

When the device is ready to accept the command packet from the host the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7:0)							
Byte count high (Cylinder High)	Byte count (15:8)							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Byte count High/Low - shall reflect the value set by the host when the command was issued.

## Interrupt reason register -

Tag - If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be cleared to zero indicating transfer to the device.

C/D - Shall be set to one indicating the transfer of a command packet.

## Device/Head register -

DEV shall indicate the selected device.

## Status register -

BSY - Shall be cleared to zero.

DRDY - na.

DMRD (DMA ready) - Shall be cleared to zero.

SERV (Service) - Shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DRQ - Shall be set to one.

CHK - Shall be cleared to zero.

**8.21.5.2 Data transmission**

If overlap is not supported or not indicated by the command, data transfer shall occur after the receipt of the command packet. If overlap is supported and the command indicates that the command may be overlapped, data transfer may occur after receipt of the command packet or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7:0)							
Byte count high (Cylinder High)	Byte count (15:8)							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Byte count High/Low - If the transfer is to be in PIO mode, the byte count of the data to be transferred for this DRQ assertion shall be presented.

Valid byte count values are as follows:

- 1) the byte count shall be less than or equal to the byte count limit value from the host;
- 2) the byte count shall not be zero;
- 3) the byte count shall be less than or equal to FFFh;
- 4) the byte count shall be even except for the last transfer of a command;
- 5) if the byte count is odd, the last valid byte transferred is on DD[7:0] and the data on DD[15:8] is a pad byte of undefined value;
- 6) if the last transfer of a command has a pad byte, the byte count shall be odd.

## Interrupt reason register -

Tag - If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be cleared to zero if the transfer is to the device. Shall be set to one if the transfer is to the host.

C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY - Shall be cleared to zero.

DRDY - na.

DMRD (DMA ready) - Shall be set to one if the transfer is to be a DMA or Ultra DMA transfer and the device supports overlap DMA.

SERV (Service) - Shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DRQ - Shall be set to one.

CHK - Shall be cleared to zero.

### 8.21.5.3 Bus release (overlap feature set only)

After receiving the command packet, the device sets BSY to one and clears DRQ to zero. If the command packet requires a data transfer, the OVL bit is set to one, and the device is not prepared to immediately transfer data, the device may perform a bus release by placing the following register content. If the command packet requires a data transfer, the OVL bit is set to one, and the Release interrupt is enabled, the device shall perform a bus release by setting the register content as follows.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	na							
Byte count high (Cylinder High)	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Byte count High/Low - na.

Interrupt reason register -

Tag - If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be set to one.

I/O - Shall be cleared to zero.

C/D - Shall be cleared to zero.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY - Shall be cleared to zero indicating bus release.

DRDY - na.

DMRD (DMA ready) - Shall be cleared to zero.

SERV (Service) - Shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DRQ - Shall cleared to zero.

CHK - Shall be cleared to zero.

### 8.21.5.4 Service request (overlap feature set only)

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see 6.9). When the SERVICE command is received, the device shall set outputs as described in data transfer, successful command completion, or error outputs depending on the service the device requires.

### 8.21.5.5 Successful command completion

When the device has command completion without error, the device sets the following register content.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	na							
Byte count high (Cylinder High)	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Byte count High/Low -na.

Interrupt reason register -

Tag - If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one.

C/D - Shall be set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY - Shall be cleared to zero indicating command completion.

DRDY - Shall be set to one.

DMRD (DMA ready) - na.

SERV (Service) - Shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DRQ - Shall be cleared to zero.

CHK - Shall be cleared to zero.

### 8.21.6 Error outputs

The device shall not terminate the PACKET command with an error before the last byte of the command packet has been written (see 9.8).

Register	7	6	5	4	3	2	1	0
Error	Sense key				na	ABRT	EOM	ILI
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	SERV	DRQ	na	na	CHK

#### Error register -

Sense Key is a command packet set specific error indication.

ABRT shall be set to one if the requested command has been command aborted because the command code or a command parameter is invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

EOM - the meaning of this bit is command set specific. See the appropriate command set standard for the definition of this bit.

ILI - the meaning of this bit is command set specific. See the appropriate command set standard for the definition of this bit.

#### Interrupt reason register -

Tag - If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one.

C/D - Shall be set to one.

#### Device/Head register -

DEV shall indicate the selected device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SERV (Service) - Shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

CHK shall be set to one if an Error register sense key or code bit is set.

### 8.21.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

### 8.21.8 Description

The PACKET command is used to transfer a device command via a command packet. If the native form of the encapsulated command is shorter than the packet size reported in bits 1 and 0 of word 0 of the IDENTIFY PACKET DEVICE response, the encapsulated command shall begin at byte 0 of the packet. Packet bytes beyond the end of the encapsulated command are reserved.

If the device supports overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, the device may or may not perform a bus release. If the device is ready for the data transfer, the device may begin the transfer immediately as described in the non-overlapped protocol (see 9.8). If the data is not ready, the device may perform a bus release and complete the transfer after the execution of a SERVICE command.



## 8.22 READ BUFFER

### 8.22.1 Command code

E4h

### 8.22.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.22.3 Protocol

PIO data-in (see 9.5).

### 8.22.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E4h							

Device/Head register -

DEV shall indicate the selected device.

### 8.22.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.22.6 Error outputs

The device shall return command aborted if the command is not supported.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.22.7 Prerequisites

DRDY set equal to one. The command prior to a READ BUFFER command shall be a WRITE BUFFER command.

### 8.22.8 Description

The READ BUFFER command enables the host to read the current contents of the device's sector buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

## 8.23 READ DMA

### 8.23.1 Command code

C8h

### 8.23.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.23.3 Protocol

DMA (see 9.7).

### 8.23.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	C8h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

### 8.23.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.23.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

#### Device/Head register -

DEV shall indicate the selected device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.23.7 Prerequisites

DRDY set equal to one. The host shall initialize the DMA channel.

### 8.23.8 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

## 8.24 READ DMA QUEUED

### 8.24.1 Command code

C7h

### 8.24.2 Feature set

Overlapped feature set

- Mandatory for devices implementing the Overlapped feature set but not implementing the PACKET command feature set.
- Use prohibited for devices implementing the PACKET command feature set.

### 8.24.3 Protocol

DMA QUEUED (see 9.9).

### 8.24.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	C7h							

Features -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector count -

if the device supports command queuing, bits (7:3) contain the Tag for the command being delivered. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this field is not applicable.

Sector number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

### 8.24.5 Normal outputs

#### 8.24.5.1 Data transmission

Data transfer may occur after receipt of the command or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	SERV	DRQ	na	na	CHK

Interrupt reason register -

- Tag - This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.
- REL - Shall be set to one if a released command is outstanding.
- I/O - Shall be set to one indicating the transfer is to the host.
- C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register -

DEV shall indicate the selected device.

Status register -

- BSY - Shall be cleared to zero.
- DRDY - Shall be set to one.
- DF (Device Fault) - Shall be cleared to zero
- SERV (Service) - Shall be set to one if another command is ready to be serviced.
- DRQ - Shall be set to one.
- CHK - Shall be cleared to zero.

**8.24.5.2 Release**

If the device performs a bus release before transferring data for this command, the register content upon performing a bus release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Sector Count register -

- Tag - If the device supports command queuing, this field shall contain the Tag of the command being bus released. If the device does not support command queuing, this field shall be zeros.
- REL shall be set to one.
- I/O shall be zero.
- C/D shall be zero.

Device/Head register -

DEV shall indicate the selected device.

Status register -

- BSY shall be cleared to zero indicating bus release.
- DRDY shall be set to one.
- SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service. SERV shall be set to one when the device has prepared this command for service.
- DF (Device Fault) shall be cleared to zero
- DRQ bit shall be cleared to zero.
- ERR bit shall be cleared to zero.

**8.24.5.3 Service request**

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see 6.9). When the SERVICE command is received, the device shall set outputs as described in data transfer, command completion, or error outputs depending on the service the device requires.

### 8.24.5.4 Command completion

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Sector Count register -

Tag - If the device supports command queuing, this field shall contain the Tag of the completed command. If the device does not support command queuing, this field shall be zeros.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SERV (Service) shall be cleared to zero when no other queued command is ready for service.

SERV shall be set to one when another queued command is ready for service.

DF (Device Fault) shall be cleared to zero.

DRQ bit shall be cleared to zero.

ERR bit shall be cleared to zero.

### 8.24.6 Error outputs

The Sector Count register contains the Tag for this command if the device supports command queuing. The device shall return command aborted if the command is not supported or if the device has not had overlapped interrupt enabled. The device shall return command aborted if the device supports command queuing and the Tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	Tag					REL	I/O	C/D
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if ABRT is not set to one.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count register -

Tag - If the device supports command queuing, this field shall contain the Tag of the completed command. If the device does not support command queuing, this field shall be zeros.

REL shall be cleared to zero.

I/O shall be set to one.

Bit 0 - C/D shall be set to one.

Sector Number, Cylinder Low, Cylinder High, Device/Head -

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SERV (Service) shall be cleared to zero when no other queued command is ready for service.

SERV shall be set to one when another queued command is ready for service.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.24.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

### 8.24.8 Description

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or may execute the data transfer without performing a bus release if the data is ready to transfer.

## 8.25 READ MULTIPLE

### 8.25.1 Command code

C4h

### 8.25.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.



### 8.25.3 Protocol

PIO data-in (see 9.5).

### 8.25.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	C4h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

### 8.25.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.25.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error register -

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

#### Sector Number, Cylinder Low, Cylinder High, Device/Head -

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.25.7 Prerequisites

DRDY set equal to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall precede a READ MULTIPLE command.

### 8.25.8 Description

The READ MULTIPLE command performs the same as the READ SECTOR(S) command except that when the device is ready to transfer data for a block of sectors, the device clears BSY, sets DRDY and DRQ (and sets DF, ERR, and the bits in the Error register, as required), and enters the interrupt pending state only before the data transfer for the first sector of the block sectors. The remaining sectors for the block are transferred without the device asserting INTRQ. In addition, the DRQ qualification of the transfer is required only before the first sector of a block, not before each sector of the block.

The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits 0-7 in word 47 in the IDENTIFY DEVICE information.

If bit 8 equals 1 and bits 0-7 are equal to zero in word 59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts shall be programmed by the SET MULTIPLE MODE command before issuing the first READ MULTIPLE or WRITE MULTIPLE command after a power on or hardware reset. If bit 8 in word 1 equals one and bits 0-7 are not equal to zero in word

59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts may be reprogrammed by the SET MULTIPLE MODE command before issuing the next READ MULTIPLE or WRITE MULTIPLE command.

When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for  $n$  sectors, where  $n = \text{remainder}(\text{sector count} / \text{block count})$ .

If the READ MULTIPLE command is received when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with command aborted.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set to one and the data transfer shall take place, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

## 8.26 READ NATIVE MAX ADDRESS

### 8.26.1 Command code

F8h

### 8.26.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set is implemented.
- Use prohibited when Removable feature set is implemented.

### 8.26.3 Protocol

Non-data command (see 9.4).

### 8.26.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	LBA	obs	DEV	na			
Command	F8h							

Device/Head -

- If LBA is set to one, the maximum address shall be reported as an LBA value.
- If LBA is cleared to zero, the maximum address shall be reported as a CHS value.
- DEV shall indicate the selected device.

### 8.26.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Native max address sector number or LBA							
Cylinder Low	Native max address cylinder low or LBA							
Cylinder High	Native max address cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Native max address head or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Sector Number -

maximum native sector number (IDENTIFY DEVICE word 6) or LBA bits (7:0) for native max address on the device.

Cylinder Low -

maximum native cylinder number low or LBA bits (15:8) for native max address on the device.

Cylinder High -

maximum native cylinder number high or LBA bits (23:16) for native max address on device.

Device/Head -

maximum native head number (IDENTIFY DEVICE word 3 minus one) or LBA bits (27:24) for native max address on the device.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.26.6 Error outputs

If this command is not supported the device shall return command aborted. The device shall return command aborted if a CHS address is requested and the device does not support a CHS translation.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be set to one if an Error register bit is set to one.

### 8.26.7 Prerequisites

DRDY set equal to one.

### 8.26.8 Description

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS command.

## 8.27 READ SECTOR(S)

### 8.27.1 Command code

20h

### 8.27.2 Feature set

General feature set

- Mandatory for all devices.
- PACKET Command feature set devices (see 8.27.5.2).

### 8.27.3 Protocol

PIO data-in (see 9.5).

### 8.27.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	20h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

## 8.27.5 Outputs

### 8.27.5.1 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.27.5.2 Outputs for PACKET Command feature set devices

In response to this command, devices that implement the PACKET Command feature set shall post command aborted and place the PACKET Command feature set signature in the Cylinder High and the Cylinder Low register (see 9.12).

## 8.27.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an

address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

**8.27.7 Prerequisites**

DRDY set equal to one.

**8.27.8 Description**

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer shall begin at the sector specified in the Sector Number register.

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition.

**8.28 READ VERIFY SECTOR(S)**

**8.28.1 Command code**

40h

**8.28.2 Feature set**

General feature set

- Mandatory for all devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

**8.28.3 Protocol**

Non-data (see 9.4).

**8.28.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	40h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

### 8.28.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.28.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an



address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

**8.28.7 Prerequisites**

DRDY set equal to one.

**8.28.8 Description**

This command is identical to the READ SECTOR(S) command, except that the DRQ bit is never set to one, and no data is transferred to the host.

**8.29 SECURITY DISABLE PASSWORD**

**8.29.1 Command code**

F6h

**8.29.2 Feature set**

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

**8.29.3 Protocol**

PIO data-out (see 9.6).

**8.29.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	F6h							

Device/Head register -

DEV shall indicate the selected device.

### 8.29.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.29.6 Error outputs

The device shall return command aborted if the command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.29.7 Prerequisites

DRDY set equal to one. Device shall be in Unlocked mode.

### 8.29.8 Description

The SECURITY DISABLE PASSWORD command requests a transfer of a single sector of data from the host. Table 23 defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the Lock mode. This command does not change the Master password that may be reactivated later by setting a User password (see 6.13).

**Table 23 – Security password content**

Word	Content
0	Control word Bit 0 Identifier 0=compare User password 1=compare Master password Bit 1-15 Reserved
1-16	Password (32 bytes)
17-255	Reserved

## 8.30 SECURITY ERASE PREPARE

### 8.30.1 Command code

F3h

### 8.30.2 Feature set

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

### 8.30.3 Protocol

Non-data (see 9.4).

### 8.30.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	F3h							

Device/Head register -

DEV shall indicate the selected device.

### 8.30.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.30.6 Error outputs

The device shall return command aborted if the command is not supported or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported or device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.30.7 Prerequisites

DRDY set equal to one.

### 8.30.8 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental erase of the device.

## 8.31 SECURITY ERASE UNIT

### 8.31.1 Command code

F4h

### 8.31.2 Feature set

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

### 8.31.3 Protocol

PIO data-out (see 9.6).

**8.31.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	F4h							

Device/Head register -  
DEV shall indicate the selected device.

**8.31.5 Normal outputs**

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

**8.31.6 Error outputs**

The device shall return command aborted if the command is not supported, the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported, device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

**8.31.7 Prerequisites**

DRDY set equal to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

**8.31.8 Description**

This command requests transfer of a single sector of data from the host. Table 24 defines the content of this sector of information. If the password does not match the password previously saved by the device, the device rejects the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device command aborts the SECURITY ERASE UNIT command.

When normal erase mode is selected, the SECURITY ERASE UNIT command writes binary zeroes to all user data areas. The enhanced erase mode is optional. When enhanced erase mode is selected, the device writes predetermined data patterns to all user data areas. In enhanced mode, all previously written user data is overwritten, including sectors that are no longer in use due to reallocation.

This command disables the device Lock mode, however, the Master password is still stored internally within the device and may be reactivated later when a new User password is set.

**Table 24 – SECURITY ERASE UNIT password**

Word	Content
0	Control word Bit 0 Identifier 0=compare User password 1=compare Master password Bit 1 Erase mode 0=Normal erase 1=Enhanced erase Bit 2-15 Reserved
1-16	Password (32 bytes)
17-255	Reserved

**8.32 SECURITY FREEZE LOCK**

**8.32.1 Command code**

F5h

### 8.32.2 Feature set

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

### 8.32.3 Protocol

Non-data (see 9.4).

### 8.32.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	F5h							

Device/Head register -

DEV shall indicate the selected device.

### 8.32.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.32.6 Error outputs

The device shall return command aborted if the command is not supported, or the device is in Locked mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported or device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.32.7 Prerequisites

DRDY set equal to one.

### 8.32.8 Description

The SECURITY FREEZE LOCK command sets the device to Frozen mode. After command completion any other commands that update the device Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If SECURITY FREEZE LOCK is issued when the device is in Frozen mode, the command executes and the device remains in Frozen mode.

Commands disabled by SECURITY FREEZE LOCK are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT

## 8.33 SECURITY SET PASSWORD

### 8.33.1 Command code

F1h

### 8.33.2 Feature set

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

### 8.33.3 Protocol

PIO data-out (see 9.6).



### 8.33.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	F1h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.33.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

### 8.33.6 Error outputs

The device shall return command aborted if the command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if this command is not supported, if device is in Frozen mode, or if device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.  
 DF (Device Fault) shall be set to one if a device fault has occurred.  
 DRQ shall be cleared to zero.  
 ERR shall be set to one if an Error register bit is set to one.

**8.33.7 Prerequisites**

DRDY set equal to one.

**8.33.8 Description**

This command requests a transfer of a single sector of data from the host. Table 25 defines the content of this sector of information. The data transferred controls the function of this command. Table 26 defines the interaction of the identifier and security level bits.

The revision code field is returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0000h to FFFDh. The initial factory shipped value of Master Password Revision Code shall be FFFEh. Value FFFFh is reserved.

**Table 25 – SECURITY SET PASSWORD data content**

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set User password 1=set Master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17	Master Password Revision Code (valid if word 0 bit 0 = 1)		
18-255	Reserved		

**Table 26 – Identifier and security level bit interaction**

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be used to unlock the device.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

**8.34 SECURITY UNLOCK**

**8.34.1 Command code**

F2h

### 8.34.2 Feature set

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

### 8.34.3 Protocol

PIO data-out (see 9.6).

### 8.34.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	F2h							

Device/Head register -

DEV shall indicate the selected device.

### 8.34.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.34.6 Error outputs

The device shall return command aborted if the command is not supported, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported or if device is in Frozen mode. ABRT may

be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.34.7 Prerequisites

DRDY set equal to one.

### 8.34.8 Description

This command requests transfer of a single sector of data from the host. Table 23 defines the content of this sector of information.

If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device compares the supplied password with the stored User password.

If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT commands are command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

## 8.35 SEEK

### 8.35.1 Command code

70h

### 8.35.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.35.3 Protocol

Non-data (see 9.4).

### 8.35.4 Inputs

The Cylinder High register, the Cylinder Low register, the head portion of Device/Head register, and the Sector Number register contain the address of a sector that the host may request in a subsequent command.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	70h							

Sector Number -

sector number or LBA address bits (7:0).

Cylinder Low -

cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) head number or LBA address bits (27:24).

### 8.35.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	DSC	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DSC (Device Seek Complete) shall be set to one concurrent with or after the setting of DRDY to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.35.6 Error outputs

Some devices may not report IDNF because they do not range check the address values requested by the host.

Register	7	6	5	4	3	2	1	0
Error	na	na	MC	IDNF	MCR	ABRT	NM	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.35.7 Prerequisites

DRDY set equal to one.

### 8.35.8 Description

This command allows the host to provide advanced notification that particular data may be requested by the host in a subsequent command. DSC shall be set to one concurrent with or after the setting of DRDY to one when updating the Status register for this command.

## 8.36 SERVICE

### 8.36.1 Command code

A2h

### 8.36.2 Feature set

Overlap and Queued feature sets

- Mandatory when the PACKET, Overlapped feature set is implemented.

### 8.36.3 Protocol

PACKET or READ/WRITE DMA QUEUED (see 9.8 and 9.9).

### 8.36.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	A2h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.36.5 Outputs

Outputs as a result of a SERVICE command are described in the command description for the command for which SERVICE is being requested.

### 8.36.6 Prerequisites

The device shall have performed a bus release for a previous overlap PACKET, READ DMA QUEUED, or WRITE DMA QUEUED command and shall have set the SERV bit to one to request the SERVICE command be issued to continue data transfer and/or provide command status (see 8.37.18).

### 8.36.7 Description

The SERVICE command is used to provide data transfer and/or status of a command that was previously bus released.

## 8.37 SET FEATURES

### 8.37.1 Command code

EFh

### 8.37.2 Feature set

General feature set

- Mandatory for all devices.
- Set transfer mode subcommand is mandatory.
- Enable/disable write cache subcommands are mandatory when a write cache is implemented.
- Enable/Disable Media Status Notification sub commands are mandatory if the Removable Media feature set is implemented.
- All other subcommands are optional.

### 8.37.3 Protocol

Non-data (see 9.4).

### 8.37.4 Inputs

Table 27 defines the value of the subcommand in the Feature register. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Subcommand specific							
Sector Number	Subcommand specific							
Cylinder Low	Subcommand specific							
Cylinder High	Subcommand specific							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	EFh							

Device/Head register -  
DEV shall indicate the selected device.

### 8.37.5 Normal outputs

See the subcommand descriptions.

### 8.37.6 Error outputs

If any subcommand input value is not supported or is invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if this subcommand is not supported or if value is invalid. ABRT may be set

to one if the device is not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be set to one if a device fault has occurred.  
DRQ shall be cleared to zero.  
ERR shall be set to one if an Error register bit is set to one.

### 8.37.7 Prerequisites

DRDY shall be set to one.

### 8.37.8 Description

This command is used by the host to establish parameters that affect the execution of certain device features. Table 27 defines these features.

At power on, or after a hardware reset, the default setting of the functions specified by the subcommands are vendor specific.



**Table 27 – SET FEATURES register definitions**

Value (see note)	
01h	Retired
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register. Table 28 defines values.
04h	Obsolete
05h	Enable advanced power management
06h	Enable Power-Up In Standby feature set.
07h	Power-Up In Standby feature set device spin-up.
09h	Reserved for Address offset reserved area boot method technical report
0Ah	Enable CFA power mode 1
31h	Disable Media Status Notification
33h	Obsolete
44h	Obsolete
54h	Obsolete
55h	Disable read look-ahead feature
5Dh	Enable release interrupt
5Eh	Enable SERVICE interrupt
66h	Disable reverting to power on defaults
77h	Obsolete
81h	Retired
82h	Disable write cache
84h	Obsolete
85h	Disable advanced power management
86h	Disable Power-Up In Standby feature set.
88h	Obsolete
89h	Reserved for Address offset reserved area boot method technical report
8Ah	Disable CFA power mode 1
95h	Enable Media Status Notification
99h	Obsolete
9Ah	Obsolete
AAh	Enable read look-ahead feature
ABh	Obsolete
BBh	Obsolete
CCh	Enable reverting to power on defaults
DDh	Disable release interrupt
DEh	Disable SERVICE interrupt
NOTE – All values not shown are reserved for future definition.	

### 8.37.9 Enable/disable write cache

Subcommand codes 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before command completion (see 8.10).

### 8.37.10 Set transfer mode

A host selects the transfer mechanism by Set Transfer Mode, subcommand code 03h, and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode and one DMA mode shall be selected at all times. The host may change the selected modes by the SET FEATURES command.

**Table 28 – Transfer mode values**

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode
Retired	00010b	na
Multiword DMA mode	00100b	mode
Ultra DMA mode	01000b	mode
Reserved	10000b	na
mode = transfer mode number		

If a device supports this standard, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000000b”, the device shall set the default PIO mode. If the value is “00000001b” and the device supports disabling of IORDY, then the device shall set the default PIO mode and disable IORDY. A device shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

Devices reporting support for Multi Word DMA mode 1 shall also support Multi Word DMA mode 0. A device shall support all Multi Word DMA modes below the highest mode supported, e.g., if Multi Word DMA mode 1 is supported Multi Word DMA mode 0 shall be supported.

A device shall support all Ultra DMA modes below the highest mode supported, e.g., if Ultra DMA mode 1 is supported Ultra DMA mode 0 shall be supported.

If an Ultra DMA mode is enabled any previously enabled Multi Word DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device.

For systems using a cable assembly, the host shall detect that an 80-conductor cable assembly is connecting the host with the device(s) before enabling any Ultra DMA mode greater than 2 in the device(s) (see Annex D).

### 8.37.11 Enable/disable advanced power management

Subcommand code 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a SET FEATURES command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table 29 shows these values.

**Table 29 – Advanced power management levels**

Level	Sector Count value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h

and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Subcommand code 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement SET FEATURES subcommand 05h.

### 8.37.12 Enable/disable Power-Up In Standby feature set

Subcommand code 06h enables the Power-Up In Standby feature set. When this feature set is enabled, the device shall power-up into Standby mode, i.e., the device shall be ready to receive commands but shall not spinup (see 6.18). Having been enabled, this feature shall remain enabled through power-down, hardware reset and software rest.

Subcommand code 86h disables the Power-Up In Standby feature set. When this feature set is disabled, the device shall power-up into Active mode. The factory default for this feature set shall be disabled.

### 8.37.13 Enable/disable CFA power mode 1

Subcommand code 0Ah enables CFA Power Mode 1. CFA devices may consume up to 500 mA maximum average RMS current for either 3.3V or 5V operation in Power Mode 1. CFA devices revert to Power Mode 1 on hardware or power on reset. CFA devices revert to Power Mode 1 on Soft Reset except when Set Features disable reverting to power on defaults is set (see 8.12.56). Enabling CFA Power Mode 1 does not spin up rotating media devices.

Subcommand 8Ah disables CFA Power Mode 1, placing the device to CFA Power Mode 0. CFA devices may consume up to 75 mA maximum average RMS current for 3.3V or 100 mA maximum average RMS current for 5V operation in Power Mode 0.

A device in Power Mode 0 the device shall accept the following commands:

Identify Device

Set Features (function codes 0Ah and 8Ah)

Standby

Standby Immediate

Sleep

Check Power Mode

Execute Device Diagnostics

Request Sense

A device in Power Mode 0 may accept any command that the device is capable of executing within the Power Mode 0 current restrictions. Commands that require more current than specified for Power Mode 0 shall be rejected with an abort error.

### 8.37.14 Power-Up In Standby feature set device spin-up

Subcommand code 07h shall cause a device that has powered-up into Standby to go to the Active state (see 6.18 and Figure 9).

### 8.37.15 Enable/disable Media Status Notification

Subcommand code 31h disables Media Status Notification and leaves the media in an unlocked state. If Media Status Notification is disabled when this subcommand is received, the subcommand has no effect.

Subcommand code 95h enables Media Status Notification and clears any previous media lock state. This subcommand returns the device capabilities for media eject, media lock, previous state of Media Status Notification and the current version of Media Status Notification supported in the Cylinder Low and Cylinder High registers as described below.

Register	7	6	5	4	3	2	1	0
Cylinder Low	VER							
Cylinder High	r	r	r	r	r	PEJ	LOCK	PENA

Cylinder Low register -

VER shall contain the Media Status Notification version supported by the device (currently 0x00h)

Cylinder High register -

PENA shall be set to one if Media Status Notification was enabled prior to the receipt of this command,

LOCK shall be set to one if the device is capable of locking the media preventing manual ejection.

PEJ shall be set to one if the device has a power eject mechanism that is capable of physically ejecting the media when a MEDIA EJECT command is sent to the device. This bit must be set to zero if the device only unlocks the media when the device receives a MEDIA EJECT command.

r (reserved) shall be cleared to zero.

### 8.37.16 Enable/disable read look-ahead

Subcommand codes AAh and 55h allow the host to request the device to enable or disable read look-ahead. Error recovery performed by the device is vendor specific.

### 8.37.17 Enable/disable release interrupt

Subcommand codes 5Dh and DDh allow a host to enable or disable the asserting INTRQ if nIEN is cleared to zero when a device releases the bus for an overlapped PACKET command.

### 8.37.18 Enable/disable SERVICE interrupt

Subcommand codes 5Eh and DEh allow a host to enable or disable the asserting of an interrupt when DRQ is set to one in response to a SERVICE command.

### 8.37.19 Enable/disable reverting to defaults

Subcommand codes CCh and 66h allow the host to enable or disable the device from reverting to power on default values. A setting of 66h allows settings that may have been modified since power on to remain at the same setting after a software reset.

## 8.38 SET MAX ADDRESS

### 8.38.1 Command code

F9h

### 8.38.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set is implemented.
- Use prohibited when the Removable feature set is implemented.

### 8.38.3 Protocol

Non-data command (see 9.4).

### 8.38.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							VV
Sector Number	Native max address sector number or set max LBA							
Cylinder Low	Set max cylinder low or LBA							
Cylinder High	Set max cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Native max address head number or set max LBA			
Command	F9h							

#### Sector Count -

VV (Value volatile). If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

#### Sector Number -

contains the native max address sector number (IDENTIFY DEVICE word 6) or LBA bits (7:0) value to be set.

#### Cylinder Low -

contains the maximum cylinder low or LBA bits (15:8) value to be set.

#### Cylinder High -

contains the maximum cylinder high or LBA bits (23:16) value to be set.

#### Device/Head -

if LBA is set to one, the maximum address value is an LBA value.

If LBA is cleared to zero, the maximum address value is a CHS value.

DEV shall indicate the selected device.

Bits (3:0) contain the native max address head number (IDENTIFY DEVICE word 3 minus one) or LBA bits (27:24) value to be set.

### 8.38.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Native max sector number or max LBA							
Cylinder Low	Max cylinder low or LBA							
Cylinder High	Max cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Native max head or max LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Sector Number -

maximum native sector number or LBA bits (7:0) set on the device.

#### Cylinder Low -

maximum cylinder number low or LBA bits (15:8) set on the device.

#### Cylinder High -

maximum cylinder number high or LBA bits (23:16) set on device.

#### Device/Head -

DEV shall indicate the selected device.

maximum native head number or LBA bits (27:24) set on the device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.38.6 Error outputs

If this command is not supported or the maximum value to be set exceeds the capacity of the device, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported, maximum value requested exceeds the device capacity, the set max cylinder number is greater than 16,383, or the command is not immediately preceded by a READ NATIVE MAX ADDRESS command. ABRT may be set to one if the device is not able to complete the action requested by the command.

IDNF shall be set to one if the command was the second non-volatile SET MAX ADDRESS command after power on or hardware reset.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be set to one if an Error register bit is set to one.

### 8.38.7 Prerequisites

DRDY set equal to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.

### 8.38.8 Description

This command allows the host to redefine the maximum address of the user-accessible address space in either LBA translation or the current CHS translation. The host may either set a new maximum cylinder number for CHS translation or a new maximum LBA address for LBA translation. After a successful SET MAX ADDRESS command using a new maximum cylinder number value the content of all IDENTIFY DEVICE words shall comply with 6.2.1 in addition to the following:

- 1) The content of words 3, 6, 55, and 56 are unchanged
- 2) The content of word 1 shall equal (the new Set max cylinder number + 1) or 16,383, whichever is less
- 3) The content of words (61:60) shall equal [(the new content of word 1 as determined by the successful SET MAX ADDRESS command) \* (the content of word 3) \* (the content of word 6)]
- 4) If the content of words (61:60) as determined by a successful SET MAX ADDRESS command is less than 16,514,064, then the content of word 54 shall be equal to [(the content of words (61:60)) ÷ ((the content of IDENTIFY DEVICE word 55) \* (the content of word 56))] or 65,535, whichever is less
- 5) If the content of word (61:60) as determined by a successful SET MAX ADDRESS command is greater than 16,514,064, then word 54 shall equal the whole number result of [[(16,514,064) ÷ [(the content of word 55) \* (the content of word 56)]]] or 65,535 whichever is less) The content of words (58:57) shall be equal to [(the new content of word 54 as determined by the successful SET MAX ADDRESS command) \* (the content of word 55) \* (the content of word 56)]

After a successful SET MAX ADDRESS command using a new maximum LBA address the content of all IDENTIFY DEVICE words shall comply with 6.2.1 in addition to the following:

- The content of words (61:60) shall be equal to the new Maximum LBA address + 1.

- If the content of words (61:60) is greater than 16,514,064 and if the device does not support CHS addressing, then the content of words 1, 3, 6, 54, 55, 56, and (58:57) shall equal zero.

If the device supports CHS addressing:

- The content of words 3, 6, 55, and 56 are unchanged.
- If the new content of words (61:60) is less than 16,514,064, then the content of word 1 shall be equal to  $[(\text{the new content of words (61:60)}) \div [(\text{the content of word 3}) * (\text{the content of word 6})]]$  or 65,535, whichever is less.
- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 1 shall be equal to 16,383.
- If the new content of words (61:60) is less than 16,514,064, then the content of word 54 shall be equal to  $[(\text{the new content of words (61:60)}) \div [(\text{the content of word 55}) * (\text{the content of word 56})]]$ .
- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 54 shall be equal to 16,383.
- Words (58:57) shall be equal to  $[(\text{the content of word 54}) * (\text{the content of word 55}) * (\text{the content of word 56})]$ .

After successful command completion, all read and write access attempts to addresses greater than specified by the successful SET MAX ADDRESS command shall be rejected with an “ID Not Found” error.

Hosts should not issue more than one non-volatile SET MAX ADDRESS command after a power on or hardware reset. Devices shall report an “ID Not Found” error upon receiving a second non-volatile SET MAX ADDRESS command after a power on or hardware reset.

The contents of IDENTIFY DEVICE words shall not be changed if a SET MAX ADDRESS command fails for any reason.

## 8.39 SET MULTIPLE MODE

### 8.39.1 Command code

C6h

### 8.39.2 Feature set

General feature set

Mandatory for devices not implementing the PACKET Command feature set.

Use prohibited for devices implementing the PACKET Command feature set.

### 8.39.3 Protocol

Non-data (see 9.4).

### 8.39.4 Inputs

If the content of the Sector Count register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value in bits 0-7 in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1, 2, 4, 8, 16, 32, 64 or 128.

If the content of the Sector Count register is zero and the SET MULTIPLE command completes without error, then the device shall respond to any subsequent READ MULTIPLE or WRITE MULTIPLE command with command aborted until a subsequent successful SET MULTIPLE command completion where the Sector Count register is not set to zero.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sectors per block							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	C6h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.39.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

### 8.39.6 Error outputs

If a block count is not supported, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if the block count is not supported. ABRT may be set to one if the device is  
not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be set to one if a device fault has occurred.  
DRQ shall be cleared to zero.



ERR shall be set to one if an Error register bit is set to one.

### 8.39.7 Prerequisites

DRDY set equal to one.

### 8.39.8 Description

This command establishes the block count for READ MULTIPLE and WRITE MULTIPLE commands.

Devices shall support the block size specified in the IDENTIFY DEVICE parameter word 47, bits 7 through 0, and may also support smaller values.

Upon receipt of the command, the device checks the Sector Count register. If the content of the Sector Count register is not zero, the Sector Count register contains a valid value, and the block count is supported, then the value in the Sector Count register is used for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and their execution is enabled. If the content of the Sector Count register is zero, the device may:

- 1) disable multiple mode and respond with command aborted to all subsequent READ MULTIPLE and WRITE MULTIPLE commands;
- 2) respond with command aborted to the SET MULTIPLE MODE command;
- 3) retain the previous multiple mode settings.

After a successful SET MULTIPLE command the device shall report the valid value set by that command in bits 0-7 in word 59 in the IDENTIFY DEVICE information.

## 8.40 SLEEP

### 8.40.1 Command code

E6h

### 8.40.2 Feature set

Power Management feature set.

- Power Management feature set is mandatory when power management is not implemented by a PACKET power management feature set.
- This command is mandatory when the Power Management feature set is implemented.

### 8.40.3 Protocol

Non-data command (see 9.4).

### 8.40.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E6h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.40.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.40.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the device does not support the Power Management feature set. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.40.7 Prerequisites

DRDY set equal to one.

### 8.40.8 Description

This command is the only way to cause the device to enter Sleep mode.

This command causes the device to set the BSY bit to one, prepare to enter Sleep mode, clear the BSY bit to zero and assert INTRQ. The host shall read the Status register in order to clear the interrupt and allow

the device to enter Sleep mode. In Sleep mode, the device only responds to the assertion of the RESET-signal and the writing of the SRST bit in the Device Control register and releases the device driven signal lines. The host shall not attempt to access the Command Block registers while the device is in Sleep mode.

Because some host systems may not read the Status register and clear the interrupt, a device may automatically release INTRQ and enter Sleep mode after a vendor specific time period of not less than 2 s.

The only way to recover from Sleep mode is with a software reset, a hardware reset, or a DEVICE RESET command.

A device shall not power on in Sleep mode nor remain in Sleep mode following a reset sequence.

## 8.41 SMART

Individual SMART commands are identified by the value placed in the Feature register. Table 30 shows these Feature register values.

**Table 30 – SMART Feature register values**

Value	Command
00h-CFh	Reserved
D0h	SMART READ DATA
D1h	Obsolete
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D3h	SMART SAVE ATTRIBUTE VALUES
D4h	SMART EXECUTE OFF-LINE IMMEDIATE
D5h	SMART READ LOG SECTOR
D6h	SMART WRITE LOG SECTOR
D7h	Obsolete
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS
DAh	SMART RETURN STATUS
DBh	obsolete
DCh-DFh	reserved
E0h-FFh	vendor specific

### 8.41.1 SMART DISABLE OPERATIONS

#### 8.41.1.1 Command code

B0h with a Feature register value of D9h.

#### 8.41.1.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

#### 8.41.1.3 Protocol

Non-data command (see 9.4).

#### 8.41.1.4 Inputs

The Features register shall be set to D9h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device/Head register -  
DEV shall indicate the selected device.

#### 8.41.1.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

#### 8.41.1.6 Error outputs

If the device does not support this command, if SMART is not enabled, or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if this command is not supported, if SMART is not enabled, or if input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.  
ERR shall be set to one if an Error register bit is set to one.

#### 8.41.1.7 Prerequisites

DRDY set equal to one. SMART enabled.

#### 8.41.1.8 Description

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After receipt of this command the device shall disable all SMART operations. SMART data shall no longer be monitored or saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles.

After receipt of this command by the device, all other SMART commands (including SMART DISABLE OPERATIONS commands), with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

### 8.41.2 SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

#### 8.41.2.1 Command code

B0h with a Feature register value of D2h.

#### 8.41.2.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

#### 8.41.2.3 Protocol

Non-data command (see 9.4).

#### 8.41.2.4 Inputs

The Features register shall be set to D2h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h. The Sector Count register is set to 00h to disable attribute autosave and a value of F1h is set to enable attribute autosave.

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device/Head register -  
DEV shall indicate the selected device.

### 8.41.2.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.41.2.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported, if SMART is disabled, or if the input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.41.2.7 Prerequisites

DRDY set equal to one. SMART enabled.

### 8.41.2.8 Description

This command enables and disables the optional attribute autosave feature of the device. Depending upon the implementation, this command may either allow the device, after some vendor specified event, to automatically save the device updated attribute values to non-volatile memory; or this command may cause

the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) shall be preserved by the device across power cycles.

A value of zero written by the host into the device's Sector Count register before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F1h written by the host into the device's Sector Count register before issuing this command shall cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command may differ from device to device. The meaning of any non-zero value written to this register at this time shall be preserved by the device across power cycles.

If this command is not supported by the device, the device shall return command aborted upon receipt from the host.

During execution of the autosave routine the device shall not set BSY to one nor clear DRDY to zero. If the device receives a command from the host while executing the autosave routine the device shall respond to the host within two seconds.

### 8.41.3 SMART ENABLE OPERATIONS

#### 8.41.3.1 Command code

B0h with a Feature register value of D8h.

#### 8.41.3.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

#### 8.41.3.3 Protocol

Non-data command (see 9.4).

#### 8.41.3.4 Inputs

The Features register shall be set to D8h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device/Head register -

DEV shall indicate the selected device.

**8.41.3.5 Normal outputs**

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

**8.41.3.6 Error outputs**

If the device does not support this command or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported or if the input register values are invalid.

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

**8.41.3.7 Prerequisites**

DRDY set equal to one.



### 8.41.3.8 Description

This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

### 8.41.4 SMART EXECUTE OFF-LINE IMMEDIATE

#### 8.41.4.1 Command code

B0h with the content of the Features register equal to D4h

#### 8.41.4.2 Feature set

SMART feature set.

- Optional when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

#### 8.41.4.3 Protocol

Non-data command (see 9.4).

#### 8.41.4.4 Inputs

The Features register shall be set to D4h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h. Table 31 defines the subcommand that shall be executed based on the value in the Sector Number register.

Register	7	6	5	4	3	2	1	0
Features	D4h							
Sector Count	na							
Sector Number	Subcommand specific							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na			
Command	B0h							

Device/Head register -  
DEV shall indicate the selected device.

#### 8.41.4.5 Normal Outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na or 4Fh							
Cylinder High	na or C2h							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Cylinder Low -  
na when the subcommand specified an off-line routine (including an off-line self-test routine).  
4Fh when the subcommand specified a captive self-test routine (see 8.41.4.8.2) that has executed without failure.

Cylinder High -

na when the subcommand specified an off-line routine (including an off-line self-test routine).  
 C2h when the subcommand specified a captive self-test routine that has executed without failure.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.  
 DRDY shall be set to one indicating that the device is capable of receiving any command.  
 DF (Device Fault) shall be cleared to zero.  
 DRQ shall be cleared to zero.  
 ERR shall be cleared to zero.

**8.41.4.6 Error Outputs**

If the device does not support this command, if SMART is disabled, or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted. When a failure occurs while executing a test in captive mode, the device shall return command aborted with the Cylinder Low register value of F4h and the Cylinder High value of 2Ch.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na or 4Fh or F4h							
Cylinder High	na or C2h or 2Ch							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

IDNF shall be set to one if SMART data sector's ID field could not be found.  
 ABRT shall be set to one if this command is not supported, if SMART is not enabled, if register values are invalid, or if a self-test fails while executing a sequence in captive mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Cylinder Low register –

na when the subcommand specified an off-line routine (including an off-line self-test routine).  
 4Fh when the subcommand specified a captive self-test routine and some error other than a self-test routine failure occurred (i.e., if the sub-command is not supported or register values are invalid)  
 F4h when the subcommand specified a captive self-test routine which has failed during execution.

Cylinder High register –

na when the subcommand specified an off-line routine (including an off-line self-test routine).  
 2Ch when the subcommand specified a captive self-test routine which has failed during execution.  
 C2h when the subcommand specified a captive self-test routine and some error other than a self-test routine failure occurred (i.e., if the sub-command is not supported or register values are invalid)

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.  
 DRDY shall be set to one indicating that the device is capable of receiving any command.  
 DF (Device Fault) shall be set to one indicating that a device fault has occurred.  
 DRQ shall be cleared to zero indicating that there is no data to be transferred.  
 ERR shall be set to one if any Error register bit is set to one.

### 8.41.4.7 Prerequisites

DRDY set to one. SMART enabled.

### 8.41.4.8 Description

This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

**Table 31 – SMART EXECUTE OFF-LINE IMMEDIATE Sector Number register values**

Value	Description of subcommand to be executed
0	Execute SMART off-line routine immediately in off-line mode
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART Extended self-test routine immediately in off-line mode
3-63	Reserved
64-126	Vendor specific
127	Abort off-line mode self-test routine
128	Reserved
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART Extended self-test routine immediately in captive mode
131-191	Reserved
192-255	Vendor specific

#### 8.41.4.8.1 Off-line mode

The following describes the protocol for executing a SMART EXECUTE OFF-LINE IMMEDIATE subcommand routine (including a self-test routine) in the off-line mode.

- a) The device shall execute command completion before executing the subcommand routine.
- b) After clearing BSY to zero and setting DRDY to one after receiving the command, the device shall not set BSY nor clear DRDY during execution of the subcommand routine.
- c) If the device is in the process of performing the subcommand routine and is interrupted by any new command from the host except a SLEEP, SMART DISABLE OPERATIONS, SMART EXECUTE OFF-LINE IMMEDIATE, or STANDBY IMMEDIATE command, the device shall suspend or abort the subcommand routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command from the host the device may immediately re-initiate or resume the subcommand routine without any additional commands from the host (see 8.41.5.8.4).
- d) If the device is in the process of performing a subcommand routine and is interrupted by a SLEEP command from the host, the device may abort the subcommand routine and service the host after receipt of the command. If the device is in the process of performing any self-test routine and is interrupted by a SLEEP command from the host, the device shall abort the subcommand routine and service the host after receipt of the command.
- e) If the device is in the process of performing the subcommand routine and is interrupted by a SMART DISABLE OPERATIONS command from the host, the device shall suspend or abort the subcommand routine and service the host within two seconds after receipt of the command. Upon receipt of the next SMART ENABLE OPERATIONS command the device may, either re-initiate the subcommand routine or resume the subcommand routine from where it had been previously suspended.
- f) If the device is in the process of performing the subcommand routine and is interrupted by a SMART EXECUTE OFF-LINE IMMEDIATE command from the host, the device shall abort the subcommand routine and service the host within two seconds after receipt of the command. The device shall then service the new SMART EXECUTE OFF-LINE IMMEDIATE subcommand.
- g) If the device is in the process of performing the subcommand routine and is interrupted by a STANDBY IMMEDIATE command from the host, the device shall suspend or abort the subcommand routine, and service the host within two seconds after receipt of the command. After receiving a new command that causes the device to exit a power saving mode, the device shall initiate or resume the subcommand

routine without any additional commands from the host unless these activities were aborted by the host (see 8.41.5.8).

- h) While the device is performing the subcommand routine it shall not automatically change power states (e.g., as a result of its Standby timer expiring).

If an error occurs while a device is performing a self-test routine the device may discontinue the testing and place the test results in the Self-test execution status byte.

#### **8.41.4.8.2 Captive mode**

When executing a self-test in captive mode, the device sets BSY to one and executes the self-test routine after receipt of the command. At the end of the routine the device places the results of this routine in the Self-test execution status byte and executes command completion. If an error occurs while a device is performing the routine the device may discontinue its testing, place the results of this routine in the Self-test execution status byte, and complete the command.

#### **8.41.4.8.3 SMART off-line routine**

This routine shall only be performed in the off-line mode. The results of this routine are placed in the Off-line data collection status byte (see Table 33).

#### **8.41.4.8.4 SMART Short self-test routine**

Depending on the value in the Sector Number register, this self-test routine may be performed in either the captive or the off-line or mode. This self-test routine should take on the order of ones of minutes to complete (see 8.41.5.8).

#### **8.41.4.8.5 SMART Extended self-test routine**

Depending on the value in the Sector Number register, this self-test routine may be performed in either the captive or the off-line or mode. This self-test routine should take on the order of tens of minutes to complete (see 8.41.5.8).

### **8.41.5 SMART READ DATA**

#### **8.41.5.1 Command code**

B0h with the content of the Features register equal to D0h.

#### **8.41.5.2 Feature set**

SMART feature set.

- Optional when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

#### **8.41.5.3 Protocol**

PIO data-in (see 9.5).

#### **8.41.5.4 Inputs**

The Features register shall be set to D0h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na			
Command	B0h							

Device/Head register -  
DEV shall indicate the selected device.

#### 8.41.5.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one indicating that the device is capable of receiving any command.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

#### 8.41.5.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
UNC shall be set to one if SMART data is uncorrectable.  
IDNF shall be set to one if SMART data sector's ID field could not be found or data structure checksum occurred.  
ABRT shall be set to one if this command is not supported, if SMART is not enabled, or if register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.  
 DRDY shall be set to one indicating that the device is capable of receiving any command.  
 DF (Device Fault) shall be set to one indicating that a device fault has occurred.  
 DRQ shall be cleared to zero indicating that there is no data to be transferred.  
 ERR shall be set to one if any Error register bit is set to one.

#### 8.41.5.7 Prerequisites

DRDY set to one. SMART enabled.

#### 8.41.5.8 Description

This command returns the Device SMART data structure to the host.

Table 32 defines the 512 bytes that make up the Device SMART data structure. All multi-byte fields shown in this structure follow the byte ordering described in 3.2.9.

**Table 32 – Device SMART data structure**

Byte	F/V	Descriptions
0-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374-385	R	Reserved
386-510	X	Vendor specific
511	V	Data structure checksum
Key: F=the content of the byte is fixed and does not change. V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device. X=the content of the byte is vendor specific and may be fixed or variable. R=the content of the byte is reserved and shall be zero.		

##### 8.41.5.8.1 Off-line collection status byte

The value of the off-line data collection status byte defines the current status of the off-line activities of the device. Table 33 lists the values and their respective definitions.

**Table 33 – Off-line data collection status byte values**

Value	Definition
00h or 80h	Off-line data collection activity was never started.
01h	Reserved
02h or 82h	Off-line data collection activity was completed without error.
03h	Reserved
04h or 84h	Off-line data collection activity was suspended by an interrupting command from host.
05h or 85h	Off-line data collection activity was aborted by an interrupting command from host.
06h or 86h	Off-line data collection activity was aborted by the device with a fatal error.
07h-3Fh	Reserved
40h-7Fh	Vendor specific
81h	Reserved
83h	Reserved
87h-BFh	Reserved
C0h-FFh	Vendor specific

**8.41.5.8.2 Self-test execution status byte**

The self-test execution status byte reports the execution status of the self-test routine.

- Bits 0-3 (Percent Self-Test Remaining) The value in these bits indicates an approximation of the percent of the self-test routine remaining until completion in ten percent increments. Valid values are 0 through 9. A value of 0 indicates the self-test routine is complete. A value of 9 indicates 90% of total test time remaining.
- Bits 4-7 (Self-test Execution Status) The value in these bits indicates the current Self-test Execution Status (see Table 34).

**Table 34 – Self-test execution status values**

Value	Description
0	The previous self-test routine completed without error or no self-test has ever been run
1	The self-test routine was aborted by the host
2	The self-test routine was interrupted by the host with a hard or soft reset
3	A fatal error or unknown test error occurred while the device was executing its self-test routine and the device was unable to complete the self-test routine.
4	The previous self-test completed having a test element that failed and the test element that failed is not known.
5	The previous self-test completed having the electrical element of the test failed.
6	The previous self-test completed having the servo (and/or seek) test element of the test failed.
7	The previous self-test completed having the read element of the test failed.
8-14	Reserved.
15	Self-test routine in progress.

**8.41.5.8.3 Total time to complete off-line data collection**

The total time in seconds to complete off-line data collection activity word specifies how many seconds the device requires to complete the sequence of off-line data collection activity. Valid values for this word are from 0001h to FFFFh.

**8.41.5.8.4 Off-line data collection capabilities**

The following describes the definition for the off-line data collection capability bits. If the value of all of these bits is equal to zero, then no off-line data collection is implemented by this device.

- Bit 0 (EXECUTE OFF-LINE IMMEDIATE implemented bit) - If this bit is set to one, then the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented by this device. If this bit is cleared to zero, then the SMART EXECUTE OFF-LINE IMMEDIATE command is not implemented by this device.
- Bit 1 (vendor specific).
- Bit 2 (abort/restart off-line by host bit) - If this bit is set to one, then the device shall abort all off-line data collection activity initiated by an SMART EXECUTE OFF-LINE IMMEDIATE command upon receipt of a new command within 2 seconds of receiving the new command. If this bit is cleared to zero, the device shall suspend off-line data collection activity after an interrupting command and resume off-line data collection activity after some vendor-specified event.
- Bit 3 (off-line read scanning implemented bit) - If this bit is cleared to zero, the device does not support off-line read scanning. If this bit is set to one, the device supports off-line read scanning.
- Bit 4 (self-test implemented bit) – If this bit is cleared to zero, the device does not implement the Short and Extended self-test routines. If this bit is set to one, the device implements the Short and Extended self-test routines.
- Bits 5-7 (reserved).

#### **8.41.5.8.5 SMART capabilities**

The following describes the definition for the SMART capabilities bits. If all of these bits are cleared to zero, then automatic saving of SMART data is not implemented by this device.

- Bit 0 (power mode SMART data saving capability bit) - If this bit is set to one, the device saves SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If this bit is cleared to zero, the device does not save SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.
- Bit 1 (SMART data autosave after event capability bit) - This bit is set to one for devices complying with this standard.
- Bits 2-15 (reserved).

#### **8.41.5.8.6 Self-test routine recommended polling time**

The self-test routine recommended polling time shall be equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

#### **8.41.5.8.7 Data structure checksum**

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

### **8.41.6 SMART READ LOG SECTOR**

#### **8.41.6.1 Command code**

B0h with the content of the Features register equal to D5h.



### 8.41.6.2 Feature set

SMART feature set.

- Optional when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

### 8.41.6.3 Protocol

PIO data-in (see 9.5).

### 8.41.6.4 Inputs

The Features register shall be set to D5h. The Sector Count register shall indicate the number of sectors to be read from the log number indicated by the Sector Number register. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D5h							
Sector Count	Number of sectors to be read							
Sector Number	Log address							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na			
Command	B0h							

Sector count – Indicates the number of sectors that the host would like to read from the indicated log. The log transferred by the drive will always start at the first sector in the indicated log, regardless of the sector count requested.

Sector number - Indicates the log to be returned as described in Table 35. If this command is implemented, all address values for which the contents are defined shall be implemented and all address values defined as host vendor specific shall be implemented. The host vendor specific logs may be used by the host to store any data desired. If a host vendor specific log has never been written by the host, when read the content of the log shall be zeros. Device vendor specific logs may be used by the device vendor to store any data and need only be implemented if used.

**Table 35 – Log sector addresses**

Log sector address	Content	R/W
00h	Log directory	RO
01h	SMART error log	RO
02h-05h	Reserved	see note
06h	SMART self-test log	RO
07h-7Fh	Reserved	see note
80h-9Fh	Host vendor specific	R/W
A0h-BFh	Device vendor specific	VS
C0h-FFh	Reserved	see note
Key – RO - Log is read only by the host. R/W - Log is read or written by the host. VS - Log is vendor specific thus read/write ability is vendor specific.  NOTE – Log is reserved and read/write status will be assigned when the address is assigned.		

Device/Head register -  
DEV shall indicate the selected device.

### 8.41.6.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.41.6.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, Sector Number, **Sector Count**, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	Na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

UNC shall be set to one if SMART log sector is uncorrectable.

IDNF shall be set to one if SMART log sector's ID field was not found or data structure checksum error occurred.

ABRT shall be set to one if this command is not supported, if SMART is not enabled, if the log sector address is not implemented, or if other register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be set to one indicating that a device fault has occurred.

DRQ shall be cleared to zero indicating that there is no data to be transferred.

ERR shall be set to one if any Error register bit is set to one.

### 8.41.6.7 Prerequisites

DRDY set to one. SMART enabled.

### 8.41.6.8 Description

This command returns the indicated log to the host.

#### 8.41.6.8.1 SMART Log Directory

Table 36 defines the 512 bytes that make up the SMART Log Directory, which is optional. If implemented, it is SMART Log number zero, and is defined as one sector long.

**Table 36 – SMART Log Directory**

Byte	Descriptions
0-1	SMART Logging Version
2	Number of sectors in Log 1
3	Reserved
4	Number of sectors in Log 2
5	Reserved
...	...
510	Number of sectors in Log 255
511	Reserved

The value of the SMART Logging Version word shall be 01h if the drive supports multi-sector SMART logs. In addition, if the drive supports multi-sector logs, then log numbers 80-9Fh shall each be defined as 16 sectors long.

If the drive does not support multi-sector SMART logs, then log number zero is defined as reserved, and the drive shall return a command aborted response to the host's request to read log number zero.

If the host issues a SMART READ LOG or SMART WRITE LOG command with a Sector Count value of zero, the device shall return command aborted.

#### 8.41.6.8.2 Error log sector

Table 37 defines the 512 bytes that make up the SMART error log sector. All multi-byte fields shown in this structure follow the byte ordering described in 3.2.9. Error log data structures shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. They shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or invalid addresses.

**Table 37 – SMART error log sector**

Byte	Descriptions
0	SMART error log version
1	Error log index
2-91	First error log data structure
92-181	Second error log data structure
182-271	Third error log data structure
272-361	Fourth error log data structure
362-451	Fifth error log data structure
452-453	Device error count
454-510	Reserved
511	Data structure checksum

#### 8.41.6.8.2.1 Error log version

The value of the SMART error log version byte shall be 01h.

### 8.41.6.8.2.2 Error log index

The error log index indicates the error log data structure representing the most recent error. Only values 1 through 5 are valid.

### 8.41.6.8.2.3 Error log data structure

An error log data structure shall be presented for each of the last five errors reported by the device. These error log data structure entries are viewed as a circular buffer. That is, the first error shall create the first error log data structure; the second error, the second error log structure; etc. The sixth error shall create an error log data structure that replaces the first error log data structure; the seventh error replaces the second error log structure, etc. The error log pointer indicates the most recent error log structure. If fewer than five errors have occurred, the unused error log structure entries shall be zero filled. Table 38 describes the content of a valid error log data structure.

**Table 38 – Error log data structure**

Byte	Descriptions
n thru n+11	First command data structure
n+12 thru n+23	Second command data structure
n+24 thru n+35	Third command data structure
n+36 thru n+47	Fourth command data structure
n+48 thru n+59	Fifth command data structure
n+60 thru n+89	Error data structure

#### 8.41.6.8.2.3.1 Command data structure

The fifth command data structure shall contain the command or reset for which the error is being reported. The fourth command data structure should contain the command or reset that preceded the command or reset for which the error is being reported, the third command data structure should contain the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures shall be zero filled, for example, if only three commands and resets preceded the command or reset for which the error is being reported, the first command data structure shall be zero filled. In some devices, the hardware implementation may preclude the device from reporting the commands that preceded the command for which the error is being reported or that preceded a reset. In this case, the command data structures are zero filled.

If the command data structure represents a command or software reset, the content of the command data structure shall be as shown in Table 39. If the command data structure represents a hardware reset, the content of byte n shall be FFh, the content of bytes n+1 through n+7 are vendor specific, and the content of bytes n+8 through n+11 shall contain the timestamp.

**Table 39 – Command data structure**

Byte	Descriptions
n	Content of the Device Control register when the Command register was written.
n+1	Content of the Features register when the Command register was written.
n+2	Content of the Sector Count register when the Command register was written.
n+3	Content of the Sector Number register when the Command register was written.
n+4	Content of the Cylinder Low register when the Command register was written.
n+5	Content of the Cylinder High register when the Command register was written.
n+6	Content of the Device/Head register when the Command register was written.
n+7	Content written to the Command register.
n+8	Timestamp (least significant byte)
n+9	Timestamp (next least significant byte)
n+10	Timestamp (next most significant byte)
n+11	Timestamp (most significant byte)

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

#### 8.41.6.8.2.3.2 Error data structure

The error data structure shall contain the error description of the command for which an error was reported as described in Table 40. If the error was **logged** for a hardware reset, the content of bytes n+1 through n+7 shall be vendor specific and the remaining bytes shall be as defined in Table 40.

**Table 40 – Error data structure**

Byte	Descriptions
n	Reserved
n+1	Content of the Error register after command completion occurred.
n+2	Content of the Sector Count register after command completion occurred.
n+3	Content of the Sector Number register after command completion occurred.
n+4	Content of the Cylinder Low register after command completion occurred.
n+5	Content of the Cylinder High register after command completion occurred.
n+6	Content of the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 thru n+26	Extended error information
n+27	State
n+28	Life timestamp (least significant byte)
n+29	Life timestamp (most significant byte)

Extended error information shall be vendor specific.

State shall contain a value indicating the state of the device when command was written to the Command register or the reset occurred as described in Table 41.

**Table 41 – State field values**

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique
The value of x is vendor specific and may be different for each state.	

Sleep indicates the reset for which the error is being reported was received when the device was in the Sleep mode.

Standby indicates the command or reset for which the error is being reported was received when the device was in the Standby mode.

Active/Idle with BSY cleared to zero indicates the command or reset for which the error is being reported was received when the device was in the Active or Idle mode and BSY was cleared to zero.

Executing SMART off-line or self-test indicates the command or reset for which the error is being reported was received when the device was in the process of executing a SMART off-line or self-test.

Life timestamp shall contain the power-on lifetime of the device in hours when command completion occurred.

#### 8.41.6.8.2.4 Device error count

The device error count field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. These errors shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached, the count shall remain at the maximum value when additional errors are encountered and logged.

#### 8.41.6.8.2.5 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

#### 8.41.6.8.3 Self-test log sector

Table 42 defines the 512 bytes that make up the SMART self-test log sector. All multi-byte fields shown in this structure follow the byte ordering described in 3.2.9.

**Table 42 – Self-test log data structure**

<b>Byte</b>	<b>Descriptions</b>
0-1	Self-test log data structure revision number

### 8.41.6.8.3.3 Self-test index

The self-test index shall point to the most recent entry. Initially, when the log is empty, the index shall be set to zero. It shall be set to one when the first entry is made, two for the second entry, etc., until the 22nd entry, when the index shall be reset to one.

### 8.41.6.8.3.4 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

## 8.41.7 SMART RETURN STATUS

### 8.41.7.1 Command code

B0h with a Feature register value of DAh.

### 8.41.7.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

### 8.41.7.3 Protocol

Non-data command (see 9.4).

### 8.41.7.4 Inputs

The Features register shall be set to DAh. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	DAh							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device/Head register -

DEV shall indicate the selected device.

### 8.41.7.5 Normal outputs

If the device has not detected a threshold exceeded condition, the device sets the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If the device has detected a threshold exceeded condition, the device sets the Cylinder Low register to F4h and the Cylinder High register to 2Ch.



Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh or F4h							
Cylinder High	C2h or 2Ch							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Cylinder Low -

4Fh if threshold not exceeded, F4h if threshold exceeded.

Cylinder High -

C2h if threshold not exceeded, 2Ch if threshold exceeded.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

#### 8.41.7.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported, if SMART is disabled, or if the input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

#### 8.41.7.7 Prerequisites

DRDY set equal to one. SMART enabled.

#### 8.41.7.8 Description

This command is used to communicate the reliability status of the device to the host at the host's request. If a threshold exceeded condition is not detected by the device, the device shall set the Cylinder Low register

to 4Fh and the Cylinder High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the Cylinder Low register to F4h and the Cylinder High register to 2Ch.

## 8.41.8 SMART SAVE ATTRIBUTE VALUES

### 8.41.8.1 Command code

B0h with a Feature register value of D3h.

### 8.41.8.2 Feature set

SMART feature set.

- Optional and not recommended when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

### 8.41.8.3 Protocol

Non-data command (see 9.4).

### 8.41.8.4 Inputs

The Features register shall be set to D3h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D3h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device/Head register -

DEV shall indicate the selected device.

### 8.41.8.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.41.8.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported, if SMART is disabled, or if the input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero..

ERR shall be set to one if an Error register bit is set to one.

### 8.41.8.7 Prerequisites

DRDY set equal to one. SMART enabled.

### 8.41.8.8 Description

This command causes the device to immediately save any updated attribute values to the device's non-volatile memory regardless of the state of the attribute autosave timer.

## 8.41.9 SMART WRITE LOG SECTOR

### 8.41.9.1 Command code

B0h with the content of the Features register equal to D6h.

### 8.41.9.2 Feature set

SMART feature set.

- Optional when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

### 8.41.9.3 Protocol

PIO data-out (see 9.6).

#### 8.41.9.4 Inputs

The Features register shall be set to D6h. The Sector Count register shall indicate the number of sectors that shall be written to the log number indicated by the Sector Number register. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D6h							
Sector Count	Number of sectors to be written							
Sector Number	Log sector address							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	obs	na	obs	DEV	na			
Command	B0h							

Sector count – Indicates the number of sectors that the host would like to write to in the indicated log. If the number is greater than the number indicated in the “Log directory” (which is available in Log number zero), the drive shall return command aborted. The log transferred to the drive will always be stored by the drive starting at the first sector in the indicated log.

Sector number - Indicates the log to be written as described in Table 35. If this command is implemented, all address values defined as host vendor specific shall be implemented. These host vendor specific logs may be used by the host to store any data desired. Support for device vendor specific logs is optional. If the host attempts to write to a read only (RO) log address, the device shall return command aborted.

Device/Head register -

DEV shall indicate the selected device.

#### 8.41.9.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

#### 8.41.9.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, Sector Number, Sector Count, Cylinder Low, or Cylinder High registers are invalid, the device shall return command aborted. If the host attempts to write to a read only (RO) log address, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	obs
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	Na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

IDNF shall be set to one if SMART log sector's ID field could not be found.

ABRT shall be set to one if this command is not supported, if SMART is not enabled, if the log sector address is not implemented, or if other register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be set to one indicating that a device fault has occurred.

DRQ shall be cleared to zero indicating that there is no data to be transferred.

ERR shall be set to one if any Error register bit is set to one.

#### 8.41.9.7 Prerequisites

DRDY set to one. SMART enabled.

#### 8.41.9.8 Description

This command writes an **indicated number of 512 byte data sectors** to the indicated log.

### 8.42 STANDBY

#### 8.42.1 Command code

E2h

#### 8.42.2 Feature set

Power Management feature set.

- Power Management feature set is mandatory when power management is not implemented by a PACKET power management feature set.
- This command is mandatory when the Power Management feature set is implemented **when the PACKET Command feature set is not implemented**.

#### 8.42.3 Protocol

Non-data command (see 9.4).

#### 8.42.4 Inputs

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer. Table 22 defines these values.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Time period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E2h							

Device/Head register -  
DEV shall indicate the selected device.

#### 8.42.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be cleared to zero.  
DRQ shall be cleared to zero.  
ERR shall be cleared to zero.

#### 8.42.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -  
ABRT shall be set to one if the Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -  
DEV shall indicate the selected device.

Status register -  
BSY shall be cleared to zero indicating command completion.  
DRDY shall be set to one.  
DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.  
 ERR shall be set to one if an Error register bit is set to one.

**8.42.7 Prerequisites**

DRDY set equal to one.

**8.42.8 Description**

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer (see Table 22).

If the Sector Count register is zero then the Standby timer is disabled.

**8.43 STANDBY IMMEDIATE**

**8.43.1 Command code**

E0h

**8.43.2 Feature set**

Power Management feature set.

- Power Management feature set is mandatory when power management is not implemented by a PACKET power management feature set.
- This command is mandatory when the Power Management feature set is implemented.

**8.43.3 Protocol**

Non-data command (see 9.4).

**8.43.4 Inputs**

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E0h							

Device/Head register -  
 DEV shall indicate the selected device.

### 8.43.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.43.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the Power Management feature set is not supported. ABRT may be set to

one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.43.7 Prerequisites

DRDY set equal to one.

### 8.43.8 Description

This command causes the device to immediately enter the Standby mode.



## 8.44 WRITE BUFFER

### 8.44.1 Command code

E8h

### 8.44.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.44.3 Protocol

PIO data-out (see 9.6).

### 8.44.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Command	E8h							

Device/Head register -

DEV shall indicate the selected device.

### 8.44.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

### 8.44.6 Error outputs

The device shall return command aborted if the command is not supported.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

#### 8.44.7 Prerequisites

DRDY set equal to one.

#### 8.44.8 Description

This command enables the host to write the contents of one sector in the device's buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

### 8.45 WRITE DMA

#### 8.45.1 Command code

CAh

#### 8.45.2 Feature set

General feature set

Mandatory for devices not implementing the PACKET Command feature set.

Use prohibited for devices implementing the PACKET Command feature set.

#### 8.45.3 Protocol

DMA (see 9.7).

#### 8.45.4 Inputs

The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	CAh							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

#### 8.45.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

#### 8.45.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with address of first unrecoverable error.

DEV shall indicate the selected device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.45.7 Prerequisites

DRDY set equal to one. The host shall initialize the DMA channel.

### 8.45.8 Description

The WRITE DMA command allows the host to write data using the DMA data transfer protocol.

## 8.46 WRITE DMA QUEUED

### 8.46.1 Command code

CCh

### 8.46.2 Feature set

Overlapped feature set

- Mandatory for devices implementing the Overlapped feature set but not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.46.3 Protocol

DMA QUEUED (see 9.9).

### 8.46.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	CCh							

Features -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector count -

if the device supports command queuing, bits (7:3) contain the Tag for the command being delivered. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this field is not applicable.

Sector number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

### 8.46.5 Normal outputs

#### 8.46.5.1 Data transmission

Data transfer may occur after receipt of the command or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	SERV	DRQ	na	na	CHK

Interrupt reason register -

Tag - This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be set to one if a released command is outstanding.

I/O - Shall be cleared to zero indicating the transfer is from the host.

C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register -

DEV - Shall indicate the selected device.

Status register -

BSY - Shall be cleared to zero.

DRDY - Shall be set to one.

DF (Device Fault) - Shall be cleared to zero.

SERV (Service) - Shall be set to one if another command is ready to be serviced.

DRQ - Shall be set to one.

CHK - Shall be cleared to zero.

**8.46.5.2 Bus release**

If the device performs a bus release before transferring data for this command, the register content upon performing a bus release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Sector Count register -

Tag - If the device supports command queuing, this field shall contain the Tag of the command being bus released. If the device does not support command queuing, this field shall be zeros.

REL bit shall be set indicating that the device has bus released an overlap command.

I/O shall be cleared to zero.

C/D shall be cleared to zero.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating bus release.

DRDY shall be set to one.

SERV (Service) shall be cleared to zero if no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service. This bit shall be set to one when the device has prepared this command for service.

DF (Device Fault) shall be cleared to zero.

DRQ bit shall be cleared to zero.

ERR bit shall be cleared to zero.

**8.46.5.3 Service request**

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see 6.9). When the SERVICE command is received, the device shall set outputs as described in data transfer, command completion, or error outputs depending on the service the device requires.

**8.46.5.4 Command completion**

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Sector Count register -

Tag - If the device supports command queuing, this field shall contain the Tag of the completed command. If the device does not support command queuing, this field shall be zeros.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SERV (Service) shall be cleared to zero when no other queued command is ready for service.

SERV shall be set to one when another queued command is ready for service.

DF (Device Fault) shall be cleared to zero.

DRQ bit shall be cleared to zero.

ERR bit shall be cleared to zero.

#### 8.46.6 Error outputs

The Sector Count register contains the Tag for this command if the device supports command queuing. The device shall return command aborted if the command is not supported or if the device has not had overlapped interrupt enabled. The device shall return command aborted if the device supports command queuing and the Tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	na
Sector Count	Tag					REL	I/O	C/D
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count register -

Tag - If the device supports command queuing, this field shall contain the Tag of the completed command. If the device does not support command queuing, this field shall be zeros.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

Sector Number, Cylinder Low, Cylinder High, Device/Head -

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SERV (Service) shall be cleared to zero when no other queued command is ready for service.

SERV shall be set to one when another queued command is ready for service.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

#### **8.46.7 Prerequisites**

DRDY set to one. The host shall initialize the DMA channel.

#### **8.46.8 Description**

This command executes in a similar manner to a WRITE DMA command. The device may perform a bus release the bus or may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

Once the data transfer is begun, the device shall not perform a bus release until the entire data transfer has been completed.

### **8.47 WRITE MULTIPLE**

#### **8.47.1 Command code**

C5h

#### **8.47.2 Feature set**

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

#### **8.47.3 Protocol**

PIO data-out (see 9.6).



#### 8.47.4 Inputs

The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	C5h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Number -

starting sector number or LBA address bits (7:0).

Cylinder Low -

starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High -

starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head -

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

#### 8.47.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

#### 8.47.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	WP	MC	IDNF	MCR	ABRT	NM	na
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

#### Error register -

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

#### Sector Number, Cylinder Low, Cylinder High, Device/Head -

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

#### Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

### 8.47.7 Prerequisites

DRDY set equal to one. If bit 8 of IDENTIFY DEVICE word 59 is equal to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

### 8.47.8 Description

The WRITE MULTIPLE command performs the same as the WRITE SECTOR(S) command except that the device does not a) set DF, as required, b) set ERR and the bits in the Error register, as required, c) clear DRQ and BSY, and d) assert INTRQ until data is transferred for all sectors in the block. Data for all of the other sectors in the block are transferred without the device asserting INTRQ. In addition, the DRQ qualification of the transfer is required only before the first sector of a block, not before each sector of the block.

The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits 0-7 in word 47 in the IDENTIFY DEVICE information.

If bit 8 equals 1 and bits 0-7 are equal to zero in word 59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts shall be programmed by the SET MULTIPLE MODE command before issuing the first READ MULTIPLE or WRITE MULTIPLE command after a power on or hardware reset. If bit 8 in word 1 equals one and bits 0-7 are not equal to zero in word

59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts may be reprogrammed by the SET MULTIPLE MODE command before issuing the next READ MULTIPLE or WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for  $n$  sectors, where:

$$n = \text{Remainder (sector count/ block count)}.$$

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The Write command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupts are generated when the DRQ bit is set to one at the beginning of each block or partial block.

## 8.48 WRITE SECTOR(S)

### 8.48.1 Command code

30h

### 8.48.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

### 8.48.3 Protocol

PIO data-out (see 9.6).

### 8.48.4 Inputs

The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Head number or LBA			
Command	30h							

Sector Count -

number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

**Sector Number -**

starting sector number or LBA address bits (7:0).

**Cylinder Low -**

starting cylinder number bits (7:0) or LBA address bits (15:8).

**Cylinder High -**

starting cylinder number bits (15:8) or LBA address bits (23:16).

**Device/Head -**

bit 6 set to one if LBA address, cleared to zero if CHS address.

DEV shall indicate the selected device.

bits (3:0) starting head number or LBA address bits (27:24).

**8.48.5 Normal outputs**

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

**Device/Head register -**

DEV shall indicate the selected device.

**Status register -**

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

**8.48.6 Error outputs**

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	WP	MC	IDNF	MCR	ABRT	NM	na
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	obs	na	obs	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

**Error register -**

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

#### **8.48.7 Prerequisites**

DRDY set equal to one.

#### **8.48.8 Description**

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.

## **9 Protocol**

Commands are grouped into different classes according to the protocol followed for command execution. The command classes with their associated protocol are defined in state diagrams in this clause, one state diagram for host actions and a second state diagram for device actions. Figure 11 shows the overall relationship of the host protocol state diagrams. Figure 12 shows the overall relationship of the device protocol state diagrams. State diagrams defining these protocols are not normative descriptions of implementations, they are normative descriptions of externally apparent device or host behavior. Different implementations are allowed. See 3.2.7 for state diagram conventions.

A device shall not timeout any activity when waiting for a response from the host.

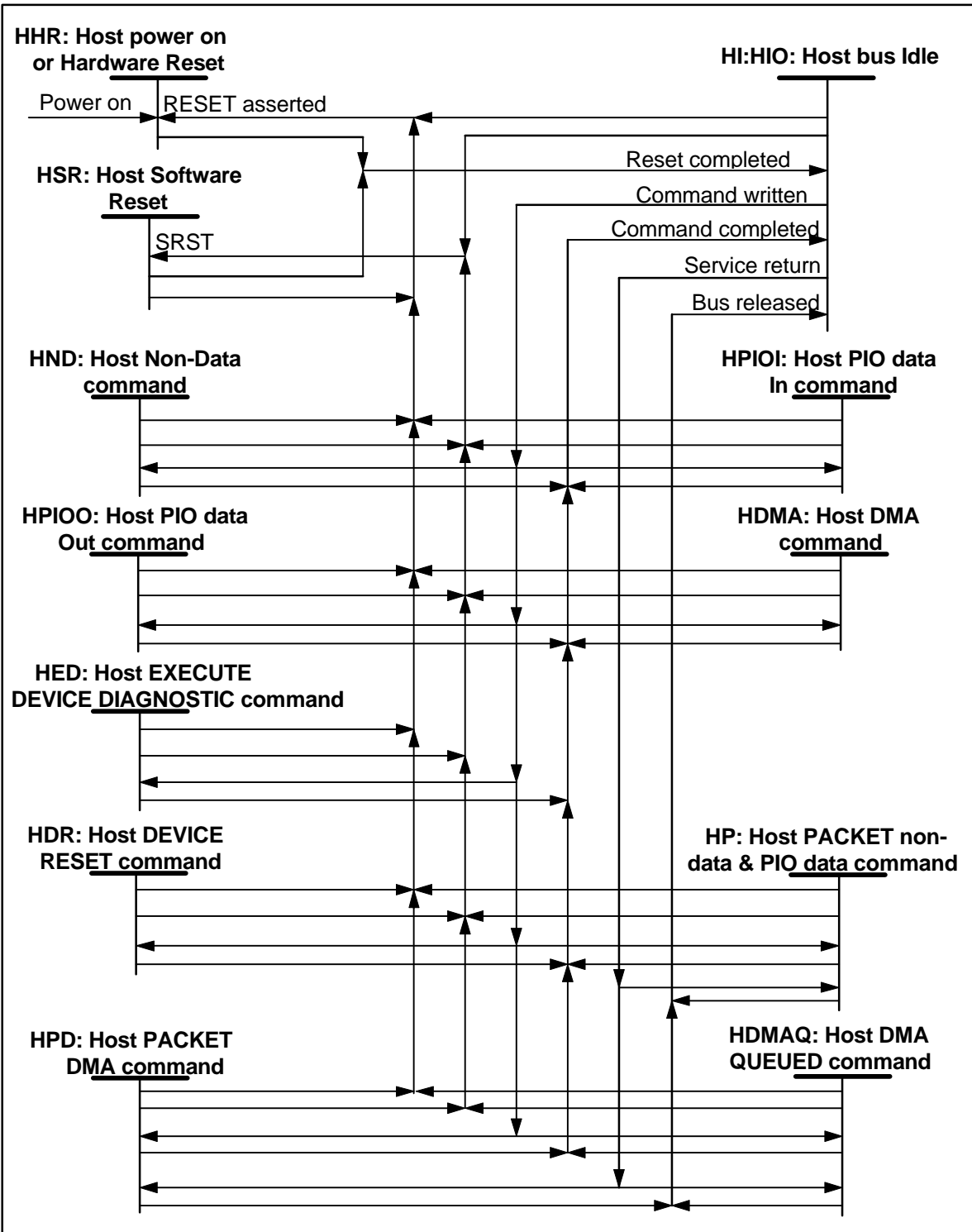


Figure 11 – Overall host protocol state sequence

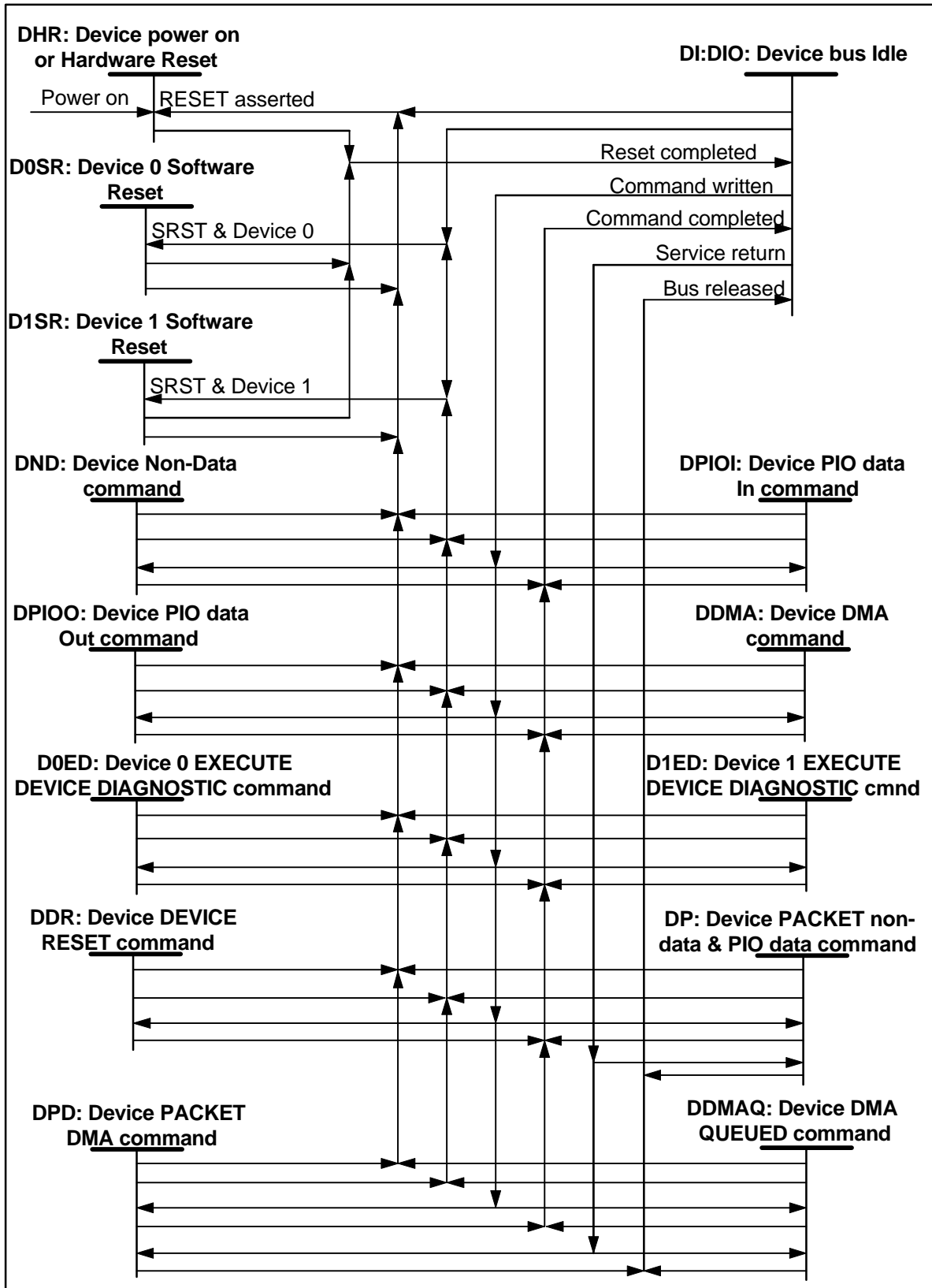


Figure 12 – Overall device protocol state sequence

## 9.1 Power on and hardware reset protocol

This clause describes the protocol for processing of power on and hardware resets.

If the host asserts RESET- **regardless of the power management mode**, the device shall execute the hardware reset protocol. If the host reasserts RESET- before a device has completed the power on or hardware reset protocol, then the device shall restart the protocol from the beginning.

The host should not set the SRST bit to one in the Device Control register or issue a DEVICE RESET command while the BSY bit is set to one in either device Status register as a result of executing the power on or hardware reset protocol. If the host sets the SRST bit in the Device Control register to one or issues a DEVICE RESET command before devices have completed execution of the power on or hardware reset protocol, then the devices shall ignore the software reset or DEVICE RESET command.

A host should issue an IDENTIFY DEVICE and/or IDENTIFY PACKET DEVICE command after the power on or hardware reset protocol has completed to determine the current status of features implemented by the device(s).

Figure 13 and the text following the figure describes the power on or hardware reset protocol for the host. Figure 14 and the text following the figure describes the power on or hardware reset protocol for the devices.

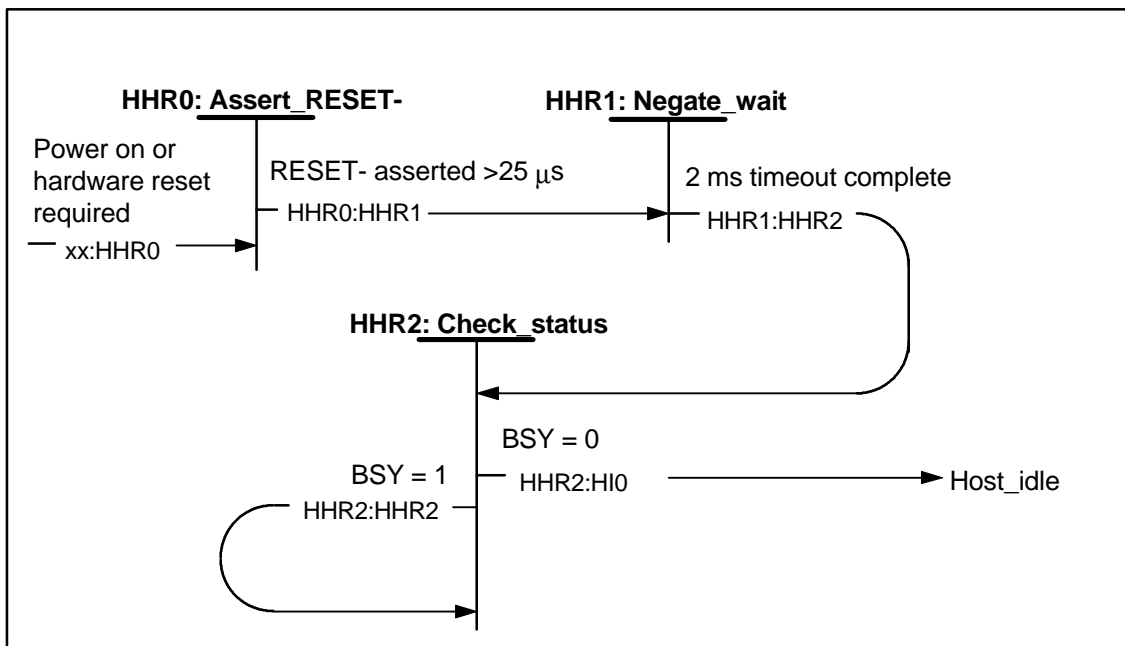


Figure 13 – Host power on or hardware reset protocol

**HHR0: Assert\_RESET- State:** This state is entered at power on or when the host recognizes that a hardware reset is required.

When in this state, the host asserts RESET-. The host shall remain in this state with RESET- asserted for at least 25 μs.

**Transition HHR0:HHR1:** When the host has had RESET- asserted for at least 25 μs, the host shall transition to the HHR1: Negate\_wait state.

**HHR1: Negate\_wait State:** This state is entered when RESET- has been asserted for at least 25 μs.

When in this state, the host shall negate RESET-. The host shall remain in this state for at least 2 ms after negating RESET-. **If the host tests CBLID- it shall do so at this time.**



**Transition HHR1:HHR2:** When RESET- has been negated for at least 2 ms, the host shall transition to the HHR2: Check\_status state.

**HHR2: Check\_status State:** This state is entered when RESET- has been negated for at least 2 ms.

When in this state the host shall read the Status or Alternate Status register.

**Transition HHR2:HHR2:** When BSY is set to one, the host shall transition to the HHR2: Check\_status state.

**Transition HHR2:HI0:** When BSY is cleared to zero, the host shall transition to the HI0: Host\_idle state (see Figure 18). If status indicates that an error has occurred, the host shall take appropriate error recovery action.

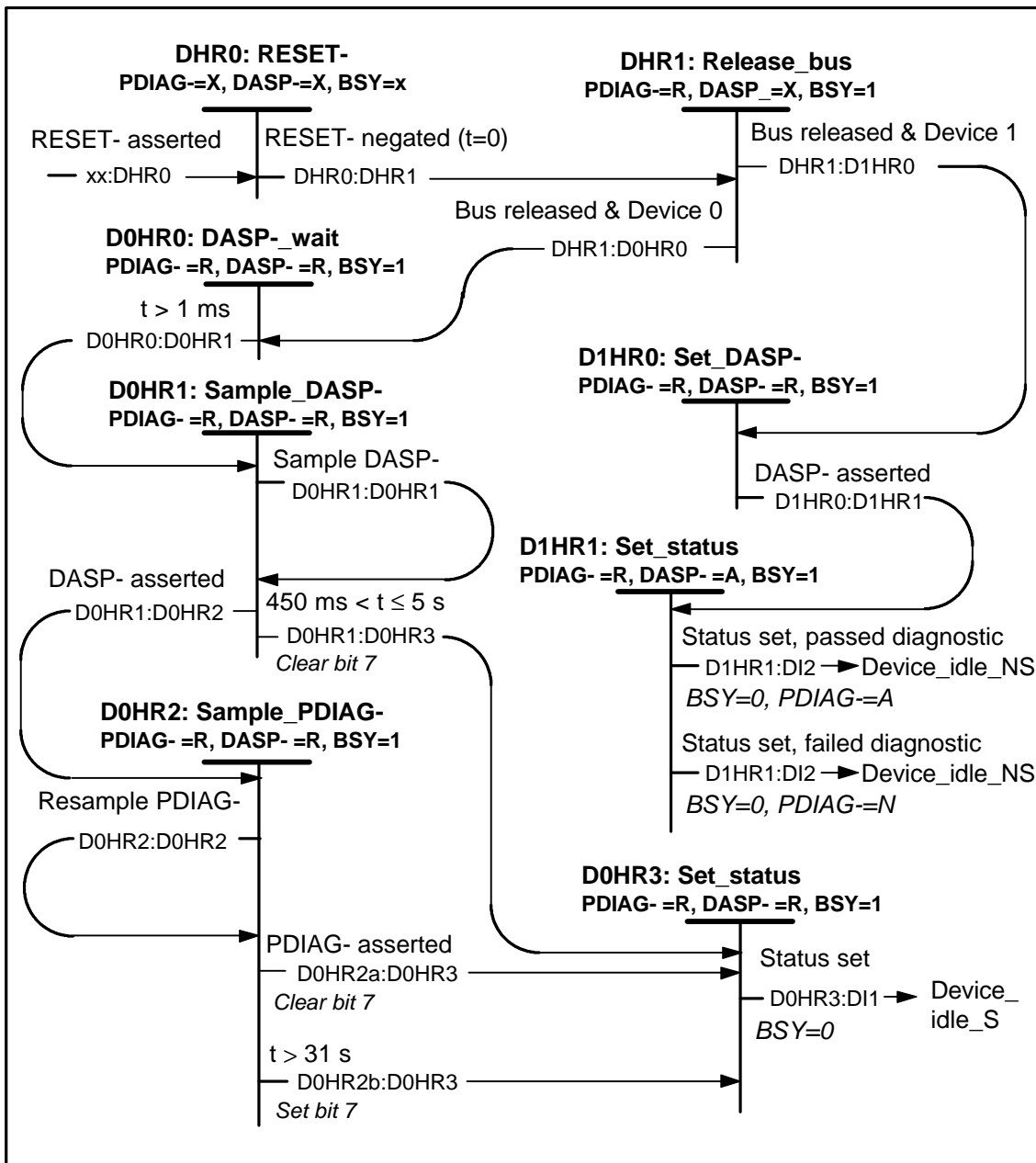


Figure 14 – Device power on or hardware reset protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	0	0	0	0	0	R	R	v	v

**DHR0: RESET State:** This state is entered when a valid assertion of the RESET- signal is recognized. The device shall not recognize a RESET- assertion shorter than 20 ns as valid. Devices may recognize a RESET- assertion greater than 20 ns as valid and shall recognize a RESET- assertion equal to or greater than 25  $\mu$ s as valid.

**Transition DHR0:DHR1:** When a valid RESET- signal is negated, the device shall transition to the DHR1: Release\_Bus state.

**DHR1: Release\_bus State:** This state is entered when a valid RESET- signal is negated.

When in this state, the device shall release bus signals PDIAG-, INTRQ, IORDY, DMARQ, and DD(15:0) and shall set BSY to one within 400 ns after entering this state. The device shall determine if the device is Device 0 or Device 1 by checking the jumper, switch, or CSEL.

**Transition DHR1:D0HR0:** When the device has determined that the device is Device 0, has released the bus signals, and has set BSY to one, then the device shall transition to the D0HR0: DASP-\_wait state.

**Transition DHR1:D1HR0:** When the device has determined that the device is Device 1, has released the bus signals, and has set BSY to one, then the device shall transition to the D1HR0: Set\_DASP- state.

**D0HR0: DASP-\_wait State:** This state is entered when the device has released the bus signals, set BSY to one, and determined that the device is Device 0.

When in this state, the device shall release DASP- within 1 ms of the negation of RESET-.

**Transition D0HR0:D0HR1:** When at least 1 ms has elapsed since the negation of RESET-, the device shall transition to the D0HR1: Sample\_DASP- state.

**D0HR1: Sample\_DASP- State:** This state is entered when at least 1 ms has elapsed since the negation of RESET-.

When in this state, the device should begin performing the hardware initialization and self-diagnostic testing. This may revert the device to the default condition (the device's settings may now be different than they were before the host asserted RESET-). All Ultra DMA modes shall be disabled.

When in this state, the device shall sample the DASP- signal.

**Transition D0HR1:D0HR2:** When the sample indicates that DASP- is asserted, the device shall transition to the D0HR2: Sample\_PDIAG- state.

**Transition D0HR1:D0HR1:** When the sample indicates that DASP- is negated and less than 450 ms have elapsed since the negation of RESET-, then the device shall transition to the D0HR1: Sample\_DASP- state. When the sample indicates that DASP- is negated and greater than 450 ms but less than 5 s have elapsed since the negation of RESET-, then the device may transition to the D0HR1: Sample\_DASP- state.

**Transition D0HR1:D0HR3:** When the sample indicates that DASP- is negated and 5 s have elapsed since the negation of RESET-, then the device shall clear bit 7 in the Error register and transition to the D0HR3: Set\_status state. When the sample indicates that DASP- is negated and greater than 450 ms but less than 5 s have elapsed since the negation of RESET-, then the device may clear bit 7 in the Error register and transition to the D0HR3: Set\_status state.

**D0HR2: Sample\_PDIAG- State:** This state is entered when the device has recognized that DASP- is asserted.

When in this state, the device shall sample the PDIAG- signal.

**Transition D0HR2a:D0HR3:** When the sample indicates that PDIAG- is asserted, the device shall clear bit 7 in the Error register and transition to the D0HR3: Set\_status state.

**Transition D0HR2b:D0HR3:** When the sample indicates that PDIAG- is not asserted and 31 s have elapsed since the negation of RESET-, then the device shall set bit 7 in the Error register and transition to the D0HR3: Set\_status state.

**Transition D0HR2:D0HR2:** When the sample indicates that PDIAG- is not asserted and less than 31 s have elapsed since the negation of RESET-, then the device shall transition to the D0HR2: Sample\_PDIAG-state.

**D0HR3: Set\_status State:** This state is entered when Bit 7 in the Error register has been set or cleared.

When in this state the device shall complete the hardware initialization and self-diagnostic testing begun in the Sample DASP- state if not already completed.

The diagnostic code shall be placed in bits 6-0 of the Error register (see Table 18). The device shall set the signature values (see 9.12). The device shall clear the SRST bit to zero in the Device Control register if set to one. The content of the Features register is undefined. The device shall set word 93 in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response (see 8.12.51).

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2, and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

**Transition D0HR3:DI1:** When hardware initialization and self-diagnostic testing is completed and the status has been set, the device shall clear BSY to zero and transition to the DI1: Device\_idle\_S state (see Figure 20).

**D1HR0: Set\_DASP- State:** This state is entered when the device has released the bus, set BSY to one, and determined that the device is Device 1.

When in this state, the device shall release PDIAG- within 1 ms and assert DASP- within 400 ms of the negation of RESET-.

When in this state, the device should begin execution of the hardware initialization and self-diagnostic testing. The device may revert to the default condition (the device's settings may now be in different conditions than they were before RESET- was asserted by the host). All Ultra DMA modes shall be disabled.

**Transition D1HR0:D1HR1:** When DASP- has been asserted, the device shall transition to the D1HR1: Set\_status state.

**D1HR1: Set\_status State:** This state is entered when the device has asserted DASP-.

When in this state the device shall complete any hardware initialization and self-diagnostic testing begun in the Set DASP- state if not already completed. The diagnostic code shall be placed in the Error register (see Table 18). If the device passed self-diagnostics, the device shall assert PDIAG-. The device shall set word 93 in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response (see 8.12.51).

All actions required in this state shall be completed in  $\leq 30$  s.

The device shall set the signature values (see 9.12). The content of the Features register is undefined. The device shall clear the SRST bit to zero in the Device Control register if set set to one.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2, and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

**Transition D1HR1a:DI2:** When hardware initialization and self-diagnostic testing is completed, the device passed its diagnostics, and the status has been set, the device shall clear BSY to zero, assert PDIAG-, and transition to the DI2: Device\_idle\_NS state (see Figure 20).

**Transition D1HR1b:DI2:** When hardware initialization and self-diagnostic testing is completed, the device failed its diagnostic, and the status has been set, the device shall clear BSY to zero, negate PGIAG-, and transition to the DI2: Device\_idle\_NS state (see Figure 20).

## 9.2 Software reset protocol

This clause describes the protocol for processing of software reset when the host sets SRST.

If the host sets SRST in the Device Control register to one regardless of the power management mode, the device shall execute the software reset protocol. If the host asserts RESET- before a device has completed the software reset protocol, then the device shall execute the hardware reset protocol from the beginning.

The host should not set the SRST bit to one in the Device Control while the BSY bit is set to one in either device Status register as a result of executing the software reset protocol. If the host sets the SRST bit in the Device Control register to one or issues a DEVICE RESET command before devices have completed execution of the software reset protocol, then the devices shall restart execution of the software reset protocol from the beginning.

A host should issue an IDENTIFY DEVICE and/or IDENTIFY PACKET DEVICE command after the software reset protocol has completed to determine the current status of features implemented by the device(s).

Figure 15 and the text following the figure describe the software reset protocol for the host. Figure 16 and the text following the figure describes the software reset protocol for Device 0. Figure 17 and the text following the figure describes the software reset protocol for Device 1.

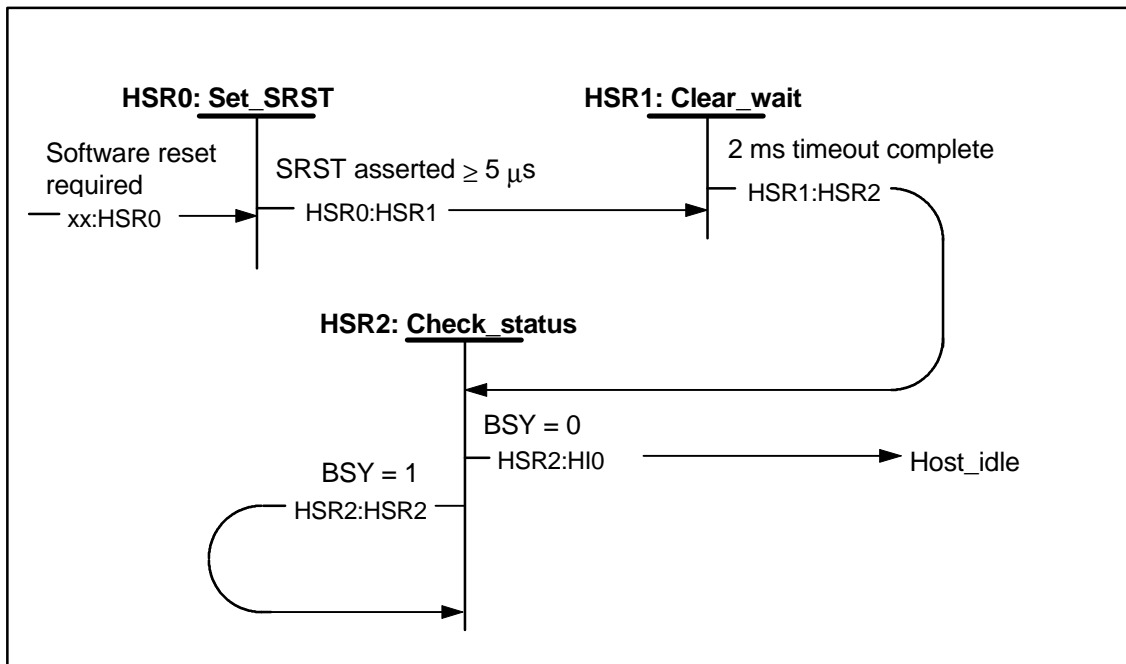


Figure 15 – Host software reset protocol

**HSR0: Set\_SRST State:** This state is entered when the host initiates a software reset.

When in this state, the host shall set SRST in the Device Control register to one. The SRST bit shall be written to both devices when the Device Control register is written. The host shall remain in this state with SRST set to one for at least 5  $\mu$ s. The host shall not set SRST to one unless the bit has been cleared to zero for at least 5  $\mu$ s.

**Transition HSR0:HSR1:** When the host has had SRST set to one for at least 5  $\mu$ s, the host shall transition to the HSR1: Clear\_wait state.

**HSR1: Clear\_wait State:** This state is entered when SRST has been set to one for at least 5  $\mu$ s.

When in this state, the host shall clear SRST in the Device Control register to zero. The host shall remain in this state for at least 2 ms.

**Transition HSR1:HSR2:** When SRST has been cleared to zero for at least 2 ms, the host shall transition to the HSR2: Check\_status state.

**HSR2: Check\_status State:** This state is entered when SRST has been cleared to zero for at least 2 ms.

When in this state the host shall read the Status or Alternate Status register.

**Transition HSR2:HSR2:** When BSY is set to one, the host shall transition to the HSR2: Check\_status state.

**Transition HSR2:HI0:** When BSY is cleared to zero, the host shall check the ending status in the Error register and the signature (see 9.16 9.12) and transition to the HI0: Host\_idle state (see Figure 18).

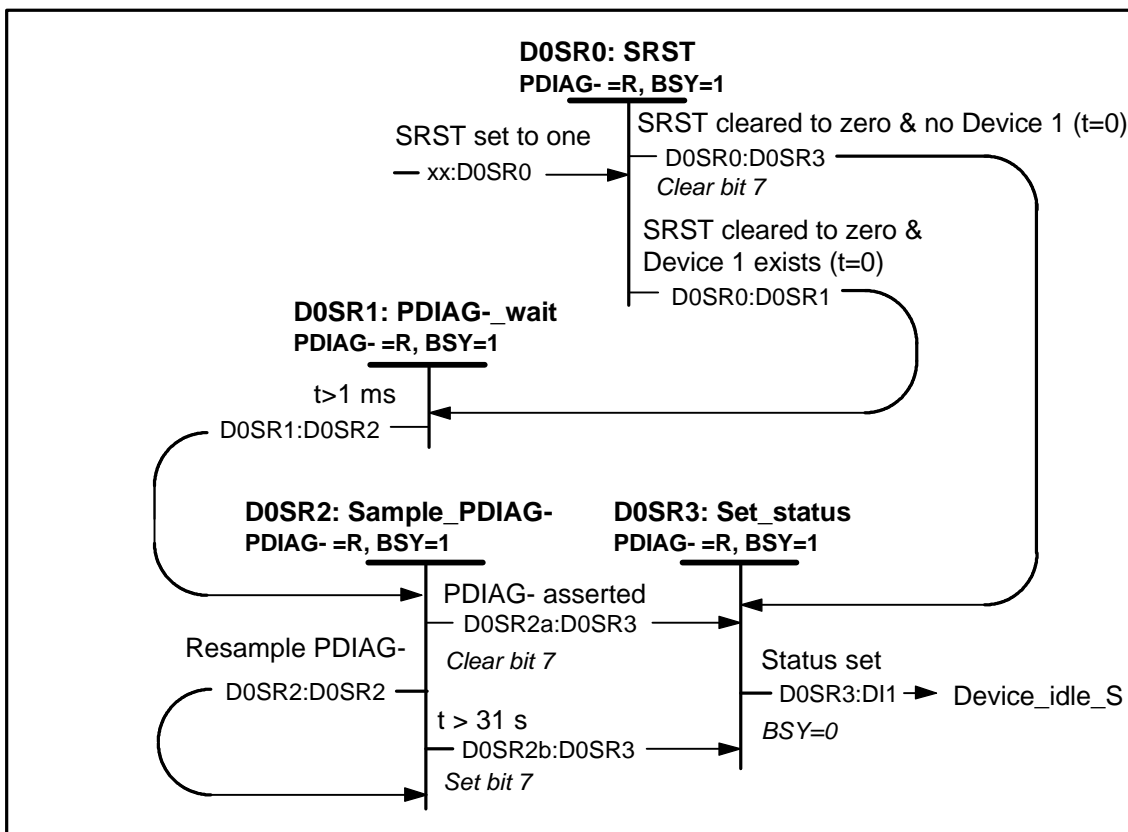


Figure 16 – Device 0 software reset protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	0	0	0	0	0	R	R	v	R

**D0SR0: SRST State:** This state is entered by Device 0 when the SRST bit is set to one in the Device Control register.

When in this state, the device shall release PDIAG-, INTRQ, IORDY, DMARQ, and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

If the device does not implement the PACKET command feature set, the device should begin performing the hardware initialization and self-diagnostic testing. The device may revert to the default condition (the device’s setting may now be in different conditions than they were before the SRST bit was set to one by the host). However, an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

If the PACKET command feature set is implemented, the device may begin performing the hardware initialization and self-diagnostic testing and the device is not expected to stop any background device activity (e.g., immediate command, see MMC or MMC-2) that was started prior to the time that SRST was set to one. The device shall not revert to the default condition and an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

**Transition D0SR0:D0SR1:** When SRST is cleared to zero and the assertion of DASP- by Device 1 was detected during the most recent power on or hardware reset, the device transitions to the D0SR1: PDIAG-\_wait state.

**Transition D0SR0:D0SR3:** When SRST is cleared to zero and the assertion of DASP- by Device 1 was not detected during the most recent power on or hardware reset, the device shall clear bit 7 to zero in the Error register and transition to the D0SR3: Set\_status state.

**D0SR1: PDIAG-\_wait State:** This state is entered when SRST has been cleared to zero and Device 1 is present.

The device shall remain in this state for at least 1 ms.

**Transition D0SR1:D0SR2:** When at least 1 ms has elapsed since SRST was cleared to zero, the device transitions to the D0SR2: Sample\_PDIAG- state.

**D0SR2: Sample\_PDIAG- State:** This state is entered when SRST has been cleared to zero for at least 1 ms.

When in this state, the device shall sample the PDIAG- signal.

**Transition D0SR2:D0SR2:** When the sample indicates that PDIAG- is not asserted and less than 31 s have elapsed since SRST was cleared to zero, then the device shall transition to the D0SR2: Sample\_PDIAG- state.

**Transition D0SR2a:D0SR3:** When the sample indicates that PDIAG- is asserted, the device shall clear bit 7 to zero in the Error register and shall transition to the D0SR3: Set\_status state.

**Transition D0SR2b:D0SR3:** When the sample indicates that PDIAG- is not asserted and 31 s have elapsed since SRST was cleared to zero, the device shall set bit 7 to one in the Error register and shall transition to the D0SR3: Set\_status state.

**D0SR3: Set\_status State:** This state is entered when Bit 7 in the Error register has been set or cleared.

When in this state the device shall complete any hardware initialization and self-diagnostic testing begun in the SRST state if not already completed.

All actions required in this state shall be completed within 31 s.

The diagnostic code shall be placed in bits 6-0 of the Error register (see Table 18). The device shall set the signature values (see 9.12). The content of the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2, and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

**Transition D0SR3:DI1:** When hardware initialization and self-diagnostic testing is completed and the status has been set, the device shall clear BSY to zero and transition to the DI1: Device\_idle\_S state (see Figure 20).

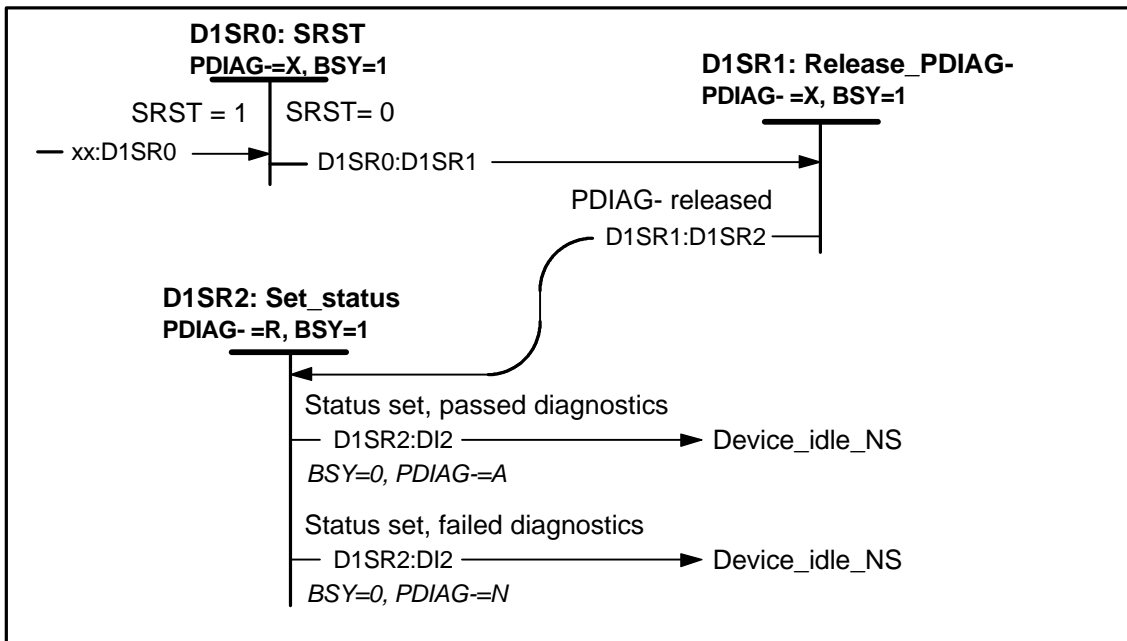


Figure 17 – Device 1 software reset protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	0	0	0	0	0	R	R	v	R

**D1SR0: SRST State:** This state is entered by Device 1 when the SRST bit is set to one in the Device Control register.

When in this state, the device shall release INTRQ, IORDY, DMARQ, and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

If the device does not implement the PACKET command feature set, the device shall begin performing the hardware initialization and self-diagnostic testing. The device may revert to the default condition (the device’s setting may now be in different conditions than they were before the SRST bit was set to one by the host). However, an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

If the PACKET command feature set is implemented, the device may begin performing the hardware initialization and self-diagnostic testing and the device is not expected to stop any background device activity (e.g., immediate command, see MMC and MMC-2) that was started prior to the time that SRST was set to one. The device shall not revert to the default condition and an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

**Transition D1SR0:D1SR1:** When SRST is cleared to zero, the device shall transition to the D1SR1: Release\_PDIAG- state.

**D1SR1: Release\_PDIAG- State:** This state is entered when SRST is cleared to zero.

When in this state, the device shall release PDIAG- within 1 ms of entering this state.

**Transition D1SR1:D1SR2:** When PDIAG- has been released, the device shall transition to the D1SR2: Set\_status state.

**D1SR2: Set\_status State:** This state is entered when the device has negated PDIAG-.



When in this state the device shall complete the hardware initialization and self-diagnostic testing begun in the SRST state if not already completed. The diagnostic code shall be placed in the Error register (see Table 18). If the device passed the self-diagnostics, the device shall assert PDIAG-.

All actions required in this state shall be completed within 30 s.

The device shall set the signature values (see 9.12). The contents of the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2, and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

**Transition D1SR2:DI2:** When hardware initialization and self-diagnostic testing is completed and the status has been set, the device shall clear BSY to zero, assert PDIAG- if it passed its diagnostics, and transition to the DI2: Device\_idle\_NS state (see Figure 20).

### 9.3 Bus idle protocol

When the selected device has BSY cleared to zero and DRQ cleared to zero the bus is idle.

If command overlap is implemented and enabled, the host may be waiting for a service request for a released command. In this case, the device is preparing for the data transfer for the released command.

If command overlap and command queuing are implemented and enabled, the host may be waiting for a service request for a number of released commands. In this case, the device is preparing for the data transfer for one of the released commands.

Figure 18 and the text following the figure describe the host state during bus idle for hosts not implementing command overlap and queuing. Figure 19 and the text following the figure describes the additional host state during bus idle required for command overlap and queuing. Figure 20 and the text following the figure describe the device state during bus idle for devices not implementing command overlap and queuing. Figure 21 and the text following the figure describe the additional device state during bus idle required for command overlap and queuing.

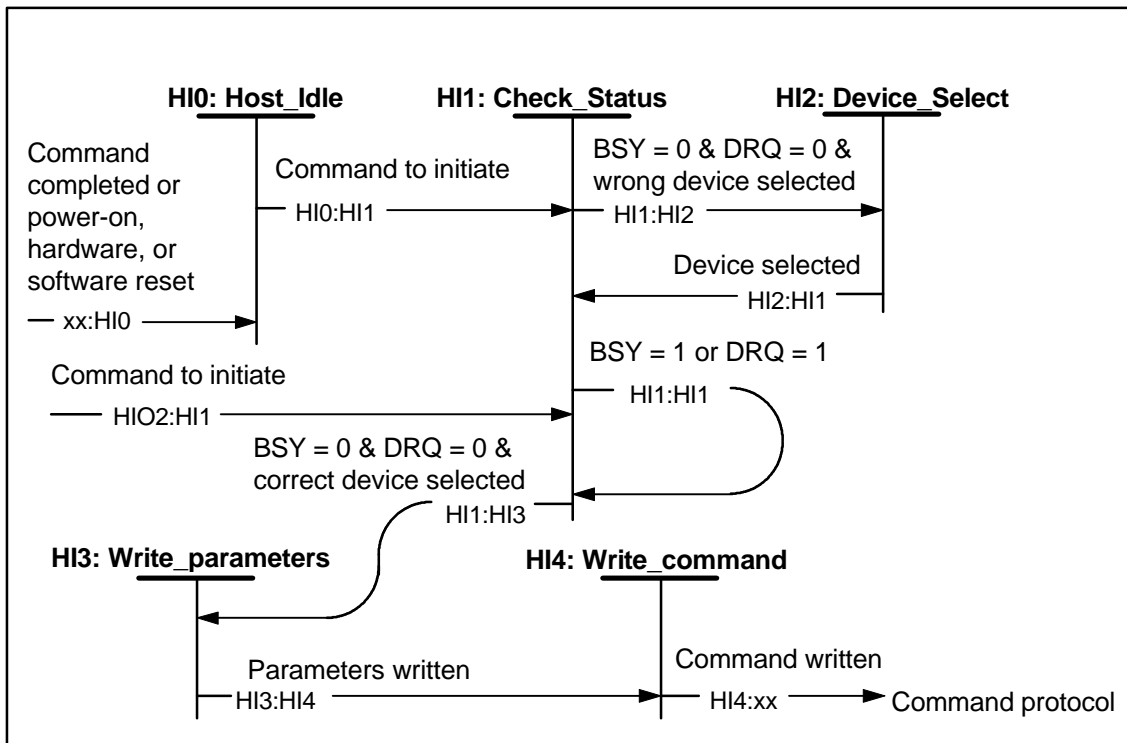


Figure 18 – Host bus idle state without overlap

**HI0: Host\_Idle State:** This state is entered when a device completes a command or when a power-on, hardware ,or software reset has occurred.

When in this state, the host waits for a command to be issued to a device.

**Transition HI0:HI1:** When the host has a command to issue to a device, the host shall transition to the HI1: Check\_Status state.

**HI1: Check\_Status State:**This state is entered when the host has a command to issue to a device.

When in this state, the host reads the device Status or Alternate Status register.

**Transition HI1:HI2:** When the status read indicates that both BSY and DRQ are cleared to zero but the wrong device is selected, then the host shall transition to the HI2: Device\_Select state.

**Transition HI1:HI1:** When the status read indicates that either BSY or DRQ is set to one, the host shall transition to the HI1: Check\_Status state to recheck the status of the selected device.

**Transition HI1:HI3:** When the status read indicates that both BSY and DRQ are cleared to zero and the correct device is selected, then the host shall transition to the HI3: Write\_Parameters state.

**HI2: Device\_Select State:** This state is entered when the wrong device is selected for issuing a new command.

When in this state, the host shall write to the Device/Head reagent to select the correct device.

**Transition HI2:HI1:** When the Device/Head register has been written to select the correct device, then the host shall transition to the HI1: Check\_Status state.

**HI3: Write\_Parameters State:** This state is entered when the host has determined that the correct device is selected and both BSY and DRQ are cleared to zero.

When in this state, the host writes all required command parameters to the device Command Block registers (see clause 8).

**Transition H13:H14:** When all required command parameters have been written to the device Command Block registers, the host shall transition to the H14: Write\_Command state.

**H14: Write\_Command State:** This state is entered when the host has written all required command parameters to the device Command Block registers.

When in this state, the host writes the command to the device Command register.

**Transition H14:xx:** When the host has written the command to the device Command register, the host shall transition to the command protocol for the command written.

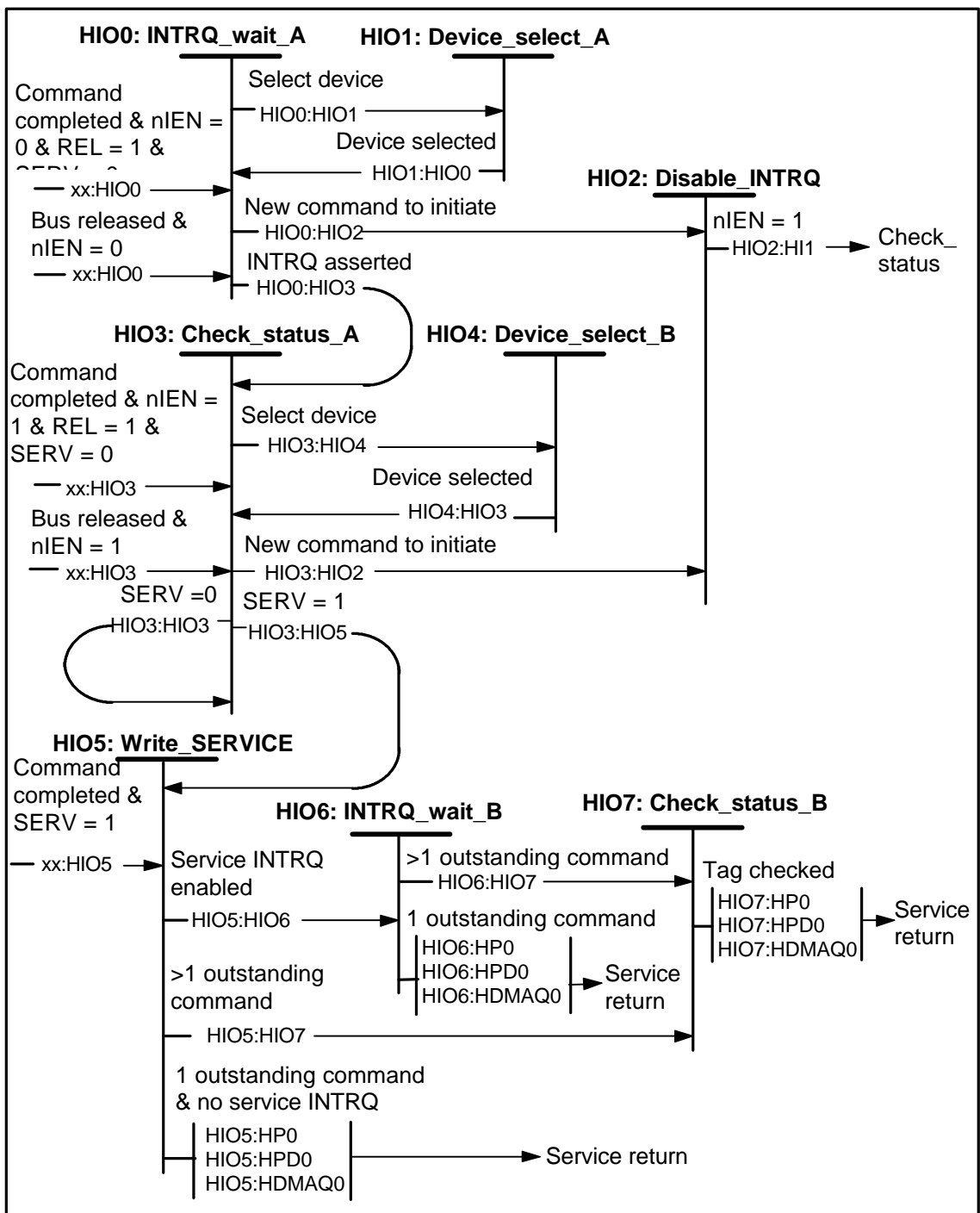


Figure 19 – Additional Host bus Idle state with Overlap or overlap and queuing

**HIO0: INTRQ\_wait\_A State:** This state is entered when a command has completed with nIEN cleared to zero, REL set to one, and SERV cleared to zero. This state is entered when the device has released the bus with nIEN cleared to zero. This state is entered when the host is waiting for INTRQ to be asserted for bus released commands.

When in this state, the host waits for INTRQ to be asserted indicating that a device is ready to resume execution of a bus released command.

**Transition HIO0:HIO1:** When the host has one or more commands outstanding to both devices, the host may transition to the HIO1: Device\_select\_A state to sample INTRQ for the other device.

**Transition HIO0:HIO2:** When the host has a new command to issue to a device and that device has no command released or supports command queuing, then the host shall transition to the HIO2: Disable\_INTRQ state.

**Transition HIO0:HIO3:** When the host detects INTRQ asserted, the host shall transition to the HIO3: Check\_status A state.

**HIO1: Device\_select\_A State:** This state is entered when the host has outstanding, bus released commands to both devices.

When in this state, the host shall disable INTRQ by setting nIEN to one, shall write the Device/Head register to select the other device, and then, shall enable INTRQ by clearing nIEN to zero.

**Transition HIO1:HIO0:** Having selected the other device, the host shall transition to the HIO0: INTRQ\_wait\_A state.

**HIO2: Disable\_INTRQ State:** This state is entered when the host has a new command to issue to a device and that device has no outstanding, bus released command or supports command queuing.

When in this state, the host shall set nIEN to one.

**Transition HIO2:HI1:** When nIEN has been set to one, the host shall transition to the HI1: Check\_status state (see Figure 18).

**HIO3: Check\_status\_A State:** This state is entered when a command is completed with nIEN set to one, REL set to one, and SERV cleared to zero. This state is entered when the device has released the bus and nIEN is set to one. This state is entered when an interrupt has occurred indicating that a device is requesting service.

When in this state, the host shall read the Status register of the device requesting service.

**Transition HIO3:HIO4:** If SERV is cleared to zero and the host has released commands outstanding to both devices, then the host may transition to the HIO4: Device\_select\_B state.

**Transition HIO3:HIO2:** If SERV is cleared to zero and the host has a new command to issue to a device, then the host shall transition to the HIO2: Disable\_INTRQ state.

**Transition HIO3:HIO3:** If SERV is cleared to zero and the host has no new command to issue, then the host shall transition to the HIO3: Check\_status state.

**Transition HIO3:HIO5:** If SERV is set to one, the host shall transition to the HIO5: Write\_SERVICE state.

**HIO4: Device\_select\_B State:** This state is entered when the host has outstanding, bus released commands to both devices.

When in this state, the host shall disable INTRQ by setting nIEN to one, shall write the Device/Head register to select the other device, and then, shall enable INTRQ by clearing nIEN to zero.

**Transition HIO4:HIO3:** Having selected the other device, the host shall transition to the HIO3: Check\_status\_A state.

**HIO5: Write\_SERVICE State:** This state is entered when a device has set SERV to one indicating that the device requests service. This state is entered when a command has completed with SERV set to one.

When in this state, the host shall write the SERVICE command to the Command register.

**Transition HIO5:HIO6:** When the device is one that implements the PACKET command feature set and the Service interrupt is enabled, then the host shall transition to the HIO6: INTRQ\_wait\_B state.

**Transition HIO5:HIO7:** When the host has more than one released command outstanding to the device and the Service interrupt is disabled, the host shall transition to the HIO7: Check\_status\_B state.

**Transition HIO5:xx:** When the Service interrupt is disabled and the host has only one released command outstanding to the device, the host shall transition to the service return for the protocol for the command outstanding (see Figure 30, Figure 32, or Figure 34).

**HIO6: INTRQ\_wait\_B State:** This state is entered when the SERVICE command has been written to a device implementing the PACKET command feature set and the Service interrupt is enabled.

When in this state, the host waits for the assertion of INTRQ.

**Transition HIO6:HIO7:** When the host has more than one released command outstanding to the device and INTRQ is asserted, the host shall transition to the HIO7: Check\_status\_B state.

**Transition HIO6:xx:** When INTRQ has been asserted and the host has only one released command outstanding to the device, then the host shall transition to the service return for the protocol for the command outstanding (see Figure 30, Figure 32, or Figure 34).

**HIO7: Check\_status\_B State:** This state is entered when the SERVICE command has been written and the host has more than one released command outstanding to the device.

When in this state the host reads the command tag to determine which outstanding command service is requested for. If a DMA data transfer is required for the command, the host shall set up the DMA engine.

**Transition HIO7:xx:** When the command for which service is requested has been determined, the host shall transition to the service return for that command protocol (see Figure 30, Figure 32, or Figure 34).

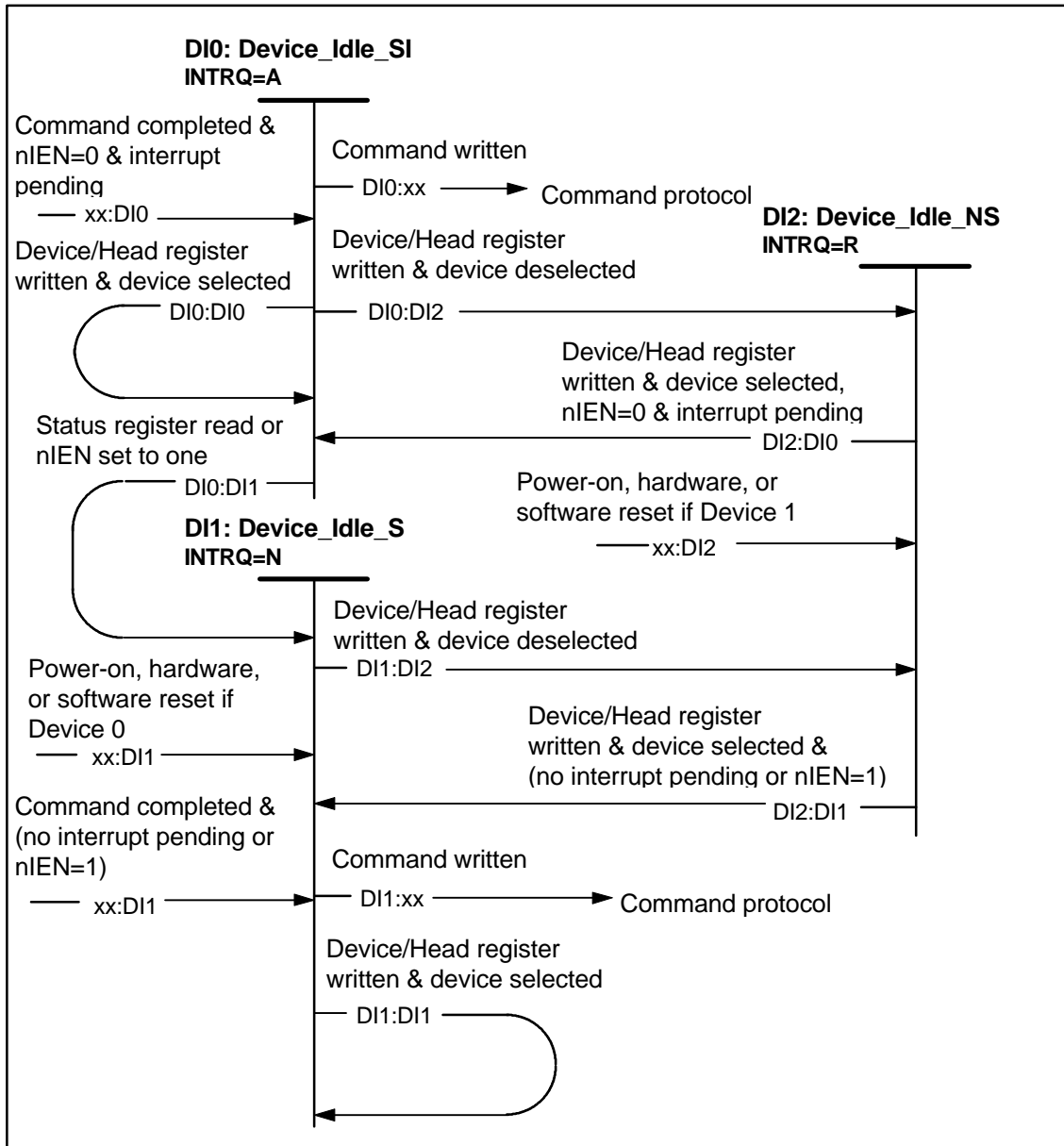


Figure 20 – Device bus Idle state without overlap

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
0	0	0	0	0	0	v	R	R	R

**DI0: Device Idle\_SI State (selected/INTRQ asserted) :** This state is entered when the device has completed the execution of a command protocol with interrupt pending and nIEN=0.

When in this state, the device shall have DRQ cleared to zero, INTRQ asserted, and BSY cleared to zero. Reading any register except the Status register shall have no effect.

**Transition DI0:xx:** If the Command register is written, the device shall clear the device internal interrupt pending, shall negate or release INTRQ within 400 ns of the negation of DIOW-, shall release PDIAG- if asserted, and shall transition to the command protocol indicated by the content of the Command register. The host should not write to the Command register at this time.

**Transition DI0:D11:** When the Status register is read, the device shall clear the device internal interrupt pending, negate or release INTRQ within 400 ns of the negation of DIOR-, and transition to the DI1:

Device\_Idle\_S state. When nIEN is set to one in the Device Control register, the device shall negate INTRQ and transition to the DI1: Device\_Idle\_S state.

**Transition DI0:DI0:** When the Device/Head register is written and the DEV bit selects this device or any other register except the Command register is written, the device shall transition to the DI0: Device\_Idle\_SI state.

**Transition DI0:DI2:** When the Device/Head register is written and the DEV bit selects the other device, then the device shall release INTRQ within 400 ns of the negation of DIOW-, and transition to the DI2: Device\_Idle\_NS state.

**DI1: Device\_Idle\_S State (selected/INTRQ negated) :** This state is entered when the device has completed the execution of a command protocol with no interrupt pending or nIEN=1, or when a pending interrupt is cleared. This state is also entered by Device 0 at the completion of a power-on, hardware, or software reset.

When in this state, the device shall have BSY and DRQ cleared to zero and INTRQ negated or released.

When entering this state from a power on, hardware, or software reset, if the device does not implement the PACKET command feature set, the device shall set DRDY to one within 30 s of entering this state. When entering this state from a power on, hardware, or software reset, if the device does implement the PACKET command feature set, the device shall not set DRDY to one.

**Transition DI1:xx:** When the Command register is written, the device shall exit the interrupt pending state, release PDIAG- if asserted and transition to the command protocol indicated by the content of the Command register.

**Transition DI1:DI1:** When the Device/Head register is written and the DEV bit selects this device or any register is written except the Command register, the device shall transition to the DI1: Device\_Idle\_S state.

**Transition DI1:DI2:** When the Device/Head register is written and the DEV bit selects the other device, the device shall transition to the DI2: Device\_Idle\_NS state.

**DI2: Device\_Idle\_NS State (not selected):** This state is entered when the device is deselected. This state is also entered by Device 1 at the completion of a power-on, hardware, or software reset.

When in this state, the device shall have BSY and DRQ cleared to zero and INTRQ shall be released.

When entering this state from a power on, hardware, or software reset, if the device does not implement the PACKET command feature set, the device shall set DRDY to one within 30 s of entering this state. When entering this state from a power on, hardware, or software reset, if the device does implement the PACKET command feature set, the device shall not set DRDY to one.

**Transition DI2:DI0:** When the Device/Head register is written, the DEV bit selects this device, the device has an interrupt pending, and nIEN is cleared to zero, then the device shall assert INTRQ within 400 ns of the negation of DIOW- and transition to the DI0: Device\_Idle\_SI state.

**Transition DI2:DI1:** When the Device/Head register is written, the DEV bit selects this device, and the device has no interrupt pending or nIEN is set to one, then the device shall transition to the DI1: Device\_Idle\_S state.



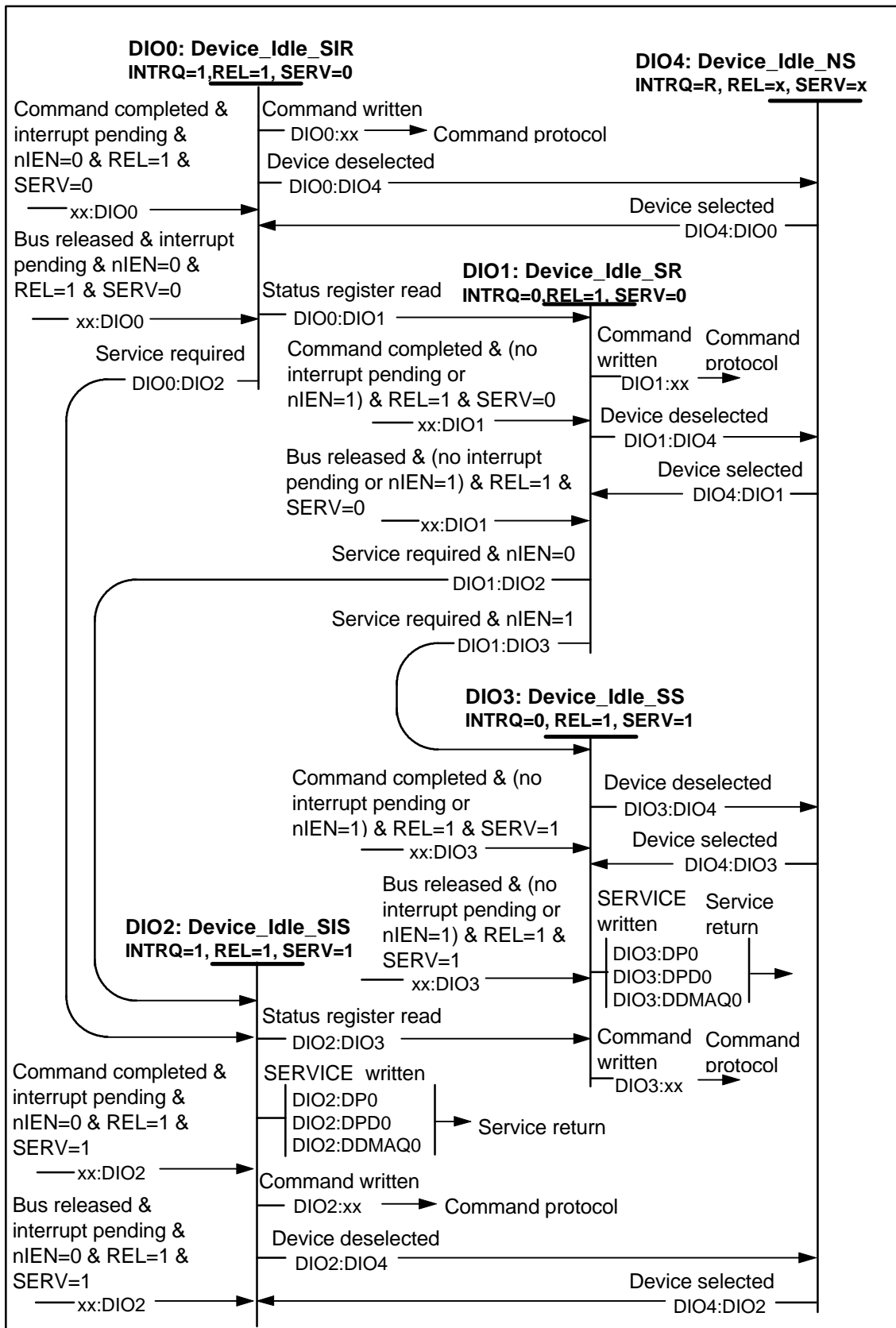


Figure 21 – Additional Device bus Idle states with Overlap or overlap and queuing

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
0	0	v	v	x	x	v	R	R	R

**DIO0: Device\_Idle\_SIR State** (selected/INTRQ asserted/REL set to one) : This state is entered when the device has completed the execution of a command protocol with interrupt pending, nIEN=0, REL set to one, and SERV cleared to zero. This state is entered when the device has released an overlapped command with interrupt pending, nIEN=0, REL set to one, and SERV cleared to zero.

When in this state, the device is preparing for completion of a released command. The device shall have BSY and DRQ cleared to zero, and INTRQ asserted.

**Transition DIO0:xx:** When the Command register is written, the device shall clear the device internal interrupt pending, shall negate or release INTRQ within 400 ns of the negation of DIOW-, and shall transition to the command protocol indicated by the content of the Command register.

NOTE – Only commands in the queued command set may be written without error.

**Transition DIO0:DIO1:** When the Status register is read, the device shall clear the device internal interrupt pending, negate or release INTRQ within 400 ns of the negation of DIOR-, and transition to the DIO1: Device\_Idle\_SR state.

**Transition DIO0:DIO2:** When the Device/Head register is written and the DEV bit selects the other device, then the device shall release INTRQ within 400 ns of the negation of DIOW- and transition to the DIO2: Device\_Idle\_NS state.

**Transition DIO0:DIO2:** When the device is ready to continue the execution of a released command, the device shall transition to the DIO2: Device\_idle\_SIS state.

**DIO1: Device\_Idle\_SR State** (selected/INTRQ negated/REL set to one) : This state is entered when the device has completed the execution of a command protocol with no interrupt pending or nIEN=1, REL set to one, and SERV cleared to zero. This state is entered when the device has released an overlapped command with no interrupt pending or nIEN=1, REL set to one, and SERV cleared to zero. This state is entered when a pending interrupt is cleared, REL is set to one, and SERV is cleared to zero.

When in this state, the device is preparing for completion of a released command. The device shall have BSY and DRQ cleared to zero, and INTRQ negated or released.

**Transition DIO1:xx:** When the Command register is written, the device shall transition to the command protocol indicated by the content of the Command register.

NOTE – Only commands in the queued command set may be written without error.

**Transition DIO1:DIO4:** When the Device/Head register is written and the DEV bit selects the other device, the device shall transition to the DIO4: Device\_Idle\_NS state.

**Transition DIO1:DIO2:** When the device is ready to continue the execution of a released command and nIEN=0, the device shall transition to the DIO2: Device\_idle\_SIS state.

**Transition DIO1:DIO3:** When the device is ready to continue the execution of a released command and nIEN=1, the device shall transition to the DIO3: Device\_idle\_SS state.

**DIO2: Device\_Idle\_SIS State** (selected/INTRQ asserted/SERV set to one) : This state is entered when the device has completed the execution of a command protocol with interrupt pending, nIEN=0, REL set to one, and SERV set to one. This state is entered when the device has released an overlapped with interrupt pending, nIEN=0, REL set to one, and SERV set to one.

**Transition DIO2:DIO3:** When the Status register is read, the device shall clear the device internal interrupt pending, negate or release INTRQ within 400 ns of the negation of DIOR-, and transition to the DIO3: Device\_Idle\_SS state.

**Transition DIO2: DIO4:** When the Device/Head register is written and the DEV bit selects the other device, the device shall release INTRQ within 400 ns of the negation of DIOW- and transition to the DIO4: Device\_Idle\_NS state.

**Transition DIO2a:xx:** When the SERVICE command is written into the Command register, the device shall set the Tag for the command to be serviced, negate or release INTRQ within 400 ns of the negation of DIOW-, and transition to the Service return of the command ready for service (see Figure 31 Device PACKET non-data and PIO data command protocol, Figure 33 Device PACKET DMA command protocol, or Figure 35 Device DMA QUEUED command protocol).

**Transition DIO2b:xx:** When any overlapped command other than SERVICE is written to the Command register, the device shall negate or release INTRQ within 400 ns of the negation of DIOW- and transition to the protocol for the new command.

**DIO3: Device\_Idle\_SS State (selected/INTRQ negated/SERV set to one) :** This state is entered when the device has completed the execution of a command protocol with no interrupt pending or nIEN=1, REL set to one, and SERV set to one. This state is entered when the device has released an overlapped with no interrupt pending or nIEN=1, REL set to one, and SERV set to one.

**Transition DIO3: DIO4:** When the Device/Head register is written and the DEV bit selects the other device, the device shall transition to the DIO4: Device\_Idle\_NS state.

**Transition DIO3a:xx:** When the SERVICE command is written into the Command register, the device shall set the Tag for the command to be serviced and transition to the Service return of the command ready for service (see Figure 31, Figure 33, or Figure 35).

**Transition DIO3b:xx:** When any overlapped command other than SERVICE is written to the Command register, the device shall transition to the protocol for the new command.

**DIO4: Device\_Idle\_NS State (not selected) :** This state is entered when the device is deselected with REL or SERV set to one.

When in this state, the device shall have BSY and DRQ cleared to zero and INTRQ shall be released.

**Transition DIO4:DIO0:** When the Device/Head register is written, the DEV bit selects this device, the device has an interrupt pending, nIEN is cleared to zero, REL is set to one, and SERV is cleared to zero, then the device shall assert INTRQ within 400 ns of the negation of DIOW- and transition to the DIO0: Device\_Idle\_SIR state.

**Transition DIO4:DIO1:** When the Device/Head register is written, the DEV bit selects this device, the device has no interrupt pending or nIEN is set to one, REL is set to one, and SERV is cleared to zero, then the device transitions to the DIO1: Device\_Idle\_SIR state.

**Transition DIO4:DIO2:** When the Device/Head register is written, the DEV bit selects this device, the device has an interrupt pending, nIEN is cleared to zero, REL is set to one, and SERV is set to one, then the device shall assert INTRQ within 400 ns of the negation of DIOW- and transition to the DIO2: Device\_Idle\_SIS state.

**Transition DIO4:DIO3:** When the Device/Head register is written, the DEV bit selects this device, the device has no interrupt pending or nIEN is set to one, REL is set to one, and SERV is set to one, then the device transitions to the DIO3: Device\_Idle\_SIR state.

## 9.4 Non-data command protocol

This class includes:

- CFA ERASE SECTORS
- CFA REQUEST EXTENDED ERROR CODE
- CHECK POWER MODE
- FLUSH CACHE
- GET MEDIA STATUS
- IDLE
- IDLE IMMEDIATE
- INITIALIZE DEVICE PARAMETERS
- MEDIA EJECT
- MEDIA LOCK
- MEDIA UNLOCK
- NOP
- READ NATIVE MAX ADDRESS
- READ VERIFY SECTOR(S)
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- SEEK
- SET FEATURES
- SET MAX ADDRESS
- SET MULTIPLE MODE
- SLEEP
- SMART DISABLE OPERATION
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATION
- SMART EXECUTE OFFLINE IMMEDIATE
- SMART RETURN STATUS
- STANDBY
- STANDBY IMMEDIATE

Execution of these commands involves no data transfer. Figure 22 and the text following the figure describes the host state. Figure 23 and the text following the figure describes the device state.

See the NOP command description in 8.20 and the SLEEP command in 8.40 for additional protocol requirements.

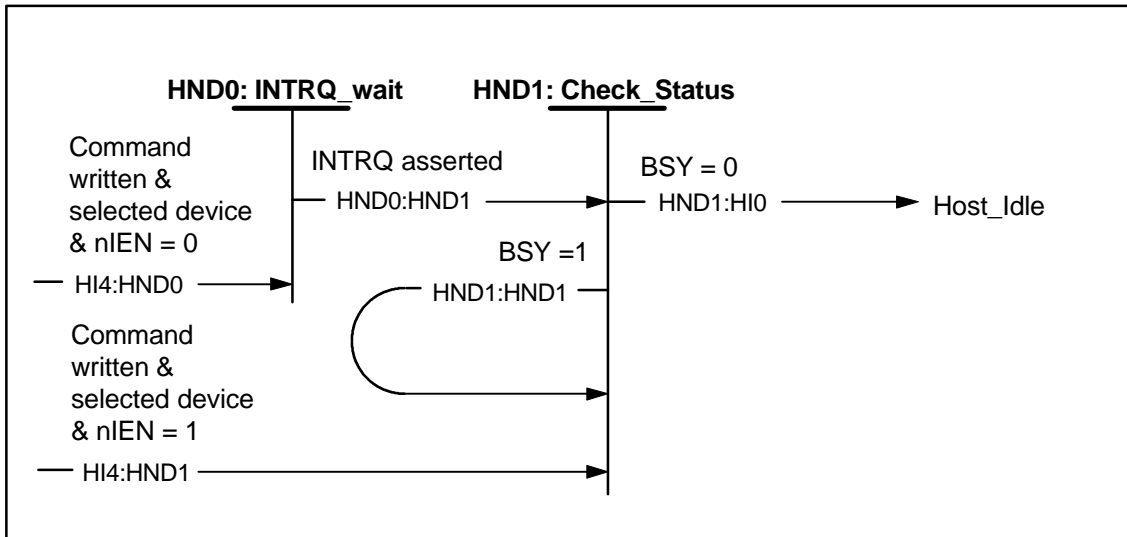


Figure 22 – Host Non-Data state

**HND0: INTRQ\_Wait\_State:** This state is entered when the host has written a non-data command to the device and the nIEN bit in the device has been cleared to zero.

When in this state the host may wait for INTRQ to be asserted by the device.

**Transition HND0:HND1:** When the device asserts INTRQ, the host shall transition to the HND1: Check\_Status state.

**HND1: Check\_Status State:** This state is entered when the host has written a non-data command to the device and the nIEN bit in the device has been set to one, or when INTRQ has been asserted.

When in this state, the host shall read the device Status register. When entering this state from another state, the host shall wait 400 ns before reading the Status register.

**Transition HND1:HIO:** When the status read indicates both BSY and DRQ are cleared to zero, the host shall transition to the HIO: Host\_Idle state (see Figure 18). If status indicates that an error has occurred, the host shall take appropriate error recovery action.

**Transition HND1:HND1:** When the status read indicates that either BSY or DRQ is set to one, the host shall transition to the HND1: Check\_Status state to recheck device status.

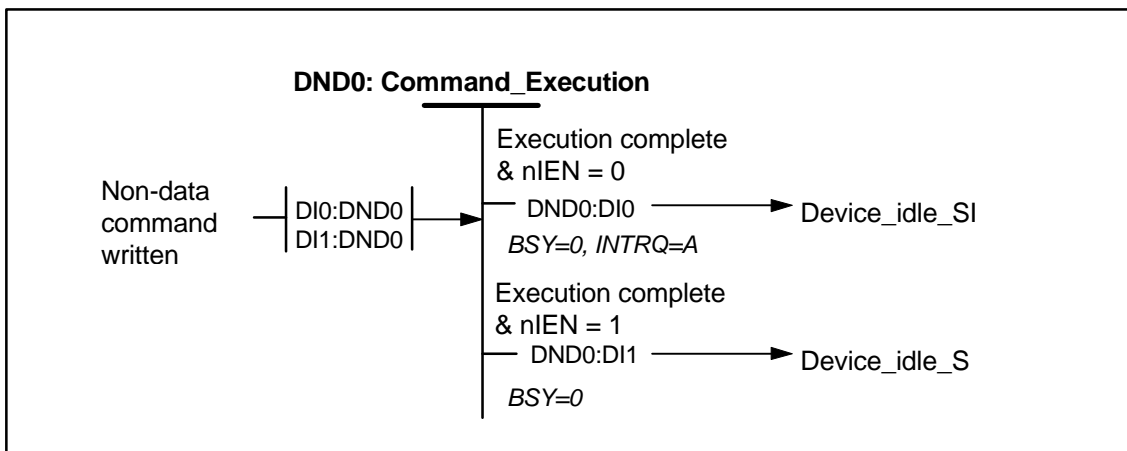


Figure 23 – Device Non-Data state

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	R	R	R	R

**DND0: Command\_Execution State:** This state is entered when a non-data command has been written to the device Command register.

When in this state, the device shall set BSY to one within 400 ns of the writing of the Command register, shall execute the requested command, and shall set the device internal interrupt pending.

**Transition DND0:DI0:** When command execution completes and nIEN is cleared to zero, then the device shall set error bits if appropriate, clear BSY to zero, assert INTRQ, and transition to the DI0: Device\_Idle\_SI state (see Figure 20).

**Transition DND0:DI1:** When command execution completes and nIEN is set to one, the device shall set error bits if appropriate, clear BSY to zero, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

## 9.5 PIO data-in command protocol

This class includes:

- CFA TRANSLATE SECTOR
- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- READ BUFFER
- READ MULTIPLE
- READ SECTOR(S)
- SMART READ DATA
- SMART READ LOG SECTOR

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. Figure 24 and the text following the figure describes the host states. Figure 25 and the text following the figure describes the device states.

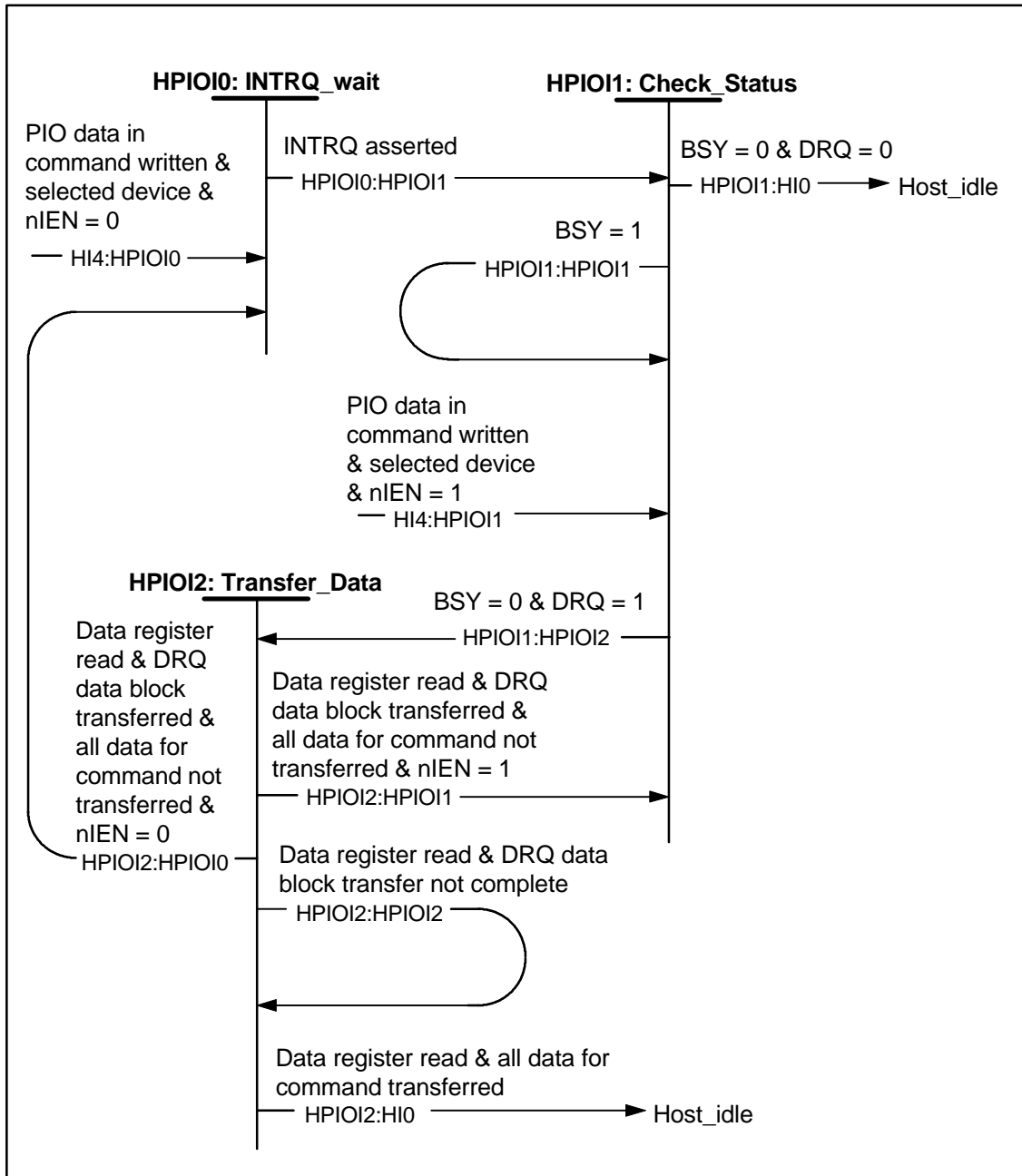


Figure 24 – Host PIO data-In state

**HPIO10: INTRQ\_Wait State:** This state is entered when the host has written a PIO data-in command to the device and nIEN is cleared to zero, or at the completion of a DRQ data block transfer if all the data for the command has not been transferred and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

**Transition HPIO10:HPIO11:** When INTRQ is asserted, the host shall transition to the HPIO11: Check\_Status state.

**HPIO11: Check\_Status State:** This state is entered when the host has written a PIO data-in command to the device and nIEN is set to one, or when INTRQ is asserted.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HPIO2 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

**Transition HPIO1:HI0:** When BSY is cleared to zero and DRQ is cleared to zero, then the device has completed the command with an error. The host shall perform appropriate error recovery and transition to the HI0: Host\_Idle state (see Figure 18).

**Transition HPIO1:HPIO1:** When BSY is set to one , the host shall transition to the HPIO1: Check\_Status state.

**Transition HPIO1:HPIO2:** When BSY is cleared to zero and DRQ is set to one, the host shall transition to the HPIO2: Transfer\_Data state.

**HPIO2: Transfer\_Data State:** This state is entered when the BSY is cleared to zero, DRQ is set to one, and the DRQ data block transfer has not completed.

When in this state, the host shall read the device Data register to transfer data.

**Transition HPIO2:HPIO0:** When the host has read the device Data register and the DRQ data block has been transferred, all blocks for the command have not been transferred, and nIEN is cleared to zero, then the host shall transition to the HPIO0: INTRQ\_Wait state.

**Transition HPIO2:HPIO1:** When the host has read the device Data register and the DRQ data block has been transferred, all blocks for the command have not been transferred, and nIEN is set to one, then the host shall transition to the HPIO1: Check\_Status state.

**Transition HPIO2:HPIO2:** When the host has read the device status register and the DRQ data block transfer has not completed, then the host shall transition to the HPIO2: Transfer\_Data state.

**Transition HPIO2:HI0:** When the host has read the device Data register and all blocks for the command have been transferred, then the host shall transition to the HI0: Host\_Idle state (see Figure 18). The host may read the Status register.



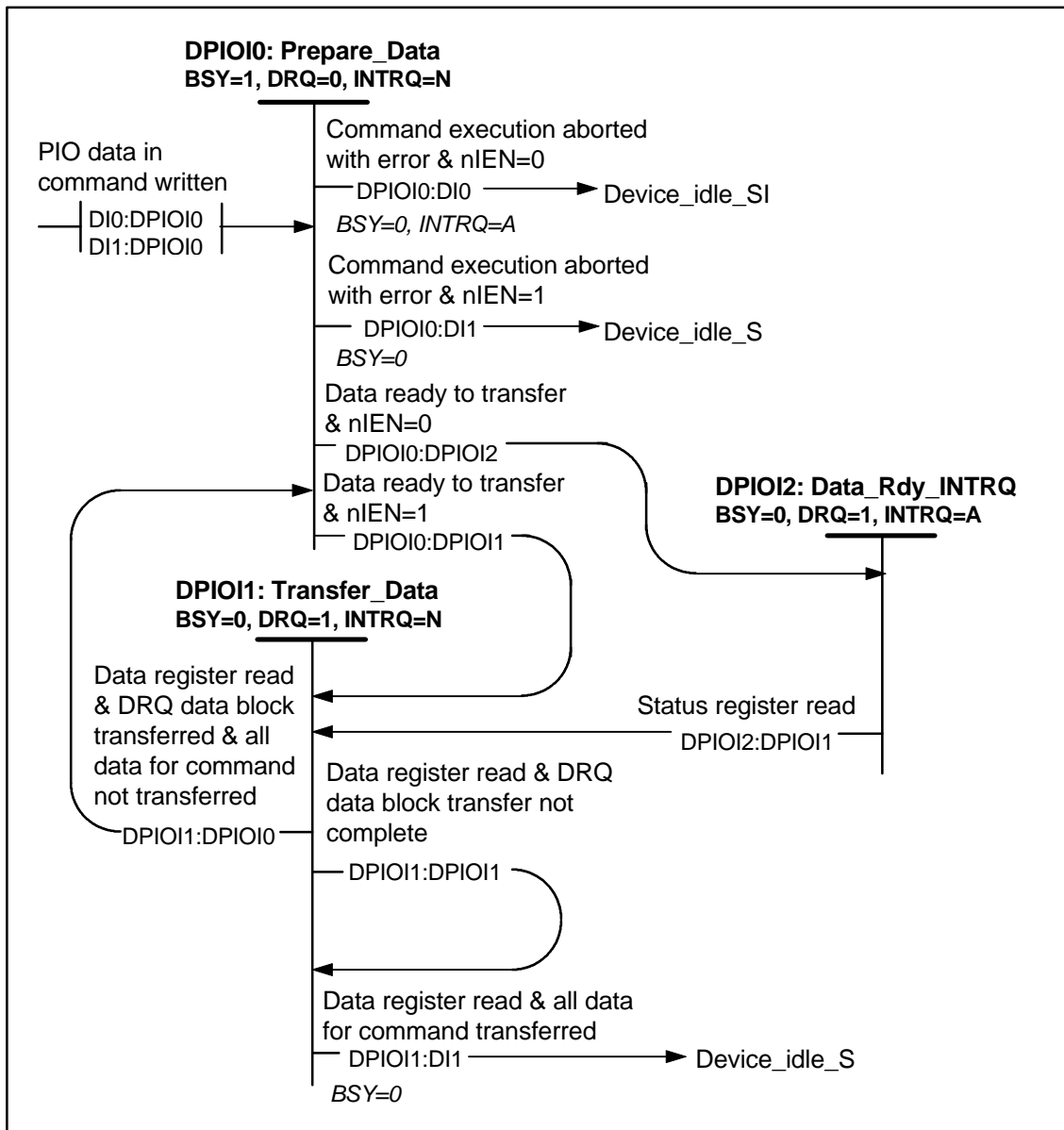


Figure 25 – Device PIO data-In state

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	0	0	0	0	v	R	R	R

**DPIOI0: Prepare Data State:** This state is entered when the device has a PIO data-in command written to the Command register.

When in this state, device shall set BSY to one within 400 ns of the writing of the Command register and prepare the requested data for transfer to the host.

For IDENTIFY DEVICE and IDENTIFY PACKET DEVICE commands, if the device tests CBLID- it shall do so and update bit 13 in word 93.

**Transition DPIOI0:DI0:** When an error is detected that causes the command to abort and nIEN is cleared to zero, then the device shall set the appropriate error bits, clear BSY to zero, assert INTRQ, and transition to the DI0: Device\_Idle\_SI state (see Figure 20).

**Transition DPIO0:DI1:** When an error is detected that causes the command to abort and nIEN is set to one, then the device shall set the appropriate error bits, clear BSY to zero, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

**Transition DPIO0:DPIO1:** When the device has a DRQ data block ready to transfer and nIEN is set to one, then the device shall transition to the DPIO1: Transfer\_Data state.

**Transition DPIO0:DPIO2:** When the device has a DRQ data block ready to transfer and nIEN is cleared to zero, then the device transitions to the DPIO2: Data\_Ready\_INTRQ state.

**DPIO1: Data\_Transfer State:** This state is entered when the device is ready to transfer a DRQ data block and nIEN is set to one, or when the INTRQ indicating that the device is ready to transfer a DRQ data block has been acknowledged by a read of the Status register.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, and the device has a data word ready in the Data register for transfer to the host.

**Transition DPIO1:DPIO1:** When the Data register is read and transfer of the DRQ data block has not completed, then the device shall transition to the DPIO1: Data\_Transfer state.

**Transition DPIO1:DPIO0:** When the Data register is read and the transfer of the current DRQ data block has completed, but all blocks for this request have not been transferred, then the device shall transition to the DPIO0: Prepare\_Data state.

**Transition DPIO1:DI1:** When the Data register is read and all blocks for this request have been transferred, then the device shall clear BSY to zero and transition to the DI1: Device\_Idle\_S state (see Figure 20). The device internal interrupt pending is not set on this transition.

**DPIO2: Data\_Ready\_INTRQ State:** This state is entered when the device has a DRQ data block ready to transfer and nIEN is cleared to zero.

When in this state, BSY is cleared to zero, DRQ is set to one, and INTRQ is asserted.

**Transition DPIO2:DPIO1:** When the Status register is read, then the device shall clear the device internal interrupt pending, negate INTRQ, and transition to the DPIO1: Data\_Transfer state.

## 9.6 PIO data-out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SMART WRITE LOG SECTOR
- WRITE BUFFER
- WRITE MULTIPLE
- WRITE SECTOR(S)

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 26 and the text following the figure describes the host states. Figure 27 and the text following the figure describes the device states.

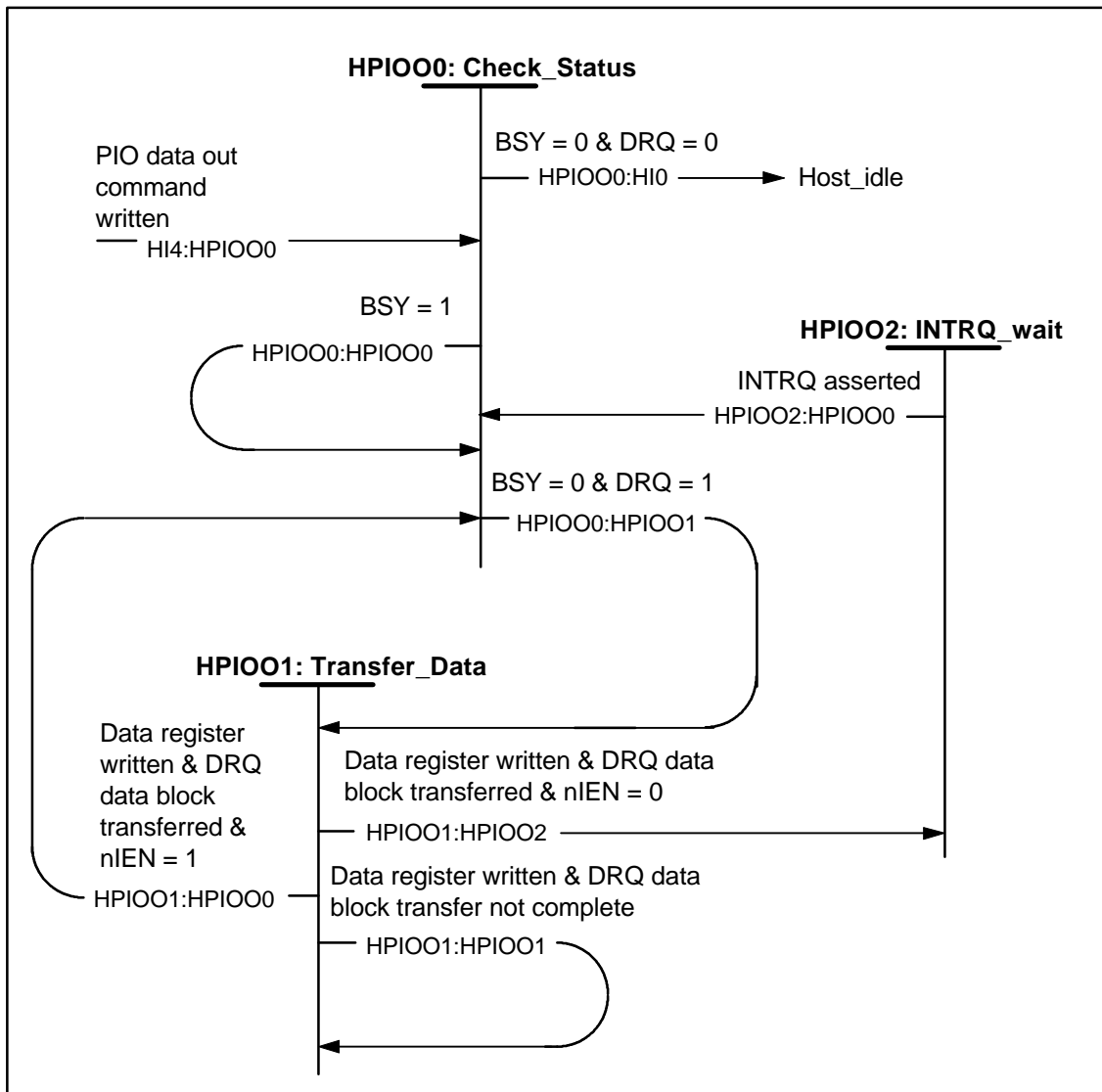


Figure 26 – Host PIO data-Out state

**HPIO00: Check\_Status State:** This state is entered when the host has written a PIO data-out command to the device; when a DRQ data block has been written and  $nIEN$  is set to one; or when a DRQ data block has been written,  $nIEN$  is cleared zero, and INTRQ has been asserted.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HPIO01 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

**Transition HPIO00:HI0:** When  $BSY$  is cleared to zero and  $DRQ$  is cleared to zero, then the device has completed the command and shall transition to the HI0: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HPIO00:HPIO00:** When  $BSY$  is set to one and  $DRQ$  is cleared to zero, the host shall transition to the HPIO00: Check\_Status state.

**Transition HPIO00:HPIO01:** When  $BSY$  is cleared to zero and  $DRQ$  is set to one, the host shall transition to the HPIO01: Transfer\_Data state.

**HPIOO1: Transfer\_Data State:** This state is entered when the BSY is cleared to zero, DRQ is set to one.

When in this state, the host shall write the device Data register to transfer data.

**Transition HPIOO1:HPIOO2:** When the host has written the device Data register, the DRQ data block has been transferred, and nIEN is cleared to zero, then the host shall transition to the HPIOO2: INTRQ\_Wait state.

**Transition HPIOO1:HPIOO0:** When the host has written the device Data register, the DRQ data block has been transferred, and nIEN is set to one, then the host shall transition to the HPIOO0: Check\_Status state.

**Transition HPIOO1:HPIOO1:** When the host has written the device Data register and the DRQ data block transfer has not completed, then the host shall transition to the HPIOO1: Transfer\_Data state.

**HPIOO2: INTRQ\_Wait State:** This state is entered when the host has completed a DRQ data block transfer and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

**Transition HPIOO2:HPIOO0:** When INTRQ is asserted, the host shall transition to the HPIOO0: Check\_Status state.

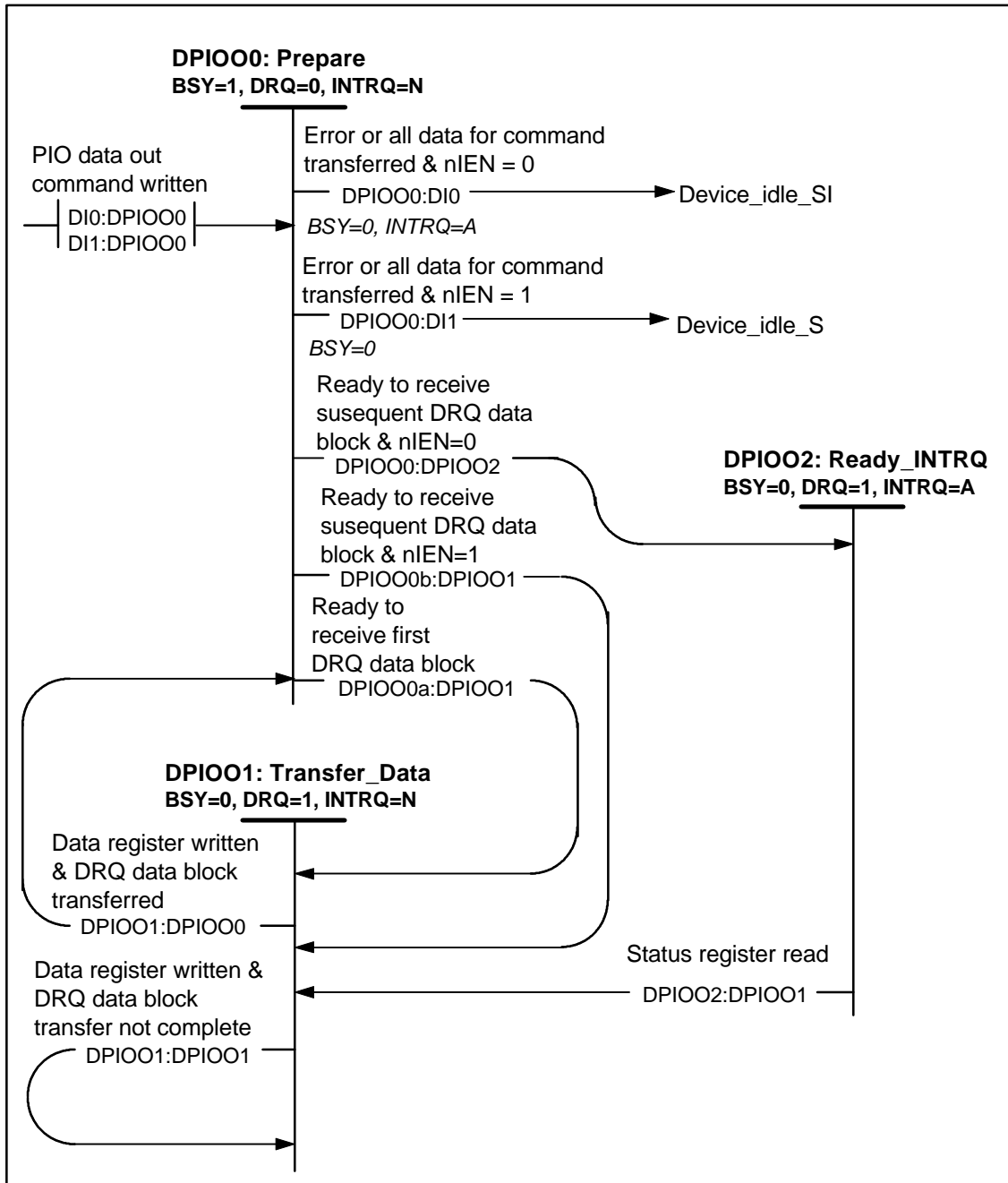


Figure 27 – Device PIO data-Out state

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	0	0	0	0	v	R	R	R

**DPIOO0: Prepare State:** This state is entered when the device has a PIO data-out command written to the Command register or when a DRQ data block has been transferred.

When in this state, device shall set BSY to one within 400 ns of the writing of the Command register, shall clear DRQ to zero, and negate INTRQ. The device shall check for errors, determine if the data transfer is complete, and if not, prepare to receive the next DRQ data block.

**Transition DPIOO0a:DPIOO1:** When the device is ready to receive the first DRQ data block for a command, the device shall transition to the DPIOO1: Transfer\_Data state.

**Transition DPIO0b:DPIO01:** When the device is ready to receive a subsequent DRQ data block for a command and nIEN is set to one, then the device shall set the device internal interrupt pending and transition to the DPIO01: Transfer\_Data state.

**Transition DPIO00:DPIO02:** When the device is ready to receive a subsequent DRQ data block for a command and nIEN is cleared to zero, then the device shall set the device internal interrupt pending and transition to the DPIO02: Ready\_INTRQ state.

**Transition DPIO00:DIO:** When all data for the command has been transferred or an error occurs that causes the command to abort, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, clear BSY to zero, assert INTRQ, and transition to the DIO: Device\_Idle\_SI state (see Figure 20).

**Transition DPIO00:DI1:** When all data for the command has been transferred or an error occurs that causes the command to abort, and nIEN is set to one, then the device shall set the device internal interrupt pending, set appropriate error bits, clear BSY to zero, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

**DPIO01: Data\_Transfer State:** This state is entered when the device is ready to receive a DRQ data block.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, and the device receives a data word in the Data register.

**Transition DPIO01:DPIO01:** When the Data register is written and transfer of the DRQ data block has not completed, then the device shall transition to the DPIO01: Data\_Transfer state.

**Transition DPIO01:DPIO00:** When the Data register is written and the transfer of the current DRQ data block has completed, then the device shall transition to the DPIO00: Prepare state.

**DPIO02: Ready\_INTRQ State:** This state is entered when the device is ready to receive a DRQ data block and nIEN is cleared to zero.

When in this state, BSY is cleared to zero, DRQ is set to one, and INTRQ is asserted.

**Transition DPIO02:DPIO01:** When the Status register is read, the device shall clear the device internal interrupt pending, negate INTRQ, and transition to the DPIO01: Data\_Transfer state.

## 9.7 DMA command protocol

This class includes:

- READ DMA
- WRITE DMA

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host or from the device to the host using DMA transfer. The host shall initialize the DMA channel prior to transferring data. A single interrupt is issued at the completion of the successful transfer of all data required by the command. Figure 28 and the text following the figure describes the host states. Figure 29 and the text following the figure describes the device states.

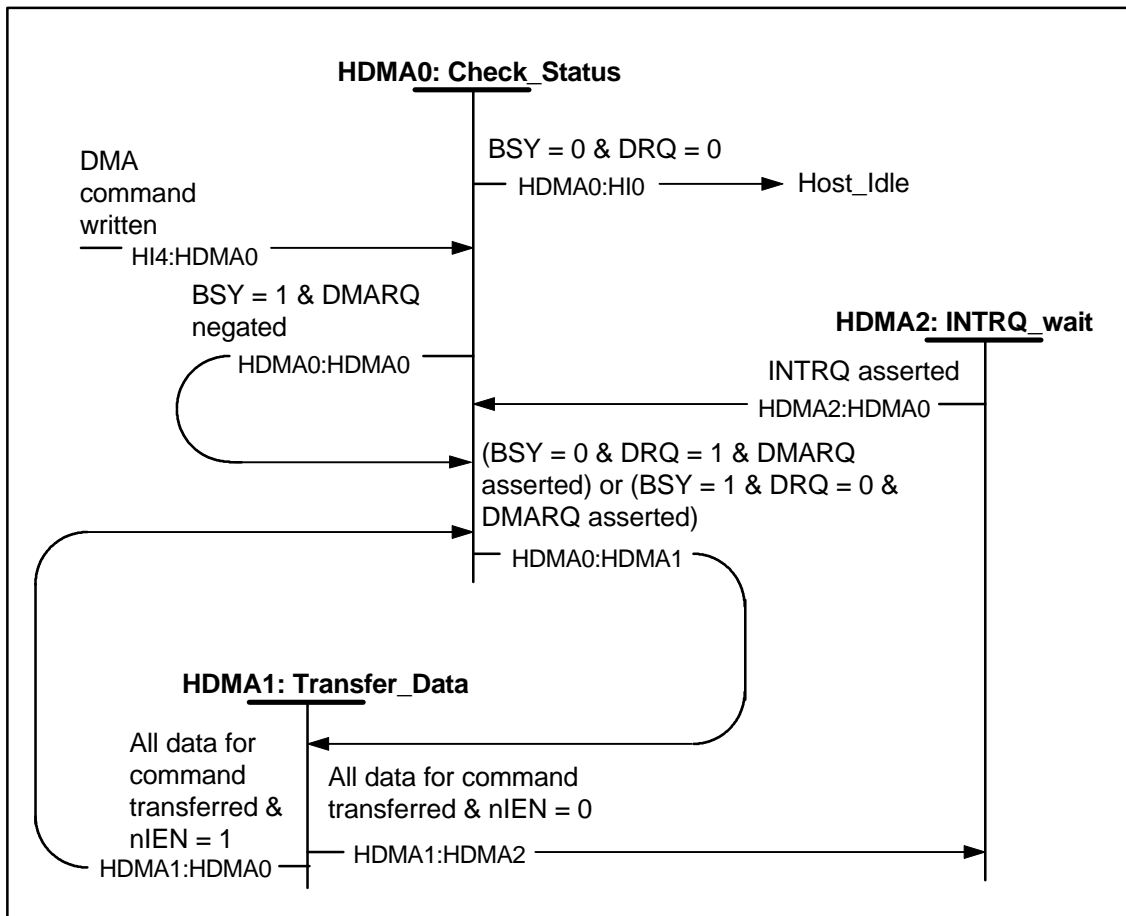


Figure 28 – Host DMA state

**HDMA0: Check\_Status State:** This state is entered when the host has written a DMA command to the device; when all data for the command has been transferred and nIEN is set to one; or when all data for the command has been transferred, nIEN is cleared zero, and INTRQ has been asserted.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HDMA1 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

**Transition HDMA0:HI0:** When the BSY is cleared to zero and DRQ is cleared to zero, then the device has completed the command and shall transition to the HI0: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HDMA0:HDMA0:** When BSY is set to one, DRQ is cleared to zero, and DMARQ is negated, then the host shall transition to the HDMA0: Check\_Status state.

**Transition HDMA0:HDMA1:** When BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted; or if BSY is set to one, DRQ is cleared to zero, and DMARQ is asserted, then the host shall transition to the HDMA1: Transfer\_Data state. The host shall have set up the host DMA engine prior to making this transition.

**HDMA1: Transfer\_Data State:** This state is entered when BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted; or BSY is set to one, DRQ is cleared to zero, and DMARQ is asserted. The host shall have initialized the DMA channel prior to entering this state.

When in this state, the host shall perform the data transfer as described in the Multiword DMA timing or the Ultra DMA protocol.

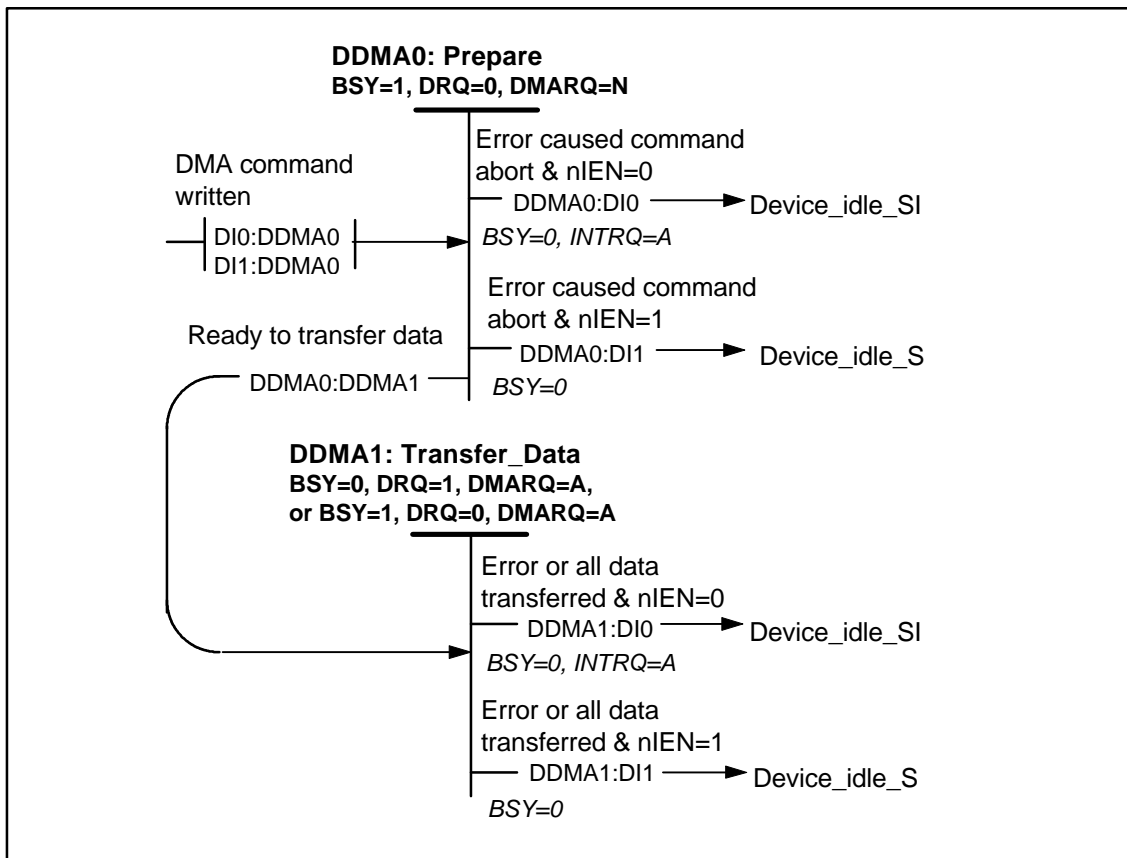
**Transition HDMA1:HDMA2:** When the host has transferred all data for the command and nIEN is cleared to zero, then the host shall transition to the HDMA2: INTRQ\_Wait state.

**Transition HDMA1:HDMA0:** When the host has transferred all data for the command and nIEN is set to one, then the host shall transition to the HDMA0: Check\_Status state.

**HDMA2: INTRQ\_Wait State:** This state is entered when the host has completed the transfer of all data for the command and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

**Transition HDMA2:HDMA0:** When INTRQ is asserted, the host shall transition to the HDMA0: Check\_Status state.



**Figure 29 – Device DMA state**

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	0	0	0	0	N	v	R	R

**DDMA0: Prepare State:** This state is entered when the device has a DMA command written to the Command register.

When in this state, device shall set BSY to one, shall clear DRQ to zero, and negate INTRQ. The device shall check for errors, and prepare to transfer data.



**Transition DDMA0:DI0:** When an error is detected that causes the command to abort and nIEN is cleared to zero, the device shall set the appropriate error bits, enter the interrupt pending state, and transition to the DI0: Device\_Idle\_SI state (see Figure 20).

**Transition DDMA0:DI1:** When an error is detected that causes the command to abort and nIEN is set to one, then the device shall set the appropriate error bits, enter the interrupt pending state, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

**Transition DDMA0:DDMA1:** When the device is ready transfer data for the command, the device shall transition to the DDMA1: Transfer\_Data state.

**DDMA1: Data\_Transfer State:** This state is entered when the device is ready to transfer data.

When in this state, BSY is cleared to zero, DRQ is set to one, and INTRQ is negated; or BSY is set to one, DRQ is cleared to zero, and INTRQ is negated. Data is transferred as described in Multiword DMA timing or Ultra DMA protocol.

**Transition DDMA1:DI0:** When the data transfer has completed or the device chooses to abort the command due to an error and nIEN is cleared to zero, then the device shall set error bits if appropriate, enter the interrupt pending state, and transition to the DI0: Device\_Idle\_SI state (see Figure 20).

**Transition DDMA2:DI1:** When the data transfer has completed or the device chooses to abort the command due to an error and nIEN is set to one, then the device shall set error bits if appropriate, enter the interrupt pending state, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

## 9.8 PACKET command protocol

This class includes:

- PACKET

There are two different protocols for the PACKET command **depending on the transfer mode requested.** Figure 30 and the text following the figure describes the host protocol for the PACKET command when non-data, PIO data-in, or PIO data-out is requested. Figure 31 and the text following the figure describes the device protocol for the PACKET command when non-data, PIO data-in, or PIO data-out is requested. Figure 32 and the text following the figure describes the host protocol for the PACKET command when DMA data transfer is requested. Figure 33 and the text following the figure describes the device protocol for the PACKET command when DMA data transfer is requested.

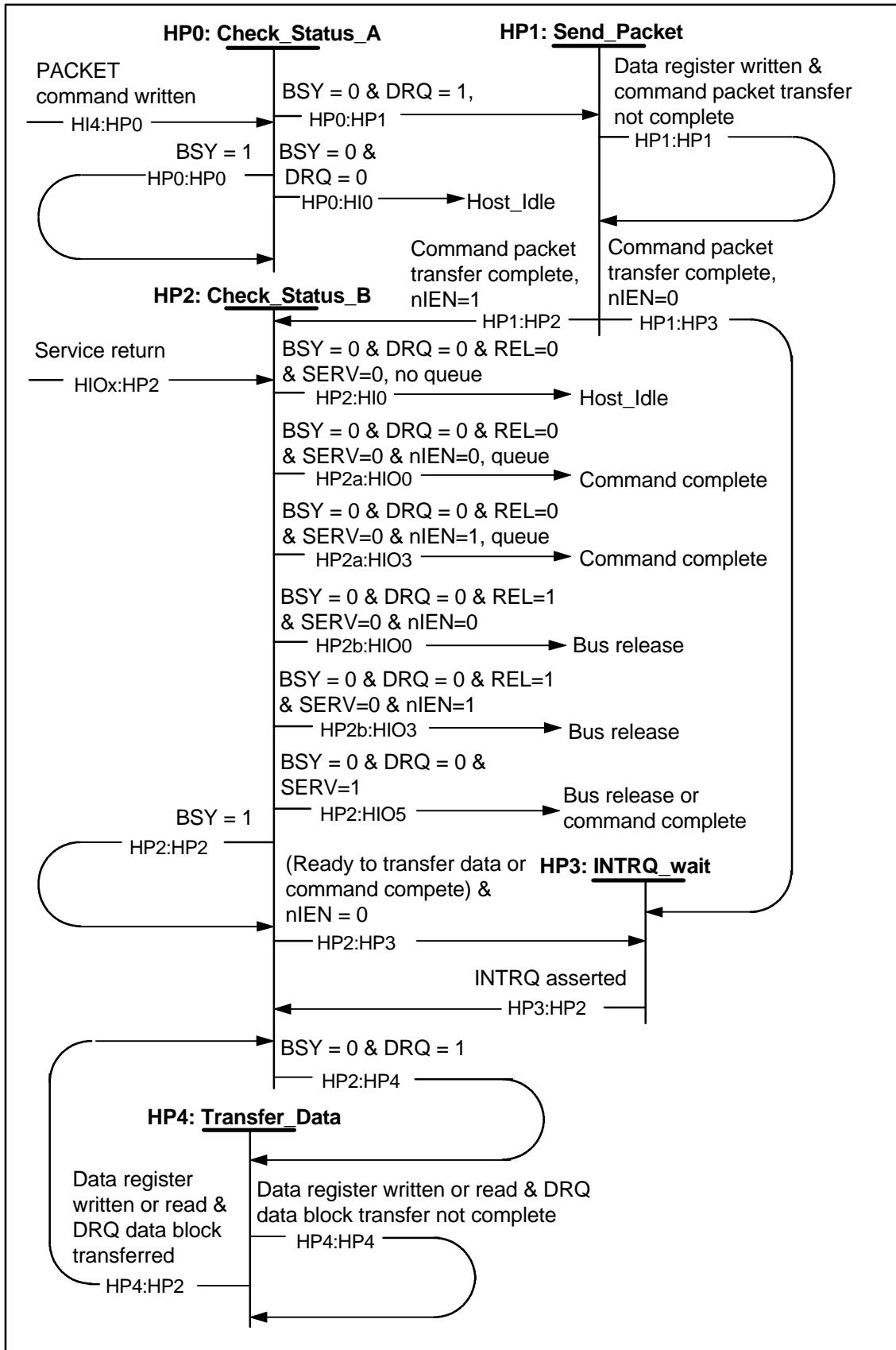


Figure 30 – Host PACKET non-data and PIO data command protocol

**HP0: Check\_Status\_A State:** This state is entered when the host has written a PACKET command to the device.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register.

**Transition HP0:HP0:**When BSY is set to one, the host shall transition to the HP0: Check\_Status\_A state.

**Transition HP0:HP1:** When BSY is cleared to zero and DRQ is set to one, then the host shall transition to the HP1: Send\_Packet state.

**Transition HP0:HI0:** When the BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, and SERV is cleared to zero, then the command is completed and the host shall transition to the HI0: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**HP1: Send\_Packet State:**This state is entered when BSY is cleared to zero, DRQ is set to one.

When in this state, the host shall write a byte of the command packet to the Data register.

**Transition HP1:HP1:** When the Data register has been written and the writing of the command packet is not completed, the host shall transition to the HP1: Send\_Packet state.

**Transition HP1:HP2:** When the Data register has been written, the writing of the command packet is completed, and nIEN is set to one, the host shall transition to the HP2: Check\_Status\_B state.

**Transition HP1:HP3:** When the Data register has been written, the writing of the command packet is completed, and nIEN is cleared to zero, the host shall transition to the HP3: INTRQ wait state.

**HP2: Check\_Status\_B State:** This state is entered when the host has written the command packet to the device, when INTRQ has been asserted indicating a data transfer is ready, when a DRQ data block has been transferred, or from a service return.

When in this state, the host shall read the device Status register. When entering this state from the HP1 or HP4 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

**Transition HP2:HP2:** When BSY is set to one, and DRQ is cleared to zero, the host shall transition to the HP2: Check\_Status\_B state.

**Transition HP2:HP3:** When the host is ready to transfer data or the command is complete, and nIEN is cleared to zero, then the host shall transition to the HP3: INTRQ\_Wait state.

**Transition HP2:HP4:** When BSY is cleared to zero and DRQ is set to one, then the host shall transition to the HP4: Transfer\_Data state.

**Transition HP2:HI0:** When the BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, and the device queue is empty, then the command is completed and the host shall transition to the HI0: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HP2a:HIO0:** When the BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero, and the device has a queue of released commands, then the command is completed and the host shall transition to the HIO0: Command completed state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HP2a:HIO3:** When the BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one, and the device has a queue of released commands, then the

command is completed and the host shall transition to the HIO3: Command completed state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transitions HP2b:HIO0:** When the BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is cleared to zero, then the host shall transition to the HIO0: INTRQ\_wait\_A state (see Figure 19). The bus has been released.

**Transitions HP2b:HIO3:** When the BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is set to one, then the host shall transition to the HIO3: Check\_status\_A state (see Figure 19). The bus has been released.

**Transitions HP2:HIO5:** When the BSY is cleared to zero, DRQ is cleared to zero, and SERV is set to one, then the host shall transition to the HIO5: Write\_SERVICE state (see Figure 19). The command is completed or the bus has been released, and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

**HP3: INTRQ\_Wait State:** This state is entered when the command packet has been transmitted, the host is ready to transfer data or when the command has completed, and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

**Transition HP3:HP2:**When INTRQ is asserted, the host shall transition to the HP2: Check\_Status\_B state.

**HP4: Transfer\_Data State:** This state is entered when the BSY is cleared to zero, DRQ is set to one, and C/D is cleared to zero.

When in this state, the host shall read the byte count then read or write the device Data register to transfer data.

**Transition HP4:HP2:** When the host has read or written the device Data register and the DRQ data block has been transferred, then the host shall transition to the HP2: Check\_Status\_B state.

**Transition HP4:HP4:** When the host has read or written the device status register and the DRQ data block transfer has not completed, then the host shall transition to the HP4: Transfer\_Data state.

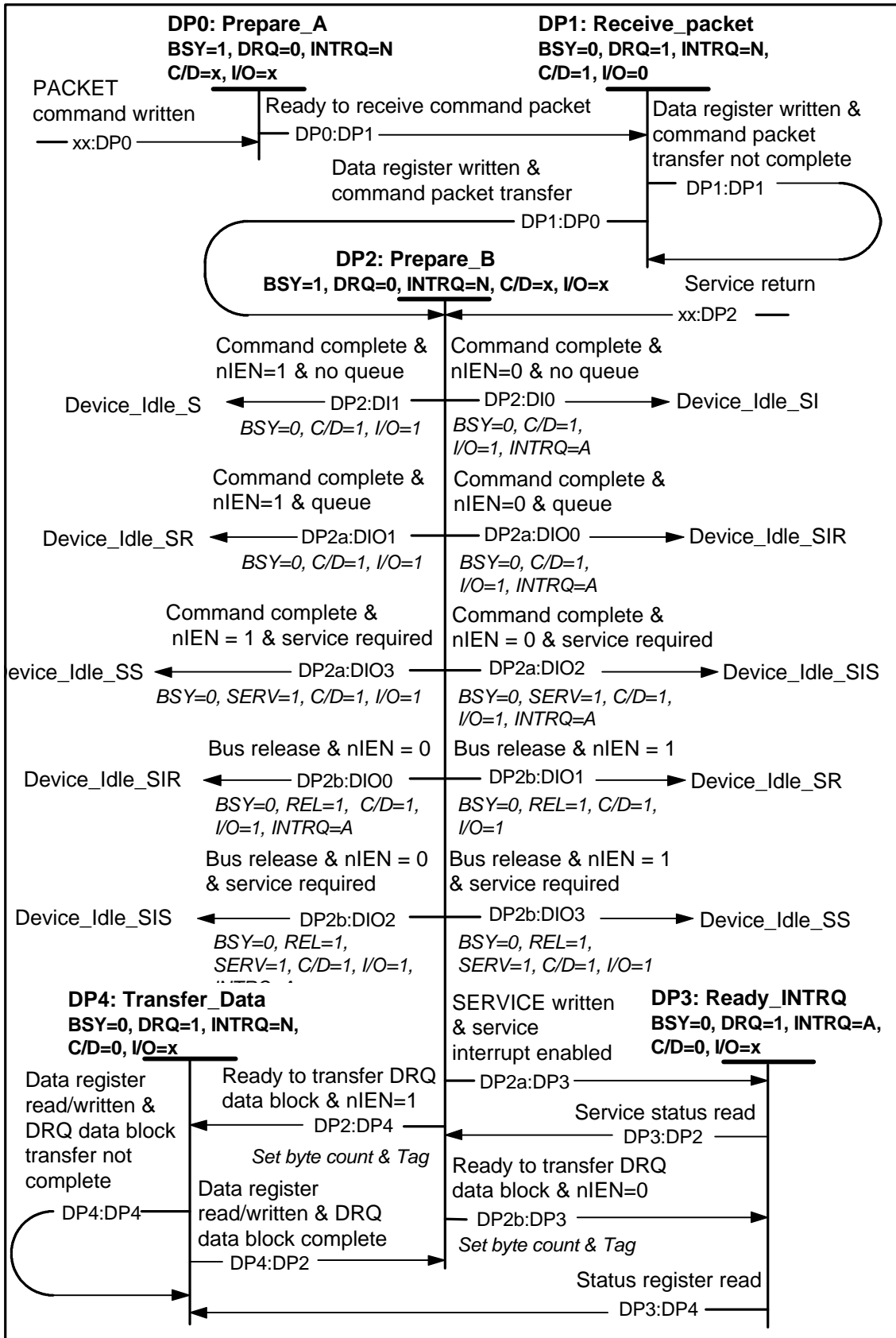


Figure 31 – Device PACKET non-data and PIO data command protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	x	x	v	v	v	R	R	R

**DP0: Prepare\_A State:** This state is entered when the device has a PACKET written to the Command register.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ within 400 ns of the receipt of the command and shall prepare to receive a command packet.

**Transition DP0:DP1:** When the device is ready to receive the command packet for a command, the device shall transition to the DP1: Receive\_Packet state.

**DP1: Receive\_Packet State:** This state is entered when the device is ready to receive the command packet.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is set to one, I/O is cleared to zero, and REL is cleared to zero. When in this state, the device Data register is written.

**Transition DP1:DP1:** If the Data register is written and the entire command packet has not been received, then the device shall transition to the DP1: Receive\_Packet state.

**Transition DP1:DP2:** When the Data register is written and the entire command packet has been received, then the device shall transition to the DP2: Prepare\_B state.

**DP2: Prepare\_B State:** This state is entered when the command packet has been received or from a Service return.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ. Non-data transfer commands shall be executed while in this state. For data transfer commands, the device shall check for errors, determine if the data transfer is complete, and if not, prepare to transfer the next DRQ data block.

If the command is overlapped and the release interrupt is enabled, the device shall bus release as soon as the command packet has been received.

**Transition DP2:DP4:** When the device is ready to transfer a DRQ data block for a command and nIEN is set to one, then the device shall set the command Tag and byte count, set the device internal interrupt pending, and transition to the DP4: Transfer\_Data state.

**Transition DP2b:DP3:** When the device is ready to transfer a DRQ data block for a command and nIEN is cleared to zero, then the device shall set the command Tag and byte count, set the device internal interrupt pending, and transition to the DP3: Ready\_INTRQ state.

**Transition DP2a:DP3:** When the service interrupt is enabled and the device has SERVICE written to the Command register, then the device shall set the command Tag and byte count and transition to the DP3: Ready\_INTRQ state.

**Transition DP2:DI0:** When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DI0: Device\_Idle\_SI state (see Figure 20).

**Transition DP2:DI1:** When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

**Transition DP2a:DIO0:** When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DIO0: Device\_Idle\_SIR state (see Figure 21).

**Transition DP2a:DIO1:** When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DIO1: Device\_Idle\_SR state (see Figure 21).

**Transition DP2a:DIO2:** When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero, and transition to the DIO2: Device\_Idle\_SIS state (see Figure 21).

**Transition DP2a:DIO3:** When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero, and transition to the DIO3: Device\_Idle\_SS state (see Figure 21).

**Transition DP2b:DIO0:** When the command is released and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero, and transition to the DIO0: Device\_Idle\_SIR state (see Figure 21).

**Transition DP2b:DIO1:** When the command is released and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero, and transition to the DIO1: Device\_Idle\_SR state (see Figure 21).

**Transition DP2b:DIO2:** When the **command** is released, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero, and transition to the DIO2: Device\_Idle\_SIS state (see Figure 21).

**Transition DP2b:DIO3:** When the command is released, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero, and transition to the DIO3: Device\_Idle\_SS state (see Figure 21).

**DP3: Ready\_INTRQ State:** This state is entered when the device is ready to transfer a DRQ data block and nIEN is cleared to zero. This state is entered to interrupt upon receipt of a SERVICE command when service interrupt is enabled.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is asserted, C/D is cleared to zero, and I/O is set to one for PIO data-out or cleared to zero for PIO data-in.

**Transition DP3:DP2:** When the Status register is read to respond to a service interrupt, the device shall transition to the DP2: Prepare\_B state.

**Transition DP3:DP4:** When the Status register is read when the device is ready to transfer data, then the device shall clear the device internal interrupt pending, negate INTRQ, and transition to the DP4: Data\_Transfer state.

**DP4: Data\_Transfer State:** This state is entered when the device is ready to transfer a DRQ data block.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is cleared to zero, I/O is set to one for PIO data-out or cleared to zero for PIO data-in, and a data word is read/written in the Data register.

**Transition DP4:DP4:** When the Data register is read/written and transfer of the DRQ data block has not completed, then the device shall transition to the DP4: Data\_Transfer state.

**Transition DP4:DP2:** When the Data register is read/written and the transfer of the current DRQ data block has completed, then the device shall transition to the DP2: Prepare\_B state.



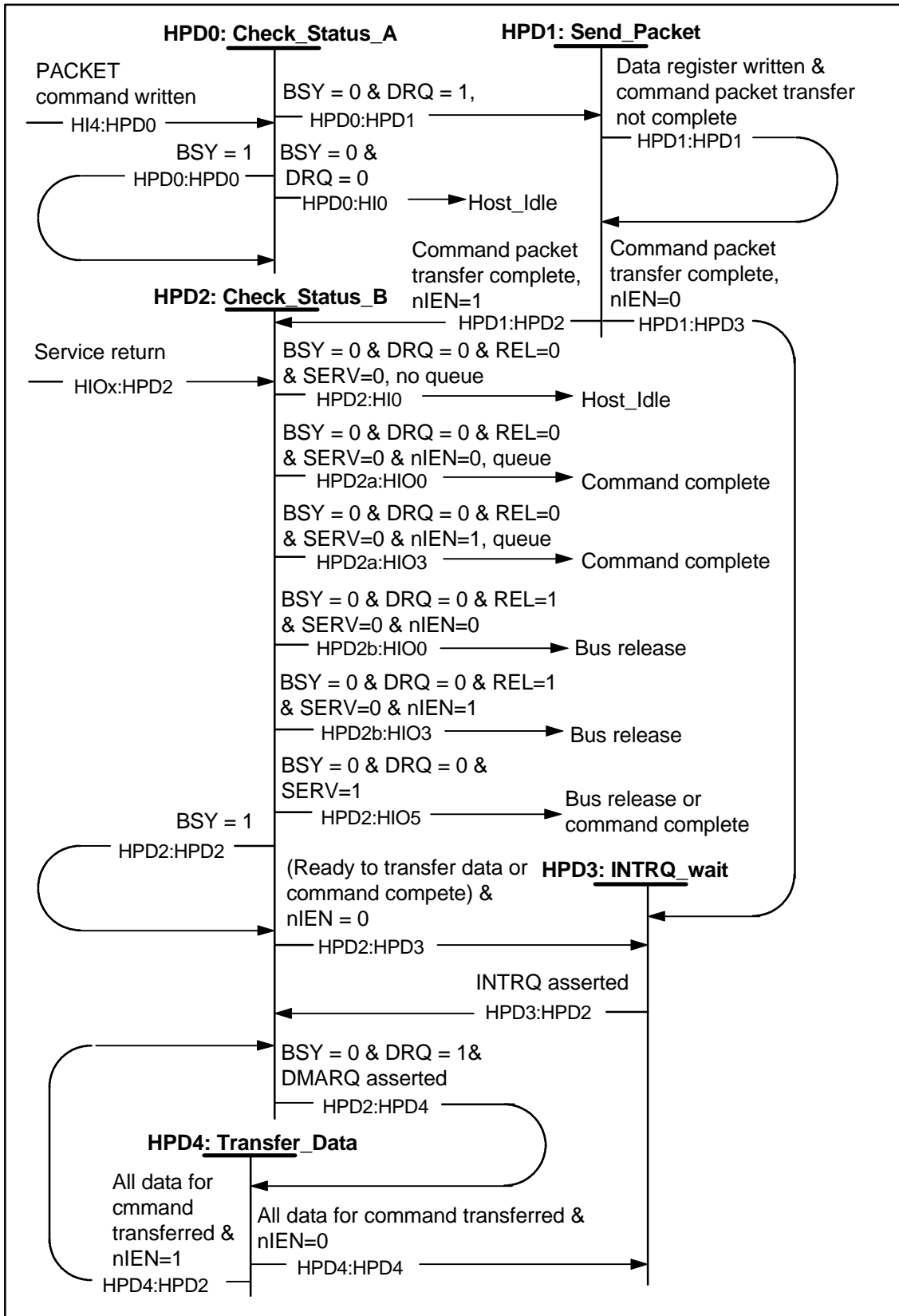


Figure 32 – Host PACKET DMA command protocol

**HPD0: Check\_Status\_A State:** This state is entered when the host has written a PACKET command to the device.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register.

**Transition HPD0:HPD0:** When BSY is set to one, the host shall transition to the HPD0: Check\_Status\_A state.

**Transition HPD0:HPD1:** When BSY is cleared to zero and DRQ is set to one, then the host shall transition to the HPD1: Send\_Packet state.

**Transition HPD0:HI0:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, and SERV is cleared to zero, then the command is completed and the host shall transition to the HI0: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**HPD1: Send\_Packet State:** This state is entered when BSY is cleared to zero, DRQ is set to one.

When in this state, the host shall write a byte of the command packet to the Data register.

**Transition HPD1:HPD1:** When the Data register has been written and the writing of the command packet is not completed, the host shall transition to the HPD1: Send\_Packet state.

**Transition HPD1:HPD2:** When the Data register has been written, the writing of the command packet is completed, and nIEN is set to one, the host shall transition to the HPD2: Check\_Status\_B state.

**Transition HPD1:HPD3:** When the Data register has been written, the writing of the command packet is completed, and nIEN is cleared to zero, the host shall transition to the HPD3: INTRQ wait state.

**HPD2: Check\_Status\_B State:** This state is entered when the host has written the command packet to the device, when INTRQ has been asserted indicating a data transfer is ready, when a DRQ data block has been transferred, or from a service return.

When in this state, the host shall read the device Status register. When entering this state from the HPD1 or HPD4 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

**Transition HPD2:HPD2:** When BSY is set to one, and DRQ is cleared to zero, the host shall transition to the HPD2: Check\_Status\_B state.

**Transition HPD2:HPD3:** When the host is ready to transfer data or the command is complete, and nIEN is cleared to zero, then the host shall transition to the HPD3: INTRQ\_Wait state.

**Transition HPD2:HPD4:** When BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted, then the host shall transition to the HPD4: Transfer\_Data state.

**Transition HPD2:HI0:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, and the device queue is empty, then the command is completed and the host shall transition to the HI0: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HPD2a:HIO0:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero, and the device has a queue of released commands, then the command is completed and the host shall transition to the HIO0: Command completed state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HPD2a:HIO3:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one, and the device has a queue of released commands, then the

command is completed and the host shall transition to the HIO3: Command completed state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transitions HPD2b:HIO0:** When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is cleared to zero, then the host shall transition to the HIO0: INTRQ\_wait\_A state (see Figure 19). The bus has been released.

**Transitions HPD2b:HIO3:** When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is set to one, then the host shall transition to the HIO3: Check\_status\_A state (see Figure 19). The bus has been released.

**Transitions HPD2:HIO5:** When BSY is cleared to zero, DRQ is cleared to zero, and SERV is set to one, then the host shall transition to the HIO5: Write\_SERVICE state (see Figure 19). The command is completed or the bus has been released, and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

**HPD3: INTRQ\_Wait State:** This state is entered when the command packet has been transmitted, the host is ready to transfer data or when the command has completed, and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

**Transition HPD3:HPD2:** When INTRQ is asserted, the host shall transition to the HPD2: Check\_Status\_B state.

**HPD4: Transfer\_Data State:** This state is entered when the BSY is cleared to zero, DRQ is set to one, andDMARQ is asserted.

When in this state, the host shall read or write the device Data port to transfer data. The host shall read the tag and if there has been a bus release initialize the DMA channel.

**Transition HPD4:HPD2:** When all data for the request has been transferred and nIEN is set to one, then the host shall transition to the HPD2: Check\_Status\_B state.

**Transition HPD4:HPD3:** When all data for the request has been transferred and nIEN is cleared to zero, then the host shall transition to the HPD3: INTRQ\_wait state.

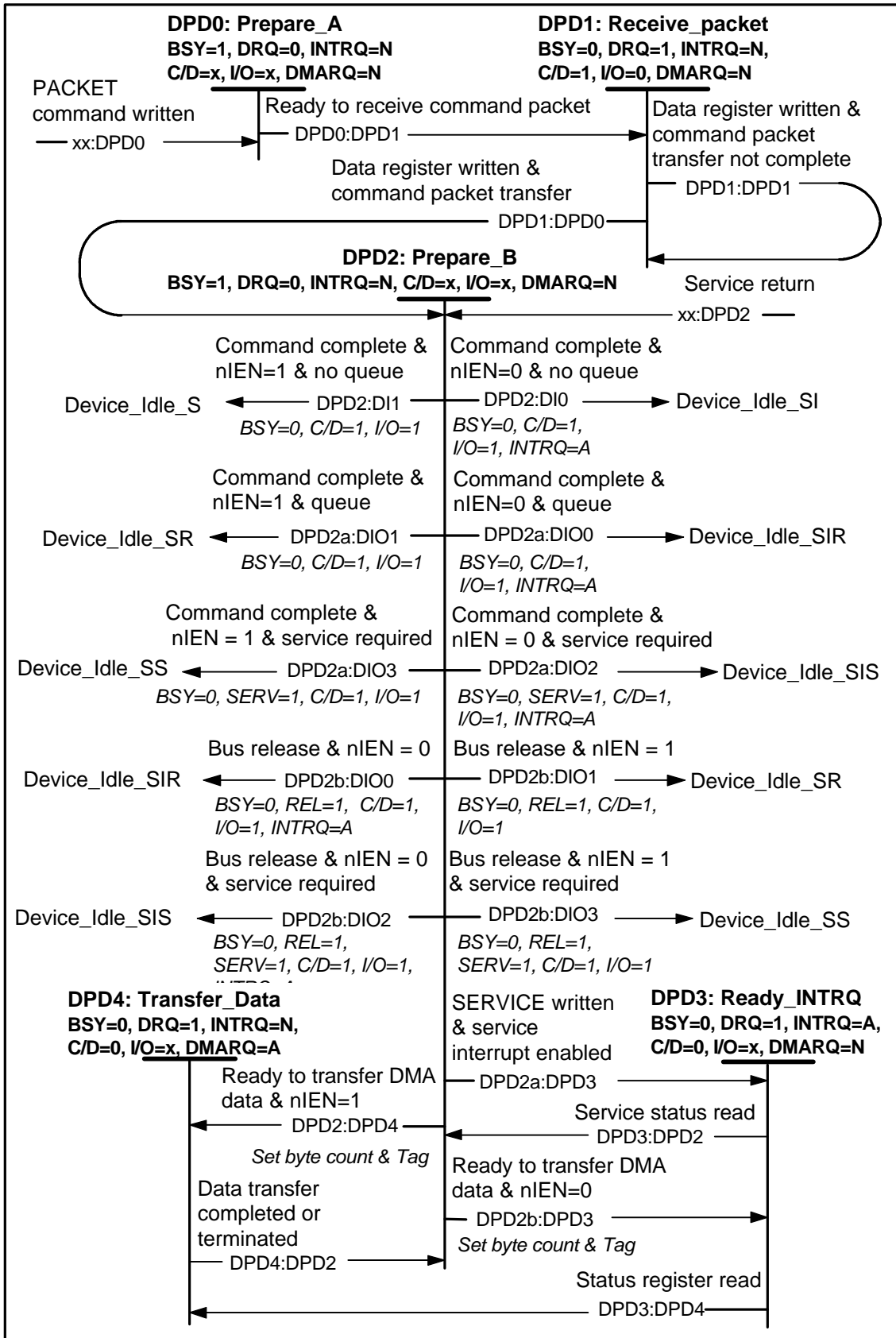


Figure 33 – Device PACKET DMA command protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	x	x	v	v	v	v	R	R

**DPD0: Prepare\_A State:** This state is entered when the device has a PACKET written to the Command register.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ within 400 ns of the receipt of the command and shall prepare to receive a command packet.

**Transition DPD0:DPD1:** When the device is ready to receive the command packet for a command, the device shall transition to the DPD1: Receive\_Packet state.

**DPD1: Receive\_Packet State:** This state is entered when the device is ready to receive the command packet.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is set to one, I/O is cleared to zero, and REL is cleared to zero. When in this state, the device Data register is written.

**Transition DPD1:DPD1:** If the Data register is written and the entire command packet has not been received, then the device shall transition to the DPD1: Receive\_Packet state.

**Transition DPD1:DPD2:** When the Data register is written and the entire command packet has been received, then the device shall transition to the DPD2: Prepare\_B state.

**DPD2: Prepare\_B State:** This state is entered when the command packet has been received or from a Service return.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ. The device shall check for errors, determine if the data transfer is complete, and if not, prepare to transfer the DMA data.

If the command is overlapped and the release interrupt is enabled, the device shall bus release as soon as the command packet has been received.

**Transition DPD2:DPD4:** When the device is ready to transfer DMA data for a command and nIEN is set to one, then the device shall set the command Tag and byte count, set the device internal interrupt pending, and transition to the DPD4: Transfer\_Data state.

**Transition DPD2b:DPD3:** When the device is ready to transfer DMA data for a command and nIEN is cleared to zero, then the device shall set the command Tag and byte count, set the device internal interrupt pending, and transition to the DPD3: Ready\_INTRQ state.

**Transition DPD2a:DPD3:** When the service interrupt is enabled and the device has SERVICE written to the Command register, then the device shall set the command Tag and byte count and transition to the DPD3: Ready\_INTRQ state.

**Transition DPD2:DI0:** When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DI0: Device\_Idle\_SI state (see Figure 20).

**Transition DPD2:DI1:** When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DI1: Device\_Idle\_S state (see Figure 20).

**Transition DPD2a:DI00:** When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is cleared to zero,

then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DIO0: Device\_Idle\_SIR state (see Figure 21).

**Transition DPD2a:DIO1:** When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is set to one, then the device shall, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and transition to the DIO1: Device\_Idle\_SR state (see Figure 21).

**Transition DPD2a:DIO2:** When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero, and transition to the DIO2: Device\_Idle\_SIS state (see Figure 21).

**Transition DPD2a:DIO3:** When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero, and transition to the DIO3: Device\_Idle\_SS state (see Figure 21).

**Transition DPD2b:DIO0:** When the command is released and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero, and transition to the DIO0: Device\_Idle\_SIR state (see Figure 21).

**Transition DPD2b:DIO1:** When the command is released and nIEN is set to one, then the device shall, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero, and transition to the DIO1: Device\_Idle\_SR state (see Figure 21).

**Transition DPD2b:DIO2:** When the is released, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero, and transition to the DIO2: Device\_Idle\_SIS state (see Figure 21).

**Transition DPD2b:DIO3:** When the command is released, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero, and transition to the DIO3: Device\_Idle\_SS state (see Figure 21).

**DPD3: Ready\_INTRQ State:** This state is entered when the device is ready to transfer DMA data and nIEN is cleared to zero. This state is entered to interrupt upon receipt of a SERVICE command when service interrupt is enabled.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is asserted, C/D is cleared to zero, and I/O is set to one for PIO data-out or cleared to zero for PIO data-in.

**Transition DPD3:DPD2:** When the Status register is read to respond to a service interrupt, the device shall transition to the DPD2: Prepare\_B state.

**Transition DPD3:DPD4:** When the Status register is read and the device is ready to transfer data, then the device shall clear the device internal interrupt pending, negate INTRQ, and transition to the DPD4: Data\_Transfer state.

**DPD4: Data\_Transfer State:** This state is entered when the device is ready to transfer DMA data.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is cleared to zero, I/O is set to one for data-out or cleared to zero for data-in, DMARQ is asserted, and data is transferred as described in Multiword DMA timing or Ultra DMA protocol.

**Transition DPD4:DPD2:** When the data transfer has been completed, then the device shall transition to the DPD2: Prepare\_B state.

## 9.9 READ/WRITE DMA QUEUED command protocol

This class includes:

- READ DMA QUEUED
- WRITE DMA QUEUED

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host or from the device to the host using DMA transfer. This command may bus release before transferring data. The host shall initialize the DMA channel prior to transferring data. Figure 34 and the text following the figure describes the host states. Figure 35 and the text following the figure describes the device states.

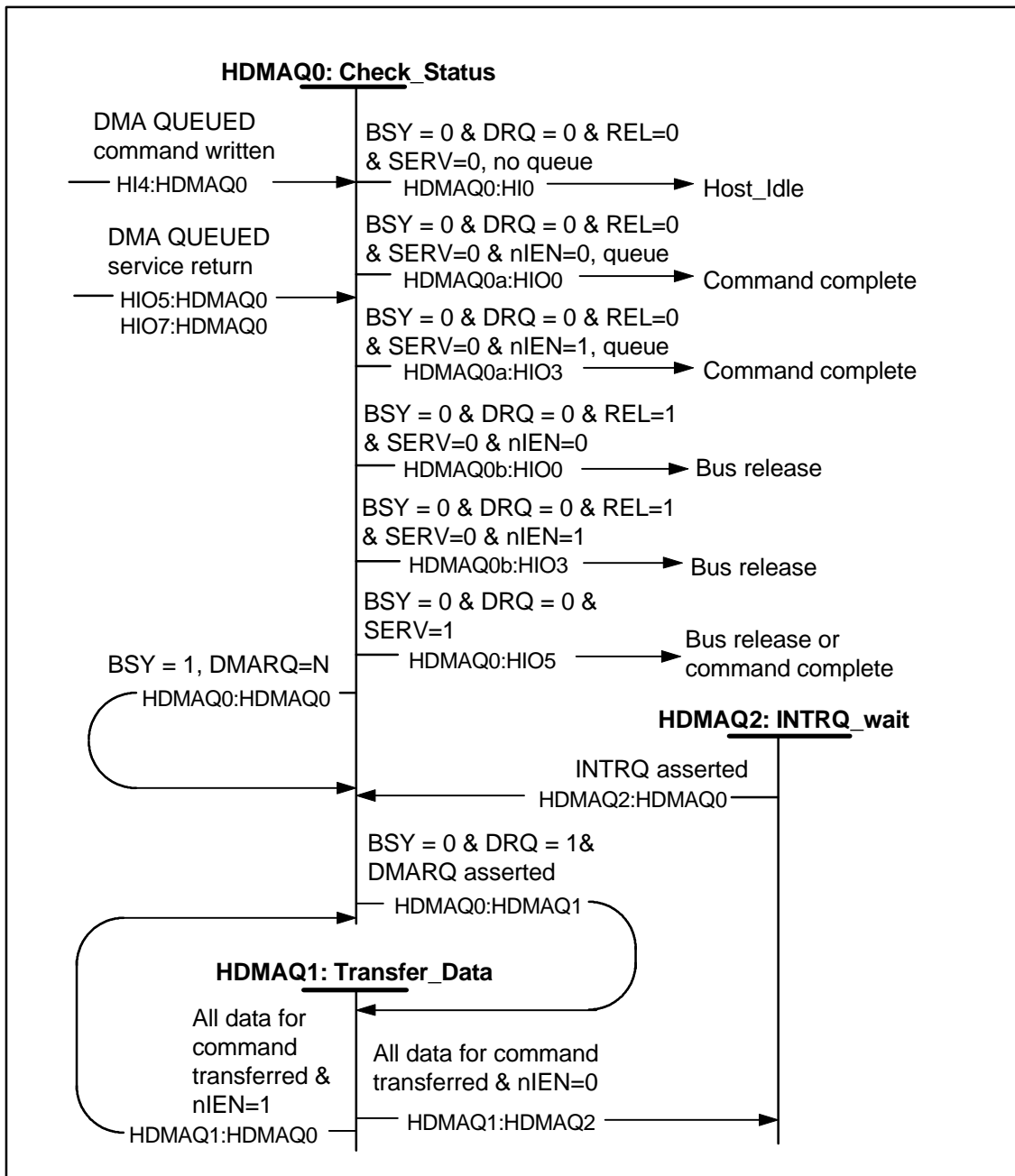


Figure 34 – Host DMA QUEUED state

**HDMAQ0: Check\_Status State:** This state is entered when the host has written a READ/WRITE DMA QUEUED command to the device, when all data for the command has been transferred and nIEN is set to one, or when all data for the command has been transferred, nIEN is cleared to zero, and INTRQ has been asserted. It is also entered when the SERVICE command has been written to continue execution of a bus released command.

When in this state, the host shall read the device Status register. When entering this state from the HI4, HIO5, or HIO7 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HDMAQ1 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

**Transition HDMAQ0:HDMAQ0:** When BSY is set to one and DMARQ is negated, the host shall transition to the HDMAQ0: Check\_Status state.



**Transition HDMAQ0:HDMAQ1:** When BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted, then the host shall transition to the HDMAQ1: Transfer\_Data state.

**Transition HDMAQ0:HIO:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, and the device queue is empty, then the command is completed and the host shall transition to the HIO: Host\_Idle state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HDMAQ0a:HIO0:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero, and the device has a queue of released commands, then the command is completed and the host shall transition to the HIO0: Command completed state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transition HDMAQ0a:HIO3:** When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one, and the device has a queue of released commands, then the command is completed and the host shall transition to the HIO3: Command completed state (see Figure 18). If an error is reported, the host shall perform appropriate error recovery.

**Transitions HDMAQ0b:HIO0:** When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is cleared to zero, then the host shall transition to the HIO0: INTRQ\_wait\_A state (see Figure 19). The bus has been released.

**Transitions HDMAQ0b:HIO3:** When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is set to one, then the host shall transition to the HIO3: Check\_status\_A state (see Figure 19). The bus has been released.

**Transitions HDMAQ0:HIO5:** When BSY is cleared to zero, DRQ is cleared to zero, and SERV is set to one, then the host shall transition to the HIO5: Write\_SERVICE state (see Figure 19). The command is completed or the bus has been released, and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

**HDMAQ1: Transfer\_Data State:** This state is entered when BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted.

When in this state, the host shall read or write the device Data port to transfer data. The host shall read the tag and if the bus has been released initialize the DMA channel.

**Transition HDMAQ1:HDMAQ0:** When all data for the request has been transferred and nIEN is set to one, then the host shall transition to the HDMAQ0: Check\_Status state.

**Transition HDMAQ1:HDMAQ2:** When all data for the request has been transferred and nIEN is cleared to zero, then the host shall transition to the HDMAQ2: INTRQ\_wait state.

**HDMAQ2: INTRQ\_Wait State:** This state is entered when the command has completed, and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

**Transition HDMAQ2:HDMAQ0:** When INTRQ is asserted, the host shall transition to the HDMAQ0: Check\_Status state.

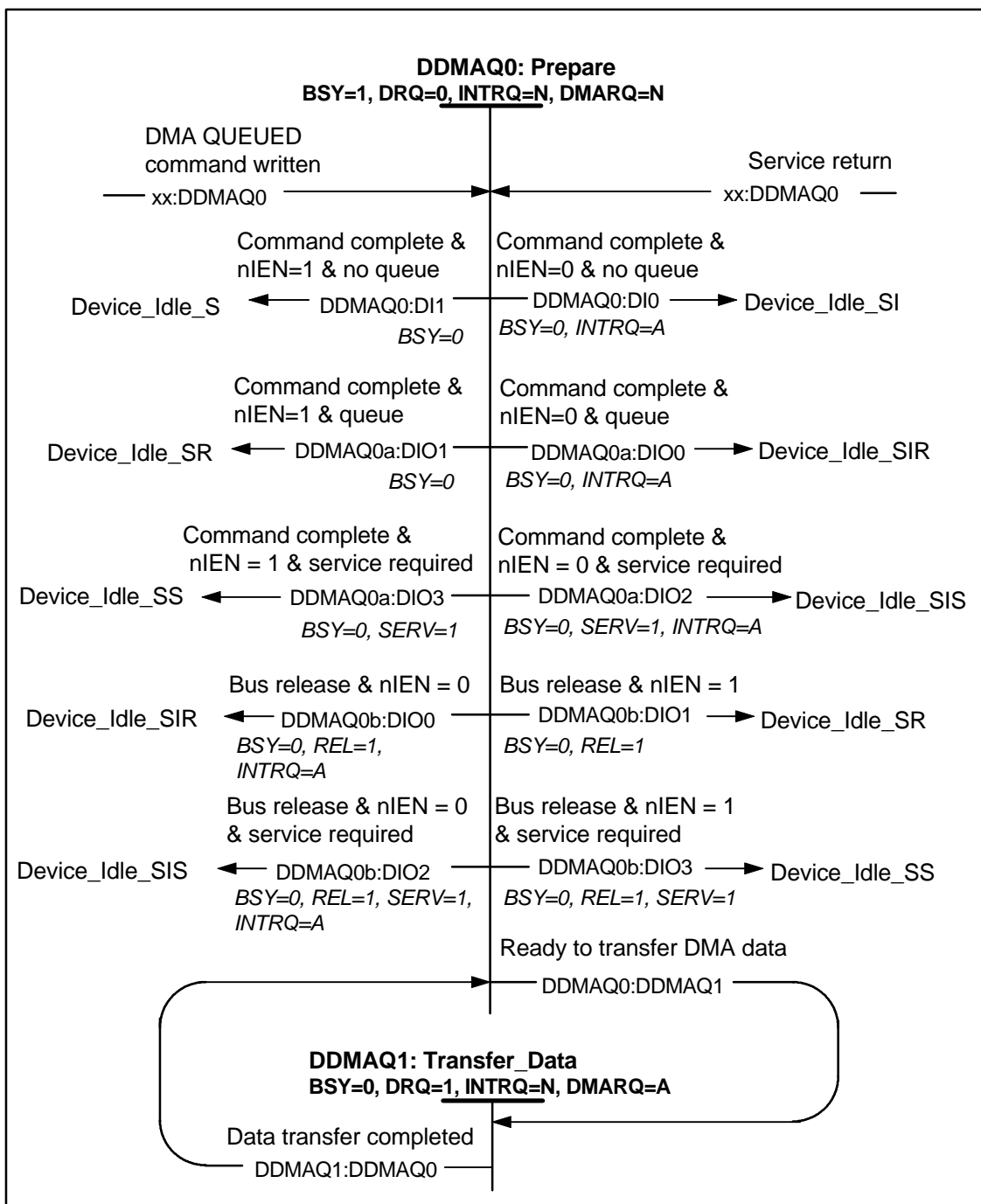


Figure 35 – Device DMA QUEUED command protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	x	x	x	x	v	v	R	R

**DDMAQ0: Prepare State:** This state is entered when the device has a READ/WRITE DMA QUEUED or SERVICE command is written to the Command register, when the data has been transferred, or when the command has completed.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ. If commands are queued, the Tag for the command to be serviced shall be placed into the Sector Count register.

**Transition DDMAQ0:DDMAQ1:** When the device is ready to transfer the data for a command, then the device shall transition to the DDMAQ1: Transfer\_Data state.

**Transition DDMAQ0:DIO:** When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, clear BSY to zero, and transition to the DIO: Device\_Idle\_SI state (see Figure 20).

**Transition DDMAQ0:DIO1:** When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is set to one, then the device shall set appropriate error bits, clear BSY to zero, and transition to the DIO1: Device\_Idle\_S state (see Figure 20).

**Transition DDMAQ0a:DIO0:** When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, clear BSY to zero, and transition to the DIO0: Device\_Idle\_SIR state (see Figure 21).

**Transition DDMAQ0a:DIO1:** When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is set to one, then the device shall, set appropriate error bits, clear BSY to zero, and transition to the DIO1: Device\_Idle\_SR state (see Figure 21).

**Transition DDMAQ0a:DIO2:** When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set SERV to one, clear BSY to zero, and transition to the DIO2: Device\_Idle\_SIS state (see Figure 21).

**Transition DDMAQ0a:DIO3:** When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set SERV to one, clear BSY to zero, and transition to the DIO3: Device\_Idle\_SS state (see Figure 21).

**Transition DDMAQ0b:DIO0:** When the command is released and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set REL to one, clear BSY to zero, and transition to the DIO0: Device\_Idle\_SIR state (see Figure 21).

**Transition DDMAQ0b:DIO1:** When the command is released and nIEN is set to one, then the device shall, set appropriate error bits, set REL to one, clear BSY to zero, and transition to the DIO1: Device\_Idle\_SR state (see Figure 21).

**Transition DDMAQ0b:DIO2:** When the is released, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the device internal interrupt pending, set appropriate error bits, set REL to one, set SERV to one, clear BSY to zero, and transition to the DIO2: Device\_Idle\_SIS state (see Figure 21).

**Transition DDMAQ0b:DIO3:** When the command is released, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set REL to one, set SERV to one, clear BSY to zero, and transition to the DIO3: Device\_Idle\_SS state (see Figure 21).

**DDMAQ1: Data\_Transfer State:** This state is entered when the device is ready to transfer DMA data.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, DMARQ is asserted, and data is transferred as described in Multiword DMA timing or Ultra DMA protocol.

**Transition DDMAQ1:DDMAQ0:** When the data transfer has been completed, then the device shall transition to the DDMAQ0: Prepare state.

## 9.10 EXECUTE DEVICE DIAGNOSTIC command protocol

This class includes:

- EXECUTE DEVICE DIAGNOSTIC

If the host asserts RESET- before devices have completed executing their EXECUTE DEVICE DIAGNOSTIC protocol, then the devices shall start executing the power on or hardware reset protocol from the beginning.

If the host sets SRST to one in the Device Control register before the devices have completed execution of their EXECUTE DEVICE DIAGNOSTIC protocol, then the devices shall start executing their software reset protocol from the beginning.

Figure 36 and the text following the figure describe the EXECUTE DEVICE DIAGNOSTIC protocol for the host. Figure 37 and the text following the figure describe the EXECUTE DEVICE DIAGNOSTIC protocol for Device 0. Figure 38 and the text following the figure describe the EXECUTE DEVICE DIAGNOSTIC protocol for Device 1.

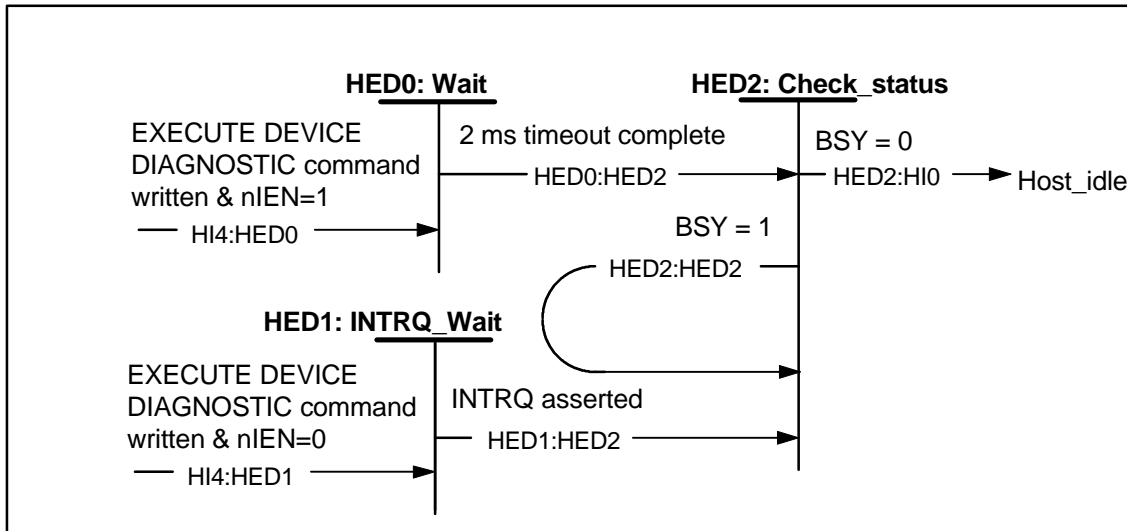


Figure 36 – Host EXECUTE DEVICE DIAGNOSTIC protocol

**HED0: Wait State:** This state is entered when the host has written the EXECUTE DEVICE DIAGNOSTIC command to the devices and nIEN is set to one.

The host shall remain in this state for at least 2 ms.

**Transition HED0:HED1:** When at least 2 ms has elapsed since the command was written, the host shall transition to the HED1: Check\_status state.

**HED1: INTRQ wait:** This state is entered when the host has written the EXECUTE DEVICE DIAGNOSTIC command to the devices and nIEN is cleared to zero.

When in this state the host shall wait for INTRQ to be asserted.

**Transition HED1:HED2:** When INTRQ is asserted, the host shall transition to the HED2: Check\_status state.

**HED2: Check\_status State:** This state is entered when at least 2 ms since the command was written or INTRQ has been asserted.

When in this state, the host shall read the Status or Alternate Status register.

**Transition HED2:HED2:**When BSY is set to one, the host shall transition to the HED1: Check\_status state.

**Transition HED2:HI0:** When BSY is cleared to zero, the host shall check the results of the command (see 9.16) and transition to the HI0: Host\_idle state (see Figure 18).

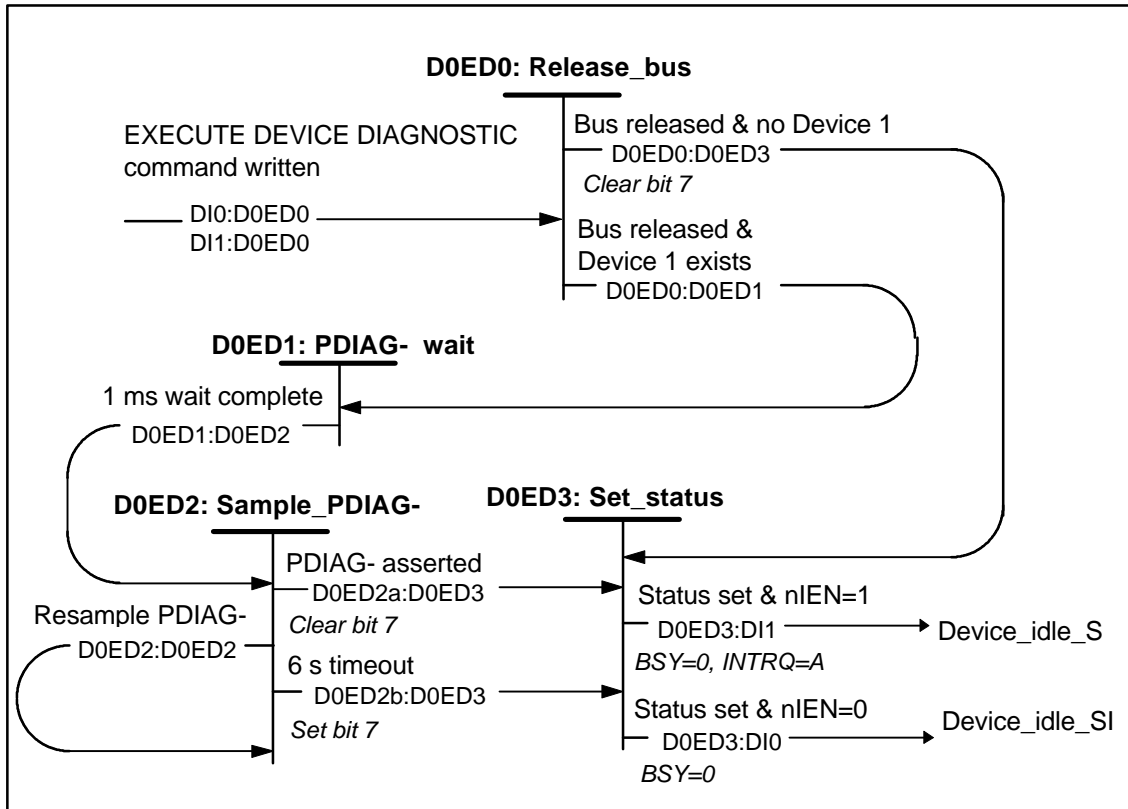


Figure 37 – Device 0 EXECUTE DEVICE DIAGNOSTIC protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	N	R	R	R

**D0ED0: Release\_bus State:** This state is entered when the EXECUTE DEVICE DIAGNOSTIC command has been written to Device 0.

When in this state, the device shall release PDIAG-, INTRQ, IORDY, DMARQ, and DD(15:0) and shall set BSY to one and clear DEV to zero within 400 ns after entering this state.

The device should begin performing the self-diagnostic testing.

**Transition D0ED0:D0ED1:** When the bus has been released, BSY set to one, and the assertion of DASP- by Device 1 was detected during the most recent power on or hardware reset, then the device shall transition to the D0ED1: PDIAG-\_wait state.

**Transition D0ED0:D0ED3:** When the bus has been released, BSY set to one, and the assertion of DASP- by Device 1 was not detected during the most recent power on or hardware reset, then the device shall clear bit 7 in the Error register and transition to the D0ED3: Set\_status state.

**D0ED1: PDIAG-\_wait State:** This state is entered when the bus has been released, BSY set to one, and Device 1 exists.

The device shall remain in this state until least 1 ms has elapsed since the command was written.

**Transition D0ED1:D0ED2:** When at least 1 ms has elapsed since the command was written, the device shall transition to the D0ED2: Sample\_PDIAG- state.

**D0ED2: Sample\_PDIAG- State:** This state is entered when at least 1 ms has elapsed since the command was written.

When in this state, the device shall sample the PDIAG- signal.

**Transition D0ED2:D0ED3:** When the sample indicates that PDIAG- is asserted, the device shall clear bit 7 in the Error register and transition to the D0ED3: Set\_status state.

**Transition D0ED2:D0ED2:** When the sample indicates that PDIAG- is not asserted and less than 6 s have elapsed since the command was written, then the device shall transition to the D0ED2: Sample\_PDIAG- state.

**Transition D0ED2:D0ED3:** When the sample indicates that DASP- is not asserted and 6 s have elapsed since the command was written, then the device shall set bit 7 in the Error register and transition to the D0ED3: Set\_status state.

**Transition D0ED3:D0ED5:** When bit 7 in the Error register has been cleared to zero, the device shall transition to the D0ED5: Set\_status state.

**D0ED3: Set\_status State:** This state is entered when Bit 7 in the Error register has been set or cleared.

When in this state the device shall complete the self-diagnostic testing begun in the Release bus state if not already completed.

Results of the self-diagnostic testing shall be placed in bits 6-0 of the Error register (see Table 18). The device shall set the signature values (see 9.12). The contents of the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2, and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

**Transition D0ED3:DI1:** When hardware initialization and self-diagnostic testing is completed, the status has been set, and nIEN is set to one, then the device shall clear BSY to zero, and transition to the DI1: Device\_idle\_S state (see Figure 20).

**Transition D0ED3:DI0:** When hardware initialization and self-diagnostic testing is completed, the status has been set, and nIEN is cleared to zero, then the device shall clear BSY to zero, assert INTRQ, and transition to the DI0: Device\_idle\_SI state (see Figure 20).

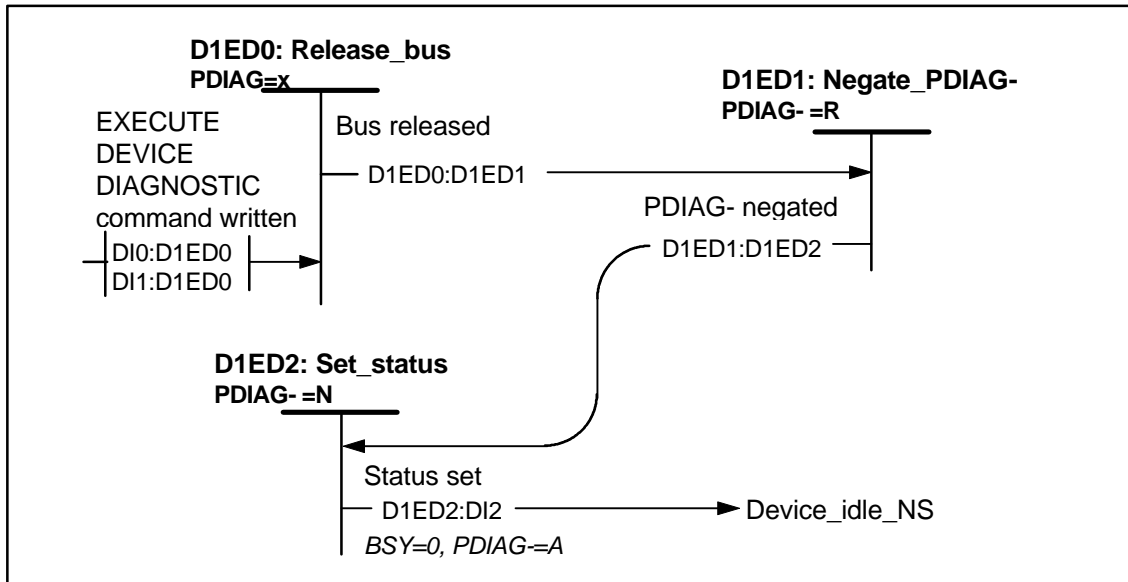


Figure 38 – Device 1 EXECUTE DEVICE DIAGNOSTIC command protocol

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	N	R	v	R

**D1ED0: Release\_bus State:** This state is entered when the EXECUTE DEVICE DIAGNOSTIC command is written to Device 1.

When in this state, the device shall release INTRQ, IORDY, DMARQ, and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one and clear DEV to zero within 400 ns after entering this state.

The device should begin performing the self-diagnostic testing.

**Transition D1ED0:D1ED1:** When the bus has been released and BSY set to one, then the device shall transition to the D1ED1: Negate\_PDIAG- state.

**D1ED1: Negate\_PDIAG- State:** This state is entered when the bus has been released and BSY set to one.

When in this state, the device shall negate PDIAG- within less than 1 ms of the receipt of the EXECUTE DEVICE DIAGNOSTIC command.

**Transition D1ED1:D1ED2:** When PDIAG- has been negated, the device shall transition to the D1ED2: Set\_status state.

**D1ED2: Set\_status State:** This state is entered when the device has negated PDIAG-.

When in this state the device shall complete the hardware initialization and self-diagnostic testing begun in the Release bus state if not already completed. Results of the self-diagnostic testing shall be placed in the Error register (see Table 18). If the device passed the self-diagnostics, the device shall assert PDIAG-.

The device shall set the signature values (see 9.12). The effect on the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2, and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

**Transition D1ED2:DI2:** When hardware initialization and self-diagnostic testing is completed and the status has been set, then the device shall clear BSY to zero, assert PDIAG- if diagnostics were passed, and transition to the DI2: Device\_idle\_NS state (see Figure 20).

### 9.11 DEVICE RESET command protocol

This class includes:

- DEVICE RESET

If the host asserts RESET- before the device has completed executing a DEVICE RESET command, then the device shall start executing the hardware reset protocol from the beginning. If the host sets the SRST bit to one in the Device Control register before the device has completed executing a DEVICE RESET command, the device shall start executing the software reset protocol from the beginning.

The host should not issue a DEVICE RESET command while a DEVICE RESET command is in progress. If the host issues a DEVICE RESET command while a DEVICE RESET command is in progress, the results are indeterminant.

Figure 39 and the text following the figure describe the DEVICE RESET command protocol for the host. Figure 40 and the text following the figure describe the DEVICE RESET command protocol for the device.

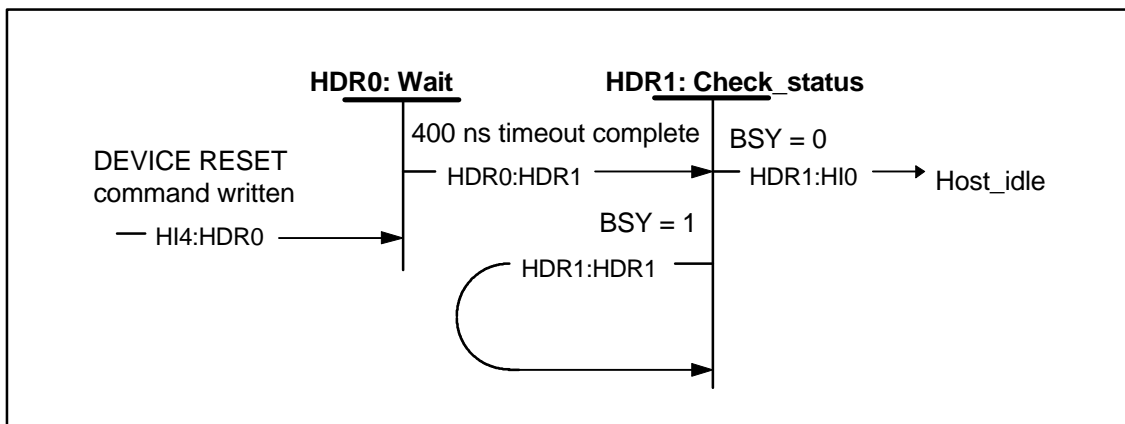


Figure 39 – Host DEVICE RESET command protocol

**HDR0: Wait State:** This state is entered when the host has written the DEVICE RESET command to the device.

The host shall remain in this state for at least 400 ns.

**Transition HDR0:HDR1:** When at least 400 ns has elapsed since the command was written, the host shall transition to the HDR1: Check\_status state.

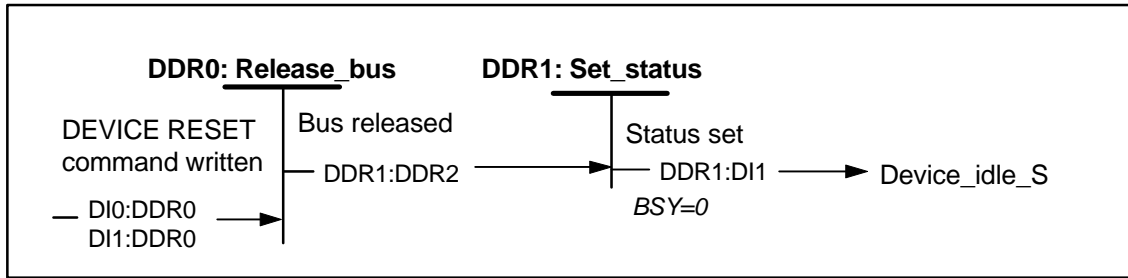
**HDR1: Check\_status State:** This state is entered when at least 400 ns has elapsed since the command was written.

When in this state the host shall read the Status register.

**Transition HDR1:HDR1:**When BSY is set to one, the host shall transition to the HDR1: Check\_status state.



**Transition HDR1:HI0:** When BSY is cleared to zero, the host shall transition to the HI0: Host\_idle state (see Figure 18). If status indicates that an error has occurred, the host shall take appropriate action.



**Figure 40 – Device DEVICE RESET command protocol**

BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	N	R	R	R

**DDR0: Release\_bus State:**This state is entered when the DEVICE RESET command is written.

When in this state, the device shall release INTRQ, IORDY, DMARQ, and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

**Transition DDR0:DDR1:** When the bus has been released and BSY set to one, the device shall transition to the DDR1: Set\_status state.

**DDR1: Set\_status State:** This state is entered when the device has released the bus and set BSY to one.

When in this state the device should stop execution of any uncompleted command. The device should end background activity (e.g., immediate commands, see MMC and MMC-2).

The device should not revert to the default condition. If the device reverts to the default condition, the device shall report a Unit Attention to a subsequent PACKET command. MODE SELECT conditions shall not be altered.

The device shall set the signature values (see 9.12). The content of the Features register is undefined.

The device shall clear bit 7 in the ERROR register to zero. The device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero.

**Transition DDR1:DI1:** When the status has been set, the device shall clear BSY to zero and transition to the DI1: Device\_idle\_S state (see Figure 20).

### 9.12 Signature and persistence

A device not implementing the PACKET command feature set shall place the signature in the Command Block registers listed below for power on reset, hardware reset, software reset, and the EXECUTE DEVICE DIAGNOSTIC command.

If the device does not implement the PACKET command feature set, the signature shall be:

Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	00h

A device implementing the PACKET command feature set shall place the signature in the Command Block registers listed below for power on reset, hardware reset, software reset, the EXECUTE DEVICE DIAGNOSTIC command, and the DEVICE RESET command. The DEVICE RESET command shall not change the value of the DEV bit when writing the signature into the Device/Head register for a device implementing the PACKET command feature set. If the device implements the PACKET command feature set, the signature is also written in the registers for the IDENTIFY DEVICE and READ SECTOR(S) commands.

If the device implements the PACKET command feature set, the signature shall be:

Sector Count	01h
Sector Number	01h
Cylinder Low	14h
Cylinder High	EBh
Device/Head	00h or 10h

If the PACKET command feature set is implemented by a device, then the signature values written by the device in the Command Block registers following power on reset, hardware reset, software reset, or the DEVICE RESET command shall not be changed by the device until the device receives a command that sets DRDY to one. These commands are a PACKET command or an IDENTIFY PACKET DEVICE command. Writes by the host to the Command Block registers that contain the signature values shall overwrite the signature values and invalidate the signature.

## 9.13 Ultra DMA data-in commands

### 9.13.1 Initiating an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.1 and 10.2.4.2 for specific timing requirements):

- a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
- b) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
- c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
- d) The host shall negate HDMARDY-.
- e) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.
- f) Steps (c), (d), and (e) shall have occurred at least  $t_{ACK}$  before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
- g) The host shall release DD(15:0) within  $t_{AZ}$  after asserting DMACK-.
- h) The device may assert DSTROBE  $t_{ZIORDY}$  after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated DMACK- at the end of an Ultra DMA burst.
- i) The host shall negate STOP and assert HDMARDY- within  $t_{ENV}$  after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
- j) The device shall drive DD(15:0) no sooner than  $t_{ZAD}$  after the host has asserted DMACK-, negated STOP, and asserted HDMARDY-.
- k) The device shall drive the first word of the data transfer onto DD(15:0). This step may occur when the device first drives DD(15:0) in step (j).
- l) To transfer the first word of data the device shall negate DSTROBE within  $t_{FS}$  after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than  $t_{DVS}$  after driving the first word of data onto DD(15:0).

### 9.13.2 The data-in transfer

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.3 and 10.2.4.2):

- a) The device shall drive a data word onto DD(15:0).
- b) The device shall generate a DSTROBE edge to latch the new word no sooner than  $t_{DVS}$  after changing the state of DD(15:0). The device shall generate a DSTROBE edge no more frequently than  $t_{CYC}$  for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than  $2t_{CYC}$  for the selected Ultra DMA mode.
- c) The device shall not change the state of DD(15:0) until at least  $t_{DVH}$  after generating a DSTROBE edge to latch the data.
- d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

### 9.13.3 Pausing an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.4 and 10.2.4.2 for specific timing requirements).

#### 9.13.3.1 Device pausing an Ultra DMA data-in burst

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.
- c) NOTE – The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate HDMARDY- and wait  $t_{RP}$  before asserting STOP.
- d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

#### 9.13.3.2 Host pausing an Ultra DMA data-in burst

- a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall pause an Ultra DMA burst by negating HDMARDY-.
- c) The device shall stop generating DSTROBE edges within  $t_{RFS}$  of the host negating HDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the host negates HDMARDY- within  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words; or, if the host negates HDMARDY- greater than  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the device.
- e) The host shall resume an Ultra DMA burst by asserting HDMARDY-.

### 9.13.4 Terminating an Ultra DMA data-in burst

#### 9.13.4.1 Device terminating an Ultra DMA data-in burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated.

The device shall terminate an Ultra DMA burst before command completion.

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.5 and 10.2.4.2 for specific timing requirements):

- a) The device shall initiate termination of an Ultra DMA burst by not generating DSTROBE edges.
- b) The device shall negate DMARQ no sooner than  $t_{SS}$  after generating the last DSTROBE edge. The device shall not assert DMARQ again until after DMACK- has been negated.
- c) The device shall release DD(15:0) no later than  $t_{AZ}$  after negating DMARQ.
- d) The host shall assert STOP within  $t_{LI}$  after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

- e) The host shall negate HDMARDY- within  $t_{LI}$  after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated. Steps (d) and (e) may occur at the same time.
- f) The host shall drive DD(15:0) no sooner than  $t_{ZAH}$  after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation (see 9.15);
- g) If DSTROBE is negated, the device shall assert DSTROBE within  $t_{LI}$  after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (f), the host shall place the result of the host CRC calculation on DD(15:0) (see 9.15).
- i) The host shall negate DMACK- no sooner than  $t_{MLI}$  after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than  $t_{DVS}$  after the host places the result of the host CRC calculation on DD(15:0).
- j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command the device shall report the first error that occurred (see 9.15).
- l) The device shall release DSTROBE within  $t_{IORDYZ}$  after the host negates DMACK-.
- m) The host shall not negate STOP nor assert HDMARDY- until at least  $t_{ACK}$  after negating DMACK-.
- n) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least  $t_{ACK}$  after negating DMACK.

#### 9.13.4.2 Host terminating an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.6 and 10.2.4.2 for specific timing requirements):

- a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall initiate Ultra DMA burst termination by negating HDMARDY-. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated.
- c) The device shall stop generating DSTROBE edges within  $t_{RFS}$  of the host negating HDMARDY-.
- d) **When operating in Ultra DMA modes 2, 1, or 0: If the host negates HDMARDY- within  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words; or, if the host negates HDMARDY- greater than  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the device.**
- e) The host shall assert STOP no sooner than  $t_{RP}$  after negating HDMARDY-. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- f) The device shall negate DMARQ within  $t_{LI}$  after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- g) If DSTROBE is negated, the device shall assert DSTROBE within  $t_{LI}$  after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The device shall release DD(15:0) no later than  $t_{AZ}$  after negating DMARQ.
- i) The host shall drive DD(15:0) no sooner than  $t_{ZAH}$  after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation (see 9.15).
- j) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (9), the host shall place the result of the host CRC calculation on DD(15:0) (see 9.15).
- k) The host shall negate DMACK- no sooner than  $t_{MLI}$  after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than  $t_{DVS}$  after the host places the result of the host CRC calculation on DD(15:0).
- l) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- m) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred (see 9.15) .

- n) The device shall release DSTROBE within  $t_{\text{IORDYZ}}$  after the host negates DMACK-.
- o) The host shall neither negate STOP nor assert HDMARDY- until at least  $t_{\text{ACK}}$  after the host has negated DMACK-.
- p) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least  $t_{\text{ACK}}$  after negating DMACK.

## 9.14 Ultra DMA data-out commands

### 9.14.1 Initiating an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.7 and 10.2.4.2 for specific timing requirements):

- a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
- b) The device shall assert DMARQ to initiate an Ultra DMA burst.
- c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
- d) The host shall assert HSTROBE.
- e) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.
- f) Steps (c), (d), and (e) shall have occurred at least  $t_{\text{ACK}}$  before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
- g) The device may negate DDMARDY-  $t_{\text{ZIORDY}}$  after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until after the host has negated DMACK- at the end of an Ultra DMA burst.
- h) The host shall negate STOP within  $t_{\text{ENV}}$  after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.
- i) The device shall assert DDMARDY- within  $t_{\text{LI}}$  after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.
- j) The host shall drive the first word of the data transfer onto DD(15:0). This step may occur any time during Ultra DMA burst initiation.
- k) To transfer the first word of data: the host shall negate HSTROBE no sooner than  $t_{\text{UI}}$  after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than  $t_{\text{DVS}}$  after the driving the first word of data onto DD(15:0).

### 9.14.2 The data-out transfer

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.8 and 10.2.4.2 for specific timing requirements):

- a) The host shall drive a data word onto DD(15:0).
- b) The host shall generate an HSTROBE edge to latch the new word no sooner than  $t_{\text{DVS}}$  after changing the state of DD(15:0). The host shall generate an HSTROBE edge no more frequently than  $t_{\text{CYC}}$  for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than  $2t_{\text{CYC}}$  for the selected Ultra DMA mode.
- c) The host shall not change the state of DD(15:0) until at least  $t_{\text{DVH}}$  after generating an HSTROBE edge to latch the data.
- d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

### 9.14.3 Pausing an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.9 and 10.2.4.2 for specific timing requirements).

### 9.14.3.1 Host pausing an Ultra DMA data-out burst

- a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall pause an Ultra DMA burst by not generating an HSTROBE edge.  
NOTE – The device shall not immediately negate DMARQ to initiate Ultra DMA burst termination when the host stops generating HSTROBE edges. If the host does not assert STOP, in order to initiate Ultra DMA burst termination, the device shall negate DDMARDY- and wait  $t_{RP}$  before negating DMARQ.
- c) The host shall resume an Ultra DMA burst by generating an HSTROBE edge.

### 9.14.3.2 Device pausing an Ultra DMA data-out burst

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by negating DDMARDY-.
- c) The host shall stop generating HSTROBE edges within  $t_{RFS}$  of the device negating DDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the device negates DDMARDY- within  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words; or, if the device negates DDMARDY- greater than  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the host.
- e) The device shall resume an Ultra DMA burst by asserting DDMARDY-.

## 9.14.4 Terminating an Ultra DMA data-out burst

### 9.14.4.1 Host terminating an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.10 and 10.2.4.2 for specific timing requirements):

- a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
- b) The host shall assert STOP no sooner than  $t_{SS}$  after the last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- c) The device shall negate DMARQ within  $t_{LI}$  after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- d) The device shall negate DDMARDY- within  $t_{LI}$  after the host has negated STOP. The device shall not assert DDMARDY- again until after the Ultra DMA burst termination is complete.
- e) If HSTROBE is negated, the host shall assert HSTROBE within  $t_{LI}$  after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- f) The host shall place the result of the host CRC calculation on DD(15:0) (see 9.15).
- g) The host shall negate DMACK- no sooner than  $t_{MLI}$  after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than  $t_{DVS}$  after placing the result of the host CRC calculation on DD(15:0).
- h) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- i) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 9.15).
- j) The device shall release DDMARDY- within  $t_{IORDYZ}$  after the host has negated DMACK-.
- k) The host shall neither negate STOP nor negate HSTROBE until at least  $t_{ACK}$  after negating DMACK-.
- l) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least  $t_{ACK}$  after negating DMACK.

#### 9.14.4.2 Device terminating an Ultra DMA data-out burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated.

The device shall terminate an Ultra DMA burst before command completion.

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.11 and 10.2.4.2 for specific timing requirements):

- a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall initiate Ultra DMA burst termination by negating DDMARDY-.
- c) The host shall stop generating an HSTROBE edges within  $t_{RFS}$  of the device negating DDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the device negates DDMARDY- within  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words; or, if the device negates DDMARDY- greater than  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the host.
- e) The device shall negate DMARQ no sooner than  $t_{RP}$  after negating DDMARDY-. The device shall not assert DMARQ again until after DMACK- is negated.
- f) The host shall assert STOP within  $t_{LI}$  after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- g) If HSTROBE is negated, the host shall assert HSTROBE within  $t_{LI}$  after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The host shall place the result of the host CRC calculation on DD(15:0) (see 9.15).
- i) The host shall negate DMACK- no sooner than  $t_{MLI}$  after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than  $t_{DVS}$  after placing the result of the host CRC calculation on DD(15:0).
- j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 9.15).
- l) The device shall release DDMARDY- within  $t_{IORDYZ}$  after the host has negated DMACK-.
- m) The host shall neither negate STOP nor HSTROBE until at least  $t_{ACK}$  after negating DMACK-.
- n) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least  $t_{ACK}$  after negating DMACK.

#### 9.15 Ultra DMA CRC rules

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

- 1) Both the host and the device shall have a 16-bit CRC calculation function.
- 2) Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
- 3) The CRC function in the host and the device shall be initialized with a seed of 4BAh at the beginning of an Ultra DMA burst before any data is transferred.
- 4) For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
- 5) At the end of any Ultra DMA burst the host shall send the results of the host CRC calculation function to the device on DD(15:0) with the negation of DMACK-.
- 6) The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a

previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

- 7) For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands: When a CRC error is detected, the error shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the "Interface CRC Error" bit. The host shall respond to this error by re-issuing the command.
- 8) For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.
- 9) For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.

NOTE – If excessive CRC errors are encountered while operating in Ultra mode 2 or 1, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.

- 10) A host may send extra data words on the last Ultra DMA burst of a data-out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data-out burst, the extra words shall be discarded by the device.
- 11) The CRC generator polynomial is:  $G(X) = X^{16} + X^{12} + X^5 + 1$ . Table 44 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

NOTE – Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where DD0 is shifted in first and DD15 is shifted in last.



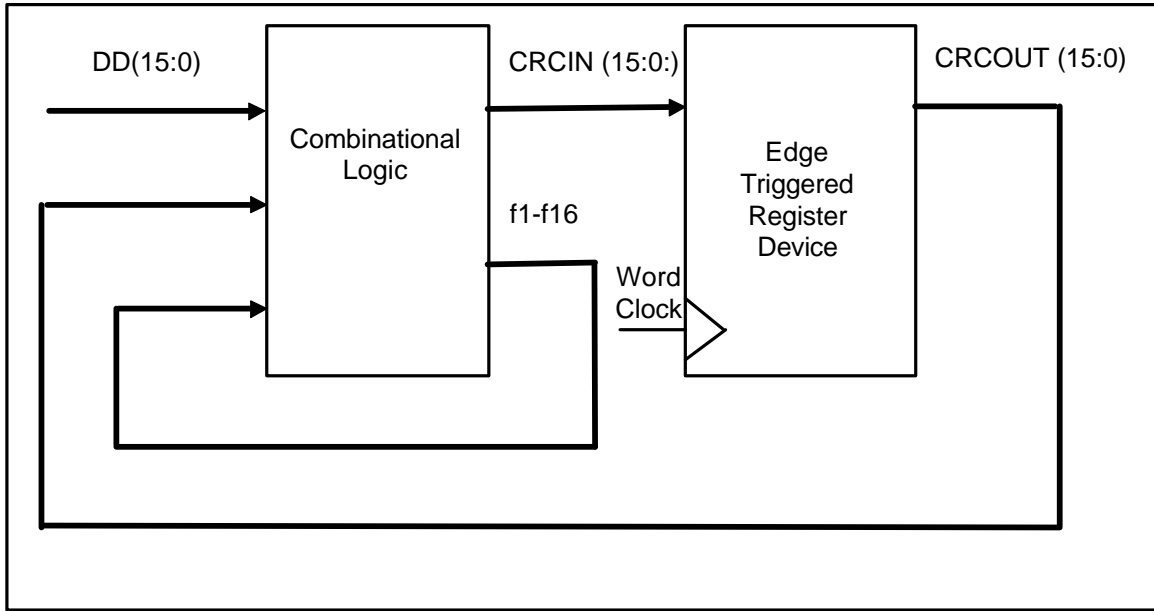


Figure 41 – Example Parallel CRC generator

Table 44 – Equations for parallel generation of a CRC polynomial

$CRCIN0 = f16$	$CRCIN8 = f8 \text{ XOR } f13$
$CRCIN1 = f15$	$CRCIN9 = f7 \text{ XOR } f12$
$CRCIN2 = f14$	$CRCIN10 = f6 \text{ XOR } f11$
$CRCIN3 = f13$	$CRCIN11 = f5 \text{ XOR } f10$
$CRCIN4 = f12$	$CRCIN12 = f4 \text{ XOR } f9 \text{ XOR } f16$
$CRCIN5 = f11 \text{ XOR } f16$	$CRCIN13 = f3 \text{ XOR } f8 \text{ XOR } f15$
$CRCIN6 = f10 \text{ XOR } f15$	$CRCIN14 = f2 \text{ XOR } f7 \text{ XOR } f14$
$CRCIN7 = f9 \text{ XOR } f14$	$CRCIN15 = f1 \text{ XOR } f6 \text{ XOR } f13$
$f1 = DD0 \text{ XOR } CRCOUT15$	$f9 = DD8 \text{ XOR } CRCOUT7 \text{ XOR } f5$
$f2 = DD1 \text{ XOR } CRCOUT14$	$f10 = DD9 \text{ XOR } CRCOUT6 \text{ XOR } f6$
$f3 = DD2 \text{ XOR } CRCOUT13$	$f11 = DD10 \text{ XOR } CRCOUT5 \text{ XOR } f7$
$f4 = DD3 \text{ XOR } CRCOUT12$	$f12 = DD11 \text{ XOR } CRCOUT4 \text{ XOR } f1 \text{ XOR } f8$
$f5 = DD4 \text{ XOR } CRCOUT11 \text{ XOR } f1$	$f13 = DD12 \text{ XOR } CRCOUT3 \text{ XOR } f2 \text{ XOR } f9$
$f6 = DD5 \text{ XOR } CRCOUT10 \text{ XOR } f2$	$f14 = DD13 \text{ XOR } CRCOUT2 \text{ XOR } f3 \text{ XOR } f10$
$f7 = DD6 \text{ XOR } CRCOUT9 \text{ XOR } f3$	$f15 = DD14 \text{ XOR } CRCOUT1 \text{ XOR } f4 \text{ XOR } f11$
$f8 = DD7 \text{ XOR } CRCOUT8 \text{ XOR } f4$	$f16 = DD15 \text{ XOR } CRCOUT0 \text{ XOR } f5 \text{ XOR } f12$
NOTES –	
1 f = feedback	
2 DD = Data to or from the bus	
3 CRCOUT = 16-bit edge triggered result (current CRC)	
4 CRCOUT(15:0) are sent on matching order bits of DD(15:0)	
5 CRCIN = Output of combinatorial logic (next CRC)	

## 9.16 Single device configurations

### 9.16.1 Device 0 only configurations

In a single device configuration where Device 0 is the only device and the host selects Device 1, Device 0 shall respond as follows:

- 1) A write to the Device Control register shall complete as if Device 0 was the selected device;

- 2) A write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected;
- 3) A write to the Command register shall be ignored, except for EXECUTE DEVICE DIAGNOSTIC;
- 4) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected;
- 5) A read of the Status or Alternate status register shall return the value 00h.

NOTE – Even though Device 1 is not present, the register content may appear valid for Device 1. Further means may be necessary to determine the existence of Device 1, e.g., issuing a command.

### 9.16.2 Device 1 only configurations

Host support of Device 1 only configurations is host specific.

In a single device configuration where Device 1 is the only device and the host selects Device 0, Device 1 shall respond to accesses of the Command Block and Control Block registers in the same way would if Device 0 was present. This is because Device 1 cannot determine if Device 0 is, or is not, present.

Host implementation of read and write operations to the Command and Control Block registers of non-existent Device 0 are host specific.

NOTE – The remainder of this section is a host implementation note. The host implementor should be aware of the following when supporting Device 1 only configurations:

- 1) Following a hardware reset or software reset, Device 1 will not be selected. The following steps may be used to reselect Device 1:
  - a) Write to the Device/Head register with DEV bit set to one;
  - b) Using one or more of the Command Block registers that may be both written and read, such as the Sector Count or Sector Number, write a data pattern other than 00h or FFh to the register(s);
  - c) Read the register(s) written in step (b). If the data read is the same as the data written, proceed to step (e);
  - d) Repeat steps (a) to (c) until the data matches in step (c) or until 31 s has past. After 31 s the host may assume that Device 1 is not functioning properly;
  - e) Read the Status register and Error registers. Check the Status and Error register contents for any error conditions that Device 1 may have posted.
- 2) Following the execution of an EXECUTE DEVICE DIAGNOSTIC command, Device 1 will not be selected. Also, no interrupt will be generated to signal command completion. After writing the EXECUTE DEVICE DIAGNOSTIC command to the Command register, execute steps (a) to (e) as described in (1) above;
- 3) At all other times, do not write zero into the DEV bit of the Device/Head register. All other commands execute normally.

## 10 Timing

### 10.1 Deskewing

For PIO and Multiword DMA modes the host shall provide cable deskewing for all signals originating from the device. The device shall provide cable deskewing for all signals originating from the host.

For Ultra DMA modes, timing parameters shall be measured at the connector of the device to which the parameter applies (unless otherwise specified). For all other modes, all timing values shall be measured at the connector of the selected device.

## 10.2 Transfer timing

The minimum cycle time supported by the device in PIO mode 3, 4 and Multiword DMA mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated mode e.g., a device supporting PIO mode 4 timing shall not report a value less than 120 ns, the minimum cycle time defined for PIO mode 4 timings.

See 3.2.8 for timing diagram conventions.

### 10.2.1 Register transfers

Figure 42 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of  $t_0$  is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 45 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO mode 3 and enable IORDY as the default.

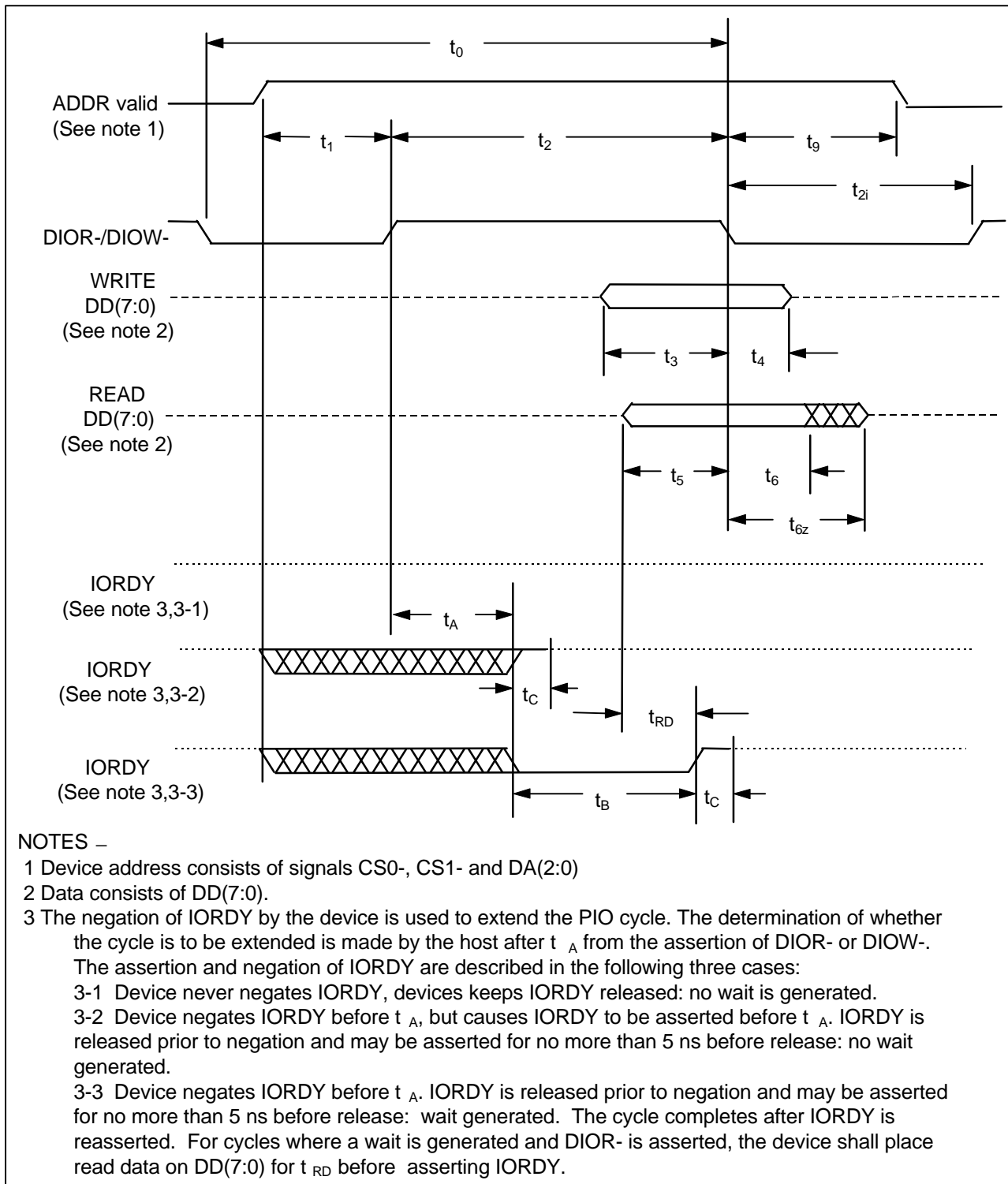


Figure 42 – Register transfer to/from device

**Table 45 – Register transfer to/from device**

PIO timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t <sub>0</sub>	Cycle time (min)	600	383	330	180	120	1,4
t <sub>1</sub>	Address valid to DIOR-/DIOW-setup (min)	70	50	30	30	25	
t <sub>2</sub>	DIOR-/DIOW- pulse width 8-bit (min)	290	290	290	80	70	1
t <sub>2i</sub>	DIOR-/DIOW- recovery time (min)	-	-	-	70	25	1
t <sub>3</sub>	DIOW- data setup (min)	60	45	30	30	20	
t <sub>4</sub>	DIOW- data hold (min)	30	20	15	10	10	
t <sub>5</sub>	DIOR- data setup (min)	50	35	20	20	20	
t <sub>6</sub>	DIOR- data hold (min)	5	5	5	5	5	
t <sub>6Z</sub>	DIOR- data tristate (max)	30	30	30	30	30	2
t <sub>9</sub>	DIOR-/DIOW- to address valid hold (min)	20	15	10	10	10	
t <sub>RD</sub>	Read Data Valid to IORDY active (if IORDY initially low after t <sub>A</sub> ) (min)	0	0	0	0	0	
t <sub>A</sub>	IORDY Setup time	35	35	35	35	35	3
t <sub>B</sub>	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t <sub>C</sub>	IORDY assertion to release (max)	5	5	5	5	5	

**NOTES –**

1 t<sub>0</sub> is the minimum total cycle time, t<sub>2</sub> is the minimum command active time, and t<sub>2i</sub> is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t<sub>0</sub>, t<sub>2</sub>, and t<sub>2i</sub> shall be met. The minimum total cycle time requirements is greater than the sum of t<sub>2</sub> and t<sub>2i</sub>. This means a host implementation may lengthen either or both t<sub>2</sub> or t<sub>2i</sub> to ensure that t<sub>0</sub> is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t<sub>A</sub> after the activation of DIOR- or DIOW-, then t<sub>5</sub> shall be met and t<sub>RD</sub> is not applicable. If the device is driving IORDY negated at the time t<sub>A</sub> after the activation of DIOR- or DIOW-, then t<sub>RD</sub> shall be met and t<sub>5</sub> is not applicable.

4 ATA/ATAPI standards prior to ATA/ATAPI-5 inadvertently specified the value for 16-bit PIO transfers in mode 2. time t<sub>0</sub>.

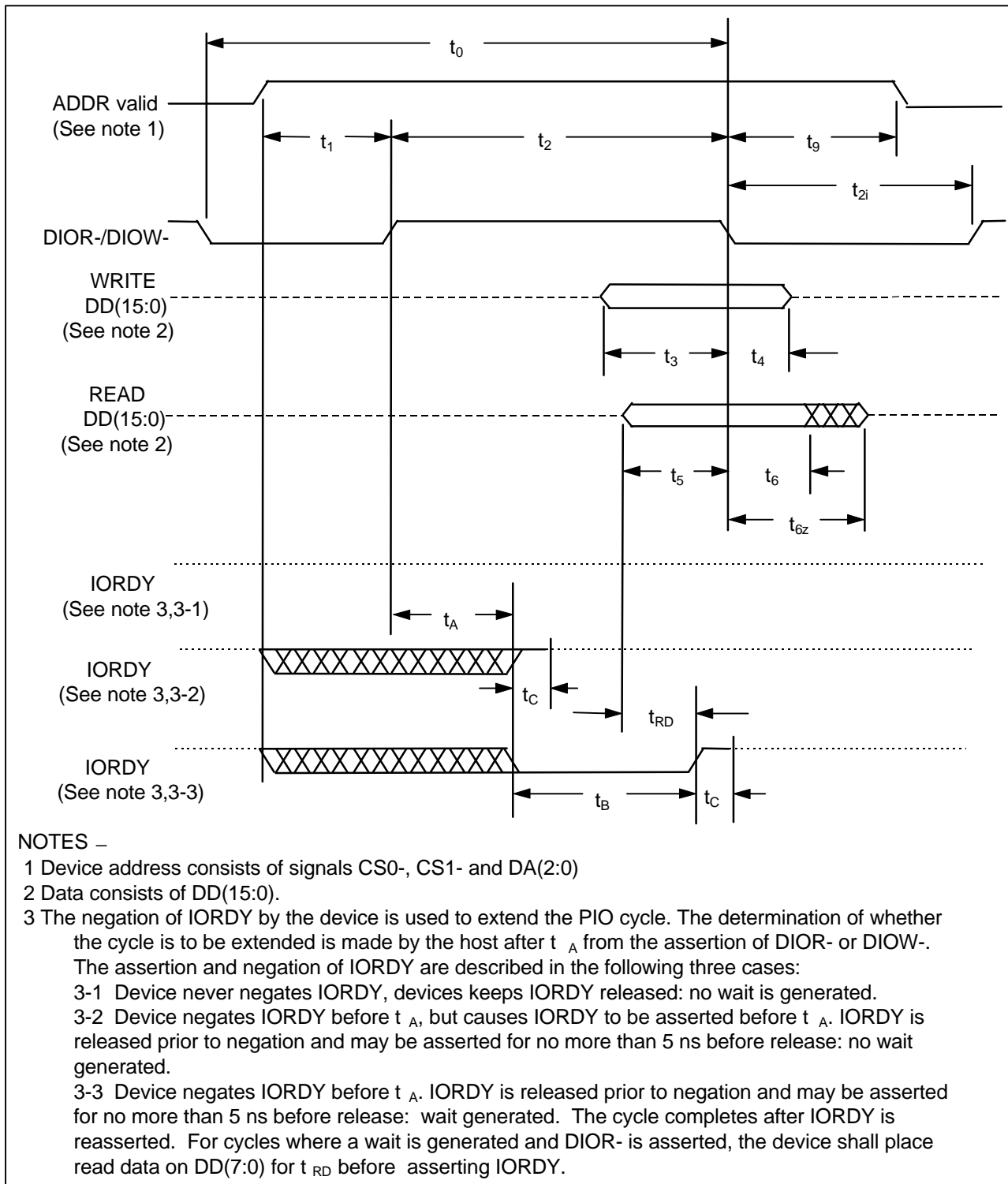
**10.2.2 PIO data transfers**

Figure 43 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t<sub>0</sub> is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 46 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO mode 3 and enable IORDY as the default.



**Figure 43 – PIO data transfer to/from device**

Table 46 – PIO data transfer to/from device

PIO timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t <sub>0</sub>	Cycle time (min)	600	383	240	180	120	1
t <sub>1</sub>	Address valid to DIOR-/DIOw-setup (min)	70	50	30	30	25	
t <sub>2</sub>	DIOR-/DIOw- 16-bit (min)	165	125	100	80	70	1
t <sub>2i</sub>	DIOR-/DIOw- recovery time (min)	-	-	-	70	25	1
t <sub>3</sub>	DIOw- data setup (min)	60	45	30	30	20	
t <sub>4</sub>	DIOw- data hold (min)	30	20	15	10	10	
t <sub>5</sub>	DIOR- data setup (min)	50	35	20	20	20	
t <sub>6</sub>	DIOR- data hold (min)	5	5	5	5	5	
t <sub>6Z</sub>	DIOR- data tristate (max)	30	30	30	30	30	2
t <sub>9</sub>	DIOR-/DIOw- to address valid hold (min)	20	15	10	10	10	
t <sub>RD</sub>	Read Data Valid to IORDY active (if IORDY initially low after t <sub>A</sub> ) (min)	0	0	0	0	0	
t <sub>A</sub>	IORDY Setup time	35	35	35	35	35	3
t <sub>B</sub>	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t <sub>C</sub>	IORDY assertion to release (max)	5	5	5	5	5	

## NOTES –

1 t<sub>0</sub> is the minimum total cycle time, t<sub>2</sub> is the minimum command active time, and t<sub>2i</sub> is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t<sub>0</sub>, t<sub>2</sub>, and t<sub>2i</sub> shall be met. The minimum total cycle time requirements is greater than the sum of t<sub>2</sub> and t<sub>2i</sub>. This means a host implementation may lengthen either or both t<sub>2</sub> or t<sub>2i</sub> to ensure that t<sub>0</sub> is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

3 The delay from the activation of DIOR- or DIOw- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t<sub>A</sub> after the activation of DIOR- or DIOw-, then t<sub>5</sub> shall be met and t<sub>RD</sub> is not applicable. If the device is driving IORDY negated at the time t<sub>A</sub> after the activation of DIOR- or DIOw-, then t<sub>RD</sub> shall be met and t<sub>5</sub> is not applicable.

### 10.2.3 Multiword DMA data transfer

Figure 44 defines the timings associated with Multiword DMA transfers.

For Multiword DMA modes 1 and above, the minimum value of t<sub>0</sub> is specified by word 65 in the IDENTIFY DEVICE parameter list. Table 47 defines the minimum value that shall be placed in word 65.

Devices shall power up with mode 0 as the default Multiword DMA mode.

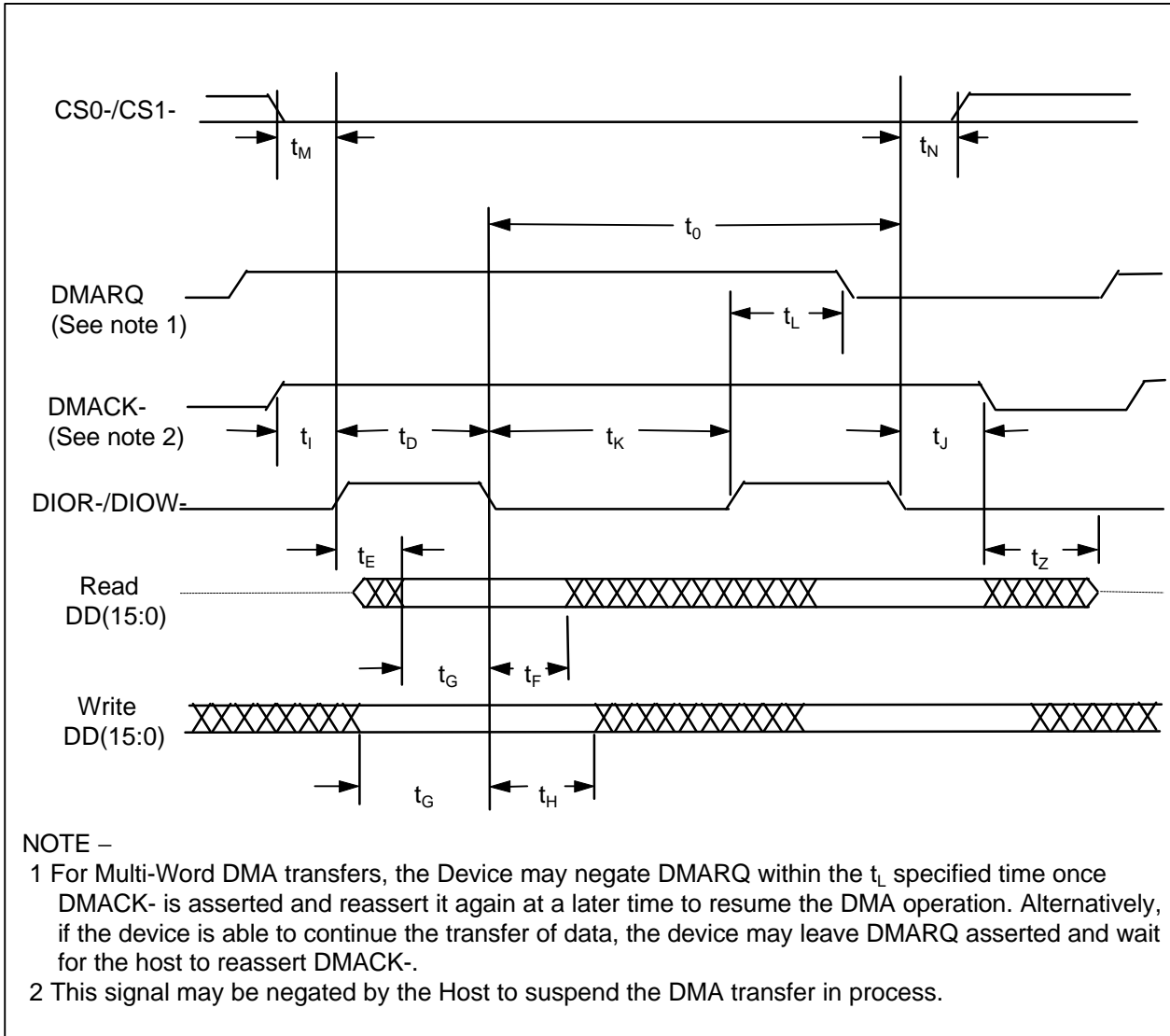


Figure 44 – Multiword DMA data transfer



Table 47 – Multiword DMA data transfer

	Multiword parameters	DMA timing	Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
$t_0$	Cycle time	(min)	480	150	120	see note
$t_D$	DIOR-/DIOW-	(min)	215	80	70	see note
$t_E$	DIOR- data access	(max)	150	60	50	
$t_F$	DIOR- data hold	(min)	5	5	5	
$t_G$	DIOR-/DIOW- data setup	(min)	100	30	20	
$t_H$	DIOW- data hold	(min)	20	15	10	
$t_I$	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
$t_J$	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
$t_{KR}$	DIOR- negated pulse width	(min)	50	50	25	see note
$t_{KW}$	DIOW- negated pulse width	(min)	215	50	25	see note
$t_{LR}$	DIOR- to DMARQ delay	(max)	120	40	35	
$t_{LW}$	DIOW- to DMARQ delay	(max)	40	40	35	
$t_M$	CS(1:0) valid to DIOR-/DIOW-	(min)	50	30	25	
$t_N$	CS(1:0) hold	(min)	15	10	10	
$t_Z$	DMACK- to tristate	(max)	20	25	25	

NOTE –  $t_0$  is the minimum total cycle time,  $t_D$  is the minimum command active time, and  $t_K$  ( $t_{KR}$  or  $t_{KW}$ , as appropriate) is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of  $t_0$ ,  $t_D$ ,  $t_K$  shall be met. The minimum total cycle time requirement,  $t_0$ , is greater than the sum of  $t_D$  and  $t_K$ . This means a host implementation may lengthen either or both  $t_D$  or  $t_K$  to ensure that  $t_0$  is equal to the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

### 10.2.4 Ultra DMA data transfer

Figures 23 through 32 define the timings associated with all phases of Ultra DMA bursts.

Table 48 contains the values for the timings for each of the Ultra DMA modes.

#### 10.2.4.1 Initiating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.

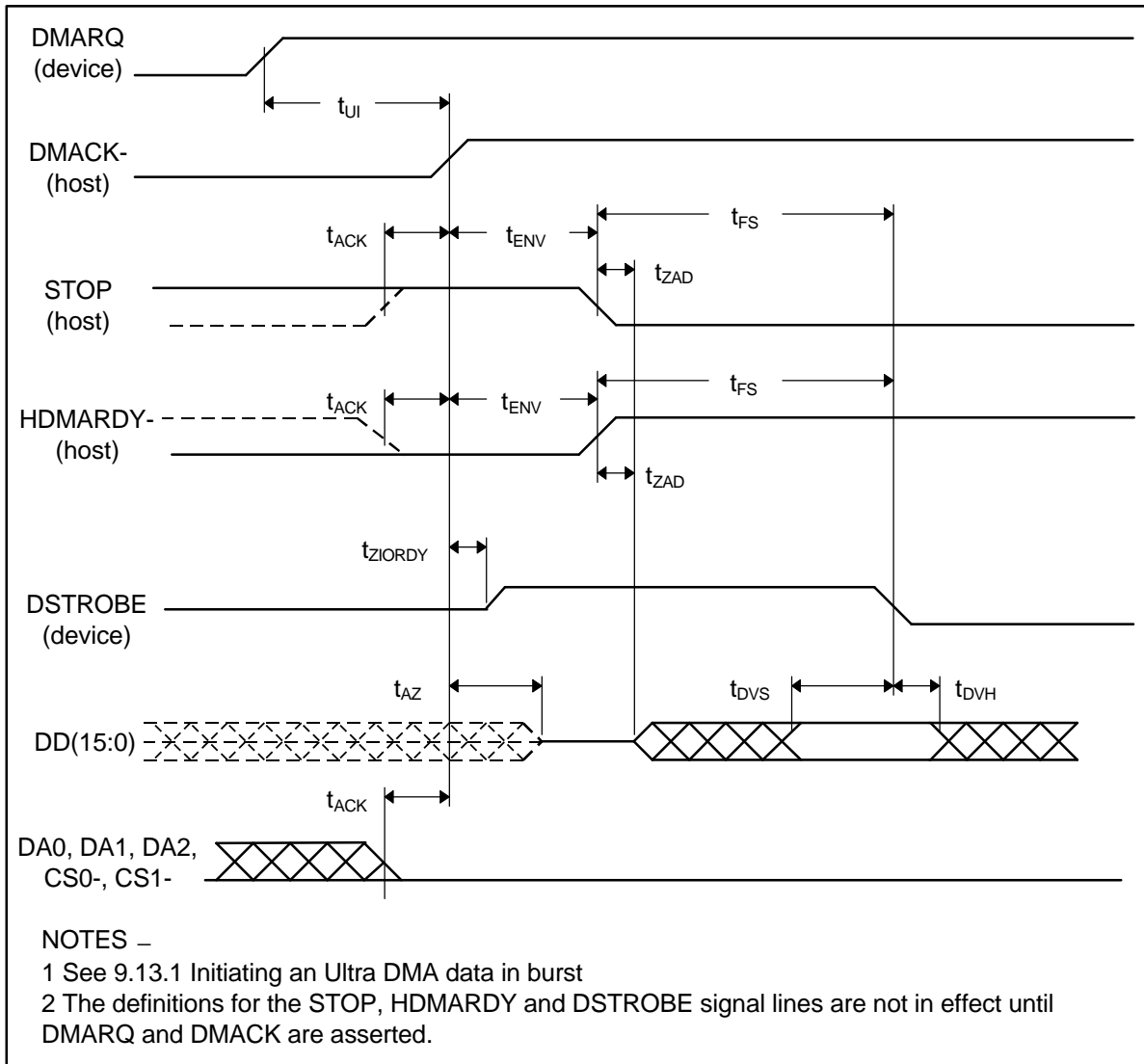


Figure 45 – Initiating an Ultra DMA data-in burst

## 10.2.4.2 Ultra DMA data burst timing requirements

Table 48 – Ultra DMA data burst timing requirements

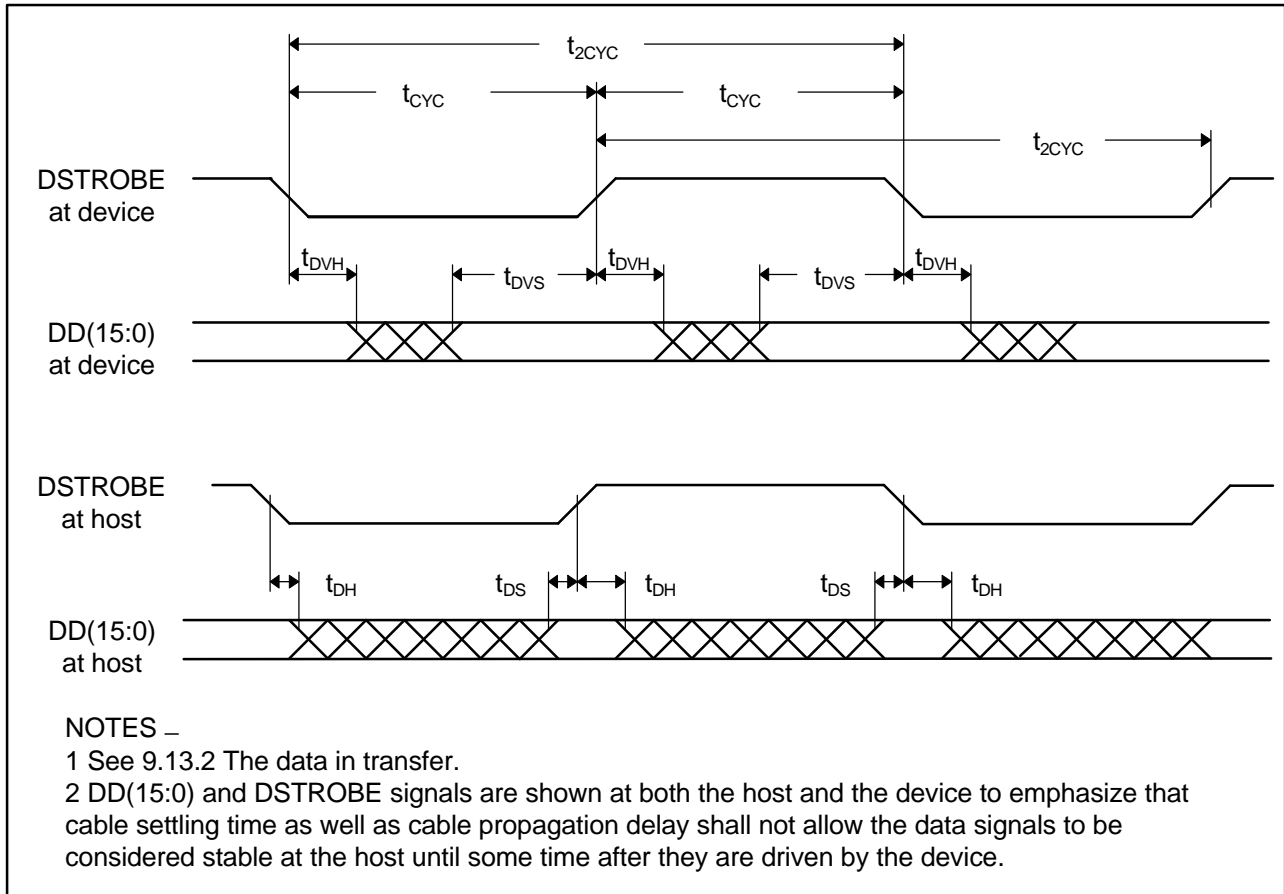
Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Comment (see Notes 1 and 2)
	min	max	min	max	min	max	min	max	min	max	
$t_{2CYCTYP}$	240		160		120		90		60		Typical sustained average two cycle time
$t_{CYC}$	112		73		54		39		25		Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
$t_{2CYC}$	230		154		115		86		57		Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
$t_{DS}$	15		10		7		7		5		Data setup time at recipient (see note 4)
$t_{DH}$	5		5		5		5		5		Data hold time at recipient (see note 4)
$t_{DVS}$	70		48		30		20		6		Data valid setup time at sender (from data valid until STROBE edge) (see Note 5)
$t_{DVH}$	6		6		6		6		6		Data valid hold time at sender (from STROBE edge until data may become invalid) (see Note 5)
$t_{FS}$	0	230	0	200	0	170	0	130	0	120	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
$t_{LI}$	0	150	0	150	0	150	0	100	0	100	Limited interlock time (see Note 3)
$t_{MLI}$	20		20		20		20		20		Interlock time with minimum (see Note 3)
$t_{UI}$	0		0		0		0		0		Unlimited interlock time (see Note 3)
$t_{AZ}$		10		10		10		10		10	Maximum time allowed for output drivers to release (from asserted or negated)
$t_{ZAH}$	20		20		20		20		20		Minimum delay time required for output
$t_{ZAD}$	0		0		0		0		0		drivers to assert or negate (from released)
$t_{ENV}$	20	70	20	70	20	70	20	55	20	55	Envelope time (from DMACK- to STOP and DMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
$t_{SR}$		50		30		20		NA		NA	STROBE-to-DMARDY- time (if DMARDY- is negated before this long after STROBE edge, the recipient shall receive no more than one additional data word)
$t_{RFS}$		75		70		60		60		60	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
$t_{RP}$	160		125		100		100		100		Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
$t_{IORDYZ}$		20		20		20		20		20	Maximum time before releasing IORDY
$t_{ZIORDY}$	0		0		0		0		0		Minimum time before driving IORDY (see note 6)
$t_{ACK}$	20		20		20		20		20		Setup and hold times for DMACK- (before assertion or negation)
$t_{SS}$	50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

## NOTES –

- Timing parameters shall be measured at the connector of the sender or receiver to which the parameter applies. For example, the sender shall stop generating STROBE edges  $t_{RFS}$  after the negation of DMARDY-. Both STROBE and DMARDY- timing measurements are taken at the connector of the sender.
- All timing measurement switching points (low to high and high to low) shall be taken at 1.5V.
- $t_{UI}$ ,  $t_{MLI}$  and  $t_{LI}$  indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.  $t_{UI}$  is an unlimited interlock that has no maximum time value.  $t_{MLI}$  is a limited time-out that has a defined minimum.  $t_{LI}$  is a limited time-out that has a defined maximum.
- Special cabling shall be required in order to meet data setup ( $t_{DS}$ ) and data hold ( $t_{DH}$ ) times in modes 3 and 4.
- Timing for  $t_{DVS}$  and  $t_{DVH}$  shall be met for all capacitive loads from 15 to 40 pF where all signals have the same capacitive load value.
- $t_{ZIORDY}$  has no maximum and may be greater than  $t_{ENV}$  since the device has a pull up on IORDY- giving it a known state when released.

### 10.2.4.3 Sustained Ultra DMA data-in burst

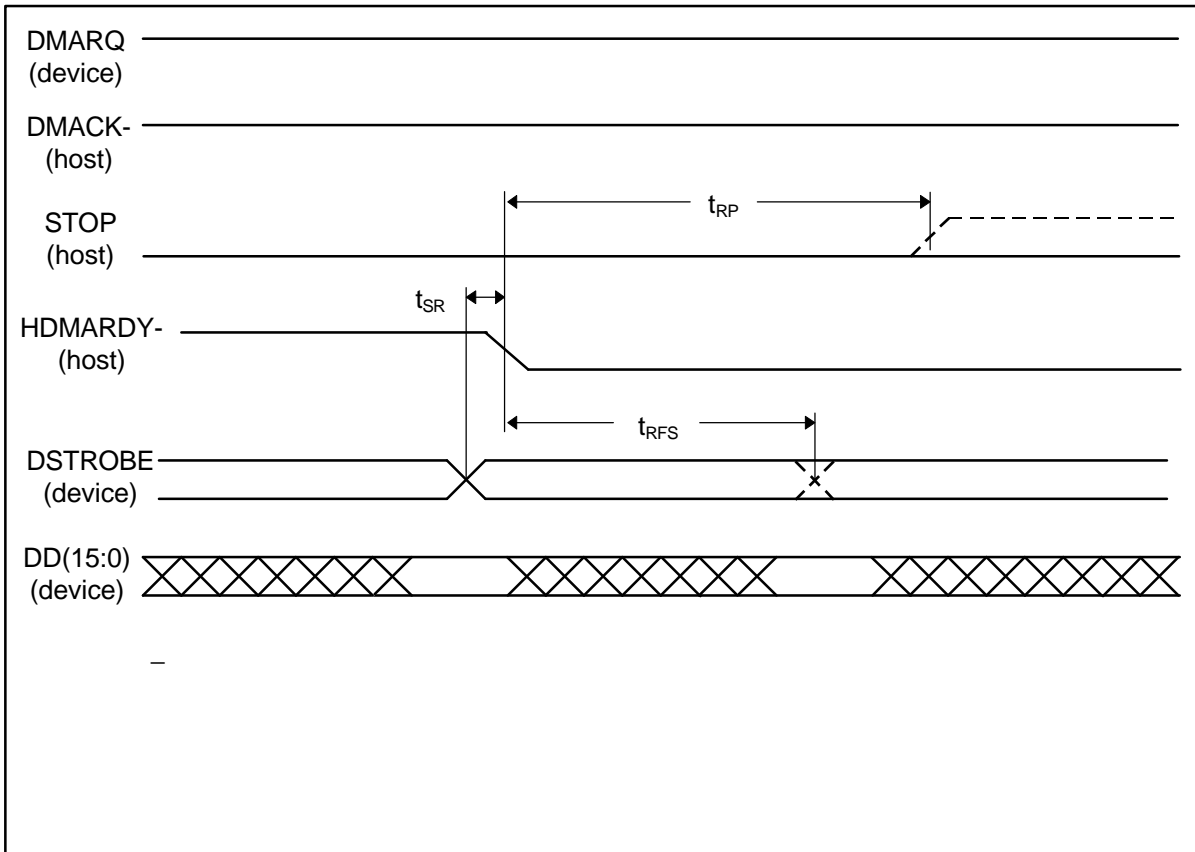
The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.



**Figure 46 – Sustained Ultra DMA data-in burst**

**10.2.4.4 Host pausing an Ultra DMA data-in burst**

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.



**Figure 47 – Host pausing an Ultra DMA data-in burst**

### 10.2.4.5 Device terminating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.

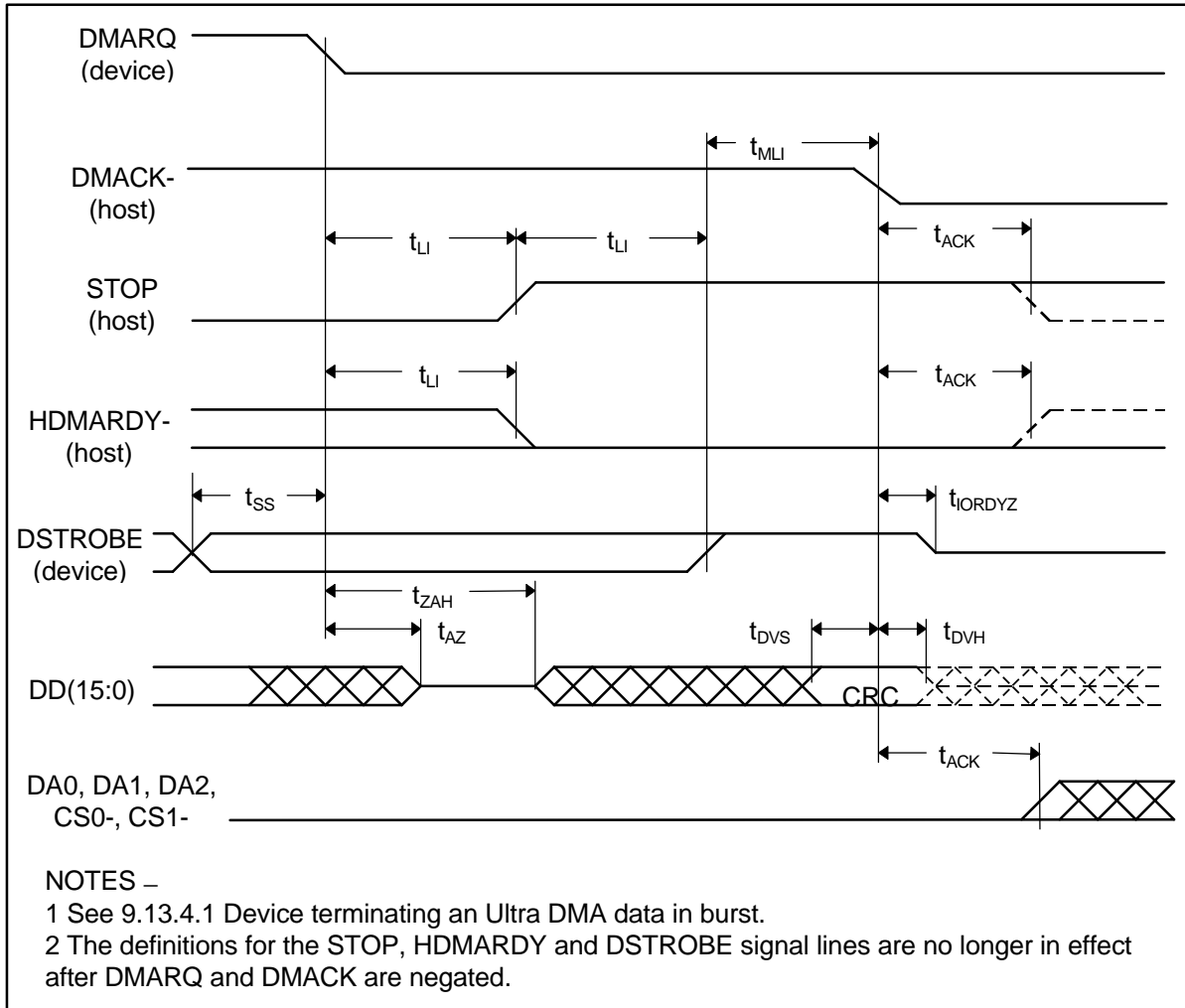
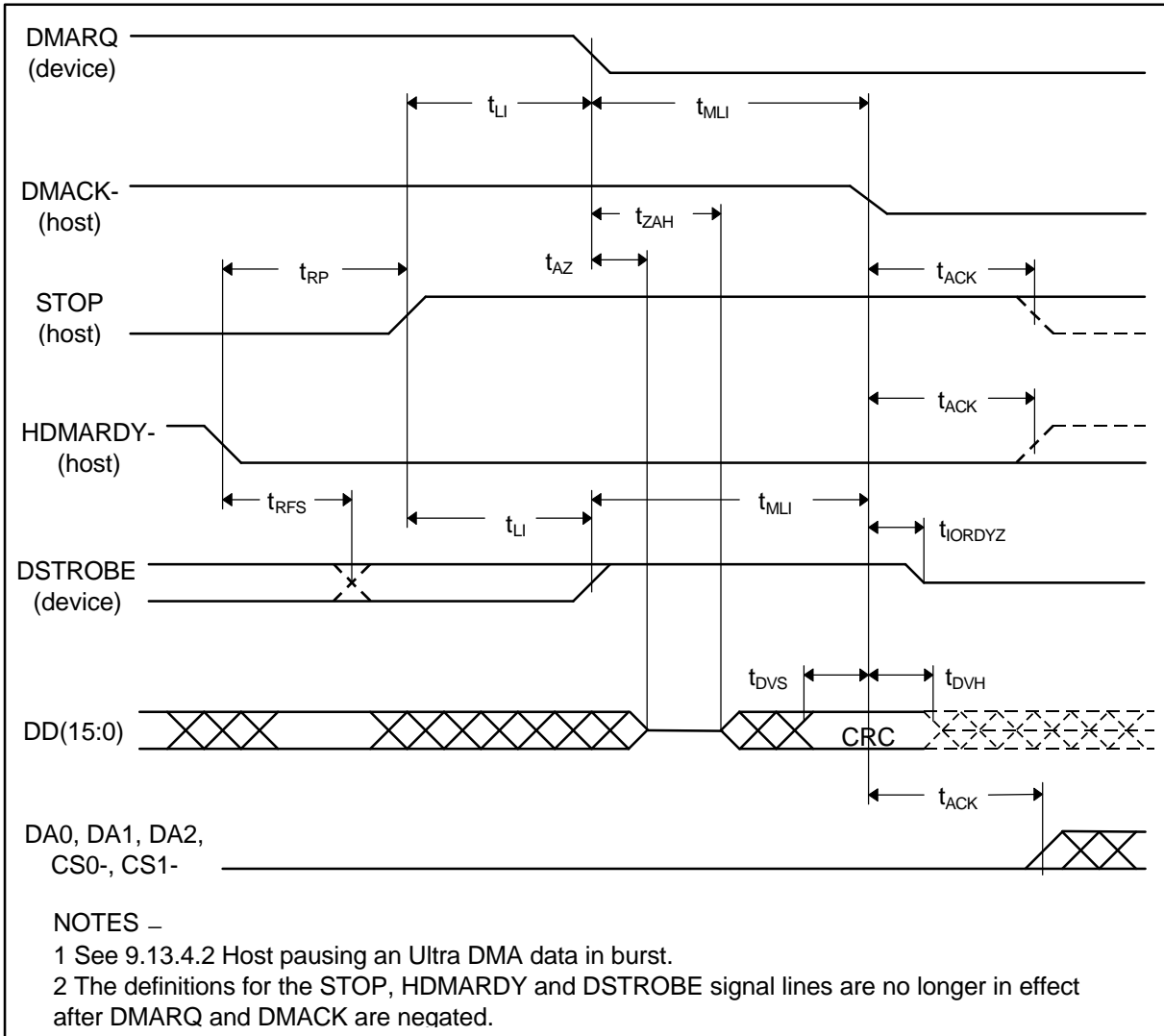


Figure 48 – Device terminating an Ultra DMA data-in burst

**10.2.4.6 Host terminating an Ultra DMA data-in burst**

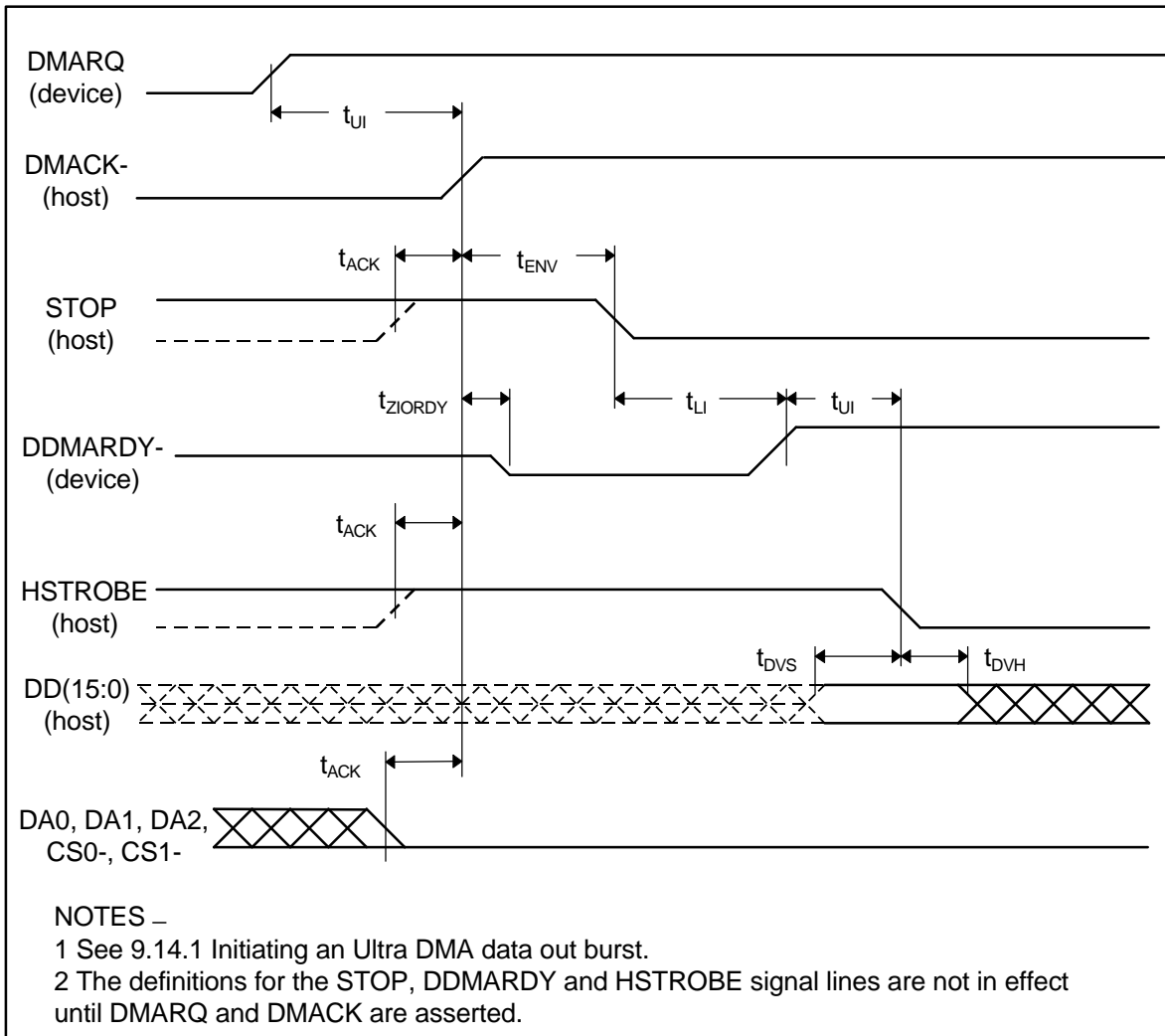
The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.



**Figure 49 – Host terminating an Ultra DMA data-in burst**

### 10.2.4.7 Initiating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.

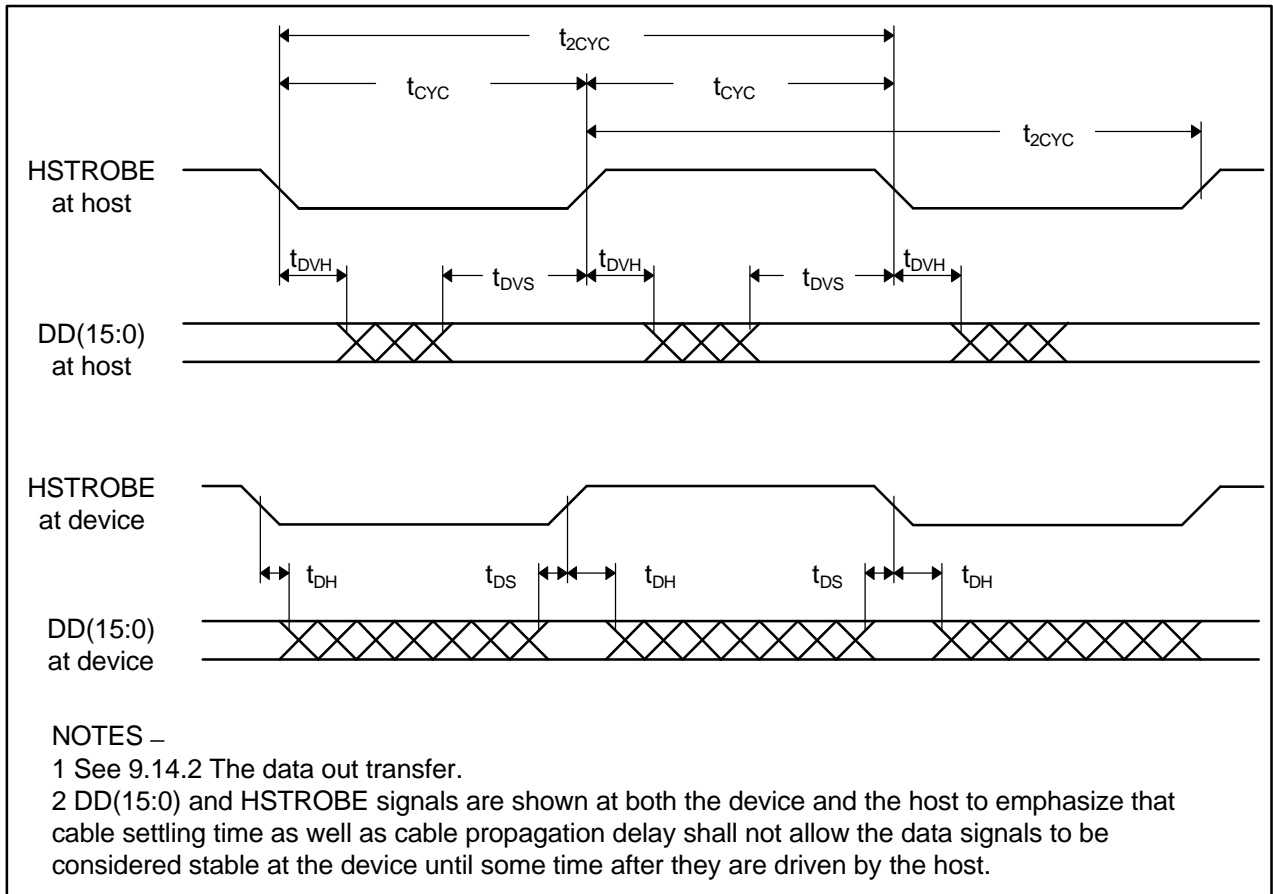


**Figure 50 – Initiating an Ultra DMA data-out burst**



**10.2.4.8 Sustained Ultra DMA data-out burst**

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.



**Figure 51 – Sustained Ultra DMA data-out burst**

### 10.2.4.9 Device pausing an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.

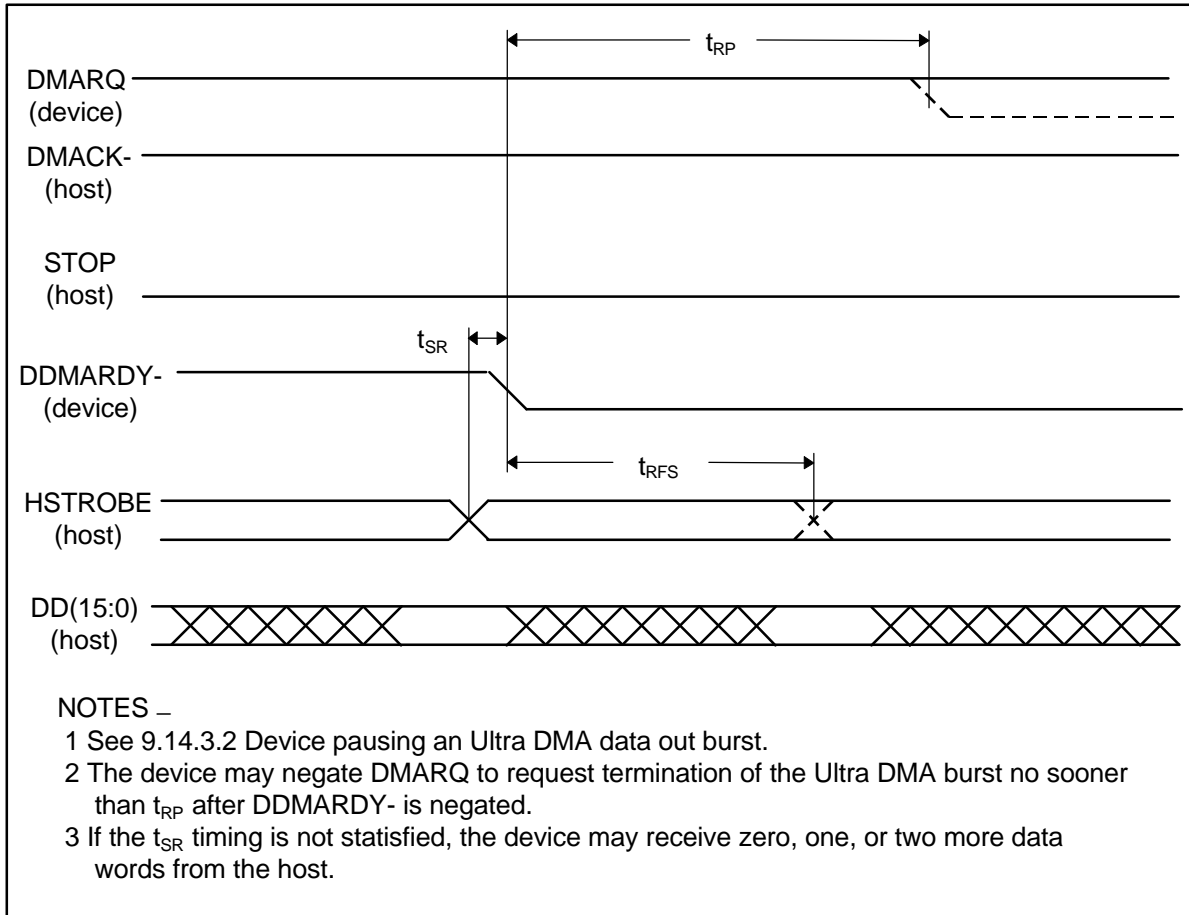
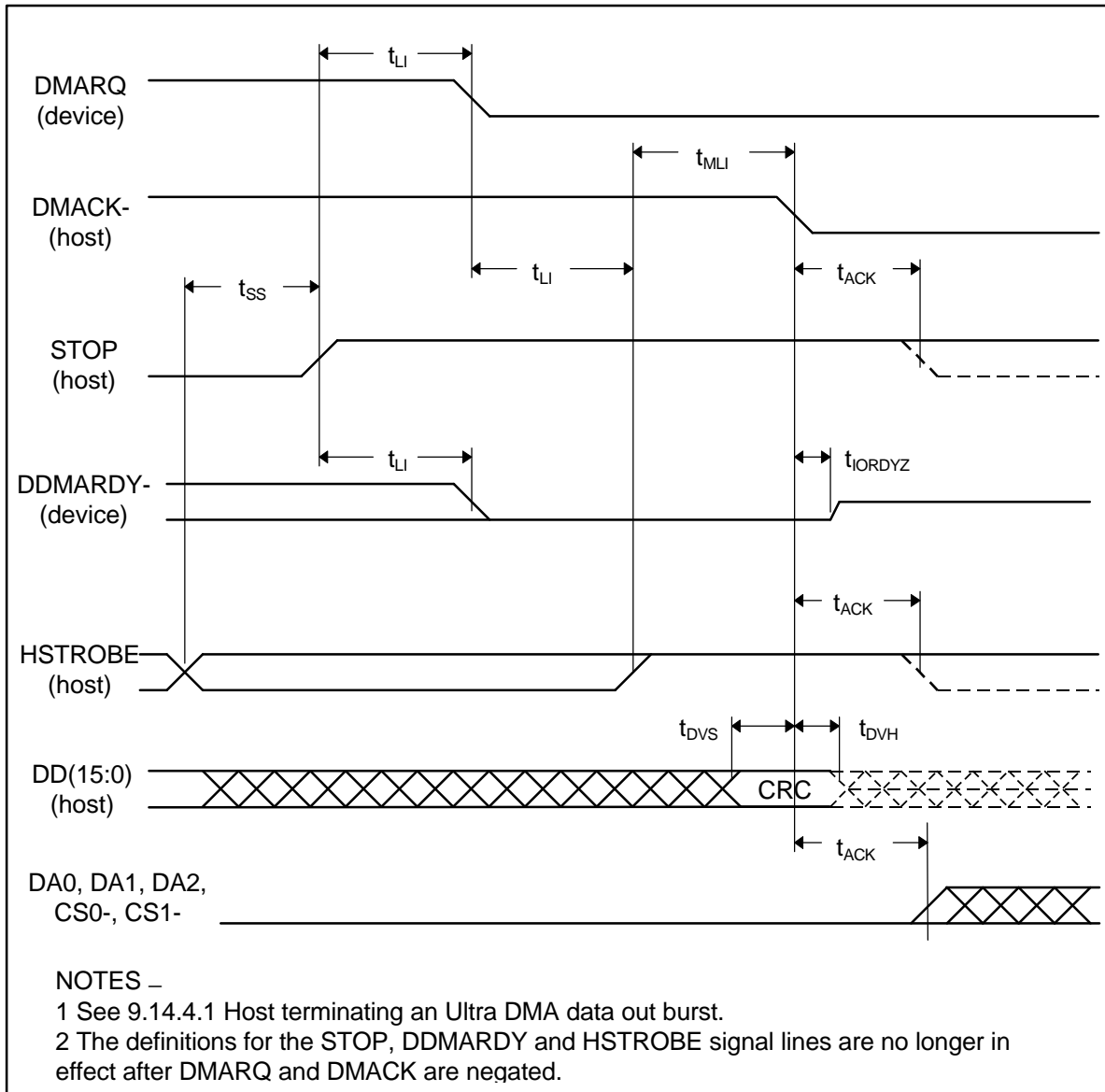


Figure 52 – Device pausing an Ultra DMA data-out burst

**10.2.4.10 Host terminating an Ultra DMA data-out burst**

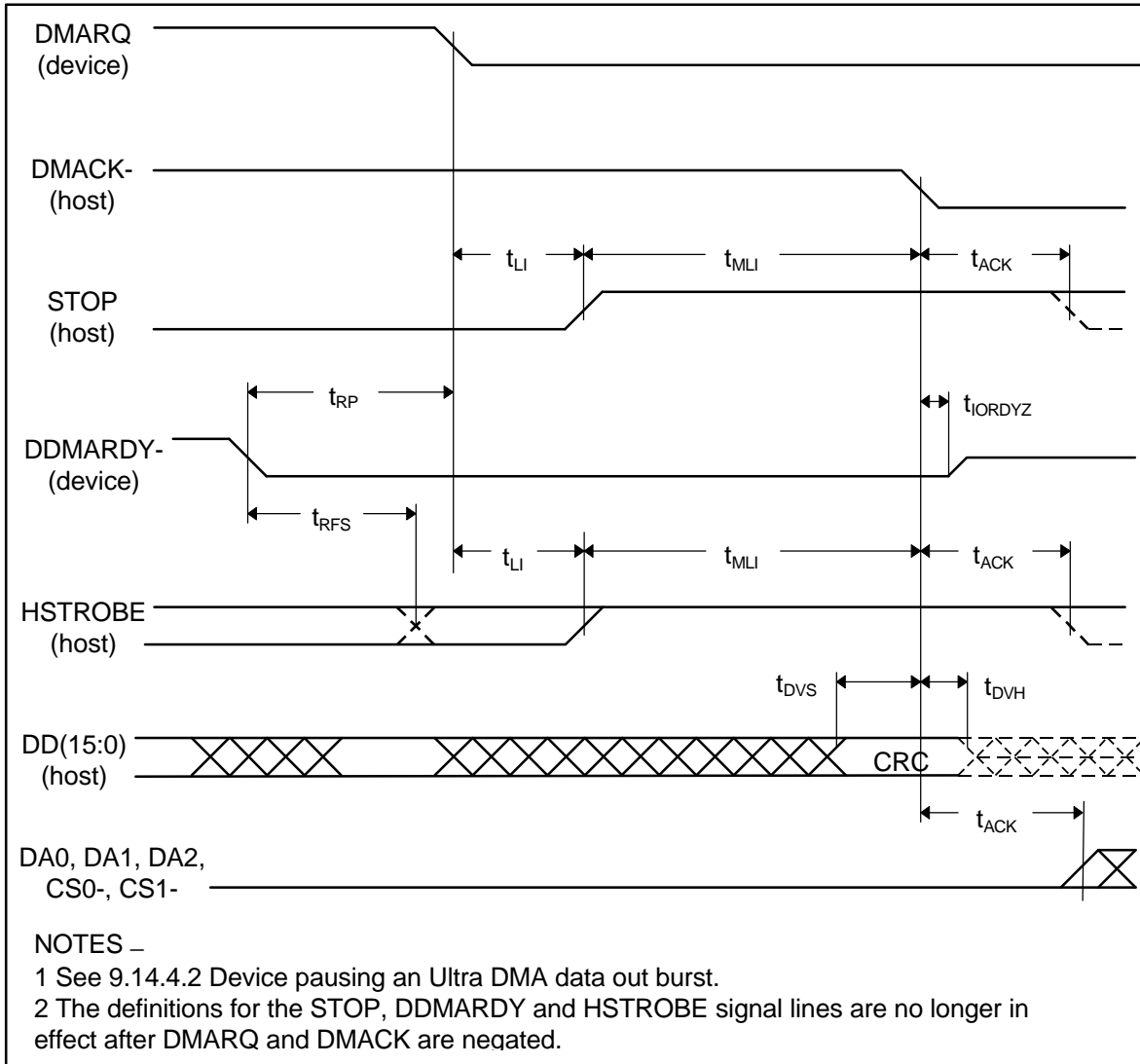
The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.



**Figure 53 – Host terminating an Ultra DMA data-out burst**

**10.2.4.11 Device terminating an Ultra DMA data-out burst**

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.2.



**Figure 54 – Device terminating an Ultra DMA data-out burst**

**Annex A**  
(normative)  
**Connectors and cable assemblies**

The device shall implement one of the connector options described in this annex.

### **A.1 40-pin Connector**

The I/O connector is a 40-pin connector. The header mounted to a host or device is shown in figure A.1 and the dimensions are shown in table A.1. The connector mounted to the end of the cable is shown in figure A.2 and the dimensions are shown in table A.2. Signal assignments on these connectors are shown in table A.3.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle may or may not be polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in figure A.3, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

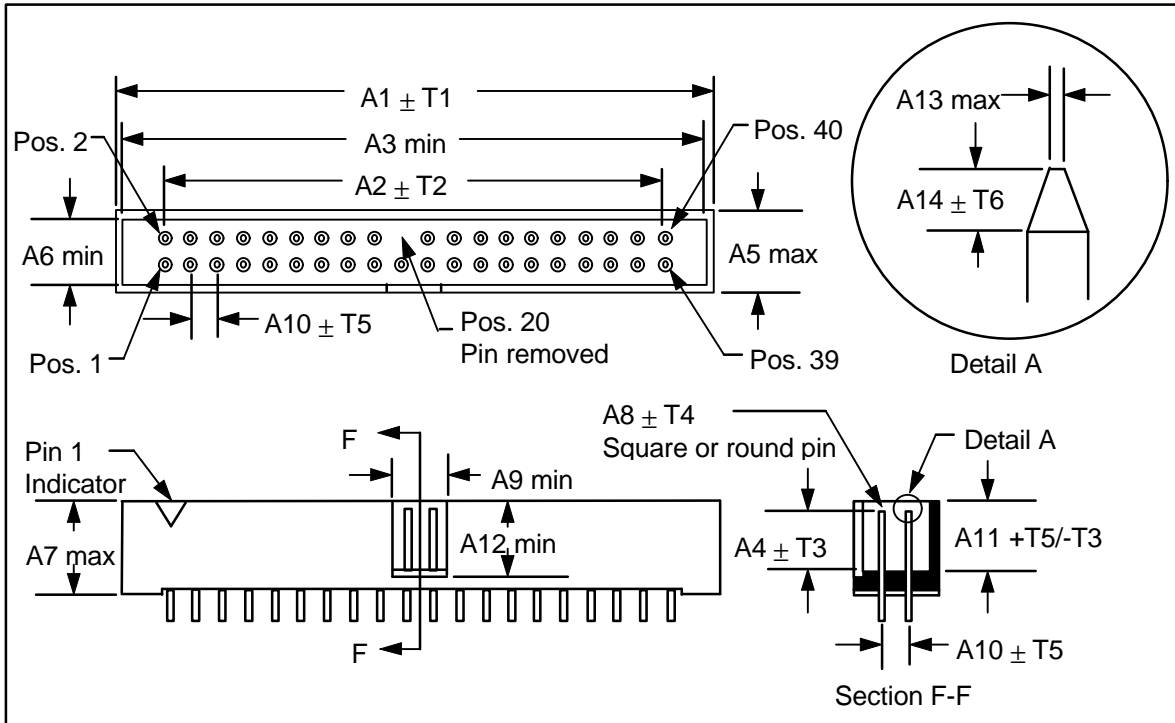
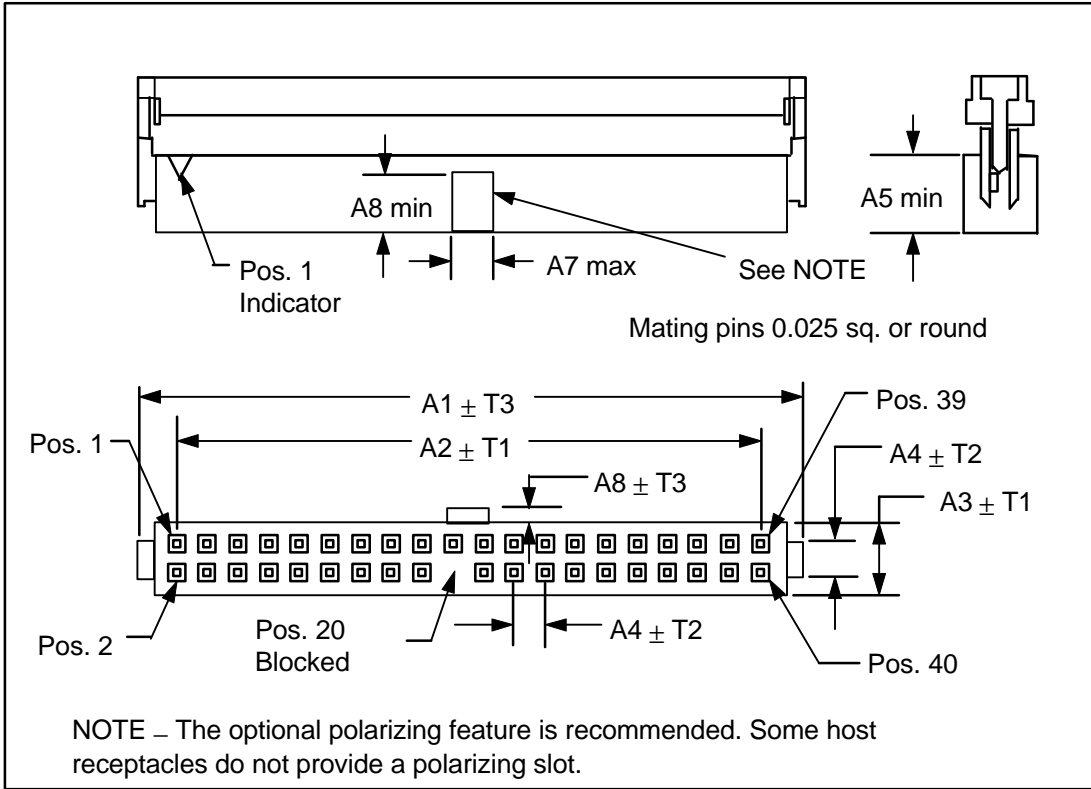


Figure A.1 – Host or device 40-pin I/O header

Table A.1 – Host or device 40-pin I/O header

Dimension	Millimeters	Inches
A 1	58.17	2.290
A 2	48.26	1.900
A 3	56.01	2.205
A 4	5.84	0.230
A 5	9.55	0.376
A 6	6.22	0.245
A 7	10.16	0.400
A 8	0.64	0.025
A 9	4.06	0.160
A 10	2.54	0.100
A 11	6.35	0.250
A 12	6.48	0.255
A 13	0.33	0.013
A 14	0.58	0.023
T 1	0.51	0.020
T 2	0.13	0.005
T 3	0.25	0.010
T 4	0.03	0.001
T 5	0.08	0.003
T 6	0.18	0.007



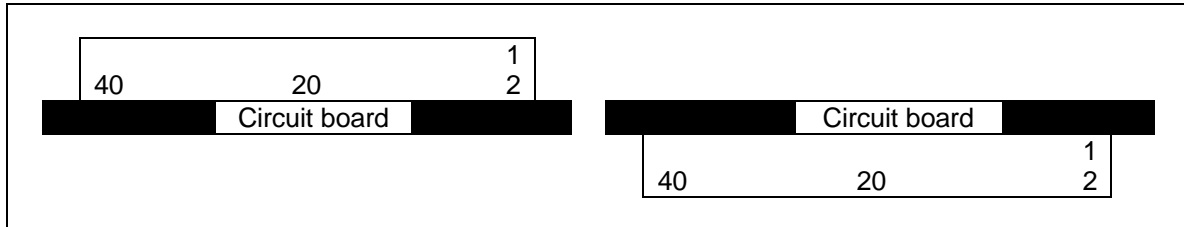
**Figure A.2 – 40-pin I/O cable connector**

**Table A.2 – 40-pin I/O cable connector**

Dimension	Millimeters	Inches
A 1	55.37	2.180
A 2	48.26	1.900
A 3	6.10	0.240
A 4	2.54	0.100
A 5	6.48	0.255
A 6	4.57	0.180
A 7	3.81	0.150
A 8	1.27	0.050
T 1	0.13	0.005
T 2	0.08	0.003
T 3	0.25	0.010

**Table A.3 – 40-pin I/O connector interface signals**

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY- :HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY- :DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-:CBLID-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

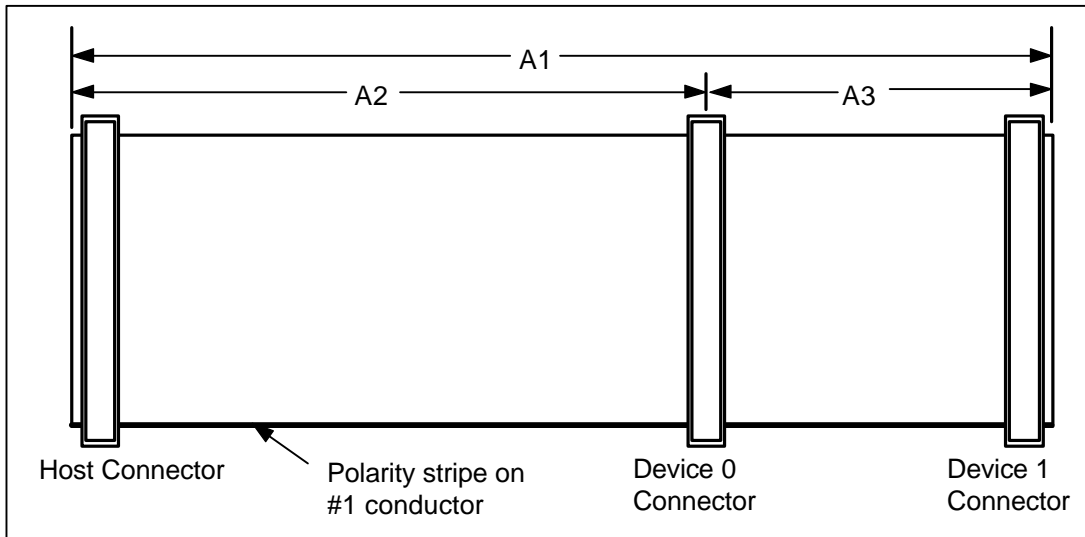


**Figure A.3 – 40-pin I/O header mounting**

**A.1.1 40-conductor cable**

The 40-conductor cable assembly is shown in figure A.4 with dimensions in table A.4. Cable capacitance shall not exceed 35 pf.





**Figure A.4 – 40-conductor cable configuration**

**Table A.4 – 40-conductor cable configuration**

Dimension	Millimeters	Inches
A 1	254.00 min 457.20 max	10.00 min 18.00 max
A 2	127.00 min 304.80 max	5.00 min 12.00 max
A 3	127.00 min 152.40 max	5.00 min 6.00 max

**A.1.2 80-conductor cable assembly using the 40-pin connector**

To provide better signal integrity, the optional 80-conductor cable assembly is specified for use with 40-pin connectors. Use of this assembly is mandatory for systems operating at Ultra DMA modes greater than 2. The mating half of the connector is as described in A.1. Every other conductor in the 80-conductor cable is connected to the ground pins in each connector.

The electrical requirements of the 80-conductor ribbon cable are shown in table A.5 and the physical requirements are described in figure A.5 and table A.6.

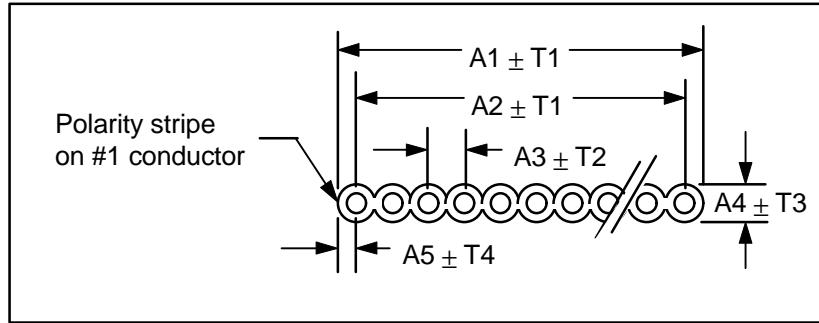
Figure A.6 and table A.7 describe the physical dimensions of the cable assembly. The connector in the center of the cable assembly labeled Device 1 Connector is optional. The System Board connector shall have a blue base and a black or blue retainer. The Device 0 Connector shall have a black base and a black retainer. The Device 1 Connector shall have a gray base and a black or gray retainer. The cable assembly may be printed with connector identifiers.

There are alternative cable conductor to connector pin assignments depending on whether the connector attaches all even or odd conductors to ground. Table A.8 shows the signal assignments for connectors that ground the even numbered conductors. Table A.9 shows the signal assignments for connectors that ground the odd numbered conductors. Only one connector type, even or odd, shall be used in a given cable assembly. Connectors shall be labeled as grounding the even or odd conductors as shown in figure A.7. Cable assemblies conforming to table A.8 are interchangeable with cable assemblies conforming to table A.9.

All connectors shall have position 20 blocked to provide keying. Pin 28 in Device 1 Connector shall not be attached to any cable conductor, the connector contact may be removed to meet this requirement. Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to ground within the connector.

**Table A.5 – 80-conductor cable electrical requirements**

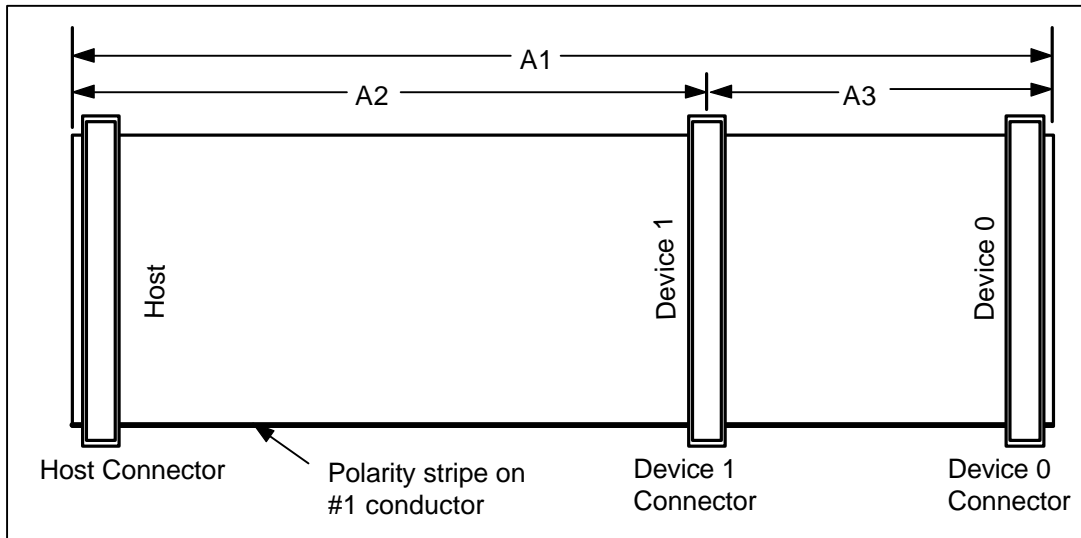
Conductor		30 AWG
Ground-signal-ground		
Single ended impedance	( $\Omega$ )	70-90
Capacitance	(pF/ft) (pF/m)	13-22 42-72
Inductance	( $\mu$ H)	0.08-0.16
Propagation delay	(nsec/ft) (nsec/m)	1.35-1.65 4.43-5.41



**Figure A.5 – 80-conductor microcable**

**Table A.6 – 80-conductor microcable**

Dimension	Millimeters	Inches
A 1	50.800	2.000
A 2	50.165	1.975
A 3	0.635	0.025
A 4	0.6858	0.027
A 5	0.3175	0.0125
T 1	0.127	0.005
T 2	0.0406	0.0016
T 3	0.0508	0.002
T 4	0.102	0.004



**Figure A.6 – 80-conductor cable configuration**

**Table A.7 – 80-conductor cable configuration**

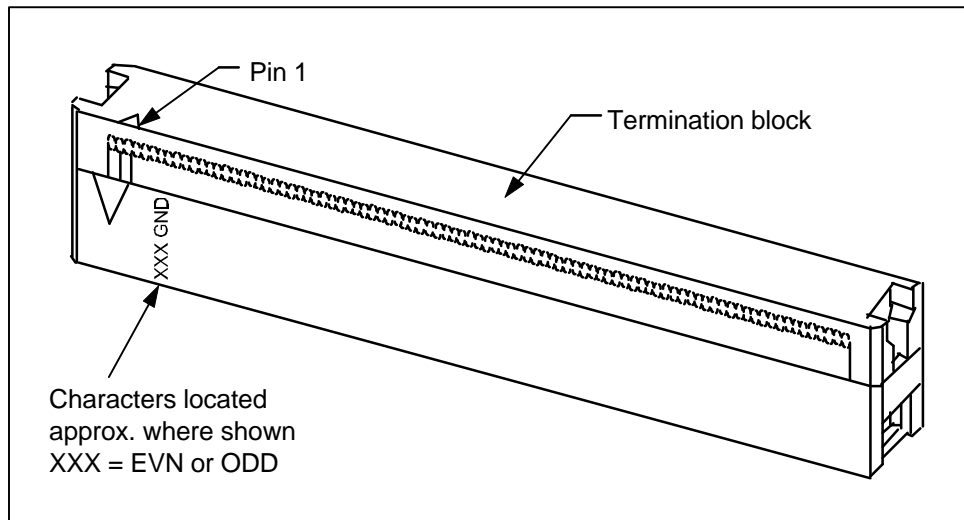
Dimension	Millimeters	Inches
A 1	457.20 max	18.00 max
A 2	127.00 min	5.00 min
A 3	152.40 max	6.00 max
A2 min shall be greater than or equal to A3.		

**Table A.8 – Signal assignments for connectors grounding even conductors**

Signal name	Connector contact	Conductor		Signal name
RESET-	1	1	2	Ground
Ground	2	3	4	Ground
DD7	3	5	6	Ground
DD8	4	7	8	Ground
DD6	5	9	10	Ground
DD9	6	11	12	Ground
DD5	7	13	14	Ground
DD10	8	15	16	Ground
DD4	9	17	18	Ground
DD11	10	19	20	Ground
DD3	11	21	22	Ground
DD12	12	23	24	Ground
DD2	13	25	26	Ground
DD13	14	27	28	Ground
DD1	15	29	30	Ground
DD14	16	31	32	Ground
DD0	17	33	34	Ground
DD15	18	35	36	Ground
Ground	19	37	38	Ground
(keypin)	20	39	40	Ground
DMARQ	21	41	42	Ground
Ground	22	43	44	Ground
DLOW-	23	45	46	Ground
Ground	24	47	48	Ground
DIOR-	25	49	50	Ground
Ground	26	51	52	Ground
IORDY	27	53	54	Ground
CSEL	28	55	56	Ground
DMACK-	29	57	58	Ground
Ground	30	59	60	Ground
INTRQ	31	61	62	Ground
reserved	32	63	64	Ground
DA1	33	65	66	Ground
PDIAG-	34	67	68	Ground
DA0	35	69	70	Ground
DA2	36	71	72	Ground
CS0-	37	73	74	Ground
CS1-	38	75	76	Ground
DASP-	39	77	78	Ground
Ground	40	79	80	Ground

**Table A.9 – Signal assignments for connectors grounding odd conductors**

Signal name	Conductor		Connector contact	Signal name
Ground	1	2	1	RESET-
Ground	3	4	2	Ground
Ground	5	6	3	DD7
Ground	7	8	4	DD8
Ground	9	10	5	DD6
Ground	11	12	6	DD9
Ground	13	14	7	DD5
Ground	15	16	8	DD10
Ground	17	18	9	DD4
Ground	19	20	10	DD11
Ground	21	22	11	DD3
Ground	23	24	12	DD12
Ground	25	26	13	DD2
Ground	27	28	14	DD13
Ground	29	30	15	DD1
Ground	31	32	16	DD14
Ground	33	34	17	DD0
Ground	35	36	18	DD15
Ground	37	38	19	Ground
Ground	39	40	20	(keypin)
Ground	41	42	21	DMARQ
Ground	43	44	22	Ground
Ground	45	46	23	DIOW-
Ground	47	48	24	Ground
Ground	49	50	25	DIOR-
Ground	51	52	26	Ground
Ground	53	54	27	IORDY
Ground	55	56	28	CSEL
Ground	57	58	29	DMACK-
Ground	59	60	30	Ground
Ground	61	62	31	INTRQ
Ground	63	64	32	reserved
Ground	65	66	33	DA1
Ground	67	68	34	PDIAG-
Ground	69	70	35	DA0
Ground	71	72	36	DA2
Ground	73	74	37	CS0-
Ground	75	76	38	CS1-
Ground	77	78	39	DASP-
Ground	79	80	40	Ground



**Figure A.7 – Connector labeling for even or odd conductor grounding**

## A.2 4-pin power connector

The power connector is a 4-pin connector. The header mounted to a device is shown in figure A.8 and the dimensions are shown in table A.10. The connector mounted to the end of the cable is shown in figure A.9 and the dimensions are shown in table A.11. Pin assignments for these connectors are shown in table A.12.

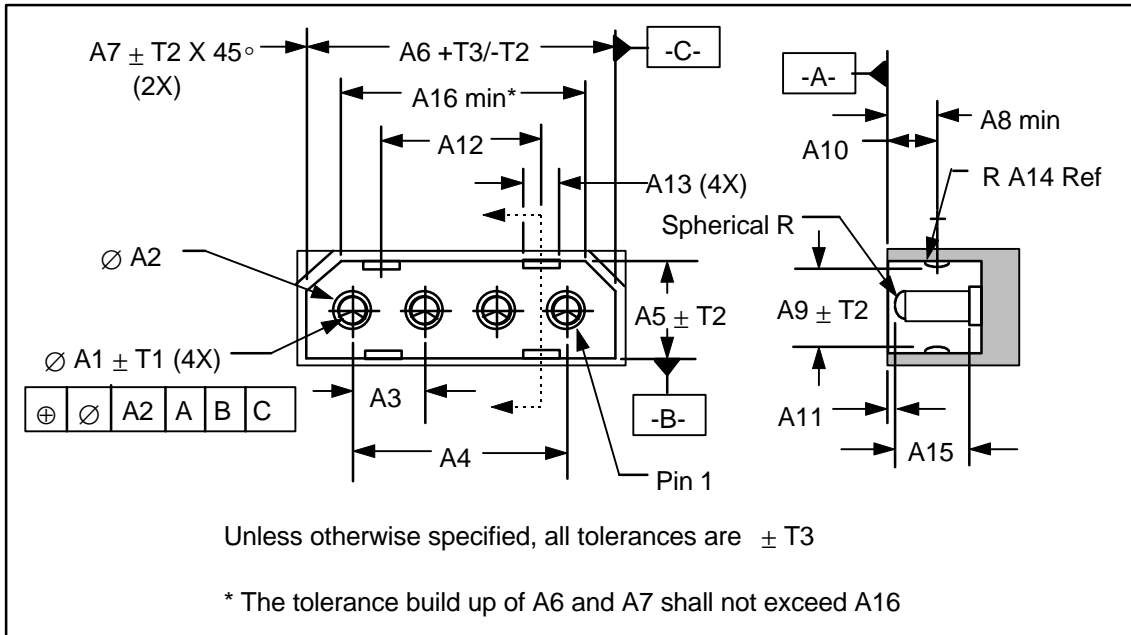
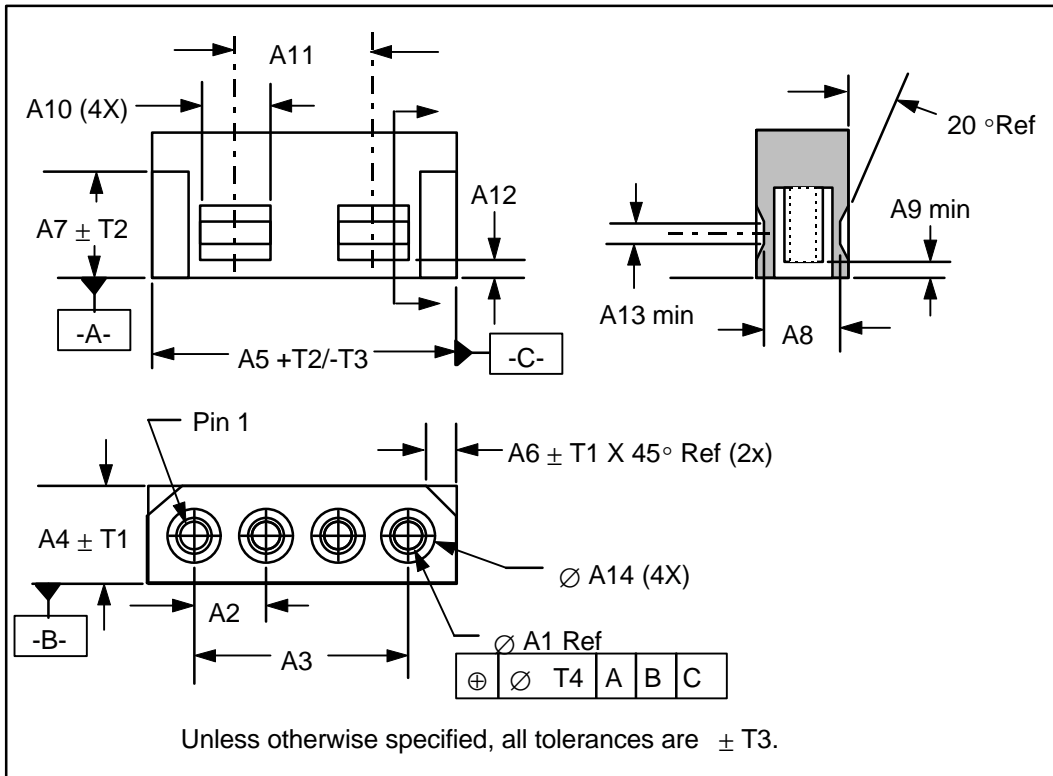


Figure A.8 – Device 4-pin power header

Table A.10 – Device 4-pin power header

Dimension	Millimeters	Inches
A 1	2.10	0.083
A 2	3.50	0.138
A 3	5.08	0.200
A 4	15.24	0.600
A 5	6.60	0.260
A 6	21.32	0.839
A 7	1.65	0.065
A 8	7.50	0.295
A 9	6.00	0.236
A 10	2.45	0.096
A 11	1.00	0.039
A 12	11.18	0.440
A 13	3.80	0.150
A 14	3.00	0.118
A 15	5.10	0.201
A 16	17.80	0.701
T 1	0.04	0.0016
T 2	0.15	0.006
T 3	0.25	0.010



**Figure A.9 – 4-pin power cable connector**

**Table A.11 – 4-pin power cable connector**

Dimension	Millimeters	Inches
A 1	2.03	0.080
A 2	5.08	0.200
A 3	15.24	0.600
A 4	6.35	0.250
A 5	21.00	0.827
A 6	1.78	0.070
A 7	7.87	0.310
A 8	5.51	0.217
A 9	1.19	0.047
A 10	5.08	0.200
A 11	11.18	0.440
A 12	1.19	0.047
A 13	2.00	0.079
A 14	4.06	0.160
T 1	0.10	0.004
T 2	0.15	0.006
T 3	0.25	0.010
T 4	0.60	0.024

**Table A.12 – 4-pin power connector pin assignments**

Power line	Pin
+12 volts	1
+12 volt return	2
+5 volt return	3
+5 volts	4

### A.2.1 Mating performance

Mating force should be 3.85 lbs (1.75 kg) maximum per contact.

Unmating force should be 0.25 lbs (113.5 g) minimum per contact.

### A.3 Unitized connectors

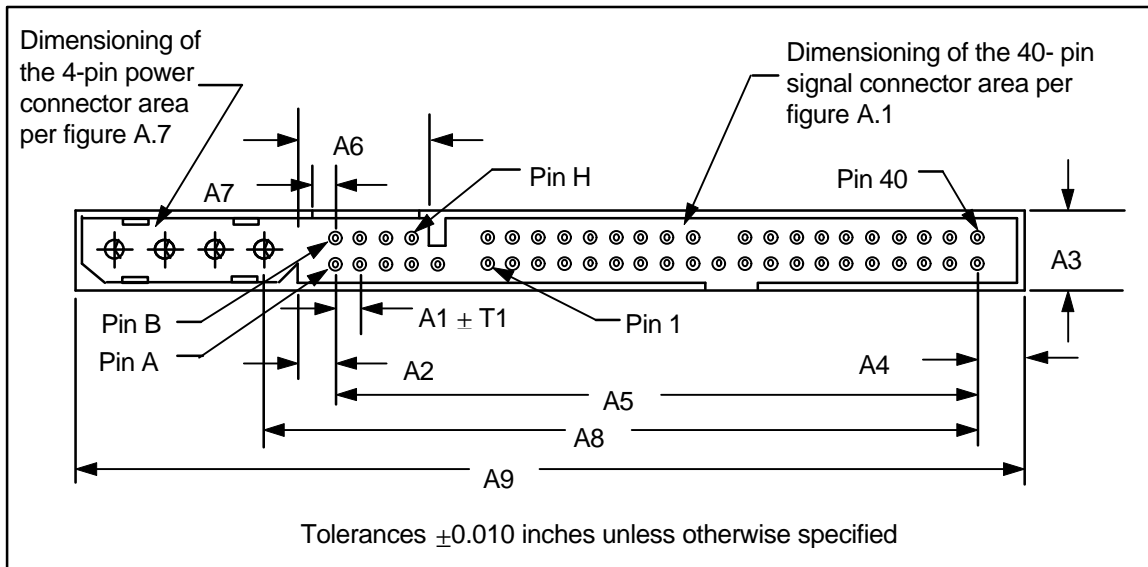
The 40-pin I/O signal header and the 4-pin power connector may be implemented in one of two unitized connectors that provide additional pins for configuration jumpers. The dimensioning of the 40-pin I/O signal area shall be as defined in figure A.1 and the dimensioning of the 4-pin power connector area shall be as defined in figure A.8 for both unitized connectors.

The first of the unitized connectors is shown in figure A.10 with dimensions as shown in table A.13. The jumper pins, A through I, have been assigned as follows:

- E-F - CSEL
- G-H - Master
- G-H and E-F - Master with slave present
- No jumper - Slave
- A through D - Vendor specific
- I - reserved

The second of the unitized connectors is shown in figure A.11 with dimensions as shown in table A.14. The jumper pins, A through J, have been assigned as follows:

- A-B - CSEL
- C-D - Slave
- E-F - Master
- G through J - Vendor specific

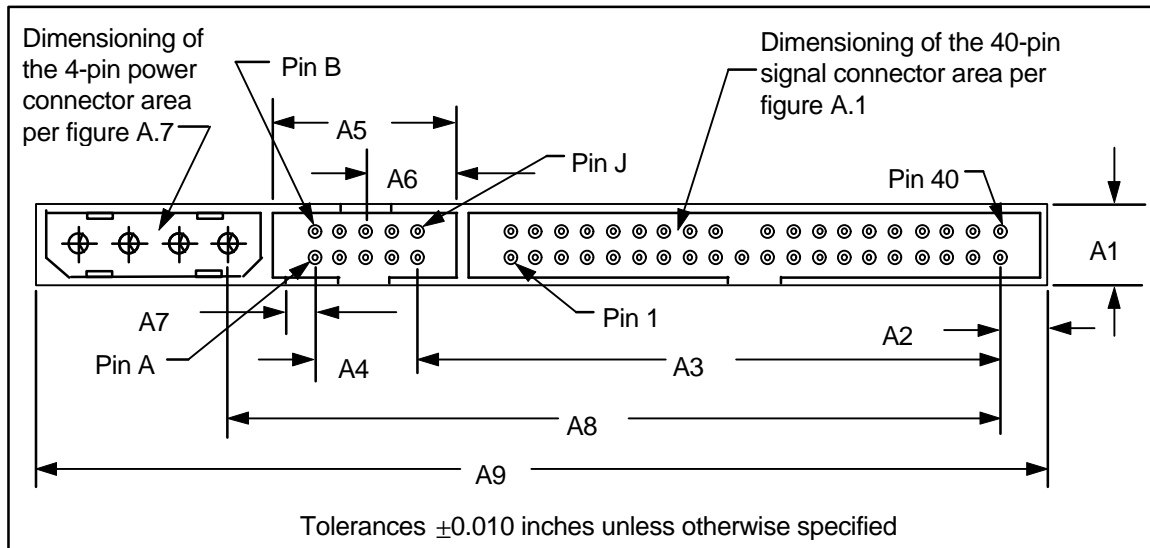


**Figure A.10– Unitized connector**



**Table A.13 – Unitized connector**

Dimension	Millimeters	Inches
A 1	2.54	0.100
A 2	4.06	0.160
A 3	8.40	0.331
A 4	5.26	0.207
A 5	63.50	2.500
A 6	13.54	0.533
A 7	2.54	0.100
A 8	70.825	2.788
A 9	95.50	3.760
T 1	0.15	0.006

**Figure A.11 – Unitized connector****Table A.14 – Unitized connector**

Dimension	Millimeters	Inches
A 1	8.51	0.335
A 2	5.51	0.217
A 3	57.15	2.250
A 4	10.16	0.400
A 5	17.88	0.704
A 6	8.94	0.352
A 7	2.54	0.100
A 8	75.29	2.964
A 9	100.33	3.950

#### A.4 50-pin connector

An alternative connector is often used for 2 1/2 inch or smaller devices. This connector is shown in figure A.12 with dimensions shown in table A.15. Signal assignments are shown in table A.16. Although there are 50 pins in the plug, a 44-pin mating receptacle may be used.

Pins E, F, and 20 are keys and are removed.

Some devices may utilize pins A, B, C, and D for option selection via physical jumpers. If a device uses pins A, B, C, and D for device selection, when no jumper is present the device should be designated as Device

0. When a jumper is present between pins B and D, the device should respond to the CSEL signal to determine the device number.

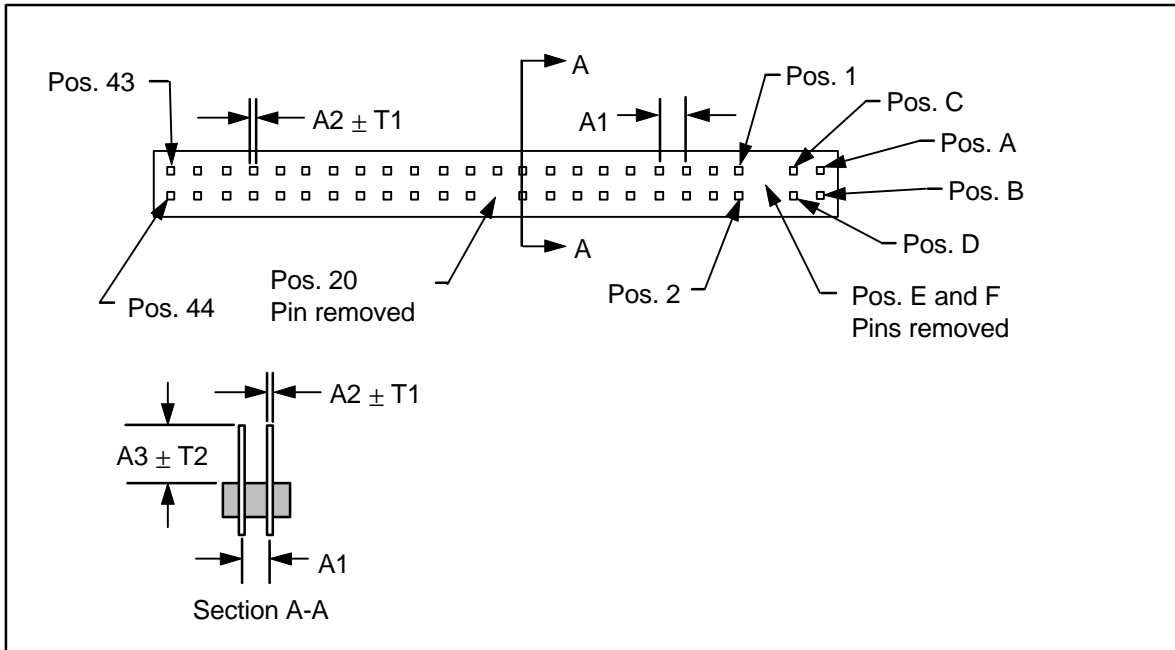


Figure A.12 – 50-pin connector

Table A.15 – 50-pin connector

Dimension	Millimeters	Inches
A 1	2.00	0.079
A 2	0.50	0.020
A 3	3.86	0.152
T 1	0.05	0.002
T 2	0.20	0.008

**Table A.16 – Signal assignments for 44-pin connector**

Signal name	Connector contact	Conductor		Connector contact	Signal name
Vendor specific (see note)	A			B	Vendor specific (see note)
Vendor specific (see note)	C			D	Vendor specific (see note)
(keypin) (see note)	E			F	(keypin) (see note)
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY- :HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY- :DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic) (see note)	41	41	42	42	+5 V (Motor) (see note)
Ground(return) (see note)	43	43	44	44	Reserved - no connection (see note)

NOTE – Pins that are additional to those of the 40-pin cable.

## A.5 68-pin PCMCIA connector

This clause defines the pinouts used for the 68-pin alternative connector for the AT Attachment Interface. This connector is defined in the PCMCIA PC Card Standard. This clause defines a pinout alternative that allows a device to function as an AT Attachment Interface compliant device, while also allowing the device to be compliant with PC Card ATA mode defined by PCMCIA. The signal protocol allows the device to identify the host interface as being 68-pin as defined in this standard or PC Card ATA.

To simplify the implementation of dual-interface devices, the 68-pin AT Attachment Interface maintains commonality with as many PC Card ATA signals as possible, while supporting full command and signal compliance with this standard.

The 68-pin pinout shall not cause damage or loss of data if a PCMCIA card is accidentally plugged into a host slot supporting this interface. The inversion of the RESET- signal between this standard and PCMCIA interfaces prevents loss of data if the device is unable to reconfigure itself to the appropriate host interface.

### A.5.1 Signals

This specification relies upon the electrical and mechanical characteristics of PCMCIA and unless otherwise noted, all signals and registers with the same names as PCMCIA signals and registers have the same meaning as defined in PCMCIA.

The PC Card-ATA specification is used as a reference to identify the signal protocol used to identify the host interface protocol.

### **A.5.2 Signal descriptions**

Any signals not defined below shall be as described in this standard, PCMCIA, or the PC Card ATA documents.

Table A.17 shows the signals and relationships such as direction, as well as providing the signal name of the PCMCIA equivalent.

Table A.17 – Signal assignments for 68-pin connector

Pin	Signal	Hst	Dir	Dev	PCMCIA	Pin	Signal	Hst	Dir	Dev	PCMCIA
1	Ground	x	→	x	Ground	35	Ground	x	→	x	Ground
2	DD3	x	↔	x	D3	36	CD1-	x	←	x	CD1-
3	DD4	x	↔	x	D4	37	DD11	x	↔	x	D11
4	DD5	x	↔	x	D5	38	DD12	x	↔	x	D12
5	DD6	x	↔	x	D6	39	DD13	x	↔	x	D13
6	DD7	x	↔	x	D7	40	DD14	x	↔	x	D14
7	CS0-	x	→	x	CE1-	41	DD15	x	↔	x	D15
8			→	i	A10	42	CS1-	x	→	x(1)	CE2-
9	SELATA-	x	→	x	OE-	43			←	i	VS1-
10						44	DIOR-	x	→	x	IORD-
11	CS1-	x	→	x(1)	A9	45	DIOW-	x	→	x	IOWR-
12			→	i	A8	46					
13						47					
14						48					
15			→	i	WE-	49					
16	INTRQ	x	←	x	READY/ IREQ-	50					
17	Vcc	x	→	x	Vcc	51	Vcc	x	→	x	Vcc
18						52					
19						53					
20						54					
21						55	M/S-	x	→	x(2)	
22			→	i	A7	56	CSEL	x	→	x(2)	
23			→	i	A6	57			←	i	VS2-
24			→	i	A5	58	RESET-	x	→	x	RESET
25			→	i	A4	59	IORDY	o	←	x(3)	WAIT-
26			→	i	A3	60	DMARQ	o	←	x(3)	INPACK-
27	DA2	x	→	x	A2	61	DMACK-	o	→	o	REG-
28	DA1	x	→	x	A1	62	DASP-	x	↔	x	BVD2/ SPKR-
29	DA0	x	→	x	A0	63	PDIAG-	x	↔	x	BVD1/ STSCHG
30	DD0	x	↔	x	D0	64	DD8	x	↔	x	D8
31	DD1	x	↔	x	D1	65	DD9	x	↔	x	D9
32	DD2	x	↔	x	D2	66	DD10	x	↔	x	D10
33		x	←	x	WP/ IOIS16	67	CD2-	x	←	x	CD2-
34	Ground	x	→	x	Ground	68	Ground	x	→	x	Ground

## Key:

Dir = the direction of the signal between host and device.

x in the Hst column = this signal shall be supported by the Host.

x in the Dev column = this signal shall be supported by the device.

i in the Dev column = this signal shall be ignored by the device while in 68-pin mode.

o = this signal is Optional.

Nothing in Dev column = no connection should be made to that pin.

## NOTES –

1 The device shall support only one CS1- signal pin.

2 The device shall support either M/S- or CSEL but not both.

3 The device shall hold this signal negated if the device does not support the function.

#### **A.5.2.1 CD1- (Card Detect 1)**

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

#### **A.5.2.2 CD2- (Card Detect 2)**

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

#### **A.5.2.3 CS1- (Device chip select 1)**

Hosts shall provide CS1- on both the pins identified in table A.17.

Devices shall recognize only one of the two pins as CS1-.

#### **A.5.2.4 DMACK- (DMA acknowledge)**

This signal is optional for hosts and devices.

If this signal is supported by the host or the device, the function of DMARQ shall also be supported.

#### **A.5.2.5 DMARQ (DMA request)**

This signal is optional for hosts.

If this signal is supported by the host or the device, the function of DMACK- shall also be supported.

#### **A.5.2.6 IORDY (I/O channel ready)**

This signal is optional for hosts.

#### **A.5.2.7 M/S- (Master/slave)**

This signal is the inverted form of CSEL. Hosts shall support both M/S- and CSEL though devices need only support one or the other.

Hosts shall assert CSEL and M/S- prior to applying VCC to the connector.

#### **A.5.2.8 SELATA- (Select 68-pin ATA)**

This pin is used by the host to select which mode to use, PC Card-ATA mode or the 68-pin mode defined in this standard. To select 68-pin ATA mode, the host shall assert SELATA- prior to applying power to the connector, and shall hold SELATA- asserted.

The device shall not re-sample SELATA- as a result of either a hardware or software reset. The device shall ignore all interface signals for 19 ms after the host supplies Vcc within the device's voltage tolerance. If SELATA- is negated following this time, the device shall either configure itself for PC Card-ATA mode or not respond to further inputs from the host.

### **A.5.3 Removability considerations**

This specification supports the removability of devices that use the protocol. As removability is a new consideration for devices, several issues need to be considered with regard to the insertion or removal of devices.

### A.5.3.1 Device recommendations

The following are recommendations to device implementors:

- CS0-, CS1-, RESET-, and SELATA- signals be negated on the device to prevent false selection during hot insertion.
- Ignore all interface signals except SELATA- until 19 ms after the host supplies VCC within the device's voltage tolerance. This time is necessary to de-bounce the device's power on reset sequence. Once in the 68-pin mode as defined in this standard, if SELATA- is ever negated following the 19 ms de-bounce delay time, the device disables itself until VCC is removed.
- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register are used to prevent unexpected removal of the device or media.

### A.5.3.2 Host recommendations

The following are recommendations to host implementors:

- Connector pin sequencing to protect the device by making contact to ground before any other signal in the system.
- SELATA- to be asserted at all times.
- All devices reset and reconfigured to the same base address each time a device at that address is inserted or removed.
- The removal or insertion of a device at the same address to be detected so as to prevent the corruption of a command.
- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register used to prevent unexpected removal of the device or media.

## **Annex B** (informative)

### **Identify device data for devices with more than 1024 logical cylinders**

#### **B.1 Definitions and background information**

The original IBM PC BIOS (Basic Input/Output System) imposed several restrictions on the support of devices, and these have been incorporated into many higher level software products. One such restriction limits the capacity of a device. BIOS software cannot support a device with more than 1,024 cylinders, 16 heads, and 63 sectors per track without translating an input logical geometry to a different output logical geometry. The maximum addressable capacity of a device that does not require BIOS translation is 1,032,192 sectors.

These rules allow BIOSes using bit shifting translation to access 15,481,935 (16,383\*15\*63) sectors, and BIOSes using LBA assisted translation to access 16,450,560 (1024\*255\*63) sectors. Extended BIOS functionality is defined in the ANSI Technical Report Enhanced BIOS Services for Disk Drives, which describes new services provided by BIOS firmware to support ATA hard disks up to 16 mega-terra-sectors.

#### **B.2 Cylinder, head, and sector addressing**

BIOSs and other software that operate a device in CHS translation employ a combination of IDENTIFY DEVICE data words 1, 3, 6, words 53-58, and words 60-61 to ascertain the appropriate translation to use and determine the capacity of a device.

Maximum compatibility is facilitated if the following guidelines are used. These guidelines limit the values placed into words 1, 3, 6, 53-58, and 60-61. Accessing beyond 15,481,935 sectors should be performed using LBA.

##### **B.2.1 Word 1**

For devices with a capacity less than or equal to 1,032,192 sectors, if IDENTIFY DEVICE data word 1 (Default Cylinders) does not specify a value greater than 1,024, then no guideline is necessary.

If a device is greater than 1,032,192 sectors, but less than or equal to 16,514,064 sectors, the maximum value that can be placed into this word is determined by the value in word 3 as shown in table B.1.

If a device is greater than 15,481,935 sectors and supports CHS, this word should contain 16,383 (3FFFh).

The INITIALIZE DEVICE PARAMETERS command does not change this value.

The value in this word is changed by the SET MAX ADDRESS command.



**Table B.1 – Word 1 value for devices between 1,032,192 and 16,514,064 sectors**

Value in word 3		Maximum value in word 1	
1	1h	65,535	FFFFh
2	2h	65,535	FFFFh
3	3h	65,535	FFFFh
4	4h	65,535	FFFFh
5	5h	32,767	7FFFh
6	6h	32,767	7FFFh
7	7h	32,767	7FFFh
8	8h	32,767	7FFFh
9	9h	16,383	3FFFh
10	Ah	16,383	3FFFh
11	Bh	16,383	3FFFh
12	Ch	16,383	3FFFh
13	Dh	16,383	3FFFh
14	Eh	16,383	3FFFh
15	Fh	16,383	3FFFh
16	10h	16,383	3FFFh

**B.2.2 Word 3**

IDENTIFY DEVICE data word 3 (Default Heads) does not specify a value greater than 16. If the device has less than or equal to 8,257,536 sectors, then set word 3 to 16 heads. If the device has more than 16,514,064 sectors, then set word 3 to 15 heads. If this value is set to 16 when the device has more than 16,514,064 sectors, some systems will not boot some operating systems.

The INITIALIZE DEVICE PARAMETERS command does not change this value.

**B.2.3 Word 6**

If the device is above 1,032,192 sectors then the value should be 63. This value does not exceed 63 (3Fh).

The INITIALIZE DEVICE PARAMETERS command does not change this value.

**B.2.4 Use of words 53 through 58**

Devices with a capacity over 1,032,192 sectors implement words 53-58. Devices with a capacity less than or equal to 1,032,192 sectors may also implement these words. These words define the address range for all sectors accessible in CHS mode under 16,514,064. The product of word 54, word 55, and word 56 must not exceed 16,514,064.

**B.2.5 Words 60-61**

IDENTIFY DEVICE data words 60-61 contain a 32-bit value that is equal to the total number of sectors that can be accessed using LBA. If the device is less than or equal to 15,481,935 sectors, this value should be the product of words 1, 3, and 6. Setting the total number of LBA sectors in this manner reduces the probability of conflicting device capacities being calculated by different operating systems.

### **B.3 Orphan sectors**

The sectors, if any, between the last sector addressable in CHS mode and the last sector addressable in LBA mode are known as "orphan" sectors. A device may or may not allow access to these sectors in CHS addressing mode.

The values in words 1, 3, and 6 are selected such that the number of orphan sectors is minimized. Normally, the number of orphan sectors should not exceed ( [word55] x [word56] - 1 ). However, the host system may create conditions where there are a larger number of orphans sectors by issuing the INITIALIZE DEVICE PARAMETERS command with values other than the values in words 3 and 6. If the recommendation in B.2.5 is followed, there will be no orphan sectors and problems associated with new operating systems calculating a different device size from older operating systems will be minimized.

## Annex C (informative) Signal integrity

### C.1 Introduction

The ATA bus (a.k.a. IDE bus) is a disk drive interface originally designed for the ISA Bus of the IBM PC/AT™. With the advent of faster devices the definition of the bus has been expanded to include new operating modes. Each of the PIO modes, numbered zero through four, is faster than the one before (higher numbers translate to faster transfer rates). PIO modes 0, 1, and 2 correspond to transfer rates for the interface as was originally defined with maximum transfer rates of 3.3, 5.2, and 8.3 MB/s, respectively. PIO mode 3 defines a maximum transfer rate of 11.1 MB/s, and PIO mode 4 defines a maximum rate of 16.7 MB/s. Additionally, Multiword DMA and Ultra DMA modes have been defined. Multiword DMA mode 0, 1, and 2 have maximum transfer rates of 4.2, 13.3, and 16.7 MB/s, respectively. Ultra DMA modes 0, 1, and 2 have maximum transfer rates of 16.7, 25, and 33.3 MB/s, respectively.

With the increases in speed the weaknesses of the original cabling scheme has become apparent. System manufacturers, chipset designers, and device manufacturers must all take measures to insure that signal integrity is maintained on the bus. The areas of concern are:

- a) ringing due to improper termination;
- b) crosstalk between signals;
- c) bus timing.

The intended audience for this annex is digital and analog engineers who design circuits interfacing to the ATA bus. Familiarity with this standard and a basic understanding of circuit theory is assumed.

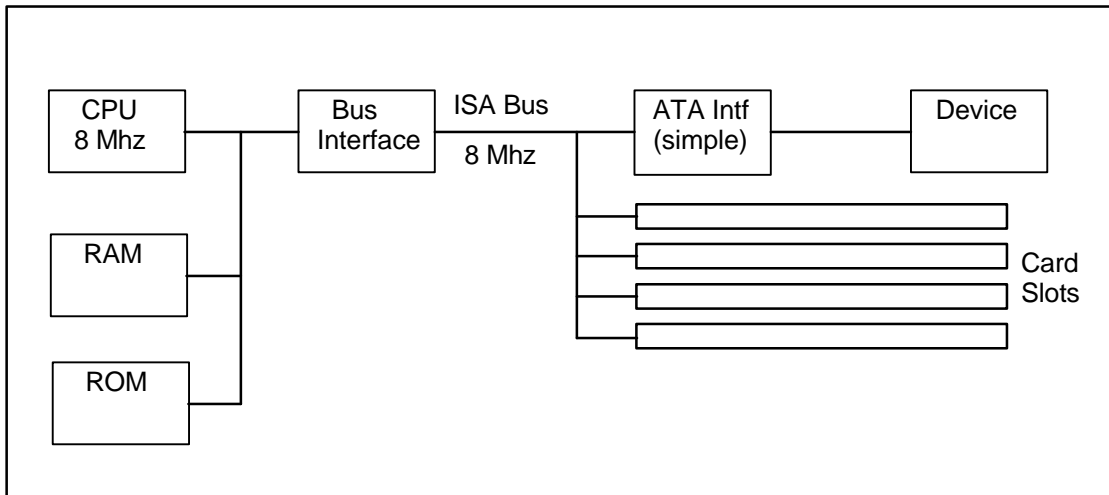
#### C.1.1 The problems

Early implementations of the bus used LS-TTL parts to drive an 18-inch cable. The slow edges of LS-TTL and the short cable length worked well at the time. PIO modes 3 and 4 demand higher performance. In an effort to cut cycle times, edge rates have inadvertently been increased, causing ringing on the cable and increased crosstalk between adjacent signals.

When a host adapter was little more than a few buffers and some gates there was no issue with host adapter timing. With the advent of local bus architectures and faster transfer rates, timing issues have become more important. Propagation delay with worst-case loads must now be taken into account when designing host adapters.

One of the frequently asked questions is, "Why are problems with ringing on the bus seen now when they were not seen before?" The answer is in the edge speed of the logic. How the edge speed changed may be found by looking at the history of the IBM PC.

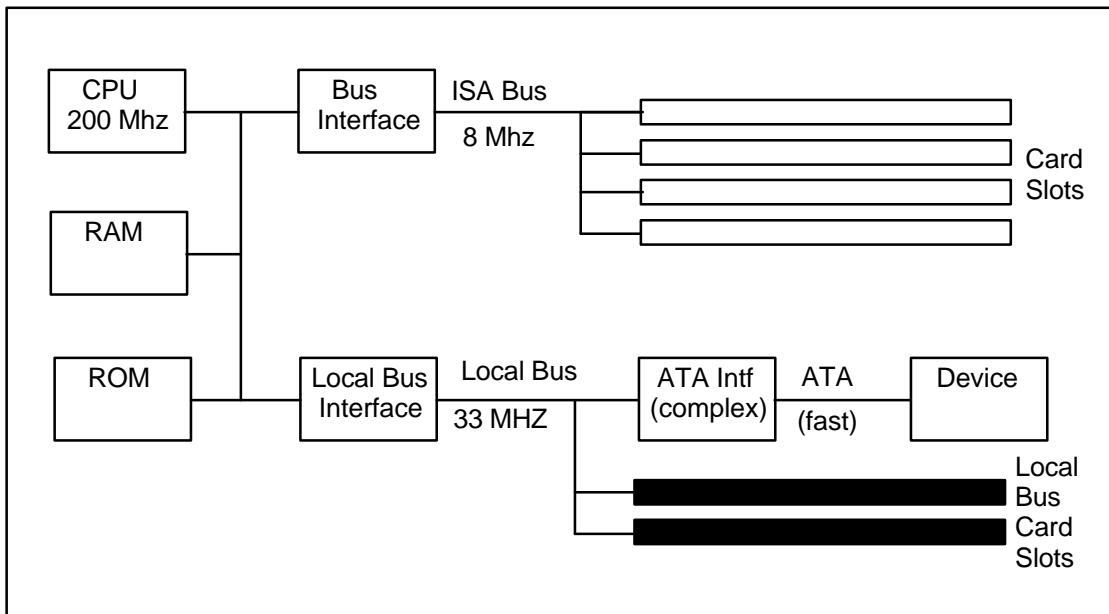
When the IBM PC/AT™ was introduced in 1983, the 8 MHz 80286 processor quickly became the dominant platform. The AT bus (now called the ISA bus) became standardized around an 8 MHz processor speed. When the first disk drive was introduced a few years later, the drive was designed as a simple extension of the bus leading to the name "AT Attachment" interface (see figure C.1). The idea was to remove the disk drive controller electronics from the PC and place them on the drive instead. What remained on the PC was a pair of bi-directional data buffers and an address decoder. This simple interface was most often implemented with a pair of 74LS245 buffers and a programmable logic device such as a PAL. These TTL devices had rise and fall times in the 5 to 6 ns range. Although this was fast enough to cause some ringing on the bus, it was not so severe as to prevent millions of successful system implementations.



**Figure C.1 – Original IBM PC/AT architecture**

The architecture of modern PCs has changed from the original PC/AT™. As the processor speed increased it became necessary to separate the processor bus from the ISA bus (see figure C.2). To maintain compatibility the ISA bus continues to run at an 8 MHz rate. Processors have increased beyond 200 MHz, and their associated busses have increased from 8 MHz to 33 MHz and above.

Devices have also increased in speed. The increase in rotational speed and linear bit density has increased the rate at that data comes off the heads, and the presence of cache on the device makes data available at the access rates of RAM. This has created a data bottleneck at the ISA bus. The device is faster, the processor is faster, but the data can't be moved from one to the other any faster.



**Figure C.2 – Modern PC architecture**

This bottleneck inspired the invention of new, faster interfaces to the processor. Local busses are designed to run at the speed of the processor bus. Two local bus standards have emerged, the VESA Local Bus (VLB) and the Peripheral Component Interconnect bus (PCI). These local busses have the potential for faster data transfer from the device to the processor.

To allow devices to transfer data faster, the standard had to be updated to allow faster transfer modes. These enhanced modes are still not as fast as a processor bus. To synchronize the data flow between 32-bit 33 MHz processor busses and slower 16-bit devices, a VLSI chip is required. Most of these bridge chips

were implemented with fast CMOS processes to achieve the required bus speeds. As a result the edge rates on the bus were often 1 to 2 ns, and sometimes less. These fast edges have aggravated the ringing on the bus to the point that system/device combinations fail to work.

In summary, the reason for signal integrity problems appearing now, when they were absent before, is the advent of faster transfer rates on the bus coupled with a change of IC process at the interface. The problems are not insurmountable, and the bus can be a robust, fast, and inexpensive interface.

### **C.1.2 The goals**

The recommendations in this annex make the following assumptions. The word “device” is used generically to describe hard disk drives and other peripheral devices on the bus.

- Backward compatibility must be maintained. Old devices must work with new host adapters, and old host adapters must work with new devices.
- This standard must be followed as closely as possible. Without this, solutions implemented by different manufacturers will tend to diverge, creating incompatible systems.
- Solutions must be simple and inexpensive. The market for these products is very cost sensitive.

## **C.2 Termination**

When analyzing the bus, the standard 18-inch ribbon cable used to connect devices must be considered in three different areas of frequency. At low frequencies it is a lumped capacitive load; higher in frequency it is a lumped LCR circuit; and at high frequencies it is a transmission line with distributed parameters. At standard transfer rates both the LCR circuit and distributed model apply.

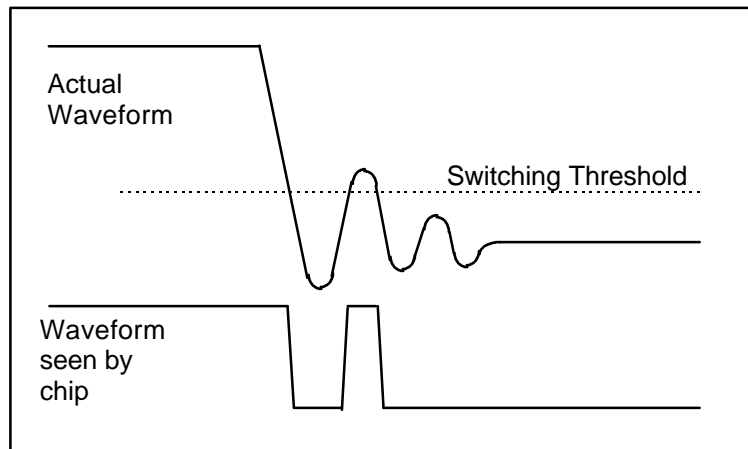
The cable used in most systems is a PVC-coated 40-conductor ribbon cable with the conductor spacing at 0.05 inches on center. This cable is modeled as a transmission line with a typical characteristic impedance of 110 ohms and propagation velocity of 60% c when connected in a ground-signal-ground configuration. When there are fewer grounds the characteristic impedance is higher. For the data lines adjacent to ground lines the characteristic impedance is about 160 ohms. The 110 ohm case applies to data strobes.

### **C.2.1 The problem**

Many users experienced problems with early implementations of PIO mode 3 devices and hosts. Most failures in the systems observed were attributed to signal integrity problems on the control lines that go from the host to the device. The problem appears most frequently as ringing on the DIOR- (during read commands) and DIOW- (during write commands) lines.

During a read cycle when DIOR- is asserted, it is possible for the ringing to create a short duration negation pulse (see figure C.3). This pulse occurs early in the read cycle. Inside the interface portion of the data path controller chip is a FIFO buffer that contains the data to be read. The extra pulse on the DIOR- line advances the FIFO pointer by one. This results in losing one word of data. The host system read operation therefore receives one word too few, and the remaining bytes are shifted. A typical data word (Wn) sequence might look like . . .W7, W8, W9, W11, W12 . . . Notice that word 10 is missing from the returned data. This also means that the host tries to read one more word from the device than the device has remaining in the host's buffer. Depending on the implementation of the BIOS, this locks up the system or simply returns a byte of random data at the end of the sector transfer.

Pulse slivers due to ringing on the DIOW- line cause a similar problem during write transfers. The pulse sliver advances the FIFO pointer by one, writing an extra word of random data into the FIFO. Subsequent data bytes are shifted by one word. A typical stored data word (Wn) sequence on the device might look like . . . W7, W8, W9, XX, W10, W11 . . . In this example an extra word was inserted during the write cycle for word 10. From the device's point of view, the host is trying to write 514 bytes rather than the expected 512 bytes. The device throws away the final word and may flag an error. A properly written BIOS detects this error and indicates a problem to the user.



**Figure C.3– Typical ringing on bus and its effect**

These are only two examples of a systemic problem. Ringing on any control signal, and possibly on data lines, may cause system failures or data loss. To address this problem it is necessary to examine the circuit structure of the bus.

Figure C.4 shows the seven basic driver/receiver structures that appear in bus interfaces. The host circuitry appears on the left side of the diagram and the device circuitry appears on the right. The first circuit in figure C.4 shows the structure of the seven control lines that go from the host to the device. A SPICE model of the circuit can be designed if some assumptions are made about the circuitry at the host and device. Virtually all devices today use a CMOS VLSI chip as part of the bus interface. This high-impedance input is modeled with clamp diodes to supply and ground and a typical input capacitance of 8 pf. Since the ringing problem is worse with CMOS VLSI bridge chips at the source, the host is modeled as a voltage source with 1 ns edges, a 12 ohm output impedance, and clamp diodes to supply and ground. The ribbon cable is modeled as a 110 ohm transmission line. The resulting SPICE model appears in figure C.5.

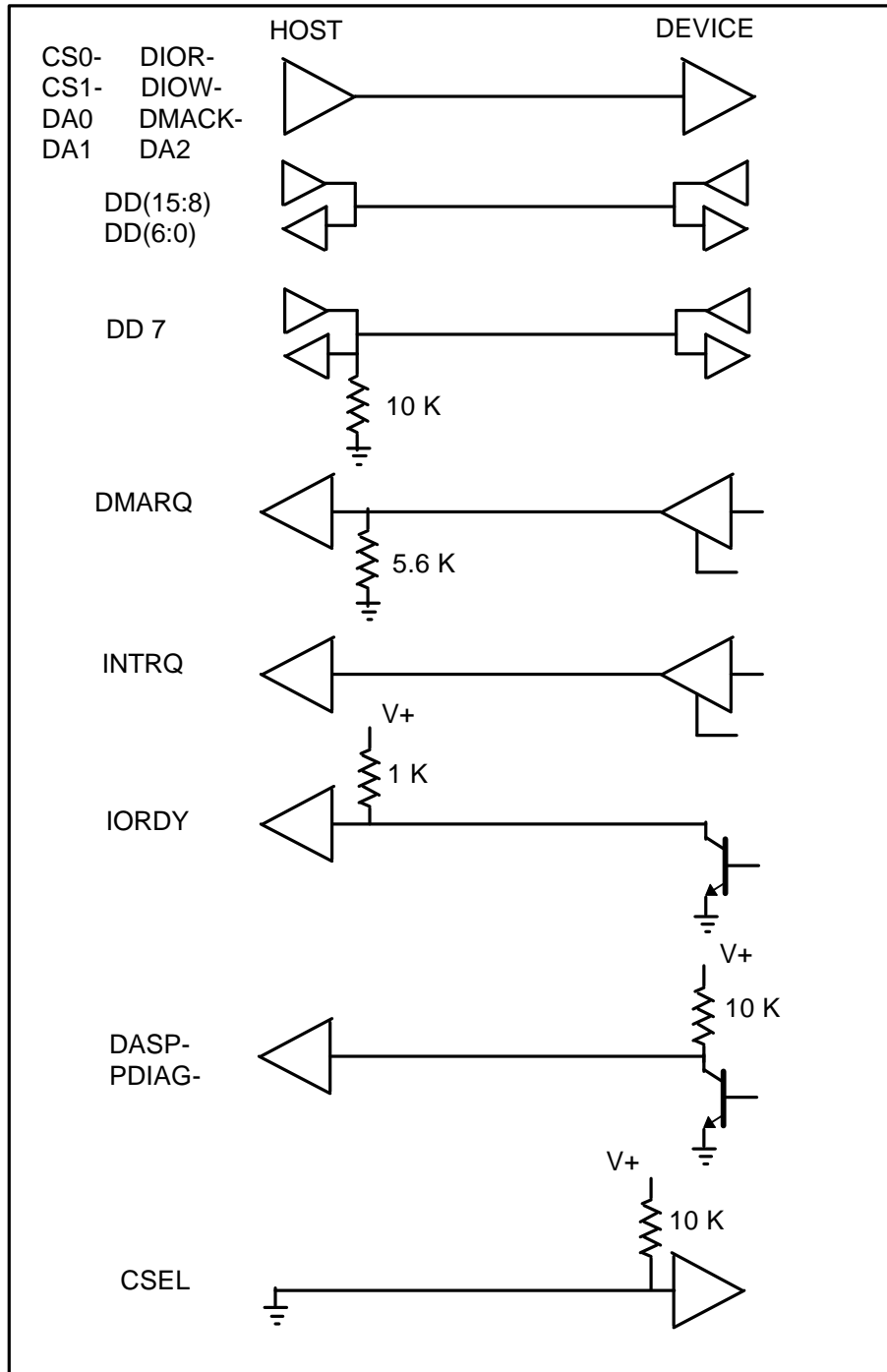
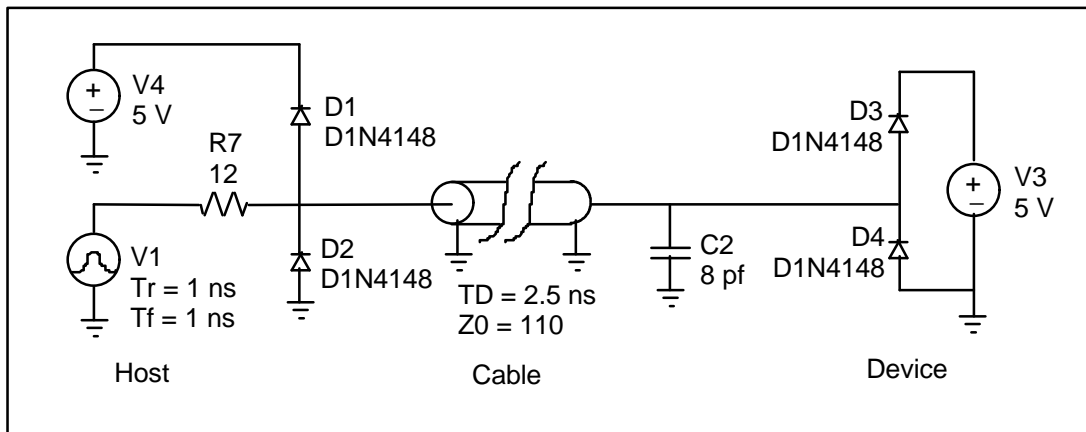
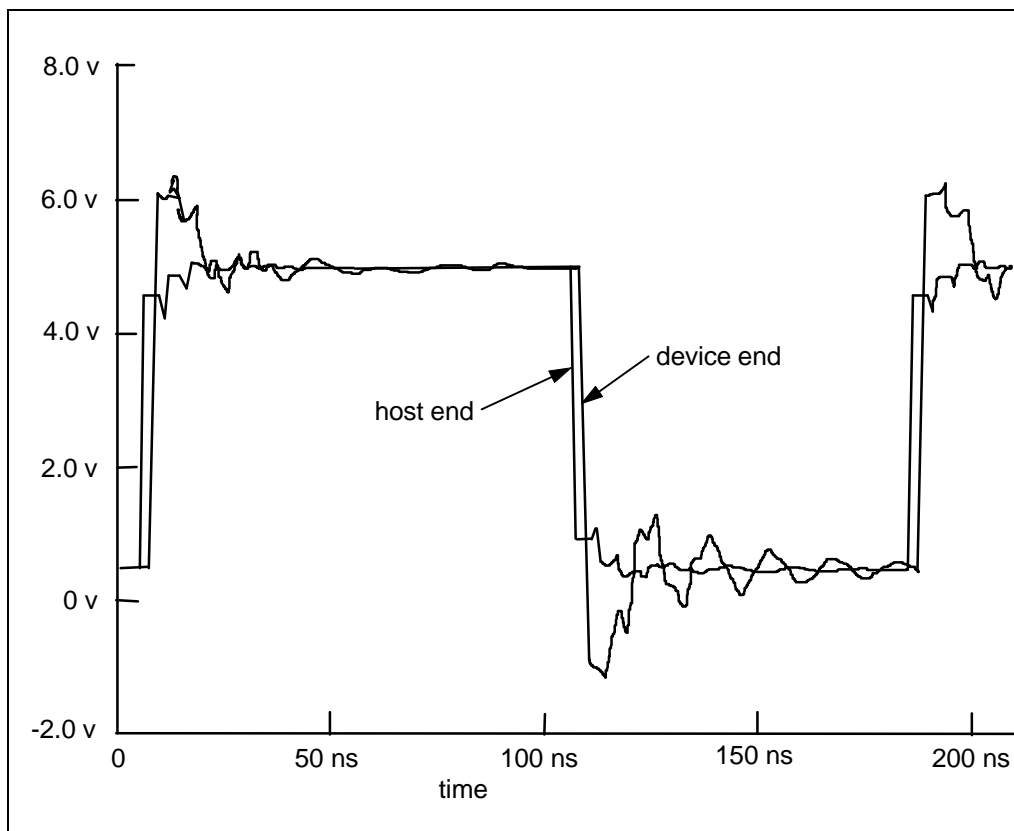


Figure C.4 – The seven basic driver/receiver structures



**Figure C.5– Schematic of SPICE simulation model**

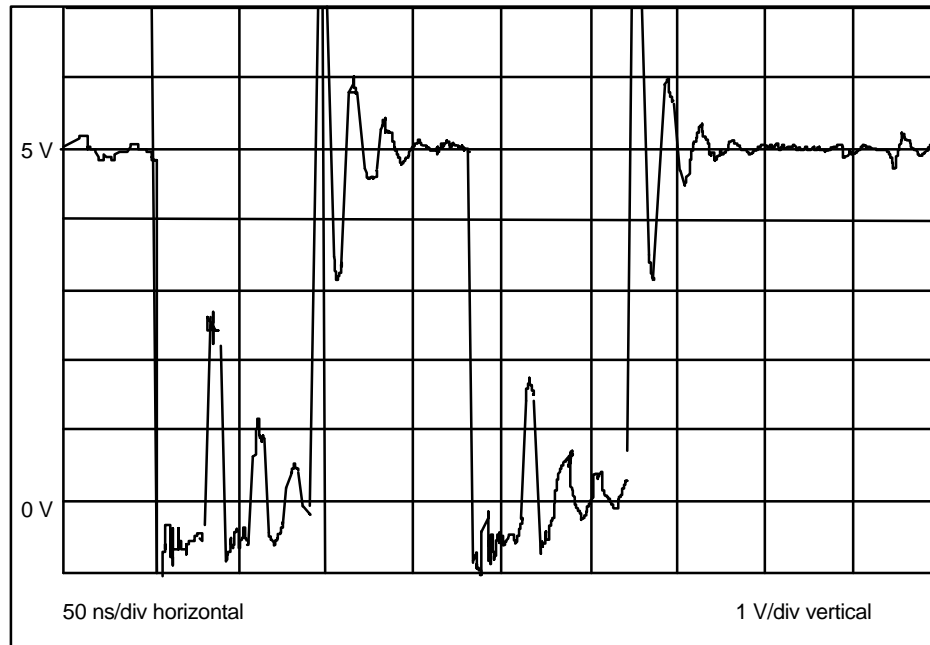


**Figure C.6– Simulation waveforms at host and device ends of cable**

The simulation results in figure C.6 show the waveforms at both the host and device ends of the cable. The signal at the device end has ringing of sufficient amplitude to cause false triggering of the device. This is confirmed by transmission line theory that indicates that ringing will occur whenever the source impedance is lower than the characteristic impedance of the cable, and the termination impedance is higher than the cable impedance. The greater the mismatch, the greater the amplitude of the ringing. The oscilloscope trace shown in figure C.7 confirms the results of the simulations.

In an effort to decrease propagation delay, some bridge chip manufacturers have increased the output drive current of the host in order to slew the output signal faster with the capacitive load of the cable. This has caused the edge rates and the output impedance to decrease, both of which increase the ringing at the device end of the cable. The oscilloscope trace in figure C.7 using a generic driver and receiver illustrates the problem of ringing that is a fundamental characteristic of the interface. This has not always been the case.





**Figure C.7 – Oscilloscope trace at device end of DIOR- signal on a typical system**

### C.2.2 What are the options?

The proper solutions are to terminate the transmission line and limit the frequency range of the signals. There are two termination possibilities: series or source, and parallel or load. Unfortunately, each of these solutions has problems of its own, and, regardless of the method of termination, ringing occurs in two-device configurations. The input impedance of devices is not infinite: they appear as a reactive load due as the input capacitance forms transmission line discontinuities.

Source termination is suited to situations where the signal is received at the far end of the line, and not in-between. But devices can be placed anywhere along a cable. The signals at the device in the middle of the cable have an initial step in their edges due to the series termination. Another problem with source termination is devices are not necessarily at one end of the cable.

Load termination has different problems. A 110 ohm termination at the device end causes excessive DC loading. The SCSI interface standard avoids ringing by requiring terminations at each end of the physical cable and having each device drive the cable with a current sink. However, SCSI configurations often have too many, too few, or improperly located terminations. Changing this standard to a user-installed termination scheme loses all backward compatibility and is therefore not considered to be a viable option.

One of the solutions used in the past to “fix” failing configurations has been to place a capacitor at the input of the device. Since the ringing is the result of a resonant system, adding purely reactive elements (capacitors and inductors) that simply change the frequency of oscillation is not recommended. These elements may fix a given configuration of a device and cable, but they really just move the interfering resonance peaks to a different frequency, solving the problem only for that particular configuration. Proper solutions include resistive elements to dissipate the energy stored in the transmission line.

No single solution meets the dual criteria of solving the ringing problem and being backward compatible with current systems. The suggested approach uses partial solutions in three different areas: partial termination at the host, partial termination at the device, and edge rate control at both the host and the device.

### C.2.3 Design goals

Before a solution can be designed the design goals must be explicitly stated. This leads to the question of "How much ringing is acceptable?" To answer this question the design and specification of the bus must be considered.

The bus was originally designed to use standard TTL signals. TTL was designed with built-in noise margin. All drivers are required to have a "low" (zero) signal level of 0.5 V or less, and a "high" (one) signal level of 2.4 V or more. All receivers are specified to accept any signal below 0.8 V as a logical zero and any signal above 2.0 V as a logical one. This results in a low-side noise margin of 0.3 V (0.8 - 0.5) and a high-side margin of 0.4 V (2.4 - 2.0). Signals between 0.8 V and 2.0 V are in no man's land, interpreted by the receiver as either a zero or a one. TTL compatible inputs typically use a switching threshold of 1.3 to 1.4 V.

Bus designers have long known that the noise margins of TTL are insufficient for signals passed on cables. To improve the noise margin inherent in TTL systems, hysteresis has been added to the receiver input. Hysteresis changes the input switching threshold depending on the present state of the logic output of the receiver. For example, if the receiver is currently in a zero state, it might require an input voltage of 1.7 V before changing to a one. Once in a one state, the receiver might require the input voltage to drop below 0.9 V before changing back to a zero. Modern design practice dictates that all signals passing across a bus be received with hysteresis.

It is desirable that, even with ringing, the input signal remain less than 0.5 V after a falling edge and remain above 2.4 V after a rising edge. With CMOS drivers only the falling edge is of concern. This is due to the input switching threshold of TTL (typically 1.4 V) being closer to ground than to the supply. It turns out that designing to the 0.5 V requirement is too restrictive, so the looser requirement of 0.8 V is used here. This relaxed requirement removes the noise margin inherent in TTL and depends on receiver hysteresis for proper operation. As input hysteresis has been the norm in device design for many years now, this limitation is not considered unreasonable.

Depending on system timing and other issues, a designer may elect to use a looser threshold of 0.9 V or a tighter one of 0.7 V. For these cases circuit simulation of the bus and receiver is done to verify the design. The resulting termination circuits have different values from those derived here.

### C.2.4 Source termination

A series resistor at the source (host) acts as a termination to the transmission line. When the value of the resistor matches the characteristic impedance of the cable (110 ohms) then the reflection returning from the load is reduced to zero. Resistor values less than the characteristic impedance will partially terminate the cable and reduce the reflection.

NOTE – This assumes that the output impedance of the driver is zero. In reality, an optimum match occurs when the output impedance and the series resistor together equal the cable impedance. This also assumes that the host is at the end of the cable. If the host is in the middle of the cable, then the host sees two cables in parallel and the optimum impedance match would be 55 ohms.

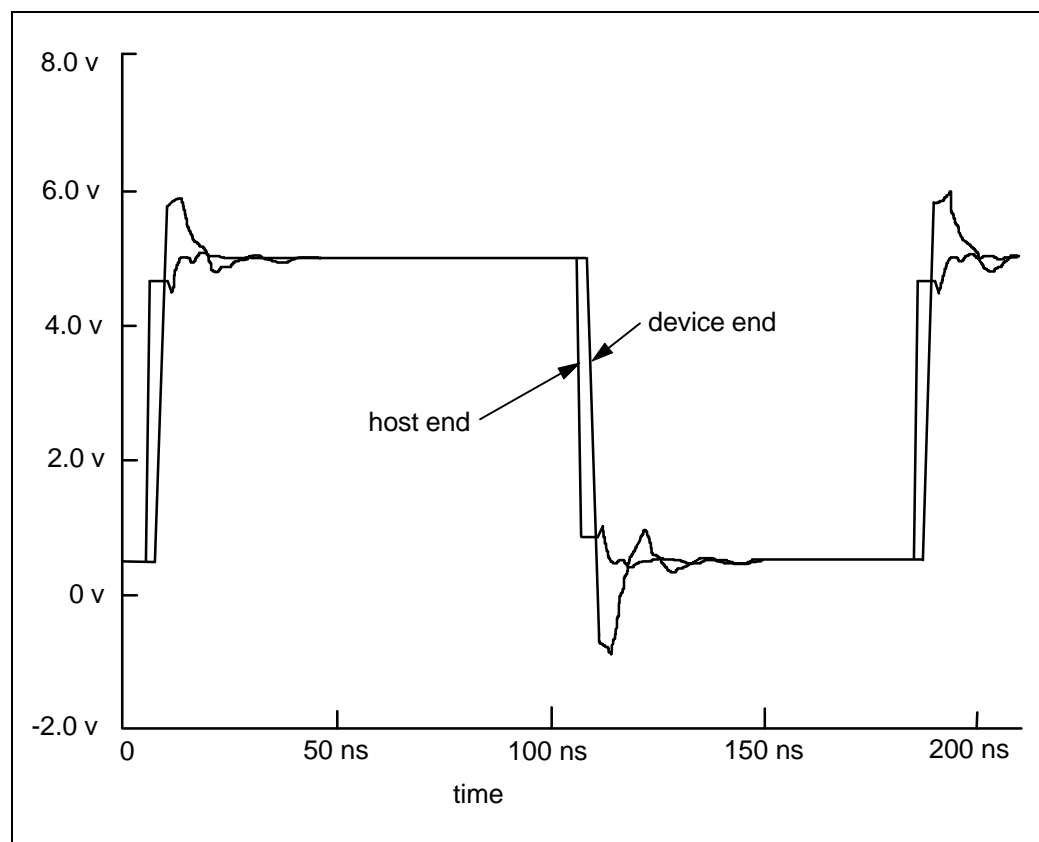
This standard requires that a source be able to sink 4 mA while maintaining a logical low output voltage of 0.5 V or less (see 4.3). For a TTL output the low output voltage is a combination of the saturation voltage and resistance of the pulldown transistor. For a CMOS output the pulldown transistor has no saturation voltage and is just a resistance. Adding a series resistor in the output of the driver causes the output logical zero voltage to increase with greater resistance. For example, if the unterminated logical zero output of the driver is 0.4 V, then a maximum series resistance of 25.0 ohms would be allowed ( $(0.5-0.4)/4\text{mA}$ ). This DC voltage drop requirement acts in opposition to the higher resistance values required for cable termination.

If it is assumed that an unterminated CMOS output driver can drive a logical low to 0.3 V at the rated sink current, then there is a 0.2 V to drop across the series resistor. This gives a maximum resistor value of 50

ohms. So the value of the series resistor depends on the CMOS output, the logical zero voltage, and the sink current.

Another consideration in selecting the value of the series resistor is the initial voltage on an edge. Assume a step function voltage source driving a transmission line through a series resistor. The initial amplitude of the edge at the input of the line is a voltage divider of the series resistor and the characteristic impedance. A receiving device can be near the source and the edge must go through logic thresholds. The worst case is a negative edge from 5 V and a control line of 110 ohms impedance. The attenuation of the voltage divider must be small enough to allow the edge to cross from 5 V through 0.8 V. Assuming that the leading edge will just reach 0 V at the source, An analysis shows the series resistor must be no larger than 21 ohms to meet this (  $(5.0)/(5.0-0.8)=(110+R)/110$  ). The closest standard five-percent value is 22 ohms. If one assumes that the leading edge will undershoot to 0.5V at the source, the resistor may be no larger than 33 ohms.

Is a 22 or 33 ohm resistor adequate for reducing the ringing? The simulation was repeated using the same model as shown in figure C.5 with a 33 ohm series resistor added. The results of that simulation appear in figure C.8. The ringing is significantly reduced from the previous simulation in figure C.6. Simulations were also performed on the model using a 22 ohm source resistor and similar reduction in ringing was observed.



**Figure C.8– Waveforms with 33 ohm series resistor at source**

For data lines there are two factors that make the considerations for selecting the series resistor significantly different. First, the characteristic impedance of a data line is higher since ground lines are farther away. Second, data lines are not edge sensitive, data settling time is the issue. The value of the series resistor is limited by the DC loading requirements, not the edge integrity. Adoption of this standard for DC loading allows further increase of the series resistance since the DC loading is the limiting factor. The characteristic impedance of lines adjacent to ground wires is the lowest of the data lines and is about 160 ohms; a higher value of series resistance is necessary to dampen reflections.

### C.2.5 Receiver termination

Device termination is more difficult than host termination. Viable solutions must work with one or two devices located anywhere along the cable. The host may or may not have termination. These and other considerations make device termination a multifaceted problem.

The first constraint is the maximum DC loading allowed. This standard requires that the host be capable of providing 400  $\mu\text{A}$  of current while in a logical one state. Assuming each device is allowed to take half of that amount, the minimum DC resistance allowed is 25K ohms.

NOTE – This assumes a CMOS output with a high output voltage of 5.0 V :  $5.0 \text{ V} / 200 \mu\text{A} = 25 \text{ K}\Omega$

For a 110 ohm transmission line, 25K ohms is as good as infinity. This means that any practical termination solution must not have significant DC loading.

One way of terminating the cable is with an “AC termination.” This is a simple RC network that provides termination for high-frequency signals but does not load the line at DC (see figure C.9). This circuit acts as both a cable termination and a filter for the ringing. The termination characteristics can be observed by looking at the ringing signal at the host when the circuit is connected or removed. When the circuit is in place, less energy is reflected back to the host, so the host waveform has less ringing. The lowpass filter characteristics of the circuit help decrease the amount of ringing presented to the interface circuitry of the device.

Although this may appear to be an unusual method of terminating the cable, it is not without precedent. The IEEE P996 committee recognized the problems inherent in the design of the IBM PC/AT™ bus and recommended a series RC termination for increased “data integrity and system reliability.” They suggested that the termination circuit be added to each end of the backplane or motherboard. The recommended values are 40 to 60 ohms for the resistor and 30 to 70 pf for the capacitor.

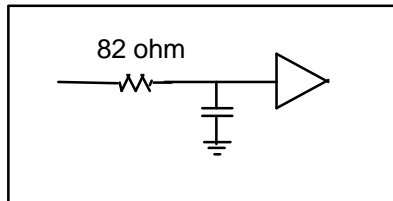
Deriving the optimum values for a bus AC termination circuit is difficult. The easiest way of determining the values is to perform a number of trial-and-error SPICE simulations for different host and device configurations. The recommended values are 82 ohms and 10 pf. Simulations show that capacitance values between 8 pf and 20 pf work well. Since the input capacitance of many interface chips is between 8 and 10 pf, a discrete capacitor is often unnecessary. This reduces the cost of implementation on the device. A conservative approach is to place pads so additional capacitance can be added if required.

Device manufacturers need to ensure that any partial termination circuits they implement present an effective capacitance of 20 pf or less. What is an effective capacitance? From a practical point of view, any circuit is valid provided the circuit does not increase the propagation delay of a worst-case cable. This is because systems manufacturers are counting on a certain cable delay in their design. The easiest way to answer the question of acceptability is to run a SPICE simulation and measure the delay. The simulation should be run twice: once with a simple 20 pf load, and again with the proposed termination circuit. If the resulting delay of the proposed termination circuit is less than or equal to that obtained with a 20 pf load, then the delay meets the criterion for acceptance. The recommended termination of 82 ohms and 10 pf passes the test.

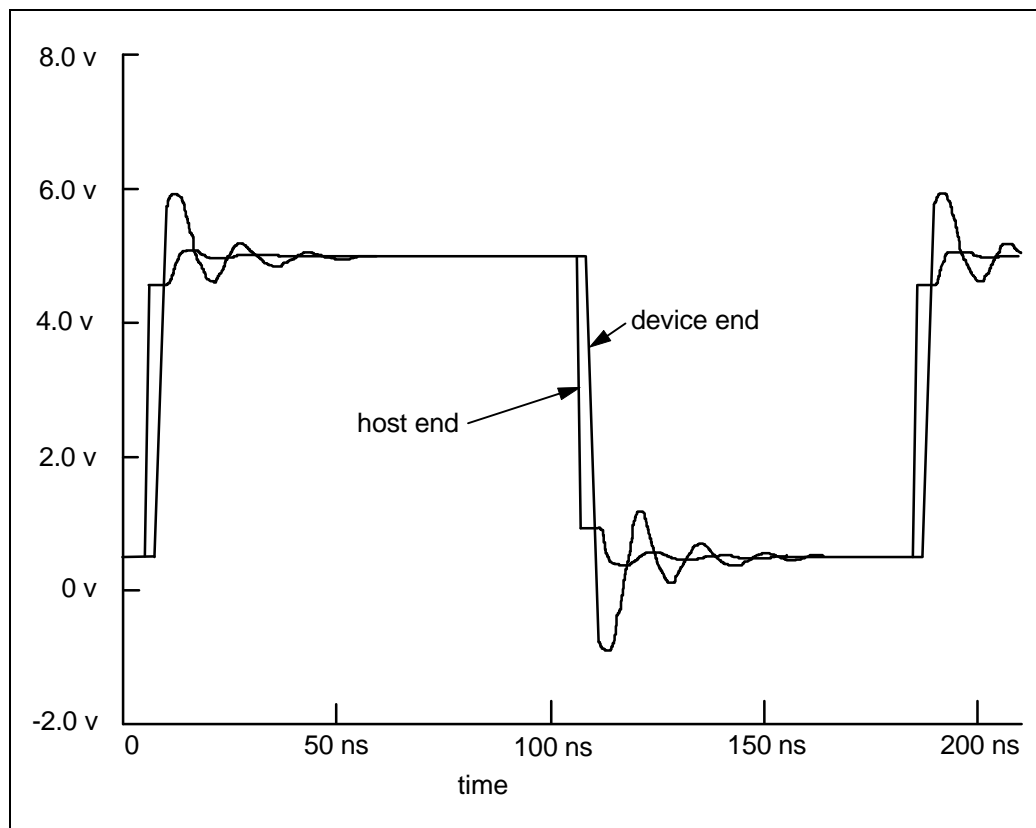
The major drawback of the RC termination circuit is that the circuit adds delay to the signal. Since this standard defines the timing at the input to the device (see clause 10), device manufacturers must ensure that their interface chip still works properly with the additional delay. The delay can be calculated for rising edges (2.0 V threshold) and falling edges (0.8 V threshold) with a fairly straightforward SPICE simulation. For the 82 ohm and 10 pf termination the delay is less than 1.5 ns (0.7 ns for the rising edge, 1.2 ns for the falling edge, derived from simulations ).

Will termination at both the host and the device “over-terminate” the transmission line? Figure C.10 shows the simulation results for device termination with no host termination, and figure C.11 shows the same simulation with a 33 ohm host termination added. It is clear that termination at both the host and the device results in the best signal integrity.

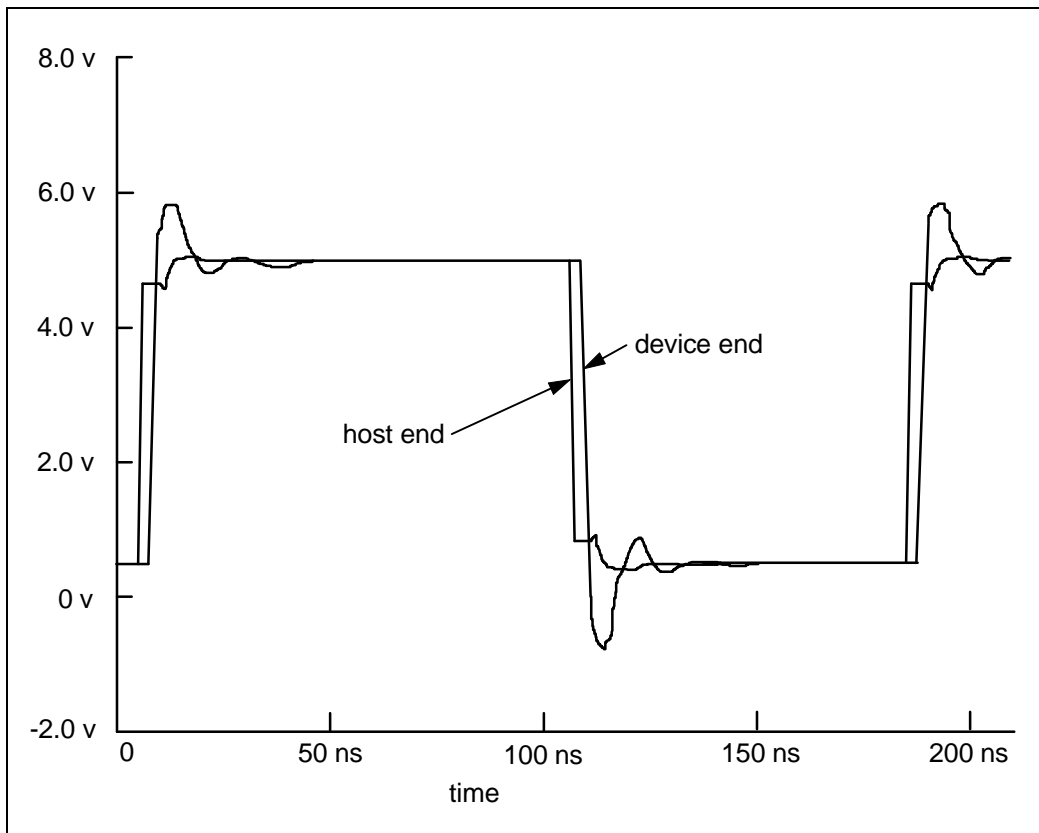
Another option for controlling ringing at the device is the use of a clamping circuit. Biased diodes have been shown to be excellent solutions, reducing the ringing to virtually zero. The advantage of clamp circuits is that they do not require any components in series with the signal, and therefore do not add any delay. This is particularly important for PIO mode 4 operation. The disadvantage of clamping circuits is that they take considerably more space on the circuit board and cost much more than passive elements. Some implementations have used clamping circuits on sensitive edge-triggered lines (such as DIOR- and DIOW-) and used passive terminations on less sensitive lines (such as data signals). Clamping circuits work well both with and without host-end termination and are worthy of further investigation.



**Figure C.9 – AC termination circuit at device end of cable**



**Figure C.10 – Device waveform with 82 ohm device termination and no host termination**



**Figure C.11 – Device waveform with 82 ohm device and 33 ohm host terminations**

### C.2.6 Edge rate control

This standard requires that all sources have a rise time of not less than 5 ns (see 4.3). The original intent of this requirement was to avoid transmission line problems on the bus. One of the common misconceptions is that limiting the rise time of the source to 5 ns will fix the ringing problem.

A rule-of-thumb for analog designers is that when the propagation delay of the cable exceeds one-quarter of the signal rise time, cable termination should be used.

NOTE – In reality this rule-of-thumb varies considerably. Various books use values of one-half, one-third, one-fifth, and even one over the square root of two times pi.

In the case of the bus, the worst case propagation delay of the cable is approximately 4 ns so by this rule rise times of less than 16 ns require termination. Many local bus to bridge chips available today have rise times of 1 to 2 ns, in violation of the requirement of 5 ns.

NOTE – Assuming 18-inch cable, 60% c velocity factor; two drives, each device having a maximum load of 25 pf.

This standard says that the rise time must be a minimum of 5 ns into a 40 pf load. The easiest way to implement this from a chip designer's point of view is to decrease the drive of the I/O cell until the timing requirement is met. Unfortunately, very few systems in the real world ever approach 40 pf. Although the cable and the devices have maximum capacitance specifications, these capacitance values are never seen by the host. At DC and low frequencies the cable looks like a capacitor. But at high frequencies (or fast edge rates) the cable appears as a transmission line. A properly terminated transmission line appears to be a resistor with no capacitance or inductance. The capacitance of the drives is changed by the transmission line and appears as anything but pure capacitance at the output of the host. As a result, real-world systems rarely see more than 25 pf of capacitive loading at the host. The reduced capacitance causes the I/O cell to

slew faster, creating rise times less than 5 ns. In actual system testing, it has been found that only a few systems have rise times slower than 3 ns.

The best solution is to use special I/O cells that have slew rate feedback to keep the rise time at 5 ns regardless of load. These are more difficult to design than conventional I/O cells and consume more die area. This could be a problem for interface chip designs that are already pad ring limited. Another approach is to use a conventional I/O cell that is designed to have 5 ns rise times into a 10 pf or 20 pf load. The total delay of the cell is greater for heavier loads, but the maximum delay is determined with SPICE modeling of a worst-case cable and load.

Rise time control is still an important tool for controlling ringing. Although rise time control is not the total solution, simulations show marked improvement between sources with 1 ns rise times and sources with 5 ns rise times. Slower rise times give the added benefit of reduced crosstalk. Figure C.12 shows the simulation with both host and device terminations with rise and fall times of 5 ns. A reduction in ringing is clearly seen.

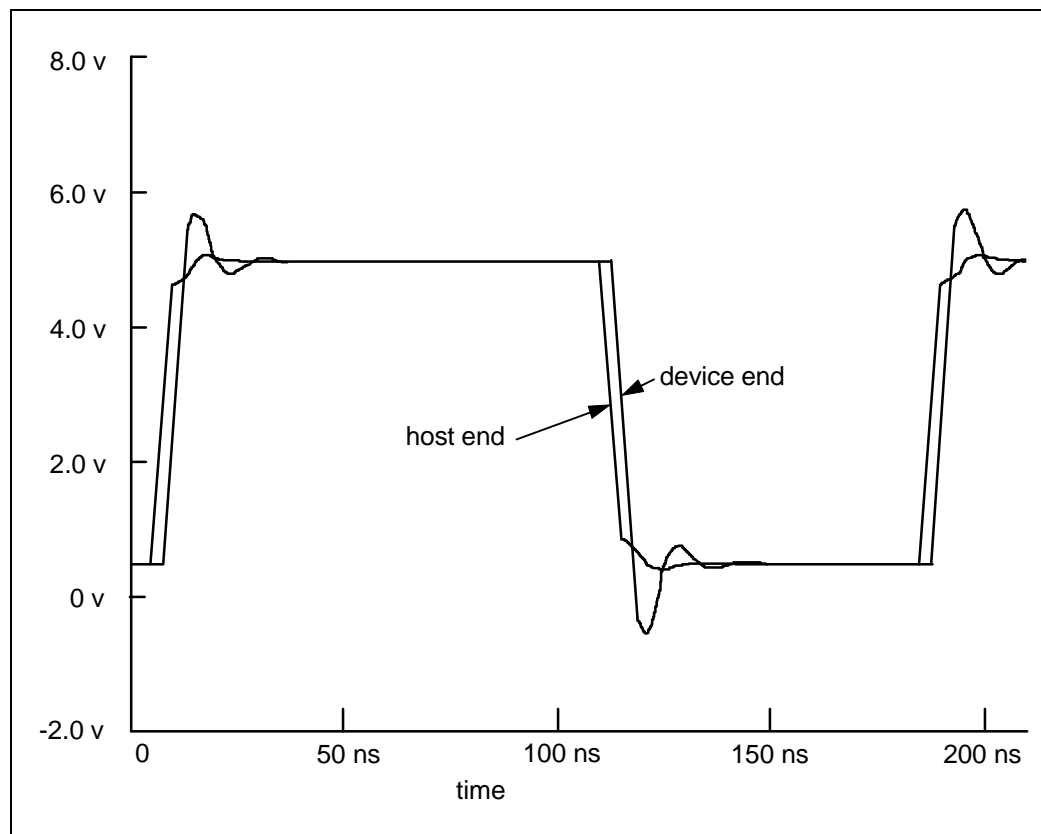


Figure C.12– Device waveform with both device and host terminations and 5 ns rise/fall times

### C.2.7 The solution: A combination

No one element (e.g., source termination, receiver termination, or rise time control) completely addresses the problem of ringing on the bus. The recommended solution is a combination of all three. Each element must be enough to exert some control over the ringing problem in order to maintain backward compatibility. With the faster transfer rates of PIO mode 4, DMA mode 2, and Ultra DMA mode 2 it is even more important to control undesired ringing on the bus. It is unlikely that any systems will function reliably without improvements from cooperation throughout the industry.

The above discussion only addressed a particular group of signals driven by the host and received by the device. There are other signals driven by the device and received by the host that are equally susceptible to ringing. These signals need termination, but in the opposite manner. The device inserts 22 or 33 ohm resistors in series with signals the device drives and the host has an RC (or just R) receiving end termination.

The data lines are different in several ways. First, they must move data bidirectionally. Second, they are not edge sensitive, ringing affects the settling time. Third, since there are no ground wires between data lines in an ATA cable, the data lines are highly coupled. Fourth, the transmission line characteristic impedances are higher than strobe lines since ground wires are farther away. These differences demand other considerations than the previous treatment.

Since data lines are bidirectional, the terminations on drives and host should be the same. For settling time, the ringing frequency and its rate of decay, or Q factor, are the concerns. The mutual coupling among data lines affects the ringing frequency causing the Q factor to be lower. The higher characteristic impedance causes the rate of decay of ringing to be slower since the Q factor is higher. Controlling the resistance in the data lines helps by limiting the Q factor, peak currents, and decay rate of the ringing. Controlling the load capacitance limits the frequency of the ringing.

Improper treatment of the data lines has several bad effects. Data settling time can increase to as long as 45 ns in severe cases. Excessive ringing on the data lines can induce spurious signals on adjacent control lines (crosstalk to DIOW- or RESET-).

Good design dictates that some type of ringing control be used on data lines, but of a different type than on control lines. A good practice is to insert 33 ohm series resistors on data lines at both the host and the device. The maximum capacitance specification in this standard must be met. The trace lengths from the load to the connector of the device or host board should be short. The driving end sees the same source termination as before. The receiving end sees an RC network of 33 ohms combined with the input capacitance of the interface chip. This is enough to substantially reduce the ringing and minimize settling time.

The IORDY line is a unique case on the bus. Under PIO modes IORDY is driven by an open collector outputs from the device, a current source rather than a voltage source. The nature of this signal makes the signal relatively insensitive to ringing that might occur. However, in Ultra DMA the IORDY line is used as a high speed data strobe from the device to the host. Termination of IORDY is recommended.

The one remaining bus structure not discussed is the open collector output driven by the device (DASP-). This signal is driven by a current source rather than a voltage source. Usually the transistor driving this signal is relatively slow and does not cause an excessive amount of ringing. The nature of DASP- makes the signal relatively insensitive to ringing that might occur.

Table C.1 summarizes the typical termination values:

**Table C.1 – Typical termination**

<b>Signal Name</b>	<b>Host Termination</b>	<b>Device Termination</b>
DIOR-, DIOW-	22 ohm series	82 ohm series
CS0-, CS1-	33 ohm series	82 ohm series
DA0, DA1, DA2	33 ohm series	82 ohm series
DMACK-	22 ohm series	82 ohm series
RESET-	33 ohm series	82 ohm series
DD0 through DD15	33 ohm series	33 ohm series
DMARQ	82 ohm series	22 ohm series
INTRQ	82 ohm series	22 ohm series
IORDY	82 ohm series	22 ohm series
DASP-, PDIAG-	no change	no change
CSEL	no change	no change
NOTE – For the 82 ohm series termination, an additional parallel capacitor may be needed if the interface chip and circuit board layout have less than 8 pf of capacitance.		



### C.2.7.1 Example of device-end termination timing

Assume that 82 ohm series resistors are inserted on all receive signals and 22 or 33 ohm series resistors on all transmit and bidirectional signals. Also assume that the input capacitance of the interface chip is 10 pf. There are three different RC configurations that occur (see figure C.13). All receive signals will see an 82 ohm and 10 pf network. The data lines will see a 33 ohm and 10 pf network when the device is receiving data. Signals driven back to the host (including data lines during a read) will see 33 ohms and 50 pf. The 50 pf assumption is the worst-case condition of both the host and another device being located nearby (negligible cable length), and both of them having the maximum allowed input capacitance.

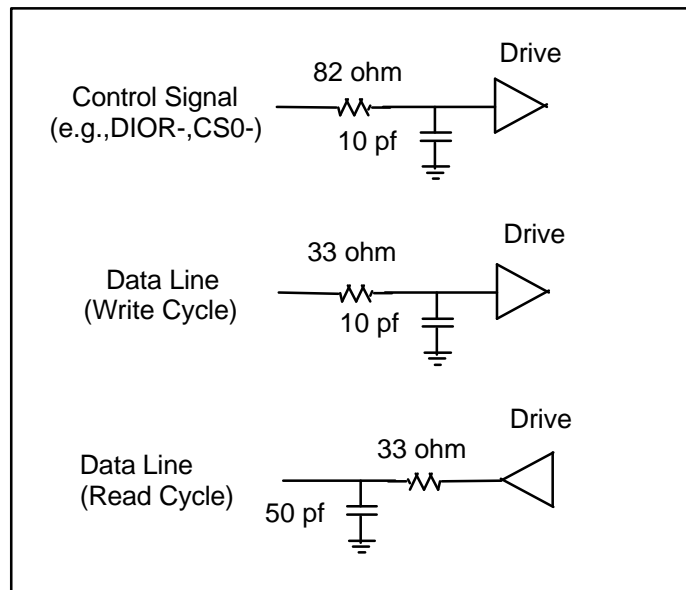


Figure C.13 – Signal models for device-end timing calculations

A simple SPICE simulation with a signal source and an RC load will show what the delays are through these three networks. Because the switching thresholds are not symmetrical with respect to the supply (0.8 V and 2.0 V) the delay for rising edges is different than that for falling edges. Since the input edge rate is unknown, both fast and slow edge inputs are simulated. The worst-case delay occurs with slow edges for rise times and fast edges for fall times. This mixture of slow rise time and fast fall time does not occur in real life, but since the edge speed is not known the worst case is planned for. The SPICE signal source is programmed for a rise time of 6.25 ns (same as 5 ns for 10% to 90%) and a fall time of 0.1 ns. The net result is six delay values. The results of the SPICE simulations are shown in table C.2.

Table C.2 – Typical device-end propagation delay times

Symbol	Description	Value
Tphlc	Propagation delay, high to low, control line	1.0 ns
Tplhc	Propagation delay, low to high, control line	0.9 ns
Tphldi	Propagation delay, high to low, data in	0.5 ns
Tplhdi	Propagation delay, low to high, data in	0.3 ns
Tphldo	Propagation delay, high to low, data out	2.5 ns
Tplhdo	Propagation delay, low to high, data out	1.1 ns

These delay values, combined with the interface chip timing specifications, will give the timing at the pins of the device. The trick is to figure out how each one of the timing parameters is affected by the delays.

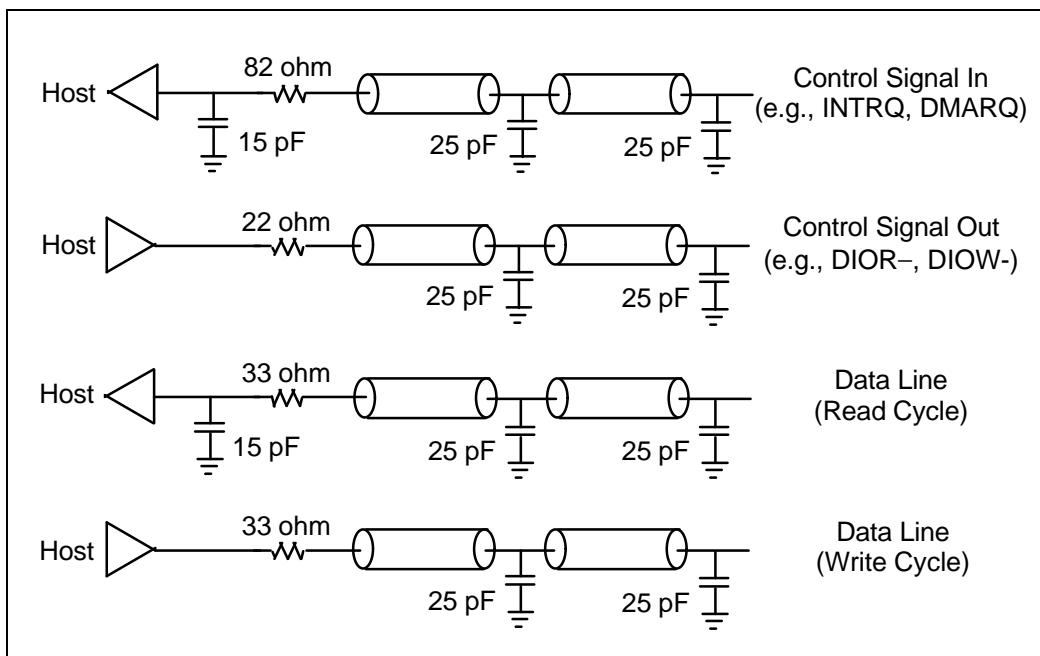
For example, consider the DIOW- Data Setup time (value t3). This is the amount of time that the data must be stable before the rising edge of DIOW-. Assume that the interface chip has a value of 2.0 ns. It is known that DIOW- is a control signal and the rising edge of control signals are delayed by 0.9 ns. This means that the setup time at the chip is actually greater than expected, but the data is delayed, too. It is not known what the data pattern is so it is assumed that the delay time is the maximum of Tphldi and Tplhdi.

The actual setup time is  $2.0 + 0.9 - \text{MAX}(0.3, 0.5) = 2.4$  ns. This is less than the requirement of 30 ns (for PIO mode 3) and therefore within spec.

This careful thought process must be repeated for all 15 of the PIO timing parameters (and for DMA and Ultra DMA also). The easiest way to do this is to make a spreadsheet and enter the six values for RC delay and the interface chip timing parameters. Spreadsheet formulas can then compute the timing at the pins of the device and highlight any that are not within specification. In this manner the difficult calculations need only be derived once and it becomes easier to verify results.

**C.2.7.2 Example of host-end termination timing calculation**

The host-end timing calculations are similar to the device-end calculations described above with a few more complicating factors added in. The four different signal configurations are shown in figure C.14. For this design 82 ohm series resistors are used on control lines received by the host and 22 or 33 ohm resistors on the data lines and control lines driven by the host. It is assumed that the host adapter chip input capacitance plus stray capacitance is 15 pf.



**Figure C.14– Host-end signal configurations with terminations**

For these values, the control signal out and the data out models are similar. The greatest uncertainty is the delay through the cable for received signals. The total cable delay depends on the source impedance of the device. This can be anything from zero to 82 ohms; the greater the impedance, the greater the delay. It is assumed for this example that the device vendor has read this document and has decided to use 22 or 33 ohms resistors. If it is desired later to make a worst-case assumption of 82 ohms, then approximately 2 ns are added to the numbers.

Using SPICE models similar to the one shown in figure C.15 the eight delay parameters required are derived. A second device appears in the model as a lumped capacitance of 25 pf that causes the maximum delay. The resulting values appear in table C.3. By examining the values in the table it should be clear why the cable propagation delay is often referred to as being about 5 ns.

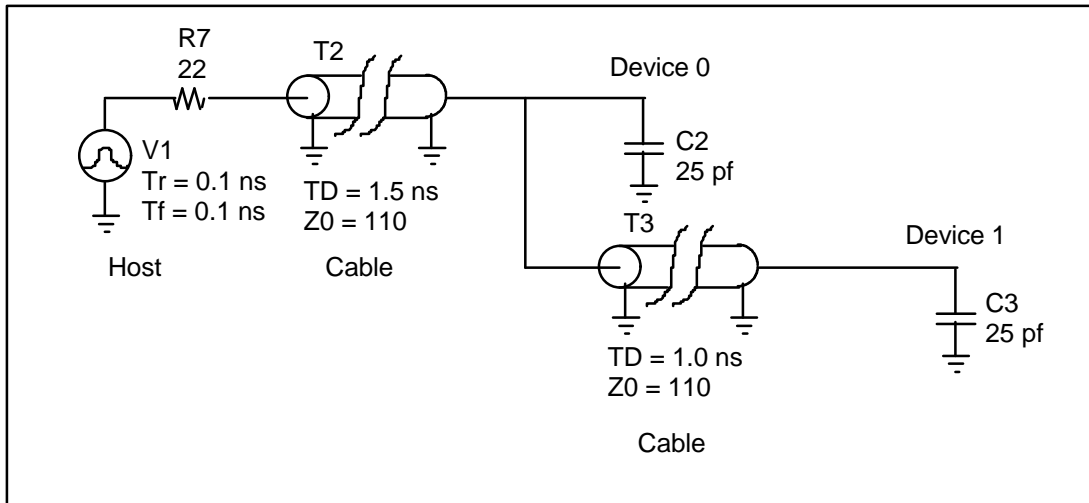


Figure C.15– SPICE model for control signal out delay calculation

Table C.3 – Typical host-end propagation delay times

Symbol	Description	Value
Tphlci	Propagation delay, high to low, control in	6.4 ns
Tplhci	Propagation delay, low to high, control in	4.7 ns
Tphlco	Propagation delay, high to low, control out	5.9 ns
Tplhco	Propagation delay, low to high, control out	4.6 ns
Tphldi	Propagation delay, high to low, data in	5.7 ns
Tplhdi	Propagation delay, low to high, data in	4.3 ns
Tphldo	Propagation delay, high to low, data out	5.9 ns
Tplhdo	Propagation delay, low to high, data out	4.6 ns

The process of finding the timing values is the same as for the device-end example. The propagation delay times are added to and subtracted from the host adapter chip timings to obtain the timings at the input to the device, in this case calculating the timing at the device furthest from the host adapter. The resulting timing values are compared against the values to determine what mode the device operates at.

### C.2.8 Dual port cabling

One of the recent enhancements to the bus has been the use of primary and secondary ports, allowing the user to attach up to four devices. The optimal way to implement dual ports is to have two completely separate interfaces that have no circuitry in common. This guarantees isolation between the ports and insures that no interference will occur.

The advent of local bus bridge chips has introduced new driving forces to the dual port cabling issue. Implementing two independent ports on a single chip requires 66 I/O pins. Due to the cost of pins, some designs have combined the data lines of the two ports into one set of pins. Sharing the data lines (or any other lines) in this way without termination allows the two cables and devices attached to interact. Simulations confirm that the ringing in such configurations is large and complex, particularly if the loads on the two cables are not balanced. Even with termination the buffer output impedance is a consideration.

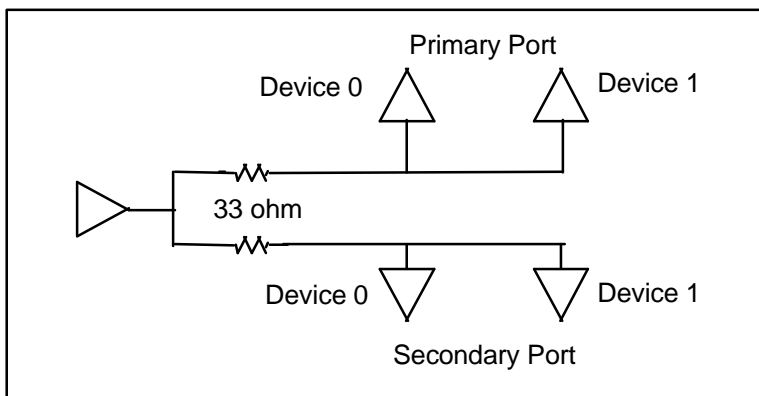
One alternative pin-saving solution would be to add a set of external buffers such as the 74ALS245. This would require three new control lines but would save 16 data lines for a net improvement of 13 pins. This also would require additional packages on the circuit board.

An economical solution is to add independent series resistors for each line (see figure C.16). Energy reflected back from the first cable passes through a series termination resistor, the shunt output impedance of the driver, a second series resistor and then into the second cable before getting to the host. This signal is reflected from the end of the second cable (with loss), and must pass through the termination resistor again before arriving at the host. The two series terminations and the shunt impedance of the buffer at the host

forms a T attenuator network isolating the two cables. The effectiveness of this network depends on the values: the series resistors need to be large, the shunt needs to be small, and the traces need to be short. The drivers must have high capacity to drive two cables, and additionally to attenuate ringing from one cable to the other. This provides sufficient attenuation of reflected signals to make ringing not a problem if all specifications are met, and all recommended terminations and trace lengths are implemented. When some recommendations and specifications are not met, the situation is more uncertain.

In practice, configurations will have devices that do not follow these recommendations. Nevertheless, it is reasonable to expect all manufacturers to conform to the ATA specification. Extensive simulation work has been done assuming specification conformance, and configurations that have at least one conforming device. The design of the host is a key factor in the performance of dual cable configurations.

Proving that any scheme works is a significant task. Simulations must be performed for all combinations of one device vs. two devices, devices with terminations and devices without terminations, devices with little load capacitance and maximum load capacitance, differing data patterns, etc. With two ports the number of combinations is daunting. Simulations have not yet revealed a combination of devices that fails to operate properly. Simulation results have been spot checked against actual systems.



**Figure C.16 – Preferred connection for shared lines in dual port systems**

Not all of the signal lines in a shared dual port interface can be shared. If the chip select lines (CS0-, CS1-) and the data strobe lines (DIOR-, DIOW-) are shared, then it is impossible to differentiate between the primary and secondary ports. A write to a device on one port causes the same action to occur on the other port, destroying the data on the other device. The data strobe lines are sensitive edge-triggered signals while the chip select lines act more like level-sensitive address lines. It is recommended that designers share the less sensitive chip select lines and not share the data strobe lines.

The purpose of the chip select lines is to select the active device. It makes sense to have independent chip select lines for primary and secondary ports. This allows the DIOR- and DIOW- lines to be shared. The ATA bus signals that can and cannot be shared are shown in table C.4.

Table C.4 makes some assumptions about how the dual porting is being implemented. If the data lines are shared, there can not be simultaneous accesses to the primary and secondary ports. The IORDY line cannot be shared since IORDY is a strobe in Ultra DMA mode and because of transmission line considerations. The INTRQ and DMARQ signals are driven by tristate buffers on the devices. Either Device 0 or Device 1 enables its tristate driver depending on the state of the DEV bit in the Device/Head Register. Therefore INTRQ and DMARQ cannot be shared because either Device 0 or Device 1 will be driving these lines at all times. The primary port devices do not know about the secondary port devices, so sharing these lines would create a conflict. In theory, the DMACK- line could be shared since DMACK- is driven by the host. In practice this is not recommended. It is likely that some devices respond unconditionally to the DMACK- signal, whether they ever requested a DMA cycle or not. This could lead to a conflict on a DMA cycle between a primary port device and a secondary port device during the data cycle. For these reasons the INTRQ, DMARQ, and DMACK- lines cannot be shared.

**Table C.4 – Possible sharing of signals in dual port configurations**

Signal name	
DIOR-, DIOW-	Not shareable
CS0-, CS1-	Shareable
DA0, DA1, DA2	Shareable
DMACK-	Not shareable
RESET-	Shareable
DD0 – DD15	Shareable
DMARQ	Not shareable
INTRQ	Not shareable
IORDY	Shareable
DASP-, PDIAG-	Not shareable
CSEL	Not shareable

The DASP- lines cannot be shared. Assume there are two devices on the primary port, and one device on the secondary port. With the DASP- lines connected, the single device on the secondary port will incorrectly “see” Device 1 on the primary port. This would be a problem for all manufacturers who follow the specifications. Similar problems can occur with the PDIAG- lines; they cannot be shared.

Sharing lines between ports will lead to lower performance than fully independent ports. Newer operating systems are multithreaded, so it is possible for accesses to be occurring independently and concurrently on the primary and secondary ports. With shared signals lines concurrent access is not possible, hence the impact on performance.

Note that the entries in table C.4 are not the last word on line sharing. There are specific conditions under which some lines may be sharable. For example, if separate DIOR- and DIOW- lines were provided for primary and secondary ports, then the CS0- and CS1- lines could be shared. Many combinations of shared and non-shared lines are possible provided that the functionality of the signals is carefully considered.

### C.3 Crosstalk

Crosstalk is switching on one signal line causing induced signals in an adjacent line. Crosstalk has not been a significant issue in the past with slower edge rates; in newer systems the problem is often masked by ringing. Once the cable is terminated and the ringing is under control, then the presence of crosstalk becomes apparent.

#### C.3.1 Coupling mechanisms

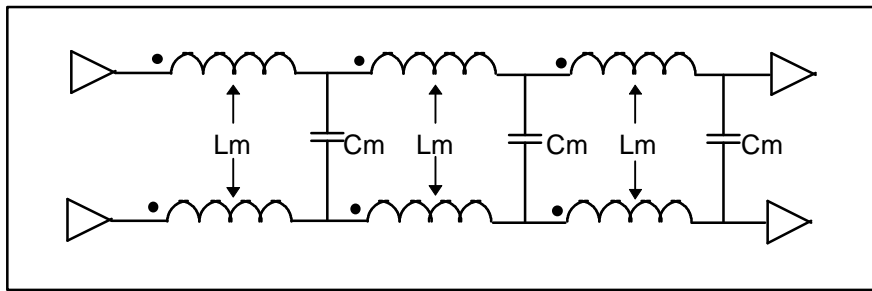
There are three mechanisms by which a signal couples into an adjacent line. The first is mutual capacitance, the second is mutual inductance, and the third is common impedance coupling. As a switching signal wavefront propagates down the cable the wavefront couples energy into the adjacent line. Once this energy is in the second transmission line, the energy propagates in both directions: forward toward the receiver and back toward the source (see figure C.17).

First the forward coupling components are examined. The coupling capacitance between the two line causes a current pulse in the secondary line proportional to the capacitance and the rate of change of voltage on the primary side. A positive voltage step on the primary line causes a positive voltage spike on the secondary line at both source and load.

The voltage induced in the second transmission line is proportional to the coupling coefficient, the inductance, and the rate of change of current in the primary side. This induced potential appears longitudinally and presents as a negative voltage at the load, and a positive voltage at the source.

An additional voltage appears in series with the load from the current carried in the ground or signal return wire. This type of coupling is called common impedance since the voltage is coupled from an impedance common to the two circuits. Here, the common impedance is that of the signal return or ground wire, and

the common impedance is primarily inductive. The voltage induced in the second line is proportional to the inductance, and the rate of current from the first line.



**Figure C.17 – Crosstalk coupling mechanisms**

These coupling mechanisms have some interesting characteristics. The polarity of the coupling at the load is opposite for the mutual inductance and coupling capacitance. If the magnitudes of these effects are comparable, then they will cancel, resulting in no forward crosstalk. Unfortunately, accurately computing these values is difficult, and the easiest way to determine the actual amount of crosstalk is to measure it. The other noteworthy characteristic is that the magnitude of the coupled signal is proportional to the rate of change of the signal in the primary line. This is a major reason for controlling the slew rate on bus drivers. Here it is seen that fast edge rates and ringing on the data lines can couple by crosstalk into adjacent control lines, causing control sequence errors through mistriggering. The presence of crosstalk-induced voltage spikes on the control signals reduces the noise margin, and can increase the long-term error rate.

The amplitude of the coupled signal is proportional to the total amount of coupling capacitance and mutual inductance, and common impedance, and is therefore proportional to cable length. Once a line is terminated properly, ringing is no longer a function of length. This leaves crosstalk as the major factor limiting cable length.

Reducing crosstalk involves reducing the mutual inductance, mutual capacitance, and common impedance, or decreasing the source signal amplitude. Controlling the inductance and capacitance can be done by either keeping the length of the cable short or by increasing the distance between conductors. Placing a ground conductor between critical signals increases the separation of the signals, adds a shielding effect from the intervening ground, and reduces the common impedance. In this environment the only control that can be exercised over the cable is to keep the length at 18 inches or less. The amplitude of the source signal can be reduced somewhat and still maintain compatibility, and some elements of the source signal can be controlled. Slew rate limitation reduces the high-frequency components of the source signal and therefore reduces the coupling of these components into adjacent lines. Terminating the lines reduces ringing that also decreases the amount of energy coupled at the ringing frequency.

## C.4 Bus timing

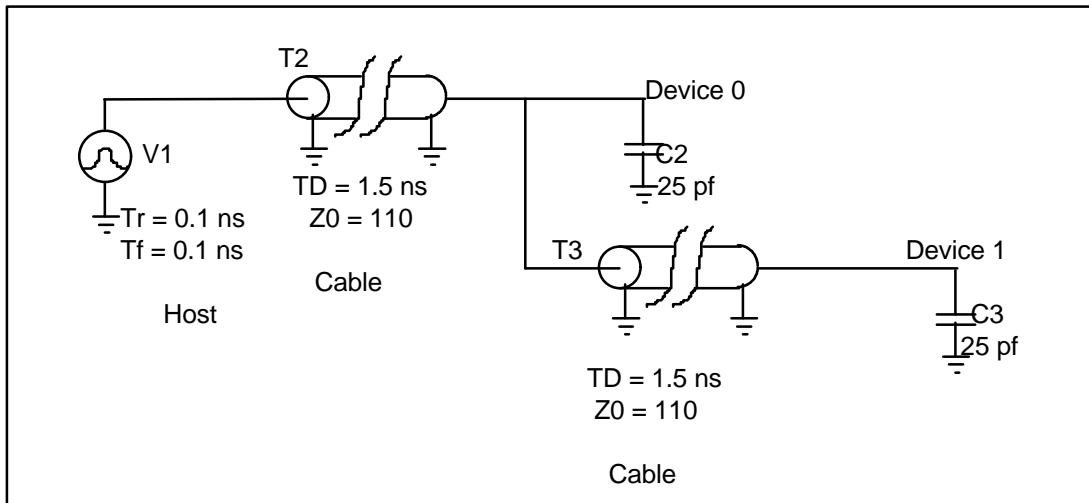
Terminating the bus has its cost. Partial terminations at the host and the device increase propagation delays throughout the system. This standard specifies that timing is referenced to the input pins of the device (see clause 10). This means that most of the timing issues must be addressed by systems manufacturers and bridge chip designers.

### C.4.1 The issues

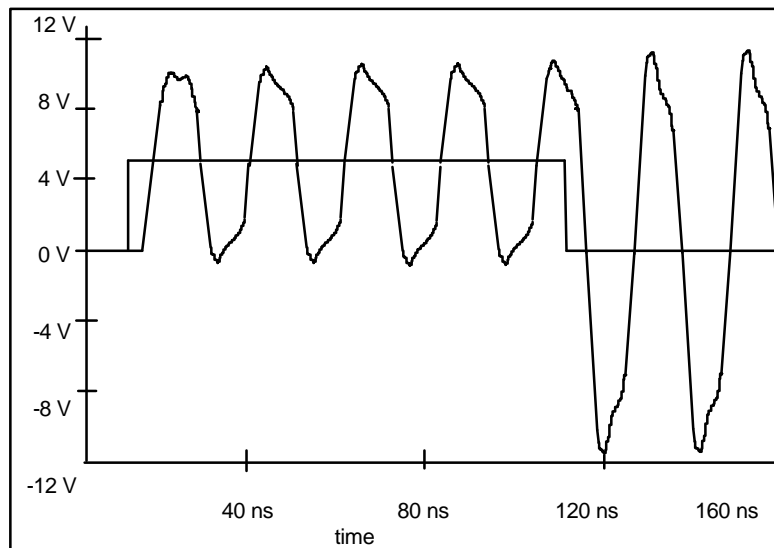
The most significant timing issue is the propagation delay of the cable. This needs to be added to the host-side timing. The SPICE model in figure C.18 shows an unterminated host with very fast rise times driving a cable with worst case loads. Two unterminated devices are assumed with the maximum allowed capacitive loading of 20 pf.

NOTE – 25 pf was specified in ATA-2.

The simulation results are shown in figure C.19. The period of the ringing is four times the propagation delay of the cable. This simulation shows a cable propagation delay of 5.6 ns. This is twice the value obtained by assuming an 18-inch cable with a propagation velocity of 60% c. The additional delay is due to the presence of the capacitive loads on the cable. This result is important to system designers who take into account worst-case cable delay when specifying the bridge chip timing.



**Figure C.18– SPICE model of cable with worst case loads**



**Figure C.19– Simulation of unterminated cable with worst case loads**

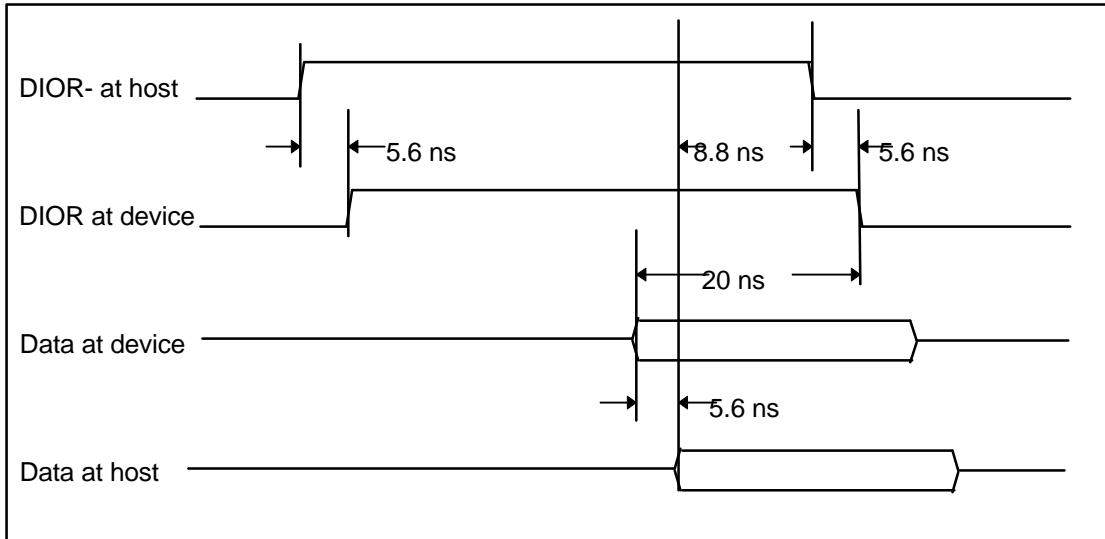
From the host point of view, all of the timings are corrected by adding the propagation delay of the cable to insure that the timing is correct at the input pins of the furthest device. Figure C.20 shows a typical corrected result using the read cycle data setup time as an example. This standard specifies a setup time at the device of 20 ns (PIO mode 3). The remaining setup time at the host is only 8.8 ns ( $20 - 2 \times 5.6$ ).

#### C.4.2 The influence of termination

If the host has a series partial termination resistor then the bridge chip includes additional timing margin to account for the RC delay of that resistor. Simulations show that the incremental delay added by a series termination resistor at the host is approximately 0.2 ns for a 33 ohm resistor and 1.7 ns for an 82 ohm resistor.

NOTE – Assuming a two device load, 25 pf at each device, an 18-inch cable, and 25 pf at host

The extra delay of higher resistor values is one of the reasons that 33 ohm series resistors at the host are recommended.



**Figure C.20 – Host data setup time during a read cycle**

The series resistor at the host is located as close as possible to the connector. To see the importance of this, SPICE simulations are done with the stray capacitance on the driver side of the series resistor and again with the stray capacitance on the cable side. The ringing is reduced when the stray capacitance of the host is on the driver side of the series resistor. A related issue is the distance from the host adapter chip (or chipset) to the connector. Some motherboards have the chip located up to 10 inches away from the connector. This effectively adds another 10 inches to the 18-inch ribbon cable, resulting in an equivalent cable length of 28 inches.

NOTE – The traces on the circuit board are from 25 to 90 ohm impedance, so the electrical length of the trace cannot simply be added to the 110 ohm ribbon cable. A SPICE simulation can be used to find the actual delay.

This additional length is not necessarily a problem. If the system manufacturer takes the extra trace delay into account in the application of the host adapter chip, and the total capacitance is kept below the host limit of 25 pf, then in theory there is no difference. Real-world experience indicates that this calculation is rarely done. The distance from the chip to the connector is not addressed in this standard. Keeping the connector within 3 inches (by trace length) of the host adapter chip is recommended.

### C.4.3 Calculating rise time

Chip designers often use a lumped capacitance model for simulating the delay of the output cell. For the simulations this sometimes consists of adding the maximum capacitance allowed for the host and the devices ((2 x 20) + (1 x 25) pf) to an estimated capacitance value for the cable (25 pf). Simulation is then performed with 100 pf capacitance on the output. This does not give an accurate measurement of the timing. A better approximation is to use an output capacitance for the motherboard, a host end termination resistor, and a transmission line to the devices (see figure C.21).

To illustrate how these models are different, suppose that the propagation delay of the output cell simulation is 2 ns too slow. The chip designer (using a 100 pf model) increases the drive current of the output devices. With enough drive current into a purely capacitive load, the 2 ns is removed, bringing the output cell timing back into spec.



Increasing the drive of the output cell in the transmission line model, the length of the cable is not increased and the speed of signal propagation in the cable is not increased. The 2 ns required time reduction is not achieved by increasing the output drive current. The time must come from somewhere else in the internal circuitry. Increasing the output drive current only increases the edge speed, making the ringing worse at the device end (some time is gained with the faster edge speed, but not nearly as much as is predicted with a simple capacitive load model). It is not possible to decrease the overhead by increasing the drive current.

Most ASIC designers find that simulations using the recommended model of figure C.21 show their output cells to be faster than in models with a 100 pf load.

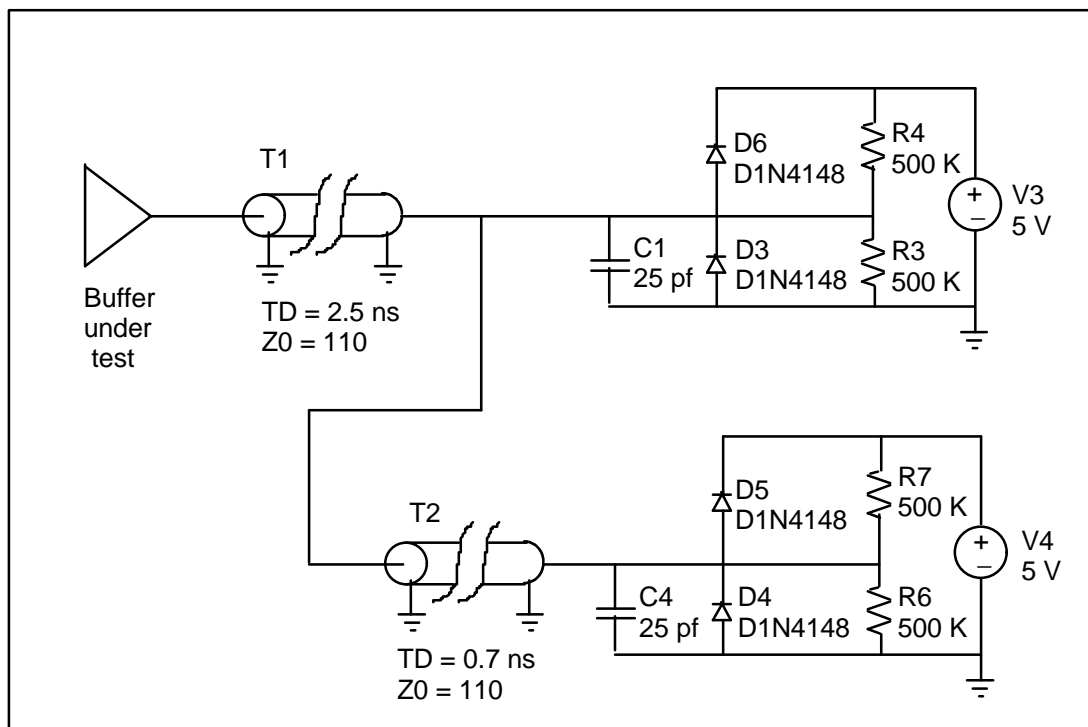


Figure C.21 – Recommended model for I/O cell propagation delay

#### C.4.4 Measuring propagation delay

Propagation delay times at the host (and at the device) are measured to the standard of 0.8 V for high to low transitions and 2.0 V for low to high transitions. Many IC manufacturers measure propagation delay at the typical switch point for TTL of 1.4 V. This is not appropriate for the interface since virtually every chip manufacturer (both host and device end) has included hysteresis for noise immunity. Since both the hysteresis window and hysteresis offset of a given receiver move with process, voltage, and temperature, the only guaranteed switch points are the TTL high and low values (0.8 V and 2.0 V).

#### C.5 Summary of guidelines

This summary is a collection of reminders for device, system, and chipset designers. They are separated into three groups by relevancy. The guidelines below are not intended to be a strict mandate, but a tool to help everyone build compatible, reliable, high-performance products.

### **C.5.1 Guidelines for device designers**

- Terminate signals as shown in table C.1. Consider adding capacitors to ground on these lines if the input capacitance is less than 8 pf, or use active clamping circuits. Place these resistors as close to the connector as possible.
- Verify that the termination circuit used on received signals has less than 20 pf of equivalent capacitance.
- Perform a timing analysis to verify that timings are met at the input to the device. Include the time delay due to propagation and cable termination circuits.

### **C.5.2 Guidelines for system designers**

- Do not use any value less than 1 K ohm for pull up resistors on open-collector signals such as IORDY (as per this standard).
- The host adapter chip should be located as close as possible to the connector. Keep the trace length between them less than 3 in.
- After circuit board fabrication, verify that the total input capacitance at the host is less than 25 pf.
- Terminate signals as shown in table C.1. Place these resistors as close to the connector as possible.
- Perform a system timing analysis to verify that timings are met at the input to the device.
- For dual port implementations, terminate signals as shown in figure C.16. These resistors should be placed as close to the connector of that port as possible.
- For dual port implementations, the signal lines CS0- and CS1- may be shared, or the signals DIOR- and DIOW- may be shared, but not both pairs.
- For dual port implementations, do not share DASP- or PDIAG- signal lines.
- For dual port implementations, perform a system timing analysis to verify that timings are met at the input of the device. In particular watch the assertion widths of DIOR- and DIOW- to insure that they meet the specification.
- Route cable away from chassis, power supplies, and high speed circuits.
- Use the shortest cable practical and never greater than 18 in.

### **C.5.3 Guidelines for chip designers**

- Design I/O cells to have rise and fall times of 5 ns or more under both minimum and maximum load conditions.
- Perform timing simulations using a transmission line load model, not a 100 pf capacitor model.
- Take worst-case cable delay into account when designing the interface. Ensure that timing can be met at the device-end of the cable. Provide typical application data with timing for system manufacturers.

## Annex D (informative)

### Device determination of cable type

#### D.1 Overview

This standard requires that, for systems using a cable assembly, an 80-conductor cable assembly shall be installed before a system may operate with Ultra DMA modes greater than 2. However, some hosts have not implemented circuitry to determine the installed cable type by detecting whether PDIAG-:CBLID- is connected to ground as mandated by this standard. The following describes an alternate method for using IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data from the device to determine the cable type. It is not recommended that a host use the method described in this annex.

If a host uses IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data from the device to determine the cable type, then a 0.047  $\mu\text{f}$  capacitor shall be installed from CBLID- to ground at the host connector. The tolerance on this capacitor is +/- 20% or less. After receiving an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command the device detects the presence or absence of the capacitor by asserting PDIAG-:CBLID- to discharge the capacitor, releasing PDIAG-, and sampling PDIAG-:CBLID- before the installed capacitor could recharge through the 10 k $\Omega$  pull-up resistor(s) on PDIAG-:CBLID- at the device(s).

If the host system has a capacitor on PDIAG-:CBLID- and a 40-conductor cable is installed, the rise time of the signal will be slow enough that the device will sample PDIAG-:CBLID- while the signal is still below  $V_{IL}$ . Otherwise, if PDIAG-:CBLID- is not connected from the host connector to the devices in an 80-conductor cable assembly, the device will detect that the signal is pulled above  $V_{IH}$  through the resistor(s) on the device(s). The capacitor test results will then be reported to the host in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. The host will use the data to determine the maximum transfer rate of which the system is capable and use this information when setting the transfer rate using the SET FEATURES command.

#### D.2 Sequence for device detection $\phi$ installed capacitor

The following is the sequence for a host using IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data from the device to determine the cable type:

- a) The host issues an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command (according to device type) first to Device 1 and then to Device 0 after every power on or hardware reset sequence (the command is issued to Device 1 first to ensure that Device 1 releases PDIAG-:CBLID- before Device 0 is selected. Device 0 will be unable to distinguish a discharged capacitor if Device 1 is driving the line to its electrically low state. Issuing the command to Device 1 forces it to release PDIAG-:CBLID-);
- b) the selected device asserts PDIAG-:CBLID- for at least 30  $\mu\text{s}$  after receipt of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command but before transferring data for the command;
- c) the device releases PDIAG-:CBLID- and samples it between two and thirteen  $\mu\text{s}$  after release;
- d) if the device detects that PDIAG-:CBLID- is below  $V_{IL}$ , then the device returns a value of zero in bit 13 of word 93 in its IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (if the host system has a capacitor on that signal and a 40-conductor cable is installed, the rise time of the signal will be slow enough that it will be sampled by the device while it is still below  $V_{IL}$ );
- e) if the device detects that the signal is above  $V_{IH}$ , then the device returns a value of one in bit 13 of word 93 in its IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (this signal is not connected between the host and the devices in an 80-conductor cable assembly, thus, the sampling device will see this signal pulled above  $V_{IH}$  through the 10 k $\Omega$  resistor(s) installed on the device(s);
- f) the host then uses its knowledge of its own capabilities and the content of words 88 and 93 to determine the Ultra DMA modes of which the system is capable;
- g) the host then uses the SET FEATURES command to set the transfer mode.

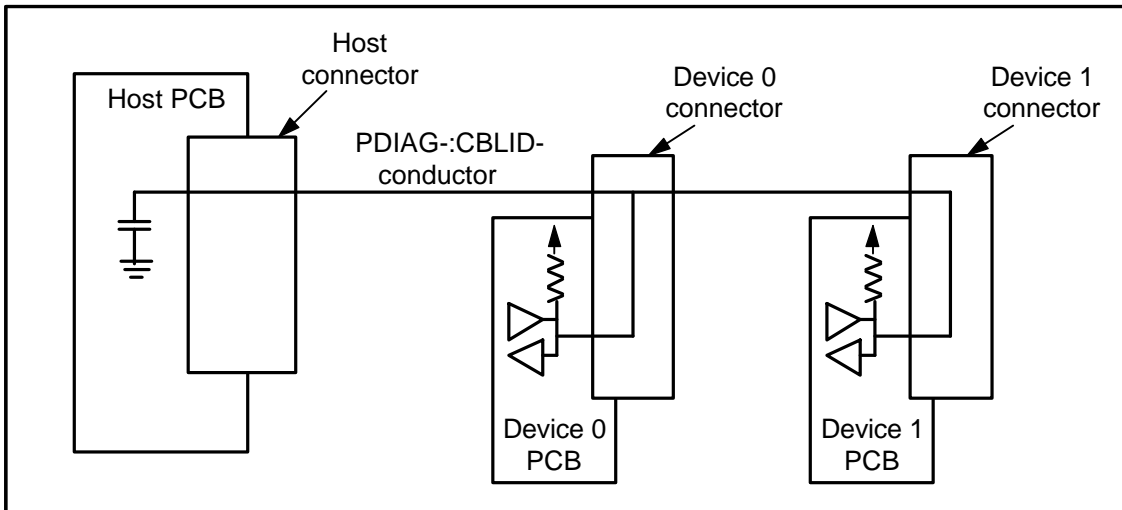


Figure D.1 – Example configuration of a system where the device detects a 40-conductor cable

Table D.1 – Device detection of installed capacitor

Cable assembly type	Device 1 releases PDIAG-ID data by device	Value reported in	Device-determined cable type	Determination correct?
40-conductor	Yes	0	40-conductor	Yes
80-conductor	Yes	1	80-conductor	Yes
40-conductor	No	0	40-conductor	Yes
80-conductor	No	0	40-conductor	No (see note)

NOTE – Ultra DMA modes 3 or 4 will not be set even though the system supports them.

Table D.2 – Results of device based cable detection if the host does not have the capacitor installed

Cable assembly type	Device 1 releases PDIAG-ID data by device	Value reported in	Device-determined cable type	Determination correct?
40-conductor	Yes	1	80-conductor	No (see note 1)
80-conductor	Yes	1	80-conductor	Yes
40-conductor	No	0	40-conductor	Yes
80-conductor	No	0	40-conductor	No (see note 2)

NOTES –

- 1 Ultra DMA mode 3 or 4 may be set incorrectly resulting in ICRC errors.
- 2 Ultra DMA modes 3 or 4 will not be set even though the system supports them.

### D.3 Using the combination of methods for detecting cable type

Determining the cable assembly type may be done either by the host sensing the condition of the PDIAG-:CBLID- signal, by relying on information from the device, or a combination of both methods. Table D.3 describes the results of using both host and device cable detection methods.

**Table D.3 – Results of using both host and device cable detection methods**

Cable assembly type	Device 1 Releases PDIAG-	Electrical state of CBLID- at host	Value reported in ID data by device	Determined cable type	Determination correct?
40-conductor	Yes	1	0	40	Yes
80-conductor	Yes	0	1	80	Yes
40-conductor	No	0	0	40	Yes (see note)
80-conductor	No	0	0	40	No (see note)

NOTE – The “0,0” result is independent of cable type and indicates that Device 1 is incorrectly asserting PDIAG-. When the host determines this result, it shall not operate with Ultra DMA modes greater than 2 and it may respond in several ways:

- a) report that Device 1 is incompatible with Ultra DMA modes higher than 2 and should be used on a different port in order to use those modes on the port being detected;
- b) report that Device 1 is not allowing the cable type to be properly detected;
- c) do not notify the user of any problem but detect the cable as a 40-conductor.

The Table D.4 below illustrates intermediate results for all combinations of cable, device, and host, for hosts that support Ultra DMA modes greater than 2.

**Table D.4 – Results for all combinations of device and host cable detection methods**

Design options			Intermediate actions and results						Results
80-conductor cable installed	Device supports UDMA modes >2	Host senses PDIAG-:CBLID-	Host uses ID data, capacitor installed	Host capacitor connected to device	Device tests for capacitor	Capacitor detected	ID word 93 Bit 13 value	Host checks ID word 93 bit 13	Host may set UDMA mode >2
No	No	Yes	No	No	No	No	0	No	No
No	Yes	Yes	No	No	Yes	No	1	No	No
Yes	No	Yes	No	No	No	No	0	No	No
Yes	Yes	Yes	No	No	Yes	No	1	No	Yes
No	No	No	Yes	Yes	No	No	0	Yes	No
No	Yes	No	Yes	Yes	Yes	Yes	0	Yes	No
Yes	No	No	Yes	No	No	No	0	Yes	No
Yes	Yes	No	Yes	No	Yes	No	1	Yes	Yes

**Annex E**  
(informative)  
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Suite of 2.5" Form Factor Specifications, SFF-8200, SFF-8201<sup>2</sup>  
Suite of 3.5" Form Factor Specifications, SFF-8300, SFF-8301, SFF-8302<sup>2</sup>  
CompactFlash Association Specification Revision 1.2<sup>3</sup>

1) QIC documents are published by:

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3) The CFA specification is published by:

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## Annex F (informative) Command set summary

The following four tables are provided to facilitate the understanding of the command set. Table F.1 provides information on which command codes are currently defined. Table F.2 provides a list of all of the commands in order of command code. Table F.3 provides a summary of all commands with the protocol, required use, command code, and registers used for each. Table F.4 shows the status and error bits used by each command.

**Table F.1 – Command matrix**

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
<b>0x</b>	C	R	R	C*	R	R	R	R	C*	R	R	R	R	R	R	R
<b>1x</b>	O	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*
<b>2x</b>	C	O	O*	O*	R	R	R	R	R	R	R	R	R	R	R	R
<b>3x</b>	C	O	O*	O*	R	R	R	R	C*	R	R	R	O*	R	R	R
<b>4x</b>	C	O	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>5x</b>	O*	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>6x</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>7x</b>	C	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*
<b>8x</b>	V	V	V	V	V	V	V	F*	V	V	V	V	V	V	V	V
<b>9x</b>	C	C	C	R	E*	E*	E*	E*	E*	E*	V	R	R	R	R	R
<b>Ax</b>	C*	C*	C*	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Bx</b>	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Cx</b>	F*	V	V	V	C	C	C	C*	C	O	C	O	C*	C*	R	R
<b>Dx</b>	R	R	R	R	R	R	R	R	R	R	C*	E*	E*	E*	C*	C*
<b>Ex</b>	C	C	C	C	C	C	C	C*	C	E*	R	R	C*	C*	O*	C
<b>Fx</b>	V	C	C	C	C	C	C	V	C	C*	V	V	V	V	V	V

Key:

C = a defined command, R = Reserved, undefined in current specifications, V = Vendor specific commands

O = Obsolete, E=a retired command, F=If the device does not implement the CFA feature set, this command code is Vendor specific, \* indicates that the definition of this command has changed from ATA-3, X3.298-1997.

**Table F.2 – Commands sorted by command value**

<b>Command name</b>	<b>Command code</b>
NOP	00h
CFA REQUEST EXTENDED ERROR CODE	03h
DEVICE RESET	08h
READ SECTOR(S)	20h
WRITE SECTOR(S)	30h
CFA WRITE SECTORS WITHOUT ERASE	38h
READ VERIFY SECTOR(S)	40h
SEEK	70h
CFA TRANSLATE SECTOR	87h
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
PACKET	A0h
IDENTIFY PACKET DEVICE	A1h
SERVICE	A2h
SMART	B0h
CFA ERASE SECTORS	C0h
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
READ DMA QUEUED	C7h
READ DMA	C8h
WRITE DMA	CAh
WRITE DMA QUEUED	CCh
CFA WRITE MULTIPLE WITHOUT ERASE	CDh
GET MEDIA STATUS	DAh
MEDIA LOCK	DEh
MEDIA UNLOCK	DFh
STANDBY IMMEDIATE	E0h
IDLE IMMEDIATE	E1h
STANDBY	E2h
IDLE	E3h
READ BUFFER	E4h
CHECK POWER MODE	E5h
SLEEP	E6h
FLUSH CACHE	E7h
WRITE BUFFER	E8h
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
SET FEATURES	EFh
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h
SECURITY FREEZE LOCK	F5h
SECURITY DISABLE PASSWORD	F6h
READ NATIVE MAX ADDRESS	F8h
SET MAX ADDRESS	F9h



Table F.3 – Command codes and parameters

proto	Command	typ	PKT fea	Command code	Parameters used				
					FR	SC	SN	CY	DH
ND	CFA ERASE SECTORS	O	N	C0h		y	y	y	y
ND	CFA REQUEST EXTENDED ERROR	O	N	03h					D
PI	CFA TRANSLATE SECTOR	O	N	87h			y	y	y
PO	CFA WRITE MULTIPLE W/OUT ERASE	O	N	CDh		y	y	y	y
PO	CFA WRITE SECTORS W/OUT ERASE	O	N	38h		y	y	y	y
ND	CHECK POWER MODE	M	M	E5h		y			D
DR	DEVICE RESET	O	M	08h					D
PO	DOWNLOAD MICROCODE	O	N	92h	y	y	y	y	D
DD	EXECUTE DEVICE DIAGNOSTIC	M	M	90h					D*
ND	FLUSH CACHE	M	M	E7h		y	y	y	y
ND	GET MEDIA STATUS	O	O	DAh					D
PI	IDENTIFY DEVICE	M	N	ECh					D
PI	IDENTIFY PACKET DEVICE	N	M	A1h					
ND	IDLE	M	O	E3h		y			D
ND	IDLE IMMEDIATE	M	M	E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	N	91h		y			y
ND	MEDIA EJECT	O	O	EDh					D
ND	MEDIA LOCK	O	O	DEh					D
ND	MEDIA UNLOCK	O	O	DFh					D
ND	NOP	O	M	00h					D
P	PACKET	N	M	A0h	y	y	y	y	D
PI	READ BUFFER	O	N	E4h					D
DM	READ DMA	M	N	C8h		y	y	y	y
DMO	READ DMA QUEUED	O	N	C7h	y	y	y	y	y
PI	READ MULTIPLE	M	N	C4h		y	y	y	y
ND	READ NATIVE MAX ADDRESS	O	N	F8h					D
PI	READ SECTOR(S)	M	N	20h		y	y	y	y
ND	READ VERIFY SECTOR(S)	M	N	40h		y	y	y	y
PO	SECURITY DISABLE PASSWORD	O	O	F6h					D
ND	SECURITY ERASE PREPARE	O	O	F3h					D
PO	SECURITY ERASE UNIT	O	O	F4h					D
ND	SECURITY FREEZE	O	O	F5					D
PO	SECURITY SET PASSWORD	O	O	F1H					D
PO	SECURITY UNLOCK	O	O	F2h					D
ND	SEEK	M	N	70h			y	y	y
P	SERVICE	N	O	A2h		y	y	y	D
ND	SET FEATURES	M	M	EFh	y				D
ND	SET MAX ADDRESS	O	N	F9h		y	y	y	y
ND	SET MULTIPLE MODE	M	N	C6h		y			D
ND	SLEEP	M	M	E6h					D
ND	SMART DISABLE OPERATIONS	O	O	B0h	y			y	D
ND	SMART ENABLE/DISABLE AUTOSAVE	O	O	B0h	y	y		y	D
ND	SMART ENABLE OPERATIONS	O	O	B0h	y			y	D
ND	SMART EXECUTE OFF_LINE	O	O	B0h	y			y	D
PI	SMART READ DATA	O	O	B0h	y			y	D
PI	SMART READ LOG SECTOR	O	O	B0h	y	y	y	y	D
ND	SMART RETURN STATUS	O	O	B0h	y			y	D
PO	SMART WRITE LOG SECTOR	O	O	B0h	y	y	y	y	D

(continued)

**Table F.3 – Command codes and parameters**(concluded)

proto	Command	typ	PKT fea	Command code	Parameters used				
					FR	SC	SN	CY	DH
ND	STANDBY	M	O	E2h		y			D
ND	STANDBY IMMEDIATE	M	M	E0h					D
PO	WRITE BUFFER	O	N	E8h					D
DM	WRITE DMA	M	N	CAh		y	y	y	y
DMO	WRITE DMA QUEUED	O	N	CCh	y	y	y	y	y
PO	WRITE MULTIPLE	M	N	C5h		y	y	y	y
PO	WRITE SECTOR(S)	M	N	30h		y	y	y	y
VS	Vendor specific	V	V	9Ah,C0h- C3h,8xh, F0h,F7h, FAh-FFh					
-	Reserved: all remaining codes	R	R						

## Key:

DM = DMA command                      ND = Non-data command                      PI = PIO data-in command  
PO = PIO data-out command              VS = Vendor specific command              O = Optional                      P=PACKET command  
DR = DEVICE RESET protocol              DD = EXECUTE DEVICE DIAGNOSTIC protocol  
DMO = Overlapped/queued DMA  
typ=Command type                      PKT fea=Command type when PACKET Command feature set implemented  
M = Mandatory                      R = Reserved                      N=Not to be used                      V = Vendor specific implementation  
CY = Cylinder registers                      SC = Sector Count register                      DH = Device/Head register  
SN = Sector Number register              FR = Features register (see command descriptions for use)  
y = the register contains a valid parameter for this command. For the Device/Head register, y means both the device and head parameters are used.  
D = only the device parameter is valid and not the head parameter.  
d = the device parameter is valid, the usage of the head parameter vendor specific.  
D\* = Addressed to device 0 but both devices execute the command.

Table F.4 – Register functions and selection addresses except PACKET and SERVICE commands

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	x	x	x	Data bus high impedance	Not used
					<b>Control block registers</b>	
N	A	N	x	x	Data bus high impedance	Not used
N	A	A	N	x	Data bus high impedance	Not used
N	A	A	A	N	Alternate Status	Device Control
N	A	A	A	A	obsolete(see note)	Not used
					<b>Command block registers</b>	
A	N	N	N	N	Data	Data
A	N	N	N	A	Error	Features
A	N	N	A	N	Sector Count	Sector Count
A	N	N	A	A	Sector Number	Sector Number
A	N	A	N	N	Cylinder Low	Cylinder Low
A	N	A	N	A	Cylinder High	Cylinder High
A	N	A	A	N	Device/Head	Device/Head
A	N	A	A	A	Status	Command
A	A	x	x	x	Invalid address	Invalid address
Key: A = signal asserted, N = signal negated, x = don't care NOTE – This register is obsolete. It is recommended that a device not respond to a read of this address.						

Table F.5 – Register functions and selection addresses for PACKET and SERVICE commands

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	x	x	x	Data bus high impedance	Not used
					<b>Control block registers</b>	
N	A	N	x	x	Data bus high impedance	Not used
N	A	A	N	x	Data bus high impedance	Not used
N	A	A	A	N	Alternate Status	Device Control
N	A	A	A	A	obsolete(see note)	Not used
					<b>Command block registers</b>	
A	N	N	N	N	Data	Data
A	N	N	N	A	Error	Features
A	N	N	A	N	Interrupt reason	
A	N	N	A	A		
A	N	A	N	N	Byte count low	Byte count low
A	N	A	N	A	Byte count high	Byte count high
A	N	A	A	N	Device select	Device select
A	N	A	A	A	Status	Command
A	A	x	x	x	Invalid address	Invalid address
Key: A = signal asserted, N = signal negated, x = don't care NOTE – This register is obsolete. A device should not respond to a read of this address.						

**Annex G**  
(informative)  
**Command packet format example**

Table G.1 is an example of the command packet for most PACKET commands.

**Table G.1 – Command packet**

Byte	7	6	5	4	3	2	1	0	
0	Operation code								
1	reserved			reserved					
2	Logical block address (if required)								
3									(MSB)
4									
5									
6	reserved								
7-8	Transfer length (if required) or Parameter list length (if required) or Allocation length (if required)								
9	reserved								
10	reserved								
11	reserved								