ZR6 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:C

DDR3 PWR TPS51116 P36 | CHARGER ISL6251 P32
THERMAL PROTECTION P40 | 3/5V SYS PWR ISL6237 P33
DISCHARGER P39 | CPU CORE PWR OZ8116LN P35
VGA CORE OZ8118 P37 | +1.05V UP6111AQDD P34

X'TAL 14.318MHz
CLOCK GENERATOR
ICS:
SELGO: SLG8SP512TTR
P2

Penryn 479
uFCPGA
P3, P4

Thermal Sensor
(G780-1P81U) P3

Fan Driver
(G991) P25

FSB
667/800/1067 Mhz

NVIDIA
N10M-GE1
VRAM DDRII
512MB P17-P23

PCIE 16X

EXT_LVDS
EXT_CRT
EXT_HDMI

SWITCH
CIRCUIT
P24

CRT P24
LVDS P24
HDMI P24

HDMI switch
(PS8101T)
P24

INT_LVDS
INT_CRT
INT_HDMI

LVDS
RGB

DDRIII
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR3
667/800 MHz

NB
Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

X4 DMI interface

HDD (SATA) *1
P25

ODD (SATA)
P25

SATA0
SATA1

SB
ICH9M
P12,P13,P14,P15

X'TAL
32.768KHz

PCI-Express
PCIE-1

Mini Card
WLAN
P26

USB8

PCIE-6

X'TAL
25MHz

Media
Cardreader
(RTS5159)
USB2 P30

Atheros
Giga-LAN
(AR8131)
P28

Card Reader
Connector
P30

Transformer P29

RJ45
P29

Ext USB Port x 2
USB 0,1 P26

Int USB Port x 1
USB 7 P26

Bluetooth
USB5 P26

CCD
USB11 P24

USB 2.0

Azalia

LPC

Audio CODEC
(CX20561) P27

EC (WPC775LDG)
P31

X'TAL
32.768KHz

SPI ROM
P31

Touch Pad
P25

K/B COON.
P31

Audio Amplifier
G1453L P27

MIC Jack
P27

Int. MIC
P27

Int.
Speaker
P27

Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, April 13, 2009	Sheet 1 of 42	

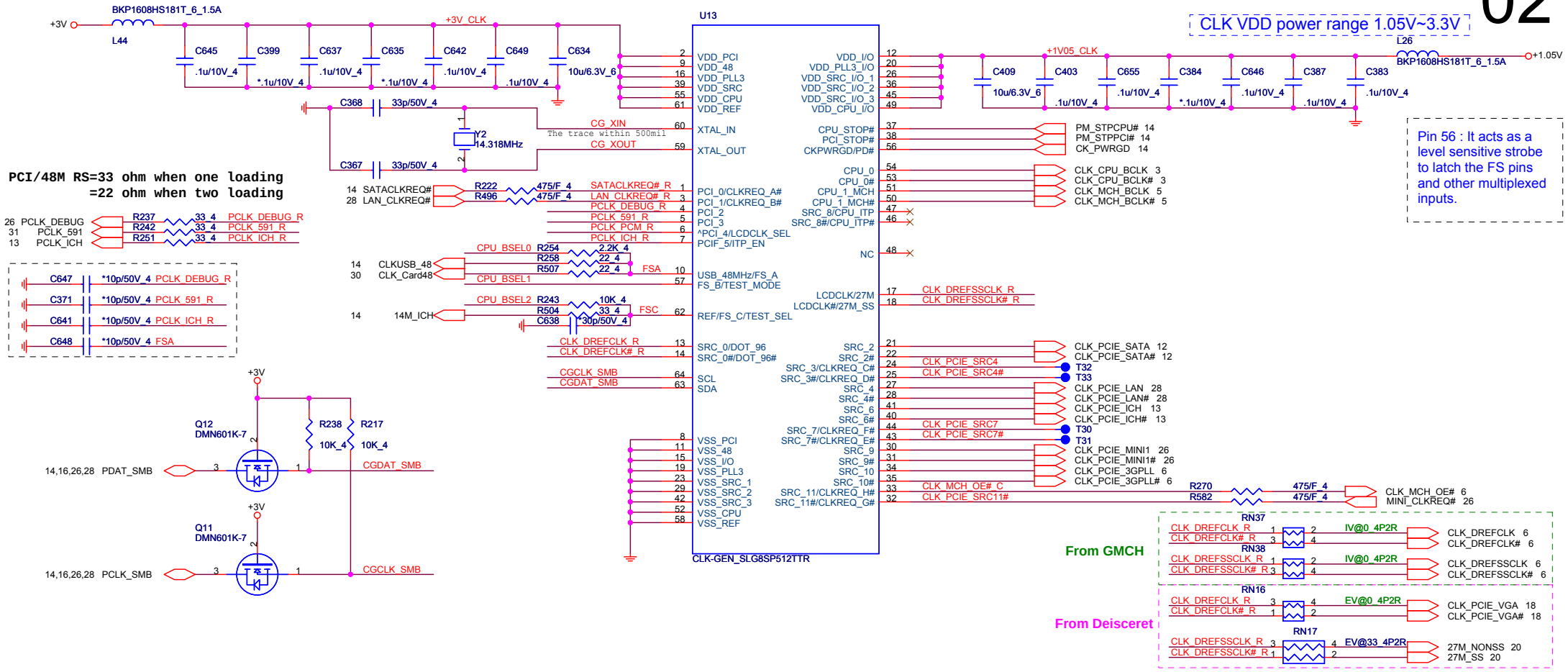
Clock Generator (CLK)

02

CLK VDD power range 1.05V~3.3V

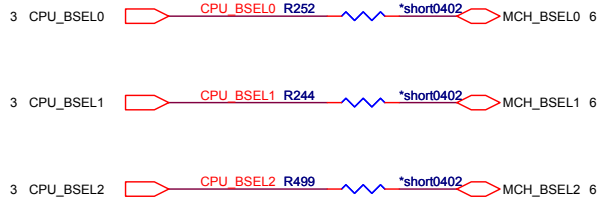
PCI/48M RS=33 ohm when one loading
=22 ohm when two loading

Pin 56 : It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.



CPU Clock select

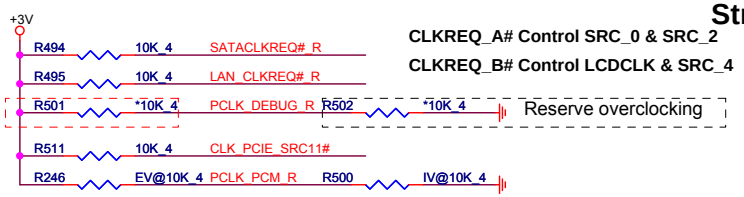
Pin 10/57/62 : For Pin CPU frequency selection



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



CLKREQ_A# Control SRC_0 & SRC_2

CLKREQ_B# Control LCDCLK & SRC_4

Reserve overclocking

Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

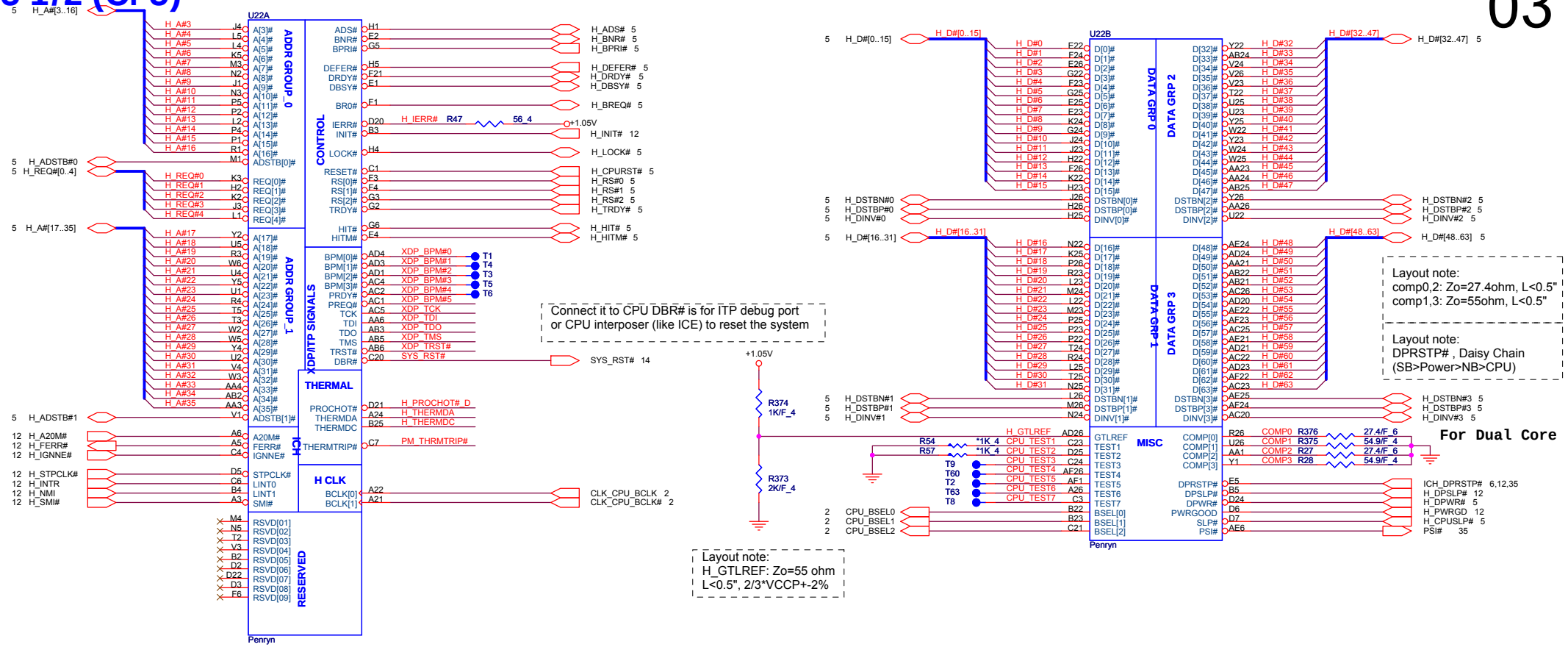
CLOCK GENERATOR

Quanta Computer Inc.
PROJECT : ZR6

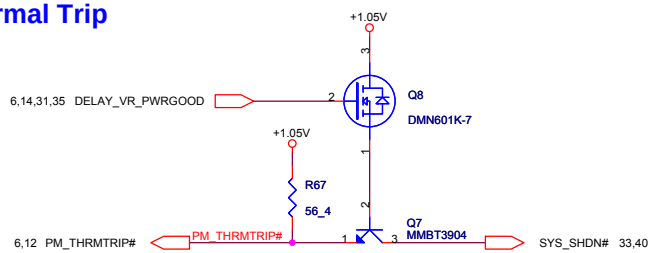
Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Monday, April 13, 2009	Sheet 2 of 42	

CPU 1/2 (CPU)

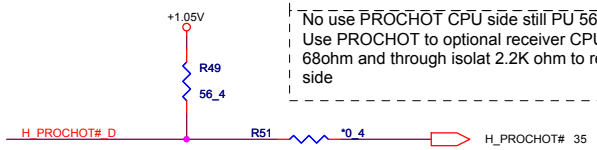
03



Thermal Trip



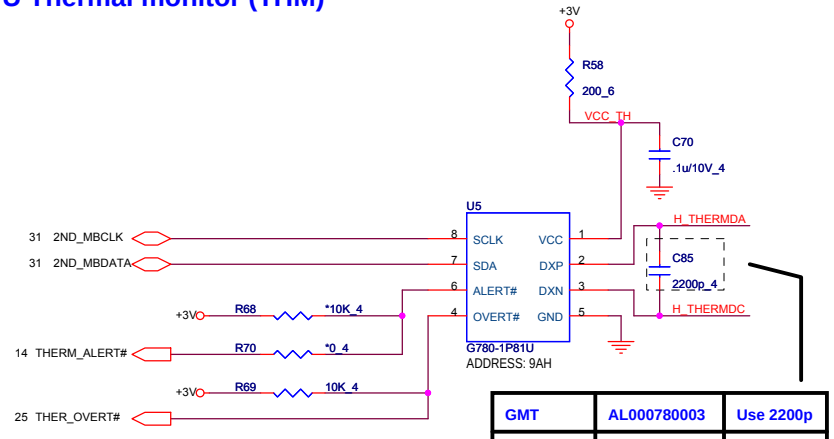
Processor hot



No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side

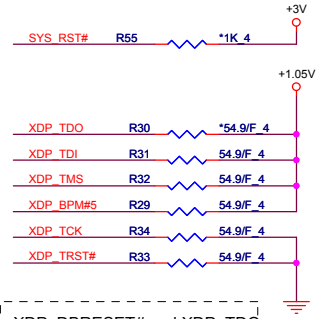
No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

CPU Thermal monitor (THM)



GMT	AL000780003	Use 2200p
WINDBOND	AL83L771001	Check

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	CPU Host Bus	1A
Date: Monday, April 13, 2009	Sheet 3 of 42	

CPU 2/2 (CPU)

04

U22D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AF25

Penryn

VCC_CORE

C25 *10u/10V_8, C49 10u/6.3V_8, C50 10u/6.3V_8, C48 *10u/10V_8, C26 10u/6.3V_8, C487 *10u/10V_8, C488 *10u/10V_8, C62 *10u/10V_8

C489 10u/6.3V_8, C495 *10u/10V_8, C496 10u/6.3V_8, C497 *10u/10V_8, C23 *10u/10V_8, C480 10u/6.3V_8, C59 *10u/10V_8, C483 *10u/10V_8

C53 *10u/10V_8, C52 *10u/10V_8, C479 *10u/10V_8, C482 10u/6.3V_8, C66 10u/6.3V_8

Layout Note:
Place these parts reference to Intel demo board.

C55 *10u/10V_8, C51 *10u/10V_8, C65 10u/6.3V_8

C63 *10u/10V_8, C64 *10u/10V_8, C60 10u/6.3V_8, C61 *10u/10V_8, C492 10u/6.3V_8, C490 *10u/10V_8

C491 10u/6.3V_8, C494 10u/6.3V_8, C498 10u/6.3V_8, C499 *10u/10V_8, C24 10u/6.3V_8, C481 *10u/10V_8

C484 *330u/2V_7343, C493 *330u/2V_7343, C58 *330u/2V_7343, C27 *330u/2V_7343

U22C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21
E12	VCC[036]	VCCP[02]	V6
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA[01]	B26
AA10	VCC[053]	VCCA[02]	C26
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AF5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AF4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AF3
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]	VCCSENSE	AF7
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AF7

Penryn

VCC_CORE

VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)

+1.05V

C57 .1u/16V_6, C56 .1u/16V_6, C54 .1u/16V_6, C500 330u/2V_7343

C67 *.1u/16V_6, C486 .1u/16V_6, C485 .1u/16V_6

VCCA:130mA

+1.5V

C69 .01u/25V_4, C68 10u/6.3V_8

H_VID0 35
H_VID1 35
H_VID2 35
H_VID3 35
H_VID4 35
H_VID5 35
H_VID6 35

R371 100/F_6 VCC_CORE

VCCSENSE 35

VSSSENSE 35

R372 100/F_6

Layout Note:
Z0=27.4,PU/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

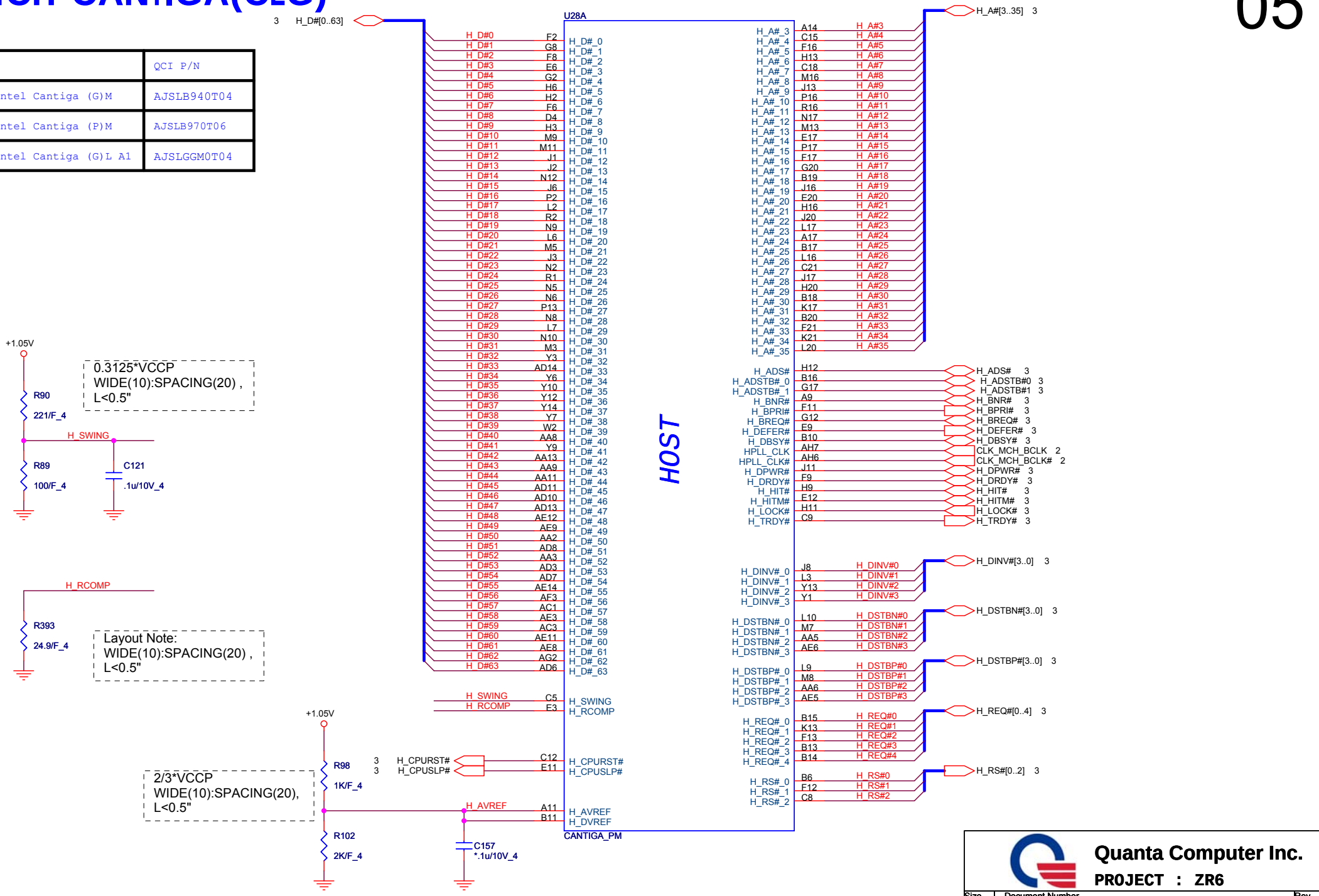
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	CPU Power	1A
Date: Monday, April 13, 2009	Sheet 4 of 42	

GMCH-CANTIGA(CLG)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	GMCH HOST	1A

Date: Monday, April 13, 2009 Sheet 5 of 42

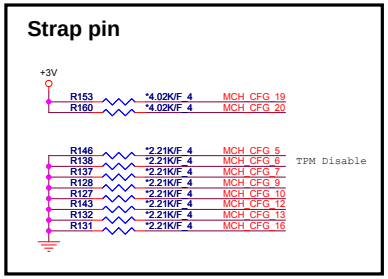
GMCH-CANTIGA(CLG)

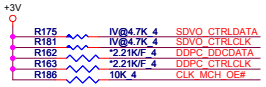
IV@
EV@

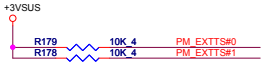
Strap table

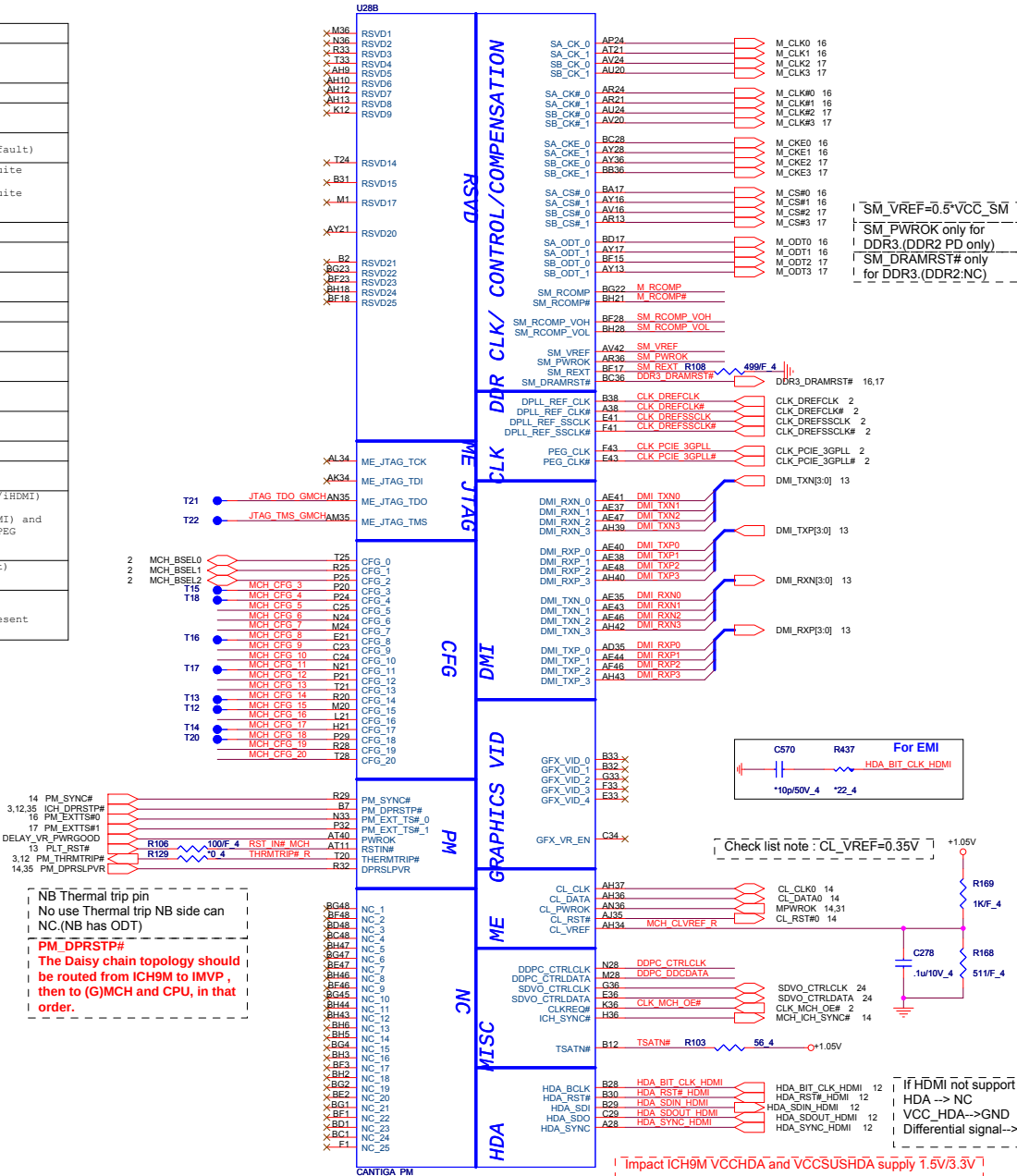
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin









SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

Check list note : CL_VREF=0.35V

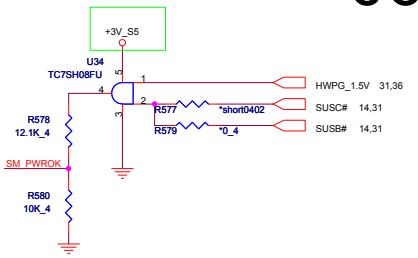
NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

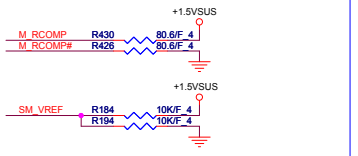
PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

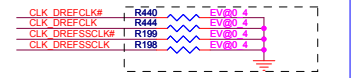
NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

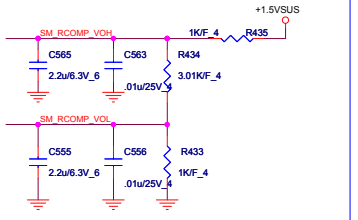




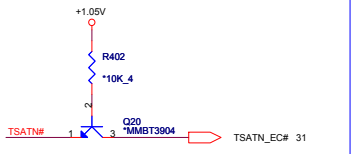
SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics





NB Thermaltrip



DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	GMCH DMI		1A
Date: Monday, April 13, 2009	Sheet 6 of 42		

GMCH-CANTIGA(CLG)

07

IV@
EV@
SP@

IV&EV Dis/Enable setting
If LVDS no use,all signal can NC

U28C

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

T37 EXP_A_COMPX R176 49.9/F_4
T36

PEG_COMPI
PEG_COMPO

24 L_BKLT_CTRL → L32 L_BKLT_CTRL
24 INT_LVDS_BLON → G32 L_BKLT_EN
R171 IV@10K_4 L_CTRL_CLK → M32 L_CTRL_CLK
+3V
R172 IV@10K_4 L_CTRL_DATA → M33 L_CTRL_DATA
24 INT_LVDS_EDIDCLK → K33 L_DDC_CLK
24 INT_LVDS_EDIDDATA → J33 L_DDC_DATA
24 INT_LVDS_DIGON → M29 L_VDD_EN
R195 IV@2.4K/F_4 LVDS_IBG → C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
24 INT_TXLCLKOUT- → INT_TXLCLKOUT- → C41 LVDSA_CLK#
24 INT_TXLCLKOUT+ → INT_TXLCLKOUT+ → C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK

24 INT_TXLOUT0- → INT_TXLOUT0- → H47 LVDSA_DATA#_0
24 INT_TXLOUT1- → INT_TXLOUT1- → E46 LVDSA_DATA#_1
24 INT_TXLOUT2- → INT_TXLOUT2- → G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3

24 INT_TXLOUT0+ → INT_TXLOUT0+ → H48 LVDSA_DATA_0
24 INT_TXLOUT1+ → INT_TXLOUT1+ → D45 LVDSA_DATA_1
24 INT_TXLOUT2+ → INT_TXLOUT2+ → F40 LVDSA_DATA_2
B40 LVDSA_DATA_3

A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3

B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm

R147 SP@75_4 INT_TV_COMP → F25 TVA_DAC
R136 SP@75_4 INT_TV_Y/G → H25 TVB_DAC
R151 SP@75_4 INT_TV_C/R → K25 TVC_DAC
H24 TV_RTN

C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TV

PCI-EXPRESS GRAPHICS

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15

PEG_RXN[15:0] 18

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AD36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15

PEG_RXP[15:0] 18,24

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_TX#_0 J41 C_PEG_TXN0 C583 .1u/10V_4 PEG_TXN0
PEG_TX#_1 M46 C_PEG_TXN1 C587 .1u/10V_4 PEG_TXN1
PEG_TX#_2 M47 C_PEG_TXN2 C591 .1u/10V_4 PEG_TXN2
PEG_TX#_3 M40 C_PEG_TXN3 C596 .1u/10V_4 PEG_TXN3
PEG_TX#_4 M42 C_PEG_TXN4 C618 EV@.1U/10V_4 PEG_TXN4
PEG_TX#_5 R48 C_PEG_TXN5 C588 EV@.1U/10V_4 PEG_TXN5
PEG_TX#_6 N38 C_PEG_TXN6 C600 EV@.1U/10V_4 PEG_TXN6
PEG_TX#_7 T40 C_PEG_TXN7 C598 EV@.1U/10V_4 PEG_TXN7
PEG_TX#_8 U37 C_PEG_TXN8 C604 EV@.1U/10V_4 PEG_TXN8
PEG_TX#_9 U40 C_PEG_TXN9 C603 EV@.1U/10V_4 PEG_TXN9
PEG_TX#_10 Y40 C_PEG_TXN10 C608 EV@.1U/10V_4 PEG_TXN10
PEG_TX#_11 AA46 C_PEG_TXN11 C594 EV@.1U/10V_4 PEG_TXN11
PEG_TX#_12 AA37 C_PEG_TXN12 C616 EV@.1U/10V_4 PEG_TXN12
PEG_TX#_13 AA40 C_PEG_TXN13 C619 EV@.1U/10V_4 PEG_TXN13
PEG_TX#_14 AD43 C_PEG_TXN14 C614 EV@.1U/10V_4 PEG_TXN14
PEG_TX#_15 AC46 C_PEG_TXN15 C593 EV@.1U/10V_4 PEG_TXN15

PEG_TXN[15:0] 18,24

PEG_TX_0 J42 C_PEG_TXP0 C580 .1u/10V_4 PEG_TXP0
PEG_TX_1 L46 C_PEG_TXP1 C585 .1u/10V_4 PEG_TXP1
PEG_TX_2 M48 C_PEG_TXP2 C590 .1u/10V_4 PEG_TXP2
PEG_TX_3 M39 C_PEG_TXP3 C597 .1u/10V_4 PEG_TXP3
PEG_TX_4 M43 C_PEG_TXP4 C611 EV@.1U/10V_4 PEG_TXP4
PEG_TX_5 R47 C_PEG_TXP5 C586 EV@.1U/10V_4 PEG_TXP5
PEG_TX_6 N37 C_PEG_TXP6 C601 EV@.1U/10V_4 PEG_TXP6
PEG_TX_7 T39 C_PEG_TXP7 C599 EV@.1U/10V_4 PEG_TXP7
PEG_TX_8 U36 C_PEG_TXP8 C605 EV@.1U/10V_4 PEG_TXP8
PEG_TX_9 U39 C_PEG_TXP9 C602 EV@.1U/10V_4 PEG_TXP9
PEG_TX_10 Y39 C_PEG_TXP10 C609 EV@.1U/10V_4 PEG_TXP10
PEG_TX_11 Y46 C_PEG_TXP11 C595 EV@.1U/10V_4 PEG_TXP11
PEG_TX_12 AA36 C_PEG_TXP12 C617 EV@.1U/10V_4 PEG_TXP12
PEG_TX_13 AA39 C_PEG_TXP13 C620 EV@.1U/10V_4 PEG_TXP13
PEG_TX_14 AD42 C_PEG_TXP14 C615 EV@.1U/10V_4 PEG_TXP14
PEG_TX_15 AD46 C_PEG_TXP15 C592 EV@.1U/10V_4 PEG_TXP15

PEG_TXP[15:0] 18,24

24 INT_CRT_BLU → INT_CRT_BLU → E28 CRT_BLUE
24 INT_CRT_GRN → INT_CRT_GRN → G28 CRT_GREEN
24 INT_CRT_RED → INT_CRT_RED → J28 CRT_RED
G29 CRT_IRTN

24 INT_CRT_DDCCLK → H32 CRT_DDC_CLK
24 INT_CRT_DDCDAT → J32 CRT_DDC_DATA
24 INT_HSYNC → R158 IV@30.1_4 HSYNC_G → J29 CRT_HSYNC
CRTIREF E29 CRT_TVO_IREF
24 INT_VSYNC → R165 IV@30.1_4 VSYNC_G → L29 CRT_VSYNC

VGA

HSYNC/VSYNC serial R place close to NB

CANTIGA_PM

Discrete Stuffed. (CRT)
HSYNC_G
VSYNC_G
R159 EV@0_4
R166 EV@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F

IV&EV Dis/Enable setting
<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm
R161 SP@1K/F_4 CRTIREF

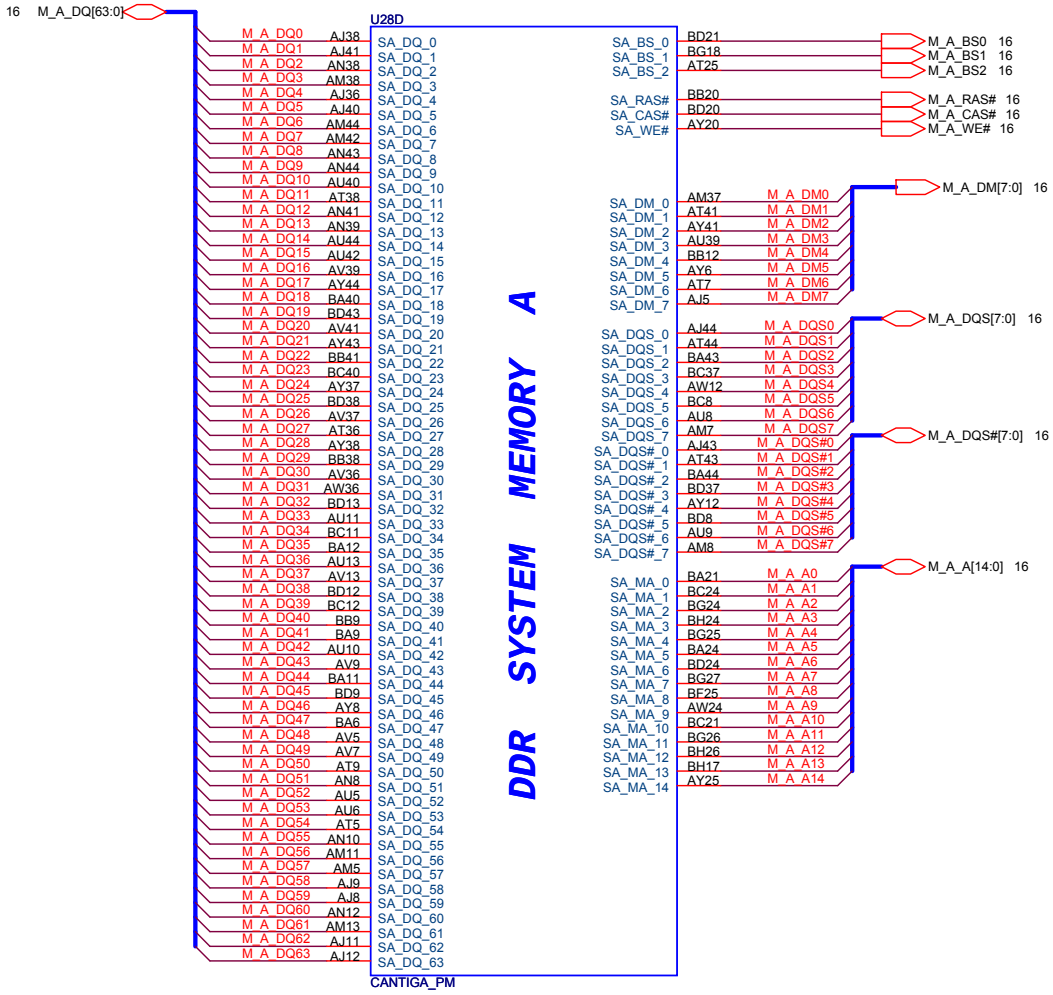
SP@
CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R155 SP@150/F_4 INT_CRT_BLU
R154 SP@150/F_4 INT_CRT_GRN
R150 SP@150/F_4 INT_CRT_RED

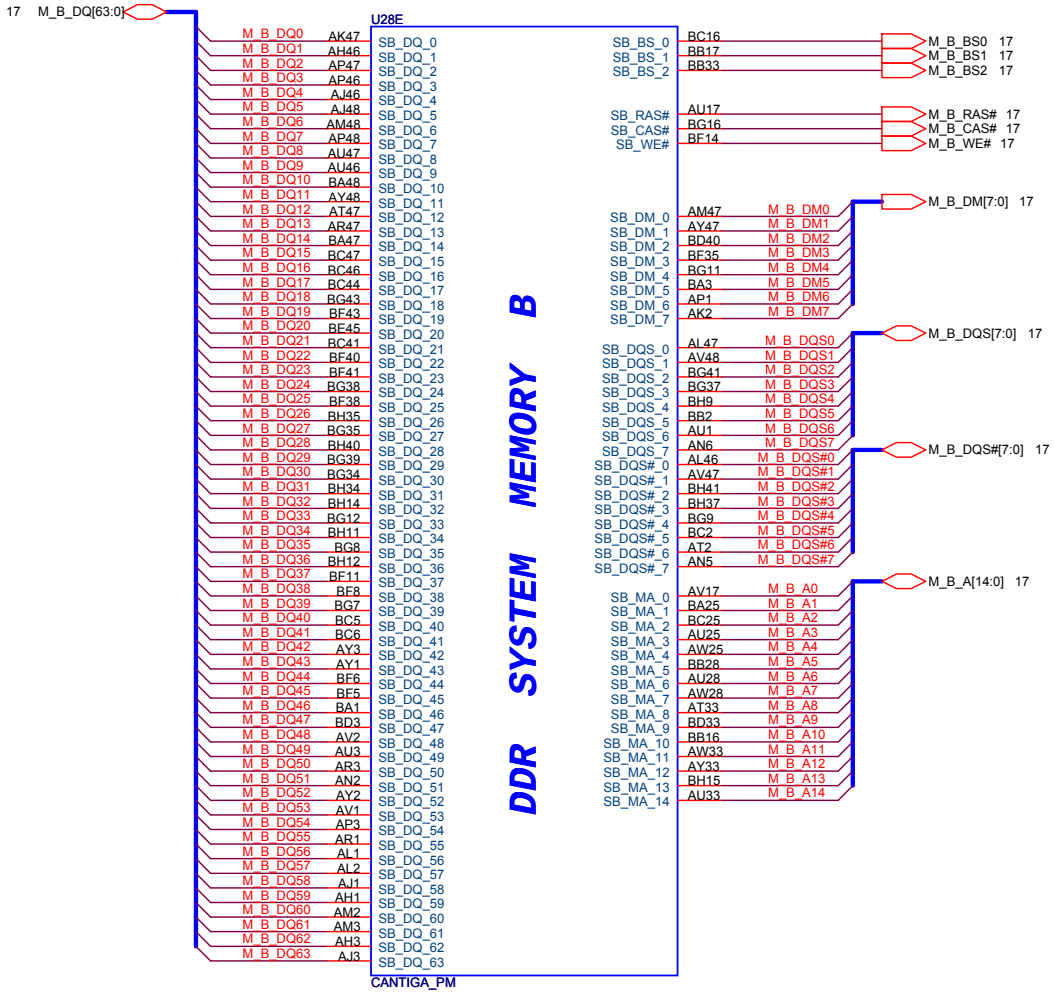
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	GMCH VGA	1A
Date: Monday, April 13, 2009	Sheet 7 of 42	

GMCH-CANTIGA(CLG)

08





Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	GMCH DDRIII	1A
Date: Monday, April 13, 2009	Sheet 8 of 42	

GMCH-CANTIGA(CLG)

IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+1.5VSUS

C606 22u/6.3V_8 | C612 *22u/6.3V_8 | C264 .1u/10V_4 | C624 330u/2V_7343

VCC_SM(1.5V) DDR3

U28G

VCC SM POWER

AP33 AN33 BH32 BG32 BF32 BD32 BC32 BB32 BA32 AY32 AW32 AV32 AU32 AT32 AR32 AP32 AN32 BH31 BG31 BF31 BG30 BH29 BG29 BF29 BD29 BC29 BB29 BA29 AY29 AW29 AV29 AU29 AT29 AR29 AP29 — VCC_SM_1 … VCC_SM_35

BA36 BB24 BD16 BB21 AW16 AW13 AT13 — VCC_SM_36/NC … VCC_SM_42/NC

+1.05V_AXG

VCC GFX NCTF POWER

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60 — W28 V28 W26 V26 W25 V25 W24 V24 W23 V23 AM21 AL21 AK21 W21 V21 U21 AM20 AK20 W20 U20 AM19 AL19 AK19 AJ19 AH19 AG19 AF19 AE19 AB19 AA19 Y19 W19 V19 U19 AM17 AK17 AH17 AG17 AE17 AC17 AB17 Y17 W17 V17 AM16 AL16 AK16 AJ16 AH16 AG16 AF16 AE16 AC16 AB16 AA16 Y16 W16 V16 U16

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between
the Graphics Core Rail,
VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL,
VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL,
VCCA_SM, VCC_AXF

+1.05V_AXG

Y26 AE25 AB25 AA25 AE24 AC24 AA24 Y24 AE23 AC23 AB23 AA23 AJ21 AG21 AE21 AC21 AA21 Y21 AH20 AF20 AE20 AC20 AB20 AA20 T17 T16 AM15 AL15 AE15 AJ15 AH15 AG15 AF15 AB15 AA15 Y15 V15 U15 AN14 AM14 U14 T14 — VCC_AXG_1 … VCC_AXG_42

VCC GFX

+1.05V_AXG

IV@ R112 IV@10/F_4 | R110 IV@10/F_4

AJ14 AH14 — VCC_AXG_SENSE VSS_AXG_SENSE

VCC SM LF

VCC_SM_LF1 … VCC_SM_LF7 — AV44 BA37 AM40 AV21 AY5 AM10 BB13

1.8V
Internal connect to power

C163 .1u/10V_4 | C151 .1u/10V_4 | C142 .22u/6.3V_4 | C211 .22u/6.3V_4 | C292 .47u/6.3V_4 | C290 1u/10V_4 | C319 1u/10V_4

CANTIGA_PM

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

+1.05V

C267 .1u/10V_4 | C283 *.22u/6.3V_4 | C266 .22u/6.3V_4 | C286 22u/6.3V_8 | C610 330u/2V_7343

Place close to
the GMCH

U28F

VCC CORE POWER

AG34 AC34 AB34 AA34 Y34 V34 U34 AM33 AK33 AJ33 AG33 AF33 — VCC_1 … VCC_12

AE33 AC33 AA33 Y33 W33 V33 U33 AH28 AF28 AC28 AA28 AJ26 AG26 AE26 AC26 AH25 AG25 AF25 AG24 AJ23 AH23 AF23 — VCC_13 … VCC_34

T32 — VCC_35

+1.05V

VCC_NCTF_1 … VCC_NCTF_44 — AM32 AJ32 AK32 AJ32 AH32 AG32 AE32 AC32 AA32 Y32 W32 U32 AM30 AL30 AK30 AH30 AG30 AF30 AE30 AC30 AB30 AA30 Y30 W30 V30 U30 AL29 AK29 AJ29 AH29 AG29 AE29 AC29 AA29 Y29 W29 V29 AL28 AK28 AL26 AK26 AK25 AK24 AK23

VCC NCTF

CANTIGA_PM

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

+1.05V +1.05V_AXG

IV@ R156 IV@0_8 | R83 IV@0_8 | R80 IV@0_8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG

+C505 IV@330u/2V_7343 | +C501 IV@330u/2V_7343 | C219 IV@.47u/6.3V_4 | SP@ C168 SP@1u/10V_6 | C149 IV@10u/6.3V_8 | C187 IV@22u/6.3V_8 | C223 IV@.1u/10V_4 | C107 IV@.1u/10V_4 | C166 IV@.1u/10V_4

Place close to the GMCH

SP@:IV Sutff 1uf
EVstuff 0 ohm

Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

Date: Monday, April 13, 2009 Sheet 9 of 42

GMCH-CANTIGA(CLG)

Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

If CRT have Flicker issue STUFF 5.6 ohm

IV&EV Dis/Enable setting

SP@:INT use 0.01U EXT use 0 ohm

SP@:INT use 0.1U EXT use 0 ohm

1210 10UH, 10% 0.45A DCR_max = 0.39

1.05V 64.8mA for DPLL_A/B

VCCA_DPLLA/B always keep to +1.05V (If no use IV dynamic core power)

USE same GND plane

1.05V 24mA

1.8V 13.2mA

1.5V 414uA

3.3V 73mA

3.3V 5mA

1.05V 139.2mA

1.05V DDR2-800 720mA

1.05V 50mA

VCCA_PEG_PLL +1.25V for Teenah use(100mA)

1.05V DDR2-800 26mA

3.3V 24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

CRB : 0 ohm
Check list : 2.2nH

3.3V 79mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V 50mA

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V 35mA

VCCD_QDAC share to TV and CRT

1.5V 48.363mA for CRT
5mA for TV

1.5V 0.5mA

CRB no 10U
Check list need min 10U~100U for VCCA_QDAC

MODIFY

1.05V 50mA

1.8V 60.31mA

SP@:INT use 1 U EXT use 0 ohm

1.05V 157.2mA

1.05V FSB-1067 852mA

1.05V 321.35mA

1.8V DDR2-800 124mA

1.8V 118.8mA

3.3V 105.3mA

1.05V 1782mA

1.05V 456mA

1.05V Internal connect to power

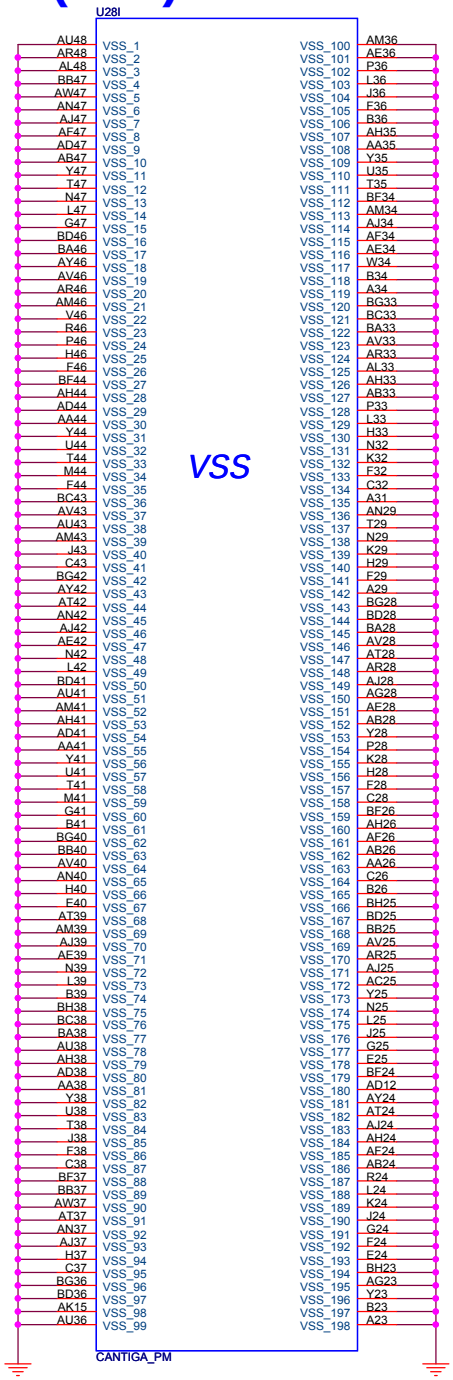
External Graphics (GMCH Integrated Graphics Disable)

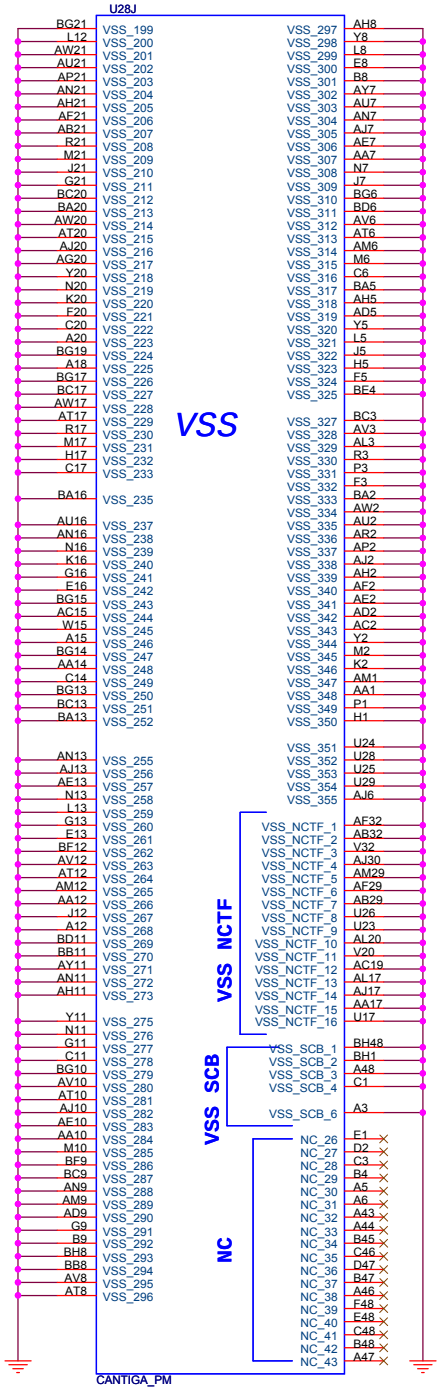
VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number	Rev
	GMCH POWER	1A
Date: Monday, April 13, 2009	Sheet 10 of 42	

GMCH-CANTIGA(CLG)



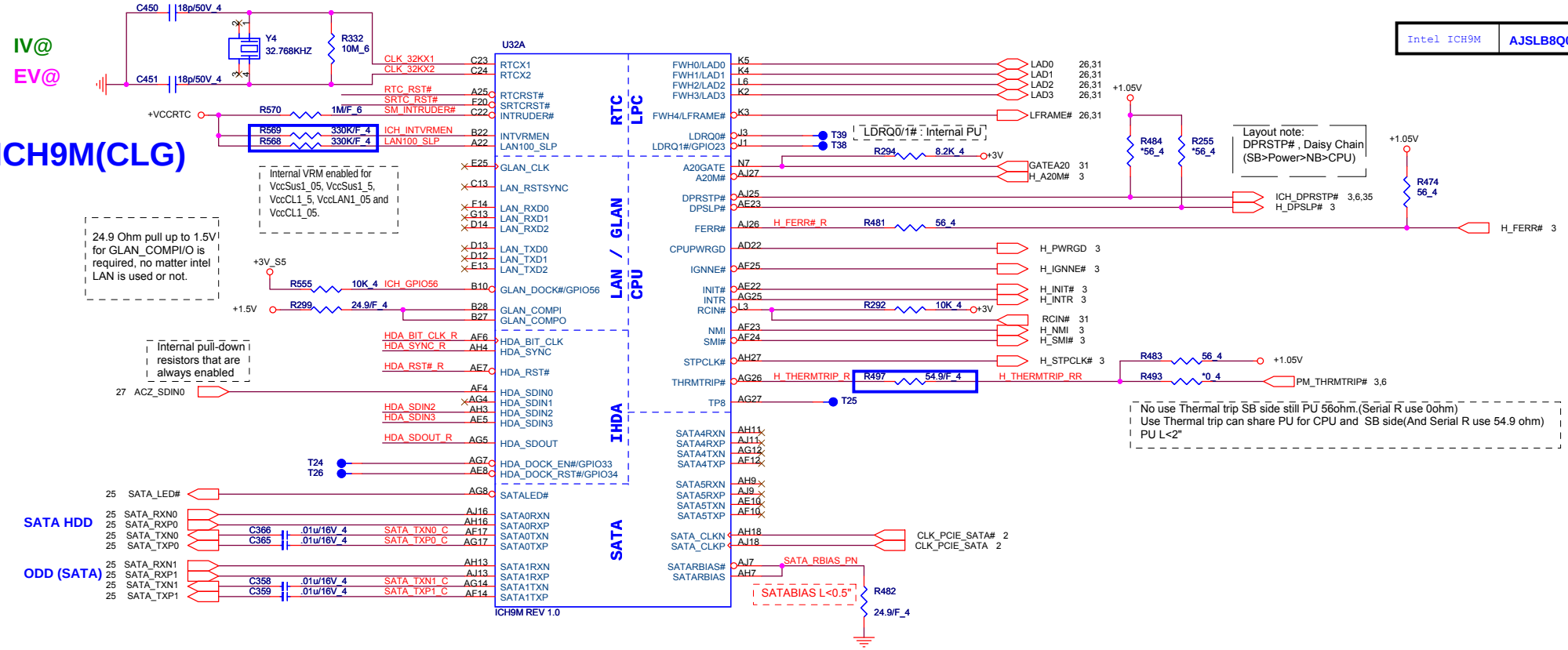


Quanta Computer Inc.	
PROJECT : ZR6	
Size	Document Number: GMCH VSS
Rev	1A
Date: Monday, April 13, 2009	Sheet 11 of 42

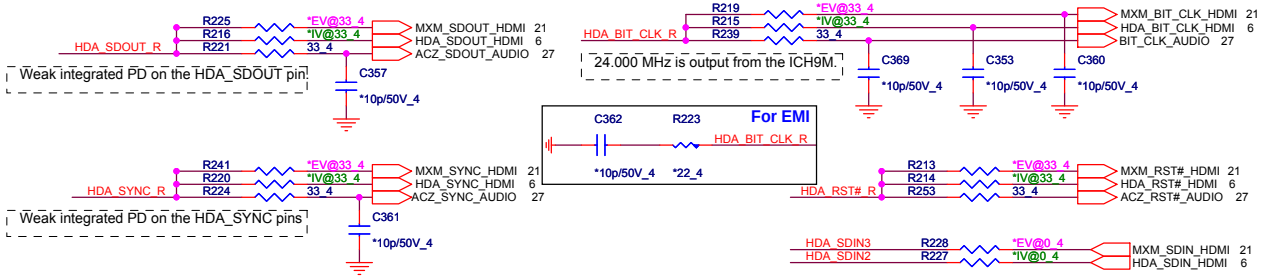
IV@

EV@

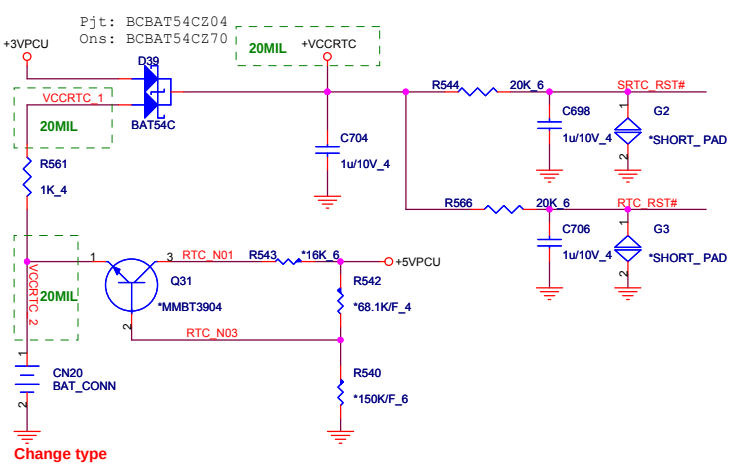
ICH9M(CLG)



HD Audio



RTC



South Bridge Strap Pin (1/3)

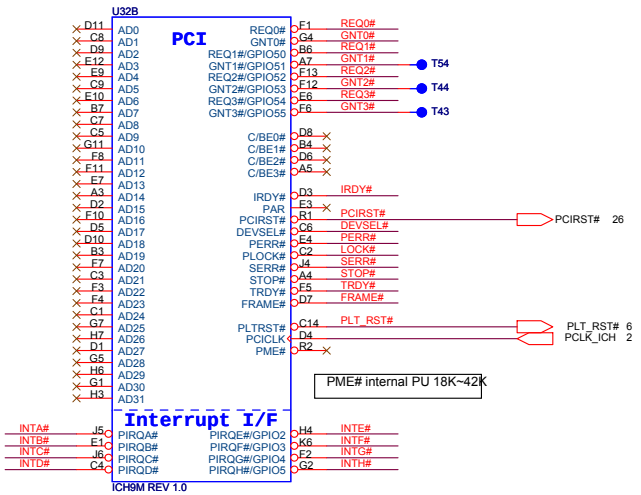
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	14 ICH_TP3 — ICH_TP3 — R545 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R240 *1K_4 — +3V

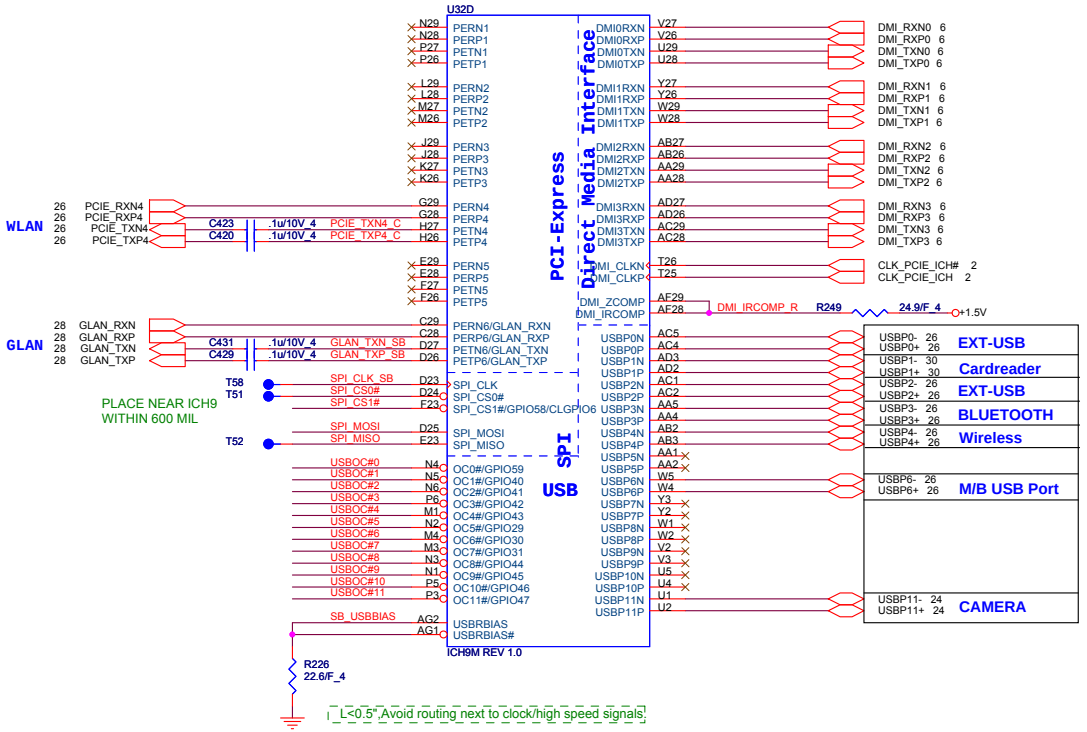
Quanta Computer Inc.

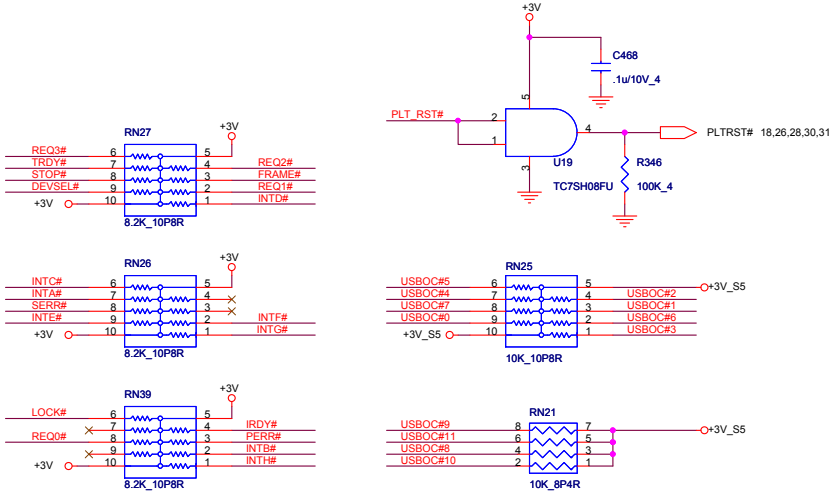
PROJECT : ZR6

Size	Document Number	Rev
	ICH9M HOST	1A
Date: Monday, April 13, 2009	Sheet 12 of 42	

ICH9M(CLG)







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R309 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R277 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R293 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R274 *1K_4

Quanta Computer Inc.
PROJECT : ZR6
Size | Document Number: ICH9M PCIE / PCI / USB | Rev 1A
Date: Monday, April 13, 2009 | Sheet 13 of 42

ICH9M(CLG)

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground

For EMI(EMI)
C428 *10p/50V_4 R288 *22_4 14M_ICH
C377 *10p/50V_4 R250 *22_4 CLKUSB_48

<Checklist ver0.8>
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs
on the NB and SB on a platform with no IAMT

PWRBTN : 16 ms of internal debounce logic on this pin and internal PU 24K

TPM Physical Presence for iTPM.

Stuff	HDMI SET
R583	HDMI
R315	No HDMI

ZS2 Default not support IAMT. So this interface follow CRB/Checklist PU only

ICH9M REV 1.0

CL VREF

VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

CL_VREF1_SB: R563 *3.24K/F_6, R558 *453/F_4, C700 *.1u/10V_4
CL_VREF0_SB: R319 3.24K/F_6, R313 453/F_4, C436 .1u/10V_4

Follow CHECK LIST V1.5

ICH PWROK

DELAY_VR_PWRGOOD need PU 2K to +3V.
ZS2 PU at power side

C430 *.1u/10V_4, U15 TC7SH08FU, R289 100K_4
ICH_PWROK → DELAY_VR_PWRGOOD 3,6,31,35
PWROK_EC → PWROK_EC 31

Resume RST

PM_RSMRST# R → Q17 MMBT3906 → RSMRST# 31
R329 10K_4, R291 4.7K_4 +3V_S5
D36 BAV99, D26 BAV99, R314 2.2K_4

ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

ID0=0 -->ZK6 ,ID0=1 -->ZR6
ID1=0 -->UMA ,ID1=1 -->Discrete

R492 *10K_4 BOARD_ID3, R491 10K_4
R487 *10K_4 BOARD_ID2, R488 10K_4
R298 EV@10K_4 BOARD_ID1, R308 IV@10K_4
R230 10K_4 BOARD_ID0, R229 *10K_4

Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R271 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R485 *1K_4

CLK Enable

C419 *.1u/10V_4, U20 NC7SZ04
35 VR_PWRGD_CK410# → VR_PWRGD_CLKEN
R339 100K_4

Quanta Computer Inc.
PROJECT : ZR6
Size | Document Number: ICH9M GPIO | Rev 1A
Date: Monday, April 13, 2009 | Sheet 14 of 42

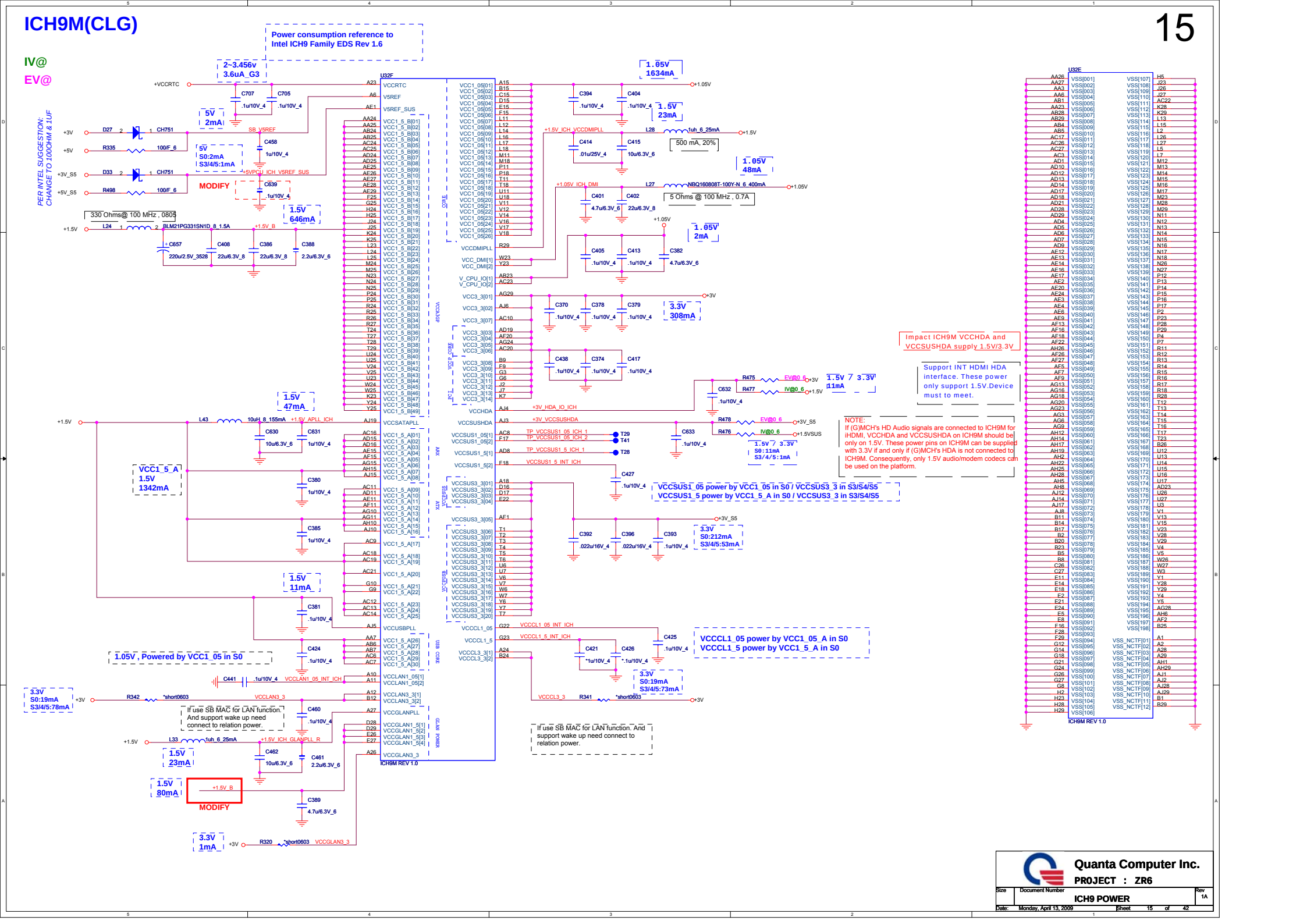
ICH9M(CLG)

IV@

EV@

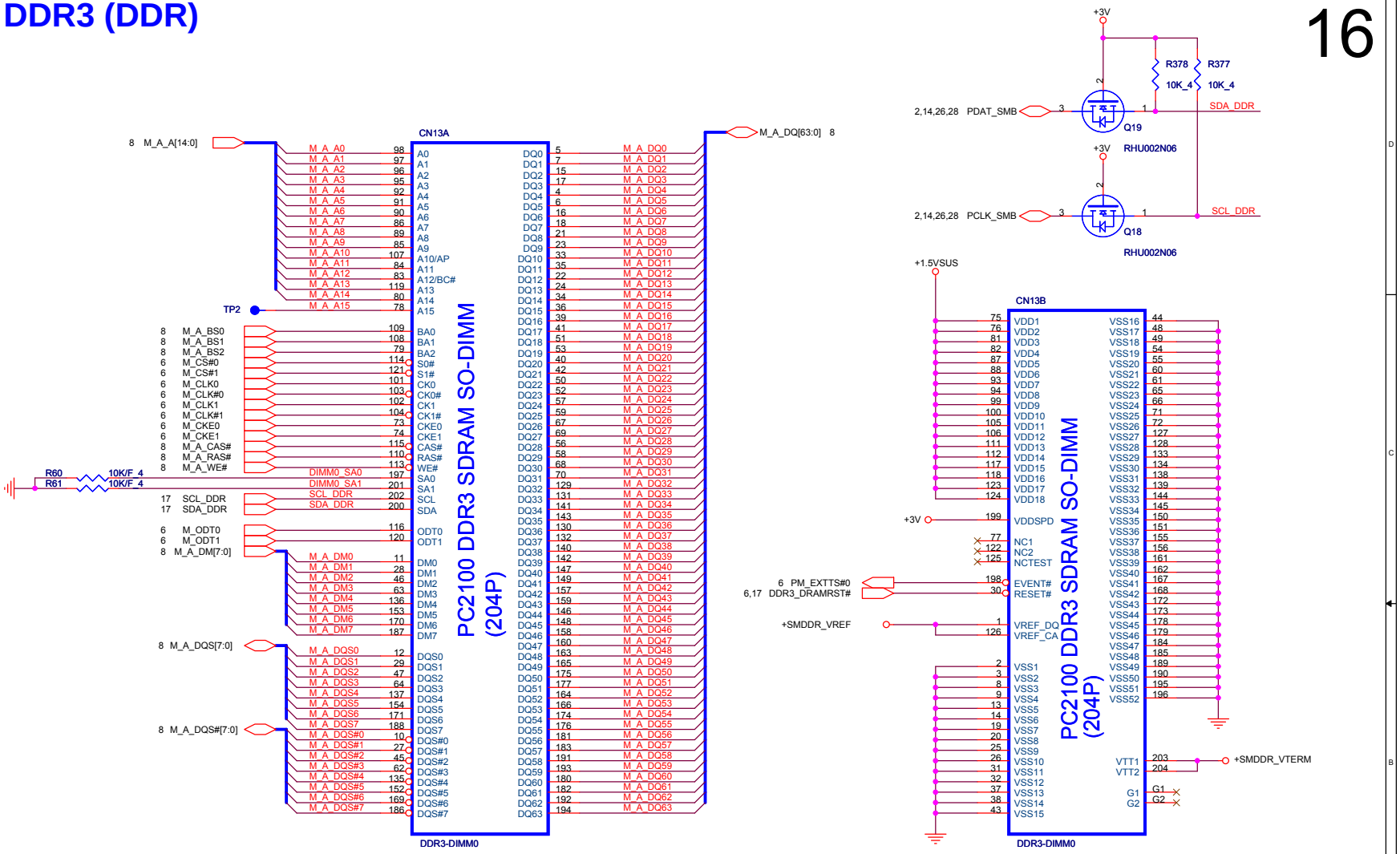
Power consumption reference to Intel ICH9 Family EDS Rev 1.6

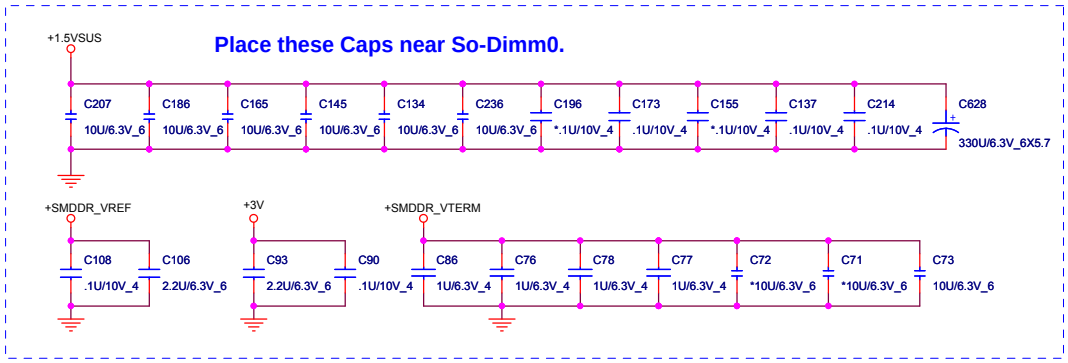
PER INTEL SUGGESTION: CHANGE TO 1000HM & 1UF

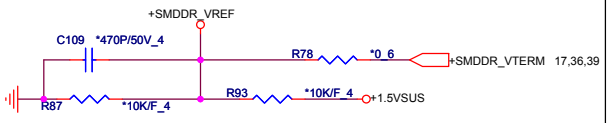


Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number	ICH9 POWER	Rev 1A
Date: Monday, April 13, 2009	Sheet 15 of 42		

DDR3 (DDR)

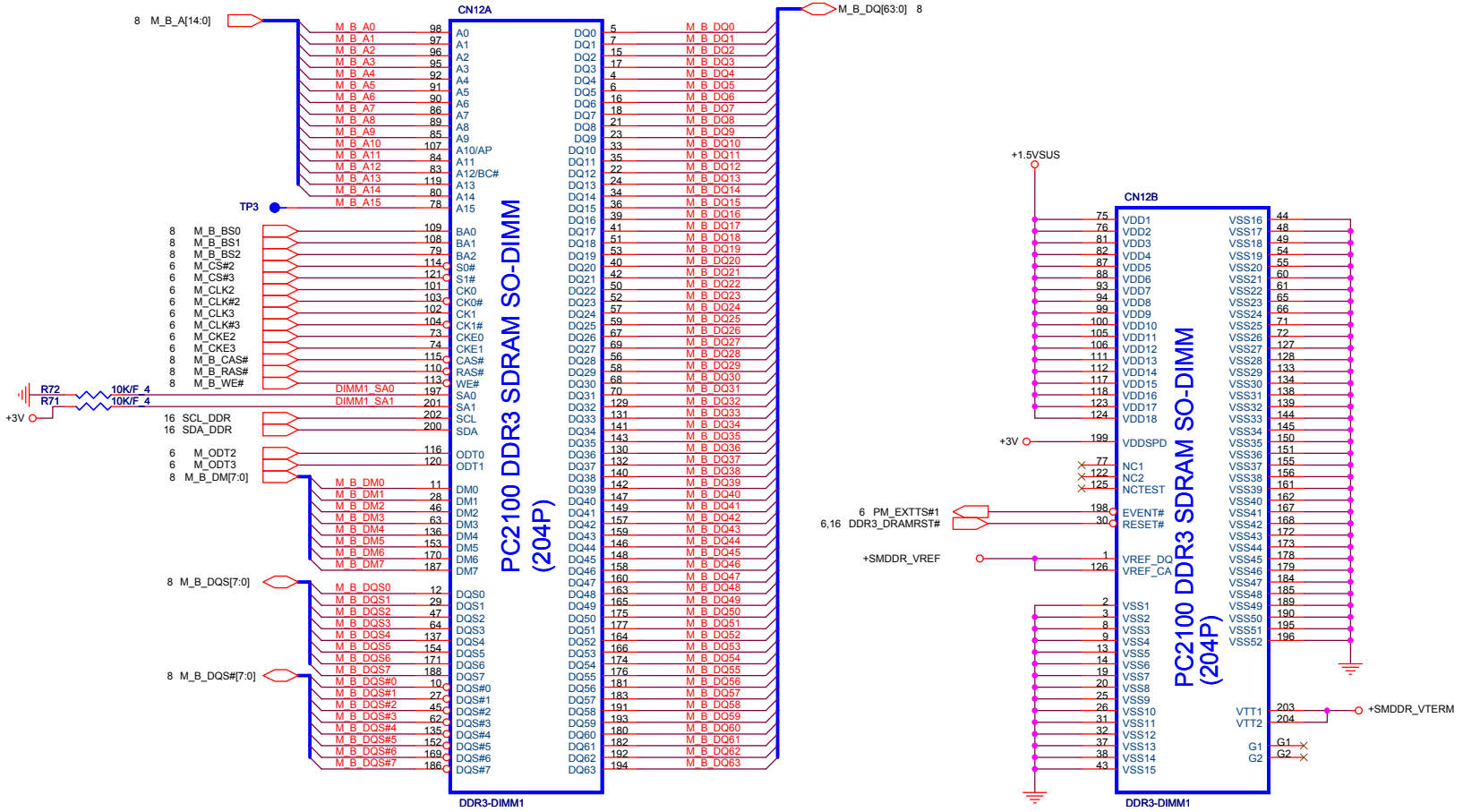


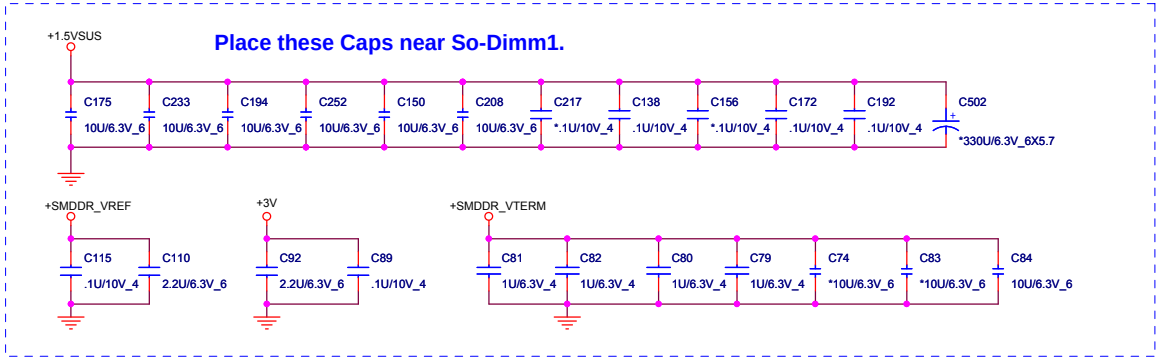




Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: DDR3 DIMM-0(H=5.2)	Rev: 1A
Date: Monday, April 13, 2009	Sheet 16 of 42	

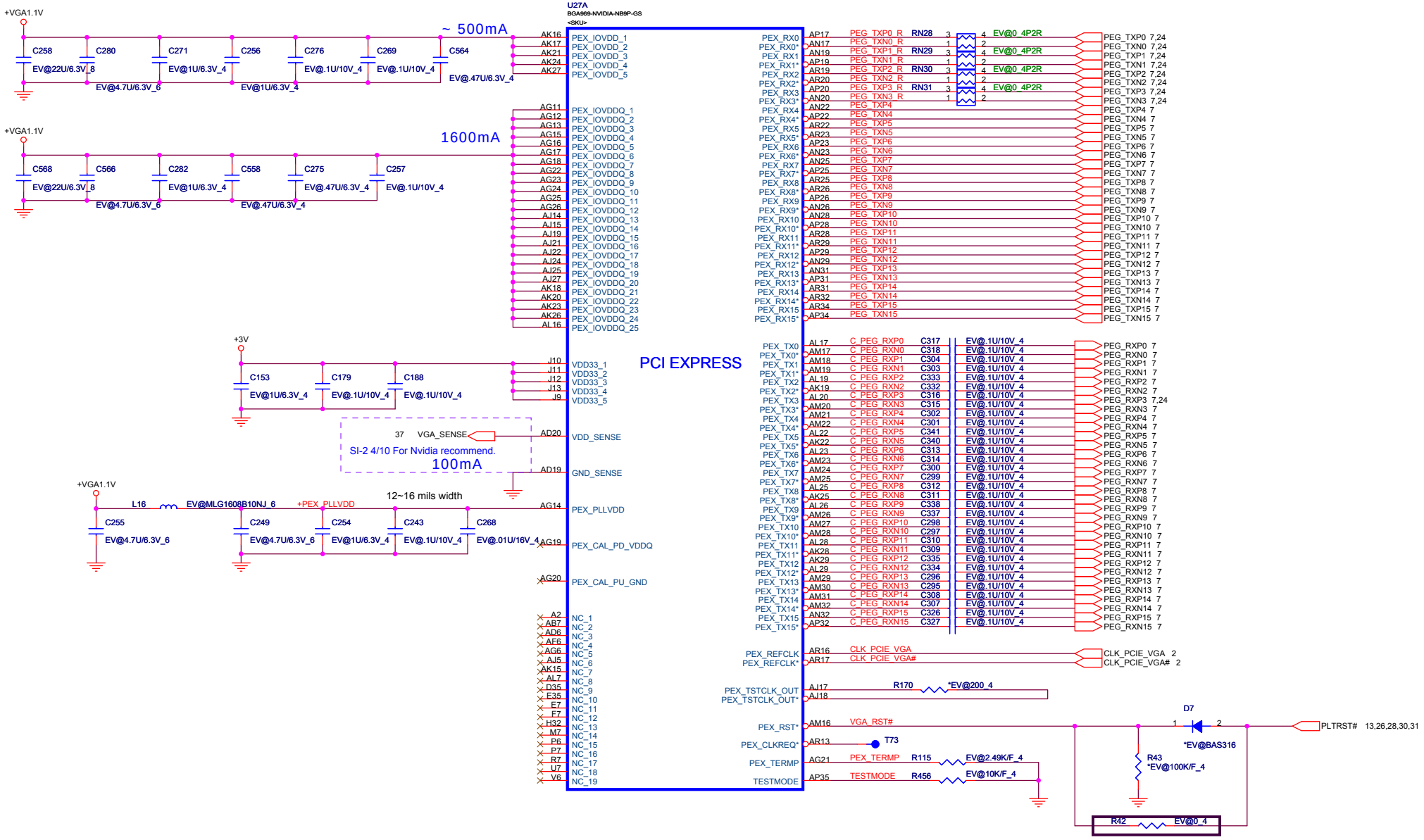
DDR3 (DDR)





Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: DDR3 DIMM-1(H=9.2)	Rev: 1A
Date: Monday, April 13, 2009	Sheet 17 of 42	

NV10M (VGA)



Quanta Computer Inc.
PROJECT : ZR6
Size | Document Number | Rev
NV10X (PCIE I/F) 1/5 | 1A
Date: Monday, April 13, 2009 | Sheet 18 of 42

NV10M (VGA)

U27B
BGA969-NVIDIA-NB9P-GS
<SKU>

MEMORY I/F A

U27C
BGA969-NVIDIA-NB9P-GS
<SKU>

MEMORY I/F B

Add for 64x16 vram

for DDR2 need use CMD11(CKE) and CMD12(ODT)

use internal Vref, ext divider no stuff

15mils width

For Debug only

R91 Install for DDR3

R86 no stuff

G96 only

Quanta Computer Inc.
PROJECT : ZR6
Size | Document Number: NV10X (MEMORY I/F) 2/5 | Rev 1A
Date: Monday, April 13, 2009 | Sheet 19 of 42

NV10M (VGA)

U27D

BGA969-NVIDIA-NB9P-GS

<SKU>

IFPAB(LVDS)

100 mA

50 mA

50 mA

IFPCD / IFPC / IFPD

TMDS channel two

IFPEF

Display port output

DACA(CRT)

DACC(CRT2)

DACB(TV)

SI Build

XTAL_PLL

65mA

50mA

25mA

SPREAD SPECTRUM

SI Build

I2C ADDRESS: 0xD4H

NVidia suggest:
10 kΩ pull-down only if
no spread chip used.

Close to GPU

Quanta Computer Inc.	
PROJECT : ZR6	
Size	Document Number: NV10X (DISPLAY) 3/5 — Rev: 1A
Date: Monday, April 13, 2009	Sheet 20 of 42

NV10M (VGA)

N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR

SEE Datasheet for details on G10x Straps!

NVidia Propose Remove C3134,C3681,R3092,R3402,R3063,R3064,C3076

Delete T31

HD Audio Level :3V

SI Build

PCI_DEVID: STRAP2			
NB9M-GE	0x06E	8	1000
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	0x064	9	1001
N10P-GE1	0x065	2	0010
N10M-GE1	0x06E	C	1100 default

Logical Strap Bit Mapping

R414 PU-VDD	PD
5K 1000	0000
10K 1001	0001
15K 1010	0010
20K 1011	0011
25K 1100	0100
30K 1101	0101
35K 1110	0110
45K 1111	0111

R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E

I2C ADDRESS: 0x98H

VGA THERMAIL CIRCUIT Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

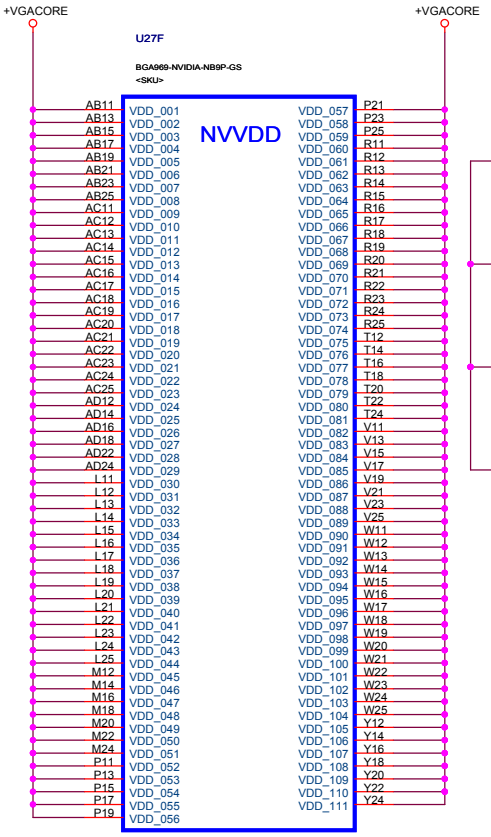
SI Build

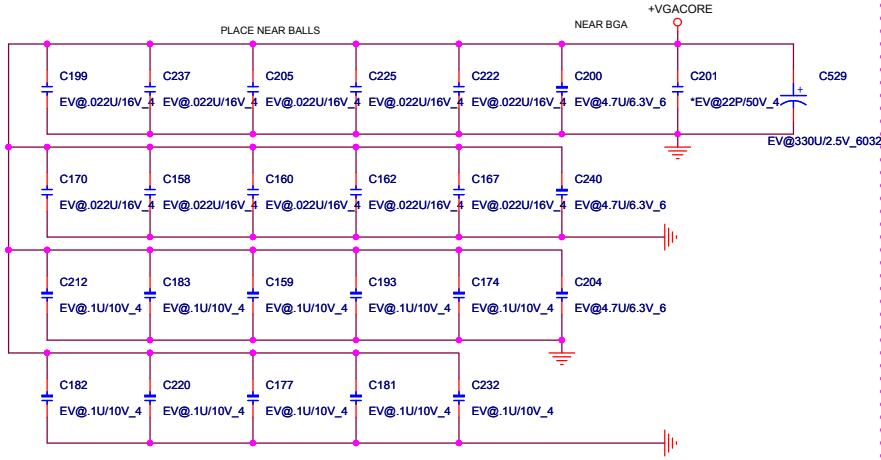
Waiting Confirm from Nvidia

NVidia Request

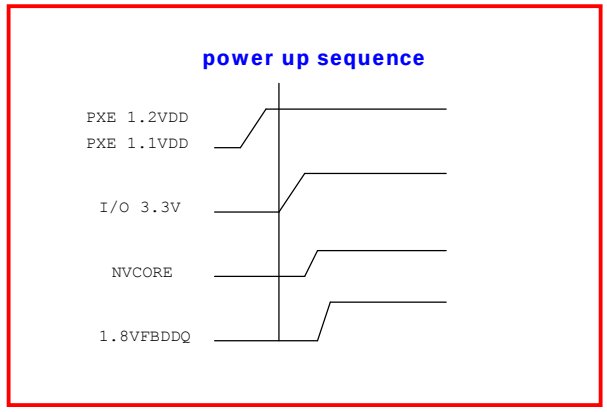
Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: NV10X (GPIO & STRRAPS) 4/5	Rev 1A
Date: Monday, April 13, 2009	Sheet 21 of 42	

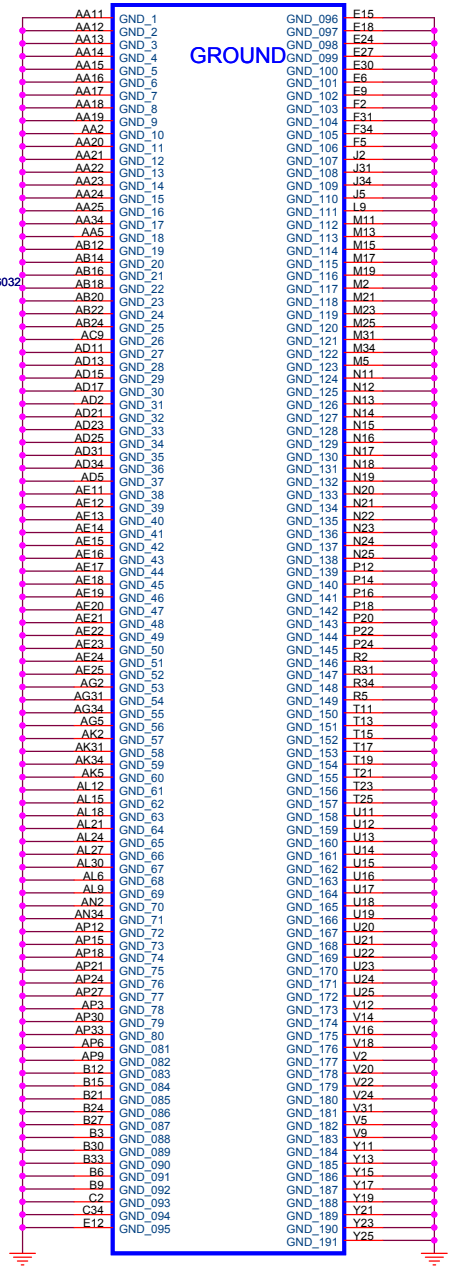
NVVDD Decoupling





Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10



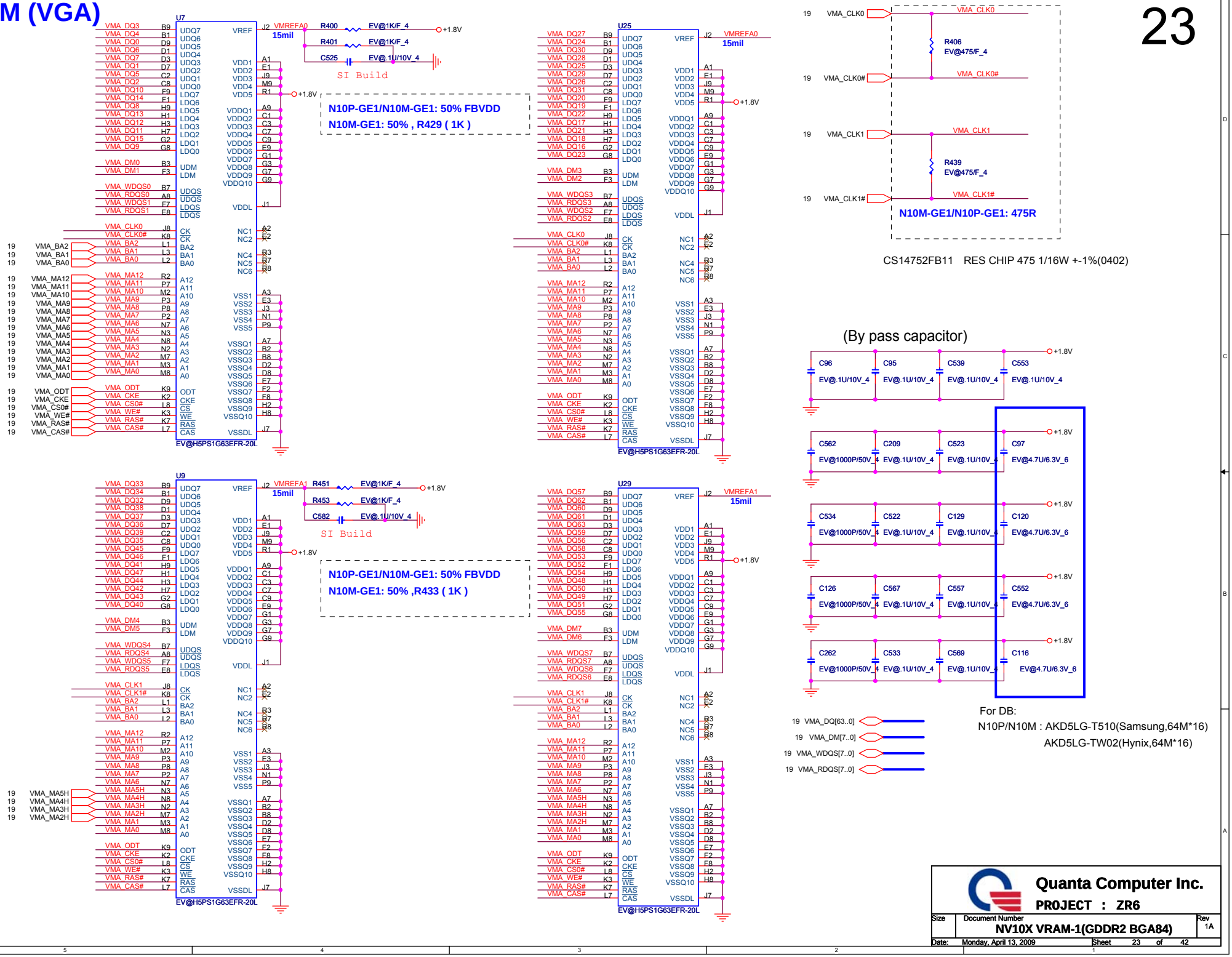


Quanta Computer Inc.

PROJECT : ZR6

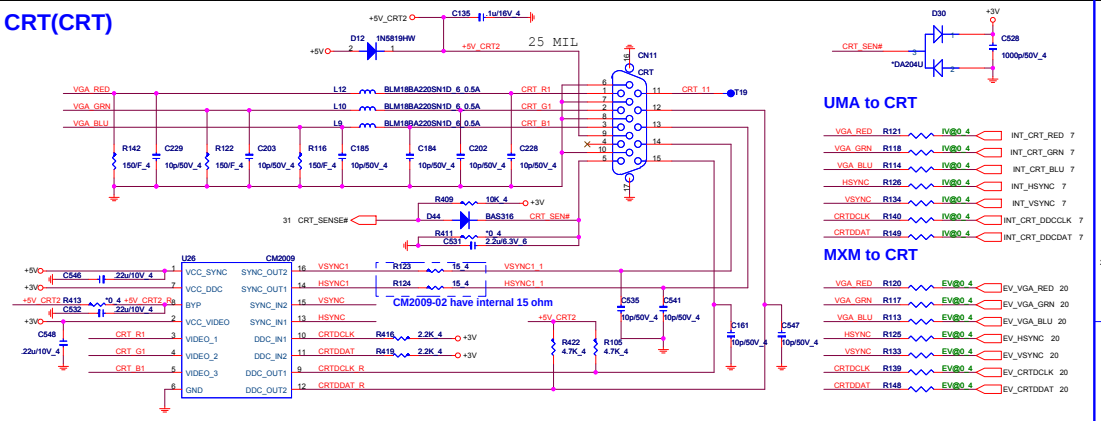
Size	Document Number	Rev
	NV10X (POWER & GND) 5/5	1A
Date: Monday, April 13, 2009	Sheet 22 of 42	

NV10M (VGA)



Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	NV10X VRAM-1(GDDR2 BGA84)		1A
Date: Monday, April 13, 2009		Sheet 23 of 42	

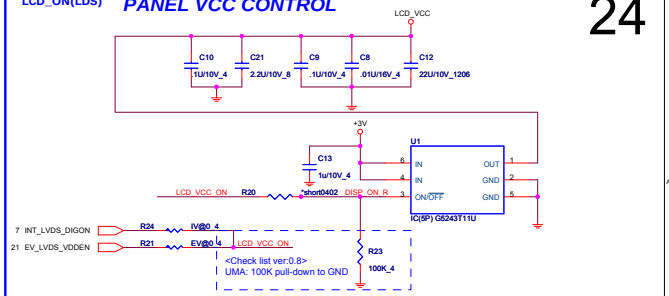
CRT(CRT)



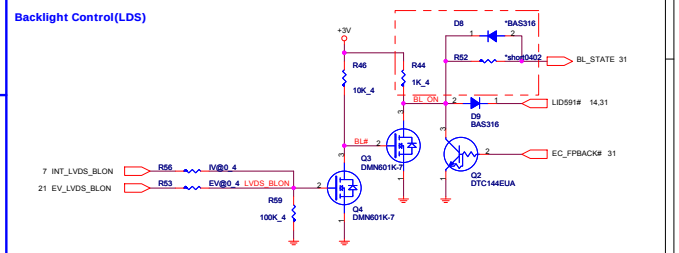
UMA to CRT

MXM to CRT

LCD_ON(LDS) PANEL VCC CONTROL



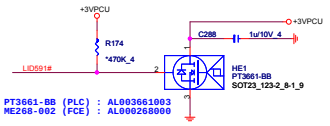
Backlight Control(LDS)



LVDS(LDS)

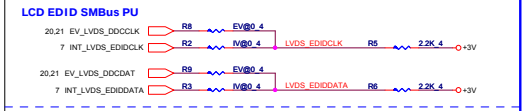
BRIGHTNESS
DPST

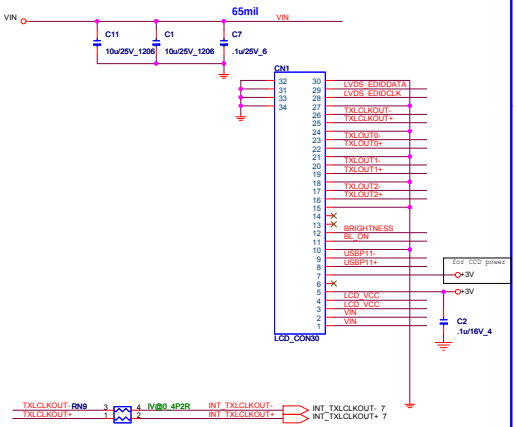
Lid Switch (HSR)

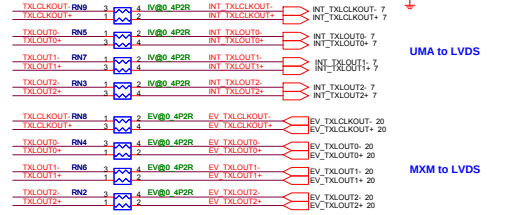


PT3661-BB (PLC) : AL003661003
ME268-002 (FCE) : AL000268000

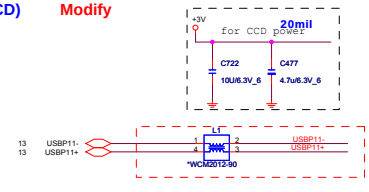
LCD EDID SMBus PU





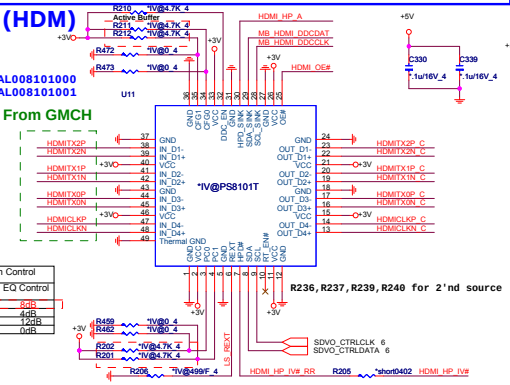


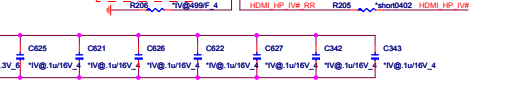
Camera(CCD) Modify

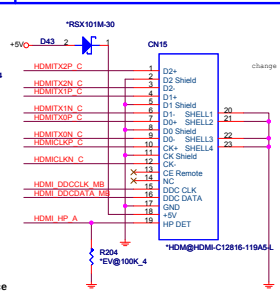


HDMI(HDM)

PS8101 : AL008101000
PS8101T : AL008101001

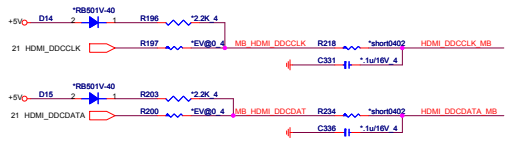




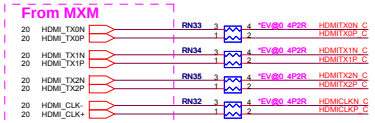


FOR UMA iHDMI HPD

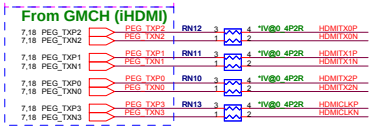
SDVO I2C Control



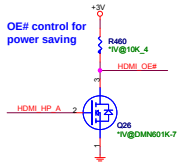
From MXM



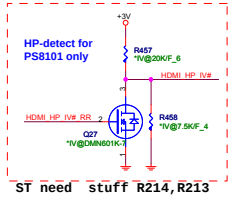
From GMCH (iHDMI)



OE# control for power saving

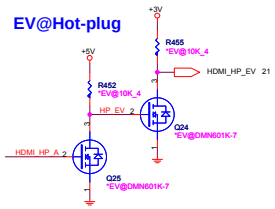


HP-detect for PS8101 only



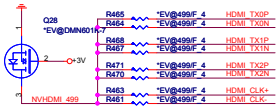
ST need stuff R214,R213

EV@Hot-plug



FOR NV HDMI

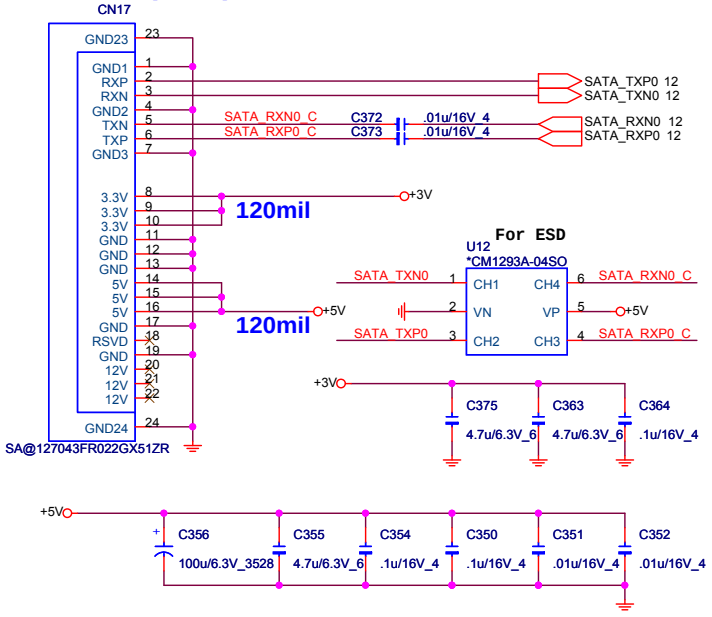
NV suggestion near HDMI connector



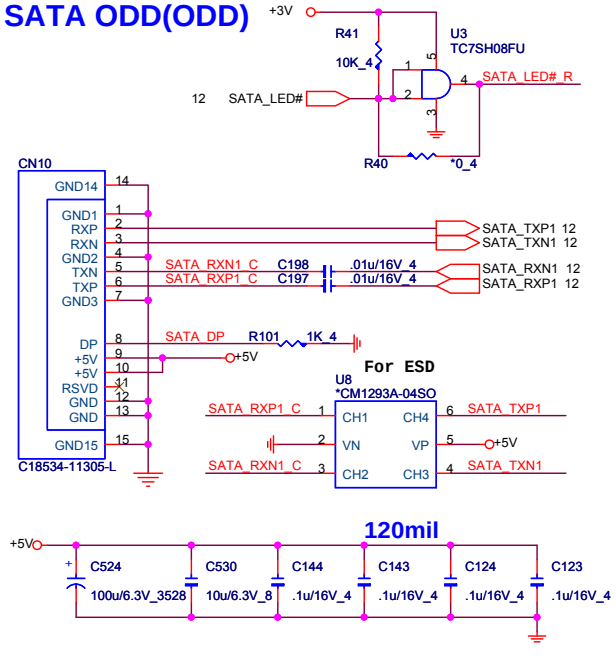
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	LVDS/CRT/CCD/HDMI/MIC	1A
Date: Monday, April 13, 2009	Sheet 24 of 42	

SATA HDD(HDD)

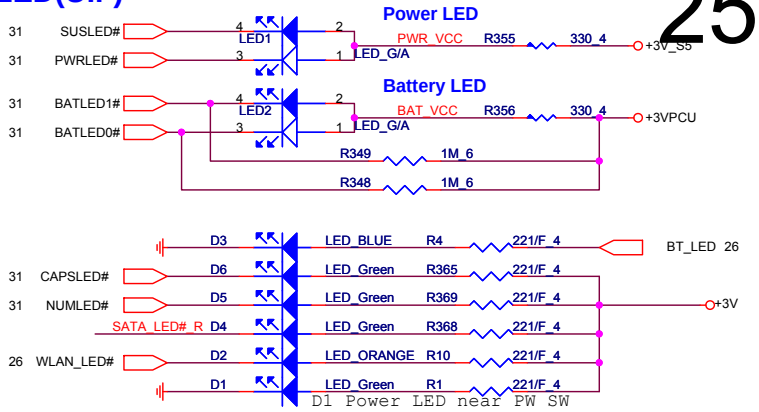


SATA ODD(ODD)

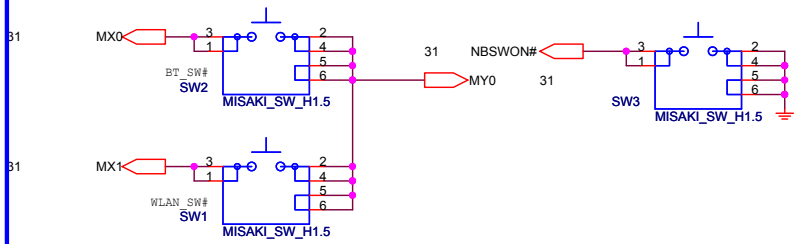


LED(UIF)

Power/Suspend: Green/Amber

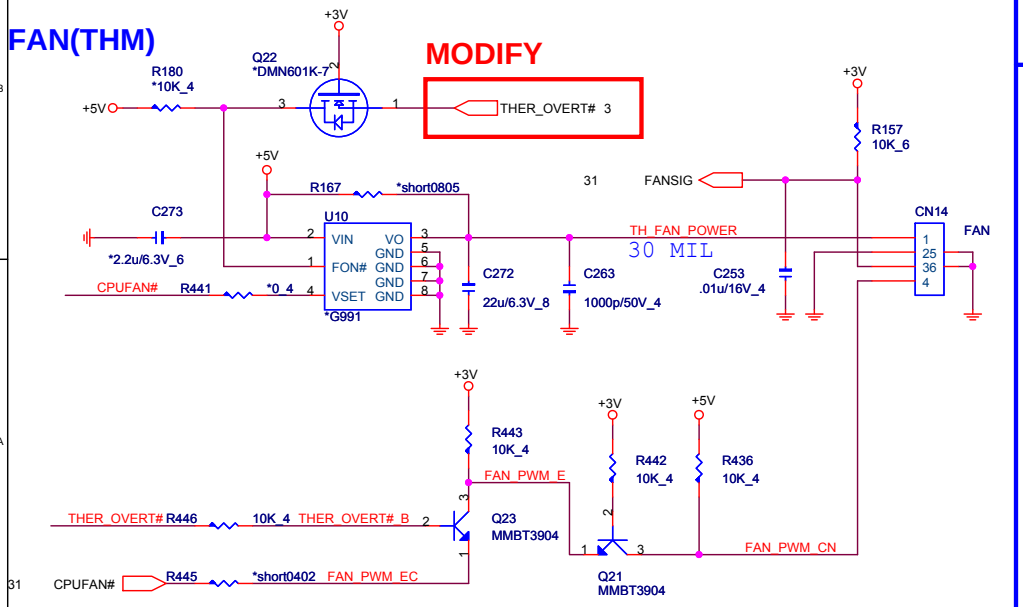


Power Button (UIF)



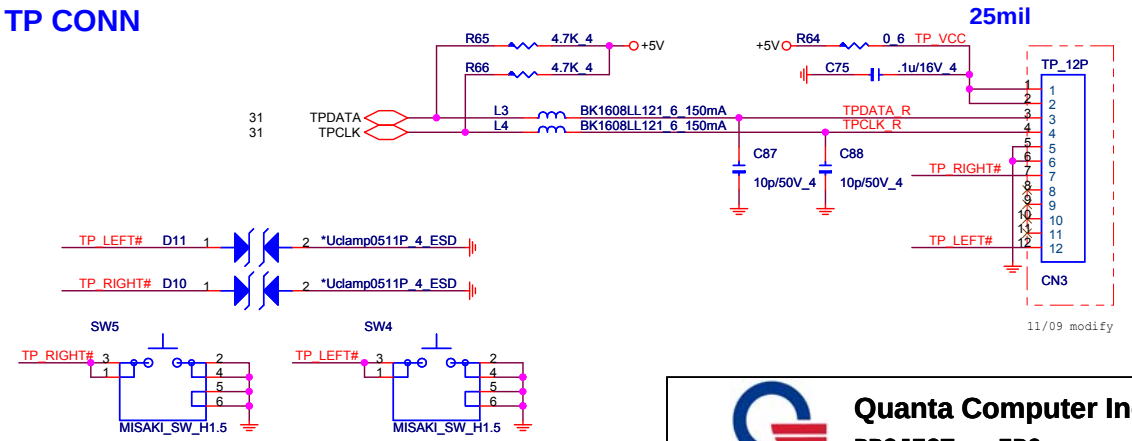
FAN(THM)

MODIFY



TP CONN

25mil



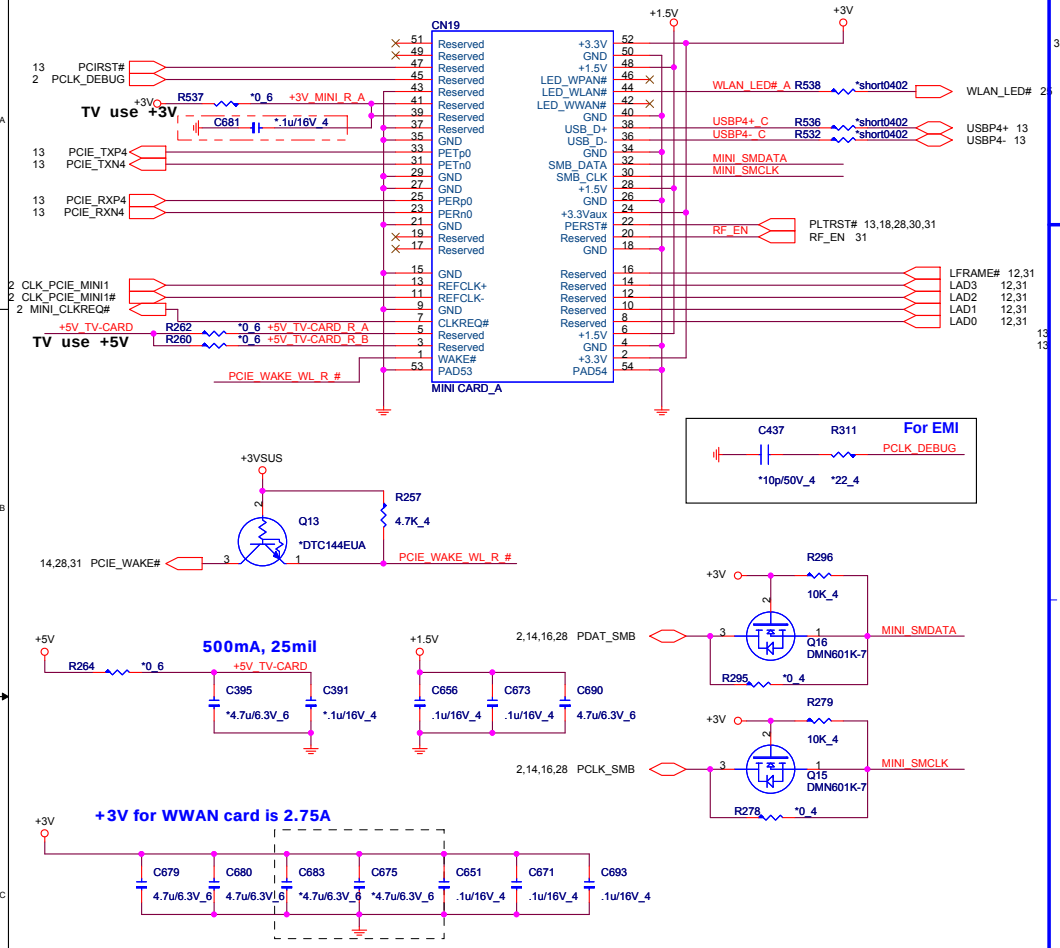
Quanta Computer Inc.

PROJECT : ZR6

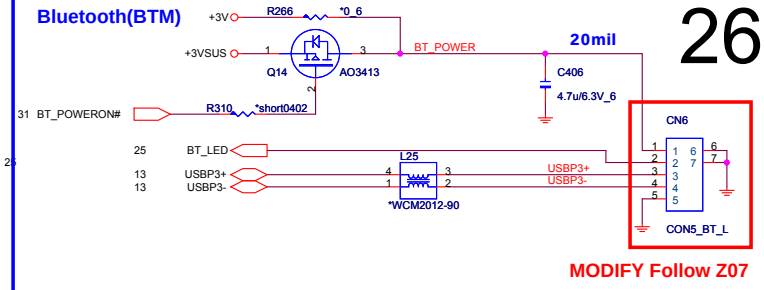
Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A

Date: Monday, April 13, 2009 Sheet 25 of 42

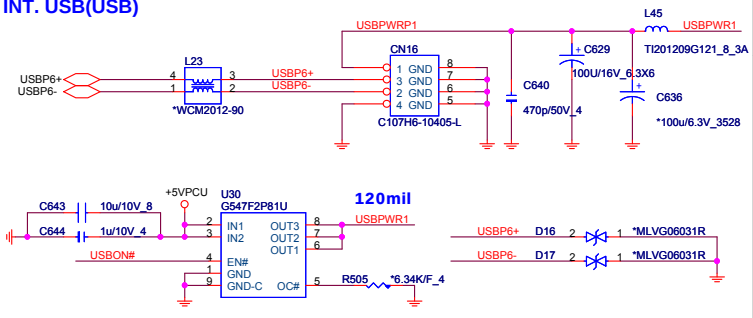
MINI-CARD(MPC)



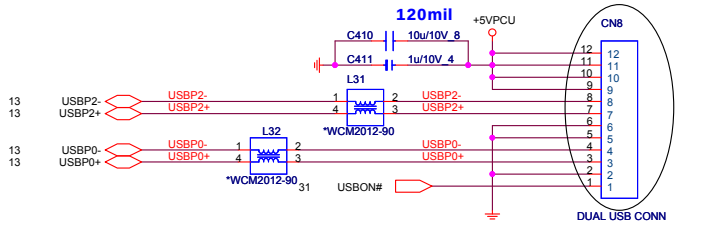
Bluetooth(BTM)



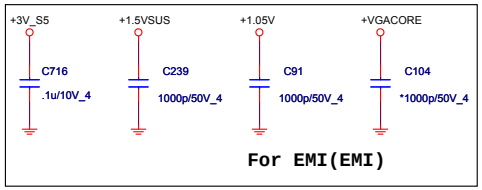
INT. USB(USB)

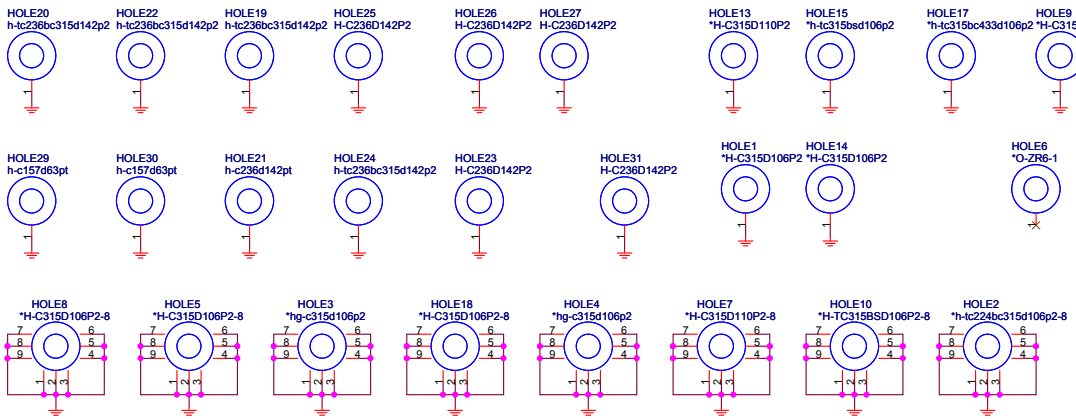


EXT. USB(USB)



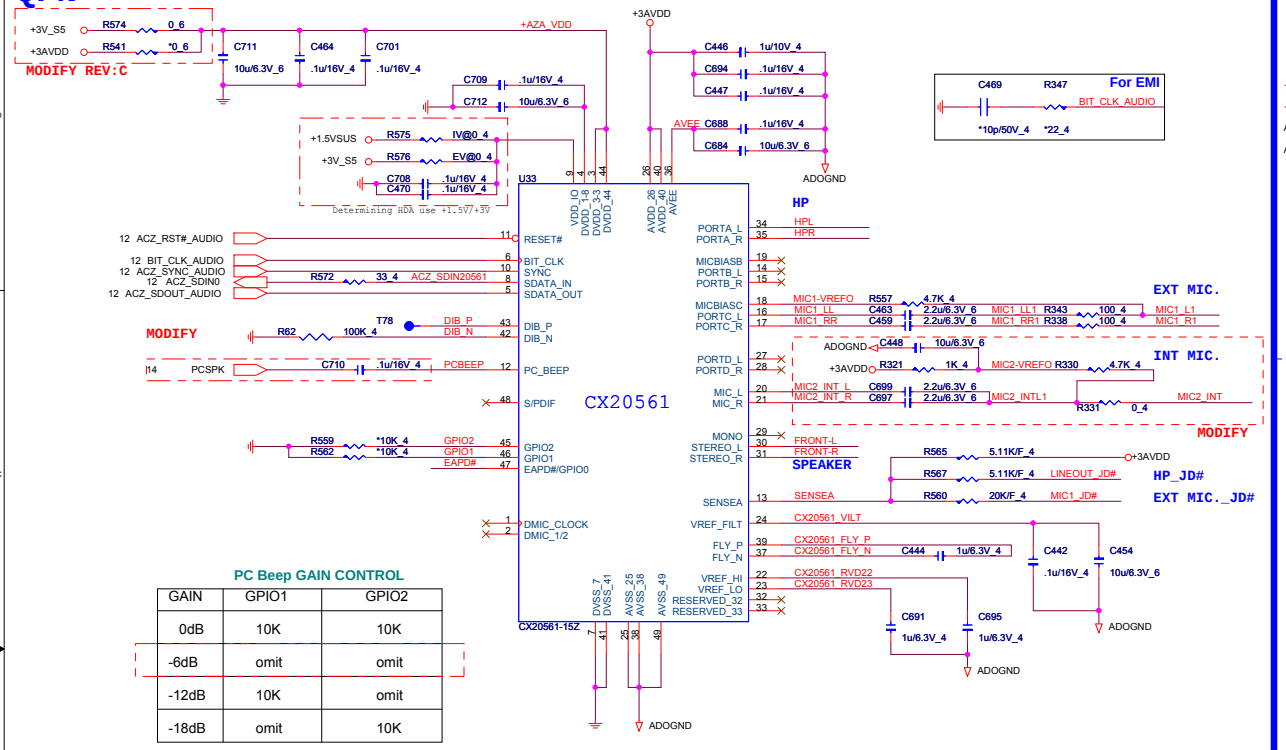
(OTH)





Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: MINI/USB/BT/HOLE	Rev: 1A
Date: Monday, April 13, 2009	Sheet 26 of 42	

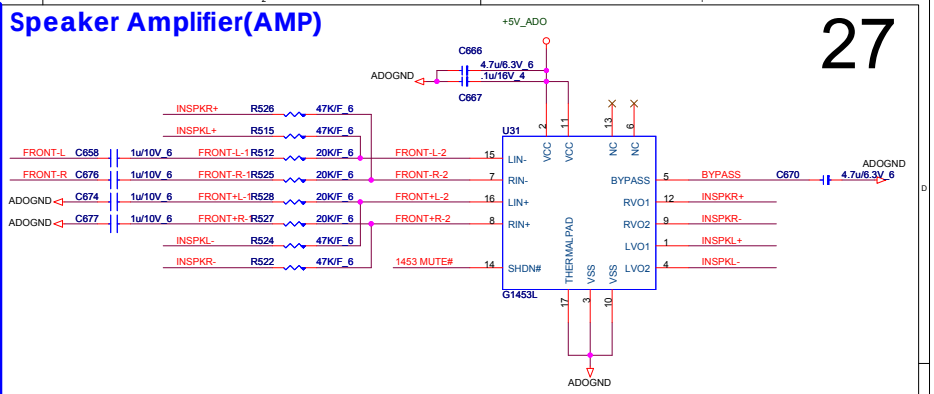
Codec CX20561-15Z (ADO)
QFN



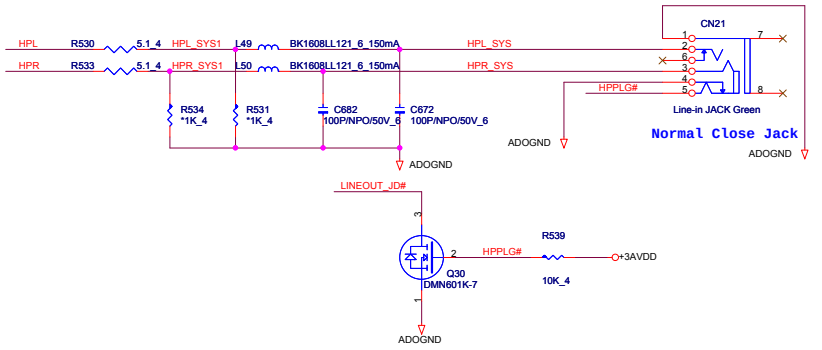
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

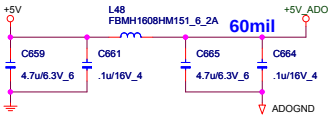
Speaker Amplifier(AMP)



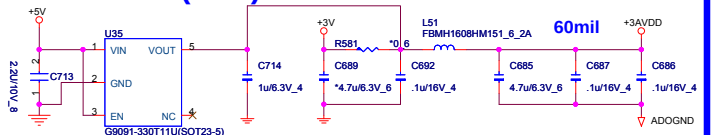
LINE OUT(AMP)



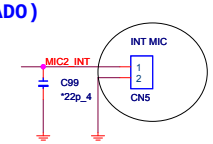
AMP Power(AMP)



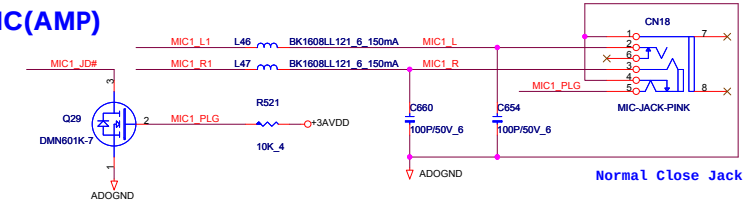
CODER Power(ADO)



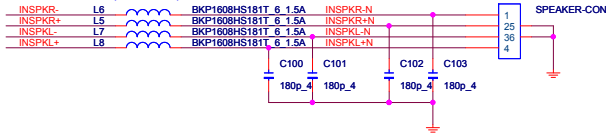
INT MIC.(ADO)



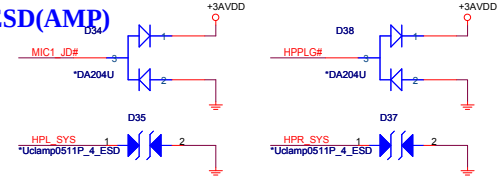
MIC(AMP)



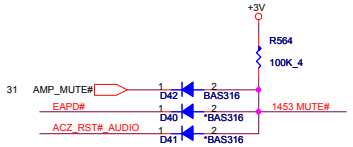
SPEAKER(AMP)



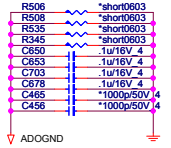
ESD(AMP)



MUTE(AMP)



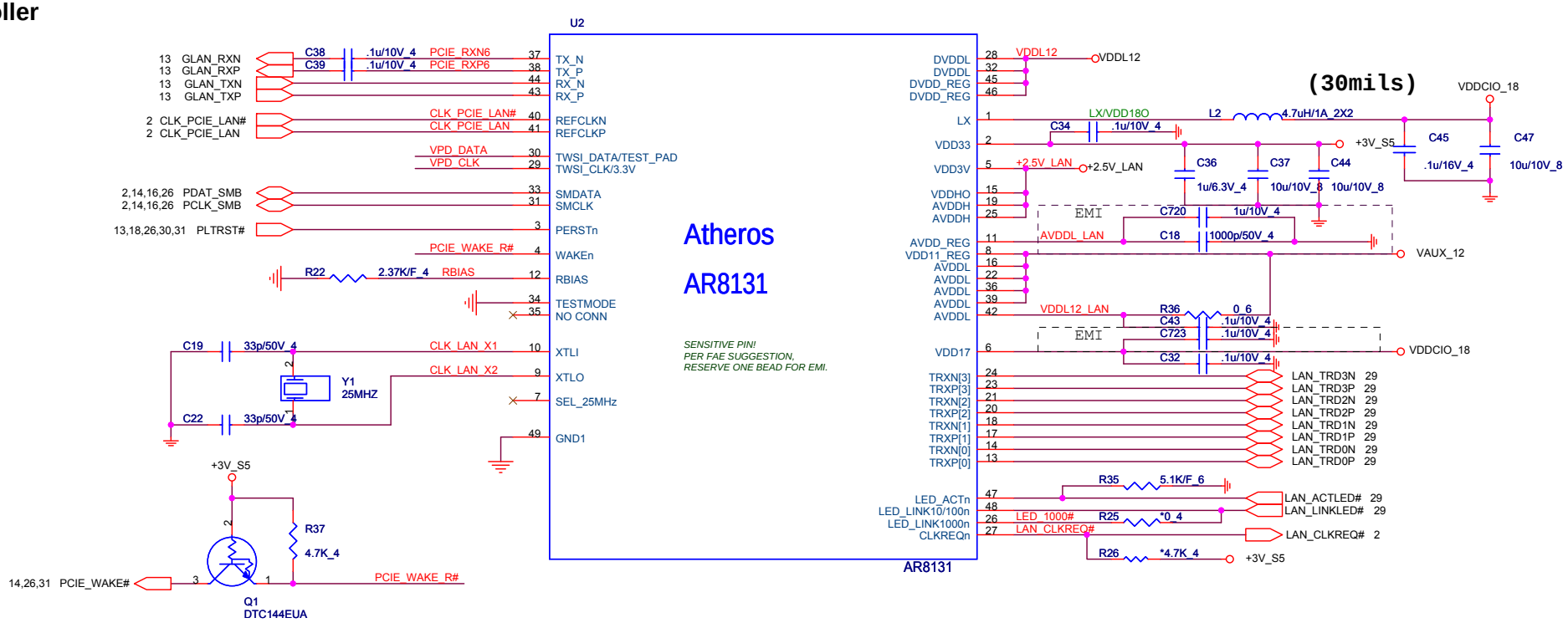
(ADO)



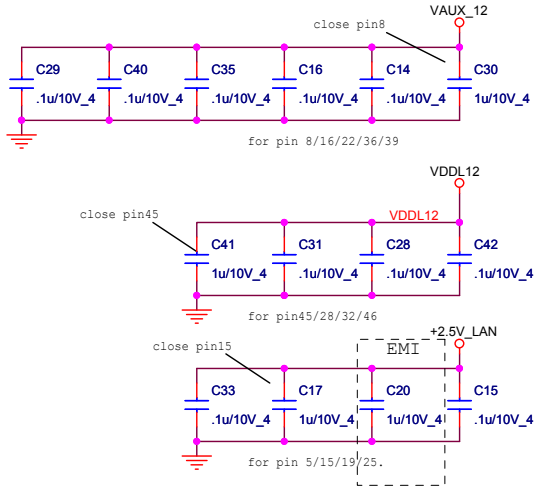
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	CODEC/AMP/MDC	1A
Date: Monday, April 13, 2009	Sheet 27 of 42	

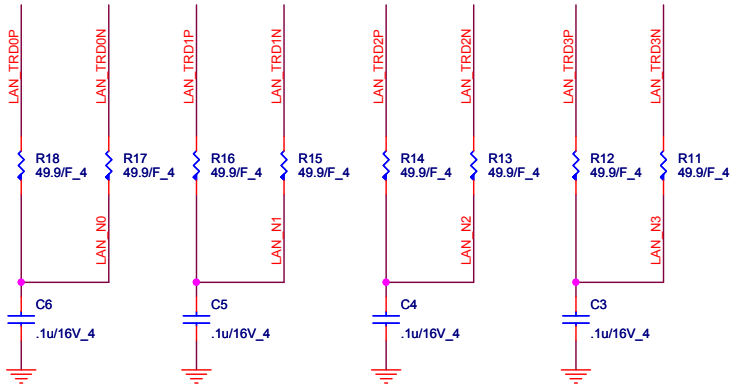
LAN Controller



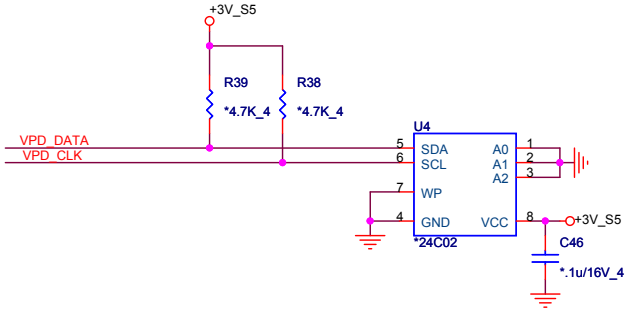
Decoupling CAP



PLACE NEAR IC SIDE



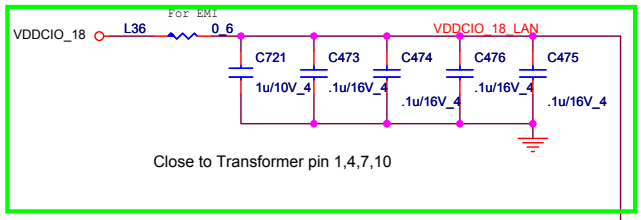
EEPROM



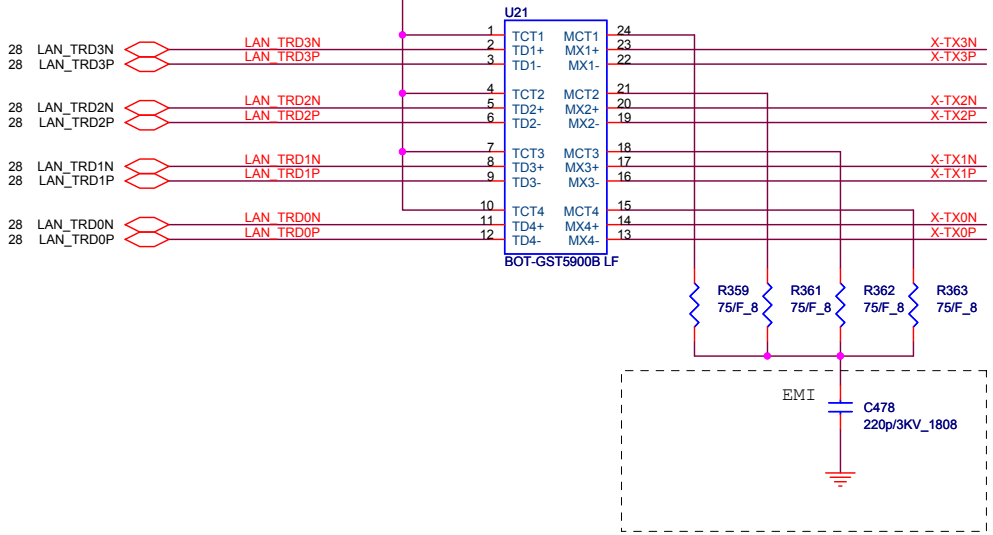
Quanta Computer Inc.

PROJECT : ZR6

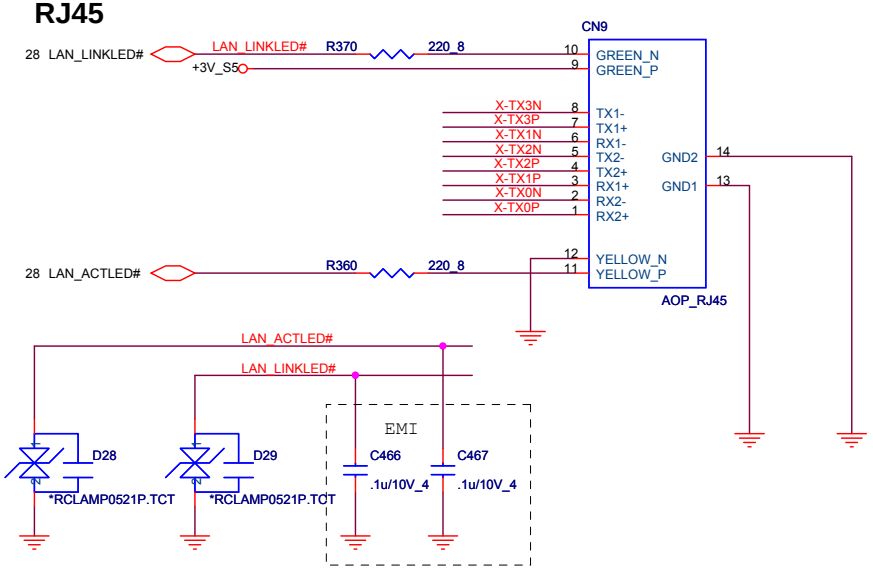
Size	Document Number	Rev
	AR8131 GLAN	1A
Date: Monday, April 13, 2009	Sheet 28 of 42	



TRANSFORMER

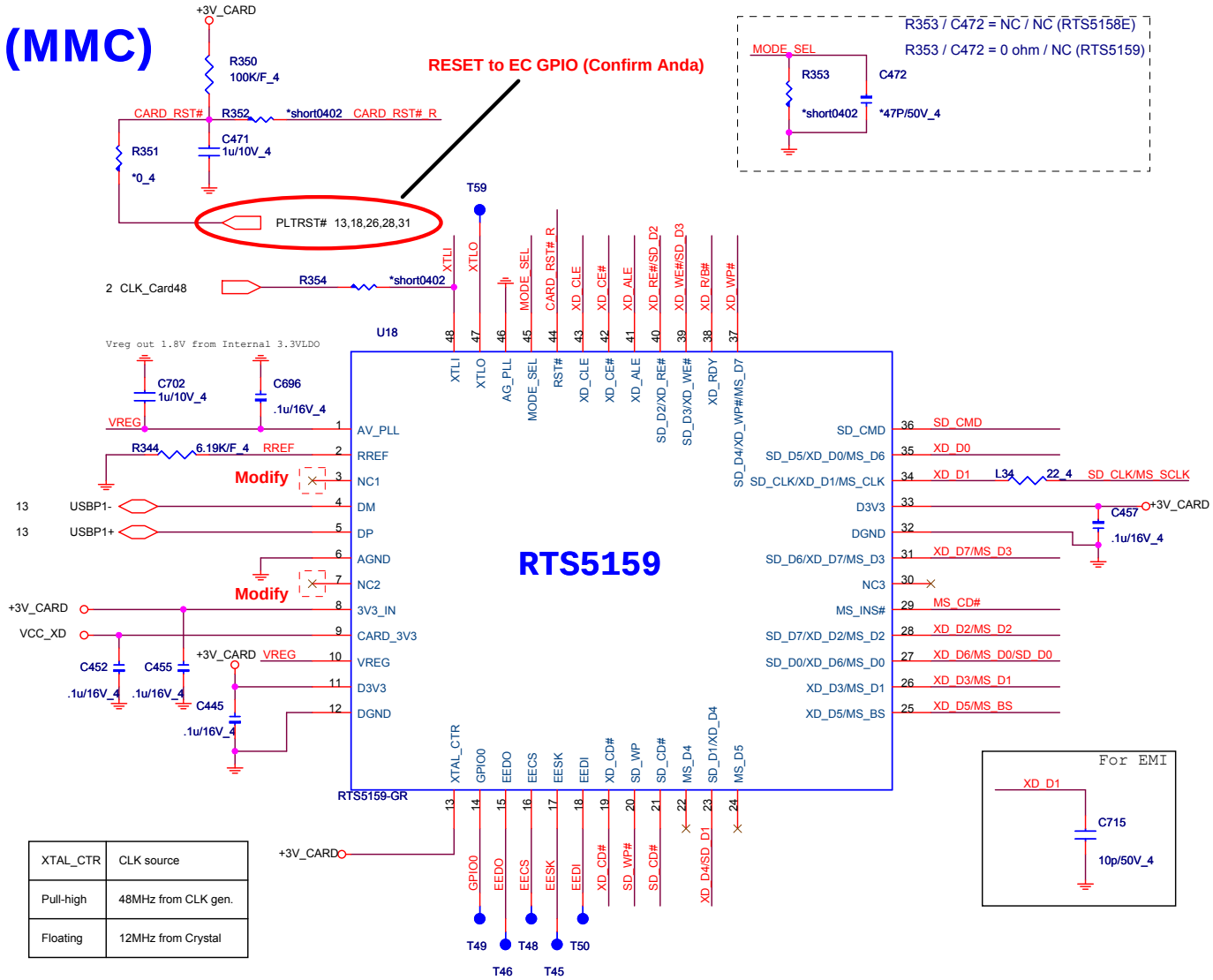


RJ45



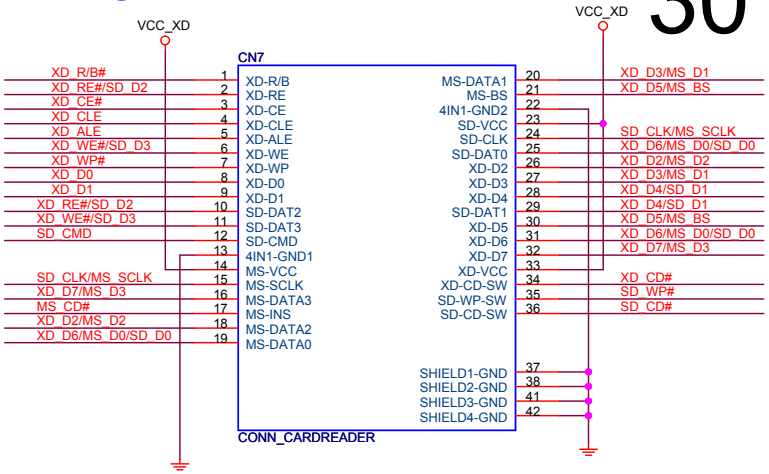
Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: LAN Transformer and RJ45/BT	Rev 1A
Date: Monday, April 13, 2009	Sheet 29 of 42	

(MMC)

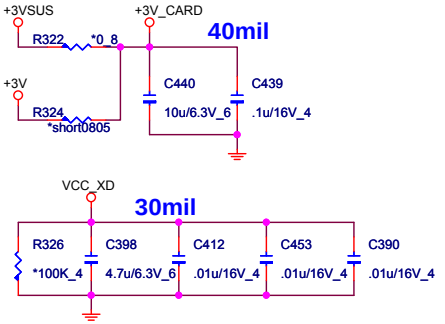


XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

4 IN 1 CARD READER



CARDREADER POWER



Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	CARD READER RTS5159	1A

Date: Monday, April 13, 2009 Sheet 30 of 42

EC(KBC)

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 R303 10K_4
BADDR1 uR_SOUT_CR R302 *10K_4
SHBM SHBM R269 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

+3VPCU
MBCLK R513 4.7K_4
MBDATA R509 4.7K_4
MXM_SMCLK R304 4.7K_4
MXM_SMDATA R305 4.7K_4
+3V
2ND_MBCLK R259 4.7K_4
2ND_MBDATA R261 4.7K_4
CRT_SENSE# R523 4.7K_4

ACER ID

MXM_SMCLK
MXM_SMDATA
U16 24C02 (SCL, SDA, A0, A1, A2, WP, VCC, GND)
+3VPCU +3V_S5
R316 *0_4
R323 *short0402
C449 *.1u/16V_4_X7R

SPI FLASH

2'nd Source AKE38ZA0Q00

SPI_SDI_uR R325 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
R333 10K_4 SPI_CS0# uR
U17 W25X16AVSSIG (SO, SI, SCK, CE, VDD, HOLD, WP, VSS)
C443 .1u/16V_4_X7R

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

+3V
R273 10K_4
1V8_ON D19 EV@BAS316
HWPG_1.5V D24 BAS316
HWPG_1.05V D20 BAS316
HWPG_1.8V D25 BAS316
SYS_HWPG D21 BAS316
DELAY_VR_PWRGOOD D22 *BAS316
HWPG_1.1V D23 EV@BAS316
R263 *short0402
MPWROK 6,14

1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

POWER-ON PAD(UIF)

G1 *SHORT_PAD
NBSWON#

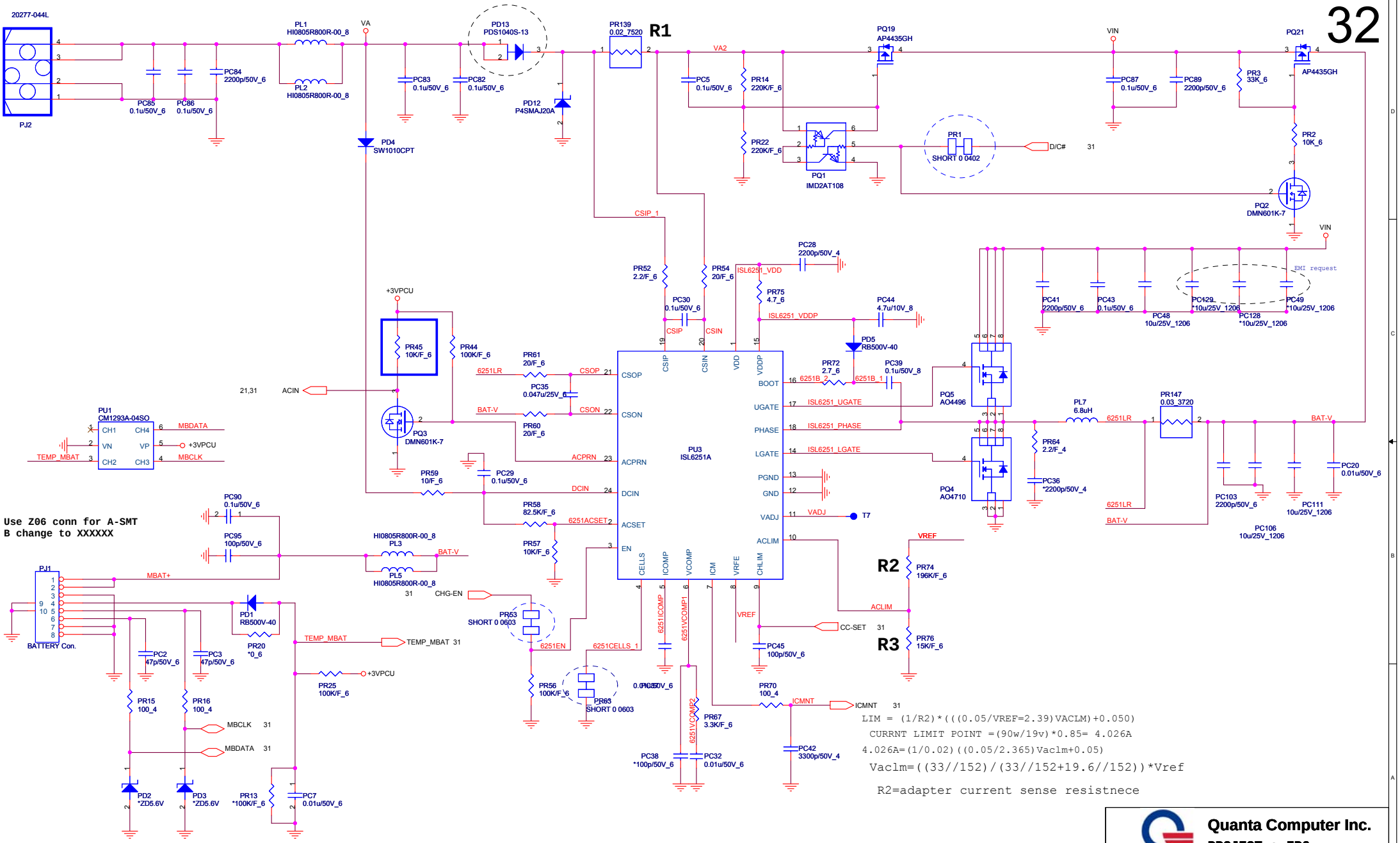
Thermal Sensor(THM)

+3V
R300 47K/F_4
R301 100K/F_4 NTC
TPD_TRIP

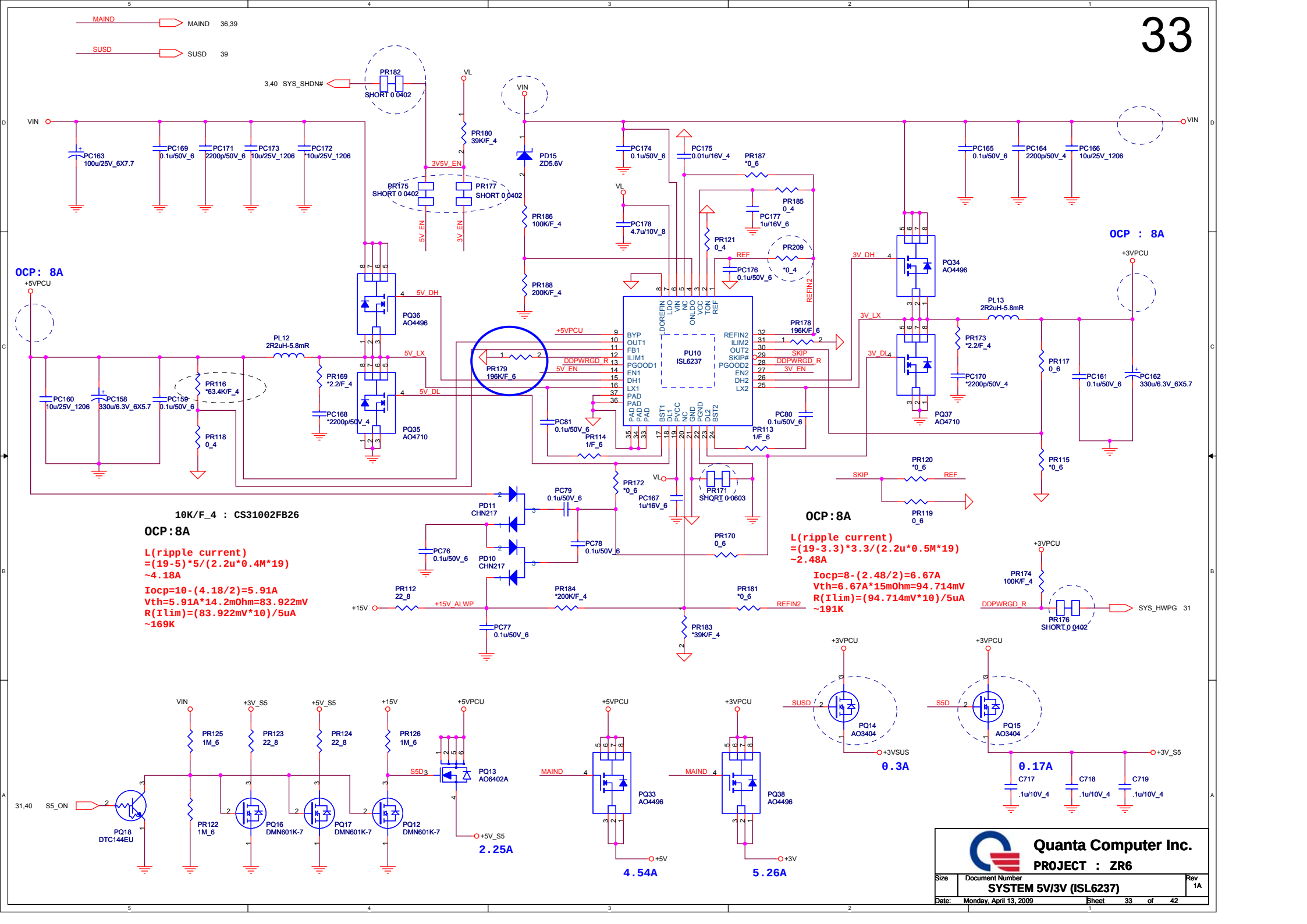
INTERNAL KEYBOARD STRIP SET

+3VPCU
MY0 R247 10K_4

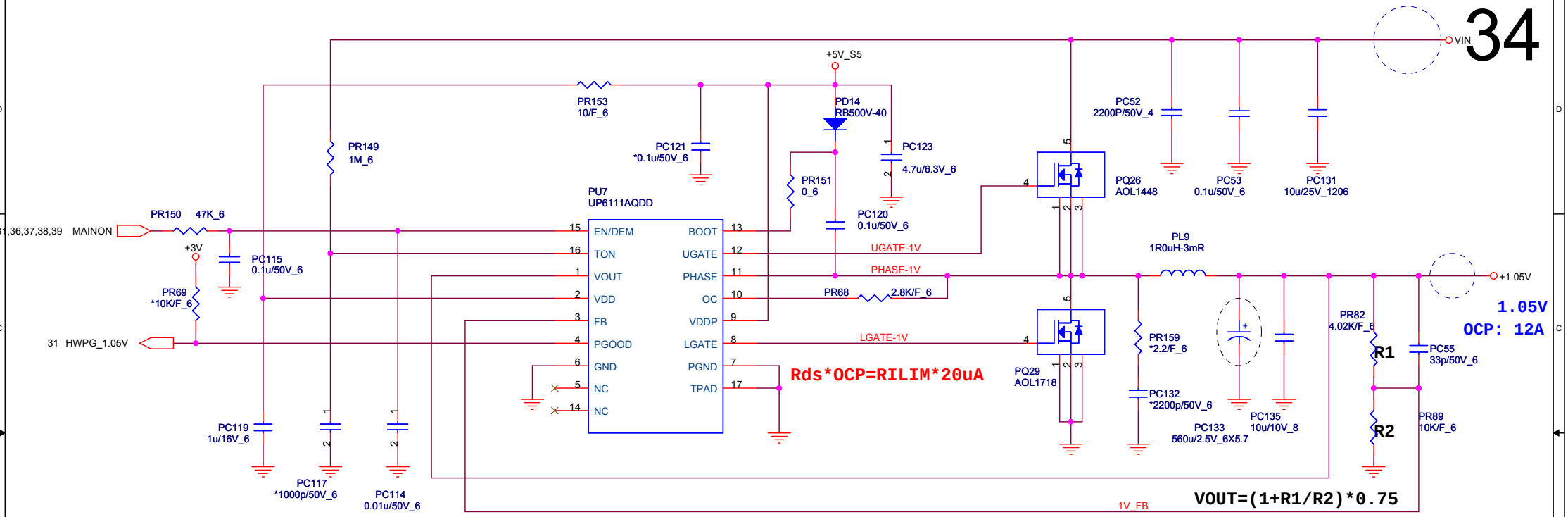
Quanta Computer Inc.
PROJECT : ZR6
Size | Document Number: WPCE775C_0DG & FLASH | Rev 1A
Date: Monday, April 13, 2009 | Sheet 31 of 42



Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: Charger (ISL6251A)	Rev: 1A
Date: Monday, April 13, 2009	Sheet 32 of 42	



Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	SYSTEM 5V/3V (ISL6237)		1A
Date: Monday, April 13, 2009		Sheet 33 of 42	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

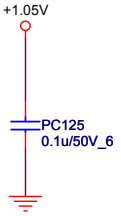
AOL1412 Rdson=4.6mOhm

OCP=16-0.8A

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA

RILIM=2.76K--- 2.8K

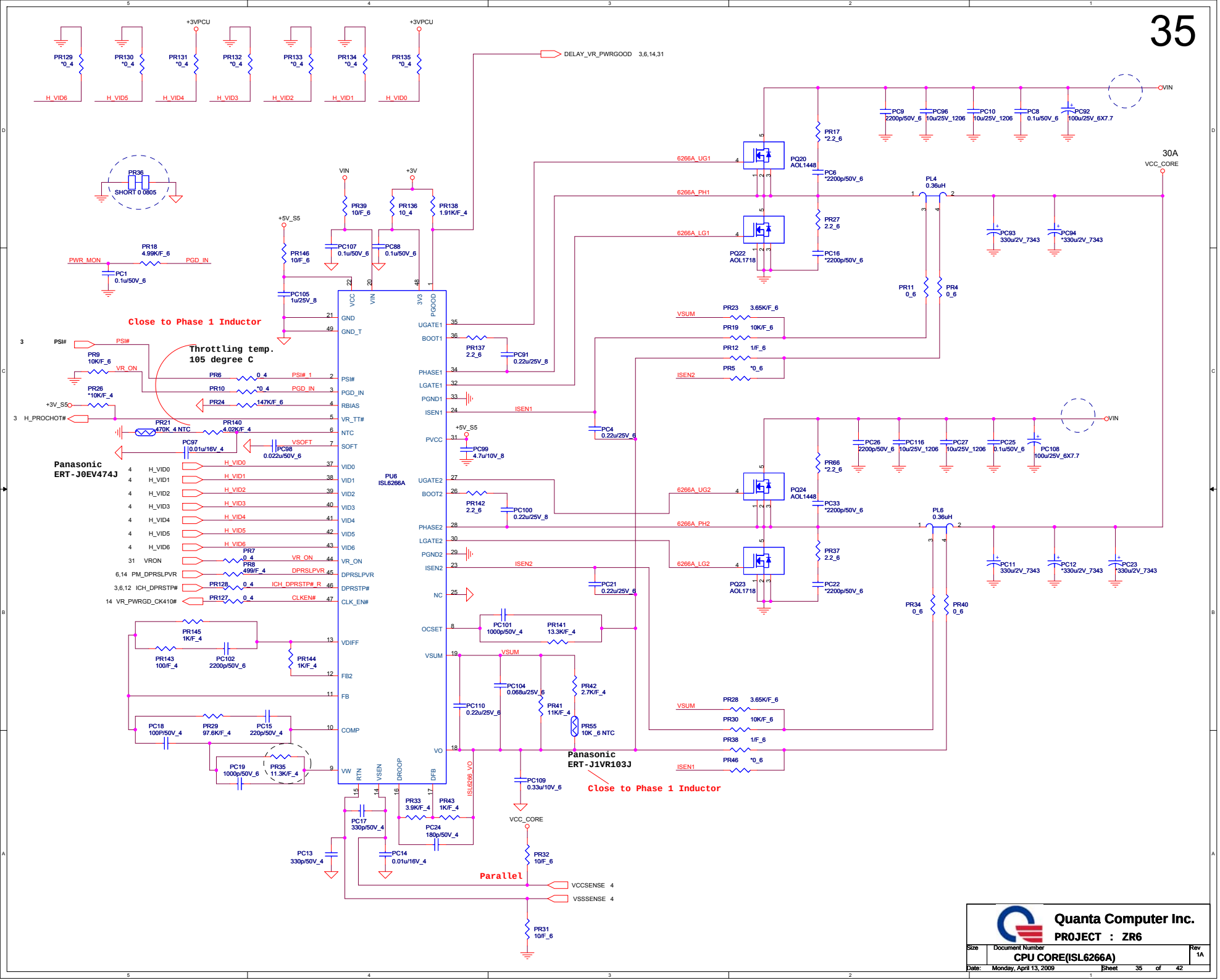


Quanta Computer Inc.

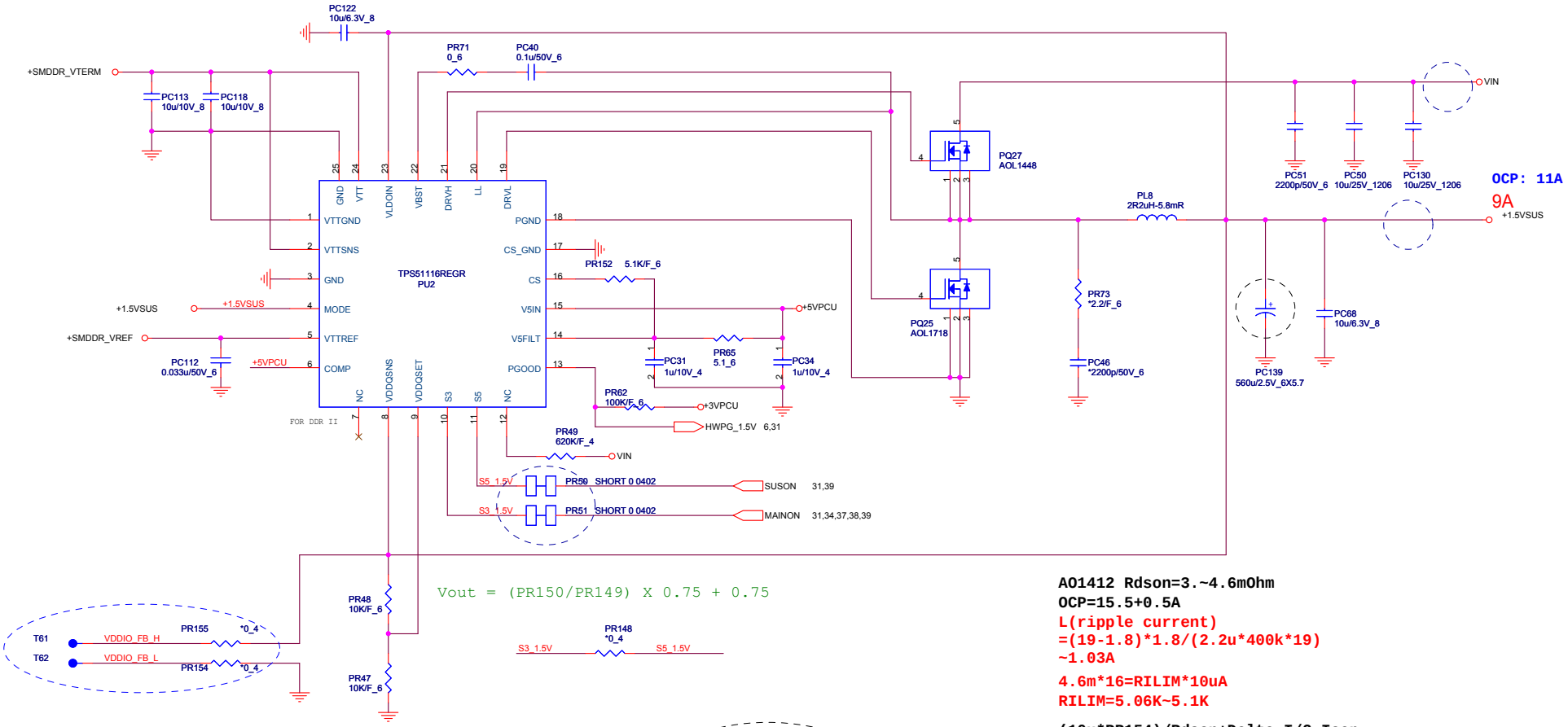
PROJECT : ZR6

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A

Date: Monday, April 13, 2009 Sheet 34 of 42



Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	CPU CORE(ISL6266A)		1A
Date: Monday, April 13, 2009		Sheet 35 of 42	



AO1412 Rdson=3.~4.6mOhm
OCP=15.5+0.5A
L(ripple current)
=(19-1.8)*1.8/(2.2u*400k*19)
~1.03A

4.6m*16=RILIM*10uA
RILIM=5.06K~5.1K

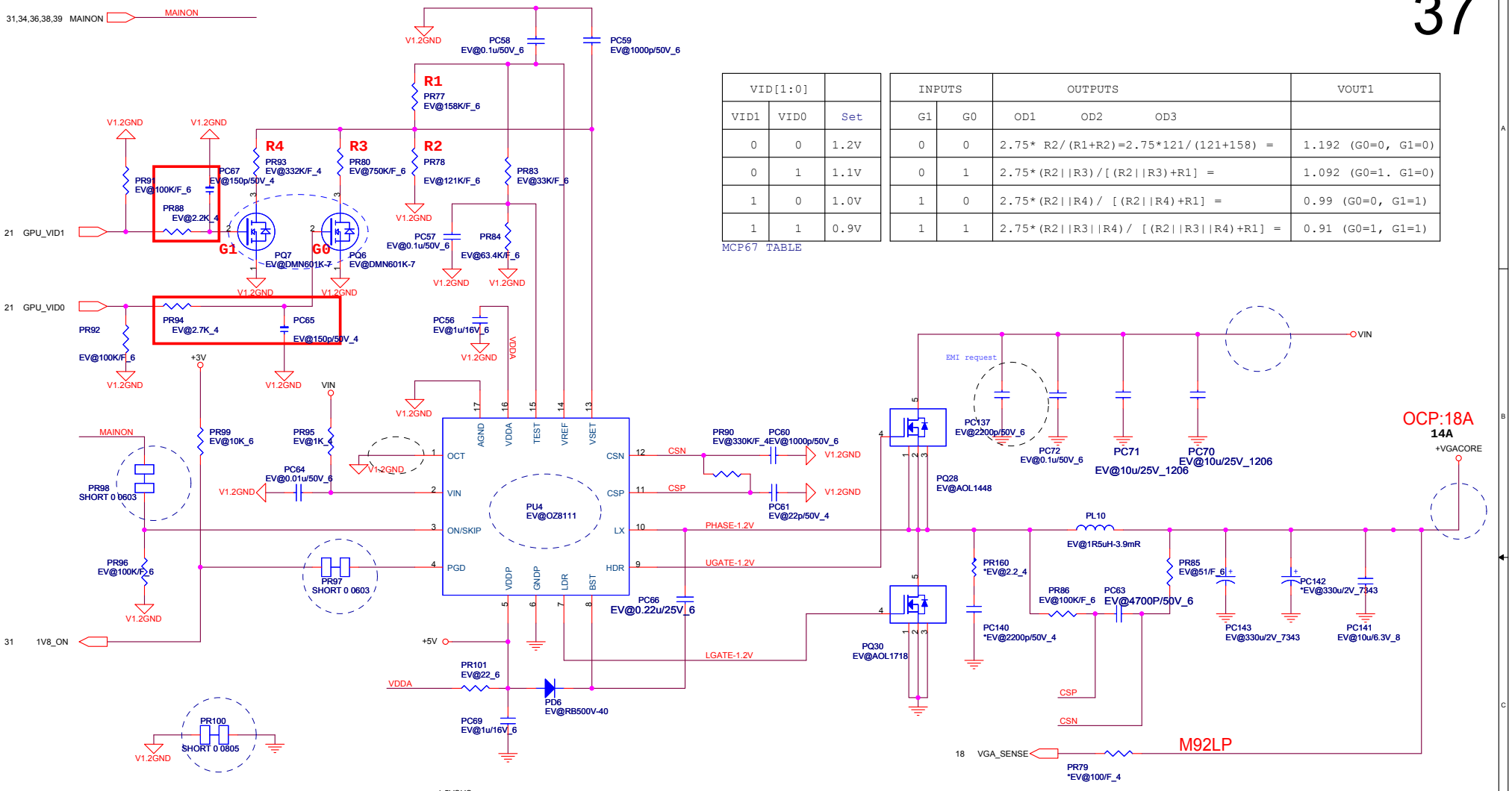
(10u*PR154)/Rdson+Delta_I/2=Iocp

Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: DDR 1.5V(TPS51116)	Rev: 1A
Date: Monday, April 13, 2009	Sheet 36 of 42	

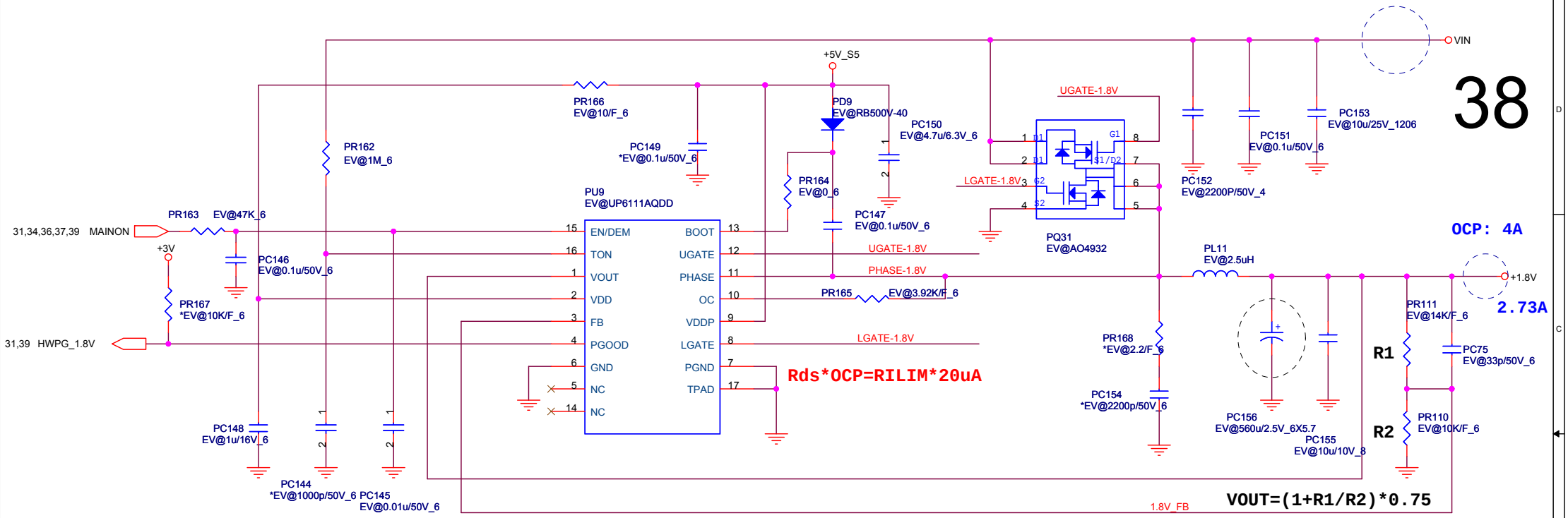
VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =	1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =	1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =	0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =	0.91 (G0=1, G1=1)



Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	VGA M92LP (OZ8118)		1A
Date: Monday, April 13, 2009		Sheet 37 of 42	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

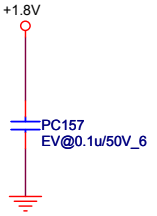
AO4932 Rds=15.6~19.6mOhm

OCP=16-0.8A

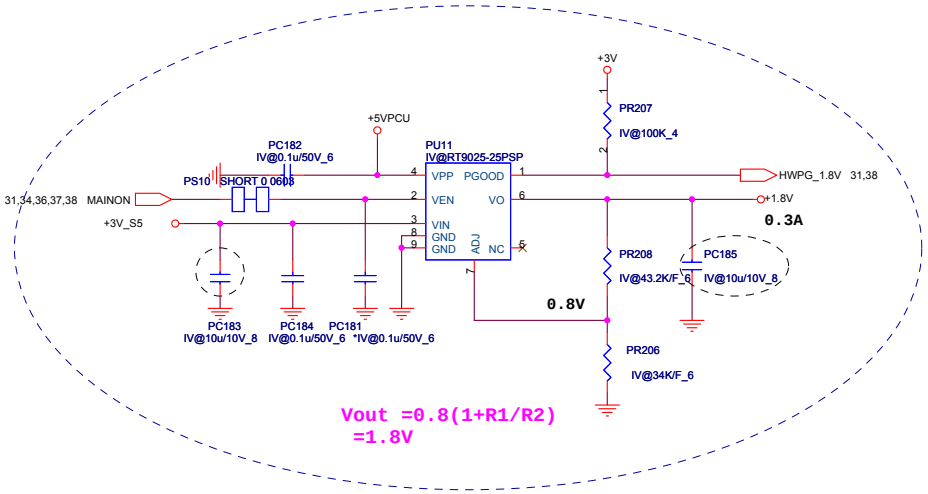
L(ripple current)
=(19-1.8)*1.8/(2.5u*272k*19)
~2.14A

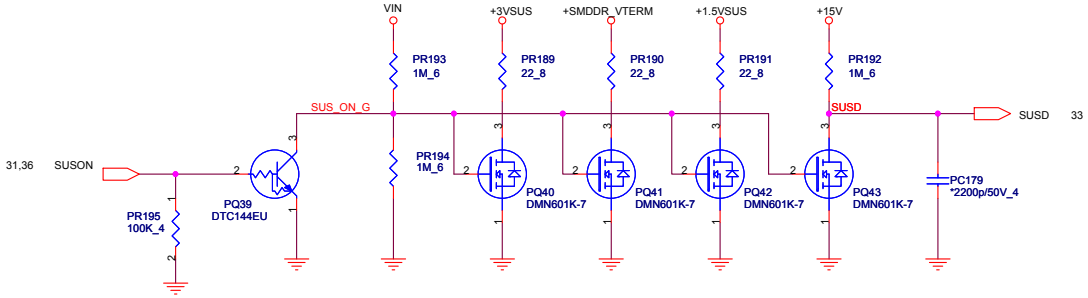
19.6m*4=RILIM*20uA

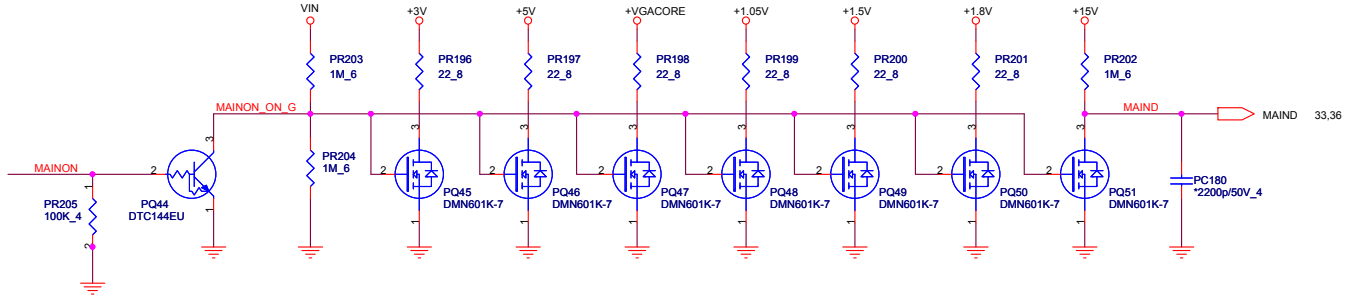
RILIM=3.92K



Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: VCCP 1.8V(UP6111A)	Rev: 1A
Date: Monday, April 13, 2009	Sheet 38 of 42	





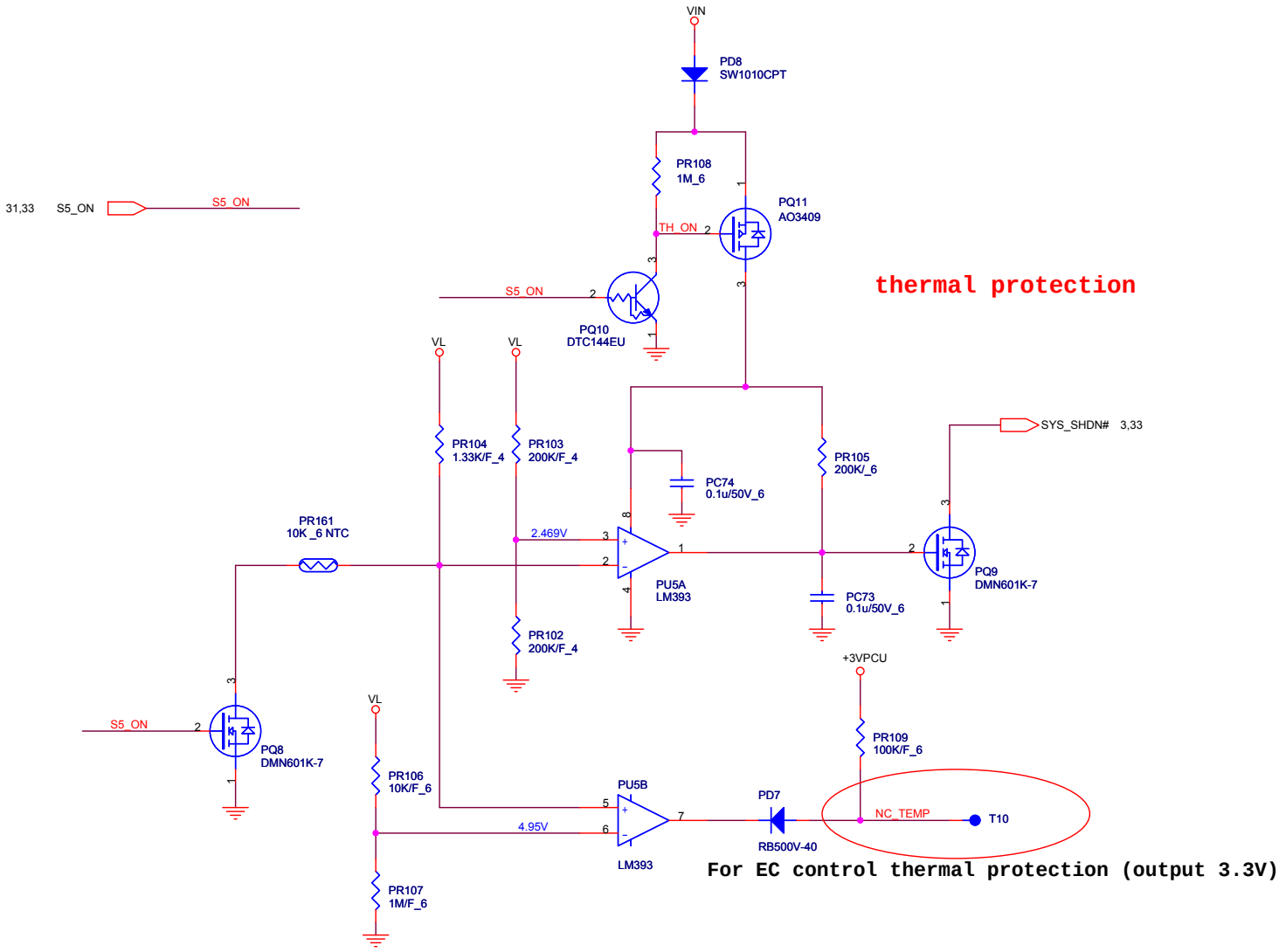


Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	Discharge	1A

Date: Monday, April 13, 2009 Sheet 39 of 42



Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Monday, April 13, 2009	Sheet 40 of 42	

MODEL:	REV	CHANGE LIST
ZR6 MB	A	*First release*
	B	*Page23:Change C209,C522,C567,C533 from CH31003MB14 to CH41002KB93* *Page10:change net name +1.8VSUS_TXLVDS-->+1.5VSUS_TXLVDS,+1.8VSUS_VCC_SM_CK-->+1.5VSUS_VCC_SM_CK* *Page24:change R174 from 100k to 470K,Del R177 to slove Hall sensor issue* *Page25:U12 No stuff and Del R248 to no stuff* *Page12:Change R543,R542,Q31 to no stuff,because ZR6 battery can't charging* *Page21:VGA ID pin R387 stuff 15k,R382 stuff 45.3K,R414 stuff 25K,R381/R415 no stuff* *Page14:MB ID pinR298 Value change to EV@,R308 Valule change to IV@* *Page26:change L25 layout and del RN19 and change L23 layout and del RN14* *Page24:change L1 layout and del RN1* *Page24:Change LCD connector(OT2)* *Page33:Mirror the PJ2 connector* *Page26:change CN19 footprint to mipci800055fb052g100pl-52p-ldv as ZG5 and Del debug card 0 ohm R518,R517,R514,R511,R510,R315,R310* *Page6:Change DD3 power OK circuit as ZK6* *Page26:Del R520,R529 and change R538,R536,R532 footprint to short pad* *Page24:U11 add pin 49 to thermal pad gnd* *Page25:Change CN3 footprint to af712l-a2g1t-12p-l-zr6* *Page32:Change CN2 footprint to 88502-260N-26P-L-ZR6* *Page29:Change U21 footprint to trf-10-1-24p-zr6* *Page27:Change U33 footprint to tqfn48-7x7-5-49p-zr6* *Page26:Change CN8 footprint to bl123-10r-10p-l-zr6* *Page25:Change D1、D2、D3 footprint to led-ht-110nb5-3p-zr6* *Page27:Change CN18 Part Number to DFTJ06FR212 and Change CN21 Part Number to DFTJ06FR211* *Page33:Change PJ1 Part Number to DFHD08MR064 for ZR6* *Page17:Change C502 to no stuff for cost down* *Page26:Change CN8 footprint to bl123-10r-10p-l-zr6& Partumber change to DFFC10FR017* *Page2:Del RN15,RN36,RN18,RN22,RN20,RN24,RN23 for cost down &Change R252,R244,R499 to short pad* *Page4:Change C58 to No stuff* *Page29:change R366,R367,R357,R358 to short pad for cost down* *Page27:change R506,R508,R535,R345 to short pad for cost down* *Page24:Del R346,R7 for cost down* *Page25:Del R218,R407 for cost down* *Page26:change C683,C675 to no stuff* *Page31:Add C715 for EMI* *Page31:Del C466,C467,L35 for cost down* *Page24:Add CN1 Pin33,Pin34 to GND ,Add R248,R218 for HDMI and Add L52,L53,L54,L55 for EMI* *Page10:change L38 to R037* *Page2:Add R511 for Mini_CLKREQ# pull up* *Page40:change +3VSUS to +3V_S5,HWPG_1.5V to HWPG_1.8V* *Page24:1.Del R248,R218,2.L19,L21 change to R218,R234,3.change D14,D15,R196,R197,R203,R200 vaule to stuff* *Page12:Change C450,C451 to 18P* *Page28:Change C19,C22 to 33P* *Page21:Add MXM ACIN circuit,R177R182,Q33,Q32,R183* *Page27:change R574 to no stuff and R541 to stuff* *Page24:Add D44 and Del R410* *Page28:change R39,R38,U4,C46 to no stuff* *Page18-23:change T65,T74,T11,T69,T68,T64,T67,T70,T73,T66,T72,T71 footprint to T3050* *Page26:Change C629 to 100uf and C636 to no stuff* *Page6:change R175 and R181 to 47K for HDMI vender request* *Page24:Change R197,R200 to EV@*

MODEL / PAGE	ZR6 MB FROM	TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70	Project :ZR6 MB	Document No.:
Approved by : Johnny O	Drawing by :Andy Chen	DATE: 2009/03/04

Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	Thermal Protection	1A

Date: Monday, April 13, 2009 Sheet 41 of 42

MODEL:	REV	CHANGE LIST
ZR6 MB	B	Page6:change R175 and R181 to 4.7K for HDMI vender request
	C	Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS Page3:Del Q5,Q6,R62,R63 Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH Page21:Del Q10,Q9,R96,R86 Page27:R574 stuff and R541 no stuff Page31:R300,R301 stuff thermal sensor Page37:change PC65,PC67 to 150pF Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip) Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone Page27:change CN8 (usb) 12 pin board to board Page26:Change CN5 footprint to cwy027-b0g1z-2p-l,CN16(USB)footprint change to usb-c107h6-10405-l-4p-r-v-nb4 Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4 Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4 Page32:Del R510,change Hole15 footprint from h-tc315bc433d106p2 to h-tc315bsd106p2 Page04:change C493 to no stuff Page27:Del T77 and Add R62 Page26:change Hole21 footprint to h-c236d142pt-8 Page24:Change D1、D2、D3 footprint to led-ht-110nb5-3p Page24:Change R218,R234 to shortpad Page26:Change R310 to shortpad Page10:Change R91,R307,R418,R466,R469 to shortpad Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND Page26:Add C716 for EMI Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1% Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number Page14:Change R282 to no stuff Page28:Change R26 to no stuff Page26:Change Hole29 part number to MBZR6005010 Page29:Del net name LAN_LNK_LED_PWR
	D	Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff Page24:change HDMI item to no stuff(remove this function) Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio Page26:Change Hole 16 footprint as hole1
	E	Page37:change PR97,PR98 to short-pad ,change PU4 OZ8116 change to OZ8111 for cost issue ,Del PC62 Page27:C670 change value from 1U to 4.7U (CH5471M9907) Page29:change c478 from 1000p to 220p.(CH122GK1I10) Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93),ADD C720 1u (CH5102K9B06) Page25:change DHP00DA1G03->DHPTME53201 Page24:add C722 (CH6101M9905) to solve ISN issue Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM. Page34:change PC133 from CC7560JMZ15 to CC7560JMZ02 for cost down Page36:change PC139 from CC7560JMZ15 to CC7560JMZ02 for cost down Page38:change PC156 from CC7560JMZ15 to CC7560JMZ02 for cost down Page33:change PC158,PC162 from CC73301MZB2 to CC73301MZ04 for cost down Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down

MODEL / PAGE	ZR6 MB FROM	TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70

Project :ZR6 MB

Document No.:

Approved by : Johnny_O

Drawing by :Andy Chen

DATE: 2009/03/04

Quanta Computer Inc.

PROJECT : ZR6

Size | Document Number: Thermal Protection | Rev: 1A

Date: Monday, April 13, 2009 Sheet 42 of 42