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ILI9327

a-Si TFT LCD Single Chip Driver
240RGBx432 Resolution and 262K color

Preliminary
Datasheet

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ILI TECHNOLOGY CORP.
8F, No. 38, Taiyuan St., Jhubei City,
Hsinchu County 302, Taiwan, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600585
http://www.ilitek.com

Content

1. Introduction

ILI9327 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx432 dots, comprising a 720-channel source driver, a 432-channel gate driver, 233,280 bytes GRAM for graphic data of 240RGBx432 dots, and power supply circuit.

The ILI9327 supports 18-/16-/9-/8-bit data bus interface (DBI) and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface (DPI) for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9327 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9327 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9327 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

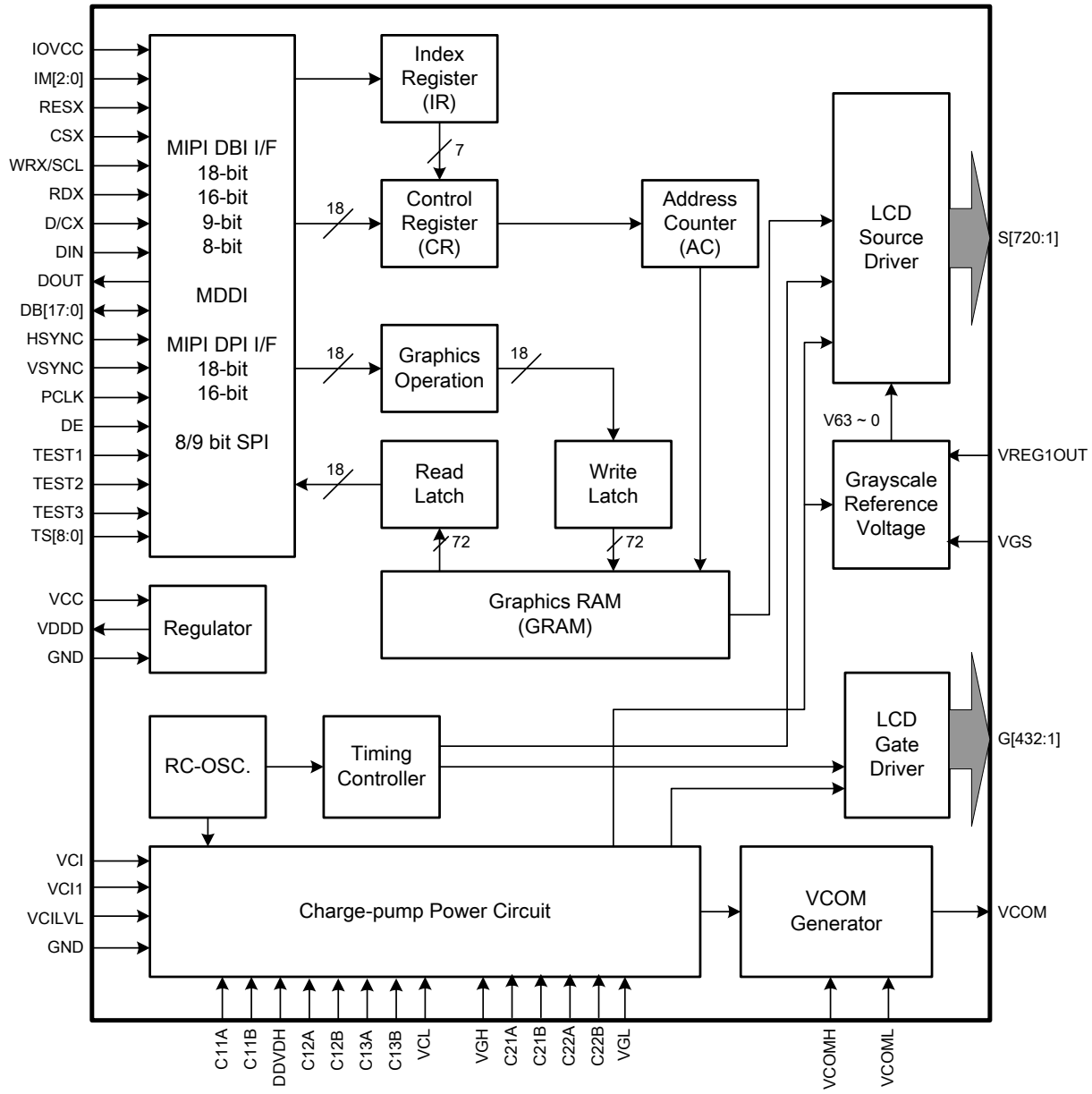
2. Features

- Display resolution: [240xRGB](H) x 432(V)
- Output:
  - 720 source outputs
  - 432 gate outputs
  - Common electrode output
- a-TFT LCD driver with on-chip full display RAM: 233,280 bytes
- MCU Interface
  - MIPI DBI
    - Type B 16-/18- bit, 8-/9- bit
    - Type C 4-line 9bit (Option 1), 8bit (Option 3)
  - MIPI DPI
    - Type B 16-/18- bit
  - MIPI DCS command sets
  - MDDI high speed serial interface
- Display mode:
  - Full color mode: 262K-color
  - Separate RGB gamma
  - Reduced color mode: 8-colors (3-bits MSB bits mode)
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
- MTP:
  - 7-bits for VCOM adjustment
- Low -power consumption architecture

- Low operating power supplies:
  - IOVcc = 1.65V ~ 3.3V (interface I/O)
  - Vci = 2.5V ~ 3.3V (analog)

- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH - GND = 4.5V ~ 6.0V
    - VCL – GND = -1.0V ~ -3.0V
    - VCI – VCL ≦ 6.0V
  - Gate driver output voltage
    - VGH - GND = 10V ~ 18V
    - VGL – GND = -5V ~ -12.5V
    - VGH – VGL ≦ 30V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (DDVDH-0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH-VCOML ≦ 6.0V
- Operate temperature range: -40℃ to 85℃

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Select the MPU system interface mode
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Type B 18-bit</td><td>DB[17:0]</td><td>262K</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Type B 9-bit</td><td>DB[8:0]</td><td>262K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Type B 16-bit</td><td>DB[15:0]</td><td>65K/262K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Type B 8-bit</td><td>DB[7:0]</td><td>65K/262K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MDDI</td><td>-</td><td>65K/262K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DBI Type C 9-bit</td><td>DIN, DOUT</td><td>8/262K</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>CPU 9-bit</td><td>DB[8:0]/DB[8:1]</td><td>262K</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DBI Type C 8-bit</td><td>DIN, DOUT</td><td>8/262K</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active</td></tr>
<tr><td>CSX</td><td>I</td><td>Chip select input pin (“Low” enable).</td></tr>
<tr><td>D/CX</td><td>I</td><td>Display data / Command selection pin
D/CX=’1’: Display data.
D/CX=’0’: Command data.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>RDX</td><td>I</td><td>Read control pin for the DBI interface.
If not used, please connect this pin to IOVCC.</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>Write control pin for the DBI interface.
When the DBI type C is selected, this pin is used as serial clock pin.
If not used, please connect this pin to IOVCC.</td></tr>
<tr><td>DB[17:9]/S_DB[8:0]
DB[8:0]</td><td>I/O</td><td>These pin are data bus.
If not used, please connect these pins to GND.
In MDDI operation, DB[17:9]/S_DB[8:0] are assigned for the sub-display interface output.</td></tr>
<tr><td>DIN/SDA</td><td>I/O</td><td>Serial data input pin and used for the DBI type C mode.
If not used, please connect this pin to ground.</td></tr>
<tr><td>DOUT</td><td>O</td><td>Serial data output pin and used for the DBI type C mode.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command.
When this pin is not activated, this pin is low. If not used, please open this pin.</td></tr>
<tr><td>PCLK</td><td>I</td><td>Pixel clock signal in DPI interface mode.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>VSYNC (S_CS)</td><td>I</td><td>Vertical sync. signal in DPI interface mode.
If not used, please fix this pin at GND level.
In MDDI operation, VSYNC is assigned for the sub-display interface output (S_CS)</td></tr>
<tr><td>HSYNC (S_RS)</td><td>I</td><td>Horizontal sync. signal in DPI interface mode.
If not used, please fix this pin at GND level.
In MDDI operation, VSYNC is assigned for the sub-display interface output (S_RS)</td></tr>
</table>

Pin Name	I/O	Descriptions
DE **(S_WR)**	I	Data enable signal in DPI interface mode. If not used, please fix this pin at GND level. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_WR)
Power Input Pins		
IOVCC	P	Power supply to interface pins Connect to external power supply (IOVCC= 1.65~3.6V).
VCI	P	Power supply to liquid crystal power supply analog circuit. Connect to external power supply (VCI=2.5~3.6V).
VCC	P	Power supply Connect to external power supply (VCC=2.5~3.6V).
DGND AGND	P	Power ground pin. Make sure GND＝0V.
LCD signals Pins		
S1 ~ S720	O	Source driver output pins.
G1 ~ G432	O	Gate driver output pins.
VDD	O	Internal logic regulator output. Used as internal logic power supply. Connect to stabilizing capacitor.
VCI1	P	Reference voltage for the step-up circuit 1. Set VCI1 level so that DDVDH, VGH and VGL are within the ratings.
DDVDH	P	Power supply for the source driver and VCOM.
VGH	P	Power supply to drive liquid crystal.
VGL	P	Power supply for LCD drive.
VCL	P	Power supply to drive VCOML.
C11A, C11B, C12A, C12B	P	Make sure to connect to capacitor that is used in internal step-up circuit 1.
C13A, C13B, C21A, C21B, C22A, C22B,	P	Make sure to connect to capacitor that is used in internal step-up circuit 2. Connect to capacitors according to the step-up factors in use.
VREG1OUT	P	Outputs voltage level generated from VRH VCILVL. The step-up factor applied to VRH VCILVL is set by VRH bits. Used as source driver grayscale reference voltage VREG1OUT, reference voltage to VCOMH, and Vcom amplitude reference voltage. Connect to stabilizing capacitor when in use. VREG1OUT=4.0～(DDVDH-0.500)[V]
VCOM	P	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle. Registers set the alternating cycle and operate or halt VCOM.
VCOMH	P	VCOM high level. Adjust the voltage by internal electronic volume (VCM)

Pin Name	I/O	Descriptions
VCOML	P	VCOM low level. Adjust the voltage by VDV bits. VCOML=(VCL+0.5)～0[V]
VGS	I	Reference level for grayscale generating circuit.
LED Driver pins		
LEDPWM	O	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High). The amplitude of LEDPWM signal is IOVCC-DGND or VCC-DGND (selected by CLED_VOL bit) If this pin is not used, please open this pin.
LEDON	O	This pin is connected to external LED driver. It's a LED driver control pin which is used for turning ON/OFF of LED backlight. The amplitude of LEDPWM signal is IOVCC-DGND or VCC-DGND (selected by CLED_VOL bit) If this pin is not used, please open this pin.
TEST pins		
TS[8:0]	I	Test pins These pins are internal pulled low. Please leave these pins as open.
TESTO[16:1]	O	Test pins Please leave these pins as open.
TEST1-5	I/O	Test pins Please leave these pins as open.
TEST_EN	I	Test pins (Internal pull low) Please leave these pins as open.
GNDDUM IOVCCDUM	-	The ground voltage level output. Pins to fix the electrical potentials of unused interface and test pins.
DUMMYR1~2	-	Dummy Pins These pins are floating.
DUMMY	-	Dummy Pins These pins are floating.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		720 pins (240x RGB)
2	TFT Gate Driver		432 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G432	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc	1.65 ~ 3.30V
		Vci	2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 18V
		VGL	-5V ~ -12.5V
		VCL	-1.0V ~ -3.0V
		VGH - VGL	Max. 32V
		Vci - VCL	Max. 6.0V
7	Internal Step-up Circuits	DDVDH	Vci1 x2
		VGH	Vci1 x4, x5, x6
		VGL	Vci1 x-3, x-4, x-5
		VCL	Vci1 x-1

5. Pad Arrangement and Coordination

Chip Size: 19030um x 840 um

Chip thickness : 280um (typ.)

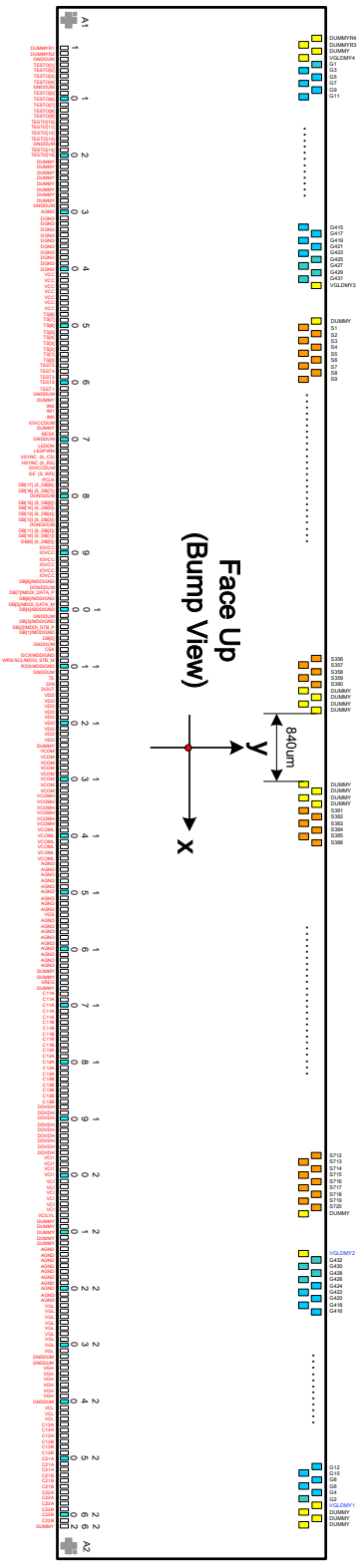
Pad Location: Pad Center.

Au bump height: 12um (typ.)

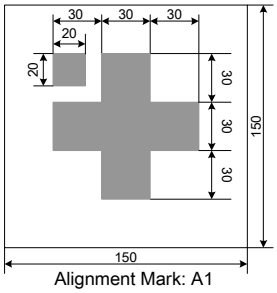
Au Bump Size:

1. 15um x 100um
   Gate: G1 ~ G432
   Source: S1 ~ S720

2. 50um x 90um
   Input Pads
   Pad 1 to 262.

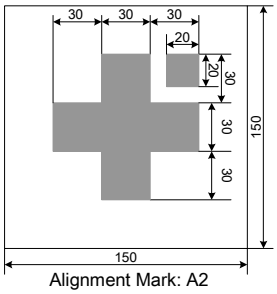


Alignment Marks



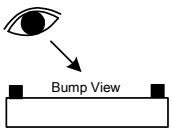
Alignment Mark: A1

Coordination (-9381.0, -251)



Alignment Mark: A2

Coordination (9381.0, -251)



Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	DUMMYR1	-9135	-349	51	TS5	-5635	-349	101	GNDDUM	-2135	-349	151	GND	1365	-349	201	VCI	4865	-349
2	DUMMYR2	-9065	-349	52	TS4	-5565	-349	102	DB3/MDDIGND	-2065	-349	152	GND	1435	-349	202	VCI	4935	-349
3	GNDDUM	-8995	-349	53	TS3	-5495	-349	103	DB2/ MDDI_STB_P	-1995	-349	153	GND	1505	-349	203	VCI	5005	-349
4	TESTO1	-8925	-349	54	TS2	-5425	-349	104	DB1/ MDDIGND	-1925	-349	154	VGS	1575	-349	204	VCI	5075	-349
5	TESTO2	-8855	-349	55	TS1	-5355	-349	105	DB0	-1855	-349	155	AGND	1645	-349	205	VCI	5145	-349
6	TESTO3	-8785	-349	56	TS0	-5285	-349	106	GNDDUM	-1785	-349	156	AGND	1715	-349	206	VCI	5215	-349
7	TESTO4	-8715	-349	57	TEST5	-5215	-349	107	CSX	-1715	-349	157	AGND	1785	-349	207	VCILVL	5285	-349
8	GNDDUM	-8645	-349	58	TEST4	-5145	-349	108	DCX/MDDIGND	-1645	-349	158	AGND	1855	-349	208	DUMMY	5355	-349
9	TESTO5	-8575	-349	59	TEST3	-5075	-349	109	WRX/SCL/MDDI_STB_M	-1575	-349	159	AGND	1925	-349	209	DUMMY	5425	-349
10	TESTO6	-8505	-349	60	TEST2	-5005	-349	110	RDX/MDDIGND	-1505	-349	160	AGND	1995	-349	210	DUMMY	5495	-349
11	TESTO7	-8435	-349	61	TEST1	-4935	-349	111	GNDDUM	-1435	-349	161	AGND	2065	-349	211	DUMMY	5565	-349
12	TESTO8	-8365	-349	62	GNDDUM	-4865	-349	112	TE	-1365	-349	162	AGND	2135	-349	212	DUMMY	5635	-349
13	TESTO9	-8295	-349	63	DUMMY	-4795	-349	113	DIN	-1295	-349	163	AGND	2205	-349	213	GND	5705	-349
14	TESTO10	-8225	-349	64	IM2	-4725	-349	114	DOUT	-1225	-349	164	DUMMY	2275	-349	214	GND	5775	-349
15	TESTO11	-8155	-349	65	IM1	-4655	-349	115	VDD	-1155	-349	165	DUMMY	2345	-349	215	GND	5845	-349
16	TESTO12	-8085	-349	66	IM0	-4585	-349	116	VDD	-1085	-349	166	VREG	2415	-349	216	GND	5915	-349
17	TESTO13	-8015	-349	67	IOVCCDUM	-4515	-349	117	VDD	-1015	-349	167	DUMMY	2485	-349	217	GND	5985	-349
18	GNDDUM	-7945	-349	68	DUMMY	-4445	-349	118	VDD	-945	-349	168	C11A	2555	-349	218	AGND	6055	-349
19	TESTO14	-7875	-349	69	RESX	-4375	-349	119	VDD	-875	-349	169	C11A	2625	-349	219	AGND	6125	-349
20	TESTO15	-7805	-349	70	GNDDUM	-4305	-349	120	VDD	-805	-349	170	C11A	2695	-349	220	AGND	6195	-349
21	TESTO16	-7735	-349	71	LEDON	-4235	-349	121	VDD	-735	-349	171	C11A	2765	-349	221	AGND	6265	-349
22	DUMMY	-7665	-349	72	LEDPWM	-4165	-349	122	VDD	-665	-349	172	C11A	2835	-349	222	AGND	6335	-349
23	DUMMY	-7595	-349	73	VSYNC **(S_CS)**	-4095	-349	123	VDD	-595	-349	173	C11B	2905	-349	223	VGL	6405	-349
24	DUMMY	-7525	-349	74	HSYNC **(S_RS)**	-4025	-349	124	DUMMY	-525	-349	174	C11B	2975	-349	224	VGL	6475	-349
25	DUMMY	-7455	-349	75	IOVCCDUM	-3955	-349	125	VCOM	-455	-349	175	C11B	3045	-349	225	VGL	6545	-349
26	DUMMY	-7385	-349	76	DE **(S_WR)**	-3885	-349	126	VCOM	-385	-349	176	C11B	3115	-349	226	VGL	6615	-349
27	DUMMY	-7315	-349	77	PCLK	-3815	-349	127	VCOM	-315	-349	177	C11B	3185	-349	227	VGL	6685	-349
28	TEST_EN	-7245	-349	78	DB17 **(S_DB[8])**	-3745	-349	128	VCOM	-245	-349	178	C12A	3255	-349	228	VGL	6755	-349
29	GNDDUM	-7175	-349	79	DB16 **(S_DB[7])**	-3675	-349	129	VCOM	-175	-349	179	C12A	3325	-349	229	VGL	6825	-349
30	GND	-7105	-349	80	GNDDUM	-3605	-349	130	VCOM	-105	-349	180	C12A	3395	-349	230	VGL	6895	-349
31	GND	-7035	-349	81	DB15 **(S_DB[6])**	-3535	-349	131	VCOM	-35	-349	181	C12A	3465	-349	231	VGL	6965	-349
32	GND	-6965	-349	82	DB14 **(S_DB[5])**	-3465	-349	132	VCOM	35	-349	182	C12A	3535	-349	232	GNDDUM	7035	-349
33	GND	-6895	-349	83	DB13 **(S_DB[4])**	-3395	-349	133	VCOMH	105	-349	183	C12B	3605	-349	233	GNDDUM	7105	-349
34	GND	-6825	-349	84	DB12 **(S_DB[3])**	-3325	-349	134	VCOMH	175	-349	184	C12B	3675	-349	234	VGH	7175	-349
35	GND	-6755	-349	85	GNDDUM	-3255	-349	135	VCOMH	245	-349	185	C12B	3745	-349	235	VGH	7245	-349
36	GND	-6685	-349	86	DB11 **(S_DB[2])**	-3185	-349	136	VCOMH	315	-349	186	C12B	3815	-349	236	VGH	7315	-349
37	GND	-6615	-349	87	DB10 **(S_DB[1])**	-3115	-349	137	VCOMH	385	-349	187	C12B	3885	-349	237	VGH	7385	-349
38	GND	-6545	-349	88	DB9 **(S_DB[0])**	-3045	-349	138	VCOMH	455	-349	188	DDVDH	3955	-349	238	VGH	7455	-349
39	GND	-6475	-349	89	IOVCC	-2975	-349	139	VCOML	525	-349	189	DDVDH	4025	-349	239	VGH	7525	-349
40	GND	-6405	-349	90	IOVCC	-2905	-349	140	VCOML	595	-349	190	DDVDH	4095	-349	240	GNDDUM	7595	-349
41	VCC	-6335	-349	91	IOVCC	-2835	-349	141	VCOML	665	-349	191	DDVDH	4165	-349	241	VCL	7665	-349
42	VCC	-6265	-349	92	IOVCC	-2765	-349	142	VCOML	735	-349	192	DDVDH	4235	-349	242	VCL	7735	-349
43	VCC	-6195	-349	93	IOVCC	-2695	-349	143	VCOML	805	-349	193	DDVDH	4305	-349	243	VCL	7805	-349
44	VCC	-6125	-349	94	IOVCC	-2625	-349	144	VCOML	875	-349	194	DDVDH	4375	-349	244	C13A	7875	-349
45	VCC	-6055	-349	95	DB8/MDDIGND	-2555	-349	145	GND	945	-349	195	DDVDH	4445	-349	245	C13A	7945	-349
46	VCC	-5985	-349	96	GNDDUM	-2485	-349	146	GND	1015	-349	196	DDVDH	4515	-349	246	C13A	8015	-349
47	VCC	-5915	-349	97	DB7/MDDI_DATA_P	-2415	-349	147	GND	1085	-349	197	VCI1	4585	-349	247	C13B	8085	-349
48	TS8	-5845	-349	98	DB6/MDDIGND	-2345	-349	148	GND	1155	-349	198	VCI1	4655	-349	248	C13B	8155	-349
49	TS7	-5775	-349	99	DB5/MDDI_DATA_M	-2275	-349	149	GND	1225	-349	199	VCI1	4725	-349	249	C13B	8225	-349
50	TS6	-5705	-349	100	DB4/MDDIGND	-2205	-349	150	GND	1295	-349	200	VCI1	4795	-349	250	C21A	8295	-349

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
251	C21A	8365	-349	301	G70	8827.5	157	351	G170	8077.5	157	401	G270	7328	157	451	G370	6578	157
252	C21A	8435	-349	302	G72	8812.5	276	352	G172	8062.5	276	402	G272	7313	276	452	G372	6563	276
253	C21B	8505	-349	303	G74	8797.5	157	353	G174	8047.5	157	403	G274	7298	157	453	G374	6548	157
254	C21B	8575	-349	304	G76	8782.5	276	354	G176	8032.5	276	404	G276	7283	276	454	G376	6533	276
255	C21B	8645	-349	305	G78	8767.5	157	355	G178	8017.5	157	405	G278	7268	157	455	G378	6518	157
256	C22A	8715	-349	306	G80	8752.5	276	356	G180	8002.5	276	406	G280	7253	276	456	G380	6503	276
257	C22A	8785	-349	307	G82	8737.5	157	357	G182	7987.5	157	407	G282	7238	157	457	G382	6488	157
258	C22A	8855	-349	308	G84	8722.5	276	358	G184	7972.5	276	408	G284	7223	276	458	G384	6473	276
259	C22B	8925	-349	309	G86	8707.5	157	359	G186	7957.5	157	409	G286	7208	157	459	G386	6458	157
260	C22B	8995	-349	310	G88	8692.5	276	360	G188	7942.5	276	410	G288	7193	276	460	G388	6443	276
261	C22B	9065	-349	311	G90	8677.5	157	361	G190	7927.5	157	411	G290	7178	157	461	G390	6428	157
262	DUMMY	9135	-349	312	G92	8662.5	276	362	G192	7912.5	276	412	G292	7163	276	462	G392	6413	276
263	DUMMY	9397.5	157	313	G94	8647.5	157	363	G194	7897.5	157	413	G294	7148	157	463	G394	6398	157
264	DUMMY	9382.5	276	314	G96	8632.5	276	364	G196	7882.5	276	414	G296	7133	276	464	G396	6383	276
265	DUMMY	9367.5	157	315	G98	8617.5	157	365	G198	7867.5	157	415	G298	7118	157	465	G398	6368	157
266	VGLDMY1	9352.5	276	316	G100	8602.5	276	366	G200	7852.5	276	416	G300	7103	276	466	G400	6353	276
267	G2	9337.5	157	317	G102	8587.5	157	367	G202	7837.5	157	417	G302	7088	157	467	G402	6338	157
268	G4	9322.5	276	318	G104	8572.5	276	368	G204	7822.5	276	418	G304	7073	276	468	G404	6323	276
269	G6	9307.5	157	319	G106	8557.5	157	369	G206	7807.5	157	419	G306	7058	157	469	G406	6308	157
270	G8	9292.5	276	320	G108	8542.5	276	370	G208	7792.5	276	420	G308	7043	276	470	G408	6293	276
271	G10	9277.5	157	321	G110	8527.5	157	371	G210	7777.5	157	421	G310	7028	157	471	G410	6278	157
272	G12	9262.5	276	322	G112	8512.5	276	372	G212	7762.5	276	422	G312	7013	276	472	G412	6263	276
273	G14	9247.5	157	323	G114	8497.5	157	373	G214	7747.5	157	423	G314	6998	157	473	G414	6248	157
274	G16	9232.5	276	324	G116	8482.5	276	374	G216	7732.5	276	424	G316	6983	276	474	G416	6233	276
275	G18	9217.5	157	325	G118	8467.5	157	375	G218	7717.5	157	425	G318	6968	157	475	G418	6218	157
276	G20	9202.5	276	326	G120	8452.5	276	376	G220	7702.5	276	426	G320	6953	276	476	G420	6203	276
277	G22	9187.5	157	327	G122	8437.5	157	377	G222	7687.5	157	427	G322	6938	157	477	G422	6188	157
278	G24	9172.5	276	328	G124	8422.5	276	378	G224	7672.5	276	428	G324	6923	276	478	G424	6173	276
279	G26	9157.5	157	329	G126	8407.5	157	379	G226	7657.5	157	429	G326	6908	157	479	G426	6158	157
280	G28	9142.5	276	330	G128	8392.5	276	380	G228	7642.5	276	430	G328	6893	276	480	G428	6143	276
281	G30	9127.5	157	331	G130	8377.5	157	381	G230	7627.5	157	431	G330	6878	157	481	G430	6128	157
282	G32	9112.5	276	332	G132	8362.5	276	382	G232	7612.5	276	432	G332	6863	276	482	G432	6113	276
283	G34	9097.5	157	333	G134	8347.5	157	383	G234	7597.5	157	433	G334	6848	157	483	VGLDMY2	6098	157
284	G36	9082.5	276	334	G136	8332.5	276	384	G236	7582.5	276	434	G336	6833	276	484	TESTO5	5888	157
285	G38	9067.5	157	335	G138	8317.5	157	385	G238	7567.5	157	435	G338	6818	157	485	S720	5873	276
286	G40	9052.5	276	336	G140	8302.5	276	386	G240	7552.5	276	436	G340	6803	276	486	S719	5858	157
287	G42	9037.5	157	337	G142	8287.5	157	387	G242	7537.5	157	437	G342	6788	157	487	S718	5843	276
288	G44	9022.5	276	338	G144	8272.5	276	388	G244	7522.5	276	438	G344	6773	276	488	S717	5828	157
289	G46	9007.5	157	339	G146	8257.5	157	389	G246	7507.5	157	439	G346	6758	157	489	S716	5813	276
290	G48	8992.5	276	340	G148	8242.5	276	390	G248	7492.5	276	440	G348	6743	276	490	S715	5798	157
291	G50	8977.5	157	341	G150	8227.5	157	391	G250	7477.5	157	441	G350	6728	157	491	S714	5783	276
292	G52	8962.5	276	342	G152	8212.5	276	392	G252	7462.5	276	442	G352	6713	276	492	S713	5768	157
293	G54	8947.5	157	343	G154	8197.5	157	393	G254	7447.5	157	443	G354	6698	157	493	S712	5753	276
294	G56	8932.5	276	344	G156	8182.5	276	394	G256	7432.5	276	444	G356	6683	276	494	S711	5738	157
295	G58	8917.5	157	345	G158	8167.5	157	395	G258	7417.5	157	445	G358	6668	157	495	S710	5723	276
296	G60	8902.5	276	346	G160	8152.5	276	396	G260	7402.5	276	446	G360	6653	276	496	S709	5708	157
297	G62	8887.5	157	347	G162	8137.5	157	397	G262	7387.5	157	447	G362	6638	157	497	S708	5693	276
298	G64	8872.5	276	348	G164	8122.5	276	398	G264	7372.5	276	448	G364	6623	276	498	S707	5678	157
299	G66	8857.5	157	349	G166	8107.5	157	399	G266	7357.5	157	449	G366	6608	157	499	S706	5663	276
300	G68	8842.5	276	350	G168	8092.5	276	400	G268	7342.5	276	450	G368	6593	276	500	S705	5648	157

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
501	S704	5632.5	276	551	S654	4882.5	276	601	S604	4132.5	276	651	S554	3383	276	701	S504	2633	276
502	S703	5617.5	157	552	S653	4867.5	157	602	S603	4117.5	157	652	S553	3368	157	702	S503	2618	157
503	S702	5602.5	276	553	S652	4852.5	276	603	S602	4102.5	276	653	S552	3353	276	703	S502	2603	276
504	S701	5587.5	157	554	S651	4837.5	157	604	S601	4087.5	157	654	S551	3338	157	704	S501	2588	157
505	S700	5572.5	276	555	S650	4822.5	276	605	S600	4072.5	276	655	S550	3323	276	705	S500	2573	276
506	S699	5557.5	157	556	S649	4807.5	157	606	S599	4057.5	157	656	S549	3308	157	706	S499	2558	157
507	S698	5542.5	276	557	S648	4792.5	276	607	S598	4042.5	276	657	S548	3293	276	707	S498	2543	276
508	S697	5527.5	157	558	S647	4777.5	157	608	S597	4027.5	157	658	S547	3278	157	708	S497	2528	157
509	S696	5512.5	276	559	S646	4762.5	276	609	S596	4012.5	276	659	S546	3263	276	709	S496	2513	276
510	S695	5497.5	157	560	S645	4747.5	157	610	S595	3997.5	157	660	S545	3248	157	710	S495	2498	157
511	S694	5482.5	276	561	S644	4732.5	276	611	S594	3982.5	276	661	S544	3233	276	711	S494	2483	276
512	S693	5467.5	157	562	S643	4717.5	157	612	S593	3967.5	157	662	S543	3218	157	712	S493	2468	157
513	S692	5452.5	276	563	S642	4702.5	276	613	S592	3952.5	276	663	S542	3203	276	713	S492	2453	276
514	S691	5437.5	157	564	S641	4687.5	157	614	S591	3937.5	157	664	S541	3188	157	714	S491	2438	157
515	S690	5422.5	276	565	S640	4672.5	276	615	S590	3922.5	276	665	S540	3173	276	715	S490	2423	276
516	S689	5407.5	157	566	S639	4657.5	157	616	S589	3907.5	157	666	S539	3158	157	716	S489	2408	157
517	S688	5392.5	276	567	S638	4642.5	276	617	S588	3892.5	276	667	S538	3143	276	717	S488	2393	276
518	S687	5377.5	157	568	S637	4627.5	157	618	S587	3877.5	157	668	S537	3128	157	718	S487	2378	157
519	S686	5362.5	276	569	S636	4612.5	276	619	S586	3862.5	276	669	S536	3113	276	719	S486	2363	276
520	S685	5347.5	157	570	S635	4597.5	157	620	S585	3847.5	157	670	S535	3098	157	720	S485	2348	157
521	S684	5332.5	276	571	S634	4582.5	276	621	S584	3832.5	276	671	S534	3083	276	721	S484	2333	276
522	S683	5317.5	157	572	S633	4567.5	157	622	S583	3817.5	157	672	S533	3068	157	722	S483	2318	157
523	S682	5302.5	276	573	S632	4552.5	276	623	S582	3802.5	276	673	S532	3053	276	723	S482	2303	276
524	S681	5287.5	157	574	S631	4537.5	157	624	S581	3787.5	157	674	S531	3038	157	724	S481	2288	157
525	S680	5272.5	276	575	S630	4522.5	276	625	S580	3772.5	276	675	S530	3023	276	725	S480	2273	276
526	S679	5257.5	157	576	S629	4507.5	157	626	S579	3757.5	157	676	S529	3008	157	726	S479	2258	157
527	S678	5242.5	276	577	S628	4492.5	276	627	S578	3742.5	276	677	S528	2993	276	727	S478	2243	276
528	S677	5227.5	157	578	S627	4477.5	157	628	S577	3727.5	157	678	S527	2978	157	728	S477	2228	157
529	S676	5212.5	276	579	S626	4462.5	276	629	S576	3712.5	276	679	S526	2963	276	729	S476	2213	276
530	S675	5197.5	157	580	S625	4447.5	157	630	S575	3697.5	157	680	S525	2948	157	730	S475	2198	157
531	S674	5182.5	276	581	S624	4432.5	276	631	S574	3682.5	276	681	S524	2933	276	731	S474	2183	276
532	S673	5167.5	157	582	S623	4417.5	157	632	S573	3667.5	157	682	S523	2918	157	732	S473	2168	157
533	S672	5152.5	276	583	S622	4402.5	276	633	S572	3652.5	276	683	S522	2903	276	733	S472	2153	276
534	S671	5137.5	157	584	S621	4387.5	157	634	S571	3637.5	157	684	S521	2888	157	734	S471	2138	157
535	S670	5122.5	276	585	S620	4372.5	276	635	S570	3622.5	276	685	S520	2873	276	735	S470	2123	276
536	S669	5107.5	157	586	S619	4357.5	157	636	S569	3607.5	157	686	S519	2858	157	736	S469	2108	157
537	S668	5092.5	276	587	S618	4342.5	276	637	S568	3592.5	276	687	S518	2843	276	737	S468	2093	276
538	S667	5077.5	157	588	S617	4327.5	157	638	S567	3577.5	157	688	S517	2828	157	738	S467	2078	157
539	S666	5062.5	276	589	S616	4312.5	276	639	S566	3562.5	276	689	S516	2813	276	739	S466	2063	276
540	S665	5047.5	157	590	S615	4297.5	157	640	S565	3547.5	157	690	S515	2798	157	740	S465	2048	157
541	S664	5032.5	276	591	S614	4282.5	276	641	S564	3532.5	276	691	S514	2783	276	741	S464	2033	276
542	S663	5017.5	157	592	S613	4267.5	157	642	S563	3517.5	157	692	S513	2768	157	742	S463	2018	157
543	S662	5002.5	276	593	S612	4252.5	276	643	S562	3502.5	276	693	S512	2753	276	743	S462	2003	276
544	S661	4987.5	157	594	S611	4237.5	157	644	S561	3487.5	157	694	S511	2738	157	744	S461	1988	157
545	S660	4972.5	276	595	S610	4222.5	276	645	S560	3472.5	276	695	S510	2723	276	745	S460	1973	276
546	S659	4957.5	157	596	S609	4207.5	157	646	S559	3457.5	157	696	S509	2708	157	746	S459	1958	157
547	S658	4942.5	276	597	S608	4192.5	276	647	S558	3442.5	276	697	S508	2693	276	747	S458	1943	276
548	S657	4927.5	157	598	S607	4177.5	157	648	S557	3427.5	157	698	S507	2678	157	748	S457	1928	157
549	S656	4912.5	276	599	S606	4162.5	276	649	S556	3412.5	276	699	S506	2663	276	749	S456	1913	276
550	S655	4897.5	157	600	S605	4147.5	157	650	S555	3397.5	157	700	S505	2648	157	750	S455	1898	157

Pad No.	Pad Name	X	Y
751	S454	1882.5	276
752	S453	1867.5	157
753	S452	1852.5	276
754	S451	1837.5	157
755	S450	1822.5	276
756	S449	1807.5	157
757	S448	1792.5	276
758	S447	1777.5	157
759	S446	1762.5	276
760	S445	1747.5	157
761	S444	1732.5	276
762	S443	1717.5	157
763	S442	1702.5	276
764	S441	1687.5	157
765	S440	1672.5	276
766	S439	1657.5	157
767	S438	1642.5	276
768	S437	1627.5	157
769	S436	1612.5	276
770	S435	1597.5	157
771	S434	1582.5	276
772	S433	1567.5	157
773	S432	1552.5	276
774	S431	1537.5	157
775	S430	1522.5	276
776	S429	1507.5	157
777	S428	1492.5	276
778	S427	1477.5	157
779	S426	1462.5	276
780	S425	1447.5	157
781	S424	1432.5	276
782	S423	1417.5	157
783	S422	1402.5	276
784	S421	1387.5	157
785	S420	1372.5	276
786	S419	1357.5	157
787	S418	1342.5	276
788	S417	1327.5	157
789	S416	1312.5	276
790	S415	1297.5	157
791	S414	1282.5	276
792	S413	1267.5	157
793	S412	1252.5	276
794	S411	1237.5	157
795	S410	1222.5	276
796	S409	1207.5	157
797	S408	1192.5	276
798	S407	1177.5	157
799	S406	1162.5	276
800	S405	1147.5	157

Pad No.	Pad Name	X	Y
801	S404	1132.5	276
802	S403	1117.5	157
803	S402	1102.5	276
804	S401	1087.5	157
805	S400	1072.5	276
806	S399	1057.5	157
807	S398	1042.5	276
808	S397	1027.5	157
809	S396	1012.5	276
810	S395	997.5	157
811	S394	982.5	276
812	S393	967.5	157
813	S392	952.5	276
814	S391	937.5	157
815	S390	922.5	276
816	S389	907.5	157
817	S388	892.5	276
818	S387	877.5	157
819	S386	862.5	276
820	S385	847.5	157
821	S384	832.5	276
822	S383	817.5	157
823	S382	802.5	276
824	S381	787.5	157
825	S380	772.5	276
826	S379	757.5	157
827	S378	742.5	276
828	S377	727.5	157
829	S376	712.5	276
830	S375	697.5	157
831	S374	682.5	276
832	S373	667.5	157
833	S372	652.5	276
834	S371	637.5	157
835	S370	622.5	276
836	S369	607.5	157
837	S368	592.5	276
838	S367	577.5	157
839	S366	562.5	276
840	S365	547.5	157
841	S364	532.5	276
842	S363	517.5	157
843	S362	502.5	276
844	S361	487.5	157
845	TESTO6	472.5	276
846	TESTO7	457.5	157
847	TESTO8	442.5	276
848	TESTO9	427.5	157
849	TESTO10	-427.5	276
850	TESTO11	-442.5	157

Pad No.	Pad Name	X	Y
851	TESTO12	-457.5	276
852	TESTO13	-472.5	157
853	S360	-487.5	276
854	S359	-502.5	157
855	S358	-517.5	276
856	S357	-532.5	157
857	S356	-547.5	276
858	S355	-562.5	157
859	S354	-577.5	276
860	S353	-592.5	157
861	S352	-607.5	276
862	S351	-622.5	157
863	S350	-637.5	276
864	S349	-652.5	157
865	S348	-667.5	276
866	S347	-682.5	157
867	S346	-697.5	276
868	S345	-712.5	157
869	S344	-727.5	276
870	S343	-742.5	157
871	S342	-757.5	276
872	S341	-772.5	157
873	S340	-787.5	276
874	S339	-802.5	157
875	S338	-817.5	276
876	S337	-832.5	157
877	S336	-847.5	276
878	S335	-862.5	157
879	S334	-877.5	276
880	S333	-892.5	157
881	S332	-907.5	276
882	S331	-922.5	157
883	S330	-937.5	276
884	S329	-952.5	157
885	S328	-967.5	276
886	S327	-982.5	157
887	S326	-997.5	276
888	S325	-1013	157
889	S324	-1028	276
890	S323	-1043	157
891	S322	-1058	276
892	S321	-1073	157
893	S320	-1088	276
894	S319	-1103	157
895	S318	-1118	276
896	S317	-1133	157
897	S316	-1148	276
898	S315	-1163	157
899	S314	-1178	276
900	S313	-1193	157

Pad No.	Pad Name	X	Y
901	S312	-1208	276
902	S311	-1223	157
903	S310	-1238	276
904	S309	-1253	157
905	S308	-1268	276
906	S307	-1283	157
907	S306	-1298	276
908	S305	-1313	157
909	S304	-1328	276
910	S303	-1343	157
911	S302	-1358	276
912	S301	-1373	157
913	S300	-1388	276
914	S299	-1403	157
915	S298	-1418	276
916	S297	-1433	157
917	S296	-1448	276
918	S295	-1463	157
919	S294	-1478	276
920	S293	-1493	157
921	S292	-1508	276
922	S291	-1523	157
923	S290	-1538	276
924	S289	-1553	157
925	S288	-1568	276
926	S287	-1583	157
927	S286	-1598	276
928	S285	-1613	157
929	S284	-1628	276
930	S283	-1643	157
931	S282	-1658	276
932	S281	-1673	157
933	S280	-1688	276
934	S279	-1703	157
935	S278	-1718	276
936	S277	-1733	157
937	S276	-1748	276
938	S275	-1763	157
939	S274	-1778	276
940	S273	-1793	157
941	S272	-1808	276
942	S271	-1823	157
943	S270	-1838	276
944	S269	-1853	157
945	S268	-1868	276
946	S267	-1883	157
947	S266	-1898	276
948	S265	-1913	157
949	S264	-1928	276
950	S263	-1943	157

Pad No.	Pad Name	X	Y
951	S262	-1958	276
952	S261	-1973	157
953	S260	-1988	276
954	S259	-2003	157
955	S258	-2018	276
956	S257	-2033	157
957	S256	-2048	276
958	S255	-2063	157
959	S254	-2078	276
960	S253	-2093	157
961	S252	-2108	276
962	S251	-2123	157
963	S250	-2138	276
964	S249	-2153	157
965	S248	-2168	276
966	S247	-2183	157
967	S246	-2198	276
968	S245	-2213	157
969	S244	-2228	276
970	S243	-2243	157
971	S242	-2258	276
972	S241	-2273	157
973	S240	-2288	276
974	S239	-2303	157
975	S238	-2318	276
976	S237	-2333	157
977	S236	-2348	276
978	S235	-2363	157
979	S234	-2378	276
980	S233	-2393	157
981	S232	-2408	276
982	S231	-2423	157
983	S230	-2438	276
984	S229	-2453	157
985	S228	-2468	276
986	S227	-2483	157
987	S226	-2498	276
988	S225	-2513	157
989	S224	-2528	276
990	S223	-2543	157
991	S222	-2558	276
992	S221	-2573	157
993	S220	-2588	276
994	S219	-2603	157
995	S218	-2618	276
996	S217	-2633	157
997	S216	-2648	276
998	S215	-2663	157
999	S214	-2678	276
1000	S213	-3693	157

Pad No.	Pad Name	X	Y
751	S454	1882.5	276
752	S453	1867.5	157
753	S452	1852.5	276
754	S451	1837.5	157
755	S450	1822.5	276
756	S449	1807.5	157
757	S448	1792.5	276
758	S447	1777.5	157
759	S446	1762.5	276
760	S445	1747.5	157
761	S444	1732.5	276
762	S443	1717.5	157
763	S442	1702.5	276
764	S441	1687.5	157
765	S440	1672.5	276
766	S439	1657.5	157
767	S438	1642.5	276
768	S437	1627.5	157
769	S436	1612.5	276
770	S435	1597.5	157
771	S434	1582.5	276
772	S433	1567.5	157
773	S432	1552.5	276
774	S431	1537.5	157
775	S430	1522.5	276
776	S429	1507.5	157
777	S428	1492.5	276
778	S427	1477.5	157
779	S426	1462.5	276
780	S425	1447.5	157
781	S424	1432.5	276
782	S423	1417.5	157
783	S422	1402.5	276
784	S421	1387.5	157
785	S420	1372.5	276
786	S419	1357.5	157
787	S418	1342.5	276
788	S417	1327.5	157
789	S416	1312.5	276
790	S415	1297.5	157
791	S414	1282.5	276
792	S413	1267.5	157
793	S412	1252.5	276
794	S411	1237.5	157
795	S410	1222.5	276
796	S409	1207.5	157
797	S408	1192.5	276
798	S407	1177.5	157
799	S406	1162.5	276
800	S405	1147.5	157

Pad No.	Pad Name	X	Y
801	S404	1132.5	276
802	S403	1117.5	157
803	S402	1102.5	276
804	S401	1087.5	157
805	S400	1072.5	276
806	S399	1057.5	157
807	S398	1042.5	276
808	S397	1027.5	157
809	S396	1012.5	276
810	S395	997.5	157
811	S394	982.5	276
812	S393	967.5	157
813	S392	952.5	276
814	S391	937.5	157
815	S390	922.5	276
816	S389	907.5	157
817	S388	892.5	276
818	S387	877.5	157
819	S386	862.5	276
820	S385	847.5	157
821	S384	832.5	276
822	S383	817.5	157
823	S382	802.5	276
824	S381	787.5	157
825	S380	772.5	276
826	S379	757.5	157
827	S378	742.5	276
828	S377	727.5	157
829	S376	712.5	276
830	S375	697.5	157
831	S374	682.5	276
832	S373	667.5	157
833	S372	652.5	276
834	S371	637.5	157
835	S370	622.5	276
836	S369	607.5	157
837	S368	592.5	276
838	S367	577.5	157
839	S366	562.5	276
840	S365	547.5	157
841	S364	532.5	276
842	S363	517.5	157
843	S362	502.5	276
844	S361	487.5	157
845	DUMMY	472.5	276
846	DUMMY	457.5	157
847	DUMMY	442.5	276
848	DUMMY	427.5	157
849	DUMMY	-427.5	276
850	DUMMY	-442.5	157

Pad No.	Pad Name	X	Y
851	DUMMY	-457.5	276
852	DUMMY	-472.5	157
853	S360	-487.5	276
854	S359	-502.5	157
855	S358	-517.5	276
856	S357	-532.5	157
857	S356	-547.5	276
858	S355	-562.5	157
859	S354	-577.5	276
860	S353	-592.5	157
861	S352	-607.5	276
862	S351	-622.5	157
863	S350	-637.5	276
864	S349	-652.5	157
865	S348	-667.5	276
866	S347	-682.5	157
867	S346	-697.5	276
868	S345	-712.5	157
869	S344	-727.5	276
870	S343	-742.5	157
871	S342	-757.5	276
872	S341	-772.5	157
873	S340	-787.5	276
874	S339	-802.5	157
875	S338	-817.5	276
876	S337	-832.5	157
877	S336	-847.5	276
878	S335	-862.5	157
879	S334	-877.5	276
880	S333	-892.5	157
881	S332	-907.5	276
882	S331	-922.5	157
883	S330	-937.5	276
884	S329	-952.5	157
885	S328	-967.5	276
886	S327	-982.5	157
887	S326	-997.5	276
888	S325	-1013	157
889	S324	-1028	276
890	S323	-1043	157
891	S322	-1058	276
892	S321	-1073	157
893	S320	-1088	276
894	S319	-1103	157
895	S318	-1118	276
896	S317	-1133	157
897	S316	-1148	276
898	S315	-1163	157
899	S314	-1178	276
900	S313	-1193	157

Pad No.	Pad Name	X	Y
901	S312	-1208	276
902	S311	-1223	157
903	S310	-1238	276
904	S309	-1253	157
905	S308	-1268	276
906	S307	-1283	157
907	S306	-1298	276
908	S305	-1313	157
909	S304	-1328	276
910	S303	-1343	157
911	S302	-1358	276
912	S301	-1373	157
913	S300	-1388	276
914	S299	-1403	157
915	S298	-1418	276
916	S297	-1433	157
917	S296	-1448	276
918	S295	-1463	157
919	S294	-1478	276
920	S293	-1493	157
921	S292	-1508	276
922	S291	-1523	157
923	S290	-1538	276
924	S289	-1553	157
925	S288	-1568	276
926	S287	-1583	157
927	S286	-1598	276
928	S285	-1613	157
929	S284	-1628	276
930	S283	-1643	157
931	S282	-1658	276
932	S281	-1673	157
933	S280	-1688	276
934	S279	-1703	157
935	S278	-1718	276
936	S277	-1733	157
937	S276	-1748	276
938	S275	-1763	157
939	S274	-1778	276
940	S273	-1793	157
941	S272	-1808	276
942	S271	-1823	157
943	S270	-1838	276
944	S269	-1853	157
945	S268	-1868	276
946	S267	-1883	157
947	S266	-1898	276
948	S265	-1913	157
949	S264	-1928	276
950	S263	-1943	157

Pad No.	Pad Name	X	Y
951	S262	-1958	276
952	S261	-1973	157
953	S260	-1988	276
954	S259	-2003	157
955	S258	-2018	276
956	S257	-2033	157
957	S256	-2048	276
958	S255	-2063	157
959	S254	-2078	276
960	S253	-2093	157
961	S252	-2108	276
962	S251	-2123	157
963	S250	-2138	276
964	S249	-2153	157
965	S248	-2168	276
966	S247	-2183	157
967	S246	-2198	276
968	S245	-2213	157
969	S244	-2228	276
970	S243	-2243	157
971	S242	-2258	276
972	S241	-2273	157
973	S240	-2288	276
974	S239	-2303	157
975	S238	-2318	276
976	S237	-2333	157
977	S236	-2348	276
978	S235	-2363	157
979	S234	-2378	276
980	S233	-2393	157
981	S232	-2408	276
982	S231	-2423	157
983	S230	-2438	276
984	S229	-2453	157
985	S228	-2468	276
986	S227	-2483	157
987	S226	-2498	276
988	S225	-2513	157
989	S224	-2528	276
990	S223	-2543	157
991	S222	-2558	276
992	S221	-2573	157
993	S220	-2588	276
994	S219	-2603	157
995	S218	-2618	276
996	S217	-2633	157
997	S216	-2648	276
998	S215	-2663	157
999	S214	-2678	276
1000	S213	-2693	157

Pad No.	Pad Name	X	Y
1001	S212	-2707.5	276
1002	S211	-2722.5	157
1003	S210	-2737.5	276
1004	S209	-2752.5	157
1005	S208	-2767.5	276
1006	S207	-2782.5	157
1007	S206	-2797.5	276
1008	S205	-2812.5	157
1009	S204	-2827.5	276
1010	S203	-2842.5	157
1011	S202	-2857.5	276
1012	S201	-2872.5	157
1013	S200	-2887.5	276
1014	S199	-2902.5	157
1015	S198	-2917.5	276
1016	S197	-2932.5	157
1017	S196	-2947.5	276
1018	S195	-2962.5	157
1019	S194	-2977.5	276
1020	S193	-2992.5	157
1021	S192	-3007.5	276
1022	S191	-3022.5	157
1023	S190	-3037.5	276
1024	S189	-3052.5	157
1025	S188	-3067.5	276
1026	S187	-3082.5	157
1027	S186	-3097.5	276
1028	S185	-3112.5	157
1029	S184	-3127.5	276
1030	S183	-3142.5	157
1031	S182	-3157.5	276
1032	S181	-3172.5	157
1033	S180	-3187.5	276
1034	S179	-3202.5	157
1035	S178	-3217.5	276
1036	S177	-3232.5	157
1037	S176	-3247.5	276
1038	S175	-3262.5	157
1039	S174	-3277.5	276
1040	S173	-3292.5	157
1041	S172	-3307.5	276
1042	S171	-3322.5	157
1043	S170	-3337.5	276
1044	S169	-3352.5	157
1045	S168	-3367.5	276
1046	S167	-3382.5	157
1047	S166	-3397.5	276
1048	S165	-3412.5	157
1049	S164	-3427.5	276
1050	S163	-3442.5	157

Pad No.	Pad Name	X	Y
1051	S162	-3458	276
1052	S161	-3473	157
1053	S160	-3488	276
1054	S159	-3503	157
1055	S158	-3518	276
1056	S157	-3533	157
1057	S156	-3548	276
1058	S155	-3563	157
1059	S154	-3578	276
1060	S153	-3593	157
1061	S152	-3608	276
1062	S151	-3623	157
1063	S150	-3638	276
1064	S149	-3653	157
1065	S148	-3668	276
1066	S147	-3683	157
1067	S146	-3698	276
1068	S145	-3713	157
1069	S144	-3728	276
1070	S143	-3743	157
1071	S142	-3758	276
1072	S141	-3773	157
1073	S140	-3788	276
1074	S139	-3803	157
1075	S138	-3818	276
1076	S137	-3833	157
1077	S136	-3848	276
1078	S135	-3863	157
1079	S134	-3878	276
1080	S133	-3893	157
1081	S132	-3908	276
1082	S131	-3923	157
1083	S130	-3938	276
1084	S129	-3953	157
1085	S128	-3968	276
1086	S127	-3983	157
1087	S126	-3998	276
1088	S125	-4013	157
1089	S124	-4028	276
1090	S123	-4043	157
1091	S122	-4058	276
1092	S121	-4073	157
1093	S120	-4088	276
1094	S119	-4103	157
1095	S118	-4118	276
1096	S117	-4133	157
1097	S116	-4148	276
1098	S115	-4163	157
1099	S114	-4178	276
1100	S113	-4193	157

Pad No.	Pad Name	X	Y
1101	S112	-4208	276
1102	S111	-4223	157
1103	S110	-4238	276
1104	S109	-4253	157
1105	S108	-4268	276
1106	S107	-4283	157
1107	S106	-4298	276
1108	S105	-4313	157
1109	S104	-4328	276
1110	S103	-4343	157
1111	S102	-4358	276
1112	S101	-4373	157
1113	S100	-4388	276
1114	S99	-4403	157
1115	S98	-4418	276
1116	S97	-4433	157
1117	S96	-4448	276
1118	S95	-4463	157
1119	S94	-4478	276
1120	S93	-4493	157
1121	S92	-4508	276
1122	S91	-4523	157
1123	S90	-4538	276
1124	S89	-4553	157
1125	S88	-4568	276
1126	S87	-4583	157
1127	S86	-4598	276
1128	S85	-4613	157
1129	S84	-4628	276
1130	S83	-4643	157
1131	S82	-4658	276
1132	S81	-4673	157
1133	S80	-4688	276
1134	S79	-4703	157
1135	S78	-4718	276
1136	S77	-4733	157
1137	S76	-4748	276
1138	S75	-4763	157
1139	S74	-4778	276
1140	S73	-4793	157
1141	S72	-4808	276
1142	S71	-4823	157
1143	S70	-4838	276
1144	S69	-4853	157
1145	S68	-4868	276
1146	S67	-4883	157
1147	S66	-4898	276
1148	S65	-4913	157
1149	S64	-4928	276
1150	S63	-4943	157

Pad No.	Pad Name	X	Y
1151	S62	-4958	276
1152	S61	-4973	157
1153	S60	-4988	276
1154	S59	-5003	157
1155	S58	-5018	276
1156	S57	-5033	157
1157	S56	-5048	276
1158	S55	-5063	157
1159	S54	-5078	276
1160	S53	-5093	157
1161	S52	-5108	276
1162	S51	-5123	157
1163	S50	-5138	276
1164	S49	-5153	157
1165	S48	-5168	276
1166	S47	-5183	157
1167	S46	-5198	276
1168	S45	-5213	157
1169	S44	-5228	276
1170	S43	-5243	157
1171	S42	-5258	276
1172	S41	-5273	157
1173	S40	-5288	276
1174	S39	-5303	157
1175	S38	-5318	276
1176	S37	-5333	157
1177	S36	-5348	276
1178	S35	-5363	157
1179	S34	-5378	276
1180	S33	-5393	157
1181	S32	-5408	276
1182	S31	-5423	157
1183	S30	-5438	276
1184	S29	-5453	157
1185	S28	-5468	276
1186	S27	-5483	157
1187	S26	-5498	276
1188	S25	-5513	157
1189	S24	-5528	276
1190	S23	-5543	157
1191	S22	-5558	276
1192	S21	-5573	157
1193	S20	-5588	276
1194	S19	-5603	157
1195	S18	-5618	276
1196	S17	-5633	157
1197	S16	-5648	276
1198	S15	-5663	157
1199	S14	-5678	276
1200	S13	-5693	157

Pad No.	Pad Name	X	Y
1201	S12	-5708	276
1202	S11	-5723	157
1203	S10	-5738	276
1204	S9	-5753	157
1205	S8	-5768	276
1206	S7	-5783	157
1207	S6	-5798	276
1208	S5	-5813	157
1209	S4	-5828	276
1210	S3	-5843	157
1211	S2	-5858	276
1212	S1	-5873	157
1213	DUMMY	-5888	276
1214	VGLDMY3	-6098	276
1215	G431	-6113	157
1216	G429	-6128	276
1217	G427	-6143	157
1218	G425	-6158	276
1219	G423	-6173	157
1220	G421	-6188	276
1221	G419	-6203	157
1222	G417	-6218	276
1223	G415	-6233	157
1224	G413	-6248	276
1225	G411	-6263	157
1226	G409	-6278	276
1227	G407	-6293	157
1228	G405	-6308	276
1229	G403	-6323	157
1230	G401	-6338	276
1231	G399	-6353	157
1232	G397	-6368	276
1233	G395	-6383	157
1234	G393	-6398	276
1235	G391	-6413	157
1236	G389	-6428	276
1237	G387	-6443	157
1238	G385	-6458	276
1239	G383	-6473	157
1240	G381	-6488	276
1241	G379	-6503	157
1242	G377	-6518	276
1243	G375	-6533	157
1244	G373	-6548	276
1245	G371	-6563	157
1246	G369	-6578	276
1247	G367	-6593	157
1248	G365	-6608	276
1249	G363	-6623	157
1250	G361	-6638	276

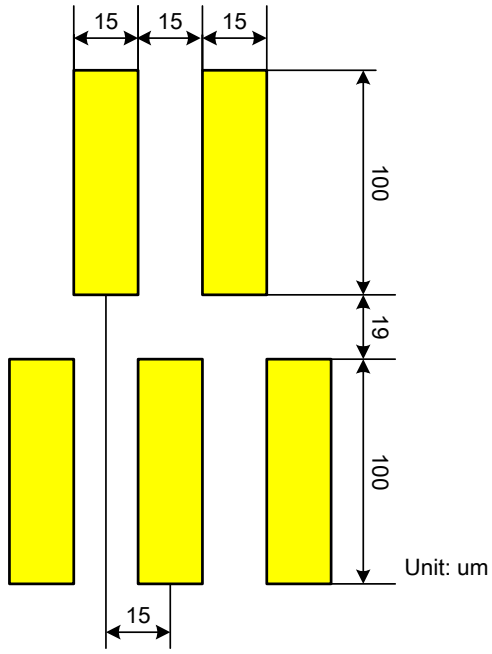
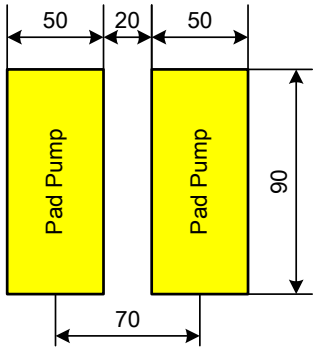
Pad No.	Pad Name	X	Y
1251	G359	-6652.5	157
1252	G357	-6667.5	276
1253	G355	-6682.5	157
1254	G353	-6697.5	276
1255	G351	-6712.5	157
1256	G349	-6727.5	276
1257	G347	-6742.5	157
1258	G345	-6757.5	276
1259	G343	-6772.5	157
1260	G341	-6787.5	276
1261	G339	-6802.5	157
1262	G337	-6817.5	276
1263	G335	-6832.5	157
1264	G333	-6847.5	276
1265	G331	-6862.5	157
1266	G329	-6877.5	276
1267	G327	-6892.5	157
1268	G325	-6907.5	276
1269	G323	-6922.5	157
1270	G321	-6937.5	276
1271	G319	-6952.5	157
1272	G317	-6967.5	276
1273	G315	-6982.5	157
1274	G313	-6997.5	276
1275	G311	-7012.5	157
1276	G309	-7027.5	276
1277	G307	-7042.5	157
1278	G305	-7057.5	276
1279	G303	-7072.5	157
1280	G301	-7087.5	276
1281	G299	-7102.5	157
1282	G297	-7117.5	276
1283	G295	-7132.5	157
1284	G293	-7147.5	276
1285	G291	-7162.5	157
1286	G289	-7177.5	276
1287	G287	-7192.5	157
1288	G285	-7207.5	276
1289	G283	-7222.5	157
1290	G281	-7237.5	276
1291	G279	-7252.5	157
1292	G277	-7267.5	276
1293	G275	-7282.5	157
1294	G273	-7297.5	276
1295	G271	-7312.5	157
1296	G269	-7327.5	276
1297	G267	-7342.5	157
1298	G265	-7357.5	276
1299	G263	-7372.5	157
1300	G261	-7387.5	276

Pad No.	Pad Name	X	Y
1301	G259	-7403	157
1302	G257	-7418	276
1303	G255	-7433	157
1304	G253	-7448	276
1305	G251	-7463	157
1306	G249	-7478	276
1307	G247	-7493	157
1308	G245	-7508	276
1309	G243	-7523	157
1310	G241	-7538	276
1311	G239	-7553	157
1312	G237	-7568	276
1313	G235	-7583	157
1314	G233	-7598	276
1315	G231	-7613	157
1316	G229	-7628	276
1317	G227	-7643	157
1318	G225	-7658	276
1319	G223	-7673	157
1320	G221	-7688	276
1321	G219	-7703	157
1322	G217	-7718	276
1323	G215	-7733	157
1324	G213	-7748	276
1325	G211	-7763	157
1326	G209	-7778	276
1327	G207	-7793	157
1328	G205	-7808	276
1329	G203	-7823	157
1330	G201	-7838	276
1331	G199	-7853	157
1332	G197	-7868	276
1333	G195	-7883	157
1334	G193	-7898	276
1335	G191	-7913	157
1336	G189	-7928	276
1337	G187	-7943	157
1338	G185	-7958	276
1339	G183	-7973	157
1340	G181	-7988	276
1341	G179	-8003	157
1342	G177	-8018	276
1343	G175	-8033	157
1344	G173	-8048	276
1345	G171	-8063	157
1346	G169	-8078	276
1347	G167	-8093	157
1348	G165	-8108	276
1349	G163	-8123	157
1350	G161	-8138	276

Pad No.	Pad Name	X	Y
1351	G159	-8153	157
1352	G157	-8168	276
1353	G155	-8183	157
1354	G153	-8198	276
1355	G151	-8213	157
1356	G149	-8228	276
1357	G147	-8243	157
1358	G145	-8258	276
1359	G143	-8273	157
1360	G141	-8288	276
1361	G139	-8303	157
1362	G137	-8318	276
1363	G135	-8333	157
1364	G133	-8348	276
1365	G131	-8363	157
1366	G129	-8378	276
1367	G127	-8393	157
1368	G125	-8408	276
1369	G123	-8423	157
1370	G121	-8438	276
1371	G119	-8453	157
1372	G117	-8468	276
1373	G115	-8483	157
1374	G113	-8498	276
1375	G111	-8513	157
1376	G109	-8528	276
1377	G107	-8543	157
1378	G105	-8558	276
1379	G103	-8573	157
1380	G101	-8588	276
1381	G99	-8603	157
1382	G97	-8618	276
1383	G95	-8633	157
1384	G93	-8648	276
1385	G91	-8663	157
1386	G89	-8678	276
1387	G87	-8693	157
1388	G85	-8708	276
1389	G83	-8723	157
1390	G81	-8738	276
1391	G79	-8753	157
1392	G77	-8768	276
1393	G75	-8783	157
1394	G73	-8798	276
1395	G71	-8813	157
1396	G69	-8828	276
1397	G67	-8843	157
1398	G65	-8858	276
1399	G63	-8873	157
1400	G61	-8888	276

Pad No.	Pad Name	X	Y
1401	G59	-8903	157
1402	G57	-8918	276
1403	G55	-8933	157
1404	G53	-8948	276
1405	G51	-8963	157
1406	G49	-8978	276
1407	G47	-8993	157
1408	G45	-9008	276
1409	G43	-9023	157
1410	G41	-9038	276
1411	G39	-9053	157
1412	G37	-9068	276
1413	G35	-9083	157
1414	G33	-9098	276
1415	G31	-9113	157
1416	G29	-9128	276
1417	G27	-9143	157
1418	G25	-9158	276
1419	G23	-9173	157
1420	G21	-9188	276
1421	G19	-9203	157
1422	G17	-9218	276
1423	G15	-9233	157
1424	G13	-9248	276
1425	G11	-9263	157
1426	G9	-9278	276
1427	G7	-9293	157
1428	G5	-9308	276
1429	G3	-9323	157
1430	G1	-9338	276
1431	VGLDMY4	-9353	157
1432	DUMMY	-9368	276
1433	DUMMYR3	-9383	157
1434	DUMMYR4	-9398	276

Alignment mark	X	Y
A1	-9381	-251
A2	9381	-251

S1 ~ S720 G1 ~ G432	
I/O Pads	

6. Block Function Description

Interface

The ILI9327 supports MIPI DBI Type B (18/16/9/8bit) and MIPI DBI Type C (Option 1, 3). The interface is selected by setting IM[2:0] pin.

IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	Colors
0	0	0	DBI Type B 18-bit	DB[17:0]	262K
0	0	1	DBI Type B 9-bit	DB[8:0]	262K
0	1	0	DBI Type B 16-bit	DB[15:0]	65K/262K
0	1	1	DBI Type B 8-bit	DB[7:0]	65K/262K
1	0	0	MDDI		65K/262K
1	0	1	DBI Type C 9-bit	DIN, DOUT	8/262K
1	1	0	CPU 9-bit	DB[8:0]/DB[8:1]	262K
1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K

Note: Set number of colors using set_pixel_format: 3Ah.

(a) MIPI DBI Type B (18-/ 16-/ 9-/ 8- bit)

The ILI9327 supports MIPI DBI Type B (18/16/9/8bit) that uses command method which has 8-bit command registers and 8-bit parameter registers. The ILI9327 also has the 18-bit write register (WDR) and read register (RDR). The WDR register is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip.

The RDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the ILI9327 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first time read and valid data is sent as the ILI9327 reads second and subsequent data from the frame memory.

Register selection

DCX	RDX	WRX	Operation
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(b) MIPI DBI Type C (Option 1, 3)

The ILI9327 also supports MIPI DBI type C 9bit (Option 1) and 8bit (Option 3) serial interface that uses signals CSX, DCX, SCL, DIN and DOUT.

2. Video Image Interface (TE-signal, DPI, VSYNC-I/F)

The ILI9327 supports TE, DPI and VSYNC interfaces as external display interface for video image. When DBI is selected, display data is written in synchronization with TE signal which is generated from internal

clock to prevent tearing effect on the panel.

When DPI is selected, externally supplied VSYNC, HSYNC and PCLK signals drive the chip. Display data (DB[17:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without tearing effect on the panel.

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CDR, the data is transferred from CDR to AC.

When data is written/read to/from GRAM, address counter (AC) will increment by +1 or –1 automatically. The ILI9327 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 233,280 bytes pattern data using 18 bits for one pixel, enabling a maximum 240RGB x 432 dot graphic display at the maximum.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. The ILI9327 displays 262,144 colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to a-TFT panel, VREG1OUT, VGH, VGL, VCOMH and VCOML.

Timing Generating

Timing generator is used to generate the timing signals for internal circuits such as the internal GRAM read/write, display control signals. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is output separately so that they do not interfere with each other.

Oscillator

The ILI9327 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The liquid crystal display driver circuit consists of 720 source drivers (S1~S720). Display pattern data is latched when 720 pixels data is input. This latched data controls source drivers and outputs drive waveform. The gate driver consists of 432 gate drivers (G1~G432) and outputs either VGH or VGL level. The shift direction of gate driver is set by GS bit. Scan direction of gate driver can also be set by the SM bit to fit the panel gate line layout.

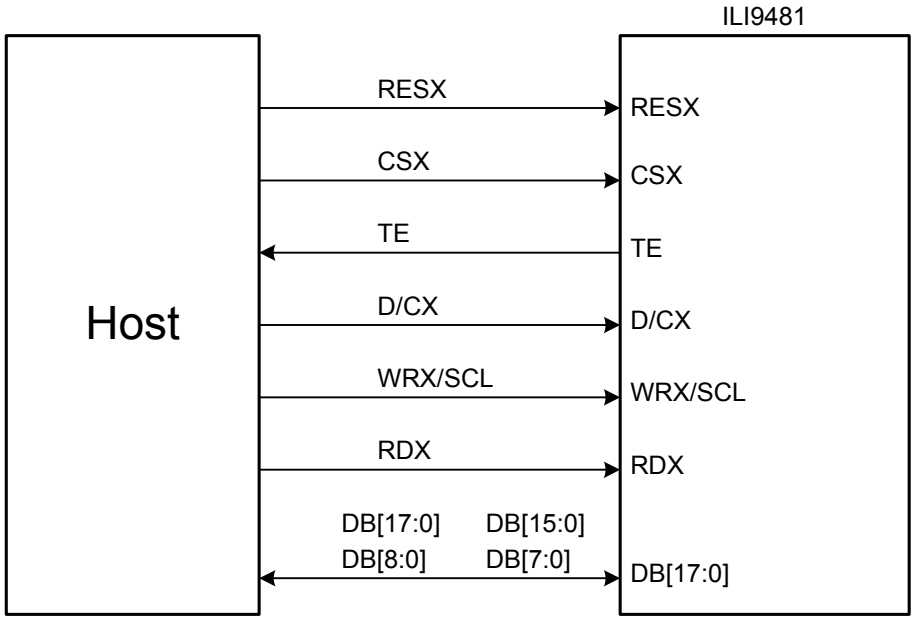
7. Interface Description

7.1. Display Bus Interface (DBI)

The ILI9327 uses a 22-wires 18-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and D[17:0] is parallel DBI data. The four 18/16/9/8-bit types interface is supported for the display data transfer.

The graphics controller chip reads the data at the rising edge of RDX signal. The D/CX is data/command flag. When D/CX = "1", D17 to D0 bits are display RAM data or command parameters. When D/CX = "0"

D7 to D0 bits are commands.



DBI Type B Interface

18-bit data bus DB[17:0] interface, IM[2:0] = 000

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit data bus DB[15:0] interface, IM[2:0] = 010

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

			First Transfer				Second Transfer				Third Transfer			
	Set_pixel_format	DFM	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
18bpp Frame Memory Write	3'h6	0	R1[5:0]		G1[5:0]		B1[5:0]		R2[5:0]		G2[5:0]		b2[5:0]	
		1			R1[5:0]		G1[5:0]		B1[5:0]				R2[5:0]	

			First Transfer				Second Transfer				Third Transfer			
	Set_pixel_format	DFM	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
Frame Memory Read	*	0	r1[5:0]		g1[5:0]		b1[5:0]		r2[5:0]		g2[5:0]		b2[5:0]	
		1			r1[5:0]		g1[5:0]		b1[5:0]				r2[5:0]	

9-bit data bus DB[8:0] interface, IM[2:0] = 001

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

			First Transfer								Second Transfer							
	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

9-bit data bus DB[8:0] interface, IM[2:0] = 110

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	
Command/Parameter Read	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	

			First Transfer								Second Transfer							
	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

8-bit data bus DB[7:0] interface, IM[2:0] = 011

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

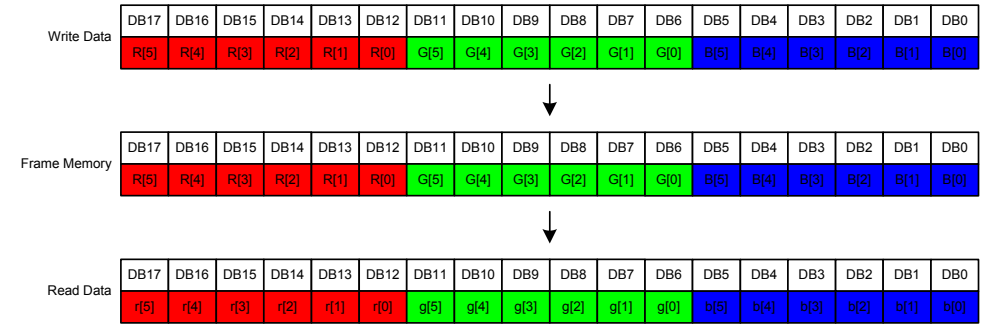
			First Transfer								Second Transfer							
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

			First Transfer								Second Transfer								Third Transfer							
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

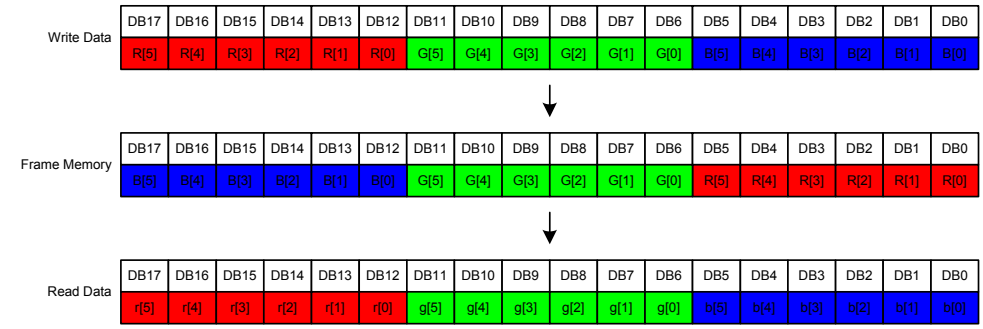
16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

BGR=0



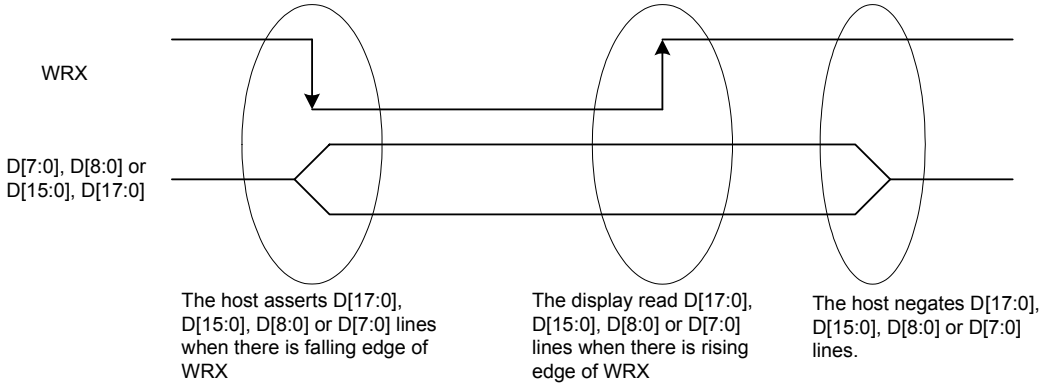
BGR=1

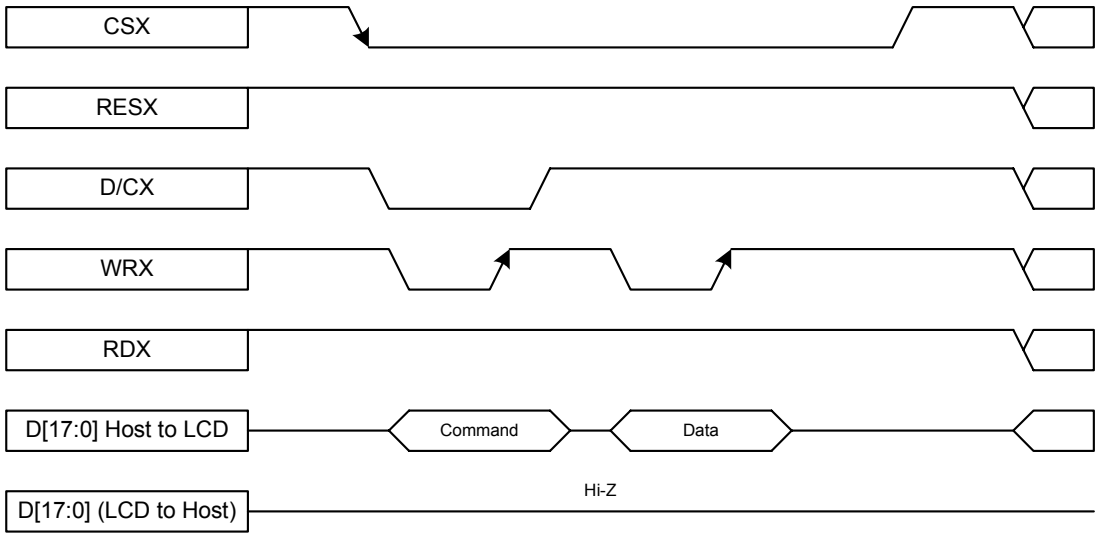


7.1.1. Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The following figure shows a write cycle for the type B interface.

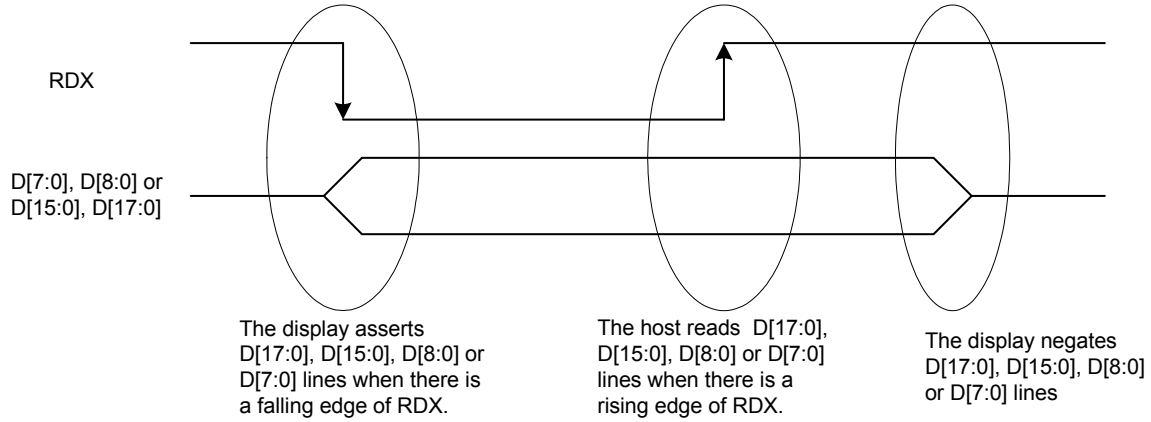




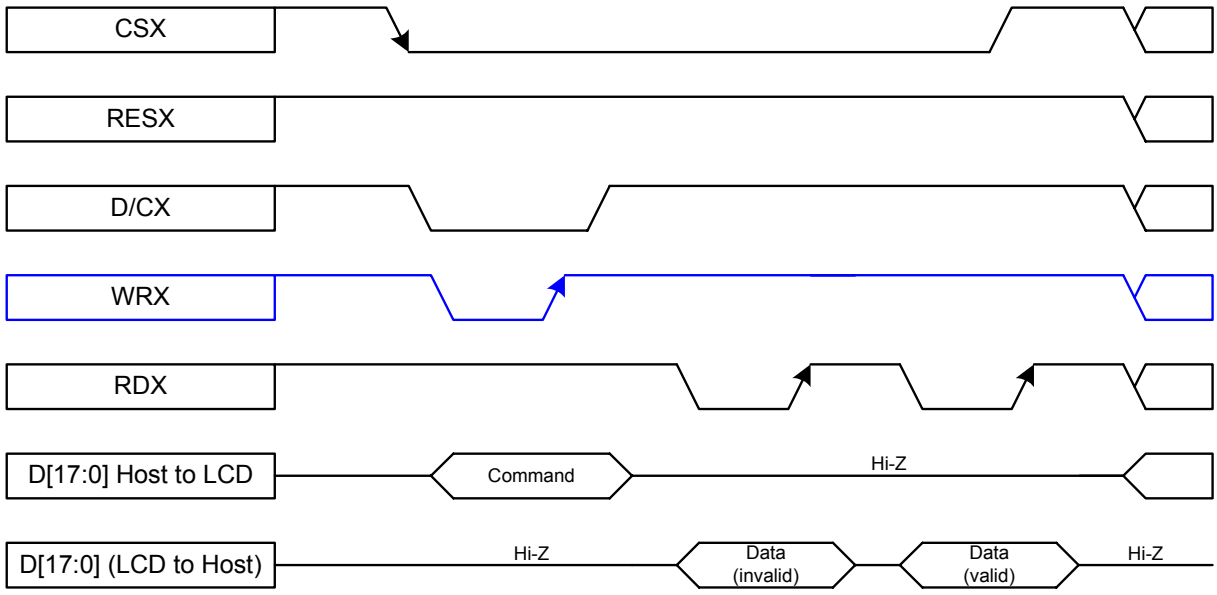
7.1.2. Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. D/CX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



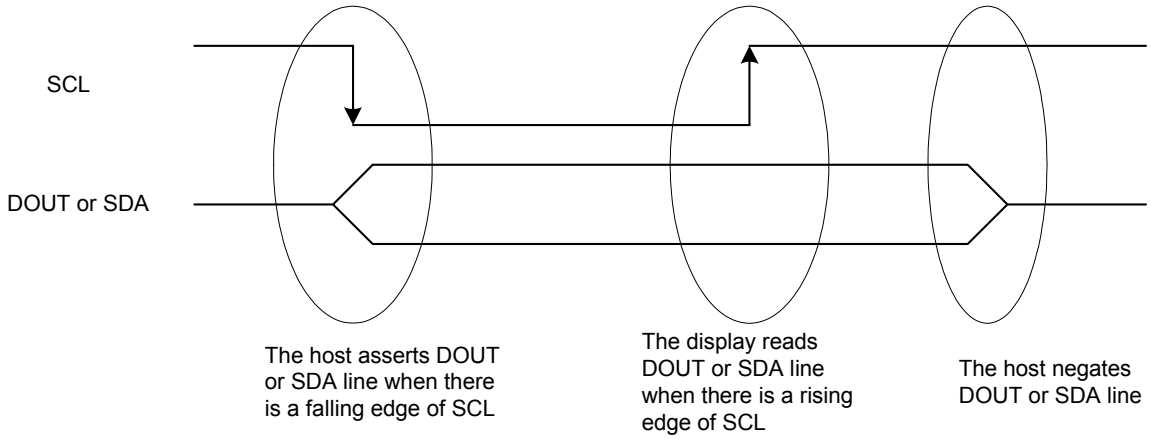
Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.2. Serial Interface (Type C)

7.2.1. Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

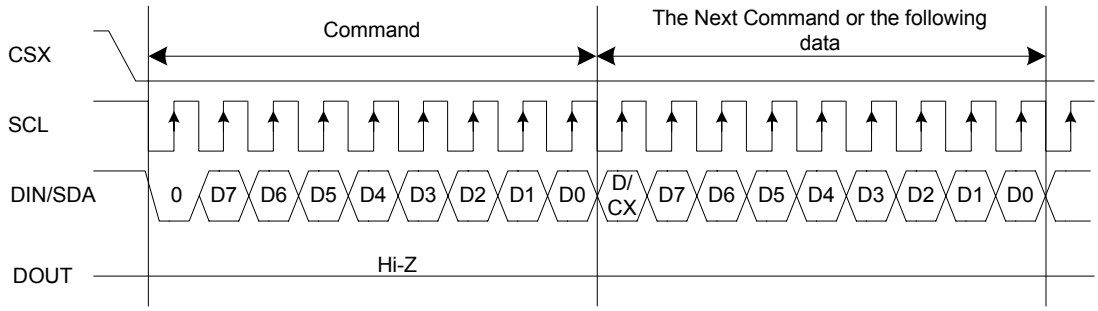
The following figure shows the write cycle for the type C interface.



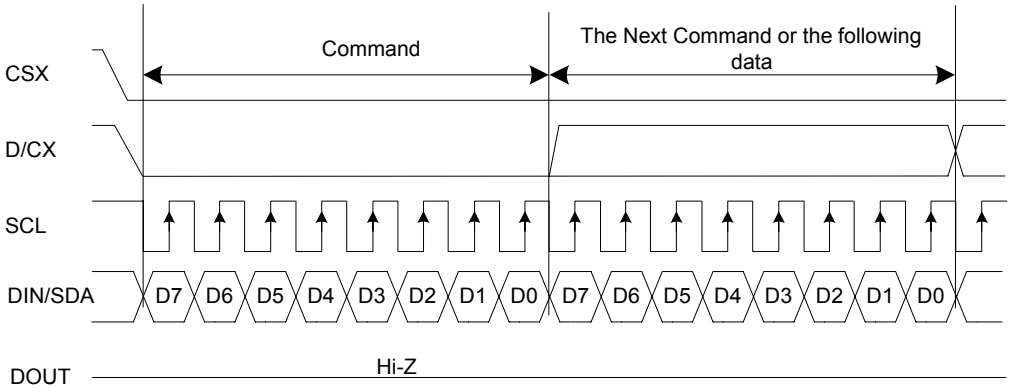
Note: SCL is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface write sequences are described in the following Figure



DBI Type C Interface Write Sequence – Option 1



DBI Type C Interface Write Sequence – Option 3

Note:

1. D7 is MSB and D0 is LSB of byte.
2. When the Interface control register (C6h) SDA_EN is set as '1', the DIN/SDA pin is bi-direction and DOUT pin is not used.
3. When the Interface control register (C6h) SDA_EN is set as '0', the DIN/SDA pin is uni-direction and DIN and DOUT pins are used for data write and read.

DBI Type C Interface IM[2:0]=101/111

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3bpp Frame Memory Write	3'h1	0			R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]			R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]			R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]
	3'h1	1		R1[0]	G1[0]	B1[0]		R2[0]	G2[0]	B2[0]		R3[0]	G3[0]	B3[0]		R4[0]	G4[0]	B4[0]		R5[0]	G5[0]	B5[0]		R6[0]	G6[0]	B6[0]
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	R[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

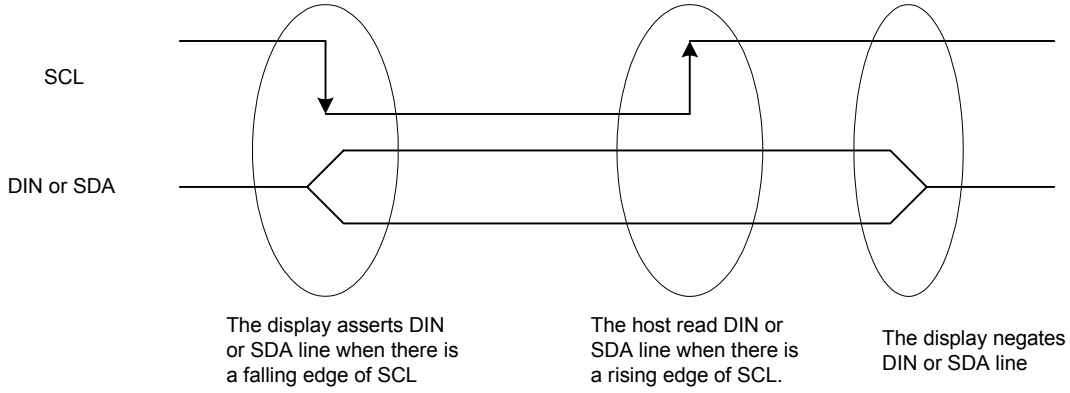
3/16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
3bpp	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]

7.2.2. Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The Type C interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL. D/CX is driven during the read cycle if it is used in option 3.

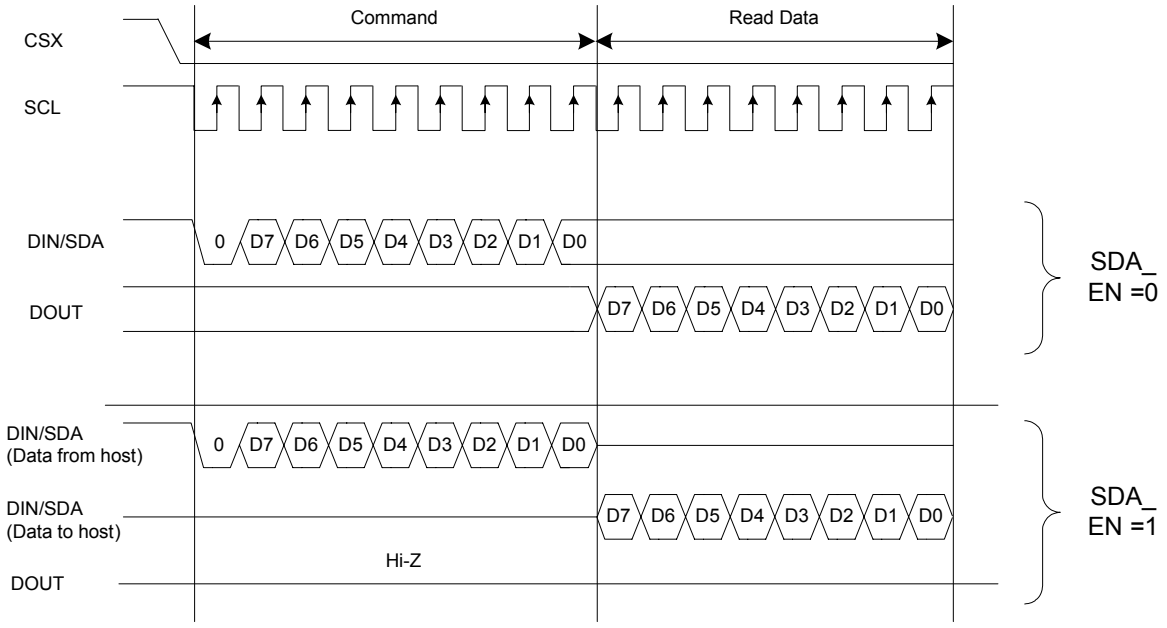
The following figure shows the read cycle for the type C interface.



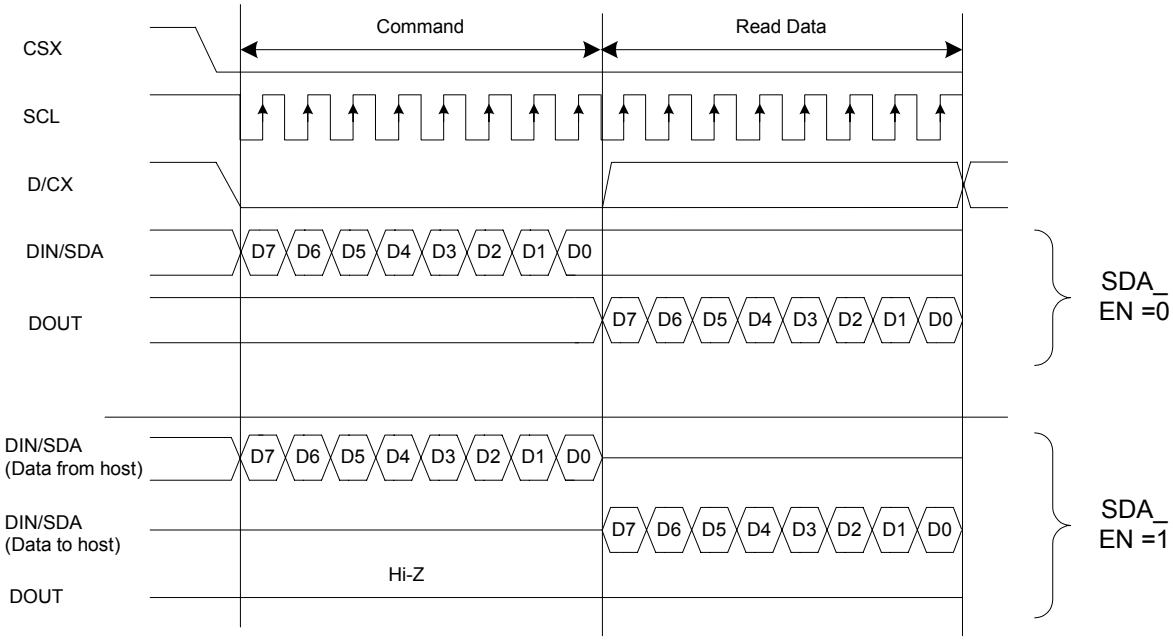
Note: SCL is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface read sequences are shown in the following figures



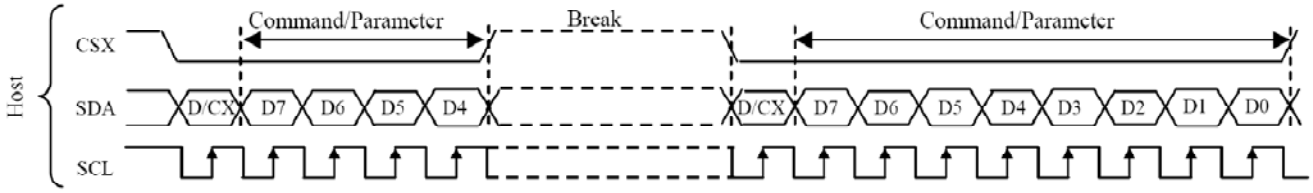
Note: D7 is MSB and D0 is LSB of byte.



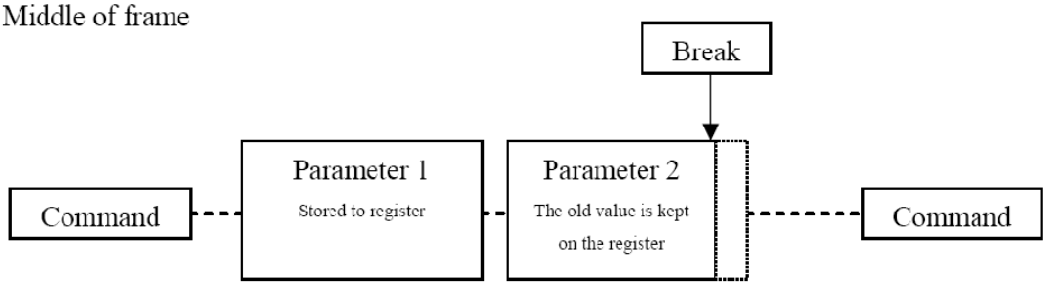
7.2.3. Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

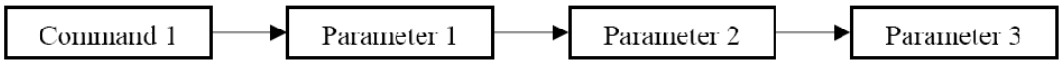


1. Middle of frame

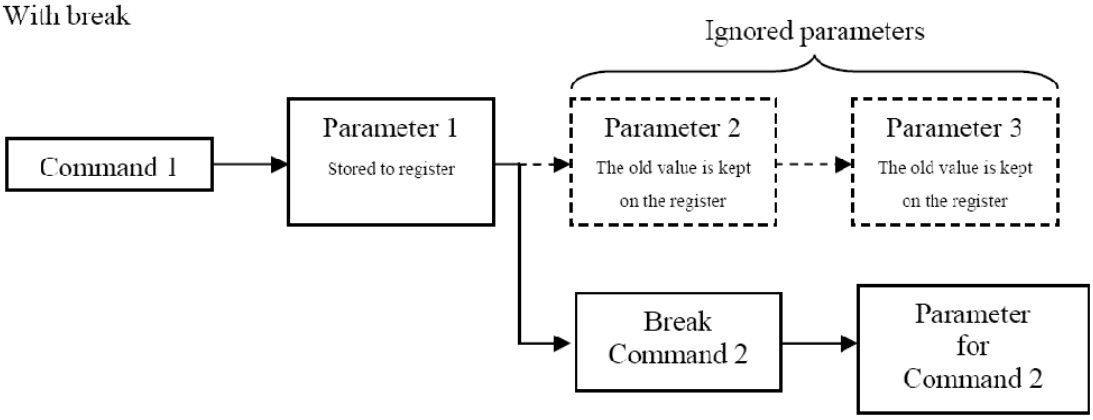


2. Between frames

Without break



With break



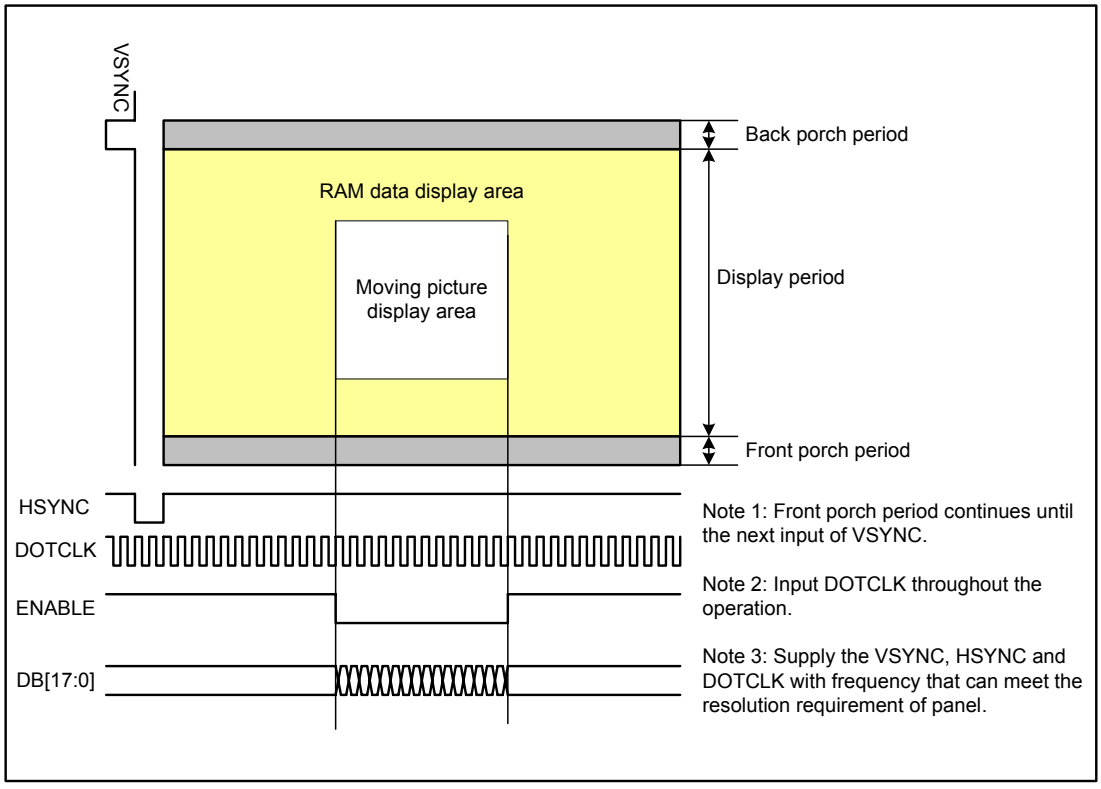
Break can be e.g. another command or noise pulse.

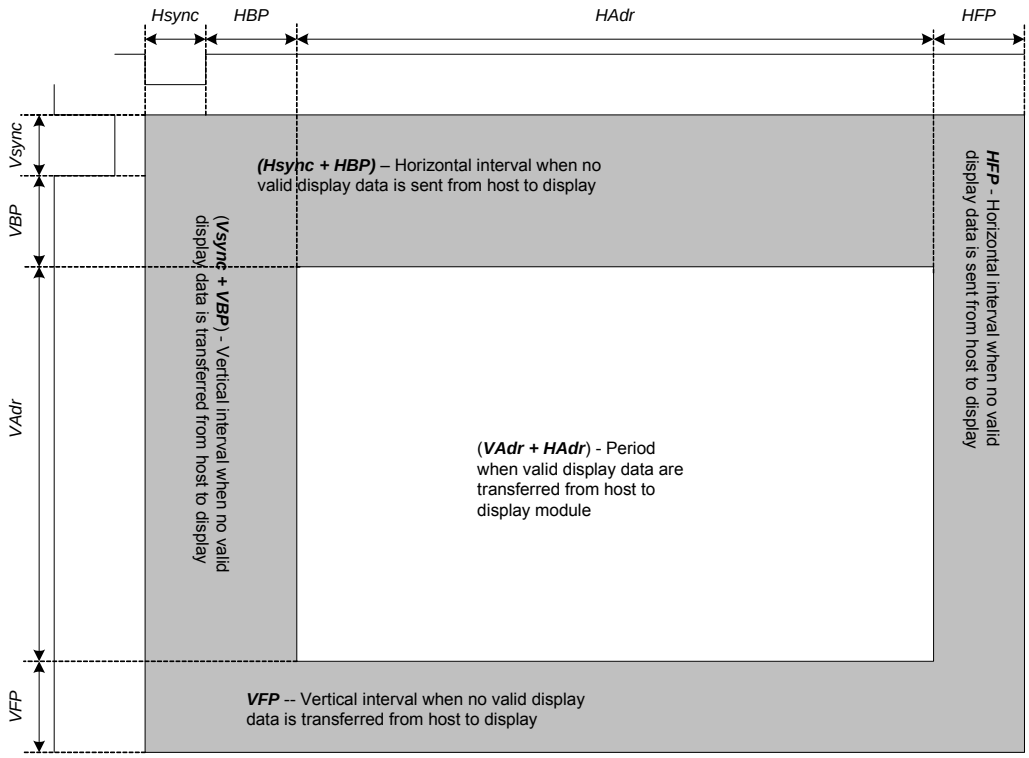
7.3. **Display Pixel Interface (DPI)**

In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image.
Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16 or 18-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.



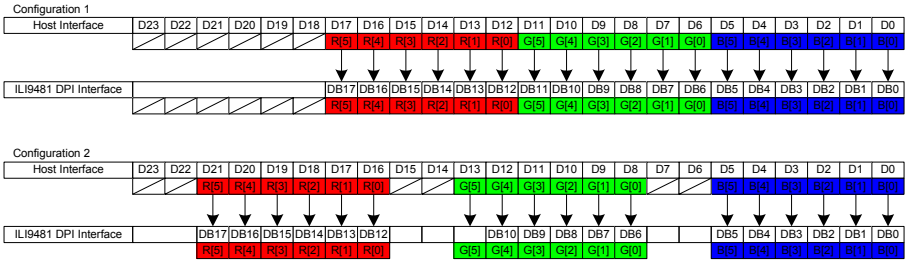


Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
PCLK Cycle	$PCLK_{CYC}$		-	88	-	ns
Horizontal Synchronization	Hsync		-	10	-	PCLK
Horizontal Back Porch	HBP		-	20	-	PCLK
Horizontal Address	HAdr		-	320	-	PCLK
Horizontal Front Porch	HFP		-	10	-	PCLK
Vertical Synchronization	Vsync		-	2	-	Line
Vertical Back Porch	VBP		-	2	-	Line
Vertical Address	VAdr		-	432	-	Line
Vertical Front Porch	VFP		-	4	-	Line
Vsync setup time	VSST				-	Hz
Vsync hold time	VSHT				-	Hz
Hsync setup time	HSST				-	Hz
Hsync hold time	HSHT				-	Hz
Data setup time	DST				-	Hz
Data hold time	DHT				-	Hz
Vertical Frequency(*)				60	-	Hz
Horizontal Frequency(*)			-	29.282	-	KHz
PCLK Frequency(*)			-	11.42Mhz	TBD	MHz

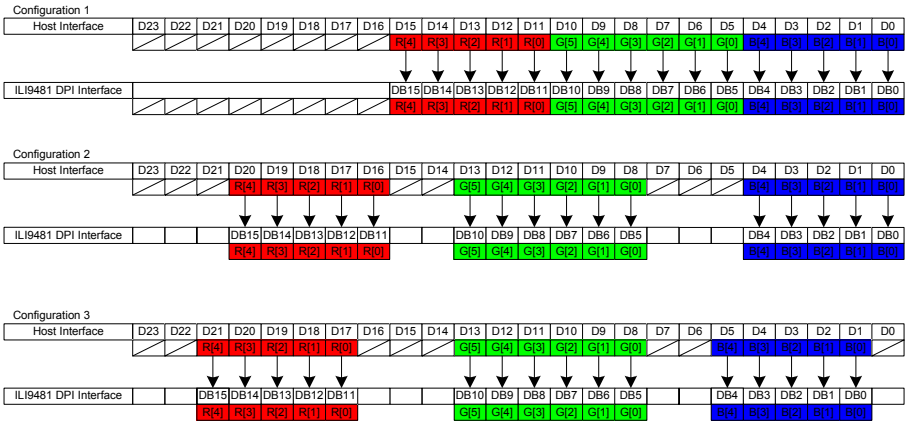
Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

18bit DPI Interface Connection: set_pixel_format D[6:4]=3'h6：18bpp



16bit DPI Interface Connection: set_pixel_format D[6:4]=3'h5：16bpp



16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]
	2'h3	R[4]	R[3]	R[2]	R[1]	R[0]	G[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	G[0]

7.4. Mobile Display Digital Interface (MDDI)

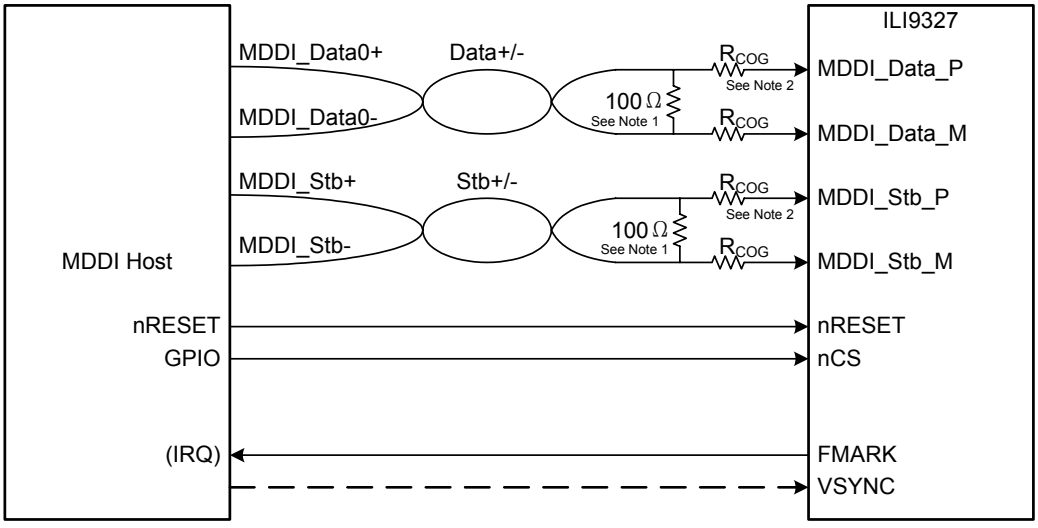
MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/- (MDDI_STBP_B, MDDI_STB_M_B), Data+/- (MDDI_DATA_P_B, MDDI_DATA_M_B).

The specifications of MDDI supported by the ILI9327 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ILI9327's MDDI.

ILI9327 MDDI Specifications

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data+/- lines
- MDDI client: the ILI9327 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems
    1. Only internal mode (one client) and Forward Link are supported
    2. Hibernation mode to save power consumption
    3. Tearing-free moving picture display via FMARK/VSYNC interface
    4. Moving picture display with low power consumption, realized by the features 2 ~ 3
    5. Shutdown mode for saving power consumption in the standby state

Incorporates an output port for sub-display interface or peripheral control providing single-chip solution for MDDI mobile display systems



Notes:

1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines
2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible (RCOG < 10 ohm).

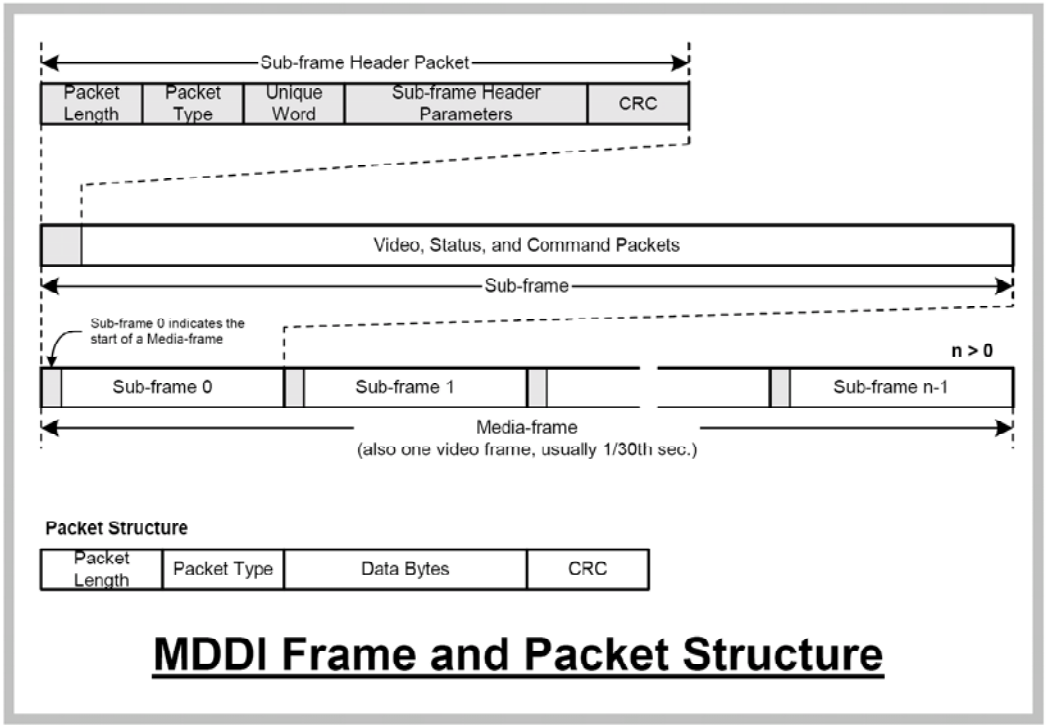
MDDI Link Protocol (Packets Supported by the ILI9327)

The MDDI Link Protocol of the ILI9327 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ILI9327 are as follows. Do not send packets not supported by the ILI9327 in the system incorporating the ILI9327.

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame and some sub-frame construct media-frame together. The following table describes 9 types of packet which is supported in ILI9327.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward



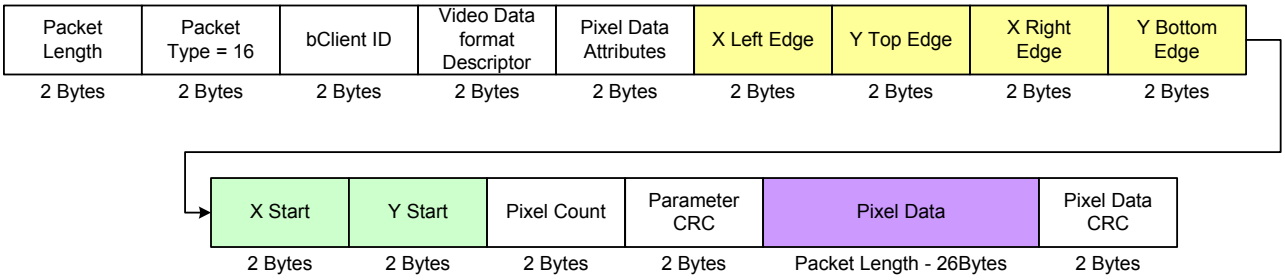
MDDI Frame and Packet Structure

Sub-Frame Header Packet

Bytes	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0x0014)							
3	Packet Type							
4	(0x3bFF)							
5	Unique Word							
6	(0x005A)							
7	Reserved 1							
8	(0x0000)							
9	Sub-Frame Length							
10								
11								
12								
13	Protocol Version							
14	(0x0000)							
15	Sub-frame Count							
16								
17	Media-frame Count							
18								
19								
20								
21	CRC							
22	(0x0000)							

Video Stream Packet

The ILI9327 writes image data to RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.



	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0010)							
5	bClient ID							
6	(0x0000)							
7	Video Data Format Descriptor							
8								
9	Bit0	Bit1	Pixel Data Attributes					
10								
11	X Left Edge							
12								
13	Y Top Edge							
14								
15	X Right Edge							
16								
17	Y Bottom Edge							
18								
19	X Start							
20								
21	Y Start							
22								
23	Pixel Count							
24								
25	Parameter CRC							
26								
	Pixel Data (Packet Length - 26 bytes)							
	CRC							

Note: The parameters colored in gray are not supported by the ILI9327.

Video Data Format Descriptor: sets the pixel data format. The ILI9327 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B=5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B=6:6:6)
Others					Setting disabled

	MDDI Bytes n								MDDI Bytes (n+1)								MDDI Bytes (n+2)							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet 16bpp	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
	Pixel 1 Blue					Pixel 1 Green						Pixel 1 Red					Pixel 2 Blue					Pixel 2		
Packet 18bpp	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	Pixel 2 Blue						Pixel 2 Green						Pixel 2 Red				Pixel 2 Blue							

Pixel Data Attributes: the image data sent vial Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Pixel Data Attributes	Bits[1:0]	Description
0x0000	**00**	**The Video Stream Packet data is recognized as the sub-panel data. The Video Stream Packet data is outputted via sub-display interface and not written in the ILI9327.**
0x0001	01	Setting disabled
0x0002	10	Setting disabled
0x0003	11	The Video Stream Packet data is recognized as the data written in the ILI9327. The Video Stream Packet data is written in the ILI9327 and not outputted via sub-display interface.
Others		

Register Access Packet

Register Access Packet is used when setting instruction to the ILI9327.

	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0092)							
5	bClient ID							
6	(0x0000)							
7	Read/Write Info.							
8								
9	Register Address							
10								
11								
12								
13	Parameter CRC							
14								
	Register Data (Packet Length - 14 bytes)							
	Register Dara CRC							

Note: The parameters colored in gray are not supported by the ILI9327.

Read/Write Info: Read or Write information in register access. The ILI9327 supports the following access setting.

Bits[15:14]	Bits[13:00]	Description
2'b00	0xn	Write one register by register access packet
2'b10	0xn	Read one register by register access packet
others		Setting disabled

Register Address: The index of the register to be accessed is set in Register Address area and the Register Address Packet is directed to the ILI9327 or the sub display is determined by the setting in Register Address area.

Bits[31:16]	Description
16'h0000	The Register Access Packet is directed to the ILI9327 via main-display interface.
16'h0001	The Register Access Packet is directed to the sub display via sub-display interface.
16'h0002 ~ 16'h7FFF	Setting disabled

Bits[15:0]	Description
16'h0000~FFFF	Bits [15:0] are used as index [15:0].

Register Data: The data for register access is written in Register Data. The length of Register Data will depends on the parameter length of command.

Example of Register Access Packet (e.g. write to the ILI9327)

	0	1	2	3	4	5	6	7
1	Packet Length					(0x12)		
2						(0x00)		
3	Packet Type					(0x92)		
4						(0x00)		
5	bClient ID					(0x00)		
6						(0x00)		
7	Read/Write Info.					(0x01)		
8						(0x00)		
9	Register Address					(index ID[7:0])		
10						(index ID[15:8])		
11						(0x00) → Main Panel (ILI9327) (0x01) → Sub panel		
12						(0x00)		
13	Parameter CRC							
14								
15	Register Data List (Various Length)					1st Parameter		
16						2nd Parameter		
17						3rd Parameter		
18						0x00		
19	Parameter CRC							
20								

Note: The parameters colored in gray are not supported by the ILI9327.

Register Access Packet Restrictions

The ILI9327's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.

	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0X0014)							
3	Packet Type							
4	(0x0045)							
5	Parameter CRC							
6								
7	All Zeros (Type-I: 16 bytes)							
22								

Note: The parameters colored in gray are not supported by the ILI9327.

Filler Packet

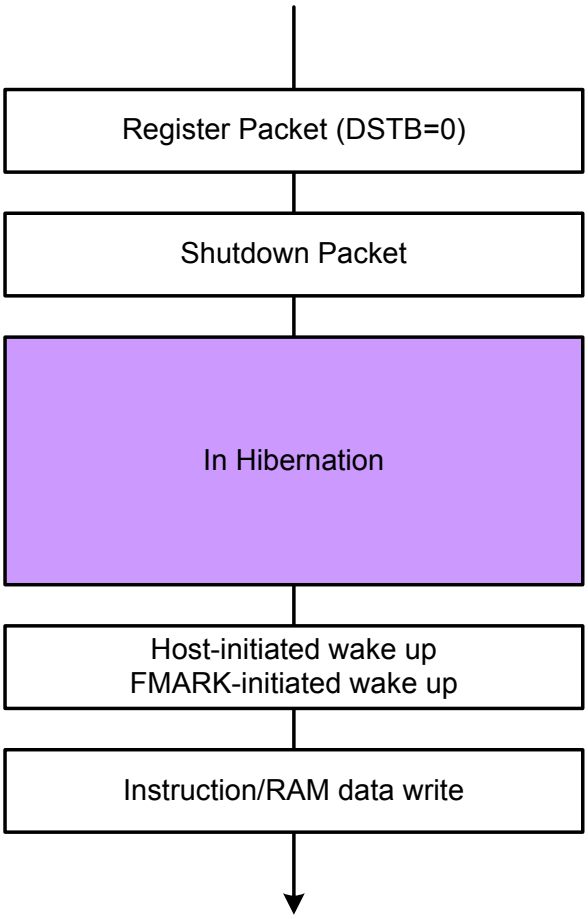
	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0000)							
	Filler bytes (all zeros) (Packet Length: 4 bytes)							
	CRC							

Hibernation Setting

The ILI9327's Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

Hibernation Cancellation	
Host-initiated wake up	In power-saving mode such as standby
FMARK-initiated wake up	Save power consumption in transferring moving picture data Host-initiated wake up triggered by the output from FMARK.

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.

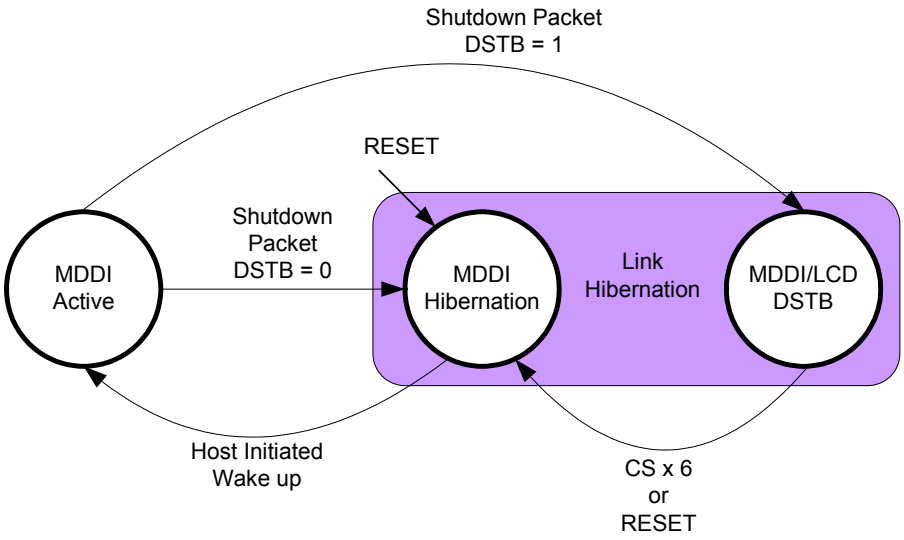


Deep Standby Mode Setting

The ILI9327's Client MDDI supports shutdown setting to bring ILI9327 to the deep standby state to save power consumption.

ILI9327 can enter into deep standby mode to save power consumption. In canceling deep standby mode, input Low pulse 6 times from CS pin or reset ILI9327. After canceling deep standby mode, cancel the Hibernation state by Host-initiated Wake up. In deep standby mode, regsiter setting and RAM data are not retained and they must be reset after canceling the Hibernation state.

When setting and canceling the Hibernation state, follow the sequence as specified in the MDDI specifications by VESA.



8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	ILI9418 Implementation
00h	nop	C	0	Yes	Yes
01h	soft_reset	C	0	Yes	Yes
06h	get_red_channel	R	1	No	No
07h	get_green_channel	R	1	No	No
08h	get_blue_channel	R	1	No	No
0Ah	get_power_mode	R	1	Yes	Yes
0Bh	get_address_mode	R	1	Yes (Bit[7:0])	Yes (Bit[7:3]) , Only)
0Ch	get_pixel_format	R	1	Yes	Yes
0Dh	get_display_mode	R	1	Yes	Yes
0Eh	get_signal_mode	R	1	Yes	Yes
0Fh	get_diagnostic _result	R	1	Bit7/6：Yes Bit5/4：Optional	Yes (Bit7/6 Only)
10h	enter_sleep_mode	C	0	Yes	Yes
11h	exit_sleep_mode	C	0	Yes	Yes
12h	enter_partial_mode	C	0	Yes	Yes
13h	enter_normal_mode	C	0	Yes	Yes
20h	exit_invert_mode	C	0	Yes	Yes
21h	enter_invert_mode	C	0	Yes	Yes
26h	set_gamma_curve	W	1	Yes	No
28h	set_display_off	C	0	Yes	Yes
29h	set_display_on	C	0	Yes	Yes
2Ah	set_column_address	W	4	Yes	Yes
2Bh	set_page_address	W	4	Yes	Yes
2Ch	write_memory_start	W	Variable	Yes	Yes
2Dh	wite_LUT	W	Variable	Optional	No
2Eh	read_memory_start	R	Variable	Yes	Yes
30h	set_partial_area	W	4	Yes	Yes
33h	set_scroll_area	W	6	Yes	Yes
34h	set_tear_off	C	0	Yes	Yes
35h	set_tear_on	W	1	Yes	Yes
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes (Bit[7:3], Bit[1:0] Only)
37h	set_scroll_start	W	2	Yes	Yes
38h	exit_idle_mode	C	0	Yes	Yes
39h	enter_idle_mode	C	0	Yes	Yes
3Ah	set_pixel_format	W	1	Yes	Yes
3Ch	write_memory _continue	W	Variable	Yes	Yes
3Eh	read_memory _continue	R	Variable	Yes	Yes
44h	set_tear_scanline	W	2	Yes	Yes
45h	get_scanline	R	2	Yes	Yes
A1h	read_DDB_start	R	5	Yes	Yes
A8h	read_DDB_continue	R	Variable	Yes	Yes

Operational Code (Hex)	Function	Command(C) Read(R)/Write(W)	Number Of Parameter
B0h	Command Access Protect	W/R	1
B1h	Low Power Mode Control	W/R	1
B3h	Frame Memory Access and Interface setting	W/R	5
B4h	Display Mode and Frame Memory Write Mode setting	W/R	1
BFh	Device code Read	R	4
C0h	Panel Driving Setting	W/R	7
C1h	Display Timing Setting for Normal Mode	W/R	3
C2h	Display Timing Setting for Partial Mode	W/R	3
C3h	Display Timing Setting for Idle Mode	W/R	3
C5h	Frame rate and Inversion Control	W/R	1
C6h	Interface Control	W/R	1
C8h	Gamma Setting	W/R	12
D0h	Power Setting	W/R	3
D1h	VCOM Control	W/R	3
D2h	Power Setting for Normal Mode	W/R	2
D3h	Power Setting for Partial Mode	W/R	2
D4h	Power Setting for Idle Mode	W/R	2
E0h	NV Memory Write	W/R	1
E1h	NV Memory Control	W/R	1
E2h	NV Memory Status	W/R	3
E3h	NV Memory Protection	W/R	2
B0～FF Except above command	LSI TEST Registers	W/R	Variable

8.2. Command Description

8.2.1. NOP (00h)

00H	NOP (No Operation)												
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart	None

8.2.2. Soft_reset (01h)

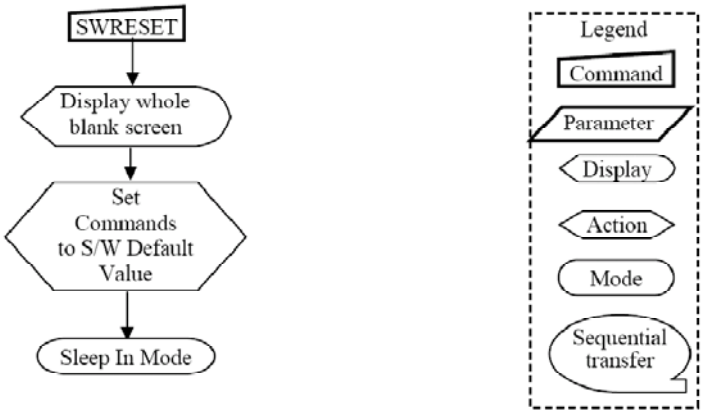
01H	Soft_reset												
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are affected by this command. X = Don't care												
Restriction	Software Reset Command cannot be sent during Sleep Out sequence. Any new command is cannot be sent for 10-frame period until the ILI9327 enters Sleep-In mode. Do not send any command.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



8.2.3. Get_power_mode (0Ah)

0AH	Get_power_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	Set to '0'
D6	Idle Mode On/Off	
D5	Partial Mode On/Off	
D4	Sleep In/Out	
D3	Display Normal Mode On/Off	
D2	Display On/Off	
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 – Booster Voltage Status

'0' = Booster Off or has a fault.

'1' = Booster On and working OK (Meets Nokia's optical requirements).

Bit D6 - Idle Mode On/Off

'0' = Idle Mode Off.

'1' = Idle Mode On.

Bit D5 – Partial Mode On/Off

'0' = Partial Mode Off.

'1' = Partial Mode On.

Bit D4 – Sleep In/Out

'0' = Sleep In Mode.

'1' = Sleep Out Mode.

Bit D3 – Display Normal Mode On/Off

'0' = Display Normal Mode Off.

'1' = Display Normal Mode On.

Bit D2 – Display On/Off

'0' = Display is Off.

'1' = Display is On.

Bit D1 – Not Defined

'This bit is not applicable for this project, so it is set to '0'

Bit D0 – Not Defined

'This bit is not applicable for this project, so it is set to '0'

X = Don't care

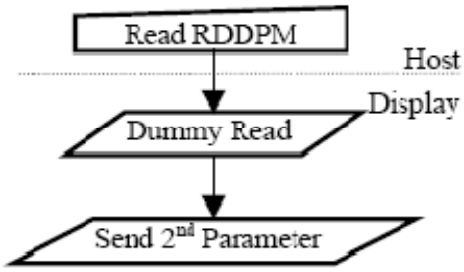
Register Availability

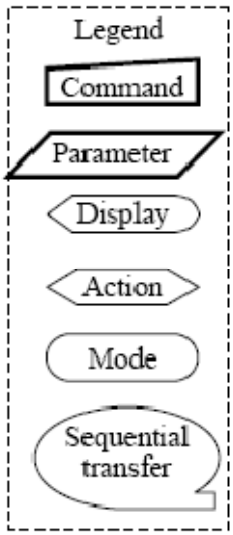
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08_{HEX}
SW Reset	08_{HEX}
HW Reset	08_{HEX}

Flow Chart





8.2.4. Get_address_mode (0Bh)

0BH	Get_address_mode												
	D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0B
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	Reserved	Set to '0'
D1	Reserved	Set to '0'
D0	Reserved	Set to '0'

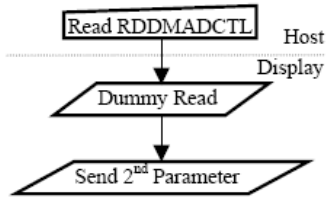
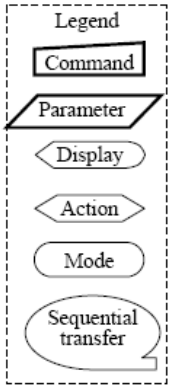
- Bit D7 – Page Address Order
  '0' = Top to Bottom
  '1' = Bottom to Top
- Bit D6 – Column Address Order
  '0' = Left to Right
  '1' = Right to Left
- Bit D5 - Page/Column Order
  '0' = Normal Mode
  '1' = Reverse Mode
  Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to memory write/read direction.
- Bit D4 – Line Address Order
  '0' = LCD Refresh Top to Bottom
  '1' = LCD Refresh Bottom to Top
- Bit D3 – RGB/BGR Order
  '0' = RGB
  '1' = BGR

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	No change
HW Reset	00_{HEX}

Flow Chart	 

8.2.5. Get_pixel_format (0Ch)

0CH	Get_pixel_format												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	0	D6	D5	D4	0	D2	D1	D0	66

Description

This command indicates the current status of the display as described in the table below:

Bit	Description
D7	DPI Pixel Format (RGB Interface Color Format)
D6	
D5	
D4	
D3	DBI Pixel Format (Control Interface Color Format)
D2	
D1	
D0	

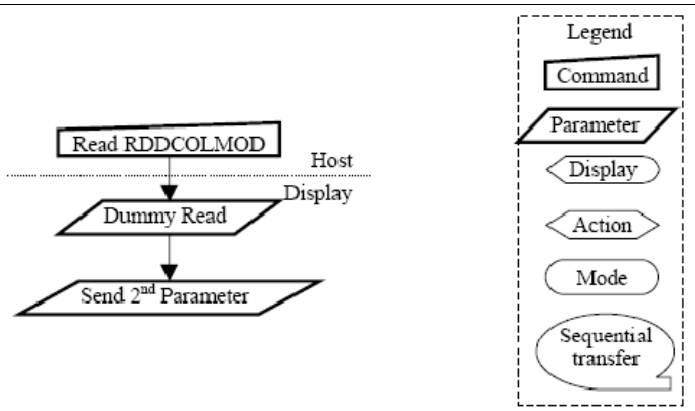
Pixel Format	D6/D2	D5/D1	D4/D0
Reserved	0	0	0
3 bits / pixel	0	0	1
Reserved	0	1	0
Reserved	0	1	1
Reserved	1	0	0
16 bits / pixel	1	0	1
18 bits / pixel	1	1	0
Reserved	1	1	1

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default value

Status	Default Value
Power On Sequence	66_{HEX}
SW Reset	66_{HEX}
HW Reset	66_{HEX}

Flow Chart	

8.2.6. Get_display_mode (0Dh)

0DH	Get_display_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	0	0	0	0	0	0	0	0	00

Description

The display module returns the Display Image Mode status.

Bit	Description	Symbol
D7	Vertical Scrolling Status	VSSON
D6	Reserved	
D5	Inversion On/Off	DSPINVON
D4	Reserved	
D3	Reserved	
D2	Gamma Curve Selection	
D1	Gamma Curve Selection	
D0	Gamma Curve Selection	

This command indicates the current status of the display as described in the table below:

- Bit D7 – Vertical Scrolling On/Off

  '0' = Vertical Scrolling is Off.

  '1' = Vertical Scrolling is On.

- Bit D6 – Reserved
- Bit D5 – Inversion On/Off

  '0' = Inversion is Off.

  '1' = Inversion is On.

- Bit D4 – Reserved
- Bit D3 – Reserved
- Bits D2, D1, D0 – Gamma Curve Selection

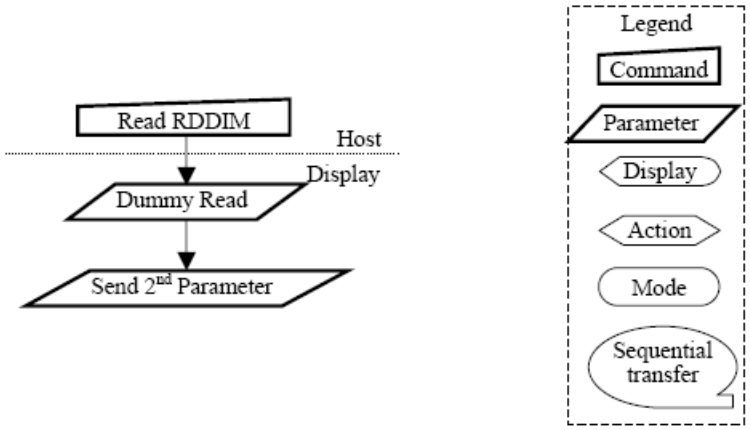
  These bits are not applicable for this project, so they are set to '000'

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart	

8.2.7. Get_signal_mode (0Eh)

0EH	Get_signal_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	00

Description

The display module returns the Display Signal Mode.

Bit	Description	Symbol
D7	Tearing Effect Line On/Off	TEON
D6	Tearing Effect Line Output Mode	TELOM
D5	Reserved	
D4	Reserved	
D3	Reserved	
D2	Reserved	
D1	Reserved	
D0	Reserved	

This command indicates the current status of the display as described in the table below:

- Bit D7 – Tearing Effect Line On/Off
  '0' = Tearing Effect Line Off.
  '1' = Tearing Effect On.
- Bit D6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions.
  '0' = Mode 1.
  '1' = Mode 2.
- Bit D[5:0] – Reserved

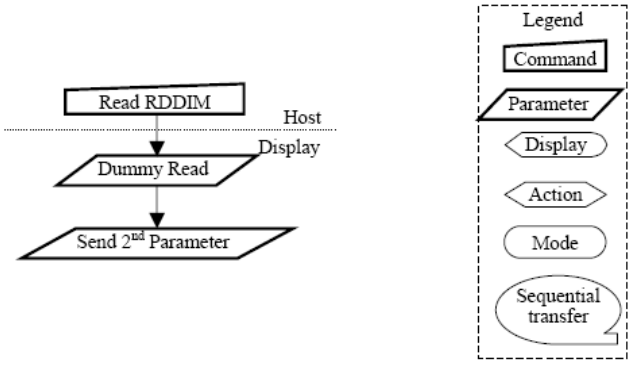
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Register Availability

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



8.2.8. Get_diagnostic_result (0Fh)

0FH	Get_diagnostic_result												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	00

Description

The display module returns the self-diagnostic results following a Sleep Out command.

Bit	Description	Symbol
D7	Register Loading Detection	SDR
D6	Functionality Detection	FUNCD
D5	Chip attachment Detection	Set '0'
D4	Display Glass Break Detection	Set '0'
D3	Reserved	Set '0'
D2	Reserved	Set '0'
D1	Reserved	Set '0'
D0	Reserved	Set '0'

Bit D7 – Register Loading Detection

Bit D6 – Functionality Detection

Bit D5 – Chip Attachment Detection

Set to '0' if feature unimplemented.

Bit D4 – Display Glass Break Detection

Set to '0' if feature unimplemented.

Bits D[3:0] – Reserved

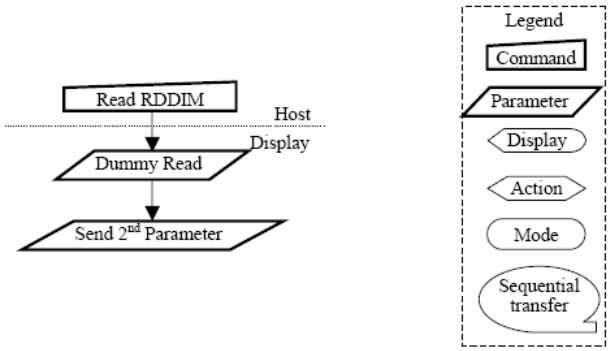
Set to '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Register Availability

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart	

8.2.9. Enter_sleep_mode (10h)

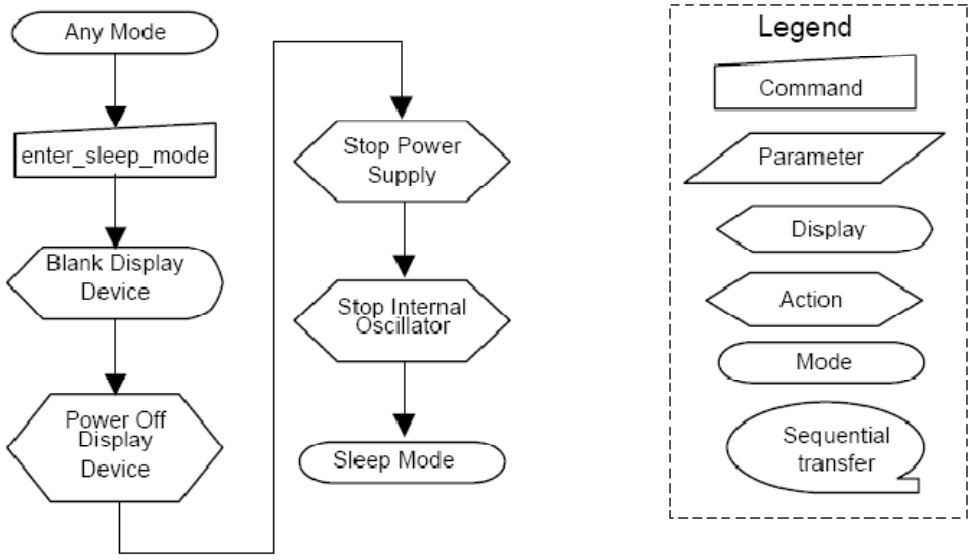
10H	Enter_sleep_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10
Parameter	No Parameter												
Description	This command causes the display module to enter the Sleep mode. This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to Type 2 and Type 3 display modules for two frames after this command is sent when the display module is in Normal mode.												
Restriction	This command has no effect when the display module is already in Sleep mode. The host processor must wait five milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart	

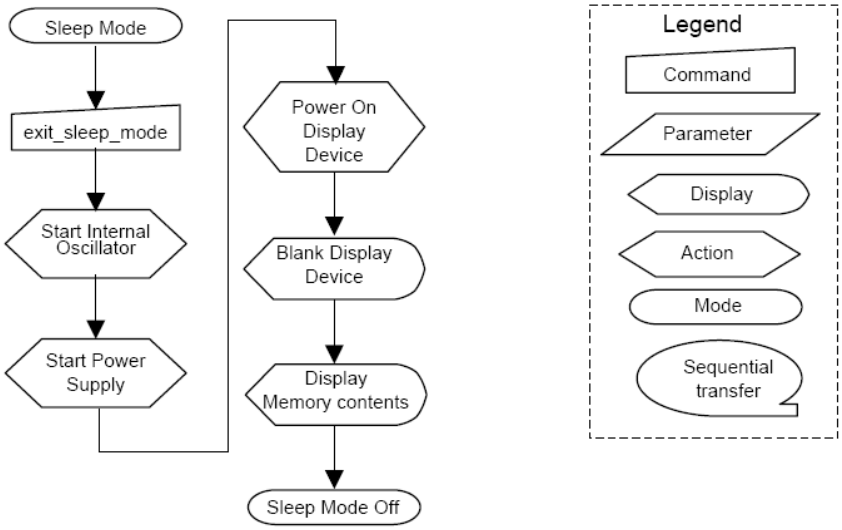
8.2.10. Exit_sleep_mode (11h)

11H	Exit_sleep_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to Type 2 and Type 3 display modules two frames before this command is sent when the display module is in Normal Mode.												
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received. See section 5.3 for a description of the self-diagnostic functions.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart	

8.2.11. Enter_Partial_mode (12h)

<table>
<tr><th>12H</th><th colspan="12">Enter_Partial_mode</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area (30h) command.
To leave Partial Display Mode, the enter_normal_mode (13h) command should be written.
The host processor continues to send PCLK, HS and VS information to Type 2 display modules for two frames after this command is sent when the display module is in Normal Display Mode.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial Display Mode is already active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">Refer to Partial Area (30h)</td></tr>
</table>

8.2.12. Enter_normal_mode (13h)

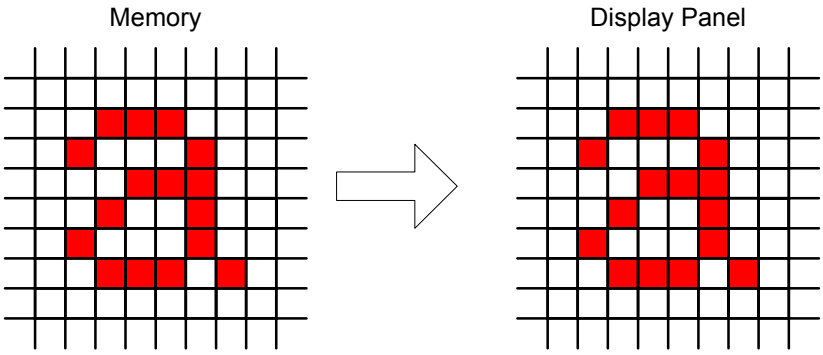
<table>
<tr><th>13H</th><th colspan="13">Enter_normal_mode</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the display module to enter the Normal mode.
Normal Mode is defined as Partial Display mode and Scroll mode are off.
The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is already active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">Refer to the description of set_partial_area(30h) and set_scroll_area(33h)</td></tr>
</table>

8.2.13. Exit_invert_mode (20h)

20H	Exit_invert_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												

Description

This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.



Restriction

This command has no effect when the display module is not inverting the display image.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

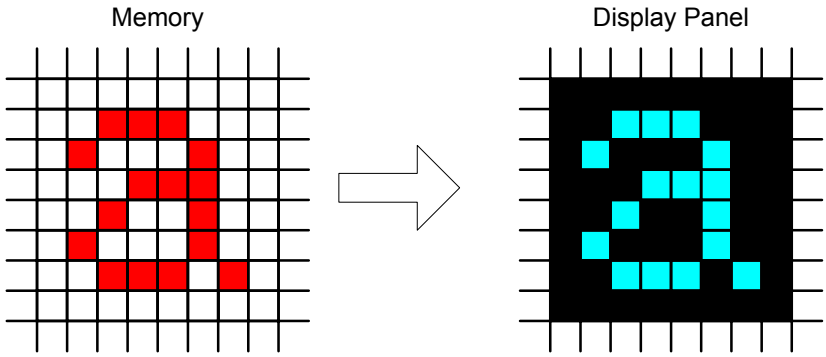
Flow Chart

8.2.14. Enter_invert_mode (21h)

21H	Enter_invert_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												

Description

This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.



Restriction

This command has no effect when module is already in inversion on mode.

Register Availability

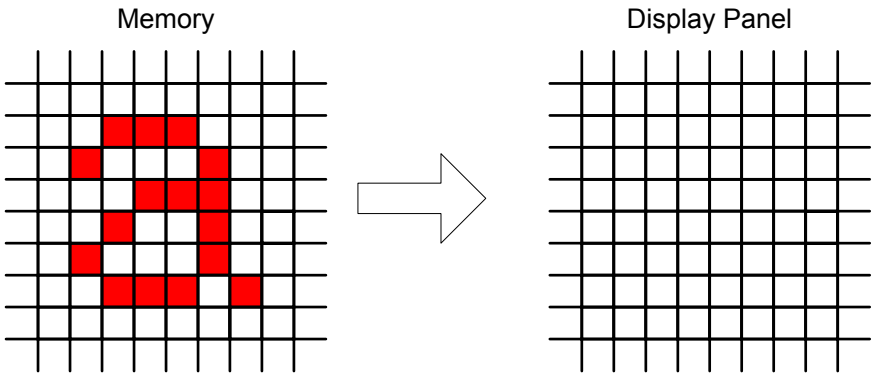
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

Flow Chart

8.2.15. Set_display_off (28h)

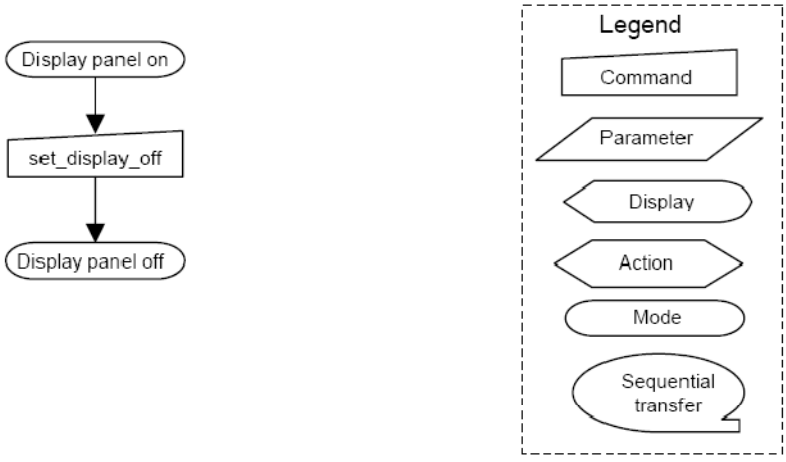
28H	Set_display_off												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in display off mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

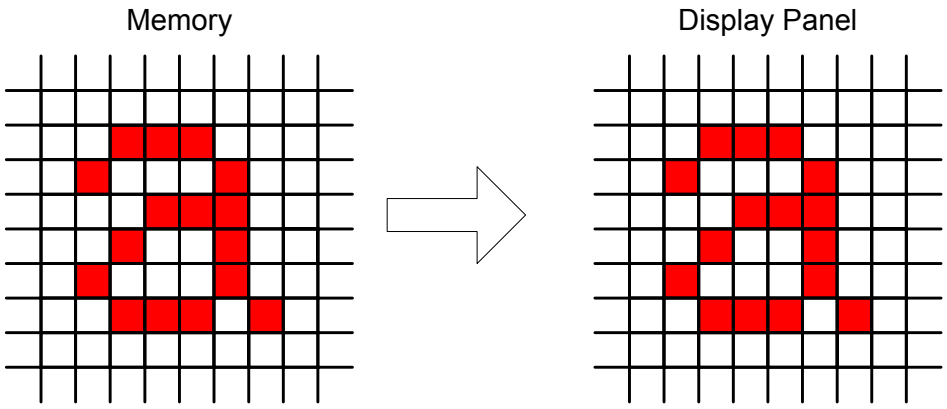
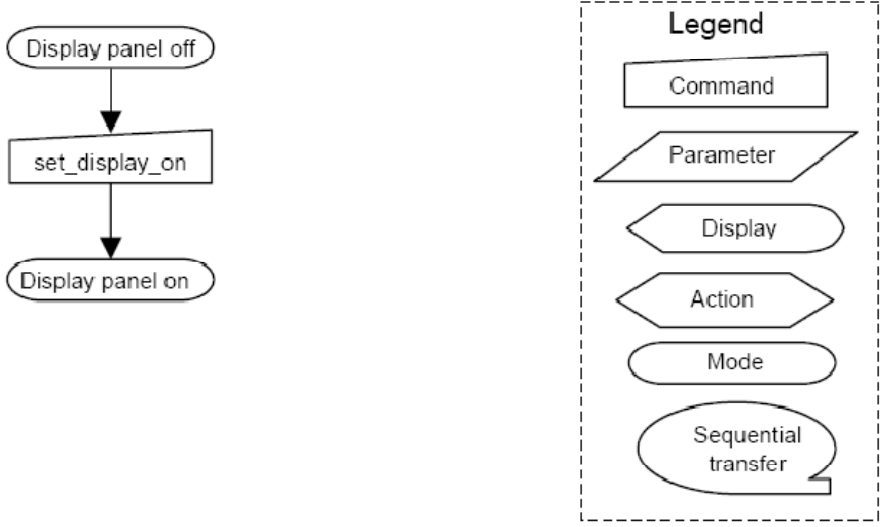
Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart



8.2.16. Set_display_on (29h)

29H	Set_display_on												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												

<table>
<tr><td>Description</td><td>This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.
 
</td></tr>
<tr><td>Restriction</td><td>This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display Off</td></tr>
<tr><td>SW Reset</td><td>Display Off</td></tr>
<tr><td>HW Reset</td><td>Display Off</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

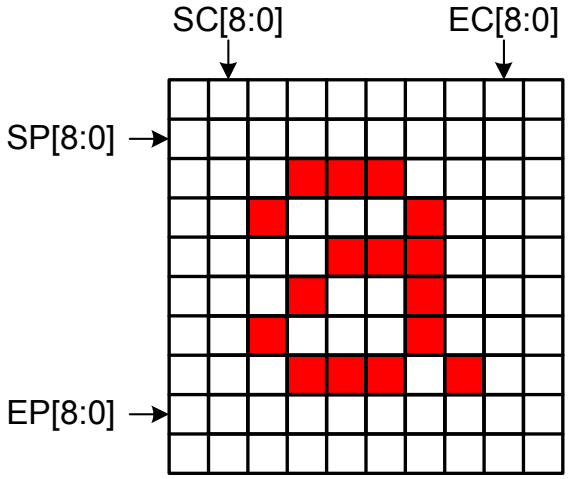
8.2.17. Set_column_address (2Ah)

2AH	Set_column_address												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SC8	Note
2nd Parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	1
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EC8	Note
4th Parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	2

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status.

Each value represents one column line in the Frame Memory.



Restriction

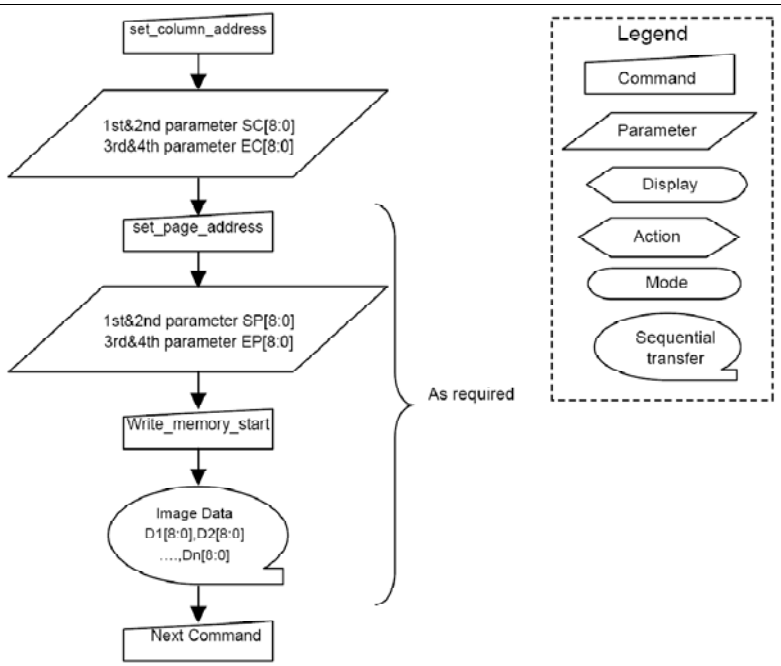
SC [8:0] always must be equal to or less than EC[8:0]. If SC[8:0] or EC[8:0] is greater than the available frame memory then the parameter is not updated.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	$SC[8:0]=0000_{HEX}$	$SE[8:0]=0EF_{HEX}$
SW Reset	$SC[8:0]=0000_{HEX}$	If Set_address_mode(36h) B5=0 : $EC[8:0]=0EF_{HEX}$ If Set_address_mode(36h) B5=1 : $EC[8:0]=1AF_{HEX}$
HW Reset	$SC[8:0]=0000_{HEX}$	$SE[8:0]=0EF_{HEX}$

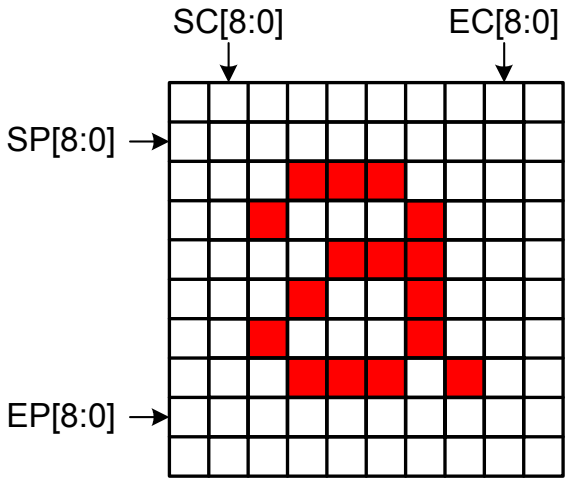
Flow Chart	

8.2.18. Set_page_address (2Bh)

2BH	Set_page_address												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SP8	xxx
2nd Parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EP8	xxx
4th Parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. No status bits are changed.



Restriction

SP [8:0] always must be equal to or less than EP [8:0].

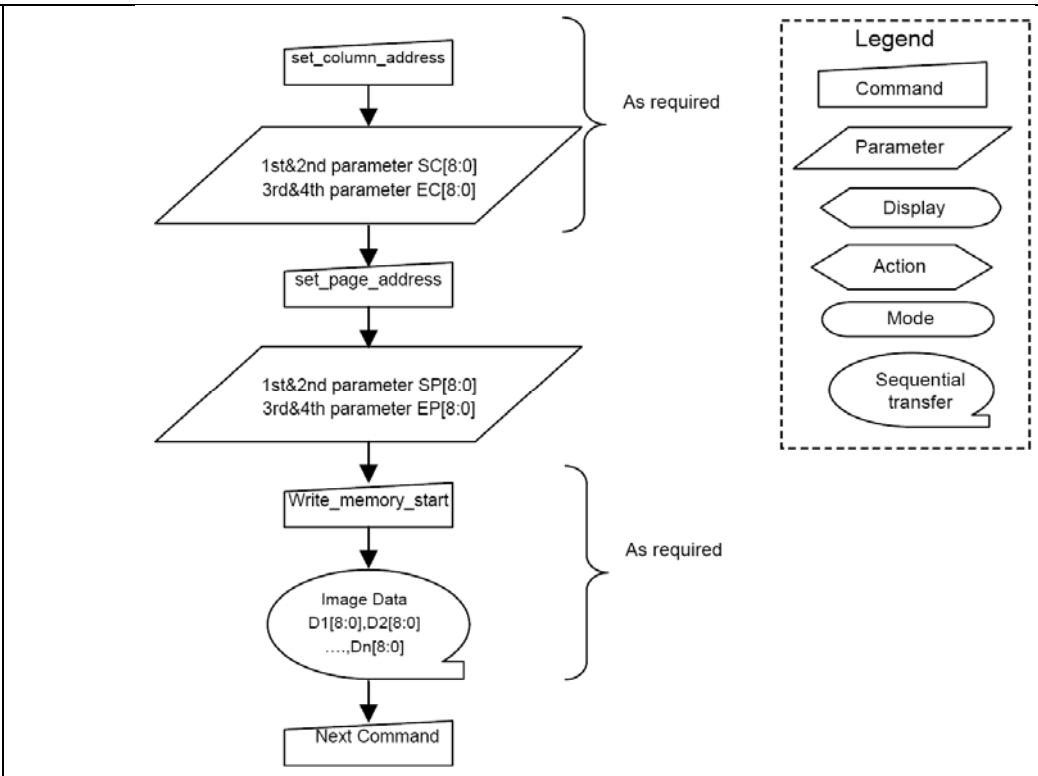
If SP[8:0] or EP[8:0] is greater than the available frame memory then the parameter is not updated.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[8:0]=0000_{HEX}	EP[8:0]=$1AF_{HEX}$
SW Reset	SP[8:0]=0000_{HEX}	If Set_address_mode(36h) B5=0 : EP[8:0]=$1AF_{HEX}$ If Set_address_mode(36h) B5=1 : EP[8:0]=$0EF_{HEX}$
HW Reset	SP8:0]=0000_{HEX}	EP[8:0]=$1AF_{HEX}$

Flow Chart	

8.2.19. Write_memory_start (2Ch)

2CH	Write_memory_start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C
1st pixel data	1	1	↑	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FFF
:	1	1	↑	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FFF
NTH pixel data	1	1	↑	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FFF

Description

This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address (2Ah) and set_page_address (2Bh) commands.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.

If set_address_mode (36h) B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode (36h) B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write location. Otherwise, data written with write_memory_start and any following write_memory_continue commands is written to undefined locations..

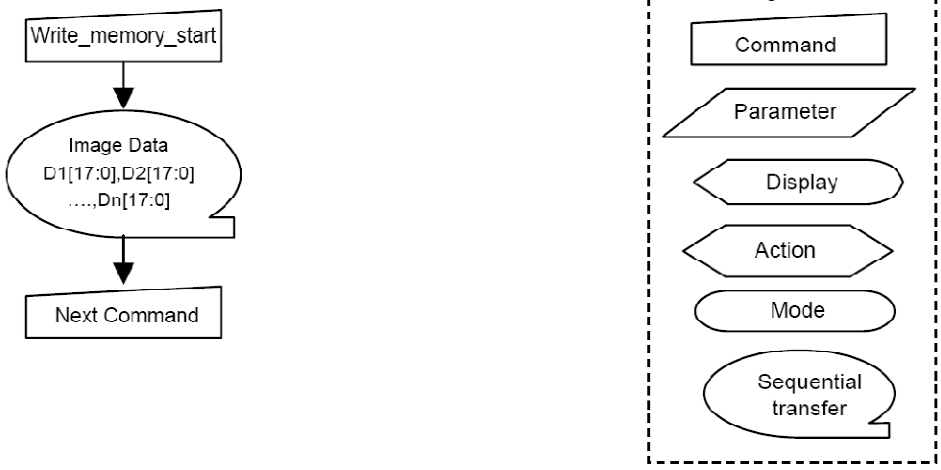
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.20. Read_memory_start (2Eh)

2EH	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2E
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FF
:	1	↑	1	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FF
(N+1)TH Parameter	1	↑	1	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FF

Description

This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If set_address_mode B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If set_address_mode B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

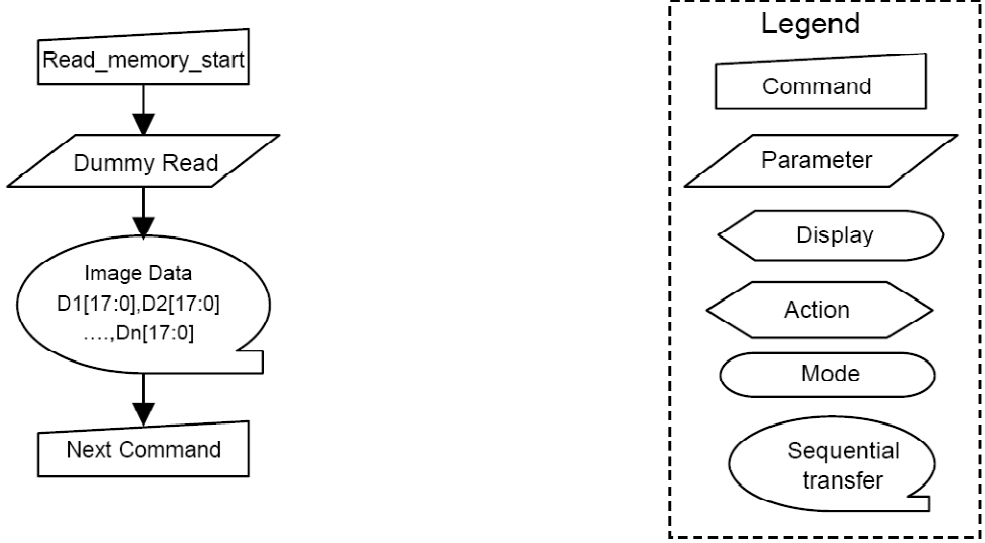
Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	

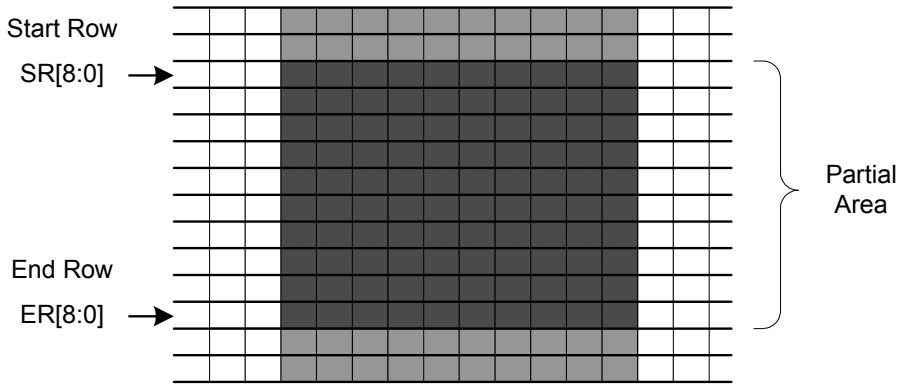
8.2.21. Set_partial_area (30h)

30H	Set_partial_area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SR8	000..1DFh
2nd Parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	ER8	000..1DFh
4th Parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	

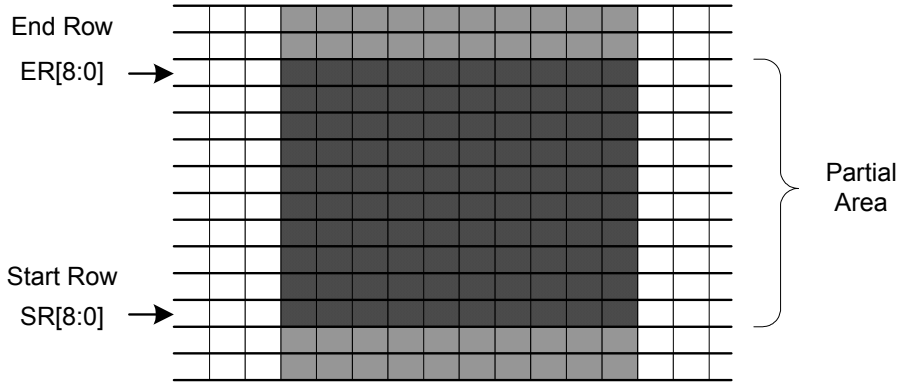
Description

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory

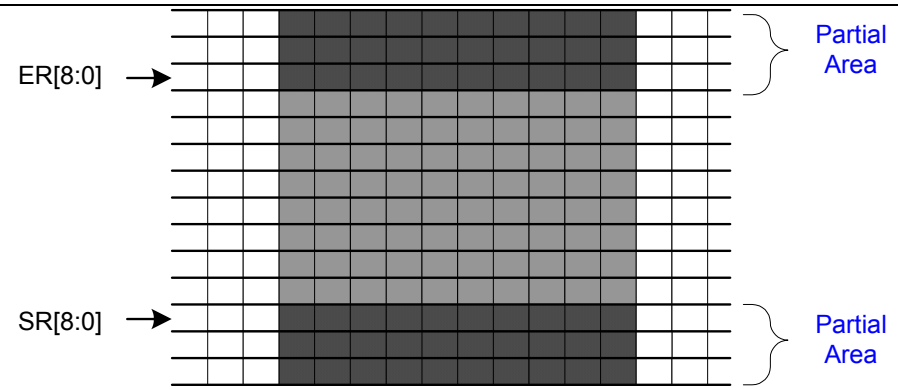
If End Row > Start Row and set_address_mode B4 = 0:



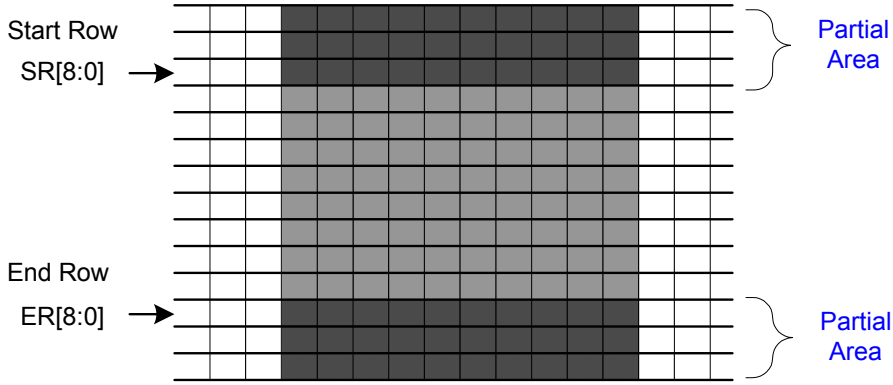
If End Row > Start Row and set_address_mode B4 = 1:



End Row < Start Row (set_address_mode(36h) B4=0)



End Row < Start Row (set_address_mode(36h) B4=1)



If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).

Register Availability

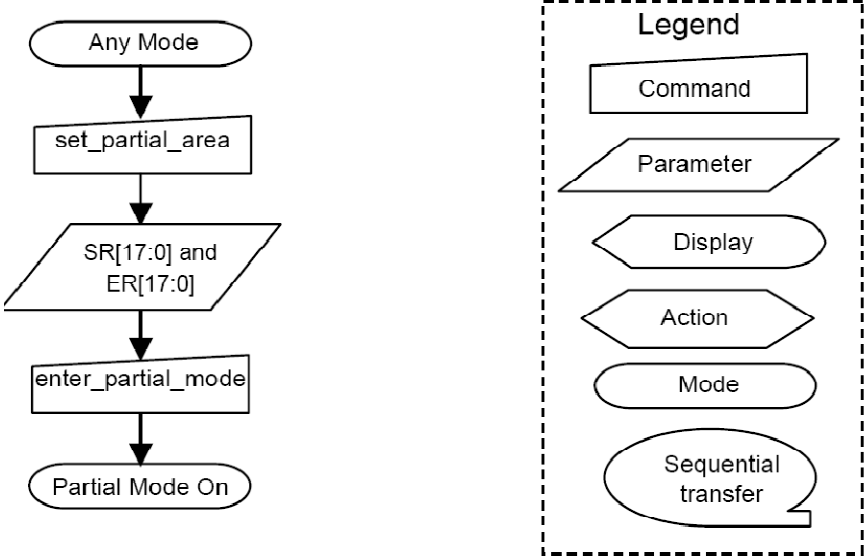
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

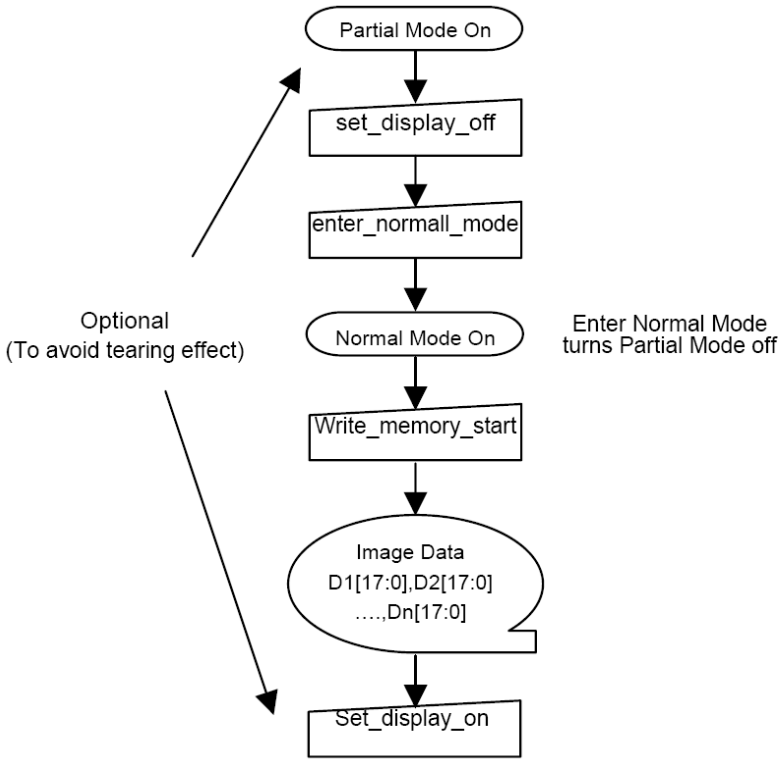
Status	Default Value	
Power On Sequence	SR[8:0]=0000_{HEX}	ER[8:0]=$1AF_{HEX}$
SW Reset	SR[8:0]=0000_{HEX}	ER[8:0]=$1AF_{HEX}$
HW Reset	SR[8:0]=0000_{HEX}	ER[8:0]=$1AF_{HEX}$

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.22. Set_scroll_area (33h)

33H	Set_scroll_area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	TFA [8]	0000 … 01E0
2nd Parameter	1	1	↑	x	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA 3]	TFA [2]	TFA [1]	TFA [0]	
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSA [8]	0000 … 01E0
4th Parameter	1	1	↑	x	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th Parameter	1	1	↑	x	0	0	0	0	0	0	0	BFA [8]	0000 … 01E0
6th Parameter	1	1	↑	x	BFA [7]	BFA [6]	BFA 5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	

Description

This command defines the display vertical scrolling area.

set_address_mode (36h) B4 = 0:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

set_scroll_area set_address_mode B4 = 0 Example

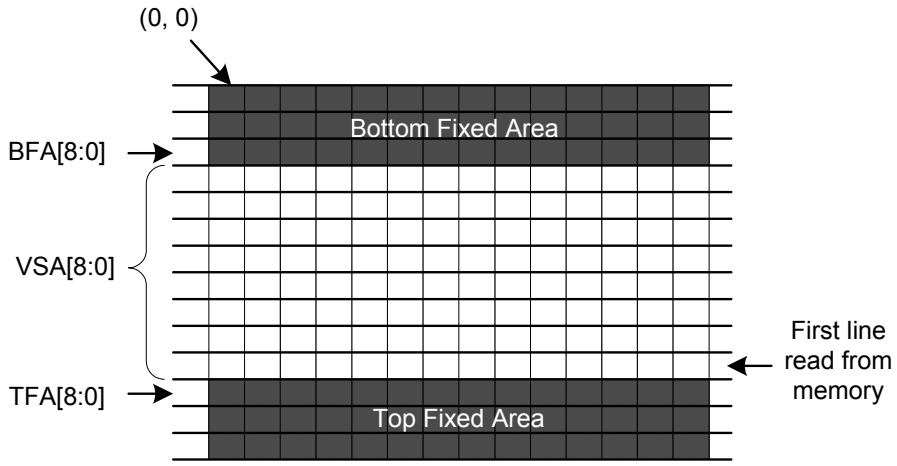
set_address_mode (36h) B4 = 1:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



set_scroll_area set_address_mode B4 = 1 Example

Restriction

The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

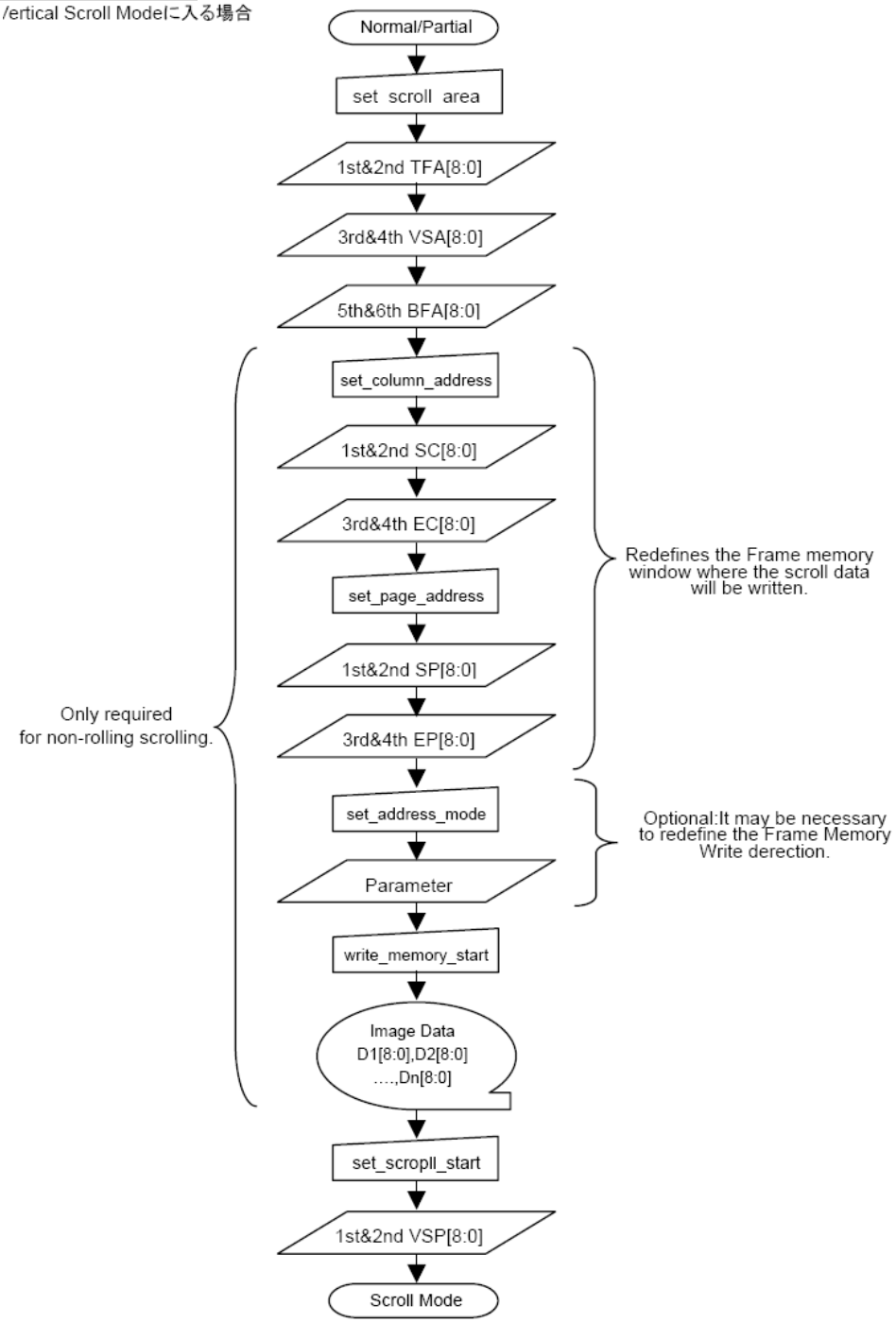
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[8:0]=0000_{HEX}	VSA[8:0]=$01B0_{HEX}$	BFA[8:0]=0000_{HEX}
SW Reset	TFA [8:0]=0000_{HEX}	VSA[8:0]=$01B0_{HEX}$	BFA[8:0]=0000_{HEX}
HW Reset	TFA [8:0]=0000_{HEX}	VSA[8:0]=$01B0_{HEX}$	BFA[8:0]=0000_{HEX}

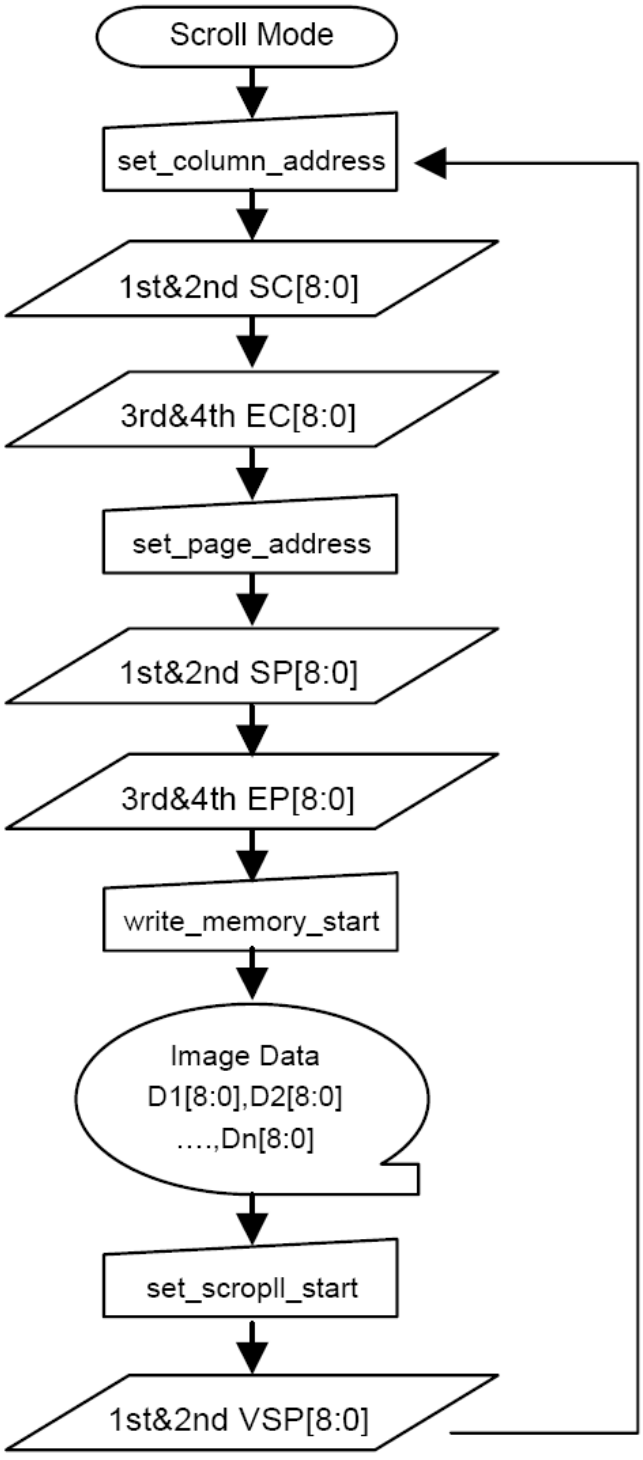
Flow Chart

1. To enter Vertical Scroll Mode:
/ertical Scroll Modeに入る場合

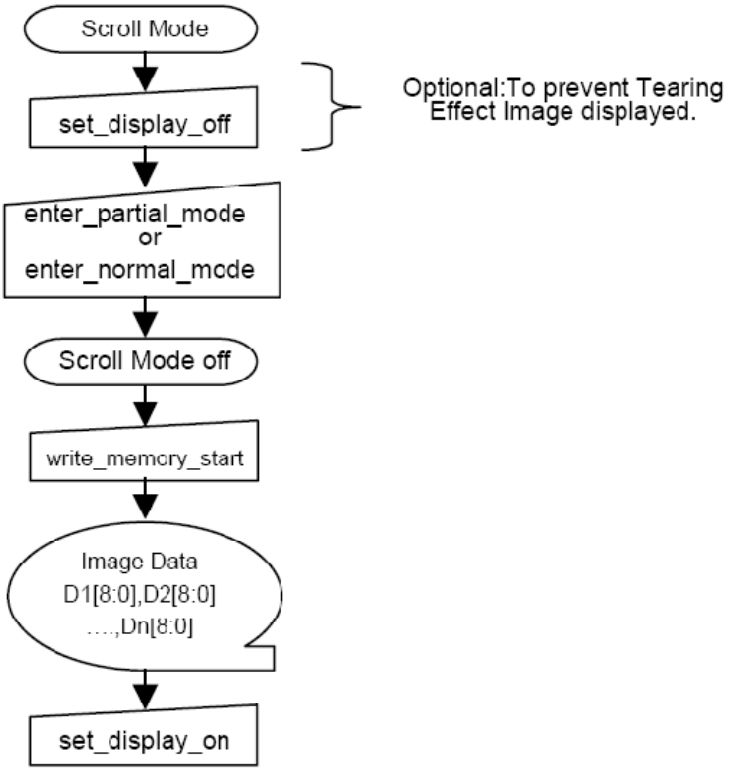


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise an undesirable image may be shown on the Display Panel.

2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



8.2.23. Set_tear_off (34h)

34H	Set_tear_off												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.												
Restriction	This command has no effect when the Tearing Effect output is already off.												

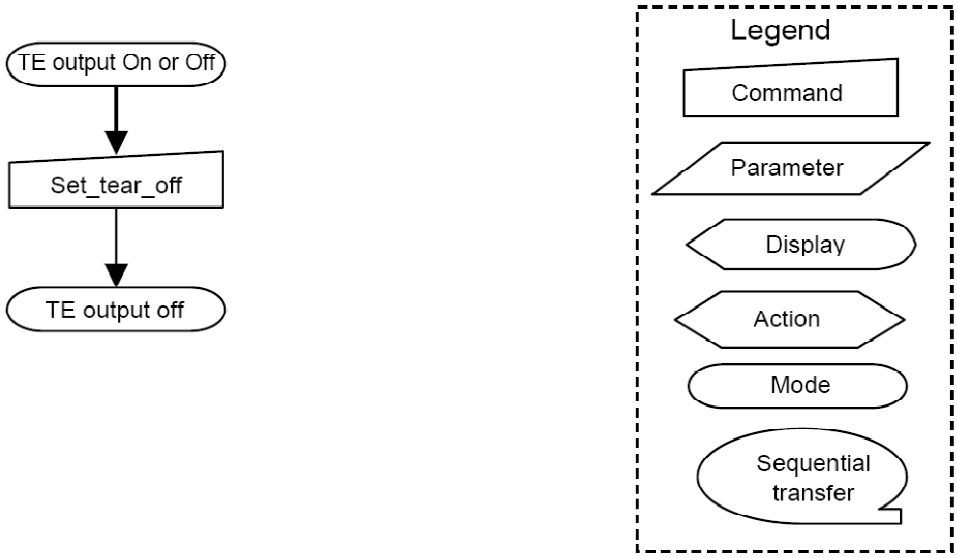
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



8.2.24. Set_tear_on (35h)

35H	Set_tear_on												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35
1st Parameter	1	1	↑	x	x	x	x	x	x	x	x	TELOM	xx

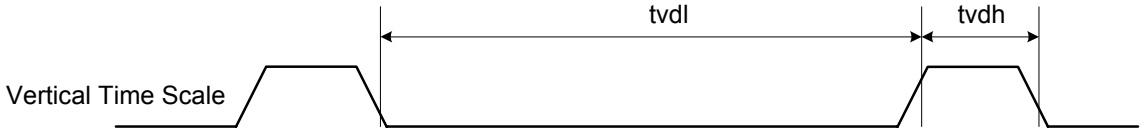
Description

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

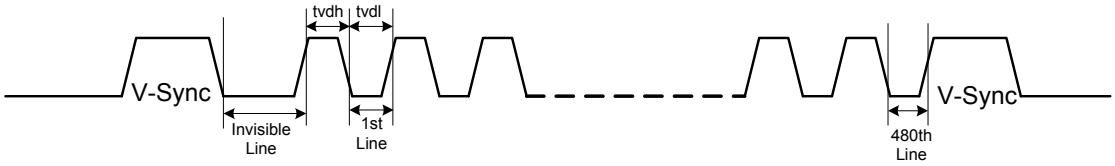
If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.



If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

This command has no effect when Tearing Effect output is already ON.

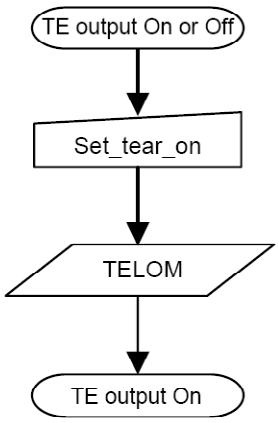
Register Availability

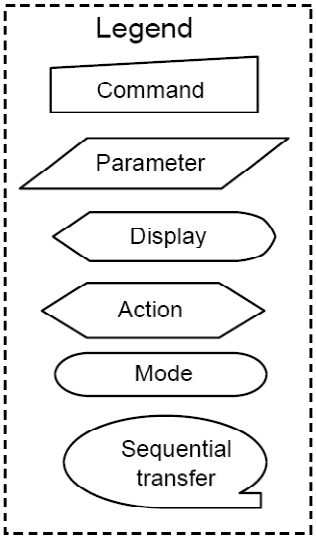
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart





8.2.25. Set_address_mode (36h)

36H	Set_address_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36
1st Parameter	1	1	↑	x	B7	B6	B5	B4	B3	0	B1	B0	xx

Description

This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

Bit	Description	Comment
B7	Page Address Order	
B6	Column Address Order	
B5	Page/Column Selection	
B4	Vertical Order	
B3	RGB/BGR Order	
B2	Display data latch data order	Set to '0'
B1	Horizontal Flip	
B0	Vertical Flip	

・Bit B7 – Page Address Order

'0' = Top to Bottom

'1' = Bottom to Top

・Bit B6 – Column Address Order

'0' = Left to Right

'1' = Right to Left

・Bit B5 – Page/Column Order

'0' = Normal Mode

'1' = Reverse Mode

・Bit B4 –Line Address Order

'0' = LCD Refresh Top to Bottom

'1' = LCD Refresh Bottom to Top

・Bit B3 – RGB/BGR Order

'0' = Pixels sent in RGB order

'1' = Pixels sent in BGR order

・Bit B2 –Display Data Latch Data Order

This bit is not applicable for this project, so it is set to '0'. (Not supported)

・Bit B1 – Horizontal Flip

'0' = Normal display

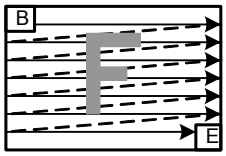
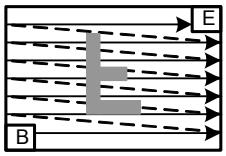
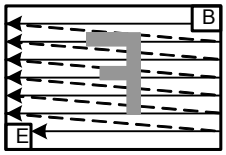
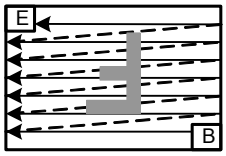
'1' = Flipped display

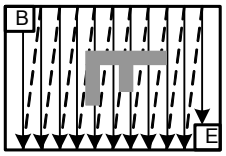
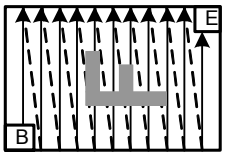
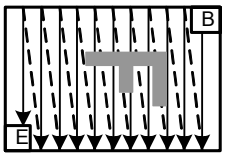
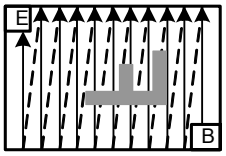
・Bit B0 – Vertical Flip

'0' = Normal display

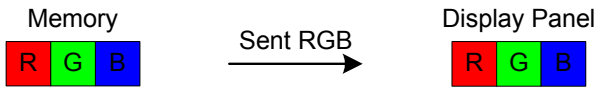
'1' = Flipped display

X = Don't care

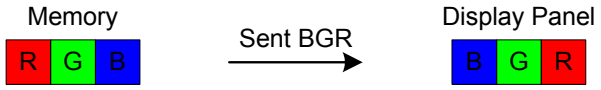
B5	B6	B7	Image in Frame Memory
0	0	0	
0	0	1	
0	1	0	
0	1	1	

B5	B6	B7	Image in Frame Memory
1	0	0	
1	0	1	
1	1	0	
1	1	1	

B3 = 0



B3 = 1



Restriction	

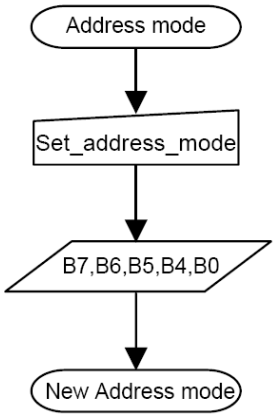
Register Availability

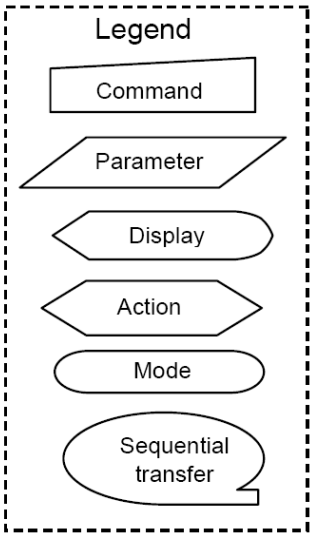
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	No Change
HW Reset	00_{HEX}

Flow Chart





8.2.26. Set_scroll_start (37h)

37H	Set_scroll_start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP [8]	xx
2nd Parameter	1	1	↑	x	VSP [7]	VSP [6]	VSP [5]	VSP [4]	VSP [3]	VSP [2]	VSP [1]	VSP [0]	xx

Description

This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command

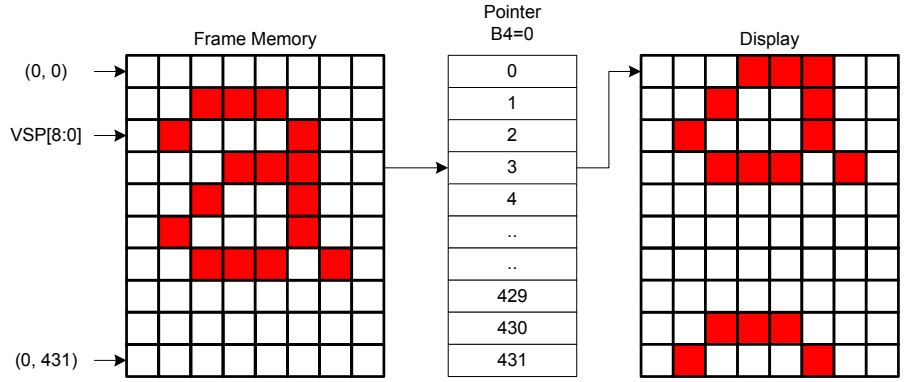
The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.

The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.

If set_address_mode (R36h) B4 = 0:

Example:

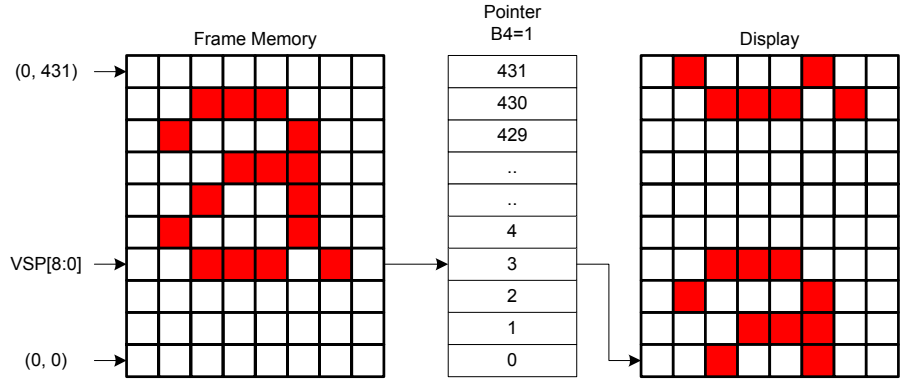
When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 432 and VSP = 3.



If set_address_mode (R36h) B4 = 1:

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 432 and VSP='3'.



Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000_{HEX}</td></tr>
<tr><td>SW Reset</td><td>0000_{HEX}</td></tr>
<tr><td>HW Reset</td><td>0000_{HEX}</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>Refer to the description set_scroll_area (33h)</td></tr>
</table>

8.2.27. Exit_idle_mode (38h)

38H	Exit_idle_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command causes the display module to exit Idle mode.												
Restriction	This command has no effect when the display module is not in Idle mode.												

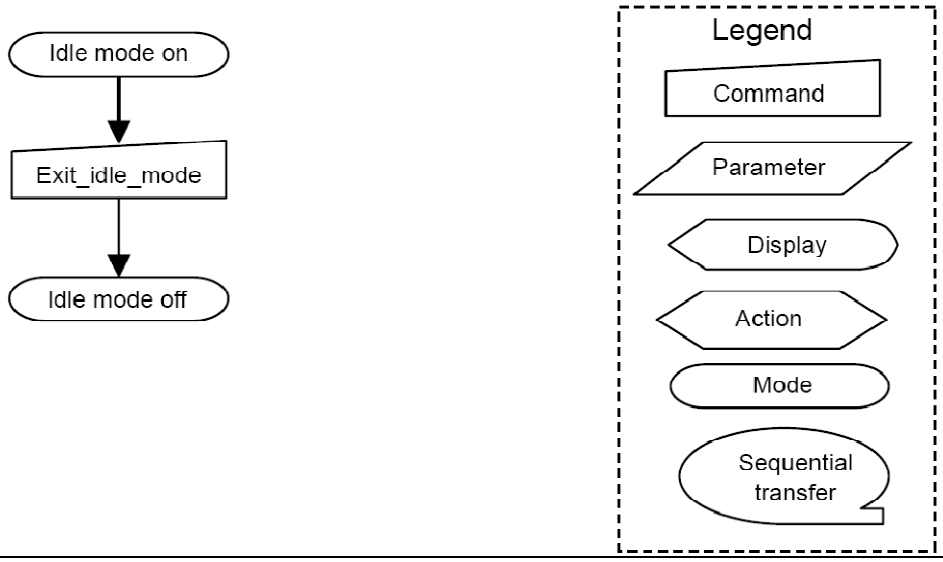
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



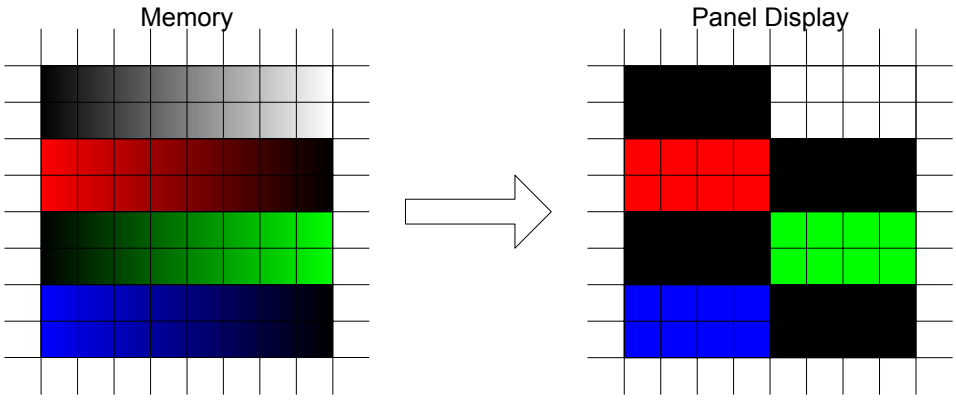
8.2.28. Enter_idle_mode (39h)

39H	Enter_idle_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command causes the display module to enter Idle Mode.

In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.



	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

This command has no effect when module is already in idle on mode.

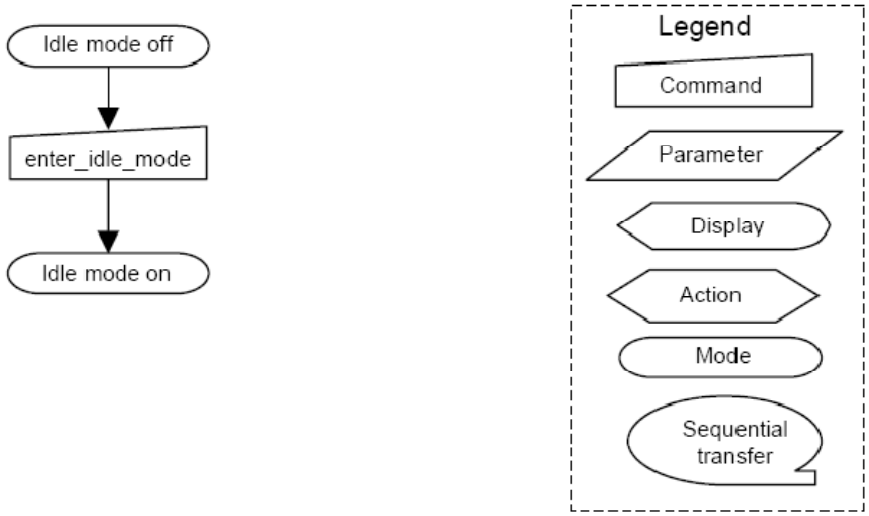
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



8.2.29. Set_pixel_format (3Ah)

3AH	Set_pixel_format												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A
1st Parameter	1	1	↑	x	x	D6	D5	D4	x	D2	D1	D0	66

Description

This command sets the pixel format for the RGB image data used by the interface.

Bits D[6:4] – DPI Pixel Format Definition

Bits D[2:0] – DBI Pixel Format Definition

Bits D7 and D3 are not used.

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Not defined	0	0	0
3bit/pixel (8 color)	0	0	1
Not defined	0	1	0
Not defined	0	1	1
Not defined	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
Not defined	1	1	1

Restriction

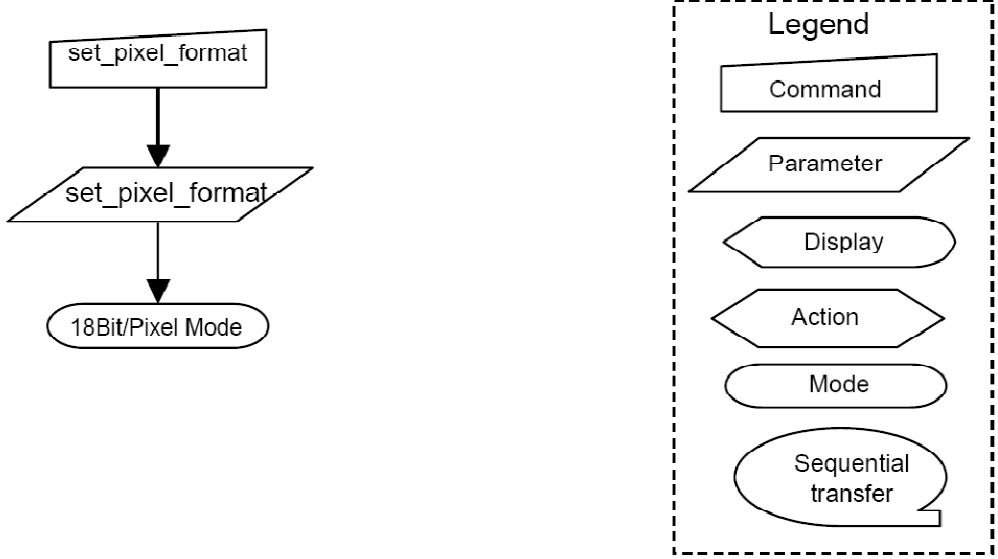
There is no visible effect until the Frame Memory is written to.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66_{HEX}
SW Reset	66_{HEX}
HW Reset	66_{HEX}

Flow Chart	

8.2.30. Write_Memory_Continue (3Ch)

3CH	Write_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C
1st Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
xst Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nst Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If set_address_mode B5 = 0:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode B5 = 1:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Sending any other command can stop frame Write.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=1

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

Restriction

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

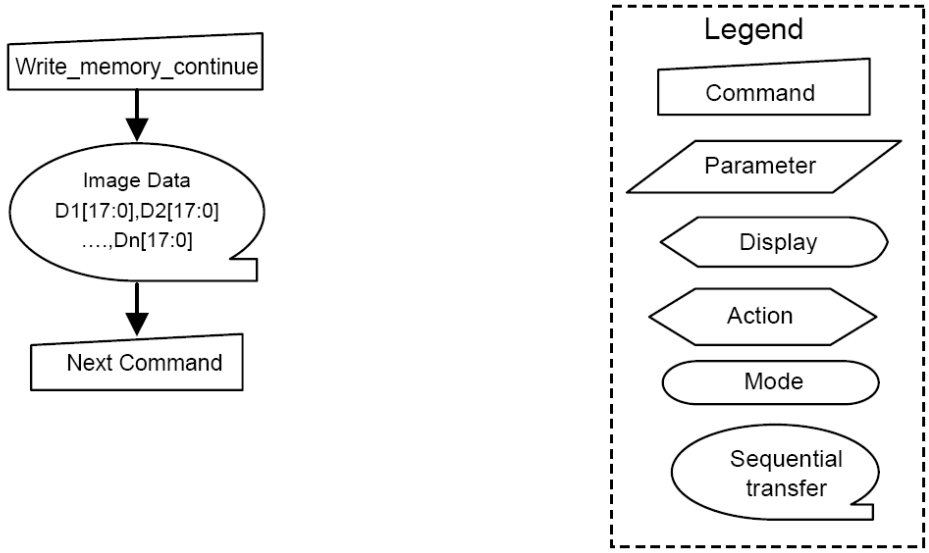
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	No

Default

Status	Default Value
Power On Sequence	Random value
SW Reset	No change
HW Reset	No change

Flow Chart



8.2.31. Read_Memory_Continue (3Eh)

3EH	Read_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3E
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
xst Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nst Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command.

If set_address_mode B5 = 0:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.

If set_address_mode B5 = 1:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.

This command makes no change to the other driver status.

Restriction

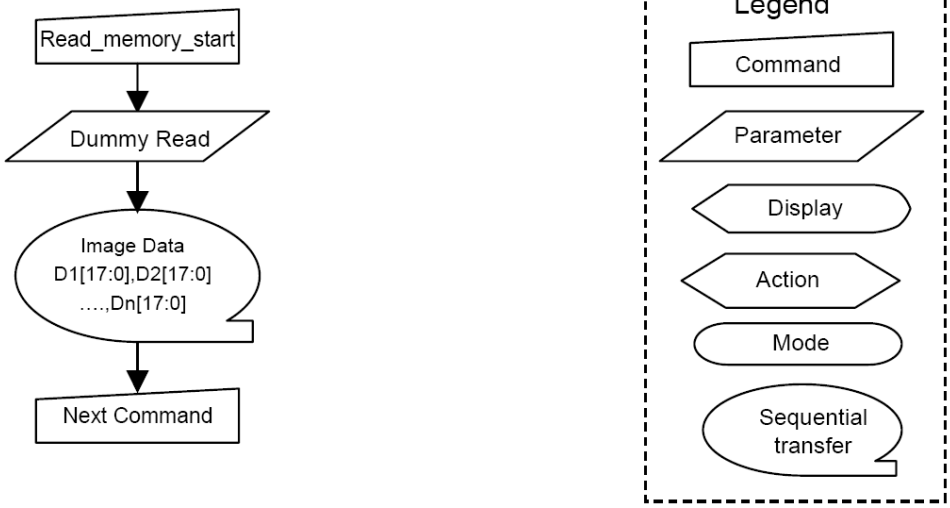
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random data
SW Reset	No change
HW Reset	No change

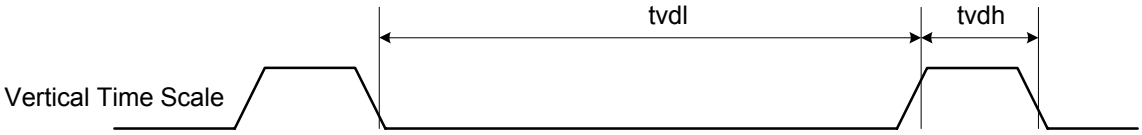
Flow Chart	

8.2.32. Set_Tear_Scanline (44h)

44H	Set_Tear_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44
1st Parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS [8]	0x
2nd Parameter	1	1	↑	xx	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	xx

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

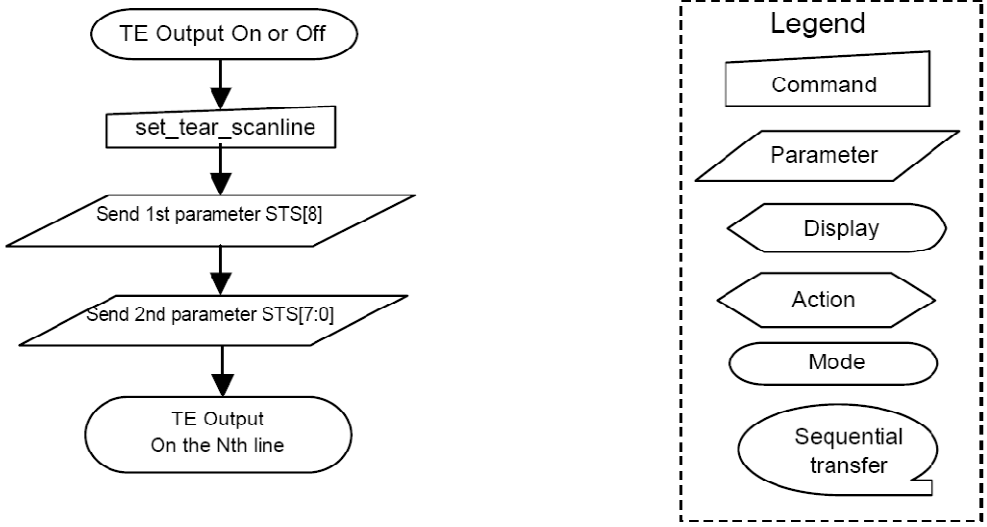
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



8.2.33. Get_Scanline (45h)

45H	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS [8]	0x
3rd Parameter	1	↑	1	xx	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	xx

Description

The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.

Restriction

None

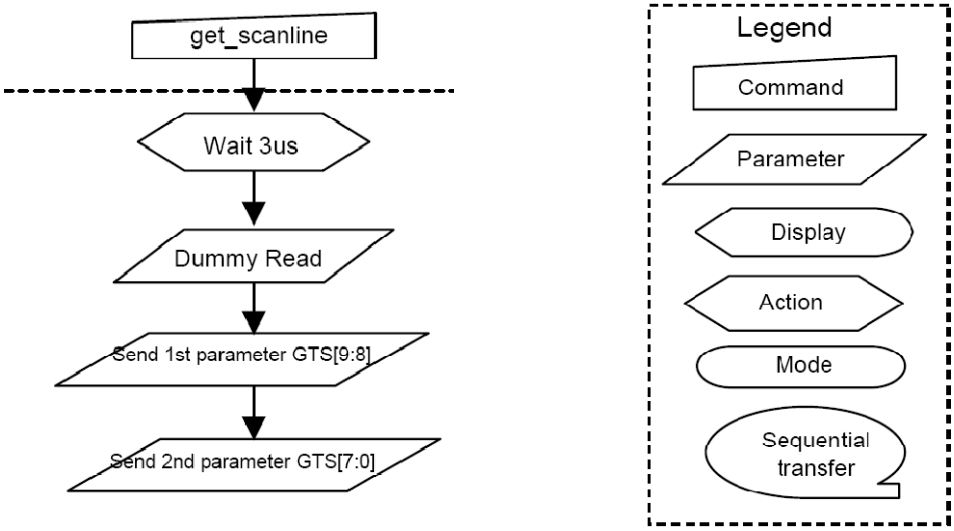
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



8.2.34. Write Display Brightness (51h)

51H	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	0	1	51
1st Parameter	1	↑	1	xx	DBV [7]	DBV [6]	DBV [5]	DBV [4]	DBV [3]	DBV [2]	DBV [1]	DBV [0]	00 .. FF
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												

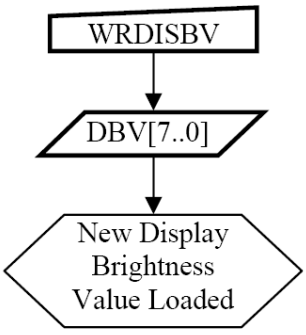
Register Availability

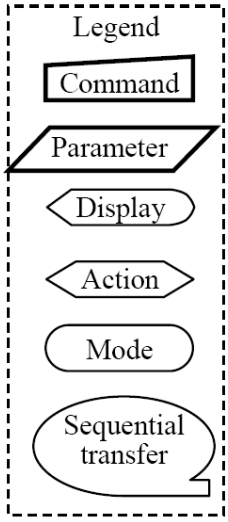
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart





8.2.35. Read Display Brightness Value (52h)

52H	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	1	0	52
1st Parameter	1	↑	1	xx	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	xx	DBV [7]	DBV [6]	DBV [5]	DBV [4]	DBV [3]	DBV [2]	DBV [1]	DBV [0]	xx

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode.

Write CTRL Display (53h)" bit DB = '1'.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'.

DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when bit BCTRL is '1' and bit A of "Write CTRL Display (53h)" command is '0'.

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.

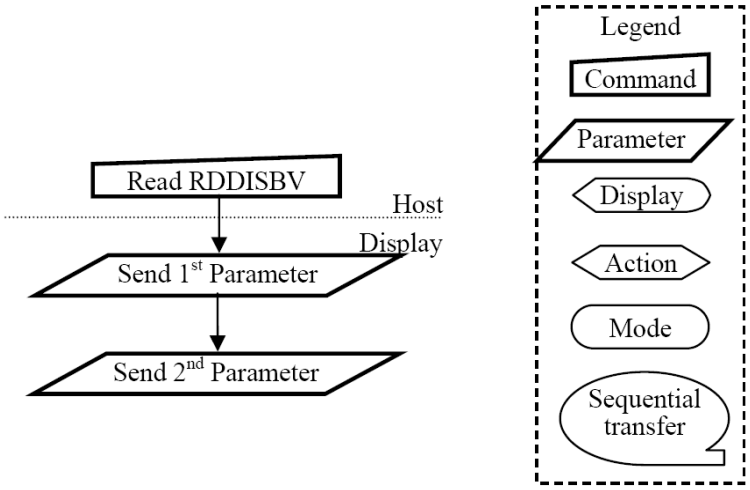
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart	

8.2.36. Write CTRL Display (53h)

53H	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	1	1	53
1st Parameter	1	↑	1	xx	0	0	BCTRL	0	DD	BL	DB	0	xx

Description

This command is used to control brightness setting.

BCTRL: Brightness Control Block On/Off,

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)

DD: Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

BL: Backlight On/Off

'0' = Off.

'1' = On.

DB: Display brightness manual/automatic

'0' = Manual, see chapter "Write Display Brightness (51h)"; Note: The user has to use this setting for manual adjustment of the brightness to have an effect.

'1' = Automatic: Information about the used brightness is included in the active profile; Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

Restriction

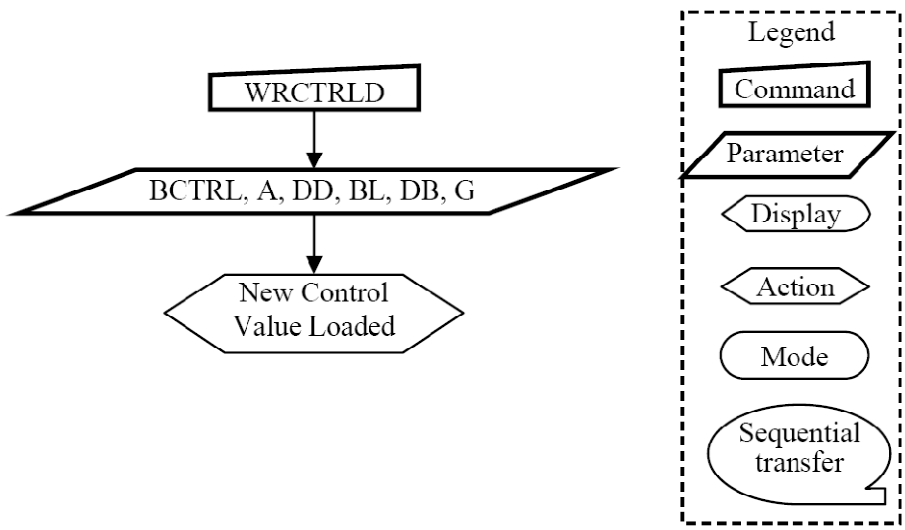
None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BCTRL=0, DD=0, BL=0, DB=0
SW Reset	BCTRL=0, DD=0, BL=0, DB=0
HW Reset	BCTRL=0, DD=0, BL=0, DB=0

Flow Chart	

8.2.37. Read CTRL Display (54h)

54H	RDCTRLD (Read Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	0	0	54
1st Parameter	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	xx	0	0	BCTRL	0	DD	BL	DB	0	xx

Description

This command is used to return brightness setting.

BCTRL: Brightness Control Block On/Off,

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)

DD: Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

BL: Backlight On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)

'1' = On

DB: Display brightness manual/automatic

'0' = Manual, see chapter "Write Display Brightness (51h)"; Note: The user has to use this setting for manual adjustment of the brightness to have an effect.

'1' = Automatic: Information about the used brightness is included in the active profile; Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

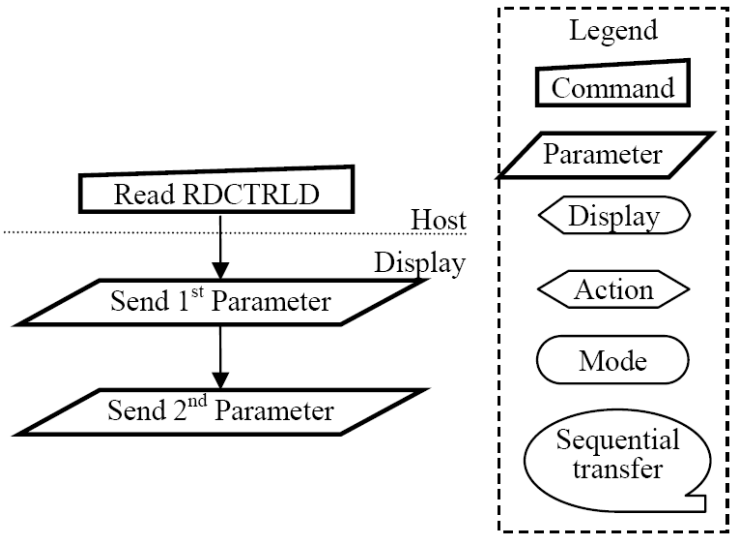
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BCTRL=0, DD=0, BL=0, DB=0
SW Reset	BCTRL=0, DD=0, BL=0, DB=0
HW Reset	BCTRL=0, DD=0, BL=0, DB=0

Flow Chart	

8.2.38. Write Content Adaptive Brightness Control (55h)

55H	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	0	1	55
1st Parameter	1	↑	1	xx	0	0	0	0	0	0	C[1]	C[0]	xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

None

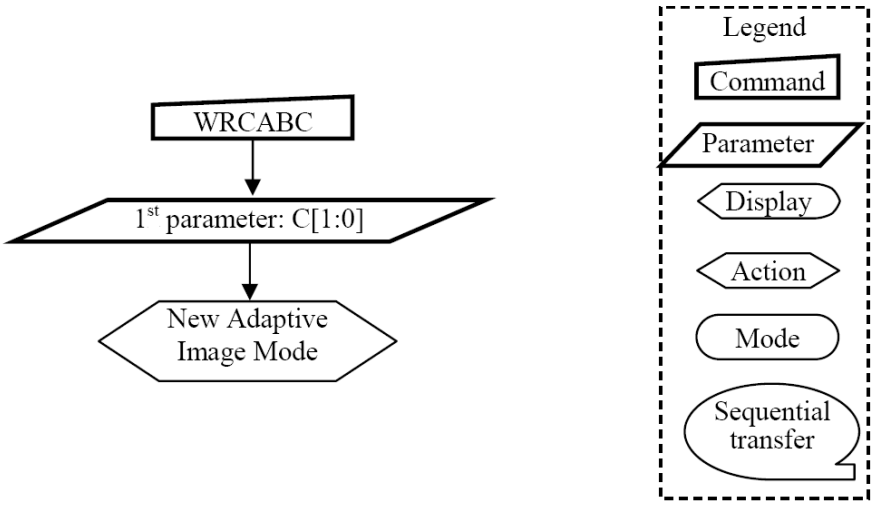
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C[1:0]=00_{HEX}
SW Reset	C[1:0]=00_{HEX}
HW Reset	C[1:0]=00_{HEX}

Flow Chart



8.2.39. Read Content Adaptive Brightness Control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	1	0	56
1st Parameter	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	xx	0	0	0	0	0	0	C[1]	C[0]	xx

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

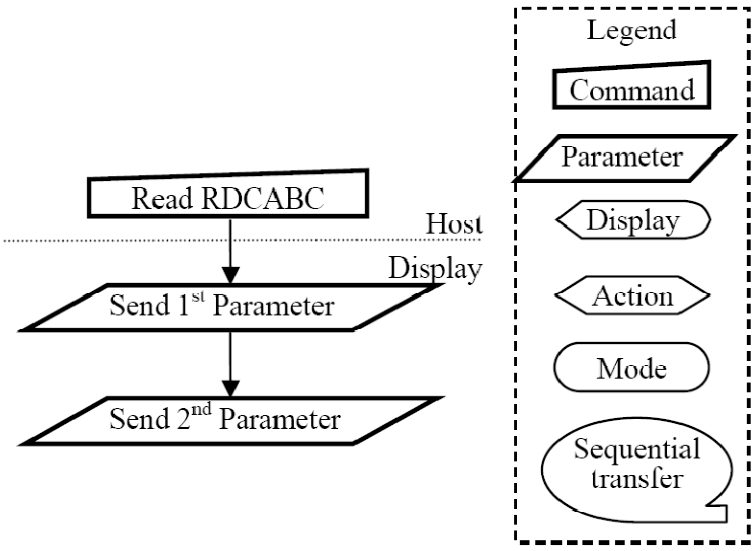
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C[1:0]=00_{HEX}
SW Reset	C[1:0]=00_{HEX}
HW Reset	C[1:0]=00_{HEX}

Flow Chart



8.2.40. Write CABC Minimum Brightness (5Eh)

B8H	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	0	0	0	B8
1st parameter	0	↑	1	xx	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1	CMB[7]	FF

Description

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

8.2.41. Read CABC Minimum Brightness (5Fh)

B8H	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	0	0	0	B8
1st parameter	0	↑	1	xx	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1	CMB[7]	FF
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

8.2.42. Read_DDB_Start (A1h)

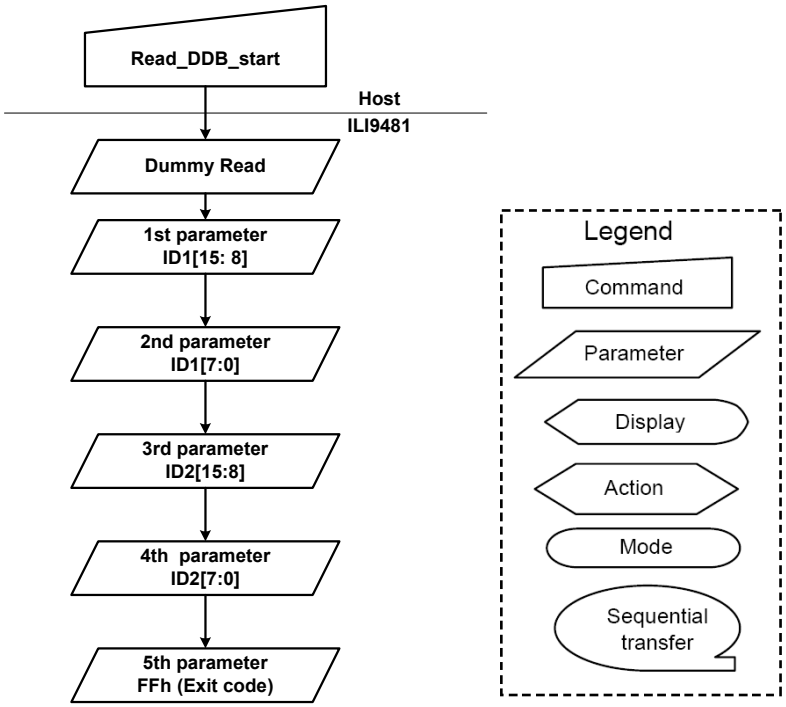
A1H	Read_DDB_Start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	0	0	0	0	1	A1
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	xx	0	0	0	0	ID[3]	ID[2]	ID[1]	ID[0]	xx
3rd Parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF
Description	1st parameter: Dummy read 2nd parameter: ID code[3:0] 3th parameter: Exit code (FFh).												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ID[3:0]=00_{HEX}
SW Reset	ID[3:0]=00_{HEX}
HW Reset	ID[3:0]=00_{HEX}

Flow Chart



8.2.43. Command Access Protect (B0h)

B0H	Command Access Protect												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	0	0	0	B0
1st parameter	0	1	↑	xx	0	0	0	0	0	0	MCAP[1]	MCAP[0]	00

Description

MCAP[1:0]	User Command	Protect command	Manufacturer Command		
	00h ~ AFh	B0h	B1h ~ DFh	E0h~EFh	F0h~FFh
2'b00	Yes	Yes	Yes	Yes	Yes
2'b01	Yes	Yes	Yes	Yes	No
2'b10	Yes	Yes	Yes	No	No
2'b11	Yes	Yes	No	No	No

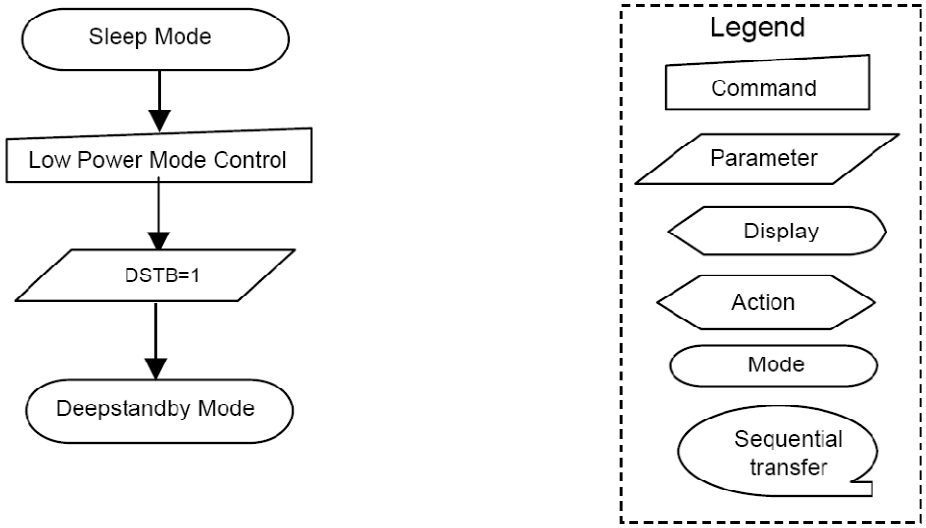
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MCAP[1:0]=2'h0
SW Reset	No change
HW Reset	MCAP[1:0]=2'h0

Flow Chart



8.2.44. Low Power Mode Control (B1h)

B1H	Low Power Mode Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	0	0	1	B1
1st parameter	0	1	↑	xx	0	0	0	0	0	0	0	DSTB	0
Description	**DSTB** The driver enters the Deep Standby Mode when DSTB=1. Internal logic power supply circuit is turned down enabling low power consumption. In the Deep Standby mode, data stored in the Frame Memory and the Instructions are not retained. Rewrite them after the Deep Standby mode is exited.												

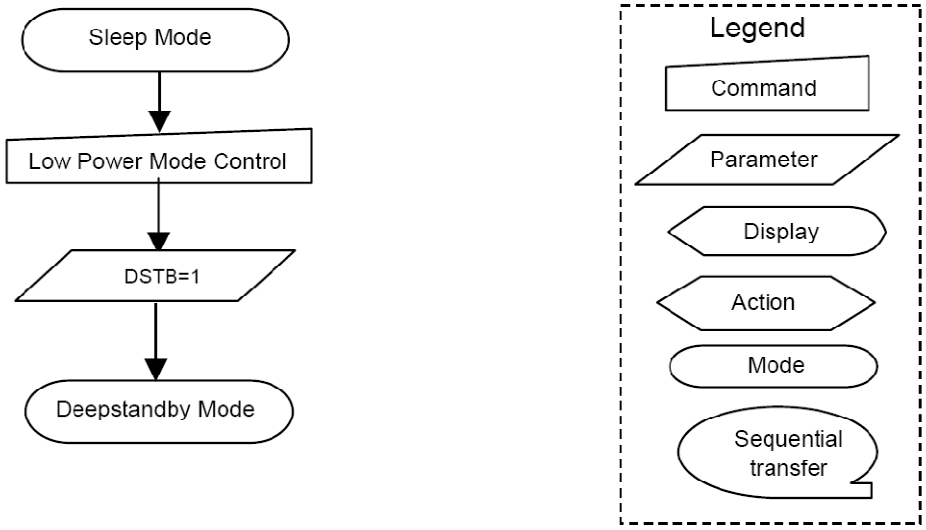
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DSTB=1'b0
SW Reset	No change
HW Reset	DSTB=1'b0

Flow Chart



8.2.45. Frame Memory Access and Interface Setting (B3h)

B3H	Frame Memory Access and Interface Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	0	1	1	B3
1st parameter	0	1	↑	xx	0	0	0	0	0	0	WEMODE	0	02
1st parameter	0	1	↑	xx	0	0	0	0	0	TEI[2]	TEI[10]	TEI[0]	00
2nd parameter	0	1	↑	xx	0	0	0	0	0	DENC[2]	DENC[1]	DENC[0]	00
4th parameter	0	1	↑	xx	0	0	EPF[1]	EPF[0]	0	0	0	DFM	20

Description

WEMODE: Memory write control

WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

TEI[2:0]: ILI9327 starts to output TE signal in the output interval set by TEI[2:0] bits.

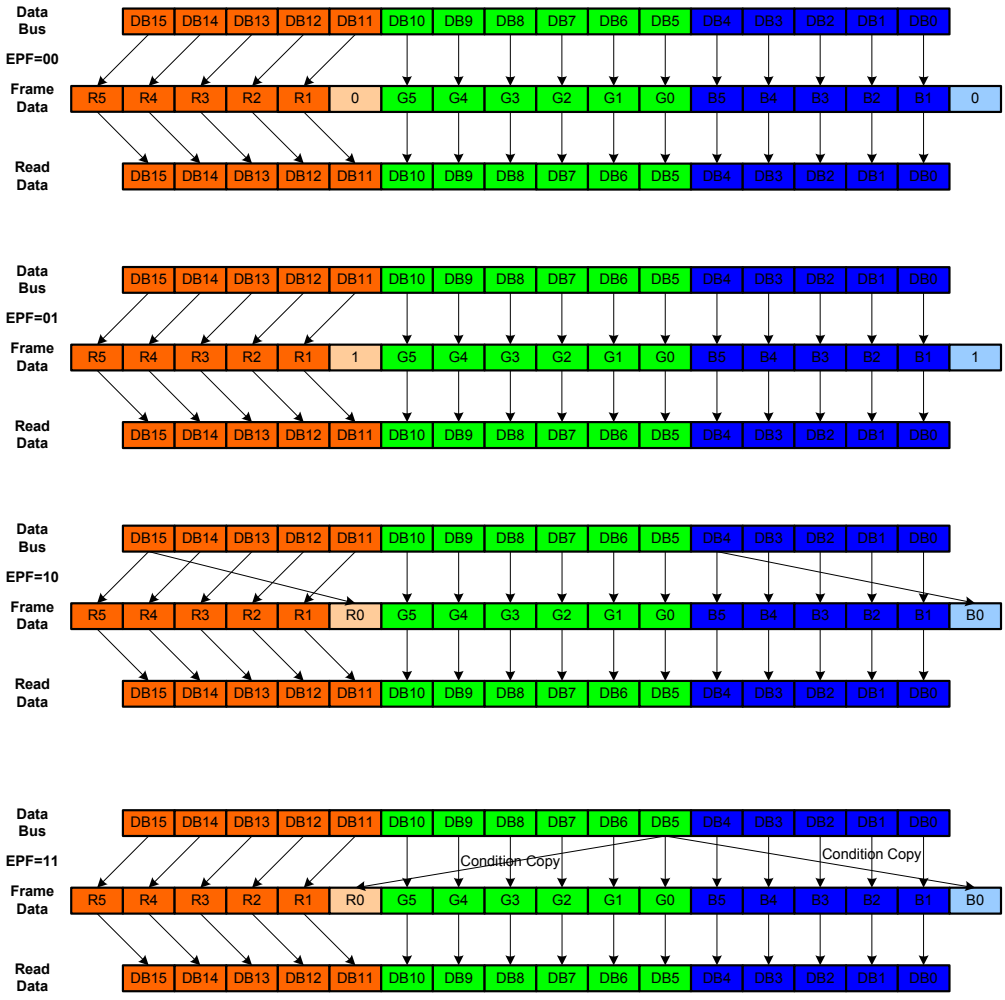
TEI[2:0]	Output Interval
3'b000	1 frame
3'b001	2 frame
3'b011	4 frame
3'b101	6 frame
Others	Setting Prohibited

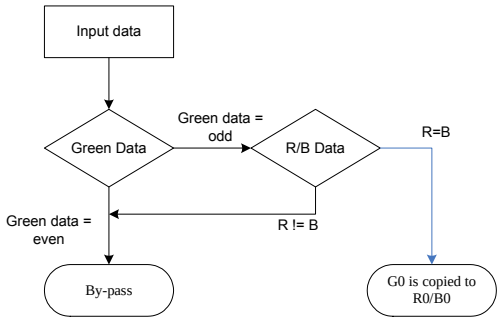
DENC[2:0]: Set the GRAM write cycle through the RGB interface

DENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

DFM: The bit is used to define image data write/read format to the Frame Memory in DBI Type B (16bit bus interface) and DBI Type C serial interface operation.

EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM.





EPF[1:0]	Expand 16bbp (R,G,B) to 18 bbp (R, G, B)
00	"0" is inputted to LSB r[5:0] = {R[4:0], 0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 0} Exception: R[4:0], B[4:0]=5'h1F → r[5:0], b[5:0] = 6'h3F
01	"1" is inputted to LSB r[5:0] = {R[4:0], 1} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1}

<table>
<tr><td></td><td></td><td>
<table>
<tr><td></td><td>Exception:
R[4:0], B[4:0]=5'h00 → r[5:0], b[5:0] = 6'h00</td></tr>
<tr><td>10</td><td>MSB is inputted to LSB
r[5:0] = {R[4:0], R[4]}
g[5:0] = {G[5:0]}
b[5:0] = {B[4:0], B[4]}</td></tr>
<tr><td>11</td><td>MSB is inputted to LSB
r[5:0] = {R[4:0], G[0]}
g[5:0] = {G[5:0]}
b[5:0] = {B[4:0], G[0]}</td></tr>
</table>
</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h2</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h2</td></tr>
</table>
</td></tr>
</table>

8.2.46. Display Mode and Frame Memory Write Mode Setting (B4h)

B4H	Display Mode and Frame Memory Write Mode Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	1	0	0	B4
1st parameter	0	1	↑	xx	0	0	0	RM	0	0	0	DM	00

Description

DM Select the display operation mode.

DM0	Display Interface
0	Internal system clock
1	DPI (RGB) interface

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	DBI Interface (CPU)
1	DPI Interface (RGB)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DM=0, RM=0
SW Reset	No change
HW Reset	DM=0, RM=0

8.2.47. Sub-Panel Control Register (B5h)

B5H	Sub-Panel Control Register												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	1	0	1	B5
1st parameter	0	1	↑	xx	0	0	0	STN_EN	0	0	0	Sub_IM[0]	00

Description

Sub_IM[1:0]: Sub-panel interface selection.

Sub_IM	Display Interface
0	8-bit interface (default)
1	9-bit interface

STN_EN[1:0]:panel type selection.

STN_EN	Display Interface
0	TFT Type sub-panel
1	STN Type sub-panel

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sub_IM=0, STN_EN=0
SW Reset	No change
HW Reset	Sub_IM=0, STN_EN=0

8.2.48. Backlight Control 1 (B8h)

B8H	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	0	0	0	B8
2nd parameter	0	↑	1	xx	0	0	0	0	TH_UI[3]	TH_UI[2]	TH_UI[1]	TH_UI[0]	04

Description

TH_UI[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_UI[3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	**92%**
4'5h	90%
4'6h	88%
4'7h	86%

TH_UI[3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	TH_UI[3:0]=4'h04
SW Reset	No change
HW Reset	TH_UI[3:0]=4'h04

8.2.49. Backlight Control 2 (B9h)

B8H	Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	0	0	1	B9
2nd parameter	0	↑	1	xx	TH_MV[3]	TH_MV[2]	TH_MV[1]	TH_MV[0]	TH_ST[3]	TH_ST[2]	TH_ST[1]	TH_ST[0]	B8

Description

TH_ST[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

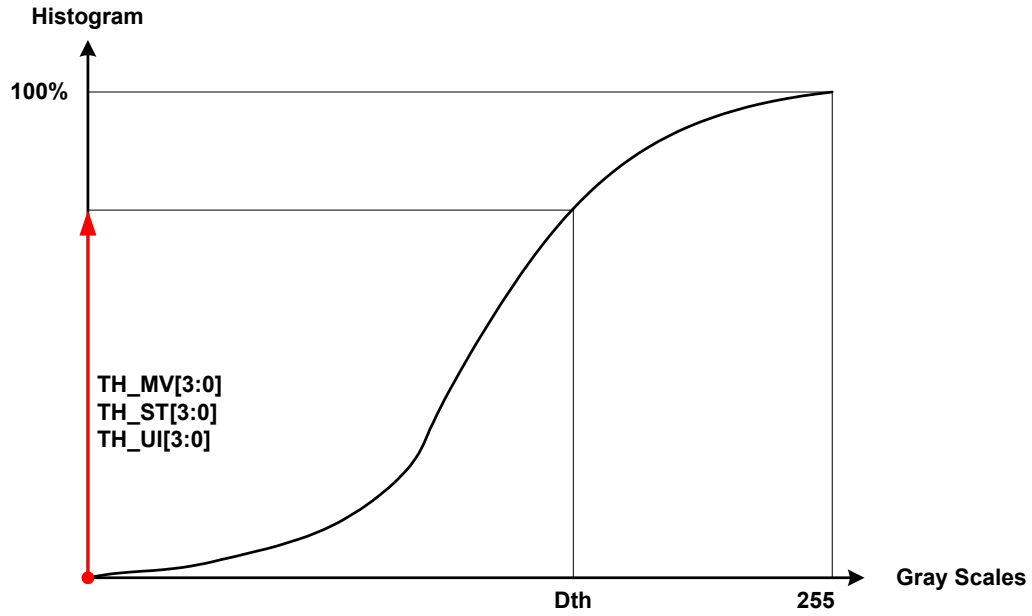
TH_ST[3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_ST[3:0]	Description
4'8h	**84%**
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

TH_MV[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_MV[3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV[3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	**78%**
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%



Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	TH_MV[3:0]=4'h0D, TH_ST[3:0]=4'h08
SW Reset	No change
HW Reset	TH_MV[3:0]=4'h0D, TH_ST[3:0]=4'h08

8.2.50. Backlight Control 3 (BAh)

B8H	Backlight Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	0	1	0	BA
2nd parameter	0	↑	1	xx	0	0	0	0	DTH_UI[3]	DTH_UI[2]	DTH_UI[1]	DTH_UI[0]	04

Description

DTH_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_UI[3:0]	Description
4'0h	252
4'1h	248
4'2h	244
4'3h	240
4'4h	**236**
4'5h	232
4'6h	228
4'7h	224

DTH_UI[3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DTH_UI[3:0]=4'h04
SW Reset	No change
HW Reset	DTH_UI[3:0]=4'h04

8.2.51. Backlight Control 4 (BBh)

B8H	Backlight Control 4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	0	1	1	BB
2nd parameter	0	↑	1	xx	DTH_MV[3]	DTH_MV[2]	DTH_MV[1]	DTH_MV[0]	DTH_ST[3]	DTH_ST[2]	DTH_ST[1]	DTH_ST[0]	C9

Description

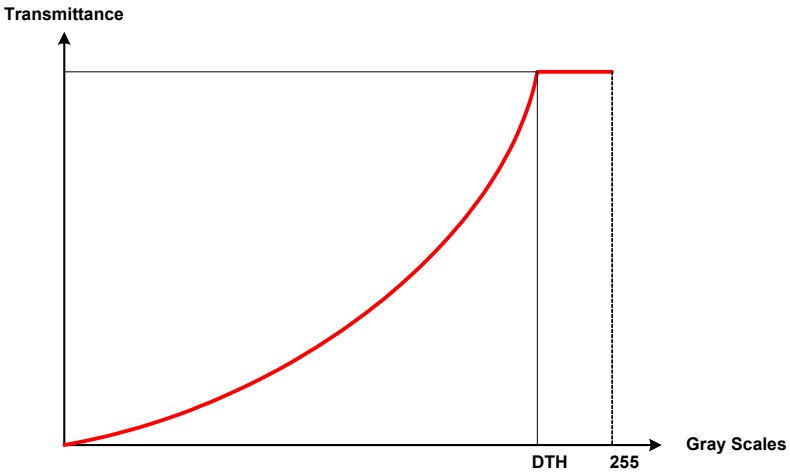
DTH_ST[3:0]/DTH_MV[3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_ST[3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_ST[3:0]	Description
4'8h	192
4'9h	**188**
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_MV[3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_MV[3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	**176**
4'Dh	172
4'Eh	168
4'Fh	164



Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DTH_MV[3:0]=4'h0C, DTH_ST[3:0]=4'h09
SW Reset	No change
HW Reset	DTH_MV[3:0]=4'h0C, DTH_ST[3:0]=4'h09

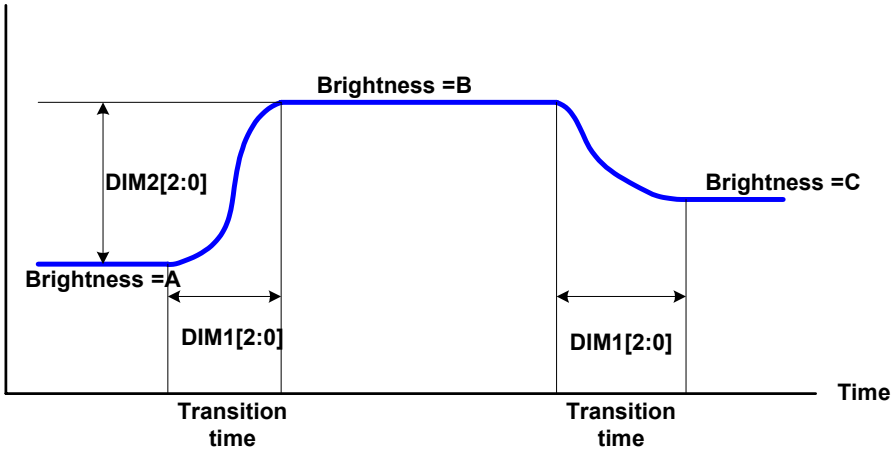
8.2.52. Backlight Control 5 (BCh)

B8H	Backlight Control 5												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	1	0	0	BC
2nd parameter	0	↑	1	xx	DIM2[3]	DIM2[2]	DIM2[1]	DIM2[0]	0	DIM1[2]	DIM1[1]	DIM1[0]	74

Description

DIM1[2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM1[2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	**8 frames**
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames



DIM2[3:0]: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than **DIM2[3:0]**, the brightness transition will be ignored.

For example:

If | brightness B – brightness A| < DIM2[2:0], the brightness transition will be ignored and keep the brightness A.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	DIM2[3:0]=4'h07, DIM1[2:0]=4'h04
SW Reset	No change
HW Reset	DIM2[3:0]=4'h07, DIM1[2:0]=4'h04

8.2.53. Backlight Control 7 (BEh)

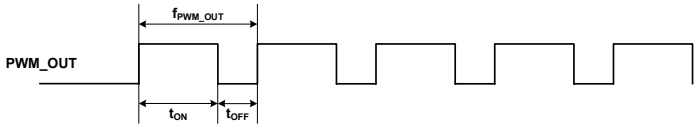
B9H	Backlight Control 7												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	1	1	0	BE
1st parameter	0	↑	1	xx	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	0F

Description

PWM_DIV[7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{pwm\_out} = \frac{8MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV[7:0]	f_{PWM_OUT}
8'h0	31.37 KHz
8'h1	15.69 KHz
8'h2	10.46KHz
8'h3	7.843 KHz
8'h4	6.27 KHz
…	…
8'hFB	523Hz
8'hFC	514Hz
8'hFD	506Hz
8'hFE	498Hz
8'hFF	490Hz



***Note**: The output frequency tolerance of internal frequency divider in CABC is ±10%*

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	PWM_DIV[7:0]=8'h0A
SW Reset	No change
HW Reset	PWM_DIV[7:0]=8'h0A

8.2.54. Backlight Control 8 (BFh)

B9H	Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	1	1	1	BF
1st parameter	0	↑	1	xx	0	0	0	0	0	LEDONR	LEDONPOL	LEDPWMPOL	00

Description

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWMPOL	LEDPWM pin
0	0	0
0	1	1
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control LEDON pin.

BL	LEDONPOL	LEDON pin
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

LEDONR: This bit is used to control LEDON pin.

LEDONR	Description
0	Low
1	High

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	LEDPWMPOL=0, LEDONPOL=0, LEDONR=0
SW Reset	No change
HW Reset	LEDPWMPOL=0, LEDONPOL=0, LEDONR=0

8.2.55. Panel Driving Setting (C0h)

C0H	Panel Driving Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1st Parameter	1	1	↑	0	0	0	0	REV	SM	GS	BGR	SS	00
2nd Parameter	1	1	↑	0	0	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	35
3rd Parameter	1	1	↑	0	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	00
4th Parameter	1	1	↑	0	0	0	0	0	0	0	PTS [1]	PTS [0]	00
5th Parameter	1	1	↑	0	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	01
6th Parameter	1	1	↑	0	0	0	0	0	0	0	DIVE [1]	DIVE [0]	02

Description

SS

The bit is used to select the shifting direction of the source driver output.

SS=0: S1 to S720 (Default)

SS=1: S720 to S1

BGR

The bit is used to reverse 18-bit write data in the Frame Memory from RGB to BGR. Set in accordance with arrangement of color filters.

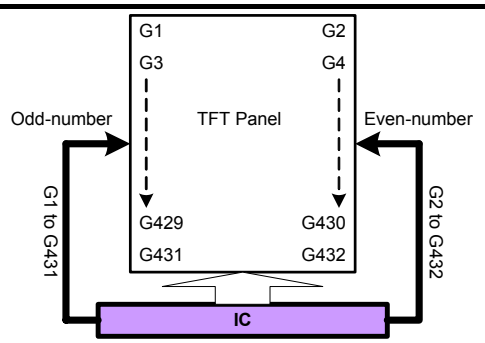
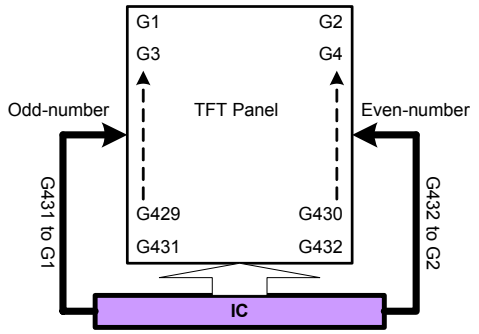
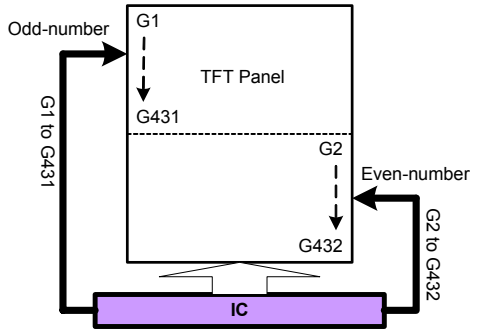
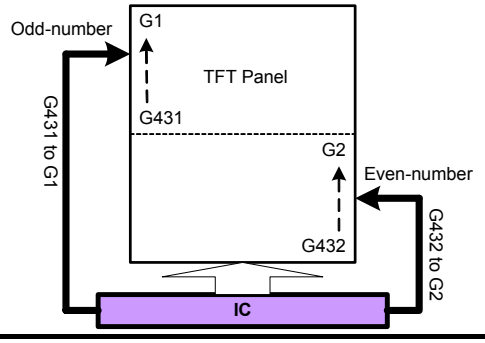
BGR=0: Display data is in RGB sequence. (Default)

BGR=1: Display data is in BGR sequence.

REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, …,G428 G429, G430, G431, G432
0	1		G432, G431, G430, …, G9 G7, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7, …,G423 G425, G427, G429, G431 G2, G4, G6, G8, …,G424 G426, G428, G430, G432
1	1		G432, G430, G428, …,G14 G12, G10, G8, G6, G4, G2 G431, G429, G427,…,G13 G11, G9, G7, G5, G3, G1

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h35	8 * (NL5:0]+1) lines
Others	Setting inhibited

SCN[6:0]: Specifies the gate line where the gate driver starts scan

SCN[6:0]	Scanning Start Position

	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h ~ 3Bh	G[1+SCN[6:0]*4]	G[432 - SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[432 - SCN[6:0]*8]
3Ch ~ 77h	G[1+SCN[6:0]*4]	G[432 - SCN[6:0]*4]	G[2+(SCN[6:0]-3Ch)*8]	G[431 – (SCN[6:0]-36h)*8]
Others	Setting disabled	Setting disabled	Setting disabled	Setting disabled

PTG: Sets the scan mode in non-display area. Select frame-inversion when interval-scan is selected.

PTG	Scan Mode in non-display area
0	Normal Scan
1	Interval Scan

ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(f_{FRAME})=60Hz
4'h0	Setting inhibited	–
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTS[2:0]:

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[1:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
00	V63	V0	V63 and V0	Register Setting(DC1, DC0)
01	V0	V63	-	-
10	GND	GND	V63 and V0	Register Setting(DC1, DC0)
11	Hi-Z	Hi-Z	V63 and V0	Register Setting(DC1, DC0)

DIVE[1:0]: DIVE[1:0] is used to set division ratio of PCLK clock frequency when the DPI interface is selected.

The divided PCLK will be used as internal clock for the source driver pre-charge, VCOM equalizing, etc.

DIVE[1:0]	Division Ratio

		2'h0	1/1
		2'h1	1/2
		2'h2	1/4
		2'h3	1/8
Restriction	-		

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2
SW Reset	No change
HW Reset	SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2

8.2.56. Display_Timing_Setting for Normal/Partial Mode (C1h)

C1H	Display_Timing_Setting for Normal/Partial Mode													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1
1st Parameter	1	1	↑	0	0	0	0	BC0	0	0	DIV0[1]	DIV0[0]	10
2nd Parameter	1	1	↑	0	0	0	0	RTN0[4]	RTN0[3]	RTN0[2]	RTN0[1]	RTN0[0]	10
3rd Parameter	1	1	↑	0	BP0[7]	BP0[6]	BP0[5]	BP0[4]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	02
4th Parameter	1	1	↑	0	FP0[7]	FP0[6]	FP0[5]	FP0[4]	FP0[3]	FP0[2]	FP0[1]	FP0[0]	02
Description	**BC0**: BC0 is used to select VCOM liquid crystal drive waveform. BC0 = 0: Frame inversion waveform is selected. BC0 = 1: Line inversion waveform is selected. **DIV0[1:0]**: DIV0[1:0] is used to set division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed.													

The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.

DIV0[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]

fosc. : internal oscillator frequency

clocks per line : RTNn setting

division ratio: DIVn setting

Line: total driving line number

BP: back porch line number

FP: front porch line number

RTN0[4:0]: RTN0[4:0] is used to set 1H (line) period.

RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line
5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

FP0[7:0], BP0[7:0]

FP0[7:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP0[7:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).

FP0[7:0] BP0[7:0]	Front and back porch period (line period)
8'h0	Setting prohibited
8'h1	Setting prohibited
8'h2	2 lines
8'h3	3 lines
8'h4	4 lines
8'h5	5 lines
8'h6	6 lines
…	…
8'h7E	126 lines
8'h7F	127 lines
8'h80	128 lines
Others	Setting Prohibited

Note to Setting BP0 and FP0

The condition in setting BP0 and FP0 bits are: BP0≧2 lines and FP0≧2 lines, FP0+BP0 ≤ 256 lines

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>BC0=1’h1, DIV0=2’h0, RTN0=5’h10, FP0=8’h2, BP=8’h2</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>BC0=1’h1, DIV0=2’h0, RTN0=5’h10, FP0=8’h2, BP0=8’h2</td></tr>
</table>
</td></tr>
</table>

8.2.57. Display_Timing_Setting for Idle Mode (C3h)

C3H	Display_Timing_Setting for Idle Mode													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3
1st Parameter	1	1	↑	0	0	0	0	BC2	0	0	DIV2[1]	DIV2[0]	00
2nd Parameter	1	1	↑	0	0	0	0	RTN2[4]	RTN2[3]	RTN2[2]	RTN2[1]	RTN2[0]	10
3rd Parameter	1	1	↑	0	BP2[7]	BP2[6]	BP2[5]	BP2[4]	BP2[3]	BP2[2]	BP2[1]	BP2[0]	02
4th Parameter	1	1	↑	0	FP2[7]	FP2[6]	FP2[5]	FP2[4]	FP2[3]	FP2[2]	FP0[1]	FP2[0]	02

Description

BC2: BC2 is used to select VCOM liquid crystal drive waveform.

BC2 = 0: Frame inversion waveform is selected.

BC2 = 1: Line inversion waveform is selected.

DIV2[1:0]: DIV2[1:0] is used to set division ratio of internal clock frequency.

The internal operation is synchronized with the frequency divided internal clock. When DIV2 setting is changed, the width of the reference clock for liquid crystal control signals is changed.

The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.

DIV2[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]

fosc. : internal oscillator frequency

clocks per line : RTNn setting

division ratio: DIVn setting

Line: total driving line number

BP: back porch line number

FP: front porch line number

RTN2[4:0]: RTN2[4:0] is used to set 1H (line) period.

RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line
5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

FP2[7:0], BP2[7:0]

FP2[7:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP2[7:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).

FP2[7:0] BP2[7:0]	Front and back porch period (line period)
8'h0	Setting prohibited
8'h1	Setting prohibited
8'h2	2 lines
8'h3	3 lines
8'h4	4 lines
8'h5	5 lines
8'h6	6 lines
…	…
8'h7E	126 lines
8'h7F	127 lines
8'h80	128 lines
Others	Setting Prohibited

Note to Setting BP2 and FP2

The condition in setting BP2 and FP2 bits are: BP2≧2 lines and FP2≧2 lines, FP2+BP2 ≤ 256 lines

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2
SW Reset	No change
HW Reset	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2

8.2.58. Source/VCOM/Gate Timing Setting (C4h)

C4H	Frame Rate Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	1	0	0	C4
1st Parameter	1	1	↑	0	0	SDT[2]	SDT[1]	SDT[0]	0	NOW[2]	NOW[1]	NOW[0]	11

Description

SDT[2:0]

The bit is used to set the source output alternating position in 1H period.

SDT[2:0]	Source Output Position
000	Setting prohibited
001	1 clock
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, and C3h).

NOW[2:0]

These bits set the gate output start position (non-overlap period).

NOW[2:0]	Gate Output Start Position
000	Setting prohibited
001	1 clock
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, and C3h).

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	NOW[2:0]=3'h1, SDT[2:0]=3'h1
SW Reset	No change
HW Reset	NOW[2:0]=3'h1, SDT[2:0]=3'h1

8.2.59. Frame Rate Control (C5h)

C5H	Frame Rate Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	1	0	1	C5
1st Parameter	1	1	↑	0	0	0	0	0	0	FRA[2]	FRA[1]	FRA[0]	04

Description

Set the frame frequency of display.

FRA[2:0]	Frame Rate (Hz)
3'h0	96
3'h1	88
3'h2	82
3'h3	76
3'h4	72 (default)
3'h5	67
3'h6	64
3'h7	60

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FRA=3'h4
SW Reset	No change
HW Reset	FRA=3'h4

8.2.60. Interface Control (C6h)

C6H	Interface Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	1	1	0	C6
1st Parameter	1	1	↑	x	SDA_EN	0	0	VSPL	HSPL	0	EPL	DPL	02

Description

DPL: Sets the signal polarity of the PCLK pin.

DPL = "0" The data is input on the rising edge of PCLK.

DPL = "1" The data is input on the falling edge of PCLK.

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB[17:0] is written when ENABLE = "0".

EPL = "1" The data DB[17:0] is written when ENABLE = "1".

HSPL: Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

SDA_EN: DBI type C interface selection

SDA_EN = "0", DIN and DOUT pins are used for DBI type C interface mode.

SDA_EN = "1", DIN/SDA pin is used for DBI type C interface mode and DOUT pin is not used.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0
SW Reset	No change
HW Reset	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0

8.2.61. Gamma Setting (C8h)

C8H	Gamma Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	1	0	0	0	C8
1st Parameter	1	1	↑	x	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	44
2nd Parameter	1	1	↑	x	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	44
3rd Parameter	1	1	↑	x	0	KP5[2]	KP5[1]	KP5[0]	0	KP4[2]	KP4[1]	KP4[0]	44
4th Parameter	1	1	↑	x	0	RP1[2]	RP1[1]	RP1[0]	0	RP0[2]	RP0[1]	RP0[0]	44
5th Parameter	1	1	↑	x	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	08
6th Parameter	1	1	↑	x	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	10
7th Parameter	1	1	↑	x	0	KN1[2]	KN1[1]	KN1[0]	0	KN0[2]	KN0[1]	KN0[0]	44
8th Parameter	1	1	↑	x	0	KN3[2]	KN3[1]	KN3[0]	0	KN2[2]	KN2[1]	KN2[0]	44
9th Parameter	1	1	↑	x	0	KN5[2]	KN5[1]	KN5[0]	0	KN4[2]	KN4[1]	KN4[0]	44
10th Parameter	1	1	↑	x	0	RN1[2]	RN1[1]	RN1[0]	0	RN0[2]	RN0[1]	RN0[0]	44
11th Parameter	1	1	↑	x	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	08
12th Parameter	1	1	↑	x	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	10

Description

KP5-0[2:0] : γ fine adjustment register for positive polarity

RP1-0[2:0] : γ gradient adjustment register for positive polarity

VRP1-0[4:0] : γ amplitude adjustment register for positive polarity

KN5-0[2:0] : γ fine adjustment register for negative polarity

RN1-0[2:0] : γ gradient adjustment register for negative polarity

VRN1-0[4:0] : γ amplitude adjustment register for negative polarity

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	KPx/KNx[2:0]=3'h4, RPx/RNx[2:0]=3'h4, VRP0/VRN0[3:0]=4'h8, VRP1/VRN1[4:0]=5'h10
SW Reset	No Change
HW Reset	KPx/KNx[2:0]=3'h4, RPx/RNx[2:0]=3'h4, VRP0/VRN0[3:0]=4'h8, VRP1/VRN1[4:0]=5'h10

8.2.62. Gamma Setting for Red/Blue Color (C9h)

C9h	Gamma Setting for Red Color												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	1	0	0	1	C9
1st Parameter	1	1	↑	x	0	0	0	0	RV0[3]	RV0[2]	RV0[1]	RV0[0]	00
2nd Parameter	1	1	↑	x	0	0	0	0	RV1[3]	RV1[2]	RV1[1]	RV1[0]	00
3rd Parameter	1	1	↑	x	0	0	0	0	RV2[3]	RV2[2]	RV2[1]	RV2[0]	00
4th Parameter	1	1	↑	x	0	0	0	0	RV3[3]	RV3[2]	RV3[1]	RV3[0]	00
…	…	…	…	…	…	…	…	…	…	…	…	…	…
61th Parameter	1	1	↑	x	0	0	0	0	RV60[3]	RV60[2]	RV60[1]	RV60[0]	00
62th Parameter	1	1	↑	x	0	0	0	0	RV61[3]	RV61[2]	RV61[1]	RV61[0]	00
63th Parameter	1	1	↑	x	0	0	0	0	RV62[3]	RV62[2]	RV62[1]	RV62[0]	00
64th Parameter	1	1	↑	x	0	0	0	0	RV63[3]	RV63[2]	RV63[1]	RV63[0]	00
65th Parameter	1	1	↑	x	0	0	0	0	BV0[3]	BV0[2]	BV0[1]	BV0[0]	00
66th Parameter	1	1	↑	x	0	0	0	0	BV1[3]	BV1[2]	BV1[1]	BV1[0]	00
67th Parameter	1	1	↑	x	0	0	0	0	BV2[3]	BV2[2]	BV2[1]	BV2[0]	00
68th Parameter	1	1	↑	x	0	0	0	0	BV3[3]	BV3[2]	BV3[1]	BV3[0]	00
…	…	…	…	…	…	…	…	…	…	…	…	…	…
125th Parameter	1	1	↑	x	0	0	0	0	BV60[3]	BV60[2]	BV60[1]	BV60[0]	00
126th Parameter	1	1	↑	x	0	0	0	0	BV61[3]	BV61[2]	BV61[1]	BV61[0]	00
127th Parameter	1	1	↑	x	0	0	0	0	BV62[3]	BV62[2]	BV62[1]	BV62[0]	00
128th Parameter	1	1	↑	x	0	0	0	0	BV63[3]	BV63[2]	BV63[1]	BV63[0]	00

Description

This register is used to fine tune the red color gamma mapping.

RVn[3:0] n=1~32	Red color gamma level (relative to green color gamma level)
4'h0	+0
4'h1	+1
4'h2	+2
4'h3	+3
4'h4	+4
4'h5	+5
4'h6	+6
4'h7	+7

RVn[3:0] n=1~32	Red color gamma level (relative to green color gamma level)
4'h8	-1
4'h9	-2
4'h10	-3
4'h11	-4
4'h12	-5
4'h13	-6
4'h14	-7
4'h15	-8

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	All the parameters are 00h
SW Reset	No change
HW Reset	All the parameters are 00h

8.2.63. Power_Setting (D0h)

D0H	Power_Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0
1st Parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	07
2nd Parameter	1	1	↑	x	0	PON	0	0	0	BT[2]	BT[1]	BT[0]	44
3rd Parameter	1	1	↑	x	VCIRE	0	0	VRH[4]	VRH[3]	VRH[2]	VRH[1]	VRH[0]	8C

Description

VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1.

VC[2:0]	Vci1 voltage
3'h0	0.95 x Vci
3'h1	090 x Vci
3'h2	0.85 x Vci
3'h3	0.80 x Vci
3'h4	0.75 x Vci
3'h5	0.70 x Vci
3'h6	Disable
3'h7	1.0 x Vci

BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci1.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5
3'h1	Vci1 x 2	- Vci1		- Vci1 x 4
3'h2				- Vci1 x 3
3'h3	Vci1 x 2	- Vci1	Vci1 x 5	- Vci1 x 5
3'h4				- Vci1 x 4
3'h5				- Vci1 x 3
3'h6	Vci1 x 2	- Vci1	Vci1 x 4	- Vci1 x4
3'h7				- Vci1 x3

Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
Note 2: Set following voltages within the respective ranges:
DDVDH = 6.0V (max)
VGH = 18.0V (max)
VGL= -12.5V (max)
VCL= -3.0V (max).

PON is used to control the operation to generate VGL.

PON=0: Halts the step-up operation to generate VGL.

PON=1: Starts the step-up operation to generate VGL.

VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.

VCIRE=0	External reference voltage Vci
VCIRE =1	Internal reference voltage 2.5V (**default**)

VRH[4:0]: Sets the factor to generate VREG1OUT from VCI

VRH[4:0]	VREG1OUT		VRH[4:0]	VREG1OUT
5'h0	Vci x 1.600		5'h0	2.5 x 1.600 = 4.0000
5'h1	Vci x 1.625		5'h1	2.5 x 1.625 = 4.0625
5'h2	Vci x 1.650		5'h2	2.5 x 1.650 = 4.1250
5'h3	Vci x 1.675		5'h3	2.5 x 1.675 = 4.1875
5'h4	Vci x 1.700		5'h4	2.5 x 1.700 = 4.2500
5'h5	Vci x 1.725		5'h5	2.5 x 1.725 = 4.3125
5'h6	Vci x 1.750		5'h6	2.5 x 1.750 = 4.3750
5'h7	Vci x 1.775		5'h7	2.5 x 1.775 = 4.4375
5'h8	Vci x 1.800		5'h8	2.5 x 1.800 = 4.5000
5'h9	Vci x 1.825		5'h9	2.5 x 1.825 = 4.5625
5'hA	Vci x 1.850		5'hA	2.5 x 1.850 = 4.6250
5'hB	Vci x 1.875		5'hB	2.5 x 1.875 = 4.6875
5'hC	Vci x 1.900		5'hC	2.5 x 1.900 = 4.7500
5'hD	Vci x 1.925		5'hD	2.5 x 1.925 = 4.8125
5'hE	Vci x 1.950		5'hE	2.5 x 1.950 = 4.8750
5'hF	Vci x 1.975		5'hF	2.5 x 1.975 = 4.9375
5'h10	Setting prohibited		5'h10	2.5 x 2.000 = 5.0000
5'h11	Setting prohibited		5'h11	2.5 x 2.025 = 5.0625
5'h12	Setting prohibited		5'h12	2.5 x 2.050 = 5.1250
5'h13	Setting prohibited		5'h13	2.5 x 2.075 = 5.1875
5'h14	Setting prohibited		5'h14	2.5 x 2.100 = 5.2500
5'h15	Setting prohibited		5'h15	2.5 x 2.125 = 5.3125
5'h16	Setting prohibited		5'h16	2.5 x 2.150 = 5.3750
5'h17	Setting prohibited		5'h17	2.5 x 2.175 = 5.4375
5'h18	Setting prohibited		5'h18	2.5 x 2.200 = 5.5000
Others	Setting prohibited		Others	Setting prohibited

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC[2:0] and VRH[3:0] setting restriction: VREG1OUT ≦ (DDVDH - 0.25)V.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VC[2:0]=3'h7, BT[2:0]=3'h4, PON=1'h1; VRH[3:0]=4'hC, VCIRE=1'h1
SW Reset	No change
HW Reset	VC[2:0]=3'h7, BT[2:0]=3'h4, PON=1'h1; VRH[3:0]=4'hC, VCIRE=1'h1

8.2.64. VCOM Control (D1h)

D1H	VCOM Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	**SEL VCM**	00
2nd Parameter	1	1	↑	x	0	VCM[6]	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	66
3rd Parameter	1	1	↑	x	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	19

Description

VCM [6:0] is used to set factor to generate VCOMH voltage from the reference voltage VREG1OUT.

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
7'h00	VREG x 0.492	7'h40	VREG x 0.748
7'h01	VREG x 0.496	7'h41	VREG x 0.752
7'h02	VREG x 0.500	7'h42	VREG x 0.756
7'h03	VREG x 0.504	7'h43	VREG x 0.760
7'h04	VREG x 0.508	7'h44	VREG x 0.764
7'h05	VREG x 0.512	7'h45	VREG x 0.768
7'h06	VREG x 0.516	7'h46	VREG x 0.772
7'h07	VREG x 0.520	7'h47	VREG x 0.776
7'h08	VREG x 0.524	7'h48	VREG x 0.780
7'h09	VREG x 0.528	7'h49	VREG x 0.784
7'h0A	VREG x 0.532	7'h4A	VREG x 0.788
7'h0B	VREG x 0.536	7'h4B	VREG x 0.792
7'h0C	VREG x 0.540	7'h4C	VREG x 0.796
7'h0D	VREG x 0.544	7'h4D	VREG x 0.800
7'h0E	VREG x 0.548	7'h4E	VREG x 0.804
7'h0F	VREG x 0.552	7'h4F	VREG x 0.808
7'h10	VREG x 0.556	7'h50	VREG x 0.812
7'h11	VREG x 0.560	7'h51	VREG x 0.816
7'h12	VREG x 0.564	7'h52	VREG x 0.820
7'h13	VREG x 0.568	7'h53	VREG x 0.824
7'h14	VREG x 0.572	7'h54	VREG x 0.828
7'h15	VREG x 0.576	7'h55	VREG x 0.832
7'h16	VREG x 0.580	7'h56	VREG x 0.836
7'h17	VREG x 0.584	7'h57	VREG x 0.840
7'h18	VREG x 0.588	7'h58	VREG x 0.844
7'h19	VREG x 0.592	7'h59	VREG x 0.848
7'h1A	VREG x 0.596	7'h5A	VREG x 0.852
7'h1B	VREG x 0.600	7'h5B	VREG x 0.856
7'h1C	VREG x 0.604	7'h5C	VREG x 0.860
7'h1D	VREG x 0.608	7'h5D	VREG x 0.864

		7'h1E	VREG x 0.612	7'h5E	VREG x 0.868
		7'h1F	VREG x 0.616	7'h5F	VREG x 0.872
		7'h20	VREG x 0.620	7'h60	VREG x 0.876
		7'h21	VREG x 0.624	7'h61	VREG x 0.880
		7'h22	VREG x 0.628	7'h62	VREG x 0.884
		7'h23	VREG x 0.632	7'h63	VREG x 0.888
		7'h24	VREG x 0.636	7'h64	VREG x 0.892
		7'h25	VREG x 0.640	7'h65	VREG x 0.896
		7'h26	VREG x 0.644	7'h66	VREG x 0.900
		7'h27	VREG x 0.648	7'h67	VREG x 0.904
		7'h28	VREG x 0.652	7'h68	VREG x 0.908
		7'h29	VREG x 0.656	7'h69	VREG x 0.912
		7'h2A	VREG x 0.660	7'h6A	VREG x 0.916
		7'h2B	VREG x 0.664	7'h6B	VREG x 0.920
		7'h2C	VREG x 0.668	7'h6C	VREG x 0.924
		7'h2D	VREG x 0.672	7'h6D	VREG x 0.928
		7'h2E	VREG x 0.676	7'h6E	VREG x 0.932
		7'h2F	VREG x 0.680	7'h6F	VREG x 0.936
		7'h30	VREG x 0.684	7'h70	VREG x 0.940
		7'h31	VREG x 0.688	7'h71	VREG x 0.944
		7'h32	VREG x 0.692	7'h72	VREG x 0.948
		7'h33	VREG x 0.696	7'h73	VREG x 0.952
		7'h34	VREG x 0.700	7'h74	VREG x 0.956
		7'h35	VREG x 0.704	7'h75	VREG x 0.960
		7'h36	VREG x 0.708	7'h76	VREG x 0.964
		7'h37	VREG x 0.712	7'h77	VREG x 0.968
		7'h38	VREG x 0.716	7'h78	VREG x 0.972
		7'h39	VREG x 0.720	7'h79	VREG x 0.976
		7'h3A	VREG x 0.724	7'h7A	VREG x 0.980
		7'h3B	VREG x 0.728	7'h7B	VREG x 0.984
		7'h3C	VREG x 0.732	7'h7C	VREG x 0.988
		7'h3D	VREG x 0.736	7'h7D	VREG x 0.992
		7'h3E	VREG x 0.740	7'h7E	VREG x 0.996
		7'h3F	VREG x 0.744	7'h7F	VREG x 1.000

VDV[4:0] is used to set the VCOM alternating amplitude in the range of VREG1OUT x 0.70 to VREG1OUT x 1.32.

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h04	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h05	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'h0B	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24
5'h0C	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26
5'h0D	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28
5'h0E	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30
5'h0F	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32

Set VDV[4:0] to let VCOM amplitude less than 6V.

SELVCM: Selection the VCM setting. When the NV memory is programmed, the SELVCM will be set as '1' automatically.

SELVCM =0	Register D1h for VCM setting
SELVCM =1	NV Memory selected for VCM setting

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VCM[5:0]=6'h00, VDV[4:0]=5'h00, SELVCM=1'h0
SW Reset	No change
HW Reset	VCM[5:0]=6'h00, VDV[4:0]=5'h00, SELVCM=1'h0

8.2.65. Power_Setting for Normal Mode (D2h)

D2H	Power_Setting for Normal Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	1	0	D2
1st Parameter	1	1	↑	x	0	0	0	0	0	AP0[2]	AP0[1]	AP0[0]	01
2nd Parameter	1	1	↑	x	0	DC10[2]	DC10[1]	DC10[0]	0	DC00[2]	DC00[1]	DC00[0]	44

Description

AP0[2:0]

AP0 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'h0	Halt operation	Halt operation
3'h1	1.00	1.00
3'h2	1.00	0.75
3'h3	1.00	0.50
3'h4	0.75	1.00
3'h5	0.75	0.75
3'h6	0.75	0.50
3'h7	0.50	0.50

DC00[2:0], DC10[2:0]

DC00/DC10 are used to select the charge-pump frequency of circuit and circuit2.

DC00[1:0]	Step-up circuit 1 clock frequency (fDCDC1)
2'h0	Fosc
2'h1	Fosc / 2
2'h2	Fosc / 4
2'h3	Fosc / 8
2'h4	Fosc / 16
2'h5	Fosc / 32
2'h6	Fosc / 64
2'h7	Halt step-up circuit 1

DC10[1:0]	Step-up circuit 2 clock frequency (fDCDC2)
2'h0	Fosc / 16
2'h1	Fosc / 32
2'h2	Fosc / 64
2'h3	Fosc / 128
2'h4	Fosc / 256
2'h5	Fosc / 512
2'h6	Setting inhibited
2'h7	Halt step-up circuit 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	AP0[2:0]=3'h1, DC10[2:0]=3'h4, DC00[2:0]=3'h4
SW Reset	No change
HW Reset	AP0[2:0]=3'h1, DC10[2:0]=3'h4, DC00[2:0]=3'h4

8.2.66. Power_Setting for Partial Mode (D3h)

D3H	Power_Setting for Partial Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3
1st Parameter	1	1	↑	x	0	0	0	0	0	AP1[2]	AP1[1]	AP1[0]	01
2nd Parameter	1	1	↑	x	0	DC11[2]	DC11[1]	DC11[0]	0	DC01[2]	DC01[1]	DC01[0]	44

Description

AP1[2:0]

AP1 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP1=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP1[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'h0	Halt operation	Halt operation
3'h1	1.00	1.00
3'h2	1.00	0.75
3'h3	1.00	0.50
3'h4	0.75	1.00
3'h5	0.75	0.75
3'h6	0.75	0.50
3'h7	0.50	0.50

DC01[2:0], DC11[2:0]

DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.

DC01[1:0]	Step-up circuit 1 clock frequency (fDCDC1)
2'h0	Fosc
2'h1	Fosc / 2
2'h2	Fosc / 4
2'h3	Fosc / 8
2'h4	Fosc / 16
2'h5	Fosc / 32
2'h6	Fosc / 64
2'h7	Halt step-up circuit 1

DC11[1:0]	Step-up circuit 2 clock frequency (fDCDC2)
2'h0	Fosc / 16
2'h1	Fosc / 32
2'h2	Fosc / 64
2'h3	Fosc / 128
2'h4	Fosc / 256
2'h5	Fosc / 512
2'h6	Setting inhibited
2'h7	Halt step-up circuit 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4
SW Reset	No change
HW Reset	AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4

8.2.67. Power_Setting for Idle Mode (D4h)

D4H	Power_Setting for Idle Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	1	0	0	D4
1st Parameter	1	1	↑	x	0	0	0	0	0	AP2[2]	AP2[1]	AP2[0]	01
2nd Parameter	1	1	↑	x	0	DC12[2]	DC12[1]	DC12[0]	0	DC02[2]	DC02[1]	DC02[0]	44

Description

AP2[2:0]

AP2 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP2=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'h0	Halt operation	Halt operation
3'h1	1.00	1.00
3'h2	1.00	0.75
3'h3	1.00	0.50
3'h4	0.75	1.00
3'h5	0.75	0.75
3'h6	0.75	0.50
3'h7	0.50	0.50

DC02[2:0], DC12[2:0]

DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.

DC02[1:0]	Step-up circuit 1 clock frequency (fDCDC1)
2'h0	Fosc
2'h1	Fosc / 2
2'h2	Fosc / 4
2'h3	Fosc / 8
2'h4	Fosc / 16
2'h5	Fosc / 32
2'h6	Fosc / 64
2'h7	Halt step-up circuit 1

DC12[1:0]	Step-up circuit 2 clock frequency (fDCDC2)
2'h0	Fosc / 16
2'h1	Fosc / 32
2'h2	Fosc / 64
2'h3	Fosc / 128
2'h4	Fosc / 256
2'h5	Fosc / 512
2'h6	Setting inhibited
2'h7	Halt step-up circuit 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	AP2[2:0]=3'h1, DC12[2:0]=3'h4, DC02[2:0]=3'h4
SW Reset	No change
HW Reset	AP2[2:0]=3'h1, DC11[2:0]=3'h4, DC02[2:0]=3'h4

8.2.68. Gate Voltage Level Control (D5h)

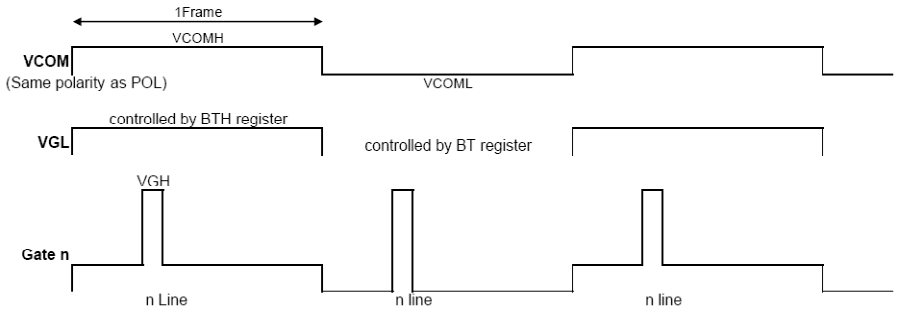
D5H	Gate Voltage Level Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	1	0	1	D5
1st Parameter	1	1	↑	x	0	0	0	VGL_INV_ON	0	BTH[2]	BTH[1]	BTH[0]	00

Description

VGL_INV_ON

When VGL_INV_ON=1, the wave form of VGL is as shown as below. And if VGL_INV_ON=0, the VGL waveform is traditional one (only one voltage level)!

VGL_INV_ON	Description
0	Normal VGL waveform
1	Specified VGL waveform



BTH[2:0]	VGL
3'h0	- Vci1 x 5
3'h1	- Vci1 x 4
3'h2	- Vci1 x 3
3'h3	- Vci1 x 5
3'h4	- Vci1 x 4
3'h5	- Vci1 x 3
3'h6	- Vci1 x4
3'h7	- Vci1 x3

BTH： Uses same multiple ratio table as BT register in RD0h (same setting as the table below)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	VGL_INV_ON=0, BTH[2:0]=3'h0.
SW Reset	No change
HW Reset	VGL_INV_ON=0, BTH[2:0]=3'h0.

8.2.69. NV Memory Write (E0h)

E0H	NV Memory Write												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	0	0	E0
1st Parameter	1	1	↑	x	VM_D [7]	VM_D [6]	VM_D [5]	VM_D [4]	VM_D [3]	VM_D [2]	VM_D [1]	VM_D [0]	00
Description	This command is used to program the NV memory data. **VM_D[7:0]:** Use to write the data (including VCM and ID code) into the NV memory data.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VM_D[7:0]=8'h00
SW Reset	No change
HW Reset	VM_D[7:0]=8'h00

8.2.70. NV Memory Control (E1h)

E1H	NV Memory Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	0	1	E1
1st Parameter	1	1	↑	x	0	0	ID_ PGM_EN	VCM_ PGM_EN	0	0	0	0	00

Description

This command is used to control the NV memory programming.

VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'.

When the VCOMH NV memory is programmed, the SELVCM bit of RD1h register will be set as '1' automatically.

ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'.

ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection
0	0	NV Memory programming disabled
0	1	VCM (VCOMH) NV Memory programming enable
1	0	ID code NV Memory programming enable
1	1	Setting Prohibited

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0
SW Reset	No change
HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0

8.2.71. NV Memory Status Read (E2h)

E2H	NV Memory Status Read												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	1	0	E2
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	0	0	0	0	0	0	PGM_ CNT1	PGM_ CNT0	00
3rd Parameter	1	↑	1	x	0	NV_ VCM[6]	NV_ VCM[5]	NV_ VCM[4]	NV_ VCM[3]	NV_ VCM[2]	NV_ VCM[1]	NV_ VCM[0]	00

Description

PGM_CNT[1:0]: NV memory programmed record. The bit will increase "+1" automatically when writing the NV_VCM [5:0].

PGM_CNT[1:0]	Description
00	NV Memory clean
01	NV Memory programmed 1 time
10	NV Memory programmed 2 times
11	NV Memory programmed 3 times

These bits are read only.

NV_VCM [6:0]: NV memory VCM data read value. These bits are read only.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0
SW Reset	No change
HW Reset	PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0

8.2.72. NV Memory Protection (E3h)

E3H	NV Memory Protection												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	--	1	1	1	0	0	0	1	1	E3
1st Parameter	1	1	↑	--	KEY [15]	KEY [14]	KEY [13]	KEY [12]	KEY [11]	KEY [10]	KEY [9]	KEY [8]	00
2nd Parameter	1	1	↑	--	KEY [7]	KEY [6]	KEY [5]	KEY [4]	KEY [3]	KEY [2]	KEY [1]	KEY [0]	00
Description	**KEY[15:0]:** NV memory programming protection key. When writing OTP data C8h, this register must be set as 0xAA55 to enable OTP programming. If C8h register is not written with 0xAA55, NV Memory programming will fail.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	KEY[15:0]=16'h0000
SW Reset	No change
HW Reset	KEY[15:0]=16'h0000

8.2.73. Device Code Read (EFh)

BFH	Device Code Read												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	1	1	0	1	1	1	1	EF
1st parameter	0	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	0	↑	1	xx	0	0	0	0	0	0	1	0	02
3rd parameter	0	↑	1	xx	0	0	0	0	0	1	0	0	04
4th parameter	0	↑	1	xx	1	0	0	1	0	1	0	0	93
5th parameter	0	↑	1	xx	1	0	0	0	0	0	0	1	27
6th parameter	0	↑	1	xx	1	1	1	1	1	1	1	1	FF
Description	1st parameter : dummy read 2nd parameter : MIPI Alliance code 3rd parameter : MIPI Alliance code 4th parameter : Device ID code of ILI9327 5th parameter : Device ID code of ILI9327 6th parameter : Exit code (FFh)												
Register Availability													

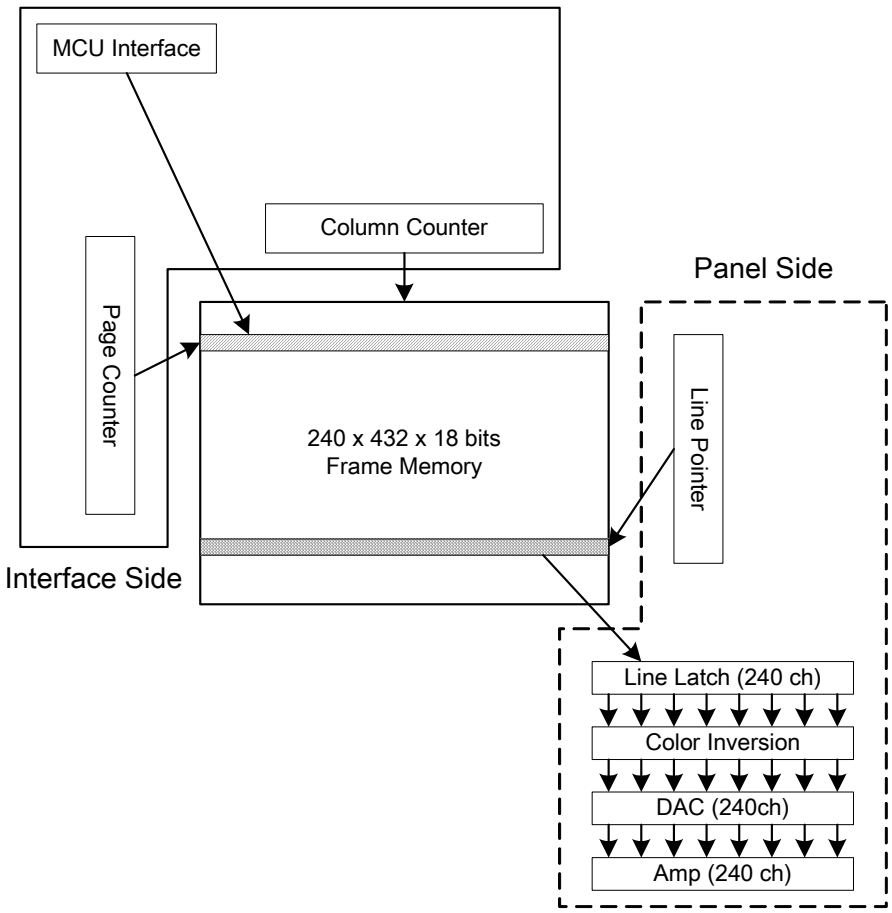
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

9. Display Data RAM

9.1. Configuration

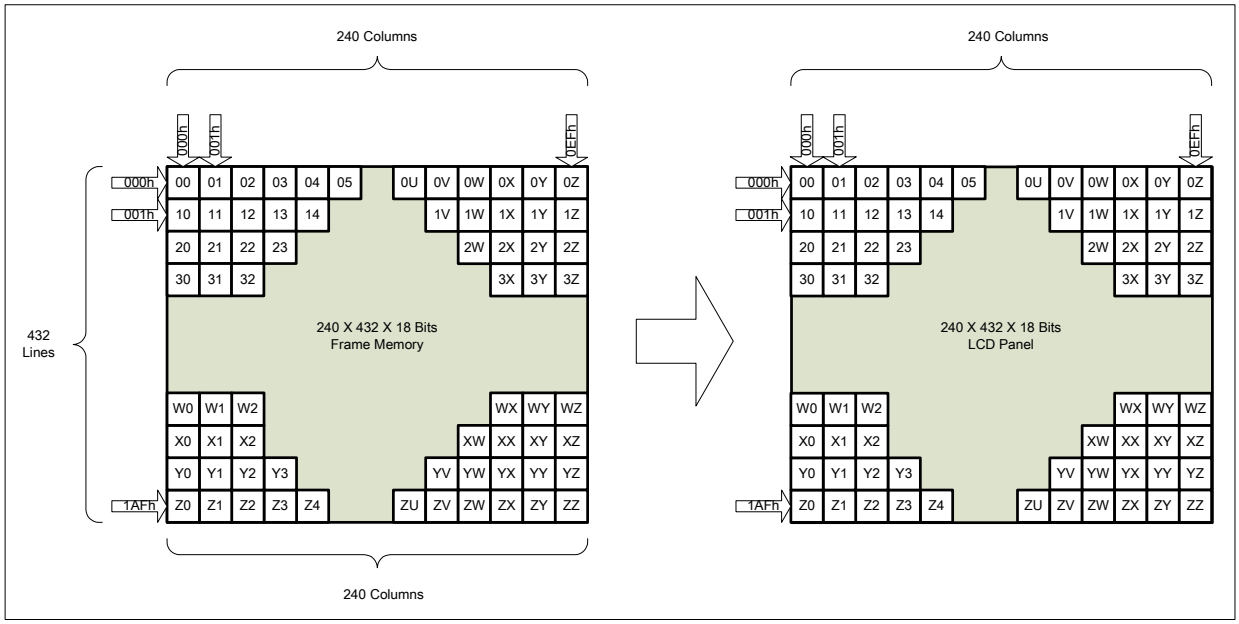
The display data RAM stores display dots and consists of 1,866,240bits (240 x 18 x 432 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



9.2. **Memory to Display Address Mapping**

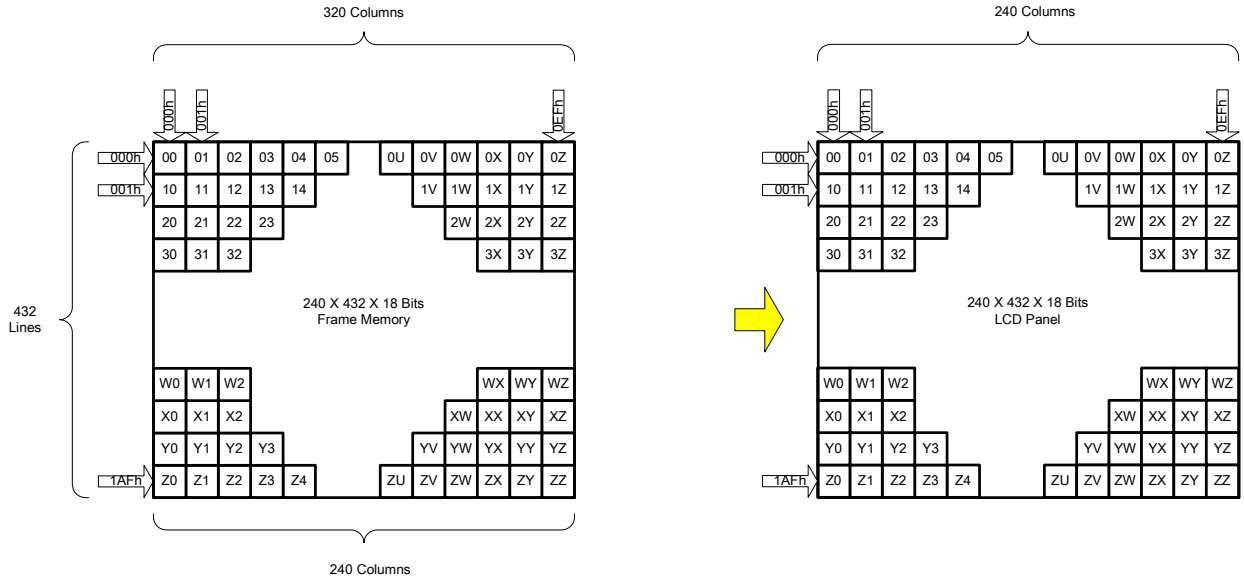
In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



9.3. **Vertical Scroll Mode**

There is a vertical scrolling mode, which is described by the commands “set_scroll_area”(33h) and “set_scroll_start”(37h).

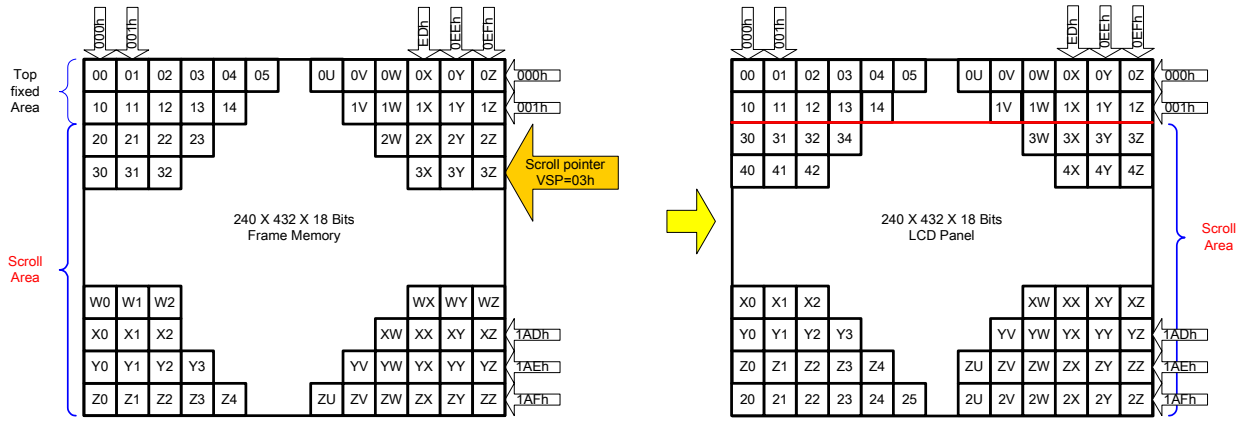
(1)Normal Display On or Partial Mode On, Vertical Scroll Off



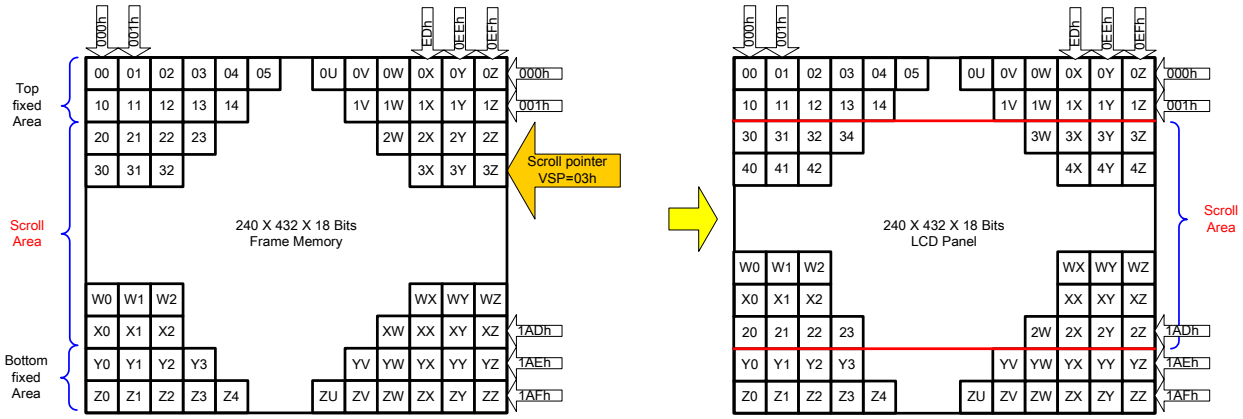
(2) Vertical Scroll Mode

“set_scroll_area(33h)”and ”set_scroll_start(37h)” setting define the scroll area.

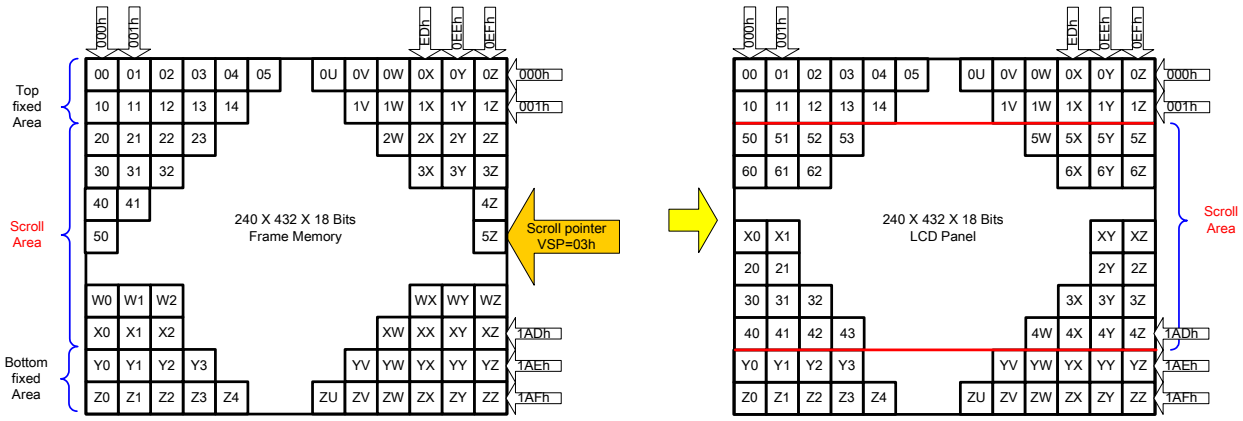
Example1: TFA=2, VSA=430, BFA=0 (set_address_mode(36h) B4=0), VSP=3



Example2: TFA=2,VSA=428,BFA=2 (set_address_mode(36h) B4=0), VSP=3



Example3: TFA=2,VSA=428,BFA=2 (set_address_mode(36h) B4=0), VSP=5

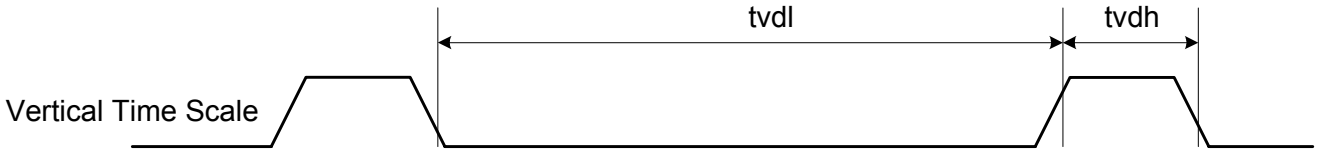


10. Tearing Effect Output

The tearing effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands.
The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

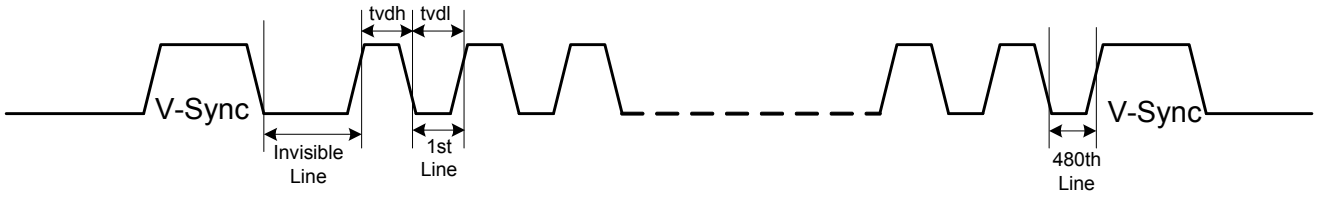
10.1. Tearing Effect Line Modes

Mode 1 (set_tear_on, TELOM=0) , the Tearing Effect Output signal consists of V-Sync information only:

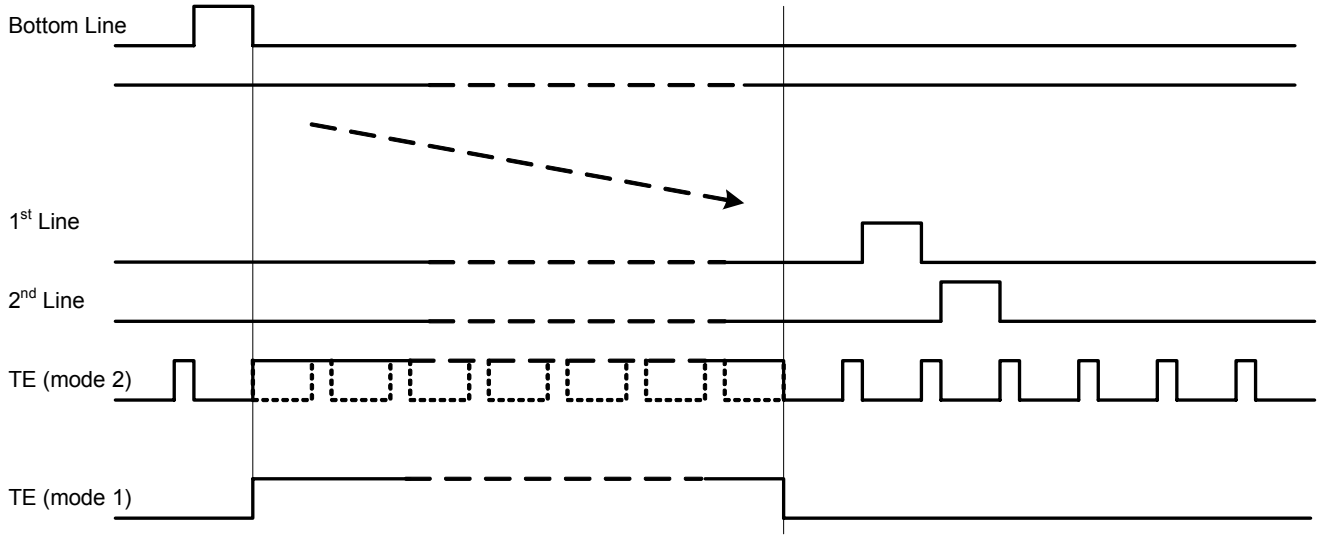


tvdh = The LCD display is not updated from the Frame Memory.
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2 (set_tear_on, TELOM=1), the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 432 H-sync pulses per field:



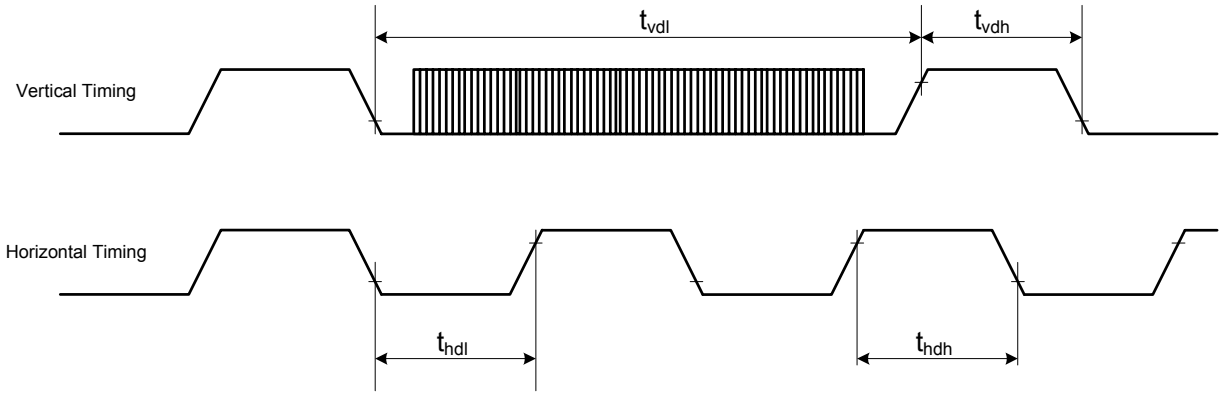
thdh = The LCD display is not updated from the Frame Memory.
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

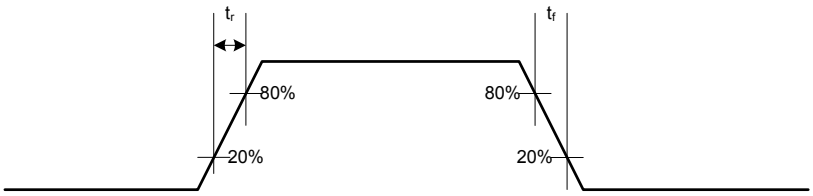


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	TBD		ms	
t_{vdh}	Vertical timing high duration	TBD		us	
t_{hdl}	Horizontal timing low duration	TBD		us	
t_{hdh}	Horizontal timing high duration	TBD		us	

Notes:

1. The timings in Table 8.3.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

TEON (35h)	TELOM (35h, 1st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

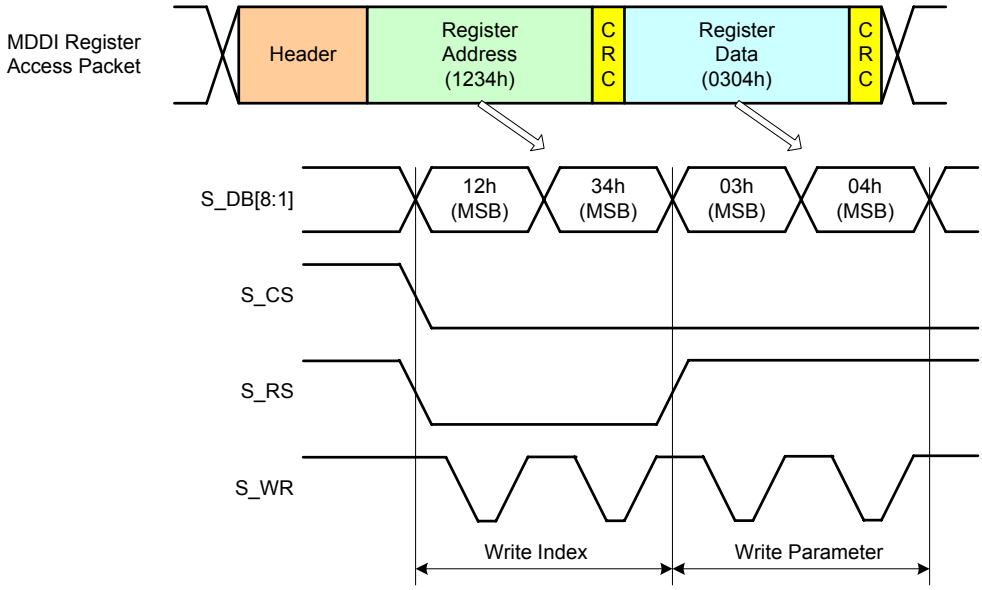
11. Sub-panel Control

TFT type sub panel timing

A. Register data transfer timing

If TFT type sub panel is selected (STN_EN=0), register setting is executed like below figure. Register data is transferred through S_DB[8:0] in 9/8 bit type. Please refer to the MDDI section for the register address direction to sub panel.

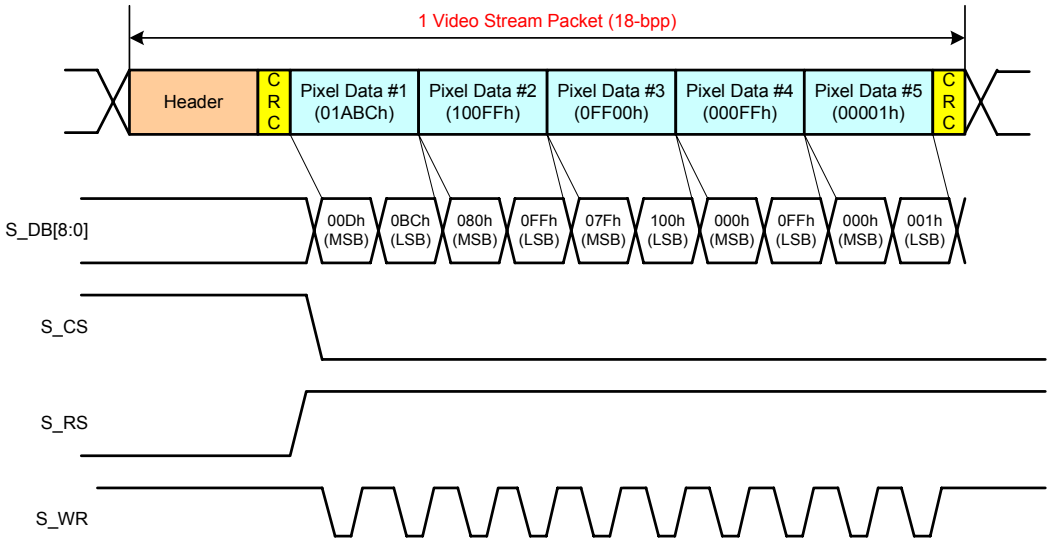
In this mode, data is transferred at two times. First transfer is MSB 8bit and second transfer is LSB 8bit.



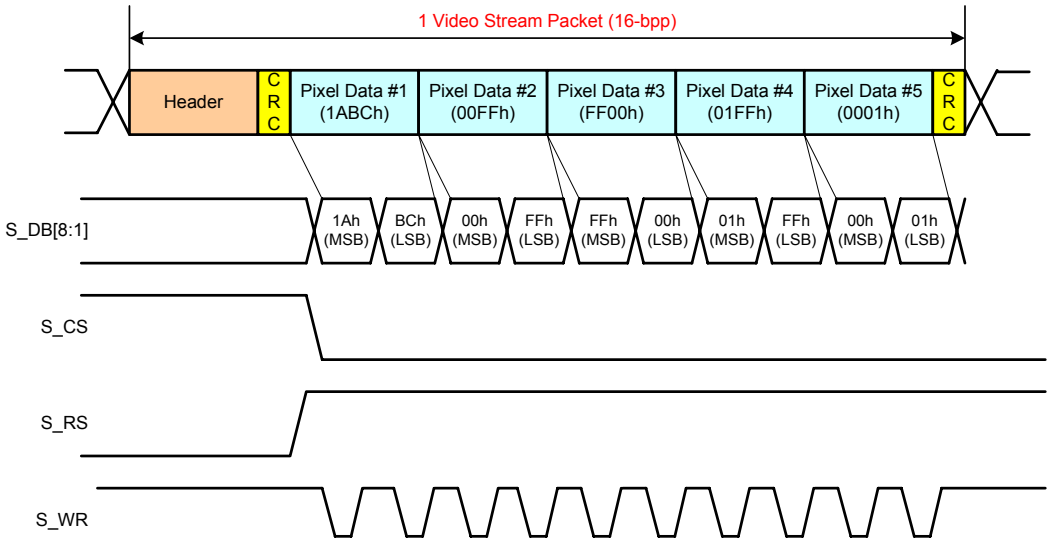
B. Video data transfer timing

In TFT type sub panel, the 9/8-bit mode is selected as setting SUB_IM register.

This figure shows 9-bit sub-panel data bus with 18-bpp video data transfer.



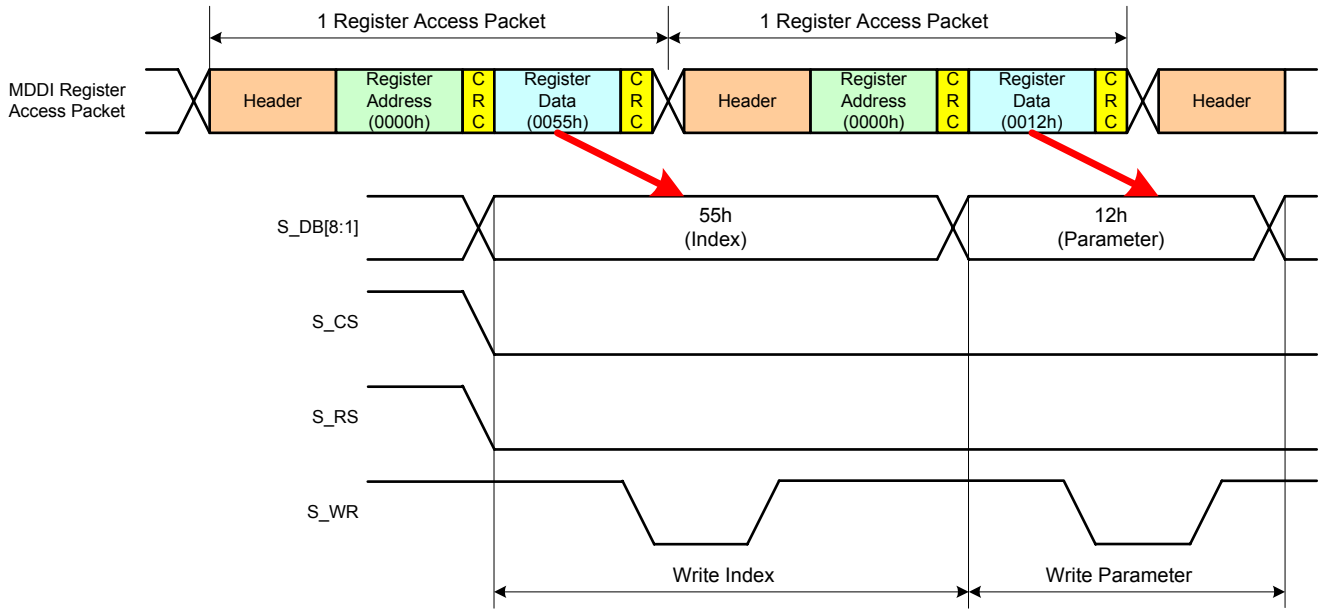
This figure shows 8-bit sub-panel data bus with 16-bpp video data transfer.



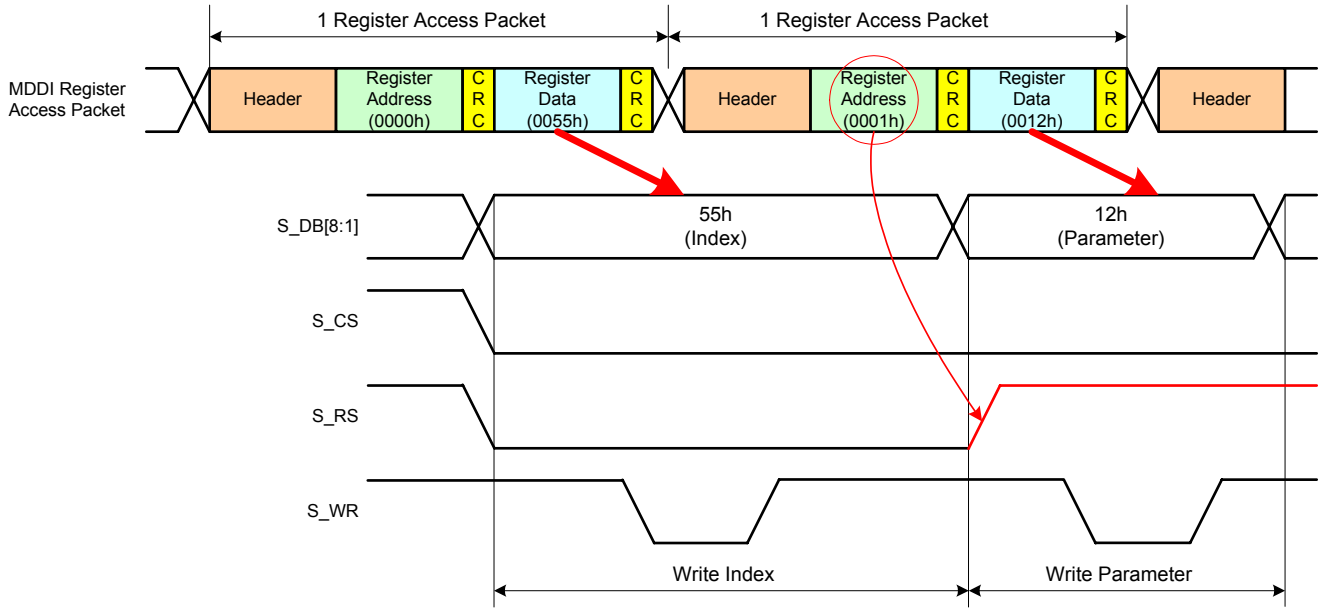
STN type sub panel timing

A. Register data transfer timing

This figure shows conventional type STN mode register data setting. Conventional type does not include parameter. Instruction type is only 8bit. To use STN type, STN_EN is set to “1”. In STN type, ILI9327 controls S_RS pin using register address[0] in register access packet. Register address[0] is “0”, then S_RS is set to “0”, and register address[0] is “1”, S_RS is set to “1”.



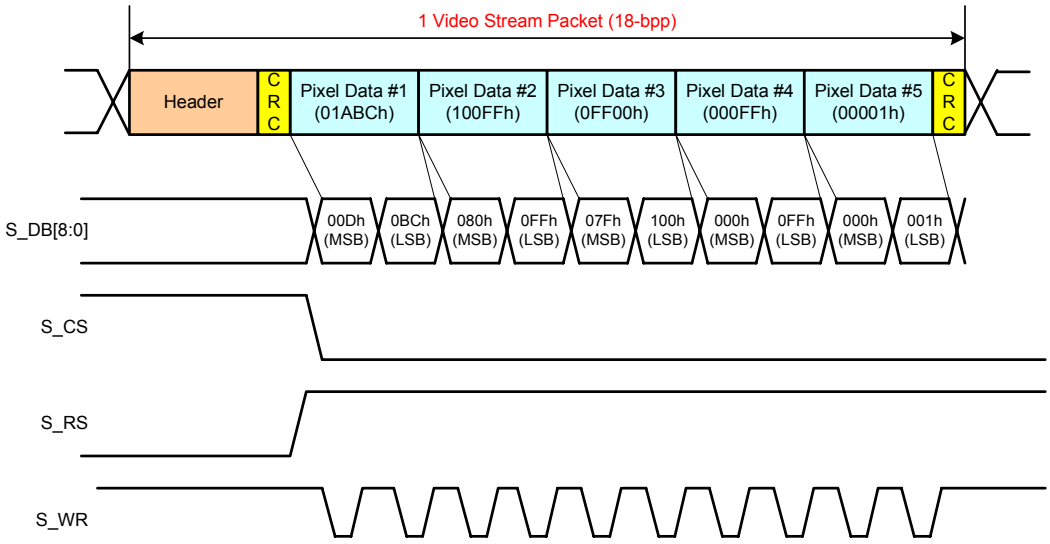
This type is used to include parameter. When instruction is transferred, S_RS is zero, and when parameter is transferred, S_RS is “1”. S_RS is controlled using register address[0] of register access packet.



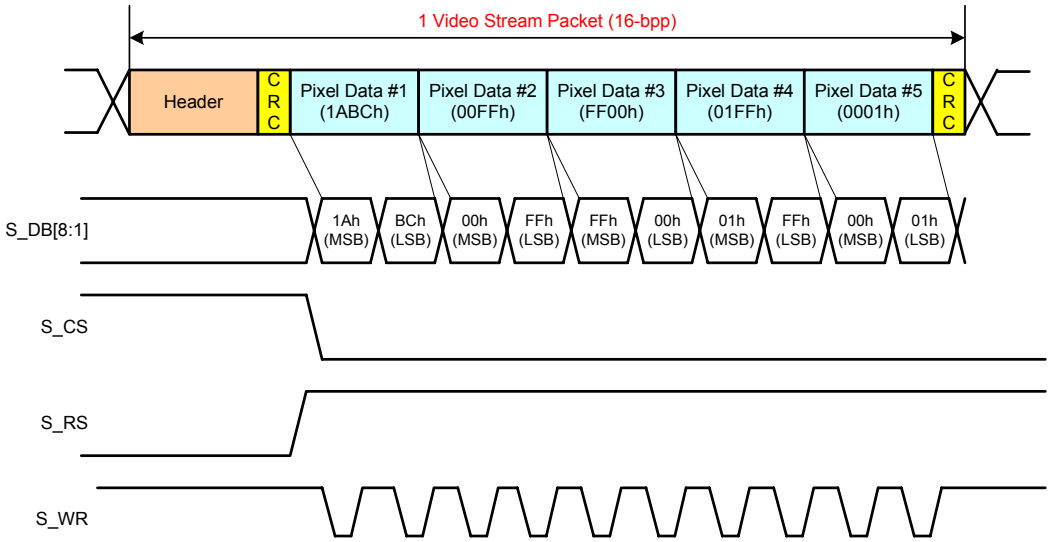
B. Video data transfer timing

In STN mode, video data start register (like 22H in TFT mode) generally is not necessary. But some STN type needs video data start register. If that type STN DDI is used, user has to set the register index.

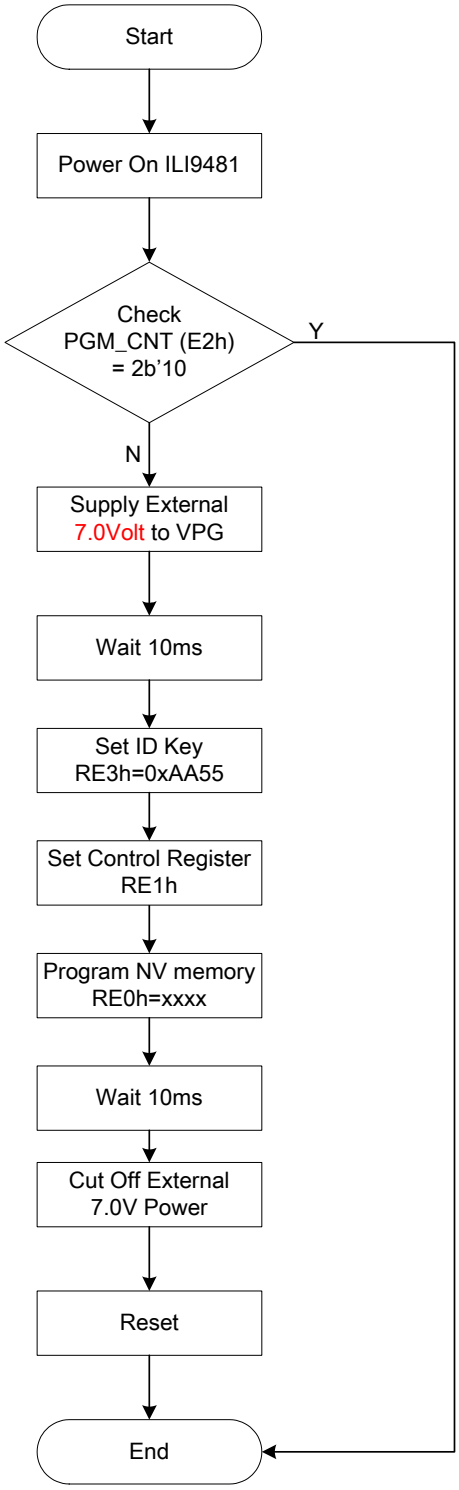
This figure shows STN 9 bit mode video data transfer.



This figure shows STN 8bit mode video data transfer. If STN video data is 16bit mode, data transfer is executed during 2 times. Fist transfer is MSB 8bits, and second is LSB 8bits.



12. NV Memory Programming Flow



13. Gamma Correction

ILI9327 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9327 available with liquid crystal panels of various characteristics.

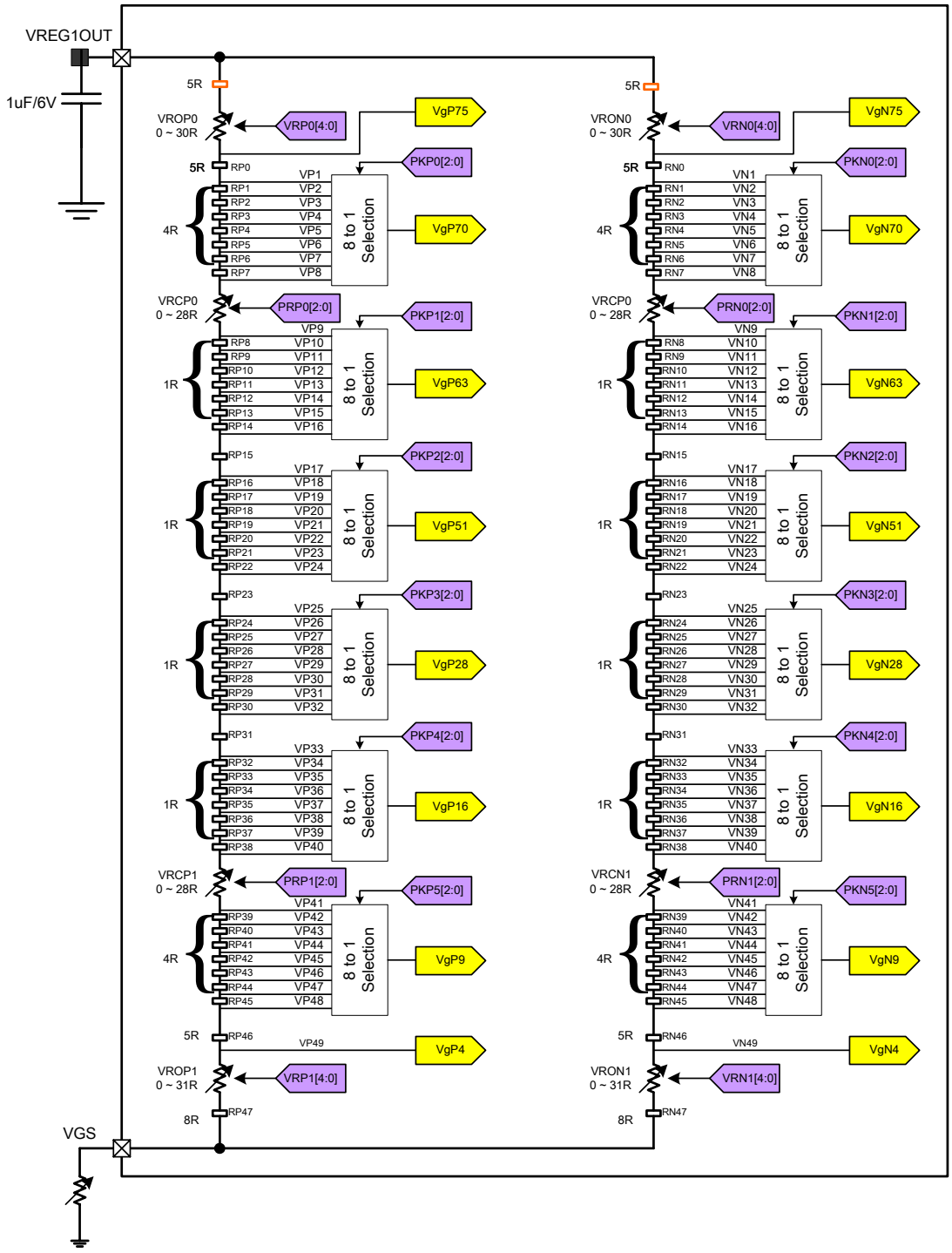
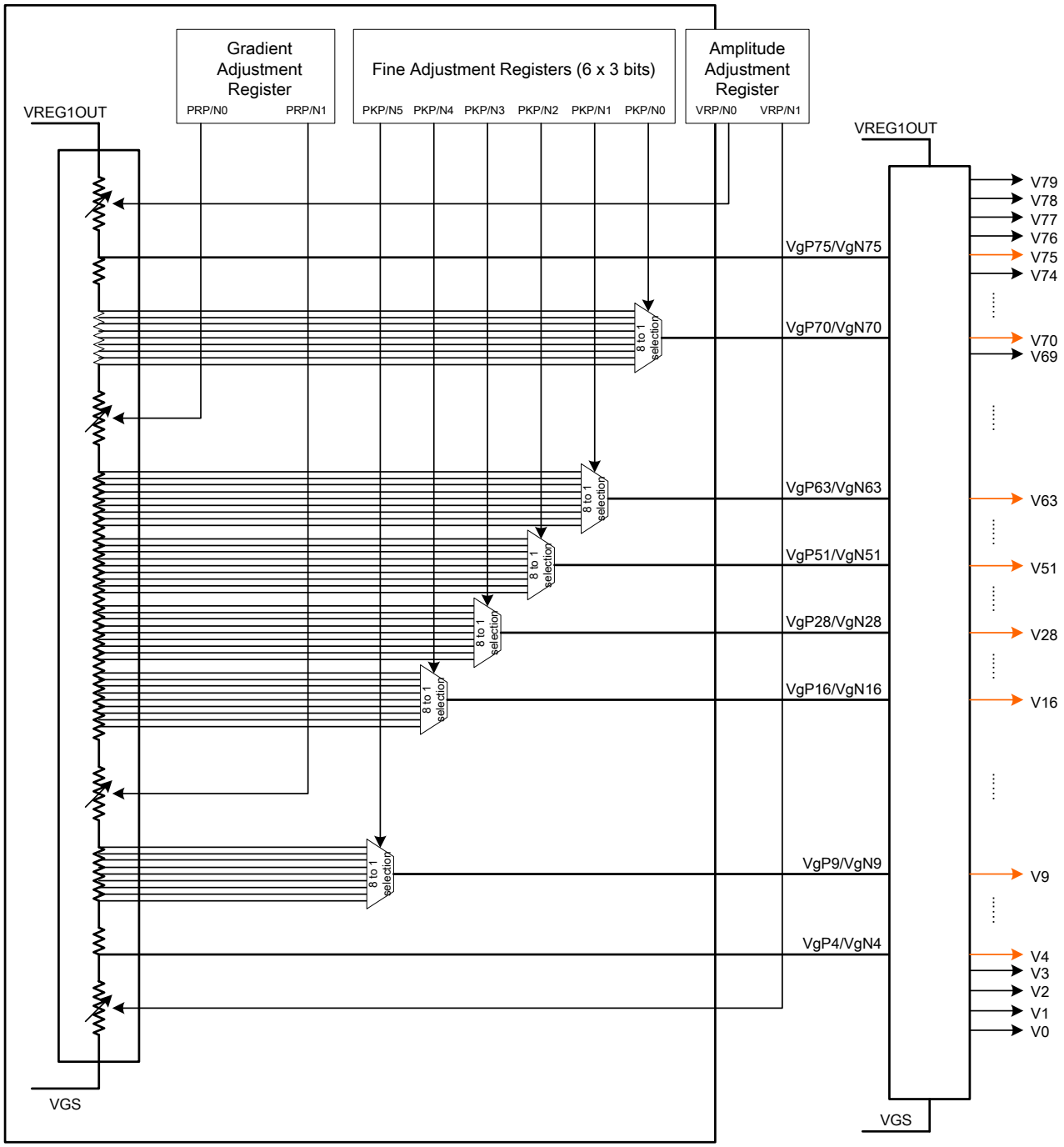


Figure 1 Grayscale Voltage Adjustment



14. Electrical Characteristics

14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9327 is used out of the absolute maximum ratings, the ILI9327 may be permanently damaged. To use the ILI9327 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9327 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage	IOVCC	V	-0.3 ~ + 4.6	1,
Power supply voltage	VCI - GND	V	-0.3 ~ + 4.6	2
Power supply voltage	DDVDH - GND	V	-0.3 ~ + 6.5	3
Power supply voltage	GND -VCL	V	-0.3 ~ + 4.6	4
Power supply voltage	DDVDH - VCL	V	-0.3 ~ + 9.0	
Power supply voltage	VGH - GND	V	-0.3 ~ + 18.5	
Power supply voltage	GND - VGL	V	-0.3 ~ + 18.5	
Power supply voltage	VGH - VGL	V	-0.3 ~ + 32	
Input voltage	Vt	V	-0.3 ~ IOVCC+ 0.3	
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

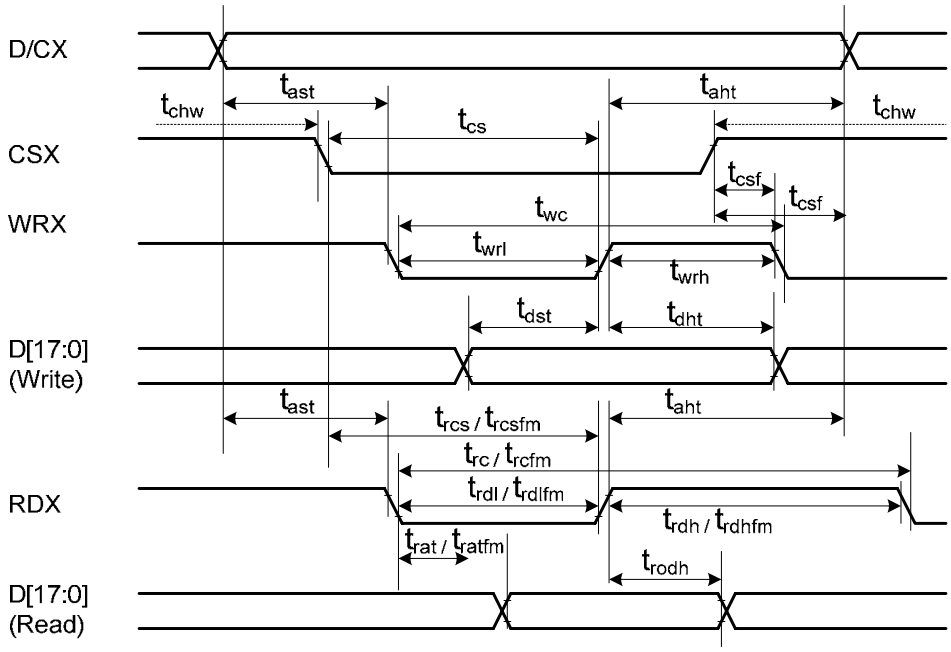
1. Make sure IOVCC ≥ GND
2. Make sure VCI ≥ AGND.
3. Make sure DDVDH ≥ VCL and DDVDH ≥ VCI
4. Make sure AGND ≥ VGL.

14.2. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply Voltage	VCI	Analog Operation Voltage	2.5	2.8	3.3	V
I/O pin Power Supply Voltage	IOVCC	I/O pin Operation Voltage	1.65	2.8	3.3	V
Logic High level input voltage	V_{IH}	IOVCC = 1.65V ~ 3.3V	0.7*IOVCC	-	IOVCC	V
Logic Low level input voltage	V_{IL}	IOVCC = 1.65V ~ 3.3V	0.0	-	0.3*IOVCC	V
Logic High level Output voltage	V_{IH}	Iout = -1 mA	0.8*IOVCC	-	IOVCC	V
Logic Low level Output voltage	V_{IL}	Iout = +1 mA	0.0	-	0.2*IOVCC	V
Logic High level input current	I_{IHD}	D[17:0]			10	uA
Logic Low level input current	I_{ILD}	D[17:0]	-10			uA

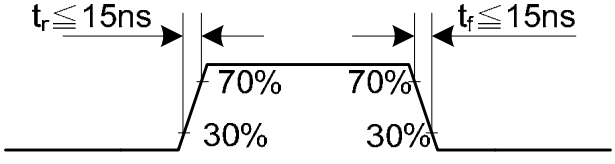
14.3. AC Characteristics

14.3.1. DBI Type B (18/16/9/8 bit) Interface Timing Characteristics

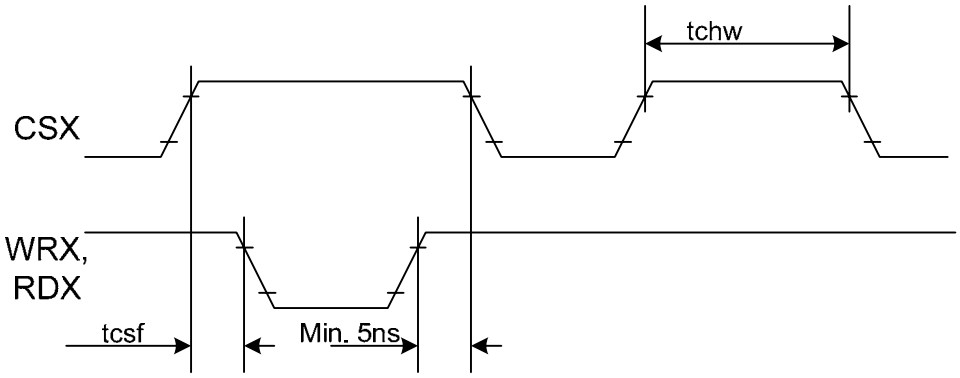


Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX “H” Pulse Width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	60	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration (ID)	90	-	ns	
	trdl	Read Control pulse L duration (ID)	45	-	ns	
RDX (FM)	trcfm	Read cycle (FM)	450	-	ns	
	trdhfm	Read Control pulse H duration (FM)	90	-	ns	
	trdlfm	Read Control pulse L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	tdst	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Data hold time	10	-	ns	
	trat	Read access time (ID)	-	40	ns	
	tratfm	Read access time (FM)	-	340	ns	
	todh	Output disable time	20	-	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, DGND=0V

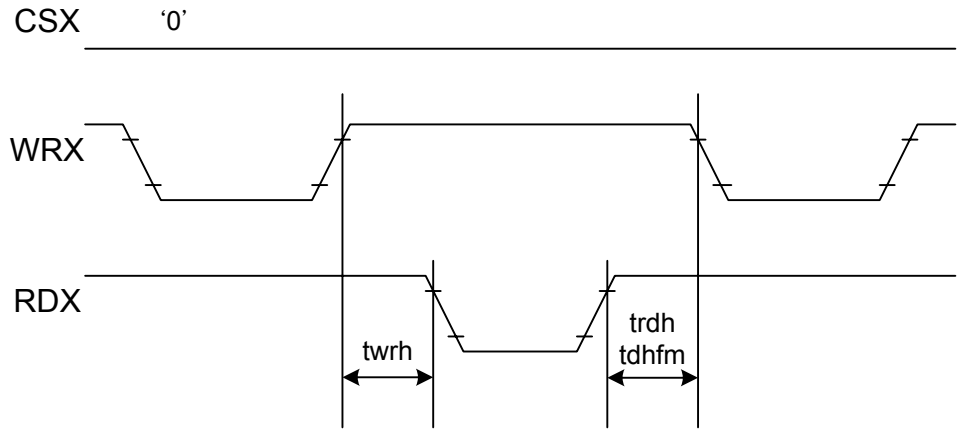


CSX timings :



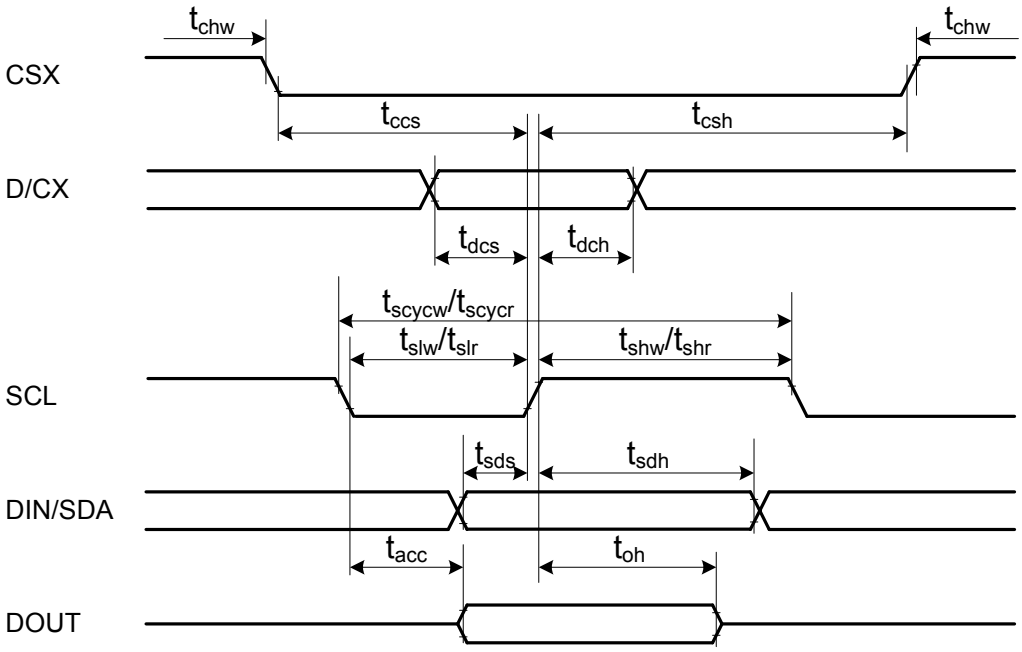
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



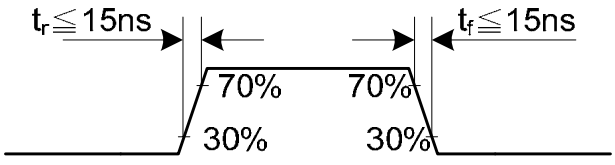
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

14.3.2. DBI Type C (SPI) Interface Timing Characteristics

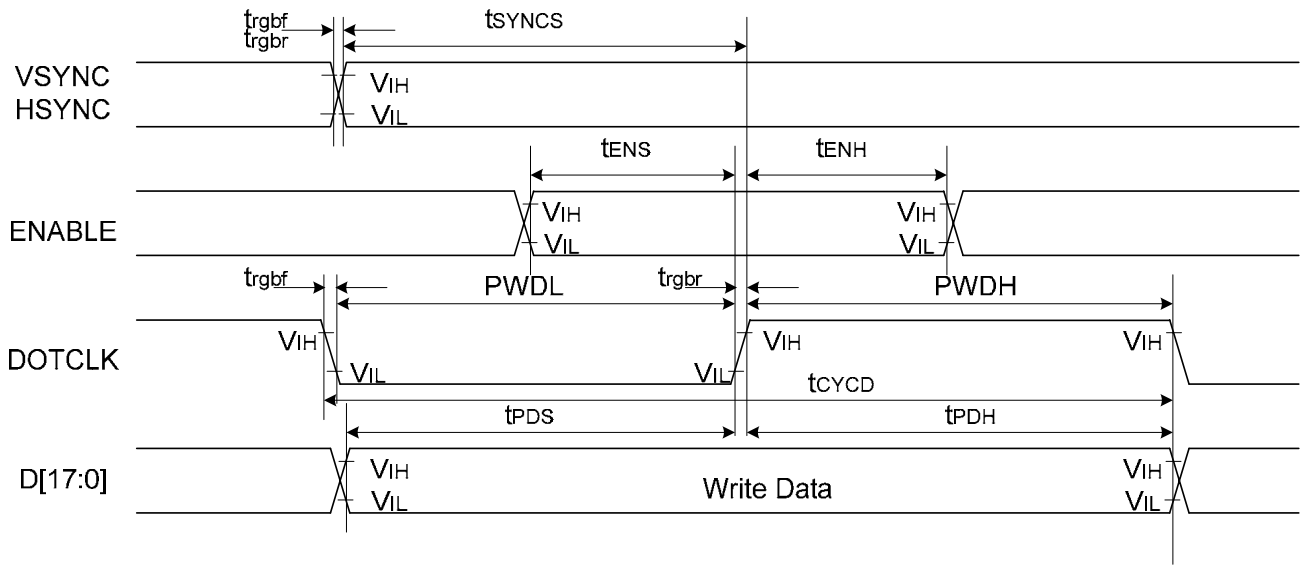


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	CSX-SCL time (Write)	15	-	ns	
	tcsh	CSX-SCL time (Write)	15	-	ns	
	tcss	CSX-SCL time (Read)	60	-	ns	
	tcsh	CSX-SCL time (Read)	60	-	ns	
	tchw	CSX “H” pulse time	40	-	ns	
SCL	tscycw	Serial clock cycle (Write)	60	-	ns	
	tshw	SCL “H” pulse width (Write)	15	-	ns	
	tslw	SCL “L” pulse width (Write)	15	-	ns	
	tscycr	Serial clock cycle (Read GRAM)	300	-	ns	
	tshr	SCL “H” pulse width (Read GRAM)	110	-	ns	
	tslr	SCL “L” pulse width (Read GRAM)	110	-	ns	
	tscycr	Serial clock cycle (Read ID)	150	-	ns	
	tshr	SCL “H” pulse width (Read GRAM)	54	-	ns	
	tslr	SCL “L” pulse width (Read GRAM)	54	-	ns	
D/CX	tdcs	D/CX setup time	7	-	ns	
	tdch	D/CX hold time	7	-	ns	
SDA (Input) (Output)	tacc	Access time	10	50	ns	For maximum CL=30pF
	toh	Output disable time	15	50	ns	For minimum CL=8pF
	tsds	Data setup time	7	-		
	tsdh	Data hold time	7	-		

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V

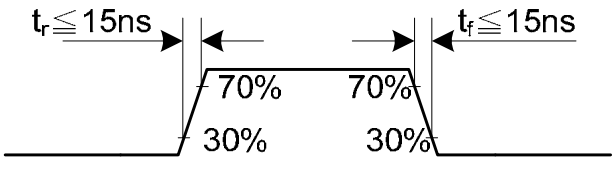


14.3.3. DPI Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V



15. Revision History

Version No.	Date	Page	Description
0.00	2008/11/24		New Formal Create