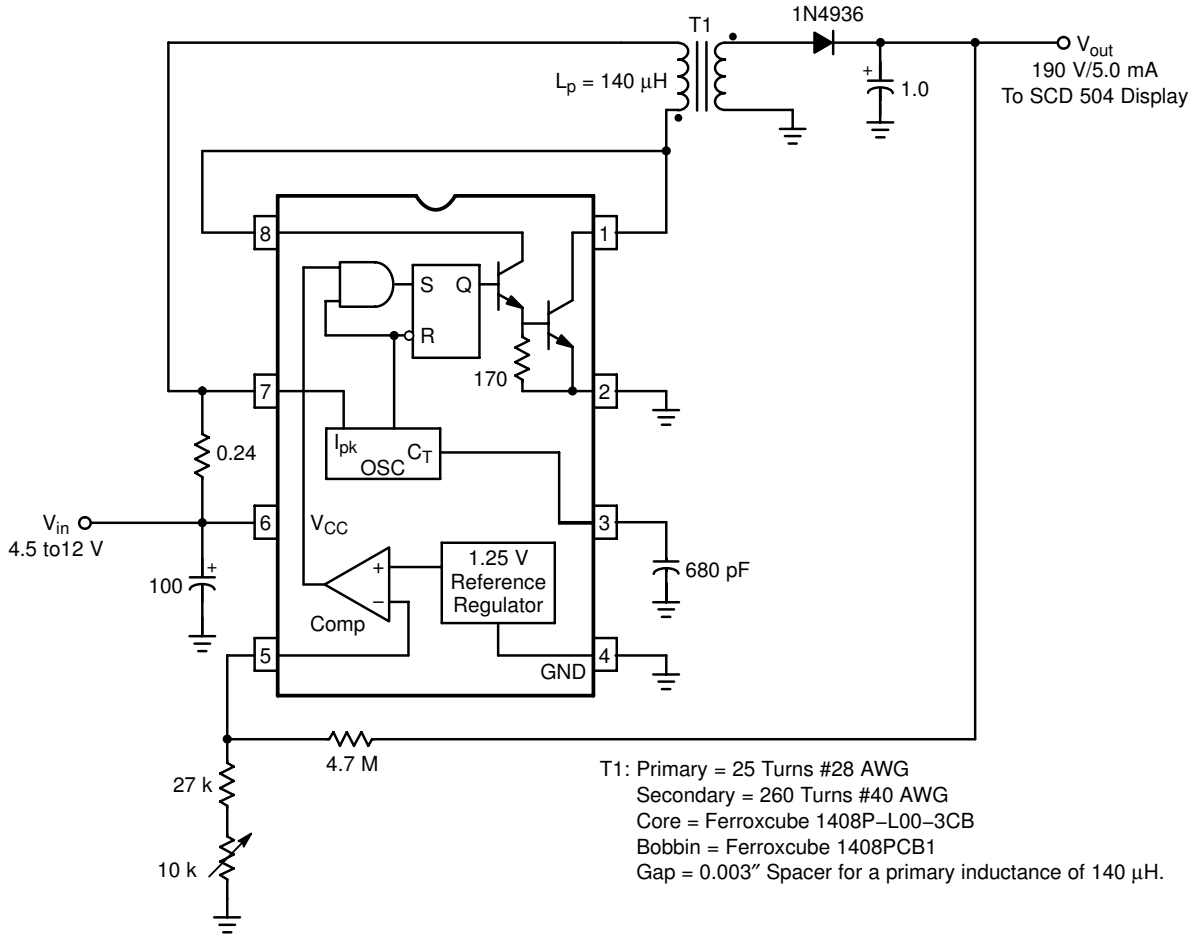


| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$ = 4.5 to 12 V, $I_{out}$ = 5.0 mA | Δ = 2.3 V or ± 0.61% |
| Load Regulation | $V_{in}$ = 5.0 V, $I_{out}$ = 1.0 to 6.0 mA | Δ = 1.4 V or ± 0.37% |
| Output Ripple | $V_{in}$ = 5.0 V, $I_{out}$ = 5.0 mA | 250 $mV_{p-p}$ |
| Short Circuit Current | $V_{in}$ = 5.0 V, $R_L$ = 0.1 Ω | 113 mA |
| Efficiency | $V_{in}$ = 5.0 V, $I_{out}$ = 5.0 mA | 68% |

This circuit was designed to power the ON Semiconductor Solid Ceramic Displays from a $V_{in}$ of 4.5 to 12 V. The design calculations are based on a step−up converter with an input of 4.5 V and a 24 V output rated at 45 mA. The 24 V level is the maximum step−up allowed by the oscillator ratio of $t_{on}/(t_{on} + t_{off})$. The 45 mA current level was chosen so that the transformer primary power level is about 10% greater than that required by the load. The maximum $V_{in}$ of 12 V is determined by the sum of the flyback and leakage inductance voltages present at the collector of the output switch during turn−off must not exceed 40 V.

**Figure 27. High−Voltage, Low Power Step−Up for Solid Ceramic Display**