

# DIGITRON SEMICONDUCTORS

2N5441-2N5446, T6420 SERIES

40 AMP SILICON TRIACS

Available Non-RoHS (standard) or RoHS compliant (add PBF suffix).

Available as "HR" (high reliability) screened per MIL-PRF-19500, JANTX level. Add "HR" suffix to base part number.

## MAXIMUM RATINGS (Sinusoidal supply voltage at frequency 50/60Hz and with resistive or inductive load)

Rating	Symbol	2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	Unit
<b>Repetitive peak off-state voltage</b> <sup>(1)</sup> Gate open, T <sub>J</sub> = -65 to 100°C	V <sub>DROM</sub>	200	400	600	V
<b>RMS on-state current (Conduction angle = 360°)</b> T <sub>C</sub> = 70°C (press-fit type) T <sub>C</sub> = 65°C (stud type) T <sub>C</sub> = 60°C (isolated stud type)	I <sub>T(RMS)</sub>		40 40 40		A
<b>Peak surge (non-repetitive) on state current</b> For one cycle of applied principal voltage 60Hz (sinusoidal) 50Hz (sinusoidal)	I <sub>TSM</sub>		300 265		A
<b>Rate of change of on-state current</b> V <sub>DM</sub> = V <sub>DROM</sub> , I <sub>GT</sub> = 200mA, t <sub>r</sub> = 0.1μs	di/dt		100		A/μs
<b>Fusing current</b> T <sub>J</sub> = -65° to 110°C, t = 1.25 to 10ms	I <sup>2</sup> t		450		A <sup>2</sup> s
<b>Peak gate trigger current</b> <sup>(2)</sup> For 1μs maximum	I <sub>GTM</sub>		12		A
<b>Gate power dissipation</b> Peak (for 10μs maximum, I <sub>GTM</sub> ≤ 4A) Average	P <sub>G(M)</sub> P <sub>G(AV)</sub>		40 0.75		W
<b>Storage temperature range</b>	T <sub>stg</sub>		-65 to 150		°C
<b>Operating temperature range</b>	T <sub>C</sub>		-65 to 110		°C
<b>Terminal temperature (during soldering)</b> For 10 s maximum (terminals and case)	T <sub>T</sub>		225		°C
<b>Maximum stud torque</b>	r <sub>s</sub>		50		In. lb.

Note 1: For either polarity of main terminal 2 voltage (V<sub>MT2</sub>) with reference to main terminal 1.

Note 2: For either polarity of gate voltage (V<sub>G</sub>) with reference to main terminal 1.

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Limits			Units
		For all types unless otherwise specified			
		Min	Typ	Max	
<b>Peak off-state current</b> <sup>(1)</sup> Gate open, T <sub>J</sub> = 110°C, V <sub>DROM</sub> = maximum rated value	I <sub>DROM</sub>	-	0.2	4	mA
<b>Maximum on-state voltage</b> <sup>(1)</sup> I <sub>T</sub> = 100A(peak), T <sub>C</sub> = 25°C I <sub>T</sub> = 56A(peak), T <sub>C</sub> = 25°C	V <sub>TM</sub>	- -	1.7 1.5	2 1.85	V
<b>DC holding current</b> <sup>(1)</sup> Gate open, initial principal current = 500mA(dc), V <sub>D</sub> = 12V T <sub>C</sub> = 25°C T <sub>C</sub> = -65°C	I <sub>HO</sub>	- -	25 -	60 100	mA
<b>Critical rate of rise of commutation voltage</b> <sup>(1)</sup> For V <sub>D</sub> = V <sub>DROM</sub> , I <sub>T(RMS)</sub> = 40A, commutating di/dt = 22A/ms, gate unenergized T <sub>C</sub> = 70°C (press fit type) T <sub>C</sub> = 65°C (stud type) T <sub>C</sub> = 60°C (isolated-stud types)	dv/dt	5 5 5	30 30 30	- - -	V/μs

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## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Limits			Units
		For all types unless otherwise specified			
		Min	Typ	Max	
<b>Critical rate of rise of off-state voltage<sup>(1)</sup></b> For $V_D = V_{DROM}$ , exponential voltage rise, gate open $T_C = 110^\circ\text{C}$ : 2N5441, 2N5444, T6420B 2N5442, 2N5445, T6420D 2N5443, 2N5446, T6420M	dv/dt	50 30 20	200 150 100	- - -	V/ $\mu\text{s}$
<b>DC trigger current</b> $(V_D = 12\text{V}, R_L = 30\Omega, T_C = 25^\circ\text{C})$ MT2(+),G(+) MT2(-), G(-) MT2(+), G(-) MT2(-), G(+) $(V_D = 12\text{V}, R_L = 30\Omega, T_C = -65^\circ\text{C})$ MT2(+),G(+) MT2(-), G(-) MT2(+), G(-) MT2(-), G(+)	$I_{GT}$	- - - - - - - -	15 20 30 40 - - - -	50 50 80 80 125 125 240 240	mA
<b>DC gate trigger voltage<sup>(1)(2)</sup></b> $V_D = 12\text{V(d.c.)}, R_L = 30\Omega$ $T_C = 25^\circ\text{C}$ $T_C = -65^\circ\text{C}$ $V_D = V_{DROM}, R_L = 125\Omega, T_C = 110^\circ\text{C}$	$V_{GT}$	- - 0.2	1.35 1.80 -	2.5 3.4 -	V
<b>Gate controlled turn on time</b> (Delay time + rise time) $V_D = V_{DROM}, I_{GT} = 200\text{mA}, t_r = 0.1\mu\text{s}, I_T = 60\text{A(peak)}, T_C = 25^\circ\text{C}$	$t_{gt}$	-	1.7	3	$\mu\text{s}$
<b>Thermal resistance, junction to case, steady state</b> Press fit types Stud types Isolated stud types	$R_{\theta JC}$	- - -	- - -	0.8 0.9 1	$^\circ\text{C/W}$

Note 1: For either polarity of main terminal 2 voltage ( $V_{MT2}$ ) with reference to main terminal 1.  
 Note 2: For either polarity of gate voltage ( $V_G$ ) with reference to main terminal 1.

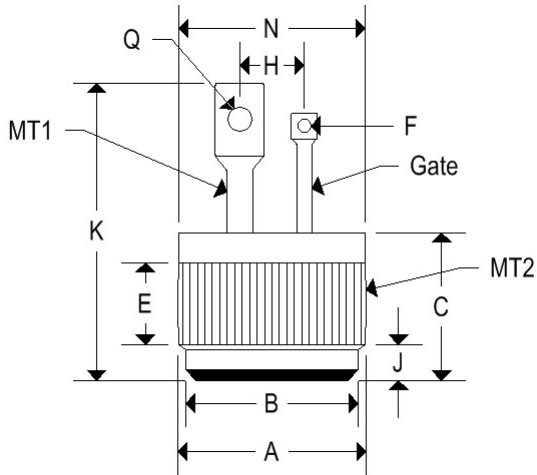
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## MECHANICAL CHARACTERISTICS

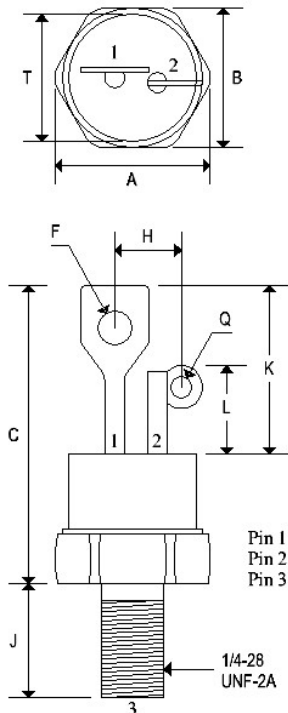
<b>Case</b>	Digi PF1 (2N5441-2N5443)
<b>Marking</b>	Alpha-numeric
<b>Polarity</b>	Cathode is stud



	DIGI PF1			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.501	0.505	12.730	12.830
F	-	0.160	-	4.060
G	0.085	0.095	2.160	2.410
H	0.060	0.070	1.520	1.780
J	0.300	0.350	7.620	8.890
K	-	1.050	-	26.670
L	-	0.670	-	17.020
Q	0.055	0.085	1.400	2.160

## MECHANICAL CHARACTERISTICS

<b>Case</b>	TO-48 (2N5444-2N5446)
<b>Marking</b>	Alpha-numeric
<b>Polarity</b>	Cathode is stud



	TO-48			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.604	0.614	15.340	15.600
B	0.551	0.559	14.000	14.200
C	1.050	1.190	2.670	30.230
F	0.135	0.160	3.430	4.060
H	-	0.265	-	6.730
J	0.420	0.455	10.670	11.560
K	0.620	0.670	15.750	17.020
L	0.300	0.350	7.620	8.890
Q	0.055	0.085	1.400	2.160
T	0.501	0.505	12.730	12.830

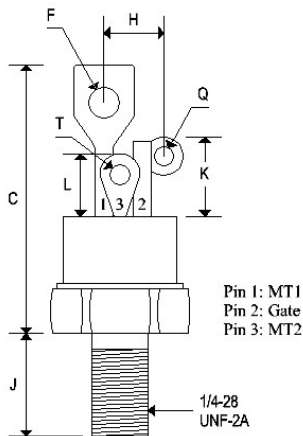
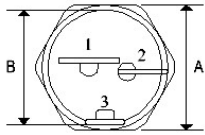
# DIGITRON SEMICONDUCTORS

2N5441-2N5446, T6420 SERIES

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## MECHANICAL CHARACTERISTICS

<b>Case</b>	TO-48 ISO (T6420 Series)
<b>Marking</b>	Alpha-numeric
<b>Polarity</b>	Cathode is stud



	TO-48 ISO			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.551	0.559	14.000	14.200
B	0.501	0.505	12.730	12.830
C	-	1.280	-	32.510
F	-	0.160	-	4.060
H	-	0.265	-	6.730
J	0.420	0.455	10.670	11.560
K	0.300	0.350	7.620	8.890
L	0.255	0.275	6.480	6.990
Q	0.055	0.085	1.400	2.160
T	0.135	0.150	3.430	3.810

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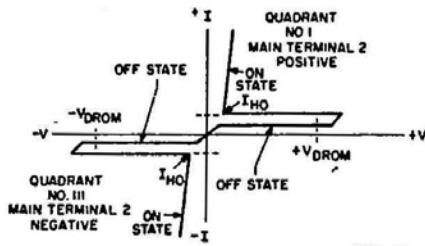


Fig. 1 - Principal voltage-current characteristic.

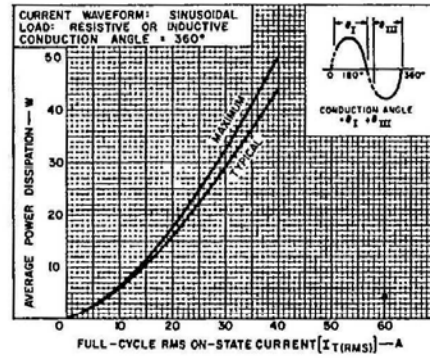


Fig. 2 - Power dissipation vs. on-state current.

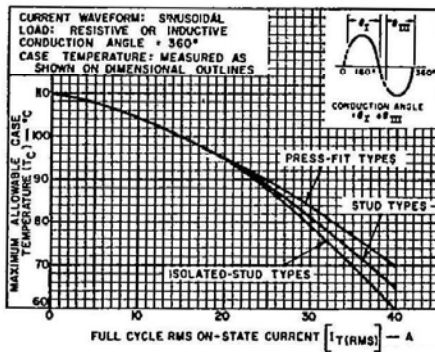


Fig. 3 - Maximum allowable case temperature vs. on-state current.

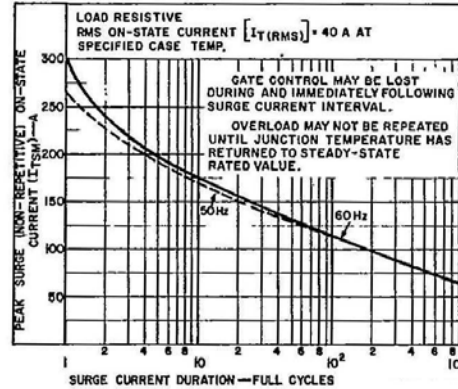


Fig. 4 - Peak surge on-state current vs. surge current duration.

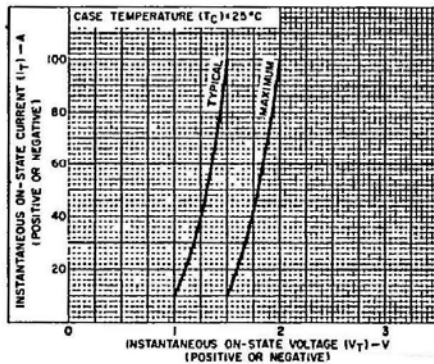


Fig. 5 - On-state current vs. on-state voltage.

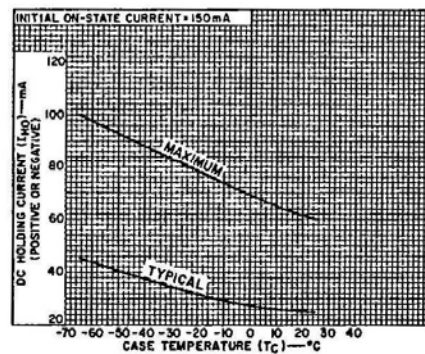


Fig. 6 - DC holding current vs. case temperature.

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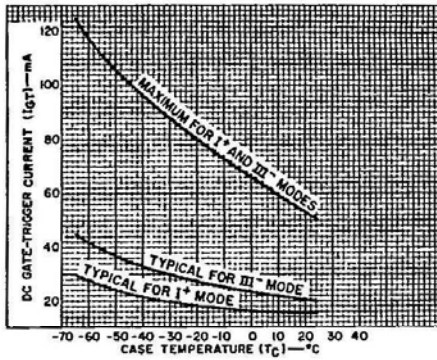


Fig. 7 - DC gate-trigger current vs. case temperature (I+ & III+ modes).

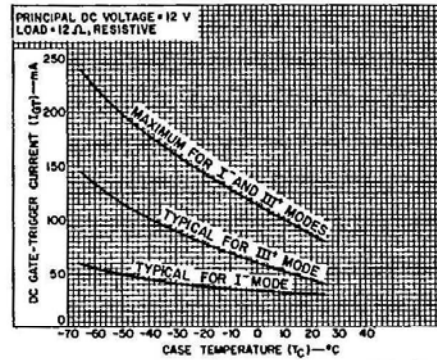


Fig. 8 - DC gate-trigger current vs. case temperature (I- & III- modes).

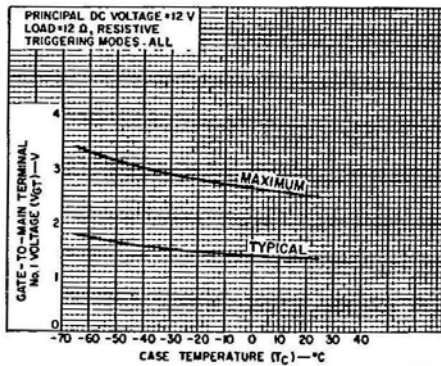


Fig. 9 - DC gate trigger voltage vs. case temperature.

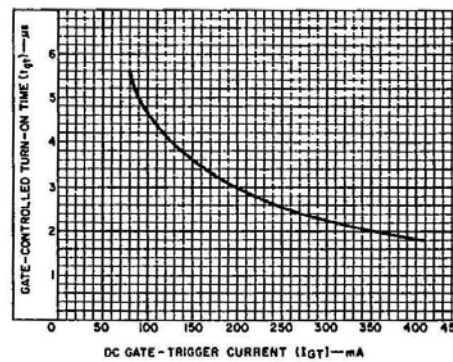


Fig. 10 - Turn-on time vs. gate-trigger current.

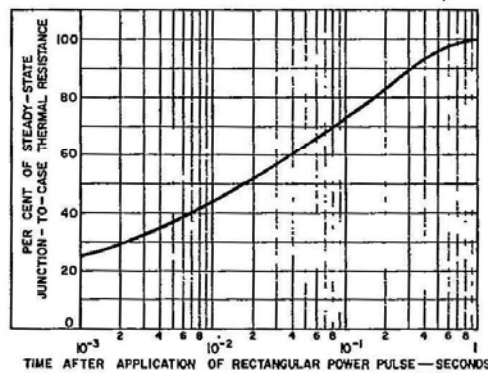


Fig. 11 - Transient junction-to-case thermal resistance vs. time for press-fit and stud types.

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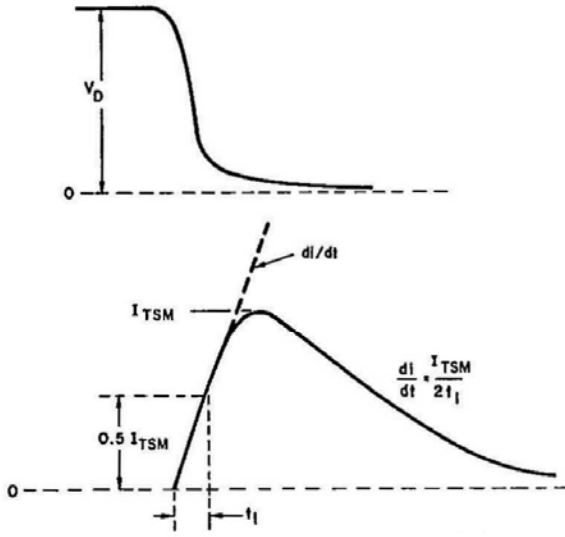


Fig. 12 - Rate of change of on-state current with time (defining  $di/dt$ ).

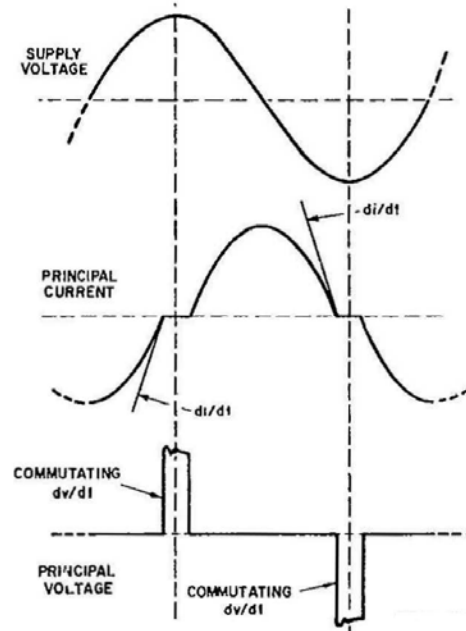


Fig. 13 - Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage ( $dv/dt$ ).

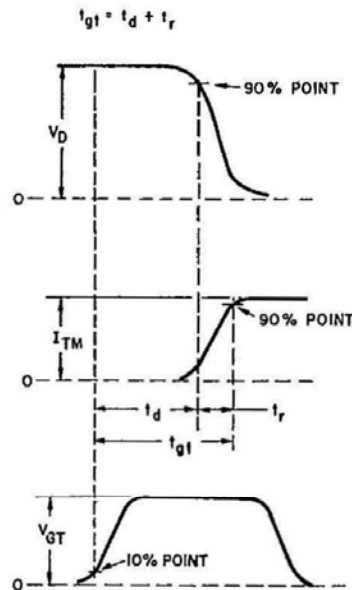


Fig. 14 - Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time ( $t_{gt}$ ).