Charge-Sensitive Front End Circuits

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Outline

- Custom monolithic front ends
  - *advantages*
  - *access to technology*
  - *design tools*
- Low noise analog design in monolithic CMOS
  - *preamplifier design*
  - *shaping amplifier*
- Circuit examples
- CMOS Scaling and Charge Sensitive Amplifier design
  - *noise mechanisms in scaled devices*
  - *optimum capacitive match to detector*
  - *noise, dynamic range, and power vs. scaling length*

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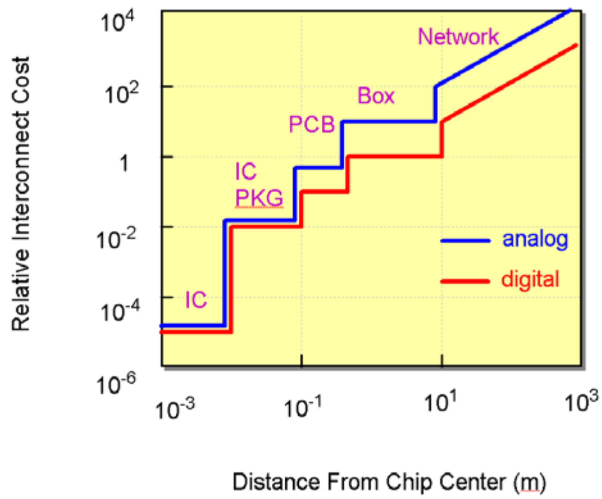
Custom monolithic front ends

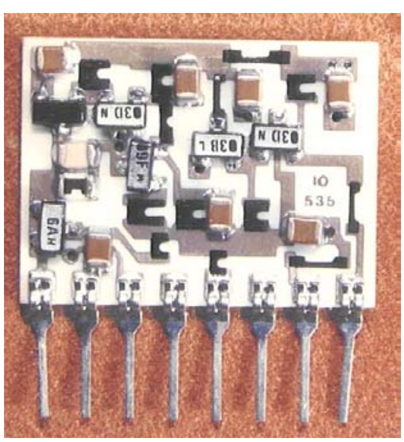
- Can be efficiently mass-produced with excellent economy of scale:
  - *E.g., maskset + 10 wafers ~ $100K, 1000 chips/wafer*
  - *Additional wafer ~ $5K*
  - *Incremental cost < $10/chip*
  - *Chip may have 16 – 128 channels*
- Can be located close to dense detector electrode arrays
  - *pixels, micropattern & segmented cathode designs*
- Can combine functions on single chip, replacing PCB/hybrid/cable connections with lower cost on-chip connection
- Can reduce power*

Cost of interconnect



ISSCC 2006

Low-Noise preamplifier – thick film ceramic hybrid

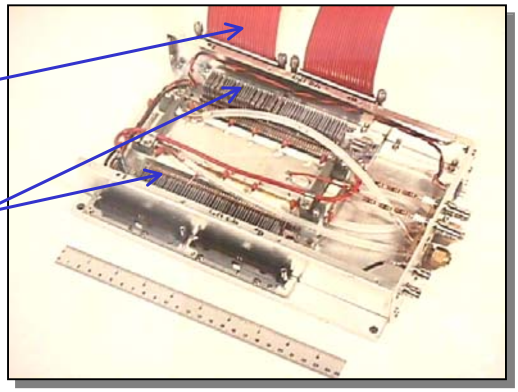


- single channel
- 29 components
- 44 solder joints
- 8 connections to PCB
- 175 mW power
- 20 x 14 x 2.5 mm
- $45

Front end box for 100-channel detector

cables to remote shapers

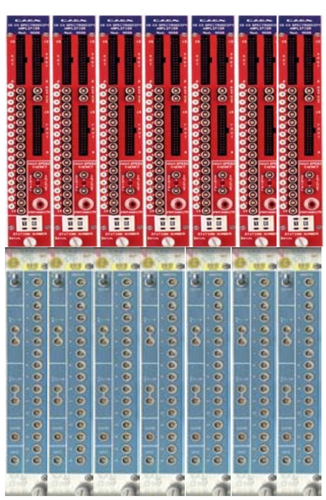
hybrid preamplifiers



100 preamp channels:

- 70 cm^3
- 18 W
- over 5000 solder connections
- \$4500 (preamps)
- \$1500 (cables)

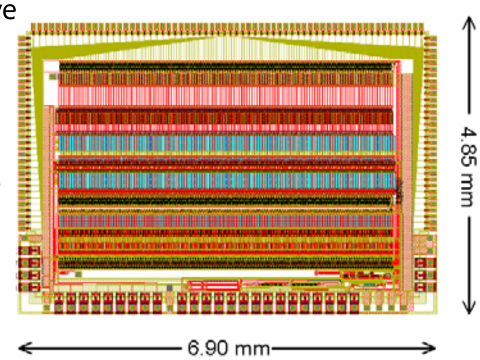
Shaping amplifiers and discriminators for 100 channels



- crate-based modules
- 27,000 cm^3
- $^>$ 500 backplane pin connections
- 200W
- ~ \$30,000 – \$70,000

IDE TA1 chip

- 128 channel charge sensitive preamplifier-shaper
- simultaneous sample and hold
- multiplexed analog readout
- level-sensitive discriminator following the shaper
- wire-or'ed trigger output
- 1.7 mW/channel



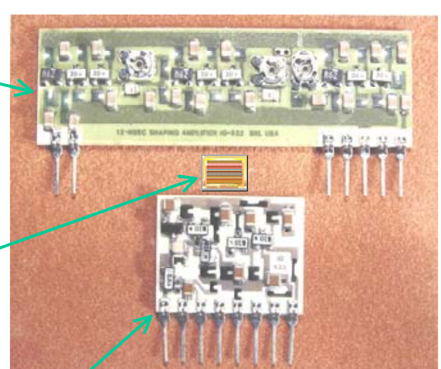
http://www.ideas.no

Advantages of monolithic realization

hybrid shaper

128-channel monolithic front end chip

hybrid preamplifier



Improvement over hybrid + rack-based system:

Cost	X 200
Power:	X 10^3
Volume:	X $2*10^6$

Monolithic also adds functionality:

- *cal. pulse distribution*
- *sample/hold*
- *multiplexing*

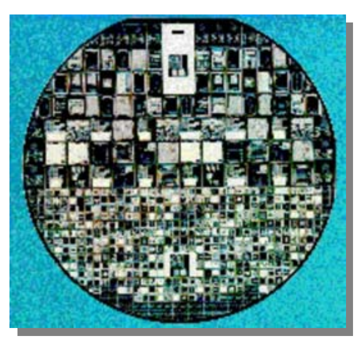
Custom monolithics – technology options

- Bipolar
  - *Workhorse of "old" analog*
  - *Available from a handful of vendors*
  - *Speed/power advantage over CMOS (diminishing)*
  - *Low integration density*
- Standard CMOS
  - *Suitable for most analog designs*
  - *Best for combining analog and digital*
  - *Highest integration density*
  - *Widely available*
  - *Short life cycle (3 years/generation)*
- BiCMOS
  - *Complex process, expensive*
- JFET/CMOS
  - *JFET has low 1/f noise but slow*
  - *Unavailable commercially*
- Silicon on insulator (SOI)
  - *Modest speed advantage for digital*
  - *Drawbacks for analog*
- SiGe
  - *Complexity equivalent to BiCMOS*
  - *Extremely fast bipolar device plus submicron CMOS*
  - *Availability increasing*
- GaAs
  - *Unsuitable for wideband analog*

Custom monolithics: technology access

Multiproject foundry services

- Combine designs from many institutions on one maskset
- Arrange for regular runs with a variety of popular foundries
- Design support
  - *Models*
  - *Design rules*
  - *Process monitoring*
- Amortize cost of run over many users

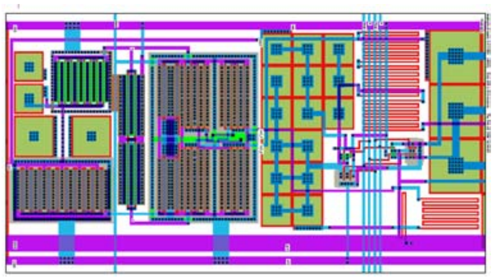


multiproject wafer

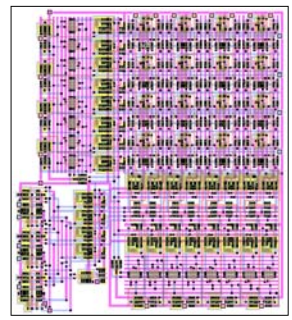
In the U.S.	*Europe*
MOSIS service www.mosis.org	Europractice www.imec.be/europractice

CMOS layout examples

Analog



Digital



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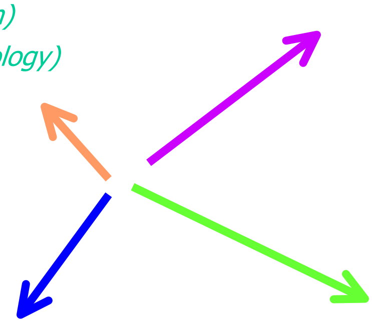
Two types of charge sensitive amplifier

1. Charge integrating
   - *Charge is delivered by detector in a steady, continuous manner*
   - *Quantity of interest: total charge generated over a fixed time interval*
   - *For measuring radiation intensity*
   - *Typical output: image*
   - *Not covered in this short course*
2. Event-by-event
   - *Charge is delivered by the detector in a series of pulse-like events*
   - *For each event, measure:*
     - quantity of charge
     - time of occurrence
   - *Typical output: histogram*

MOS charge amplifier design

- Key parameters:
  - C_{det} , I_{det} , Q_{max} *(detector)*
  - *Rate,* P_{diss} *(system)*
  - f_T , K_F , I_{in} *(technology)*

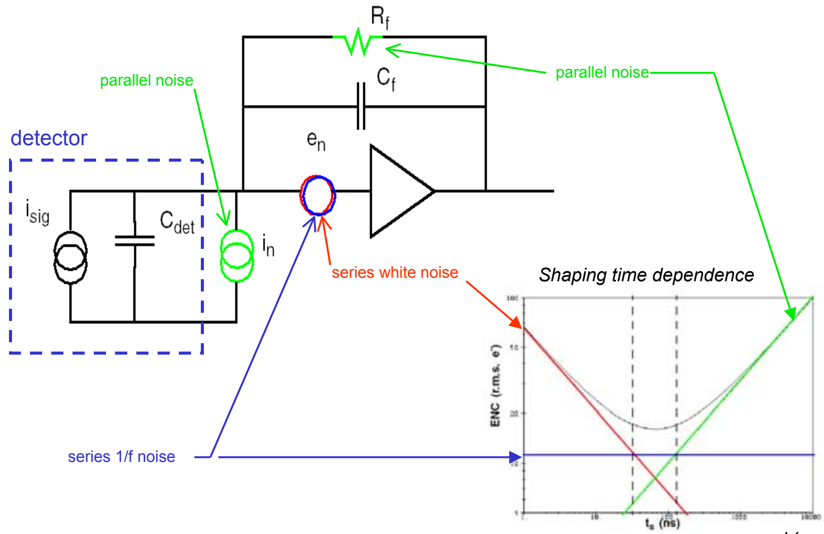
- Key design decisions
  - C_{gs}/C_{det}
  - *Reset system*
  - *Weighting function*



Monolithic preamplifier design

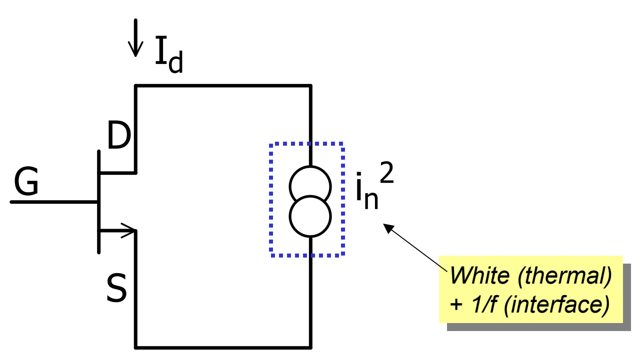
- Noise sources (MOSFET and BJT)
- ENC
- Input device optimization
- Parallel noise and the reset system

Charge amplifier noise sources



MOSFET series noise

- Drain current and its fluctuation:



MOSFET series noise

- Thermal – *Johnson (white) noise of channel incremental resistance:*

$$i_{n,th}^2 = \frac{4kT}{R_{eq}} = \frac{4kT\gamma}{(1/g_m)} \qquad \frac{2}{3} < \gamma < 1.0$$

- 1/f (flicker) – *exchange of mobile carriers between channel and interface states*

$$i_{n,1/f}^2 = \frac{K_F \cdot g_m^2}{C_{gs} f}$$

$$10^{-26}\,\mathrm{J} < K_F < 10^{-23}\,\mathrm{J}$$

Compare typical JFET $K_F \sim 10^{-27}$J

PMOS devices have 3 - 30X lower 1/f noise than NMOS FETs

Weak dependence on bias conditions.

BJT noise

BJT	**FET**
Diffusion current	**Drift current**
Minority carrier device	**Majority carrier device**
Shot noise in I_C, I_B	**Thermal noise in I_D**
Bulk conduction	**Surface conduction**
Low 1/f noise	**High 1/f noise**

Collector current shot noise:

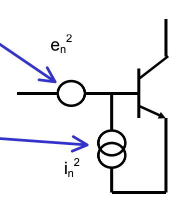
$$i_c^2 = 2qI_C = 2kTg_m$$

Base current shot noise:

$$i_b^2 = 2qI_B = \frac{2qI_C}{\beta}$$

$$e_n^2 = 4kT\left(\frac{1}{2g_m} + r_b\right)$$

$$i_n^2 = 2qI_B$$

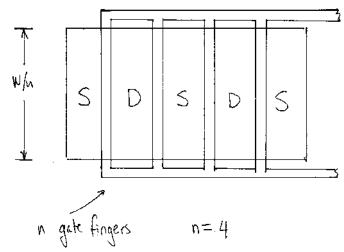


Gate resistance noise

- Polysilicon gate is resistive:
  - ρ_{poly} **25 Ω/sq.**
  - $\rho_{silicided\ poly}$ **4 Ω/sq.**

$$R_g = \rho_{poly} \cdot \frac{W}{L}$$

$$e_{ng}^2 = 4kT \cdot \frac{R_g}{12 \cdot n^2}$$

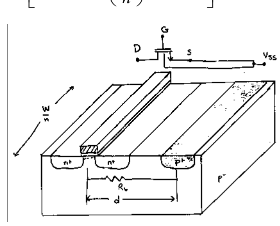


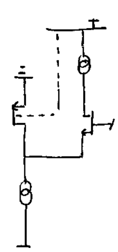
Bulk resistance noise

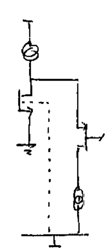
- Resistive substrate couples to the channel via the back transconductance g_{mb}.
- Substrate resistance is distributed.

$$i_{db}^2 = \left[4kT \cdot n \cdot \beta \frac{d}{\left(\frac{W}{n}\right)} \cdot \left(\frac{g_{mb}}{n}\right)^2 \right] = 4kT\beta \frac{d}{W} g_{mb}^2$$

β = geometrical factor



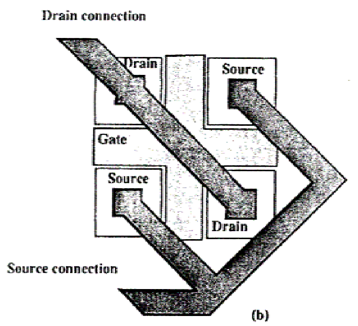




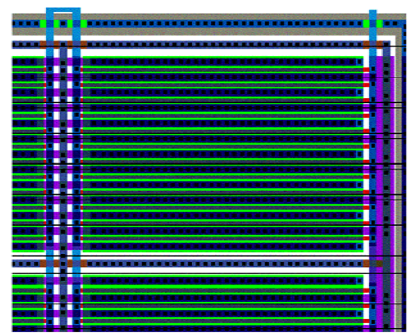
- Minimize by reverse biasing the source-substrate junction.

Layout techniques to reduce gate and bulk resistance noise

Waffle iron layout



Substrate contacts, guard ring, multiple gate fingers contacted on both ends



Induced gate current noise

Channel voltage fluctuations change charge stored in gate-channel capacitance.

Noise current generator in parallel with input:

$$i_g^2 = 4kT \cdot \frac{\omega^2 C_{gs}^2}{5 g_m} = \frac{4kTg_m}{5}\left(\frac{f}{f_T}\right)^2$$

For system with capacitive input,

$$e_g^2 = \frac{i_g^2}{\omega^2 C_{in}^2} = \frac{4kT}{5 g_m}\left(\frac{C_{gs}}{C_{in}}\right)^2$$

$$R_n = R_{n0} \cdot \left[1 + \frac{1}{3}\left(\frac{C_{gs}}{C_{in}}\right)^2\right]$$

Increase in R_n < 5%.

Input series noise: Example

N-channel MOSFET, 1.2 μm technology, for 20 pF detector.

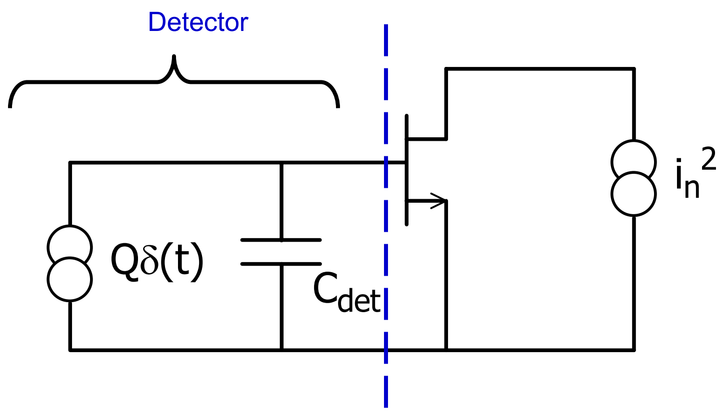
W/L = 3300/1.2 biased to g_m = 5 mS (I_D = 200 μA)

$K_F = 10^{-24}$J $C_{ox}WL$ = 6.7 pF ρ_g*W/L = 69 kΩ n=66 or 1

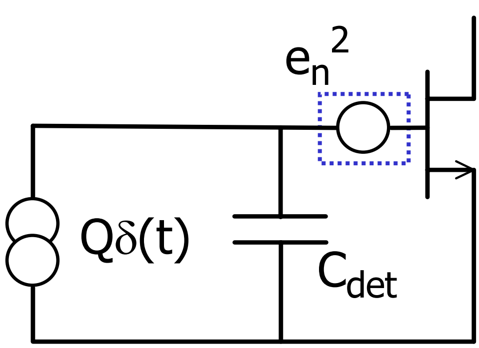
Rsubs = 2kΩ/sq., d/(W/n) = 1

	e_n, nV/√Hz	R_{eq}, Ω
thermal	1.47	133
1/f (100kHz)	1.22	91
R_g, n = 1	9.60	5750
R_g, n = 66	0.15	1.3
bulk	0.80	40
induced gate	0.27	4.5

MOSFET connected to detector



Transform noise to input

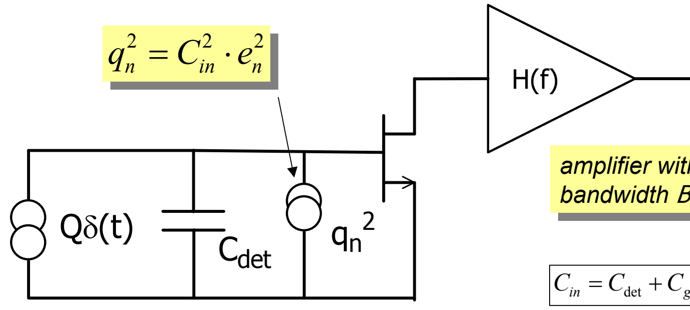


$$e_n^2 = \frac{4kT\gamma}{g_m} + \frac{K_F}{C_{gs} f}$$

white (thermal) | 1/f (interface)

Equivalent input noise charge (ENC)

$$q_n^2 = C_{in}^2 \cdot e_n^2$$



amplifier with limited bandwidth $BW = t_m^{-1}$

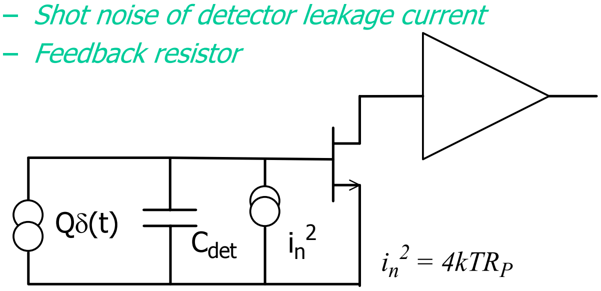
$$C_{in} = C_{\det} + C_{gs}$$

$$ENC^2 = \int_0^\infty q_n^2(f) \cdot |H(f)|^2 \, df$$

$$= C_{in}^2 \cdot \left(\underbrace{\frac{a_1 4kT\gamma}{g_m t_m}}_{\text{white}} + \underbrace{\frac{a_3 K_F}{C_{gs}}}_{1/f} \right)$$

Parallel noise

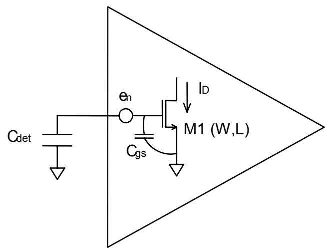
- From any noise current source connected to input:
  - *Detector biasing resistor*
  - *Shot noise of detector leakage current*
  - *Feedback resistor*



$$i_n^2 = 4kTR_P$$

$$\boxed{ENC_{par} = \sqrt{\frac{a_2 4kTt_m}{R_p}}}$$

Sizing the input transistor for minimum series noise



$$ENC^2 = \left(C_{\det} + \boxed{C_{gs}}\right)^2 \cdot \left(\frac{4kT\gamma}{\boxed{g_m}\, t_m} + \frac{K_F}{\boxed{C_{gs}}}\right)$$

M1 should have minimum L for best g_m/C_{gs} ratio

Increasing M1 width makes e_n smaller while C_{gs} gets larger

⇒ an optimum width for M1 must exist

To calculate this optimum (see Appendix I), consider two cases:

I. The FET is biased at constant current density (I_D/W = const.)

II. The FET drain current is kept constant as the width W is varied

Case I is simple and the solution is the same as that derived for JFET amplifiers in the 1950's.

$$C_{gs,\ opt} = C_{det}$$

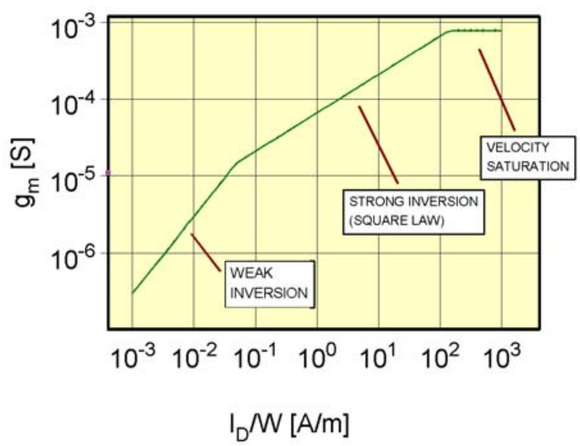
Case II requires us to look in more detail at how the MOSFET transconductance behaves as the width (and hence the current density) varies.

MOS transconductance: 3 regions

$$g_m = \begin{cases} \dfrac{I_D}{nV_t}, & \left(\dfrac{I_D}{W}\right) < \dfrac{2\mu C_{ox}(nV_t)^2}{L} & \text{weak inversion} \\[2ex] \sqrt{2\mu C_{ox}\dfrac{W}{L}I_D}, & \dfrac{2\mu C_{ox}(nV_t)^2}{L} < \left(\dfrac{I_D}{W}\right) < \dfrac{C_{ox}Lv_{sat}^2}{2\mu} & \text{strong inversion (square law)} \\[2ex] C_{ox}Wv_{sat}, & \left(\dfrac{I_D}{W}\right) > \dfrac{C_{ox}Lv_{sat}^2}{2\mu} & \text{velocity saturated} \end{cases}$$

I_D	drain current
C_{ox}	oxide capacitance
μ	mobility
W,L	channel width and length
v_{sat}	carrier saturation velocity
n	subthreshold slope factor
$V_t = \dfrac{kT}{q}$	thermal voltage

MOS transconductance: 3 regions



MOS Transconductance as a function of current density

Write g_m as explicit function of C_g (I_D=const.)

$$g_m(C_g) = \begin{cases} \dfrac{I_D}{nV_t} & \propto \quad C_g^0 & \text{weak inversion} \\[2ex] \sqrt{\dfrac{2\mu I_D C_g}{L^2}} & \propto \quad C_g^{1/2} & \text{strong inversion (square law)} \\[2ex] \dfrac{v_{sat}C_g}{L} & \propto \quad C_g^1 & \text{velocity saturated} \end{cases}$$

Minimize ENC as a function of C_g

$$ENC^2 = \frac{\alpha\left(C_{\det} + C_g\right)^2}{g_m(C_g) \cdot t_m}$$

$$\frac{d(ENC^2)}{d(C_g)} = \frac{2\alpha(C_{\det} + C_g)g_m - \alpha(C_{\det} + C_g)^2 g_m'}{g_m^2 \cdot t_m} = 0$$

$$2g_m = (C_{\det} + C_{g,opt})g_m'$$

$$C_{g,opt} = \frac{2g_m}{g_m'} - C_{\det}$$

Optimum MOSFET size for the 3 regions

$$\Rightarrow C_{g,opt} = \begin{cases} 0 & \text{weak inversion* (see below)} \\ \dfrac{C_{\det}}{3} & \text{strong inversion (square law)} \\ C_{\det} & \text{velocity saturated} \end{cases}$$

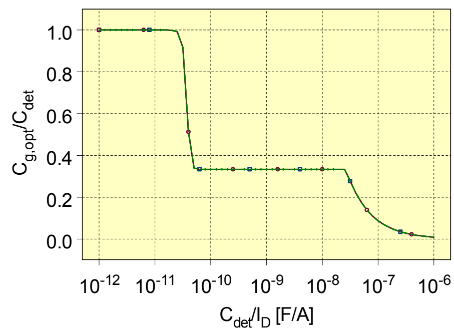
Weak inversion case:

- In weak inversion, transconductance is independent of device width.
- Hence it always pays to decrease device width, since noise source e_n stays constant but capacitance goes down.
- However, if device width approaches zero at fixed current, current density will increase until at some point the device will revert to strong inversion operation.
- As long as the device is in weak inversion at a width where $C_g = C_{det}/3$, it pays to decrease the width until the device is at the weak-strong inversion boundary:

$$C_{gopt,wi} = \frac{L_{\min}^2 I_D}{2\mu(nV_t)^2}$$

Optimum MOSFET size depends on ratio of C_{det} to drain current:

C_{det} / I_D ratio	Region of operation	Optimum capacitive match
$\frac{C_{det}}{I_D} < \frac{6\mu}{v_{sat}^2}$	Velocity saturated	$C_{gs} = C_{det}$
$\frac{6\mu}{v_{sat}^2} < \frac{C_{det}}{I_D} < \frac{3L_{min}^2}{2\mu(nV_t)^2}$	Strong-inversion square-law	$C_{gs} = C_{det} / 3$
$\frac{C_{det}}{I_D} > \frac{3L_{min}^2}{2\mu(nV_t)^2}$	Weak inversion	$C_{gs} = L_{min}^2 I_D / 2\mu(nV_T)^2$



Capacitive match – 1/f noise

$$ENC_f^2 = a_3 \frac{K_F}{C_{gs}} (C_{gs} + C_{det})^2$$

K_F is 1/f noise coefficient (J)
a_3 depends on weighting function but not on t_m.
a_3 = 4 for CR-RC shaping

min. for $C_{gs} = C_{det}$:

$$ENC_{f,\min} = 2\sqrt{a_3 K_F C_{det}}$$

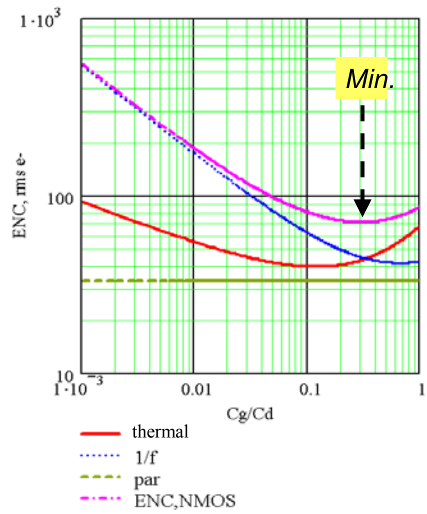
e.g. $K_F = 10^{-24}$ J, C_{det} = 10pF, a_3 = 4:

$ENC_{f,min}$ = 80 e^-

Composite noise

- C_{det} = 3 pF
- t_m = 1 μs
- P_{diss} = 1 mW
- I_{leak} = 100 pA
- Technology: 0.35 μm NMOS

- *Optimum width for series noise is a compromise between white and 1/f components*



Minimum series noise

- Input MOSFET fully optimized:

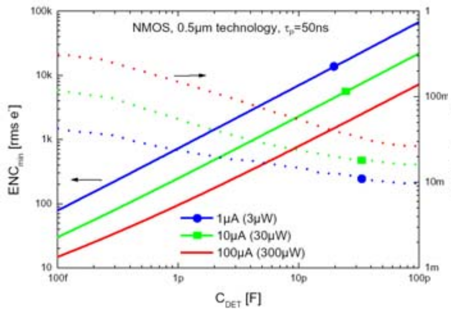
$$ENC_{sw,opt} \approx \sqrt{kTC_{\text{det}}}\sqrt{\frac{\tau_{el}}{t_m}}$$

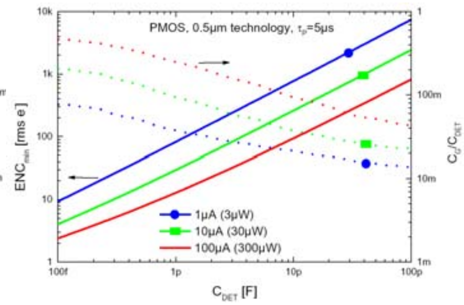
$$ENC_{1/f,opt} \approx \sqrt{K_F C_{\text{det}}}$$

τ_{el} = electron transit time under the gate $= C_{gs}/g_m$

- Key ingredients for low series ENC:
  - *low C_{det}*
  - *long t_m*
  - *short τ_{el}*
  - *low K_F*

ENC (series) vs. C_{det}





For fixed power budget,

$$ENC \propto \begin{cases} C_{DET}, \text{ weak inversion} \\ C_{DET}^{3/4}, \text{ strong inversion} \end{cases}$$

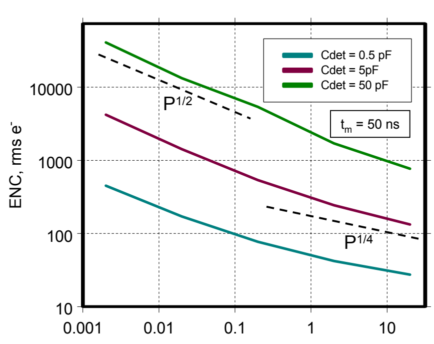
Power allowed to scale with CDET:

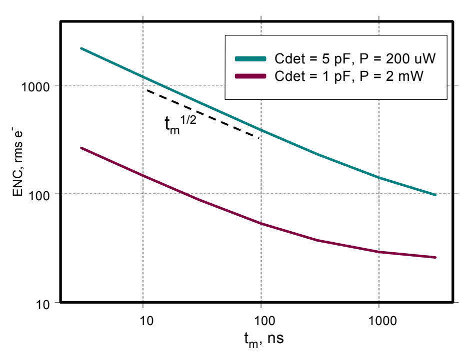
$ENC \propto C_{DET}^{1/2}$

De Geronimo et al. , NIM A 471 (2001) 192 - 199

ENC (series) vs. power and shaping time

NMOS, 0.5 µm technology





Input device optimization for BJT

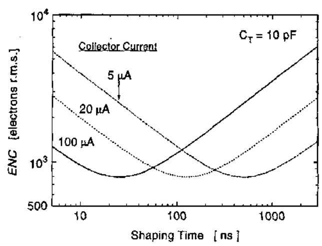
$$ENC^2 = a_1 \frac{C_T^2 (kT)^2}{I_C t_m} + a_2 \frac{I_C t_m}{\beta}$$

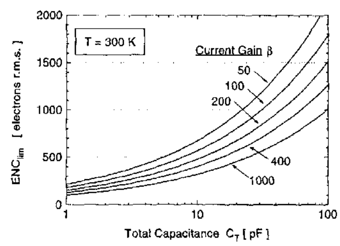
series white collector current shot noise

parallel base current shot noise

$$I_{C,opt} = \sqrt{\frac{a_1}{a_2} \frac{\beta k T C_T}{q t_m}}$$

$$ENC_{\min} = \sqrt{\frac{4 a_1 a_2}{\beta}} \cdot k T C_T$$





Bertuccio et al. , NIM A 409 (1998) 286 - 290

MOS vs. BJT front end

- MOS is favored over BJT for low noise when

$$\frac{t_m}{\tau_{el,MOS}} > \frac{8}{3a_2} \beta_{BJT}$$ white noise dominated MOS

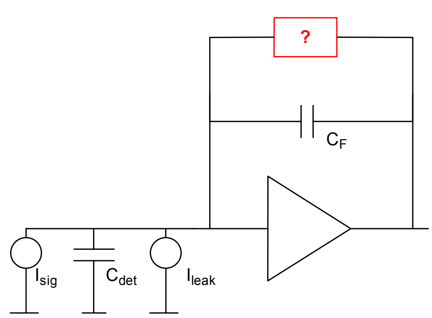
$$\frac{kT}{K_{F,MOS}} > \frac{a_3}{a_1 a_2} \beta_{BJT}$$ 1/f noise dominated MOS

$$\boxed{\frac{g_m t_m}{C_{\det}} = \sqrt{\frac{2\mu I_D}{L^2 C_{\det}}} t_m > \frac{8}{3a_2} \beta_{BJT}}$$

- MOS is favored for long t_m, low C_{det}, high power, and short gate length technology.
- MOS 1/f limit always superior to BJT if power budget is high enough:

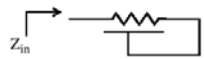
$$I_D > \left(\frac{kT}{K_F}\right)^2 \frac{C_{gs} L^2}{\mu t_m^2}$$

Preamp reset – requirements



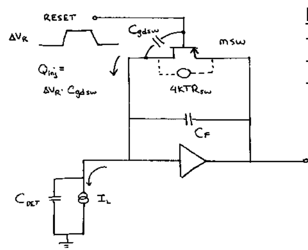
- all charge preamplifiers need DC feedback element to discharge the input node and stabilize the bias point
- usually, a resistor in the MΩ – GΩ range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - *insensitive to process, temperature, and supply variation*
  - *low capacitance*
  - *lowest possible noise*
  - *linear*

Preamplifier reset – monolithic techniques (1)



$$i_n^2 = \frac{4kT}{Re\{Z_{in}\}}$$

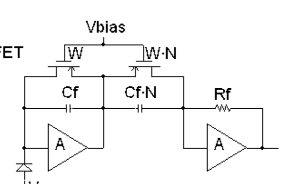
Physical resistor
- always accompanied by parasitic capacitance
- de-stabilizes circuit and increases noise
- noise higher than 4kT/R by factor ~ RC/t_m



Pulsed reset by MOS switch
- sampled noise $\sqrt{kTC_F}$
- Q_{inj} noise from switch control voltage
- leakage current integrates on output node $dV_{out}/dt = I_L/C_F$

Preamplifier reset – monolithic techniques (2)

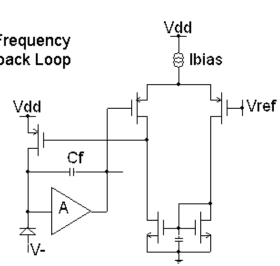
Single MOSFET



O'Connor et al., TNS v44 n3 (1997)
De Geronimo et al., NIM A421 (1999)
De Geronimo et al., TNS v47 n4 (2000)

- provides effective current gain -N
- full compensation (high linearity)
- minimum noise (thermal)
- requires baseline stabilization
- can be realized in multiple stages

Low Frequency Feedback Loop

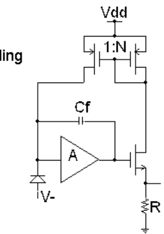


Krummenacher, NIM A350 (1991)
Ludewigt et al., TNS v41 n4, (1994)
Vandenbussche et al., TNS v45, n4 (1998)
Manfredi et al., Nucl.Phys.B 61B, Proc.Suppl. (1998)

- noise can be high
- requires baseline stabilization at high rates
- compensation an issue

Preamplifier reset – monolithic techniques (3)

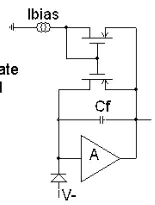
R-Scaling



Santiard et al., CERN-ECP/94-17 (1994)
Chase et al., NIM A409 (1998)
Sampietro et al., Elec.Lett. v34 n19 (1998)

- noise can be high (large values of R and N required)
- linearity an issue
- parasitic capacitor an issue
- compensation available in some configuraitions
- requires baseline stabilization

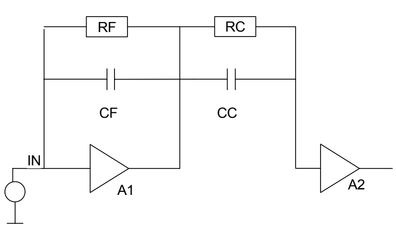
Slew-rate Limited



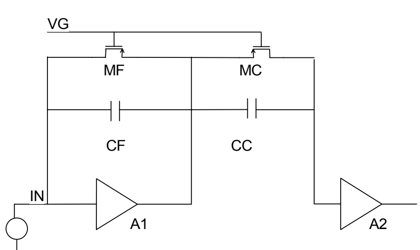
Blanquart et al., NIM A395 (1997)
Blanquart et al., NIM A439 (2000)

- MOSFET operates in saturation only when there is signal activity
- noise can be high (it requires Ibias > Idet)
- parasitic capacitor an issue
- suitable for Time-Over-Threshold processing techniques
- requires baseline stabilization at high rates
- linearity an issue
- compensation an issue

Nonlinear pole-zero compensation



- Classical
  - RF · CF = RC ·CC
  - Zero created by RC,CC cancels pole formed by RF, CF

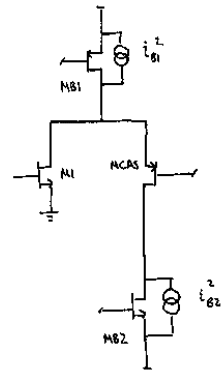


- IC Version
  - CC = N · CF
  - $(W/L)_{MC} = N \cdot (W/L)_{MF}$
  - Zero created by MC, CC cancels pole formed by MF, CF
  - Rely on good matching characteristics of CMOS FETs and capacitors

G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

Secondary noise sources in the preamp

- i_{B1}^2 and i_{B2}^2 are effectively in parallel with the input transistor
- Their contribution to input (white) thermal series noise is $(g_{mB1}/g_{m1})^2$.
- We minimize their g_m w.r.t. that of M1
- $g_{mB1,2} = \sqrt{2\mu C_{ox} W I_D / L}$
- use low W/L (i.e. long-gate) devices with large or degenerate with source resistor.
- Keep W/L as small as possible (thus V_{gs}-V_T large) while keeping $V_{DS} > V_{gs}$-V_T.
- Various ways to optimize.



Preamplifier Design – Summary

- Optimum noise performance requires selecting, biasing, dimensioning, and laying out the input device properly.
- Bipolar transistor is favored input device for fast, low-power front ends.
- Noise scaling:

$$ENC \propto \frac{C_{\det}^{\alpha}}{t_m^{\beta} P^{\gamma}}$$

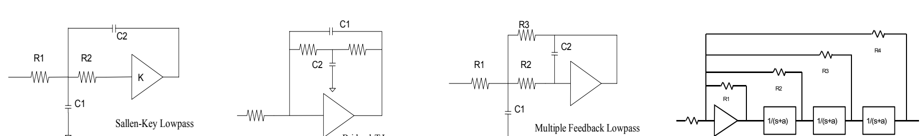
$$0.75 < \alpha < 1$$
$$\beta \approx 0.5$$
$$0.25 < \gamma < 0.5$$

- A substantial design effort is needed to realize a low-noise, high-linearity reset system in monolithic technology.

Integrated shaping amplifiers

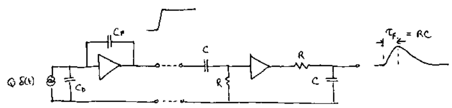
- Limits the bandwidth for noise
- Gives controlled pulse shape appropriate for rate
- Control baseline fluctuations
- Bring charge-to-voltage gain to its final value
- By its saturation characteristics, sets upper limit on Q_{in}
- Feedback circuits give the most stable and precise shaping
  - *At the expense of power dissipation*
  - *Poor tolerance of passives limits accuracy of the poles and zeros*
- High-order shapers give the lowest noise for a given pulse width

Filter topologies



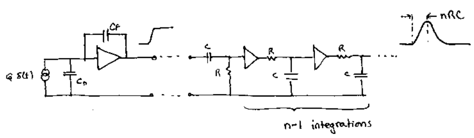
Pulse shaping filters with real poles

Simplest filter: CR-RC

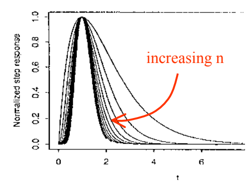


• asymmetric response

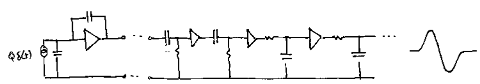
CR-RC^n, unipolar semiGaussian



• Identical real poles
• Symmetry improves with order n:



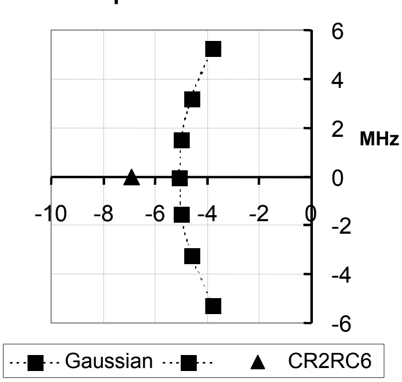
CR^2-RC^n, bipolar semiGaussian



• Area-balanced
• Derivative of CR-RC^n

Complex pole approximation to Gaussian pulse

Shaper Pole Positions



Ohkawa synthesis method (Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers")

For given filter order, gives closest approx. to a true Gaussian

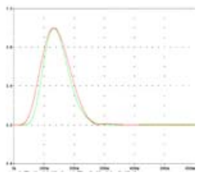
More symmetrical than CR-RC^n filter of same order for same peaking time

Noise weighting functions:

$I_{1,complex}/I_{1,CR\text{-}RC}$ = 1.18 series

$I_{2,complex}/I_{2,CR\text{-}RC}$ = 0.81 parallel

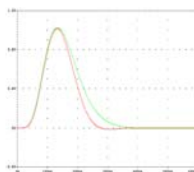
Complex shapers -- advantages



7th order complex

12th order CR-RC^n

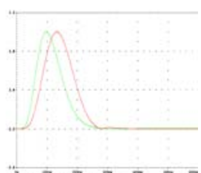
Equal peaking times, equal 1% widths



7th order complex

7th order CR-RC^n

Equal peaking times, equal order



7th order complex

7th order CR-RC^n

Equal 1% widths, equal order

Power requirements

- Fundamental limit – power per pole

$$P_{pole} \geq 8kTf_0 \cdot DR,$$

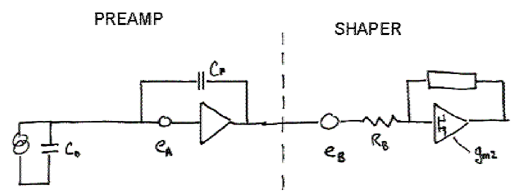
$$f_0 : \text{pole frequency} \cong \frac{n_{pole}}{t_m} \qquad DR = \frac{\text{peak signal}}{\text{noise}}$$

- Stable, low distortion filters cannot use active element for setting pole frequency

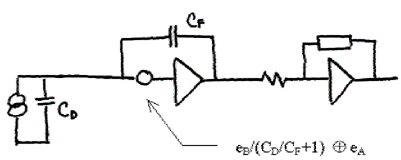
  ⇒ *Require higher GBW amplifiers, more power*

- Use topologies that realize more than one pole per amplifier
- Trim time constants using digitally switched passive elements

Second-stage noise



Transform e_B to the input:

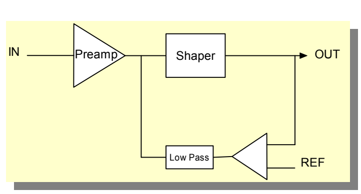


$$\frac{ENC_B}{ENC_A} = \frac{C_F}{C_D} \cdot \left(\frac{R_B}{R_A}\right)^{1/2}$$

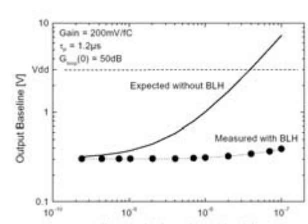
Baseline stabilization

Baseline can move due to:
1. DC coupling to detector with variable leakage
2. Temperature and power supply drift
3. Rate fluctuations in a system with AC coupling

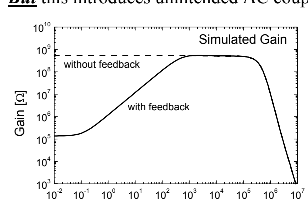
(1) and (2) can be prevented by low frequency feedback circuit:



Result:

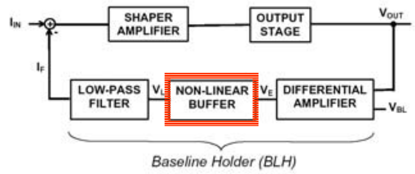


But this introduces unintended AC coupling:

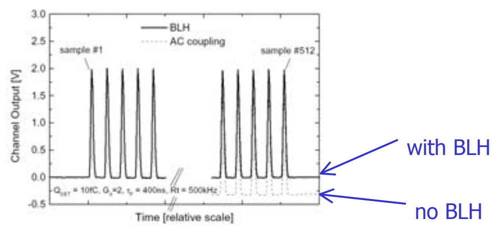


Baseline holder

Introduce a nonlinear element into the feedback loop:



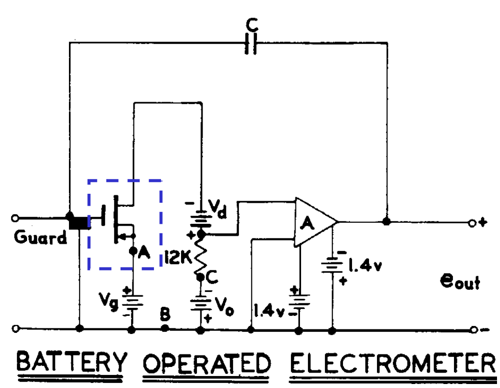
After a long train of pulses the baseline stays constant:



Outline

- Custom monolithic front ends
  - *advantages*
  - *access to technology*
  - *design tools*
- Low noise analog design in monolithic CMOS
  - *preamplifier design*
  - *shaping amplifier*
- Circuit examples
- CMOS Scaling and Charge Sensitive Amplifier design
  - *noise mechanisms in scaled devices*
  - *optimum capacitive match to detector*
  - *noise, dynamic range, and power vs. scaling length*

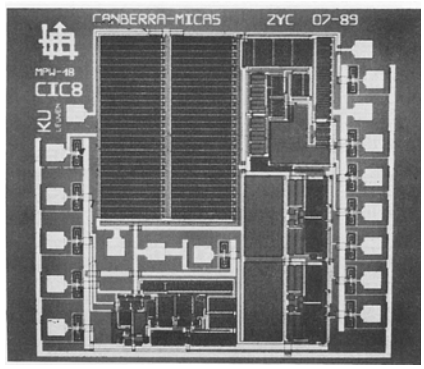
Charge Amplifier based on Silicon MOSFET (1967)



V. Negro et al., "A Guarded Insulated Gate Field Effect Electrometer", IEEE Trnas. Nucl. Sci. Feb. 1967, 135 – 142

J.B. McCaslin, "A Metal-Oxide-Semiconductor Electrometer Ionization Chamber", UCRL-11405 (1964)

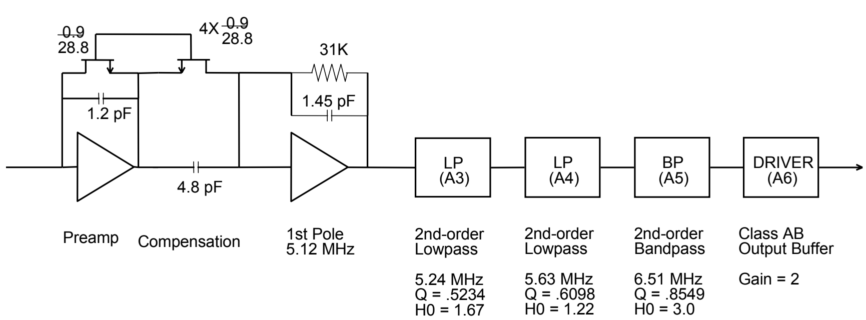
Spectroscopy amplifier (1989)



Technology	3.0 µm CMOS
Power Supply	+/- 5V
Chip size	2.5 x 2.5 mm
Channels	1
C_{det}	300 - 1000 pF
Reset	external resistor
Shaping	CR-RC^4, 1.6 µs
ENC	3800 + 4.1 e$^-$/pF
Power dissipation	96 mW

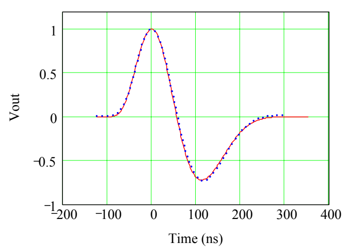
Z. Chang, W. Sansen, *Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*, Kluwer 1991 Ch. 5

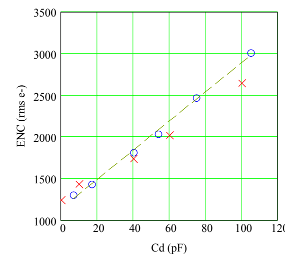
Preamp-shaper for cathode strip chamber



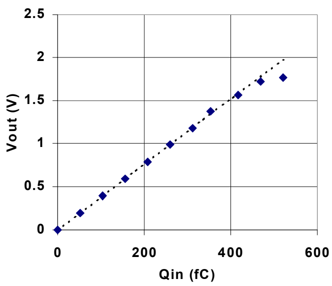
- Detector: cathode strips of 0.5m MWPC with 50 pF C_{DET}
- Charge interpolation to 1/100 of the strip pitch
- Fast (70 ns), 7th order bipolar shaping for charged particle tracking in high rate environment

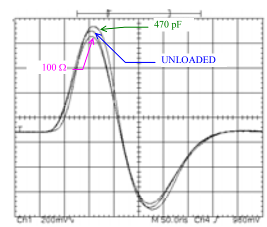
Preamp-shaper for Cathode Strip Chamber





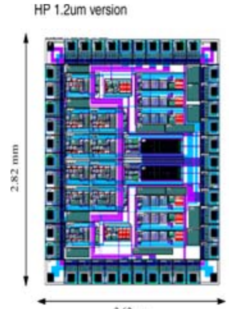
Simulated: ω
Measured: O





Drift detector preamplifier

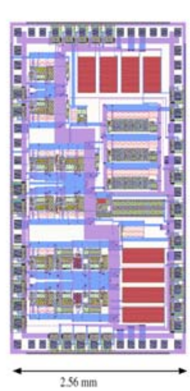
HP 1.2um version



Requirements for 100 eV resolution with a 0.2 pF detector at 1 - 5 μs shaping time:

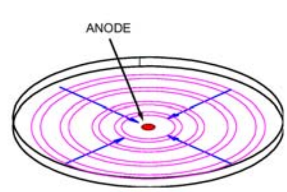
- I_{leak} < 10 pA
- R_F > 3 GΩ
- g_m > 0.4 mS
- $K_F < 1.8 \times 10^{-25}$ J

AMS 1.2um version

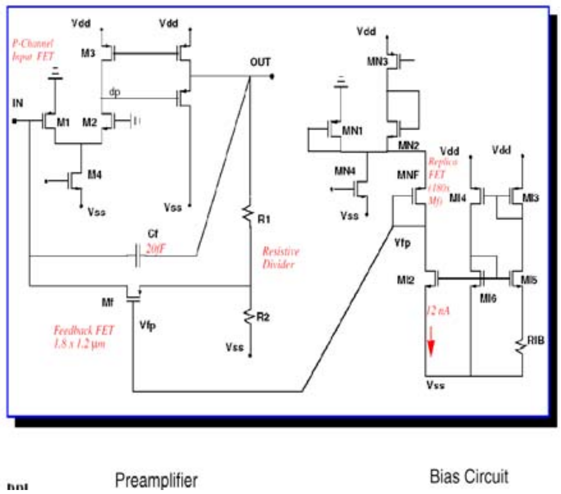


- Used with ultra-low capacitance silicon drift detector, C_{det} < 0.3 pF
- Preamp only, used with external shaper
- Purpose: explore lowest noise possible with CMOS
- Reset system: MOS transistor with special bias circuit to achieve stable, > 100 GΩ equivalent resistance

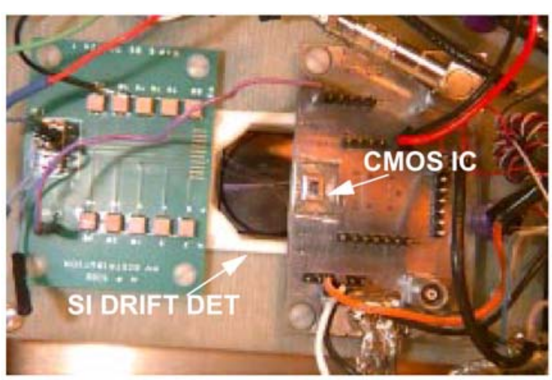
Detector



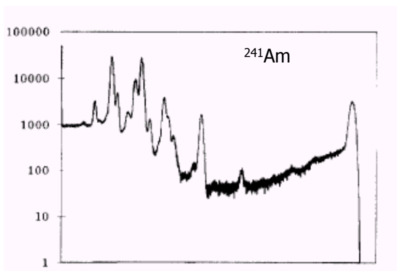
Drift detector preamplifier – simplified schematic

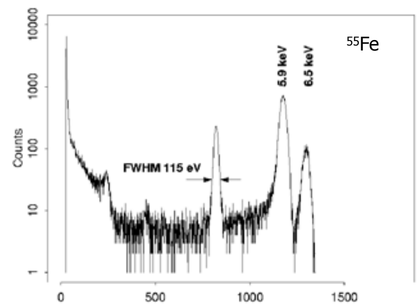


Drift detector & CMOS preamplifier



Drift detector preamplifier – results

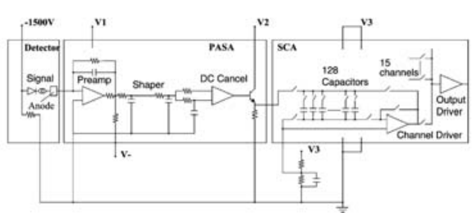


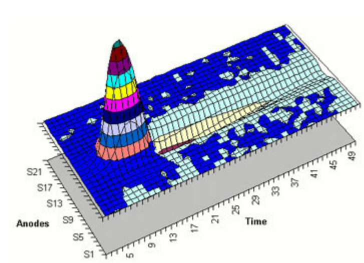


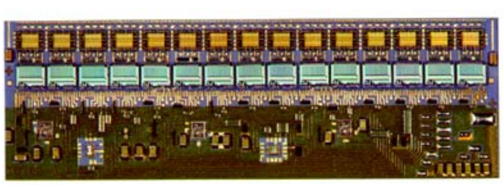
- Spectra of ^{241}Am and ^{55}Fe taken with 5mm Φ Si drift detector and CMOS X-ray preamplifier. Detector and circuit cooled to -75 C.
- External 2.4 μs shaping.
- ENC = 13 e^- rms.
- Noise without detector: 9 e^-

P. O'Connor et.al., "Ultra Low Noise CMOS Preamplifier-shaper for X-ray Spectroscopy", NIM A409 (1998), 315-321

SVT 240-channel multi-chip module







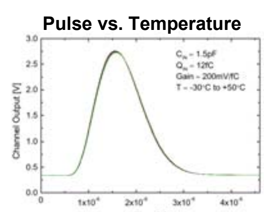
D. Lynn et al., "A 240 channel thick film multi-chip module for readout of silicon drift detectors", NIM A439 (2000), 418 - 426

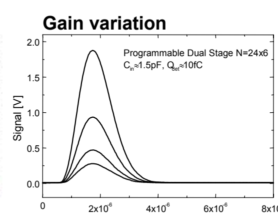
BNL Preamp/Shaper ICs, 1995 - 2001

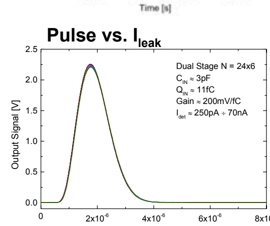
PROJECT	Hi-res. Spectroscopy	RHIC – PHENIX	RHIC – STAR	LHC – ATLAS	Industry Partnership	NSLS – HIRAX	Units
DETECTOR	Si drift	Time Expansion Chamber	Silicon Vertex Tracker	Cathode Strip Chamber	CdZnTe gamma ray detector	Si Pixel	
Function	Preamp	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper/ Counter	
C_{DET}	0.3	30	3	50	3	1.5	pF
Peaking Time	2400	70	50	70	600:1200:2000:4 000	500:1000:2000:4 000	ns
Gain	10	2.4:12 – 10/25	40:70:90	4	30:50:100:200	750:1500	mV/fC
Power	10	30	3.8	33	18	7	mW/channel
ENC	10	1250	400	2000	100	24	rms electrons
Dynamic Range	1250	4600	700	1900	5600		
Technology	CMOS 1.2 um	CMOS 1.2 um	Bipolar 4 GHz	CMOS 0.5 um	CMOS 0.5 um	CMOS 0.35 um	
Input Transistor	PMOS 150/1.2 um	NMOS 4200/1.2 um	NPN 10 uA	NMOS 5000/0.6 um	NMOS 200/0.6 um	PMOS 400/0.4 um	
Reset Scheme	Compensated PMOS, > 1GΩ	Polysilicon, 75 kΩ	Nwell, 250 kΩ	Compensated NMOS, 30 MΩ	Compensated PMOS	Compensated NMOS	
No. Channels	6	8	16	24	16	32	
Die Size	7.3	15	8	20	19	16	mm^2

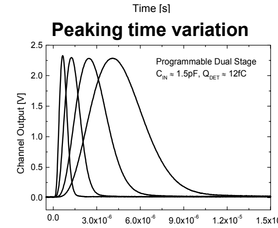
Practical amplifier considerations

- Preamplifier reset
- High order filters
- Programmable pulse parameters
- Circuit robustness:
  - Self-biasing
  - Low-swing,differential I/O
  - Circuits tolerant to variations in
    - Temperature
    - Process
    - Power supply
    - DC leakage current
    - Loading









	I_{leak}	Supply	Temperature	Rate (to 5/tp)	Cin	Zload
Gain	< 0.1%/nA	<.001%/V	-0.04%/°C	< 0.1%	<0.1%/pF	No slew-rate limit
Baseline	< 0.3mV/nA	<30 µV/V	75 µV/°C	< 8 mV	-	Zout ~ 150 Ω

G. De Geronimo et al., "A generation of CMOS readout ASICs for CZT detectors", IEEE Trans. Nucl. Sci. 47, Dec. 2000, 1857 - 1867

Outline

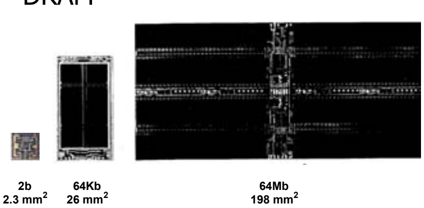
- Custom monolithic front ends
  - *advantages*
  - *access to technology*
  - *design tools*
- Low noise analog design in monolithic CMOS
  - *preamplifier design*
  - *shaping amplifier*
- Circuit examples
- CMOS Scaling and Charge Sensitive Amplifier design
  - *noise mechanisms in scaled devices*
  - *optimum capacitive match to detector*
  - *noise, dynamic range, and power vs. scaling length*

Scaling issues

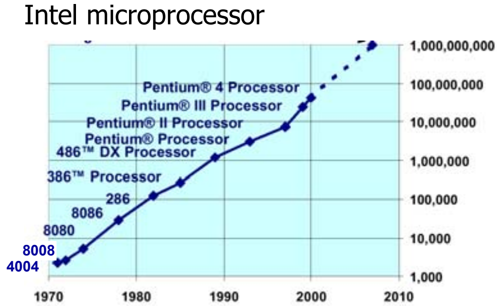
- Fundamental device noise mechanisms
  - *Hot electron effects*
  - *New process steps effect on 1/f noise*
  - *Gate tunneling current*
- Change of the current-voltage characteristics
  - *Increase of weak inversion current*
  - *Mobility decrease*
  - *Velocity saturation*
  - *Drain conductance (device intrinsic DC gain)*
- Power supply scaling

CMOS Scaling

DRAM



Intel microprocessor



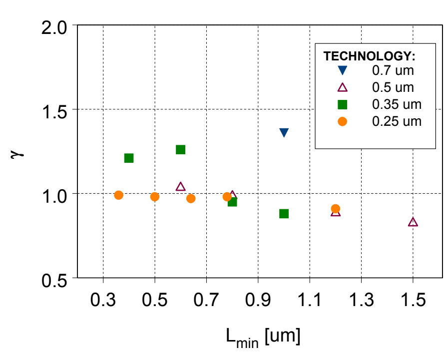
- Driven by digital VLSI circuit needs
- Goals: in each generation
  - *2X increase in density*
  - *1.5X increase in speed*
  - *Control short channel effects*
  - *Maintain reliability level of < 1 failure in 10^7 chip-hours*

CMOS Technology Roadmap

Year	85	88	91	94	97	00	02	04	07	10	13
Min. feature size [µm]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.10	0.07
Gate oxide [nm]	44	33	22	16	11	7.7	5.5	4.0	2.9	2.2	1.6
Power supply [V]	5	5	5	5	5/3.3	3.3	2.5	1.8	1.2	1	.7
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5	0.45	0.4	0.3	0.3	0.3

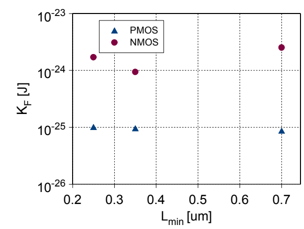
Series white noise

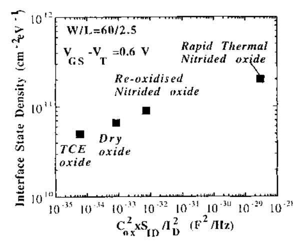
- Parameter γ = gm * Rn
- Some models predict γ >> 1 for short channel devices
- At moderate inversion and low VDS, γ remains in the range $0.8 < \gamma < 1.4$
- Shallow junctions increase S/D series resistance => noise



1/f noise in submicron CMOS

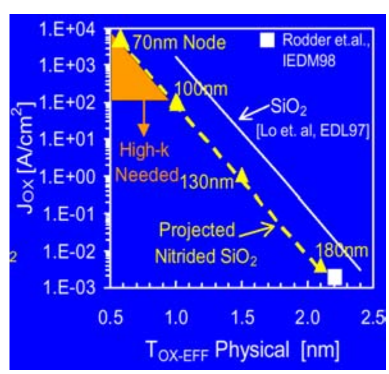
- Processes with n+/p+ poly gates and retrograde wells create surface-channel PMOS – PMOS 1/f noise to become more like NMOS?
- Shallow junctions required for scaled processes limit the thermal budget – hence gate process will have reduced post-oxidation anneal and higher trap density, higher 1/f
- For ultrathin gates new dielectrics with higher trap densities will be used (nitrided, halogenated, H2 annealed)





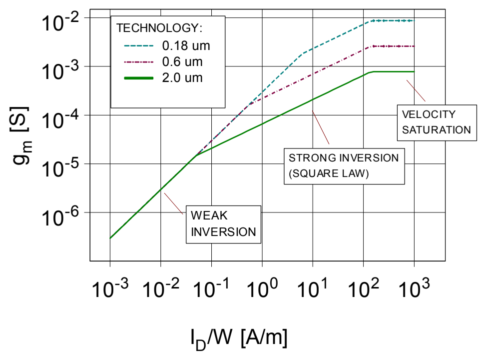
Gate tunneling current

- Gate current expected to increase 100 – 200 x per generation below 0.18 μm
- J_{ox} ~ 100 A/cm^2 projected for L_{min} = 0.1 μm generation with nitrided SiO_2
- Considered tolerable for digital circuits (total gate area per chip ~ 0.1 cm^2)
- Typical CSA input FET would have I_G ~ 1 - 10 μA; ENCp ~ 2000 - 7000 rms e- at 1 μsec



SiO_2 gate leakage current (Lo et al., Electron Dev. Letters 1997)

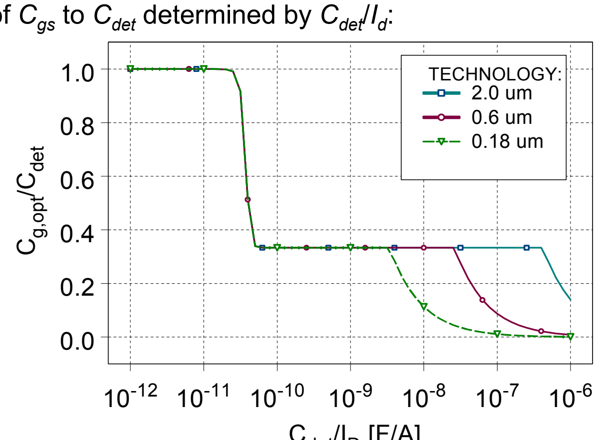
Departure from square-law characteristics



- Submicron devices are less often operated in strong inversion, square-law region.
- By the 0.13 mm generation, the square-law region will vanish altogether

Generalized capacitive matching condition

– Drain current = constant
– Ratio of C_{gs} to C_{det} determined by C_{det}/I_d:



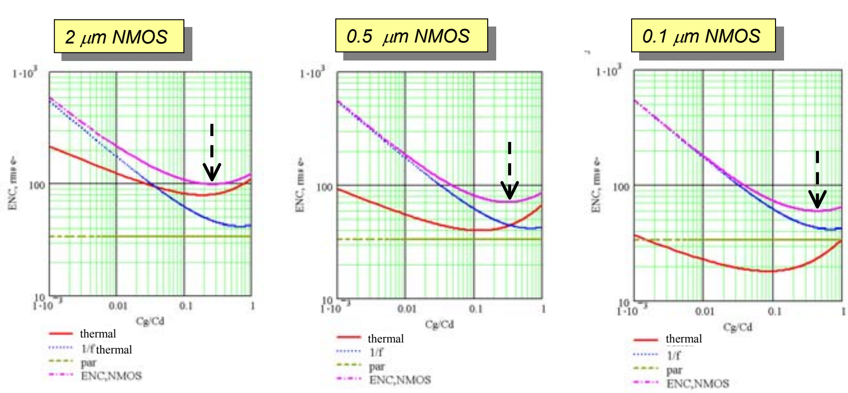
P. O'Connor, G. De Geronimo, "Prospects for Charge Sensitive Amplifiers in Scaled CMOS", NIM-A accepted for publication

Example – strong inversion limits

- NMOS input device
- I_D = 250 μA
- 2 μm technology:
  - *9.3 fF < C_{det} < 26.3 pF*
- 0.18 μm technology:
  - *9.3 fF < C_{det} < 210 fF*

Capacitive match vs. scaling – mixed white, 1/f and parallel noise

- *The contribution of thermal and 1/f changes as technology scales*
- *Example:* C_{det} = 3 pF, t_m = 1 μs, P_{diss} = 1 mW, I_{leak} = 100 pA:

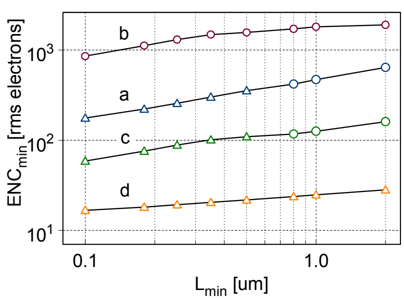


Noise vs. scaling for mixed white, 1/f, and parallel noise

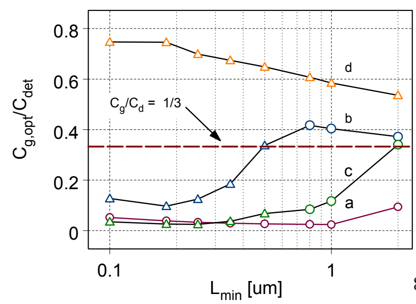
4 detector scenarios for scaling study

System	C_{det}	t_s	P	I_{leak}	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

Noise vs. scaling



Optimum gate width vs. scaling



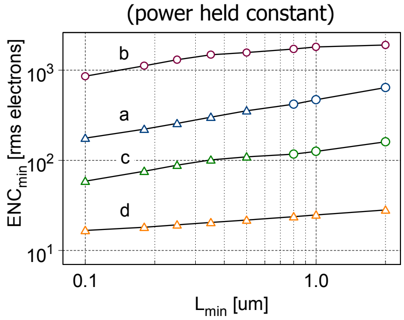
Noise and power vs. scaling

4 detector scenarios for scaling study

System	C_{det}	t_s	P	I_{leak}	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

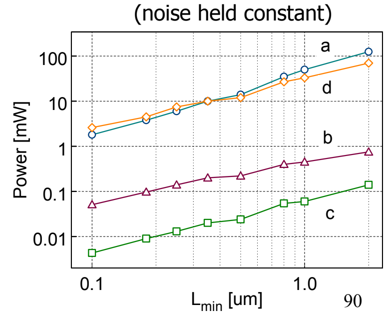
Noise vs. scaling

(power held constant)

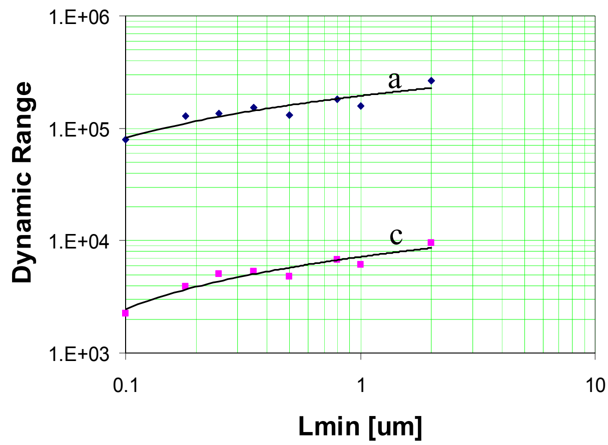


Power vs. scaling

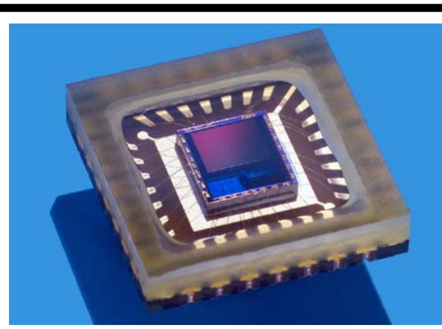
(noise held constant)

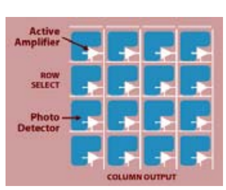


Dynamic range vs. scaling



Active Pixel Sensor: radiation detector in standard CMOS





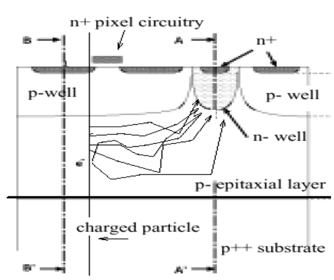
http://www.photobit.com

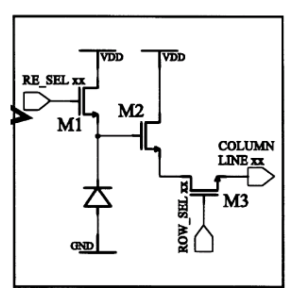
CMOS APS for particle detection/tracking

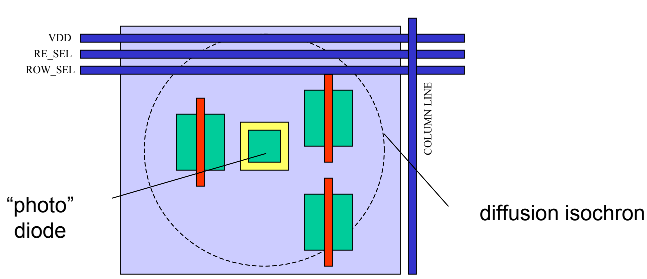
- Monolithic –special assembly technology not required
- Low cost
- Low multiple scattering
- Good spatial resolution (few µm)
- Random access
- Integration of control and DSP
- Radiation tolerance (?)

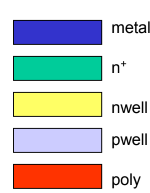
- Special process
- Collection time scales with pixel size
- Circuit architecture embryonic

Simple monolithic active pixel









Comparison of bump-bonded and active pixel sensors for tracking

	Bump-bonded sensor	Active pixel	
Technology	hybrid	monolithic	
MIP signal charge	< 24000	800	e-
ENC noise charge	100 – 300	20 – 50	e- rms
Pixel area	20,000	< 400	μm^2
Sensor capacitance	200	< 10	fF
Detector bias	100	1	V
Charge collection time	< 20	depends on pixel area	ns

Charge amplifiers in scaled CMOS – summary

- Fundamental noise mechanisms
  - *so far, no dramatic changes with scaling*
- Noise
  - *slight improvement with scaling*
  - *higher device f_T reduces series thermal noise*
- Weak- and moderate inversion operation more common
  - *need different matching to detector capacitance.*
- Reduced supply voltage
  - *difficult to get high dynamic range*
- Many difficulties with “end of the roadmap” devices

Summary and Future Directions

- Today's monolithic technology can be used effectively for low-noise front ends.
- Technology scaling, by reducing the area and power per function, wil allow increasingly sophisticated signal processing on a single die.
- Integrated sensors will be developed for some X-ray and charged-particle tracking applications.
- Interconnecting the front end to the detector and to the rest of the system will continue to pose challenges.