11061 PGN

Power, Ground and Noise

UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

Class Objective

When you finish this class you will:

- Understand the importance of considering noise early in the design cycle
- Understand the nature of electrical noise
- Observe the impact of good design practice
- Know where to find additional resources from the website and EMC community at large

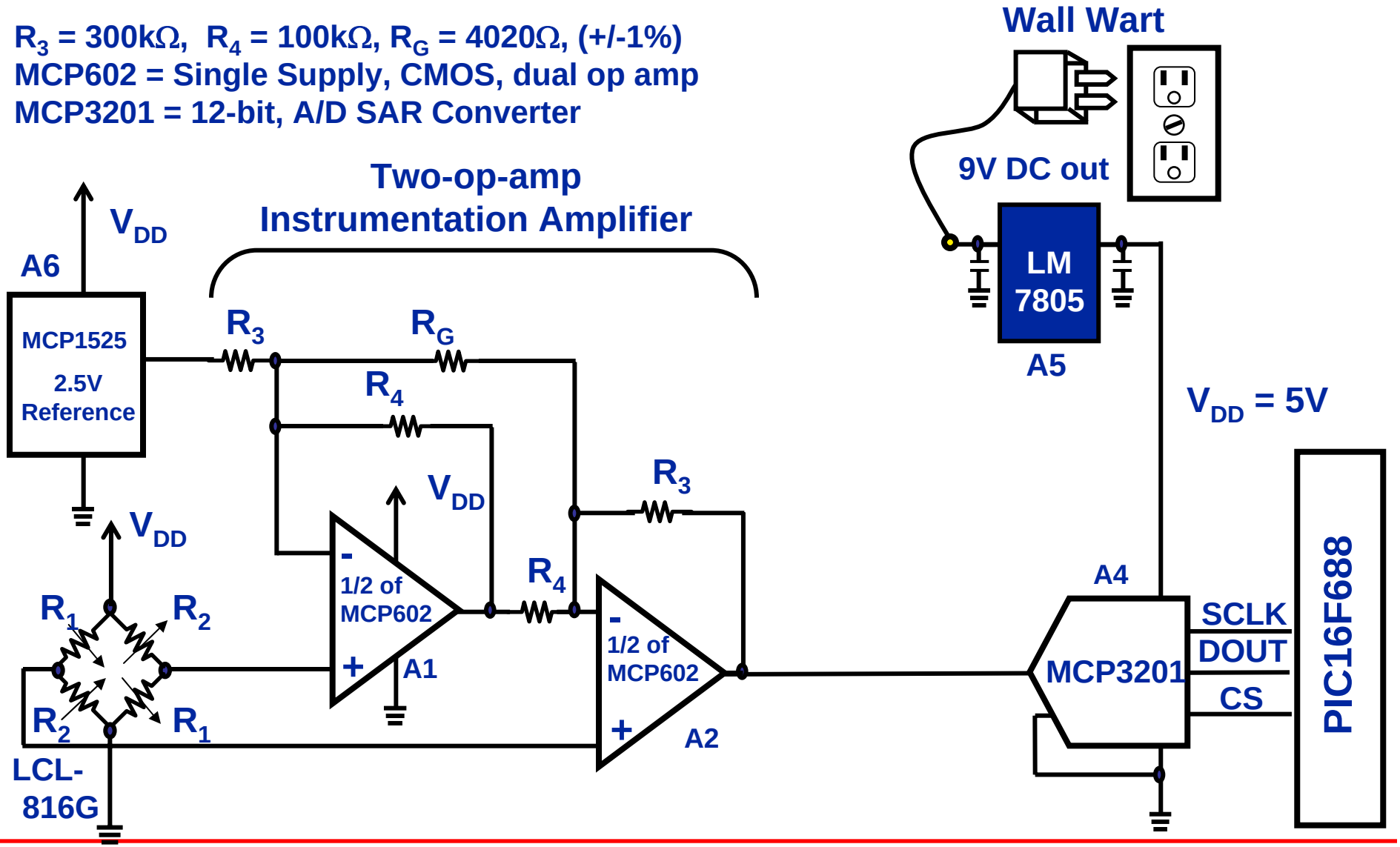
University of Microchip UofM MASTERs 2007

Agenda

- **Consequences of Designing with no Regard to Noise**
- **Areas to Concentrate on**
  - Device Noise
  - Conducted Noise
  - Radiated Noise
- **Test Results of a Good Design**

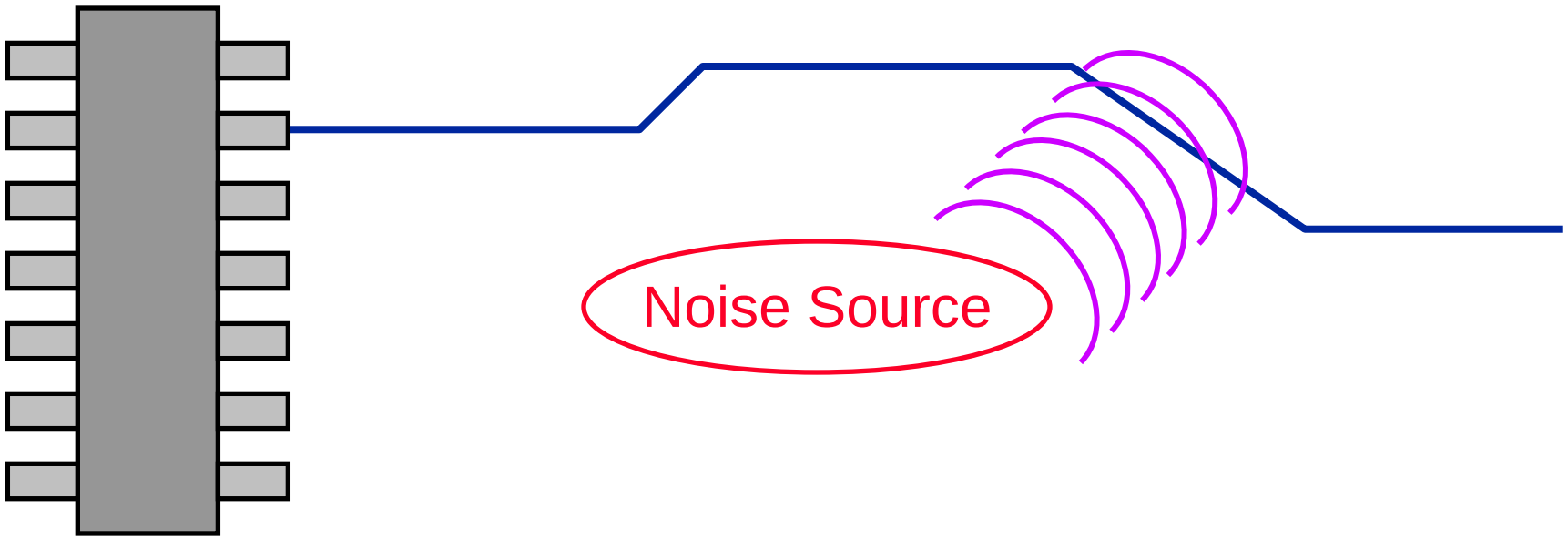
Application Circuit

R_3 = 300kΩ, R_4 = 100kΩ, R_G = 4020Ω, (+/-1%)
MCP602 = Single Supply, CMOS, dual op amp
MCP3201 = 12-bit, A/D SAR Converter



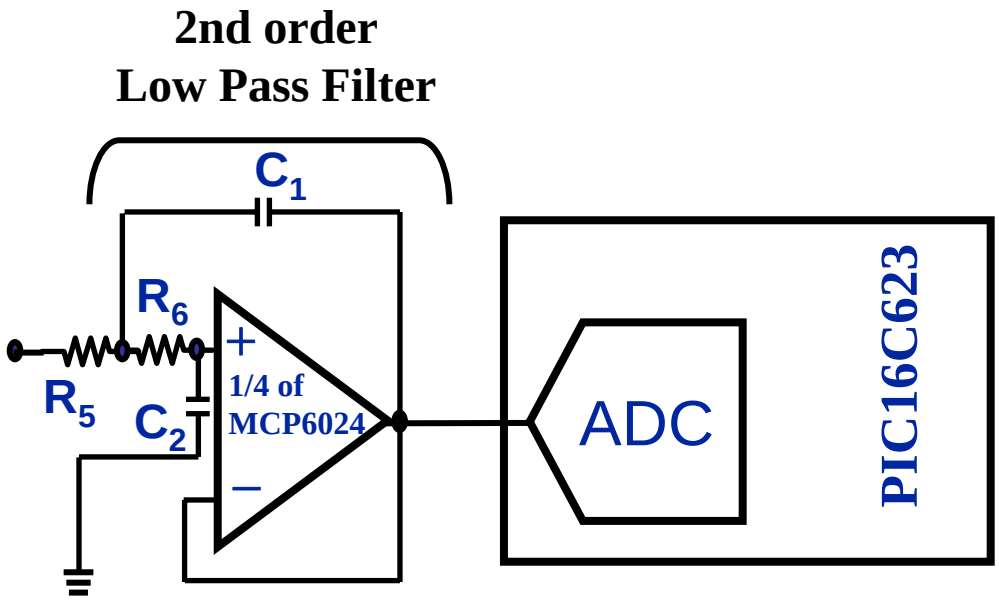
Long Traces: Antenna

- **A trace going into an ADC input longer than a few inches is a potential antenna**



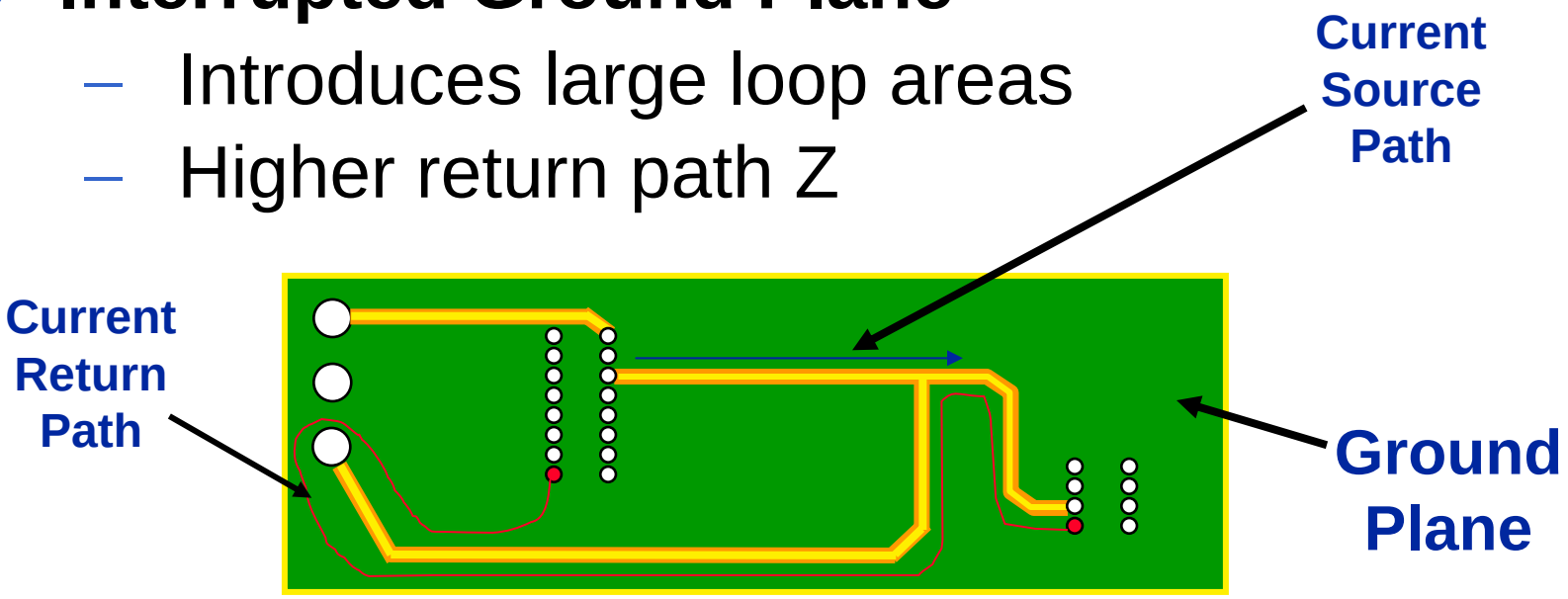
Low-Pass Filter Missing

- Traces going into ADC inputs longer than a few inches
- No anti-aliasing (or Low-Pass) Filter at the input of the ADC

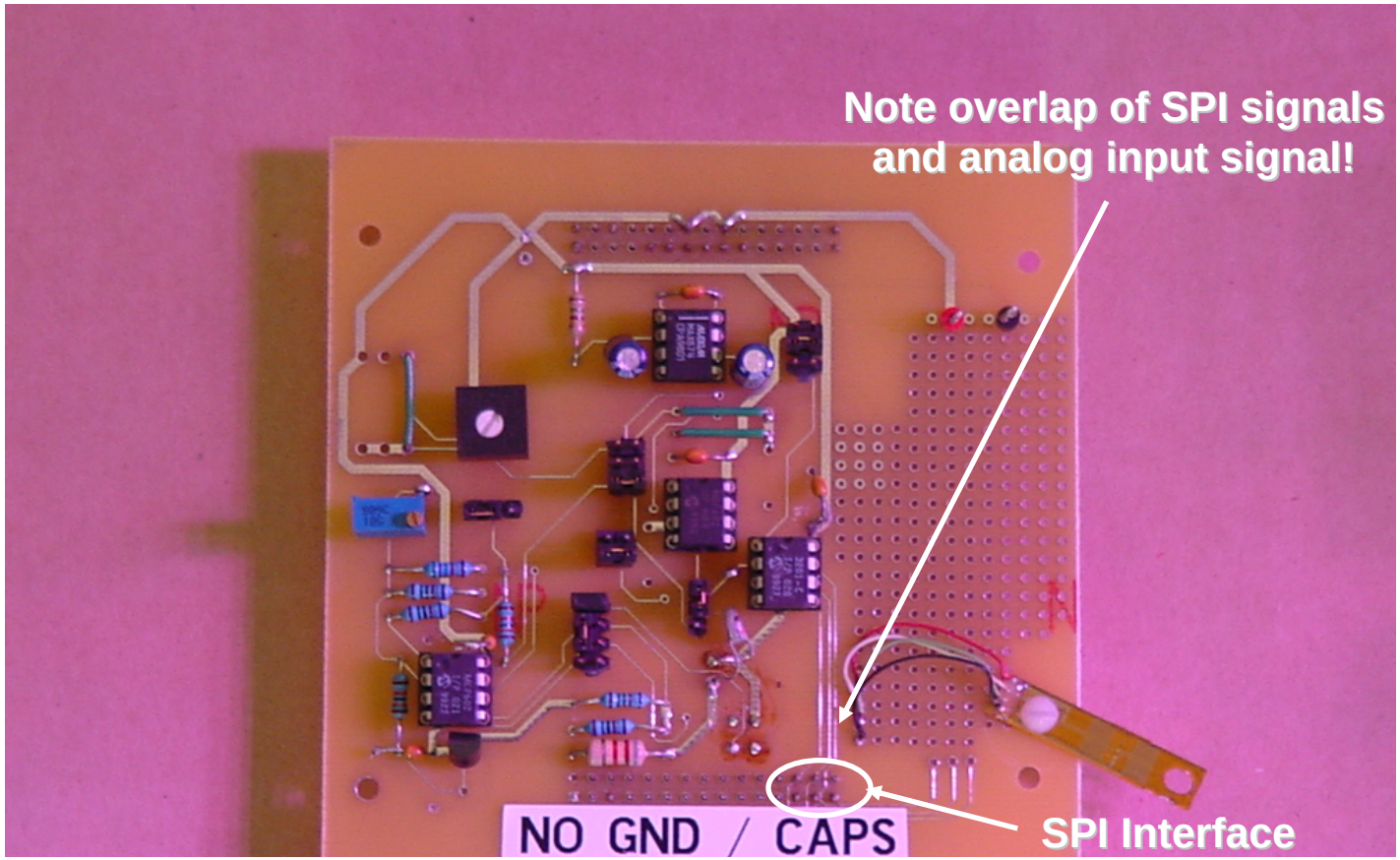


Discontinuous Ground Plane

- **Traces going into ADC inputs longer than a few inches**
- **No anti-aliasing (or Low-Pass) Filter at the input of the ADC**
- **Interrupted Ground Plane**
  - Introduces large loop areas
  - Higher return path Z

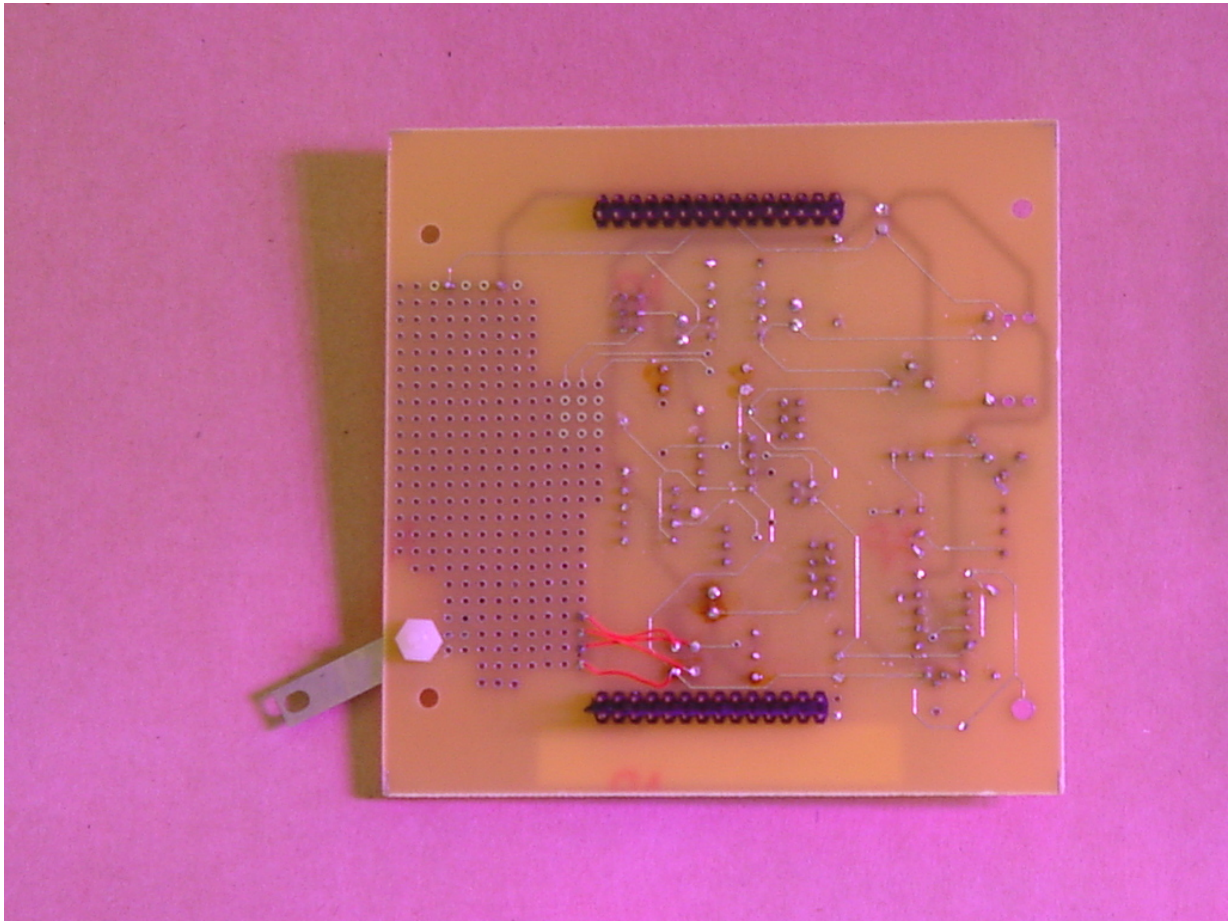


Application Board #1 (top side)



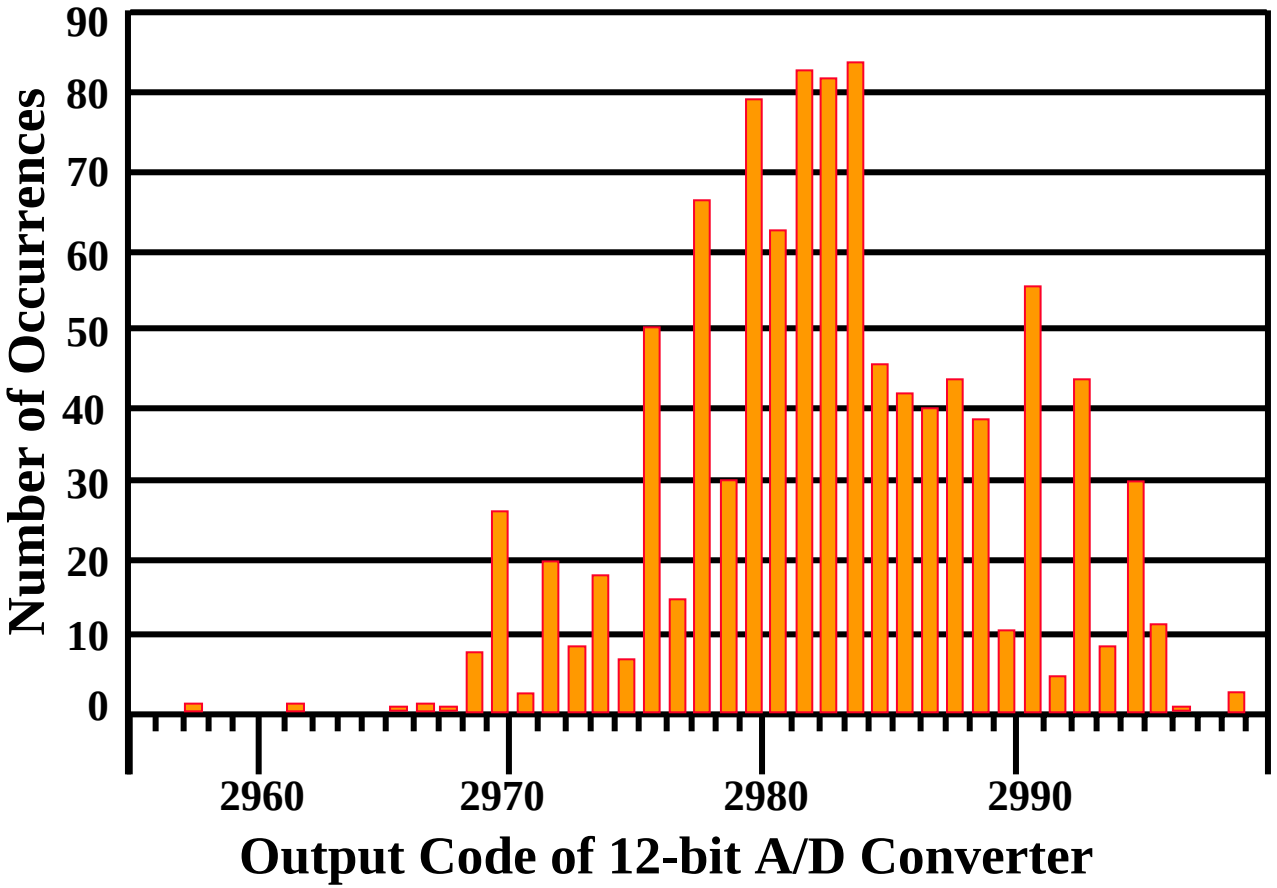
HIGHER VALUE RESISTORS / NOISY AMPLIFIER /
NO BY-PASS CAPS / NO LP FILTER / NO SUPPLY CHOKE

Application Board #1 (bottom side)



NO GROUND PLANE

Application Board #1 Test Results



Code Width of Noise = 44

(total samples = 1024)

UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

Low Noise Design

- **Device Noise – Created by the devices**
  - Resistors - Reduce Values were possible
  - Op amps - Use Lower Noise Amplifiers
- **Radiated Noise – Externally Generated**
  - Reduce trace loop areas within sensitive circuitry
  - Environment - Shield or change orientation
  - Filter low-level Signal traces
- **Conducted Noise – In the Circuit Traces**
  - Use a Continuous Ground Plane
    - Apply ‘moat’ concept to isolate digital & analog planes as needed
  - Layout - Keep analog and digital Separate
  - Filter low-level Signal traces
  - Filter/Decouple Supply traces
  - Power Supply - Replace Switching Devices

Device Noise

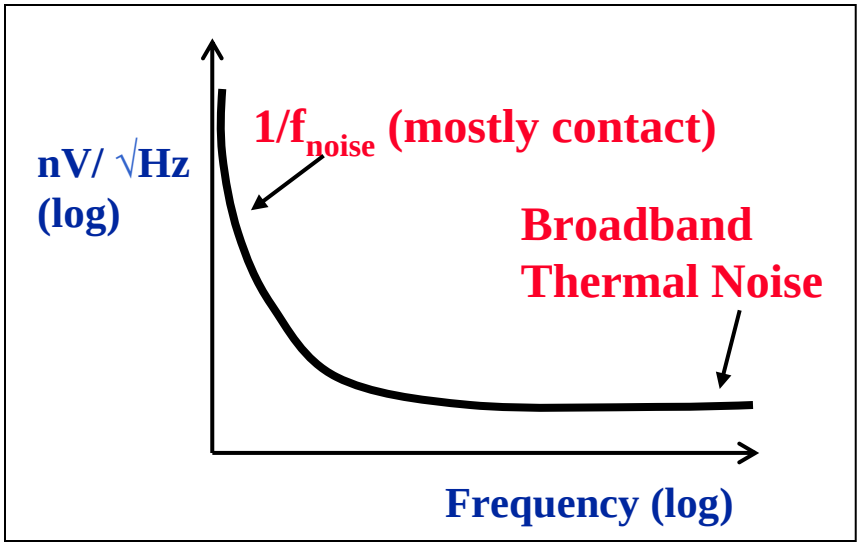
- **Resistors**
  - Johnson or Thermal Noise
  - $V_{RN} = \sqrt{4KTR(BW)}$ {Vrms}

    K = Boltzman's Constant = 1.38e $^{-23}$ JK^{-1}

    T = Temperature in Kelvin

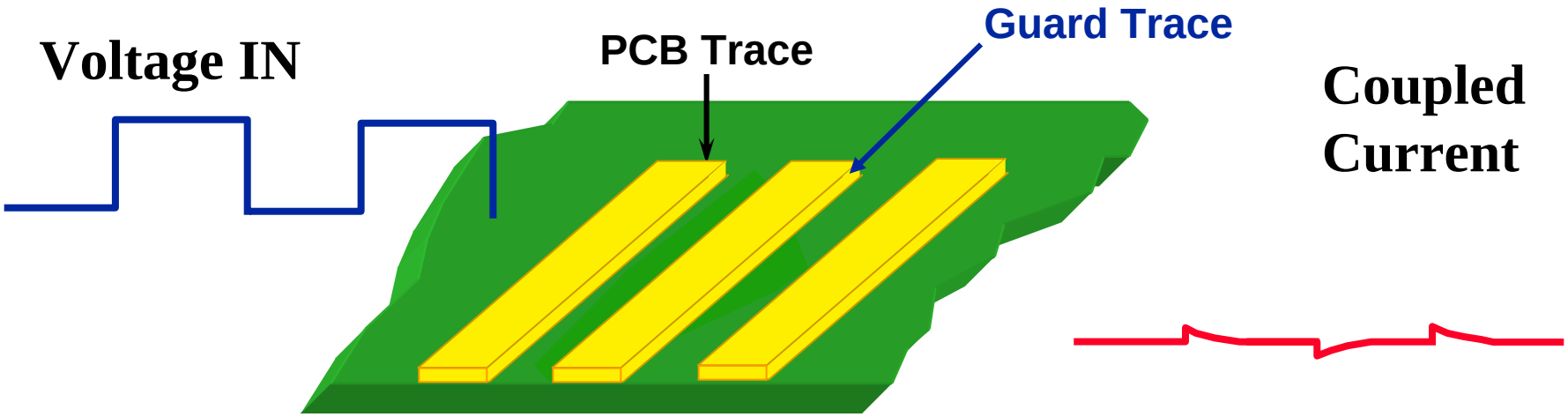
    R = Resistance in Ohms

    (BW) = Noise Bandwidth in Hz
    - **1kΩ = 4nV / $\sqrt{Hz}$**
- **Amplifiers**
  - MCP602 Specification - **29nV/ $\sqrt{Hz}$ @ 1kHz**
  - MCP6022 Specification - **10nV/ $\sqrt{Hz}$ @ 10kHz**



Coupled Noise (Crosstalk)

- Decrease “L” or Increase “d”
- Put Ground Guard Between Traces



$$C = \frac{w \bullet L \bullet e_o \bullet e_r}{d} \quad pF \qquad I = C \frac{dV}{dt} \ (amps)$$

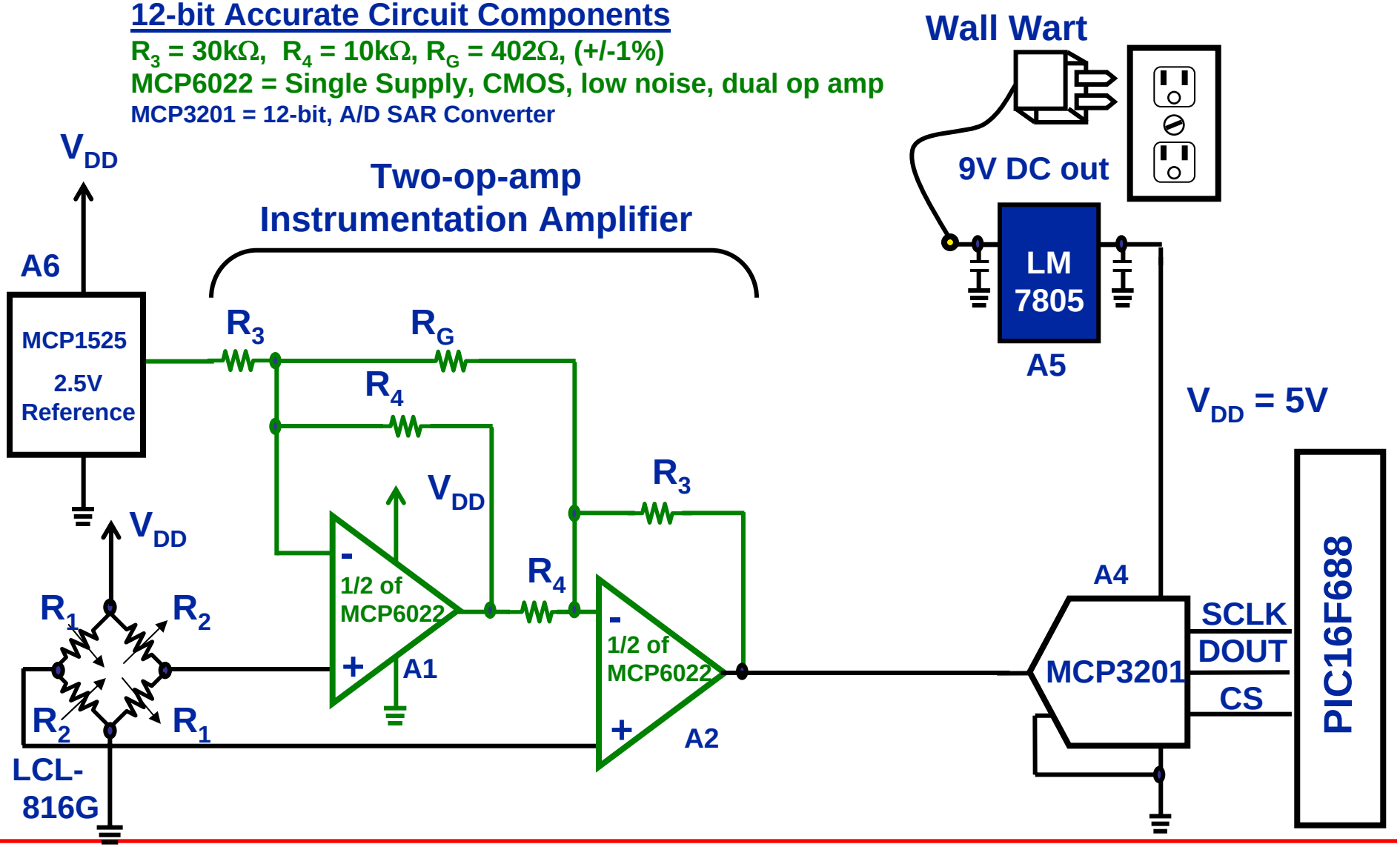
Application Circuit

12-bit Accurate Circuit Components

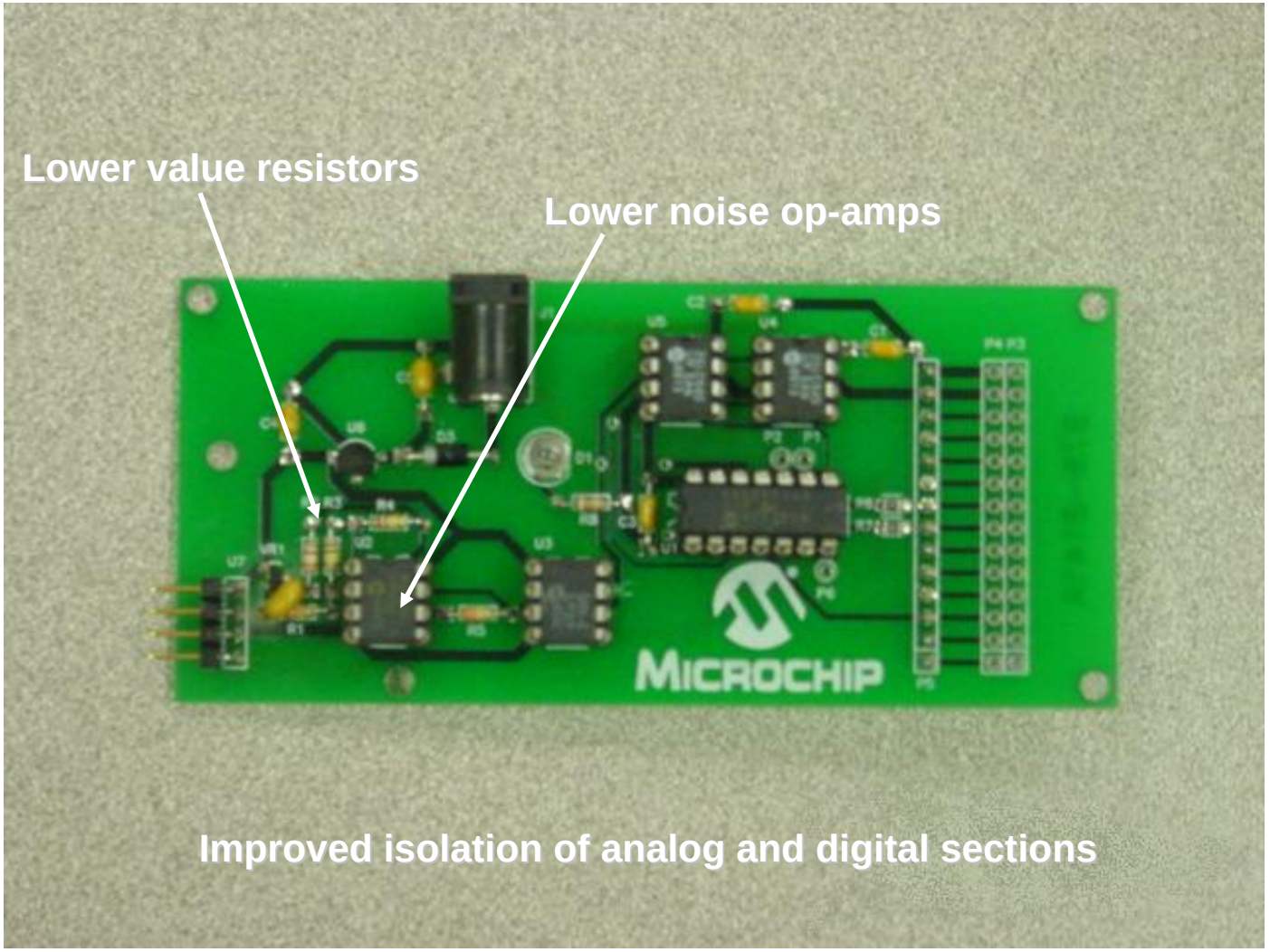
R_3 = 30kΩ, R_4 = 10kΩ, R_G = 402Ω, (+/-1%)

MCP6022 = Single Supply, CMOS, low noise, dual op amp

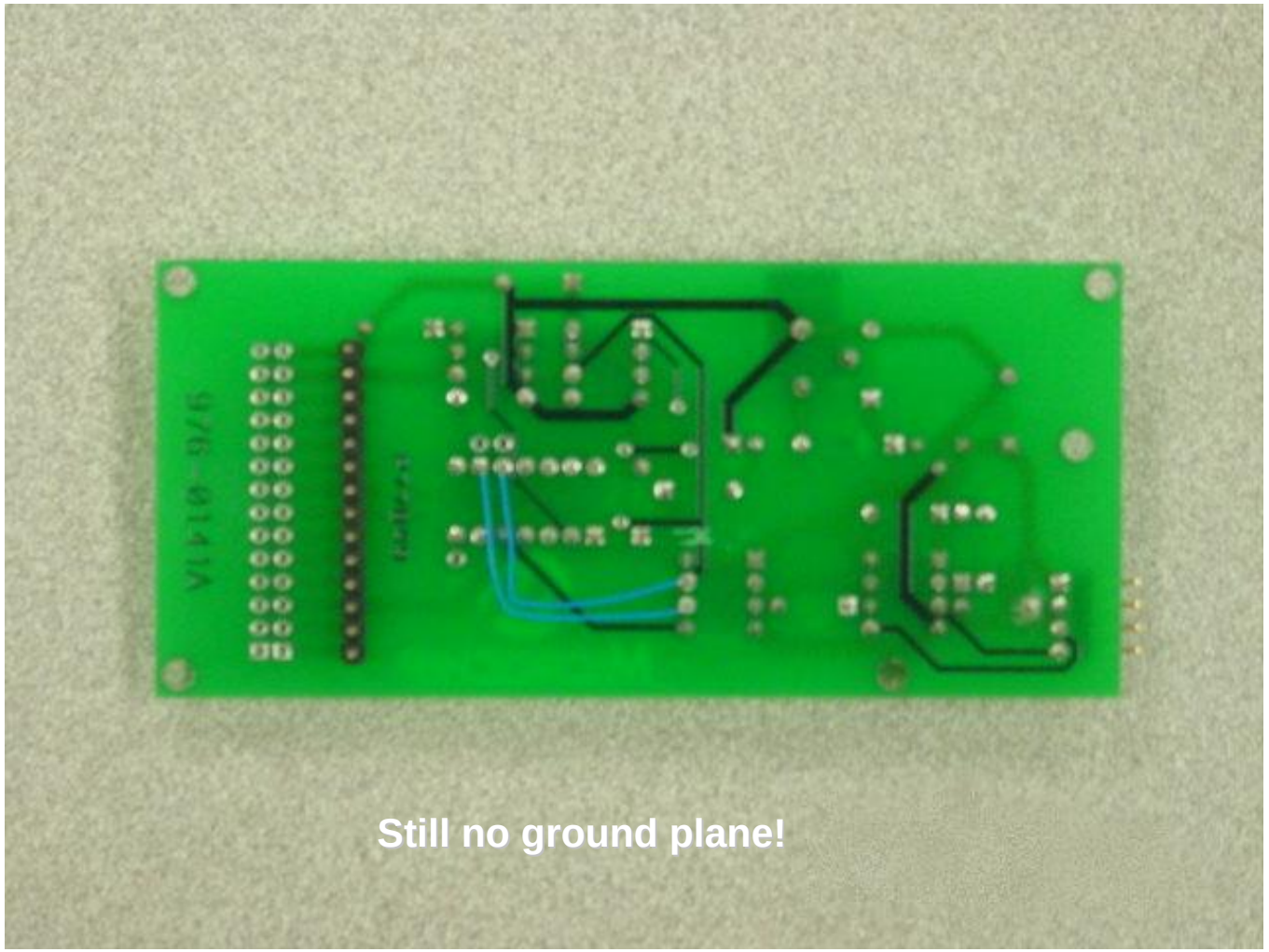
MCP3201 = 12-bit, A/D SAR Converter



Application Board #2 (top side)



Application Board #2 (bottom side)

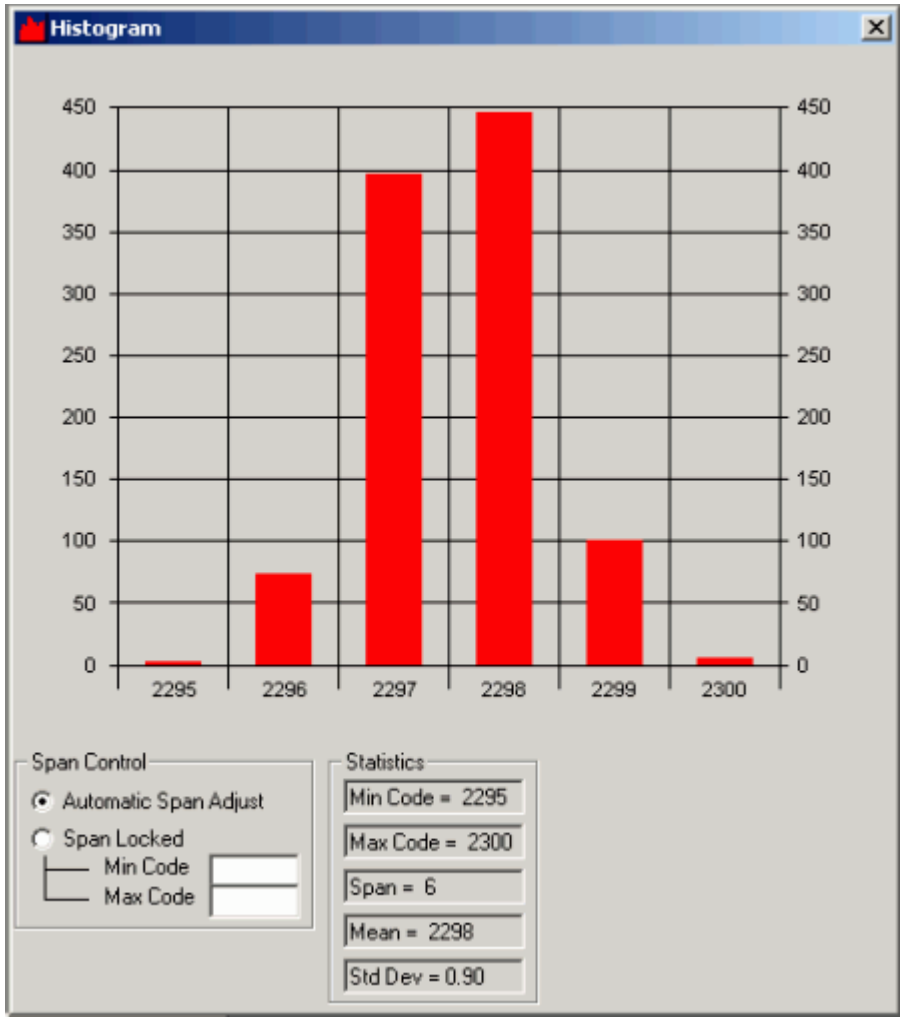


App Board #2 Test Results

Code Width of Noise = 6

(total samples = 1024)

- Causes:
  - **Environmental 50/60Hz noise on inputs**
  - **PCB common mode noise**



Conducted Noise

- **Ground and Power**
  - 50Hz or 60Hz environmental noise
  - Ground and Supply Current Return Paths

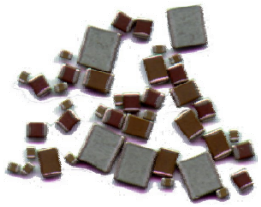
    Use continuous Ground Plane and Filter Supply traces
- **Signal Paths**
  - Digital Switching noise
  - Noise Generated by Previous Device

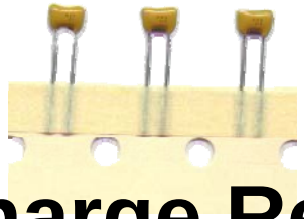
    Use Analog Filters

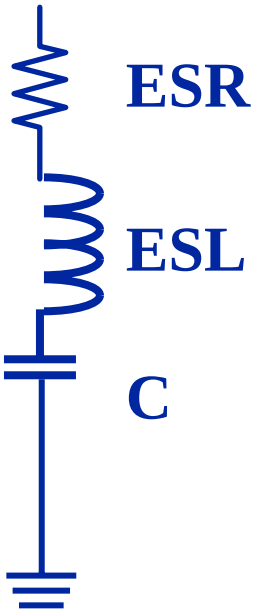
Bypass Capacitor Types

- **Filters Noise at High Frequency**
  - Ceramic - Small Case size, Inexpensive,

    Good Stability, Low Inductance
    - **NPO**
    - **X7R**



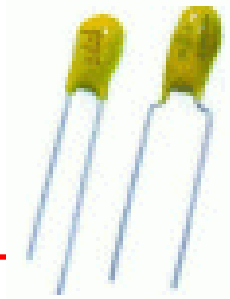




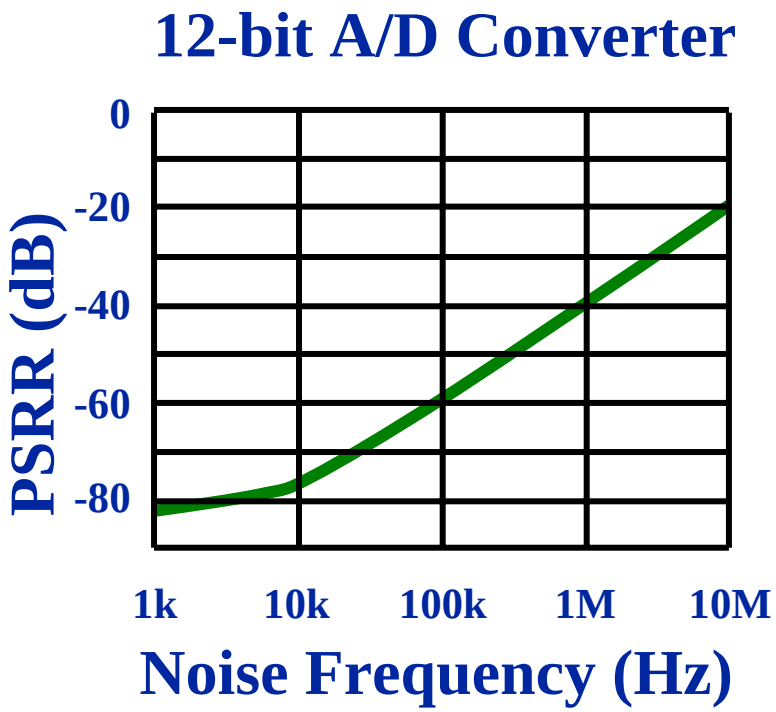
- **Acts as a Charge Reservoir for Fast Changes**
  - Tantalum Electrolytic - Small size,

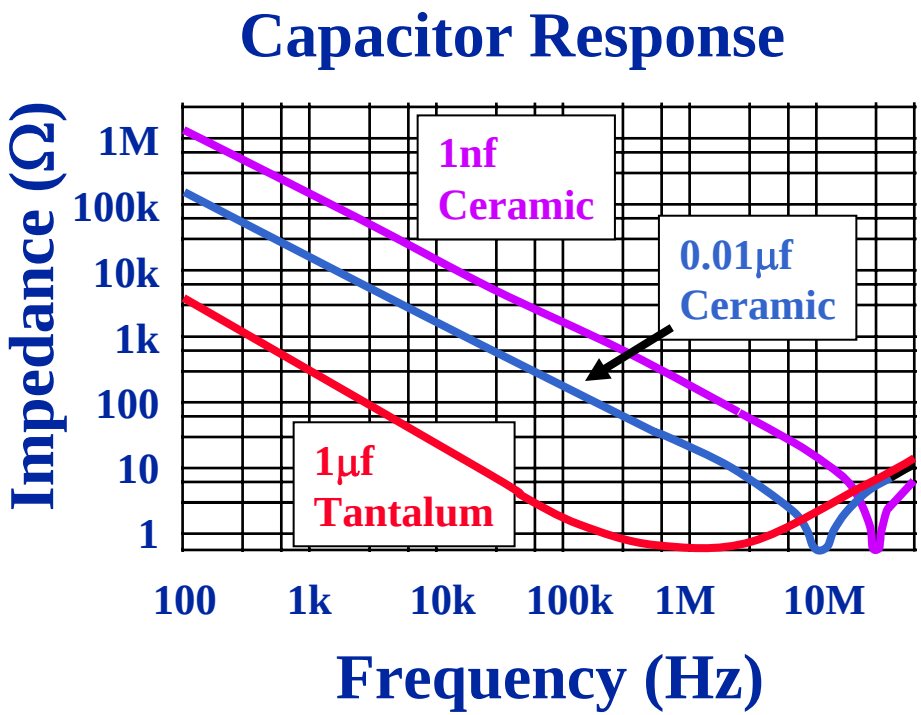
    Large Values,

    Medium Inductance



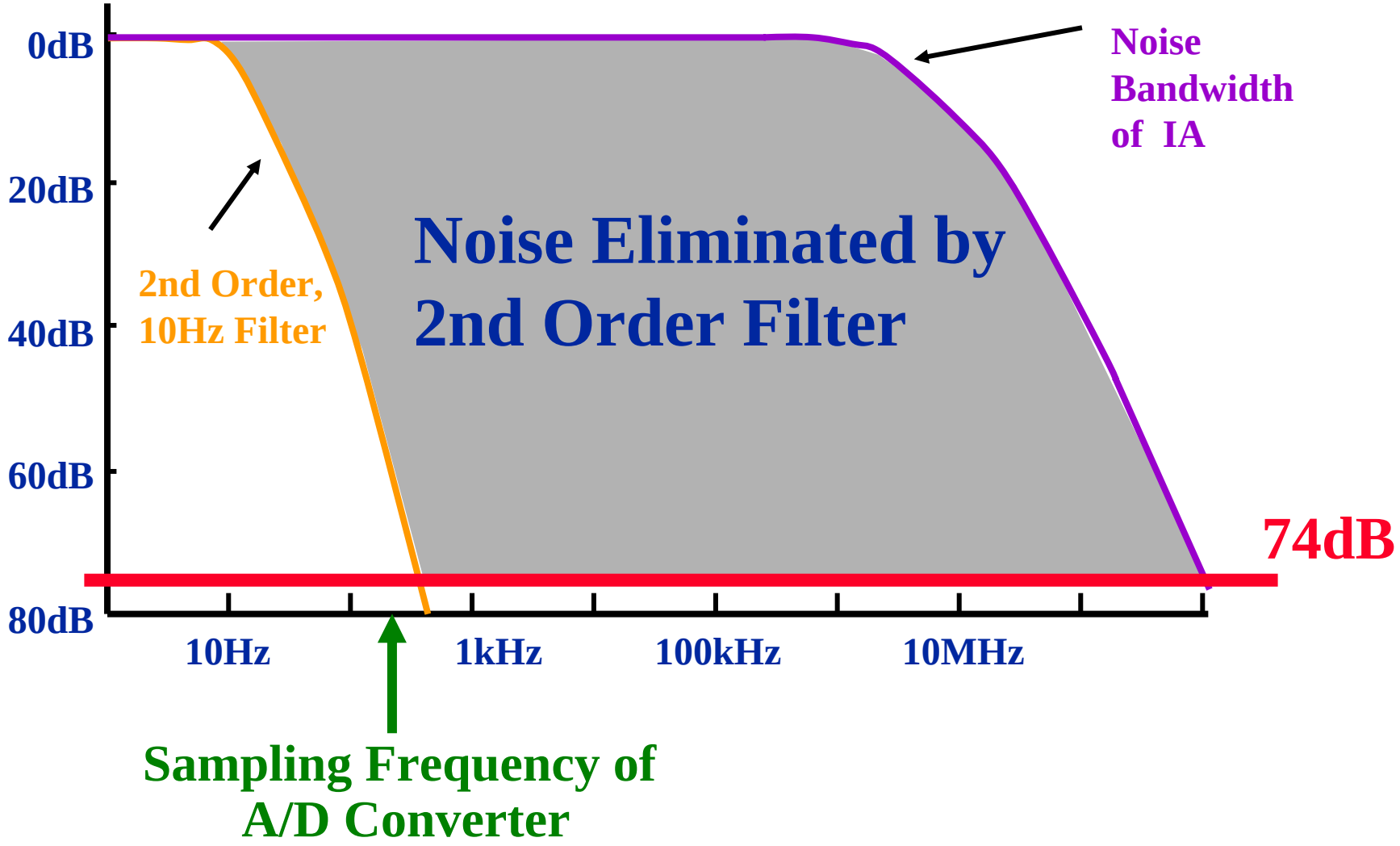
Response of Bypass Capacitors





- **Assume:** Supply = 5V ± 20mV (all white noise)
  - **To bring the noise to ± 1/4 LSB (± 0.61mV)**
  - **PSRR = 20 $\log_{10}$(δSignal / δVdd) < – 30.3dB**

Noise Reduction with Low Pass Analog Filter



Application Circuit

12-bit Accurate Circuit Components

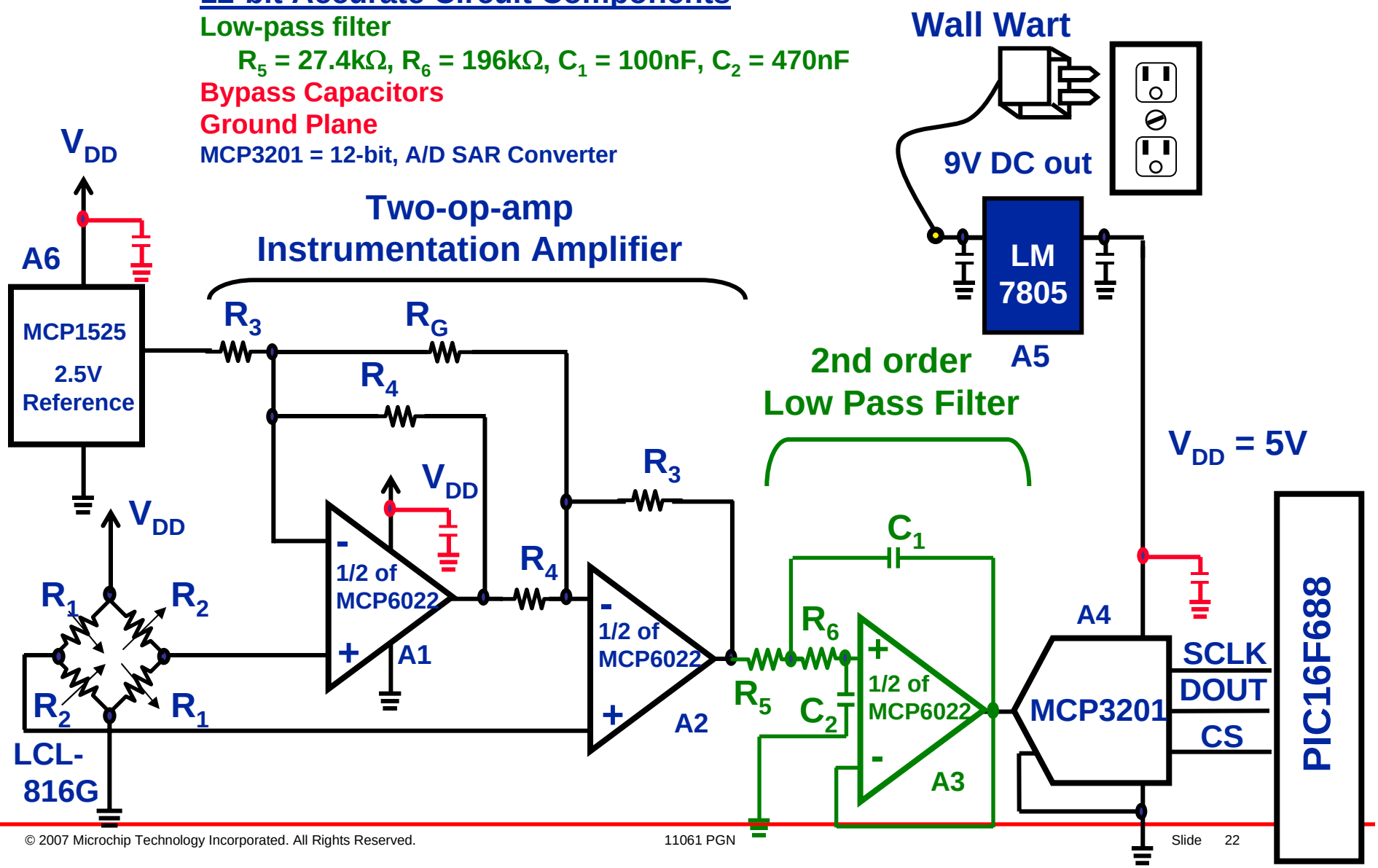
Low-pass filter

$R_5 = 27.4k\Omega$, $R_6 = 196k\Omega$, $C_1 = 100nF$, $C_2 = 470nF$

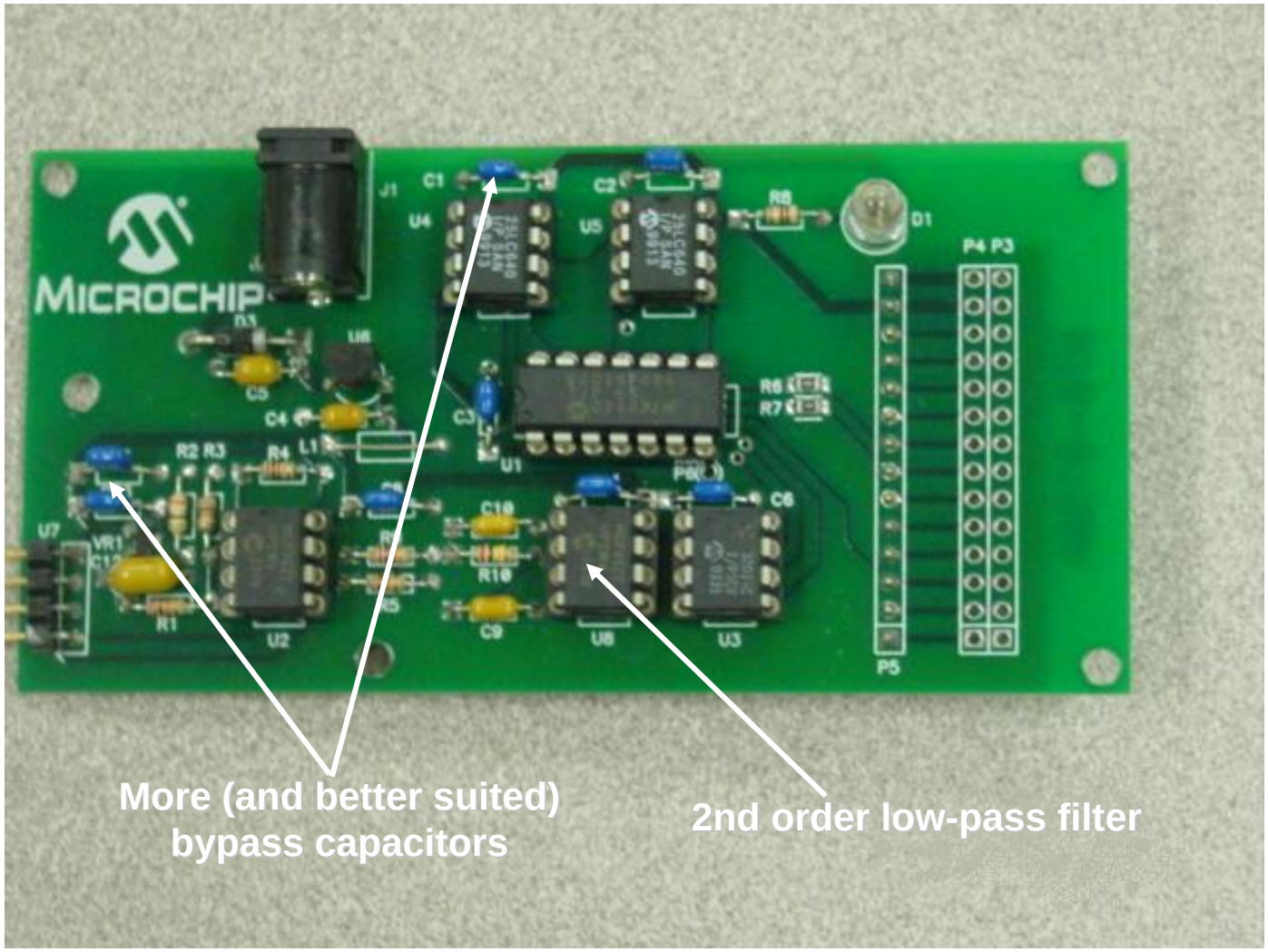
Bypass Capacitors

Ground Plane

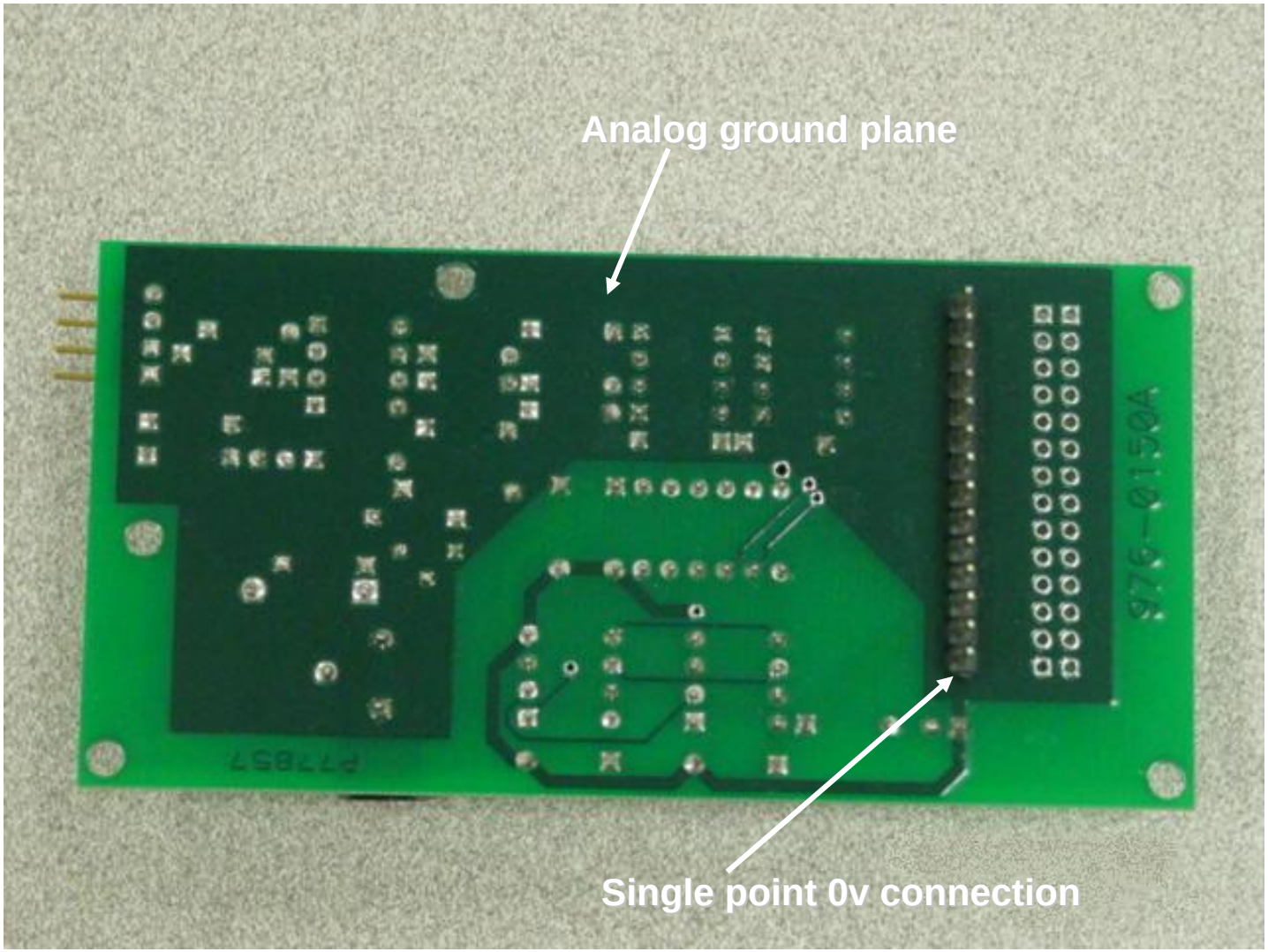
MCP3201 = 12-bit, A/D SAR Converter



Application Board #3 (top side)



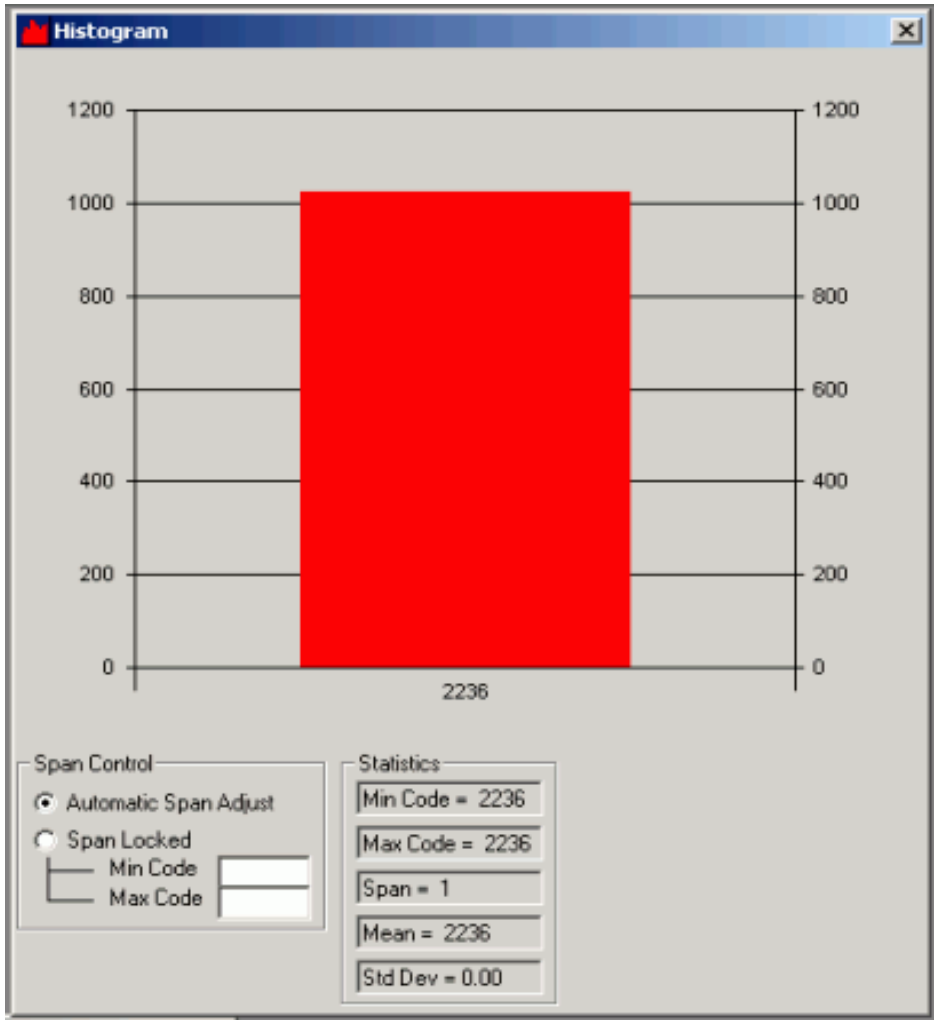
Application Board #3 (bottom side)



App Board #3 Test Results

Code Width of Noise = 1

(total samples = 1024)

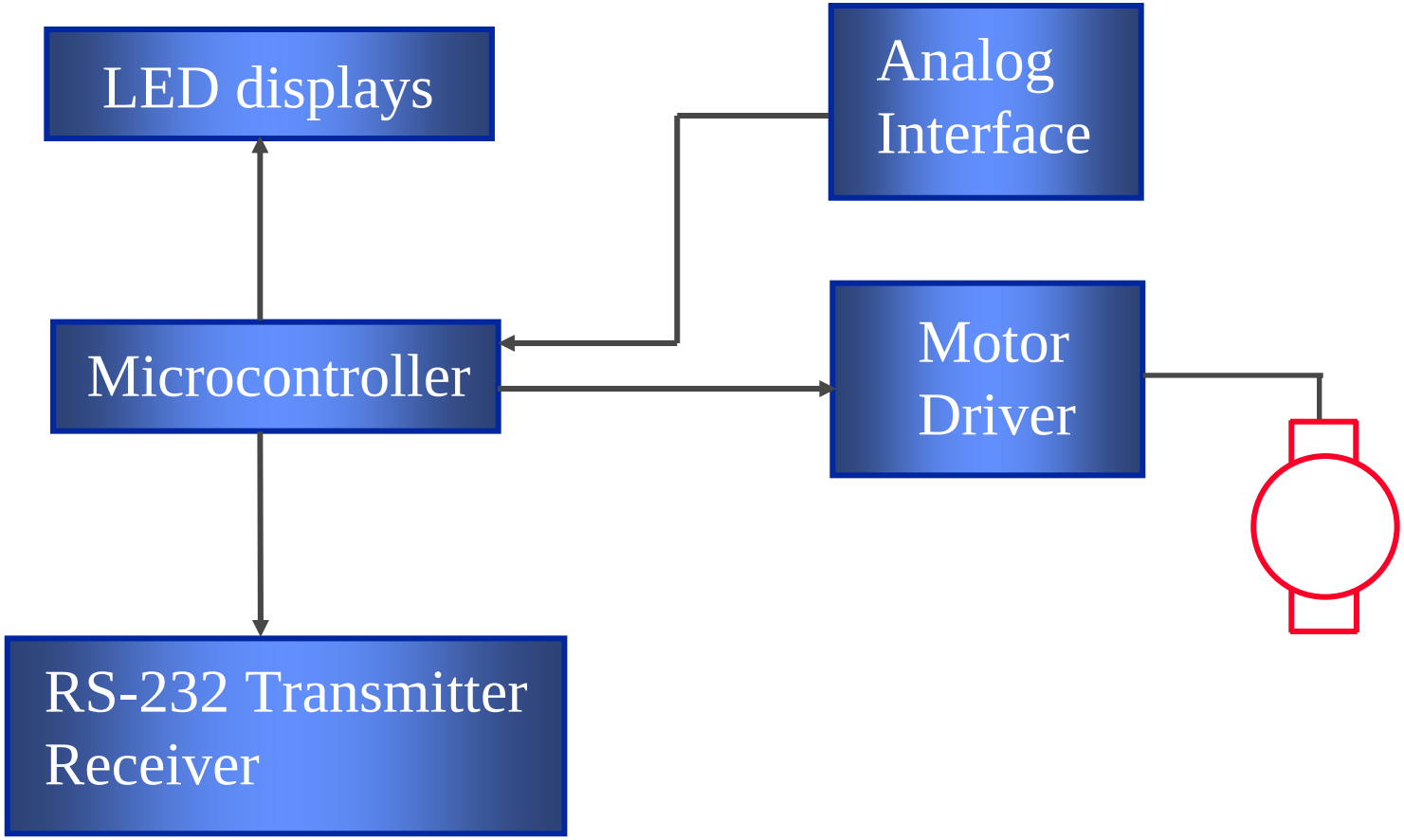


UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

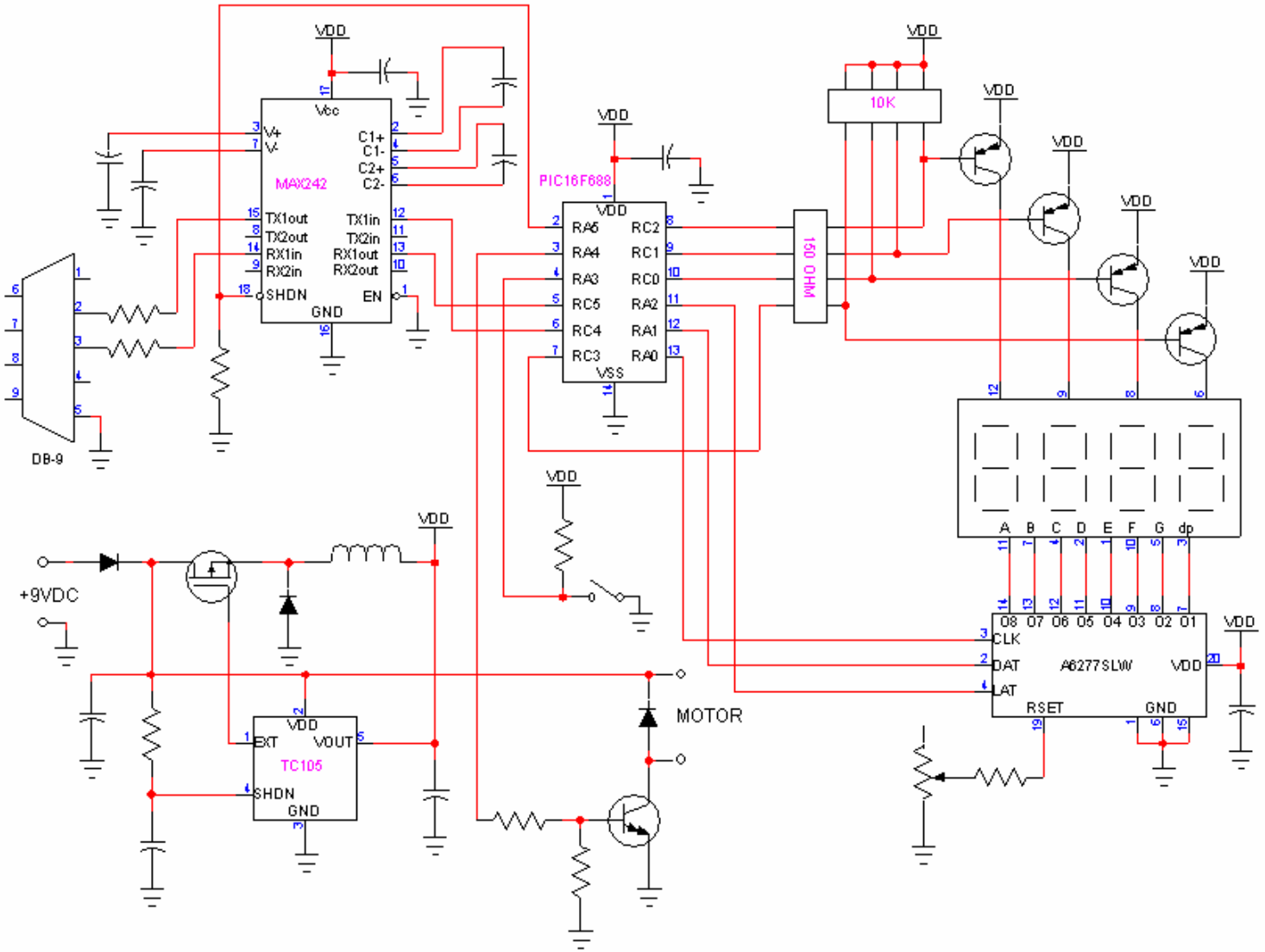
Digital Design Agenda

- **First Pass**
  - Digital Section
  - Typical design rules and Layout
  - Resulting performance
- **Second Pass**
  - Identify sources of noise
  - Identify noise pathways
  - Develop VDD and VSS distribution plan
  - New Layout and Resulting Performance

Digital Section Block Diagram



Digital Section Schematic



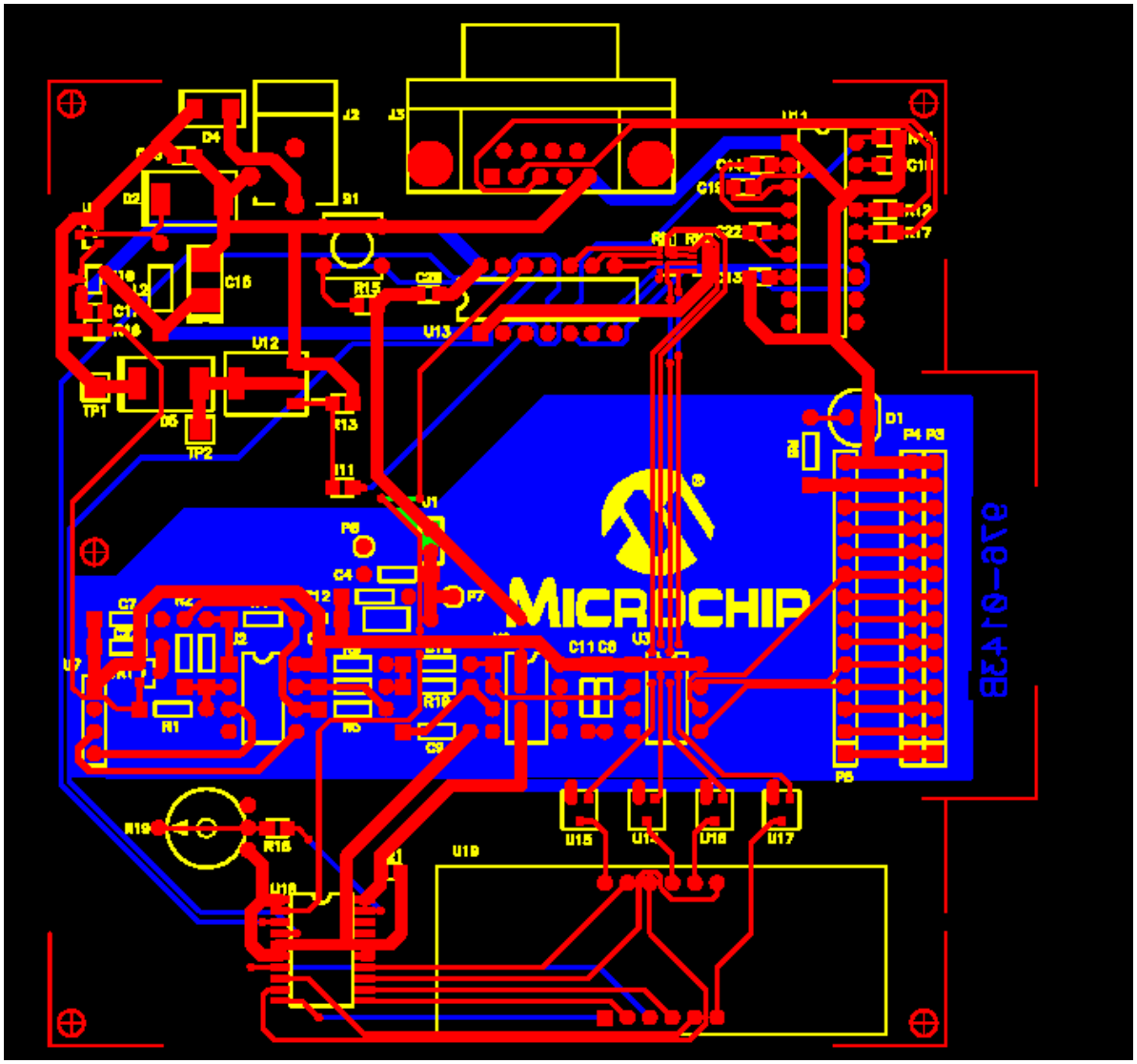
UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

Design Rules of Thumb

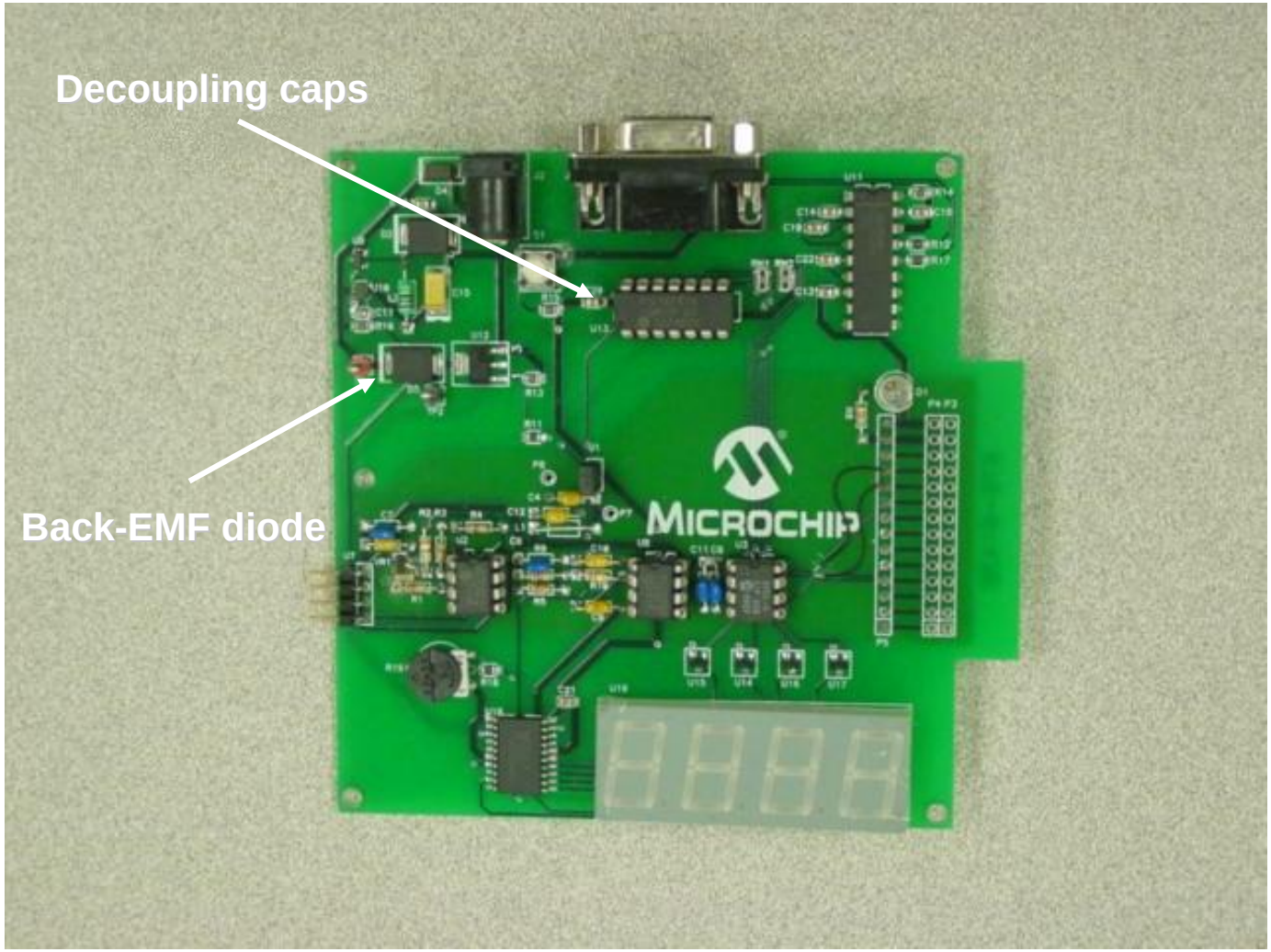
- **Digital Design Rules**
  - Use bypass capacitors for each IC
  - Use a back-EMF diode on the motor drive
  - DON'T Modify the analog circuit
- **Board Layout Rules**
  - Keep bypass capacitors near IC
  - Keep Power and Ground traces short
  - Avoid cuts in the Ground Plane
  - Make Power and Ground traces larger

UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

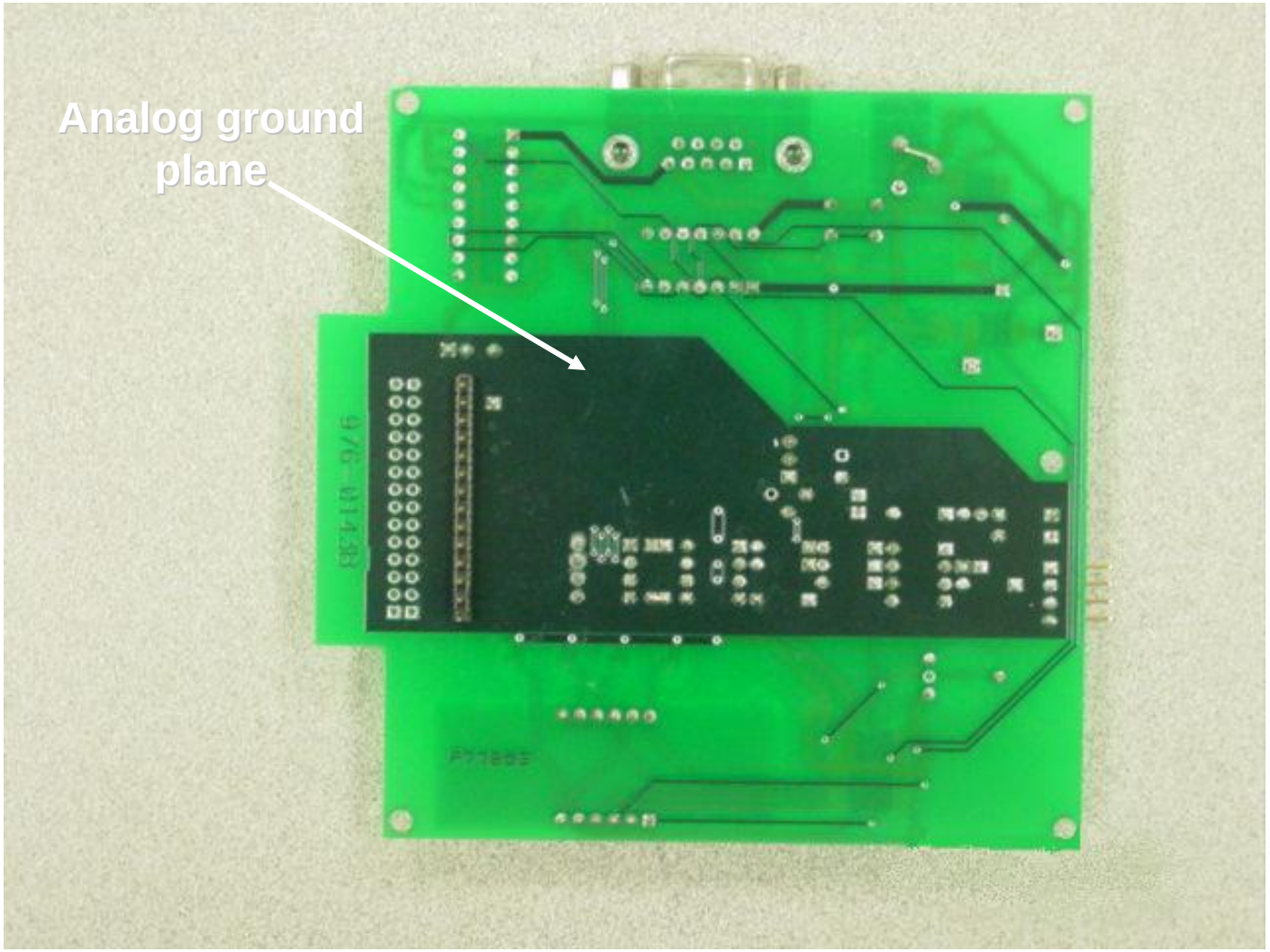
First Pass Combined Layout



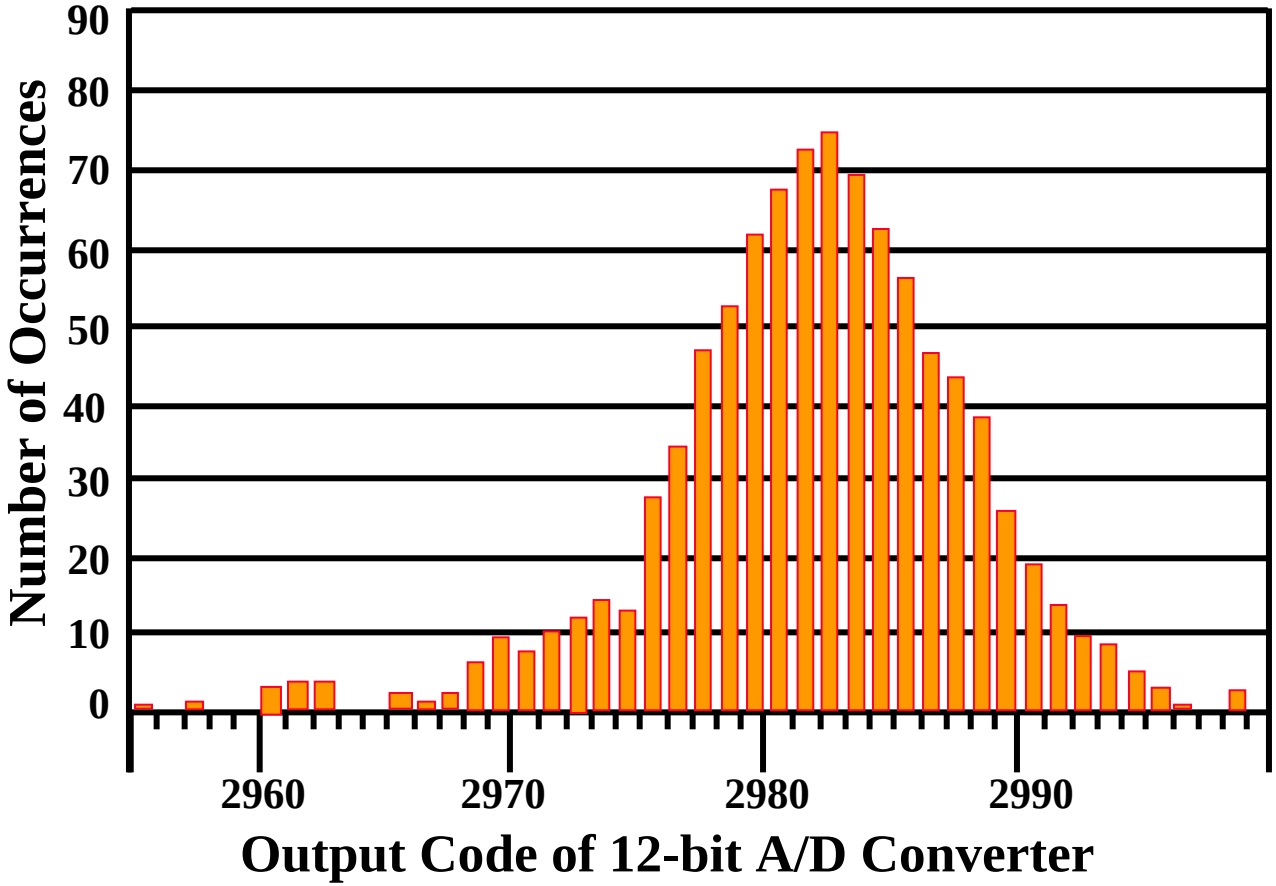
Application Board #4 (top side)



Application Board #4 (bottom side)



Combined Analog/Digital Test-Board Results



Code Width of Noise = 44

(total samples = 1024)

DENIAL!!

I didn't touch the analog section,

IT IS NOT MY FAULT!

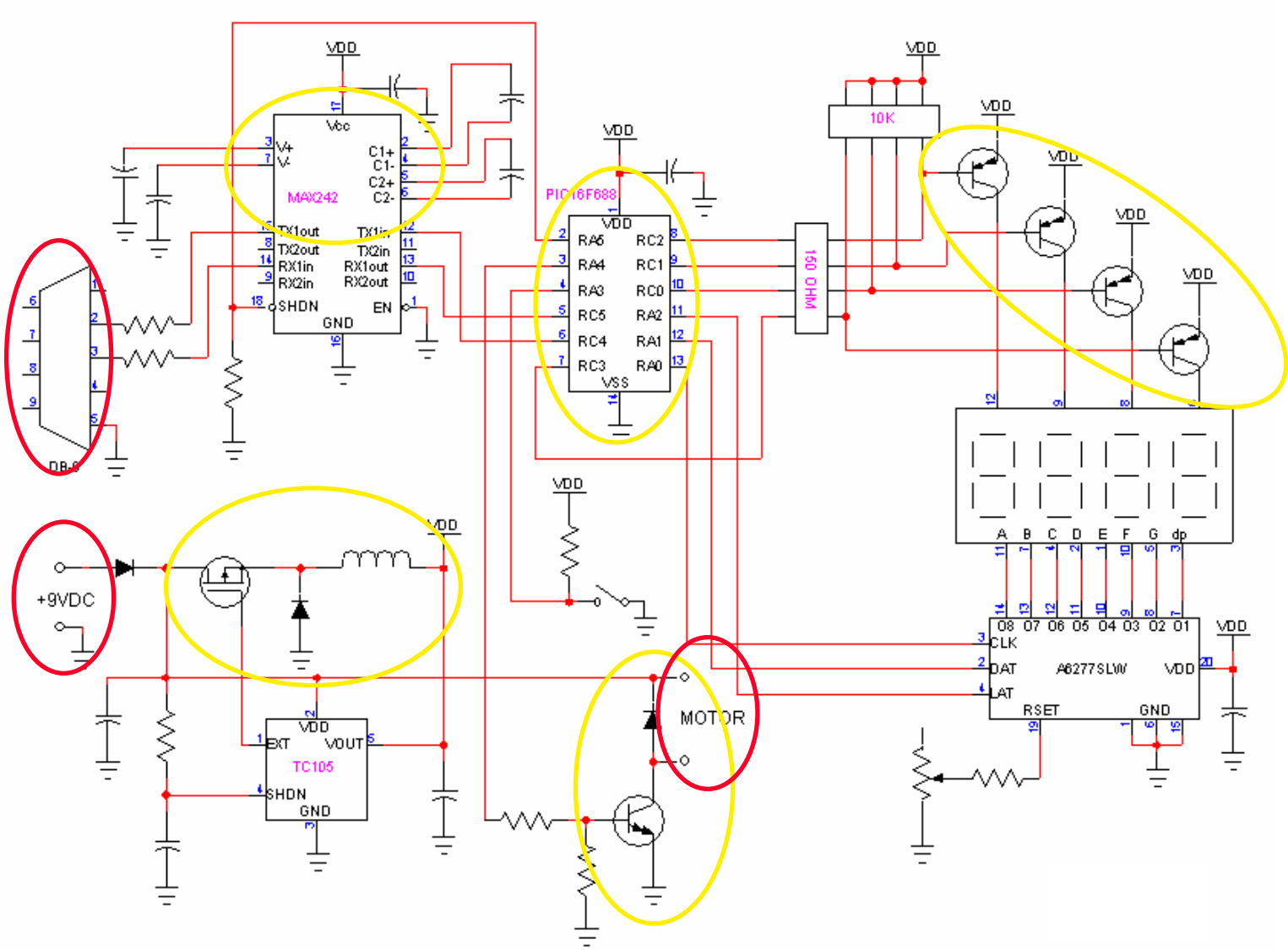
Second Pass

- **A More Holistic Approach to Power Ground and Noise**
  - Identify the noise sources
  - Identify the noise pathways
  - Develop a Power and Ground distribution plan that:
    - **Isolates the noise sources**
    - **Restricts the noise pathways**
    - **Considers the circuit as a whole**

Identify the Noise Sources

- **Internal noise sources**
  - Switching noise generated by fast rise time signals
  - Switching noise generated by high voltage/current switching
- **External noise sources**
  - Externally generated Electro-Magnetic Interference or EMI
  - May be radiated or conducted into the application

Identify the Noise Sources

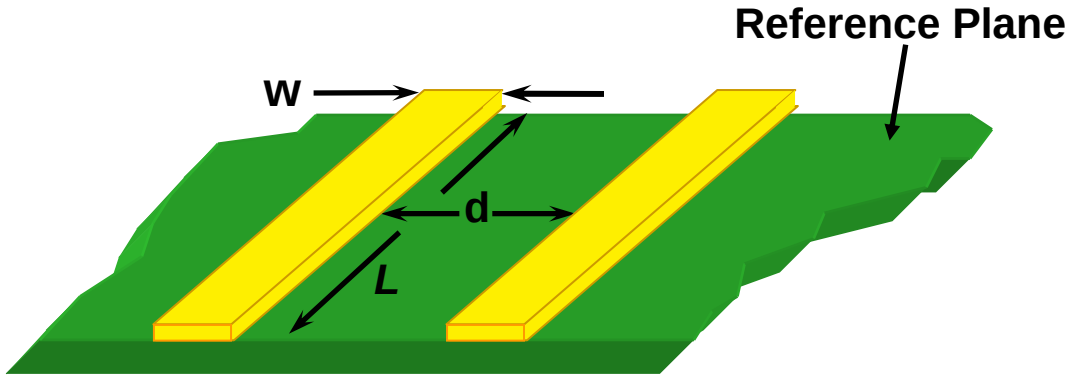


Identifying Noise Pathways

- **Pathways for Conducted noise**
  - Power and Ground currents interacting with the trace resistance and inductance
  - External wires can transport noise
- **Pathways for Radiated noise**
  - Capacitively coupled from fast rise time signals in close proximity
  - Magnetically coupled from high current signals in close proximity, or through a ferrous material
  - Traces acting as Antennas for incoming RFI

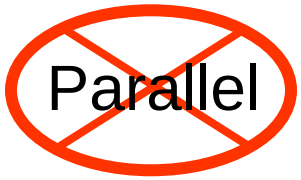
The Physics of the Problem

PCB Crosstalk



- **Reduce crosstalk noise by**
  - ↑ d (distance)
  - ↓ L (parallel length)
  - ↓ t_r (rise, fall times)
  - ↓ Characteristic impedance

- **Reduce noise by**



- **Keep R_{IN} & R_{OUT} Small**

PCB Inductance

- **Significant source of ground noise**

$$V_{noise} = L \frac{di}{dt} \text{ volts}$$

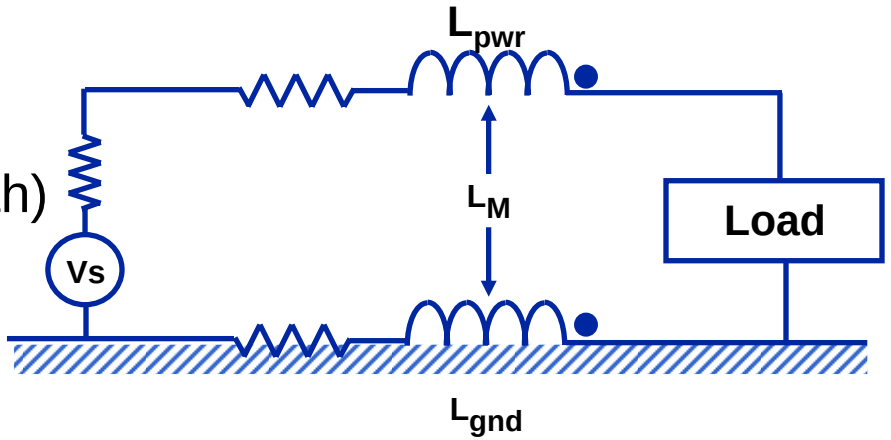
- **For a trace above a ground plane**

$$L = 0.005 \ln(2\pi H/W) \text{ uH/in}$$

- **For a current loop (e.g. power & ground return)**

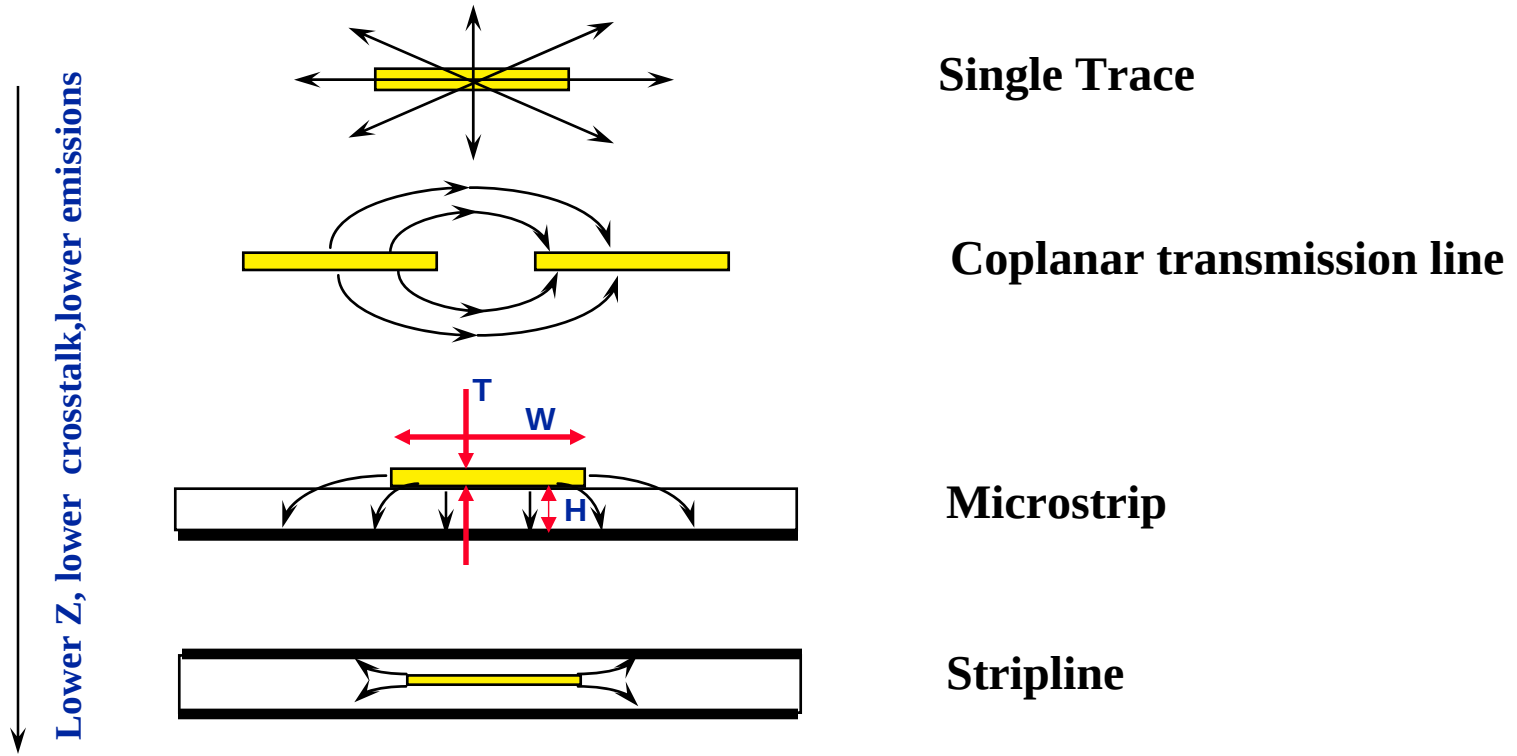
$$L_t = L_{pwr} + L_{gnd} - 2M$$ **(M=mutual inductance)**

- **Reduce Noise by**
  - ↓ H (height above return path)
  - ↑ W (width of trace)



PCB Trace Impedance

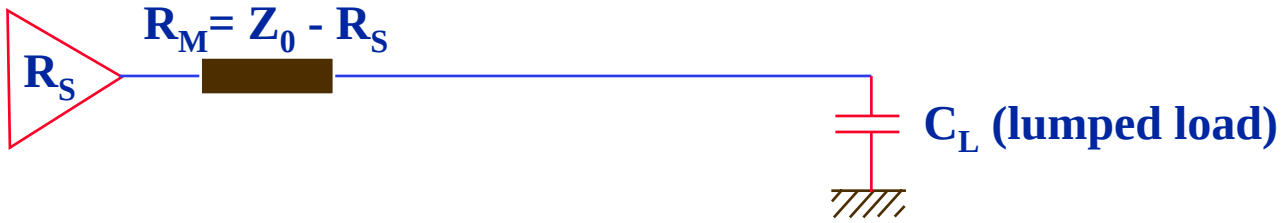
- Avoid creating traces without a clearly defined return path (especially for clock signals)
- Lower Z_0 = Less crosstalk, lower RF emissions



Reflections & Ringing

- **Traces may be unterminated if**
  - L(cm) < 9 * t_r (ns)

  [Estimate based on microstrip topology and 0.36ns/cm (FR-4)]
- **Terminated lines: series R is typically the most appropriate (but will introduce delay, T_{pd})**

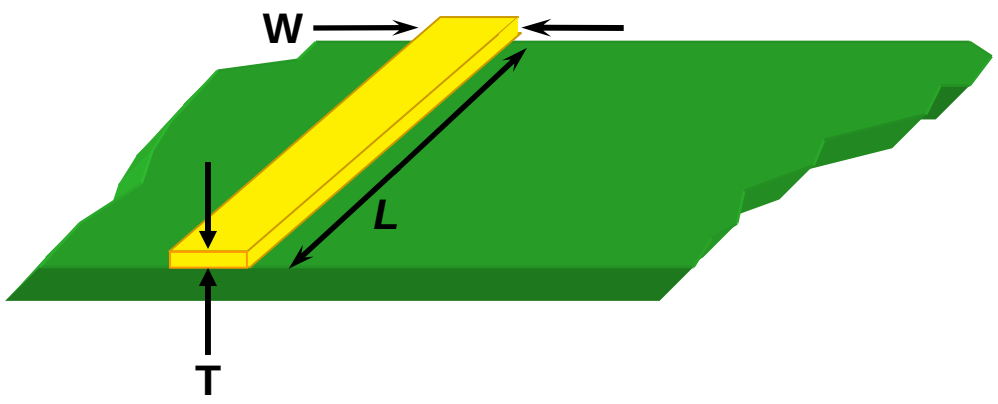


- **Z_0 varies with T, W and H. T_{pd} varies with ε_r**
  - For W >> H, $Z_0 = \frac{377}{\sqrt{\varepsilon_r}} * \frac{H}{W}$ ohms
  - Tpd = $33.37\sqrt{0.475\ \varepsilon_r + 0.67}$ ps/cm
  - See references for more precise Z_0 and T_{pd} calculation

PCB Trace Resistance

$$R = \frac{L \bullet \rho}{W \bullet T} \quad \text{ohms}$$

where ρ = resistivity



$V_{drop} = I\,R$ amps

- **Reduce Noise by**
  - ↑ W (width of trace)
  - ↓ L (length of trace)
  - ↑ T (thickness of trace)

The Usual Suspects

Ground Impedance Effects

- **Common-impedance coupling**
  - Can introduce digital noise into sensitive analog or interface subsystems
  - Can cause RF noise to couple onto external ports
- **Ground loops**
  - Source of RF emissions if the circulating current has a significant HF component
  - Can create havoc with partitioned interface circuitry
  - Can introduce line AC noise into low-level analog circuitry
- **Resonance**
  - Ground bounce can impact signal integrity of bus structures
  - Multi-point ground resonance can induce sufficient ground movement as to cause systems to fail, especially during susceptibility testing

Conducted Noise Pathway: Ground

- **Pathway: Ground, carries return currents and provides a reference voltage,**
  - Fast rise time currents react with trace inductance to generate noise voltages
  - High currents react with trace resistance to generate noise voltages

Conducted Noise Corrective Action: Ground

- **Minimize AC and DC impedances.**
  - Make all grounds as short and wide as possible
  - Ground planes are better than traces
- **Isolate noisy Ground returns**
  - No fast currents through sensitive grounds or ground planes
  - No high current in sensitive grounds or ground planes

Conducted Noise Pathway: Power

- **Pathway: Power, the source of operating current**
  - Fast rise time currents react with trace inductance to generate noise
  - High currents react with trace resistance to generate noise

Conducted Noise Corrective Action: Power I

- **Minimize Impedance**
  - Make Power traces as wide as possible
  - Keep leads to bypass capacitors short to limit inductive responses to switching (self resonance effects)
  - Use low ESR bypass capacitors to limit resistive responses to switching

Conducted Noise Corrective Action: Power II

- **Isolate noise sources using low pass filtering**
  - Isolate noisy circuits on their own power traces to create higher series impedances
  - Properly selected bypass capacitors to present a low shunt impedance
  - Together, trace inductance and bypass capacitors create a LP filter
  - Ferrite beads, inductors, and resistors can augment the lead inductance to lower the corner frequency of the low pass filter

Radiated Noise

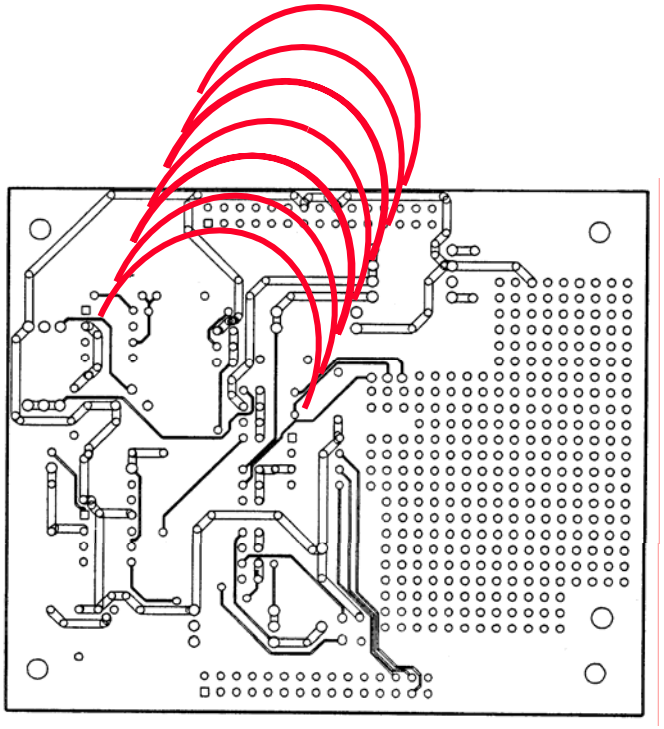
- **Pathway: Adjacent Traces**
  - Adjacent traces can create unintended capacitors which can couple fast signals
  - Adjacent traces can create unintended transformers which can couple high current signals
- **Corrective Action: Adjacent Traces**
  - Both are minimized by increased distance
  - Both are minimized by decreased common area
  - Low impedance signals are less susceptible

Radiated Noise

- **Loops: Magnetic fields can couple locally and/or radiate**
  $E \alpha A I_L f^2$ /distance **(far field E/H=377ohms)**
  E increases at 40dB/decade

- **Traces and wires can act as Antennae for noise**
  $E \alpha L I_{cm} f$ /distance
  E increases at 20dB/decade

- **High frequency signals will radiate more if not terminated**
- **The Q Multiplier effect can generate high voltages in resonant circuits**

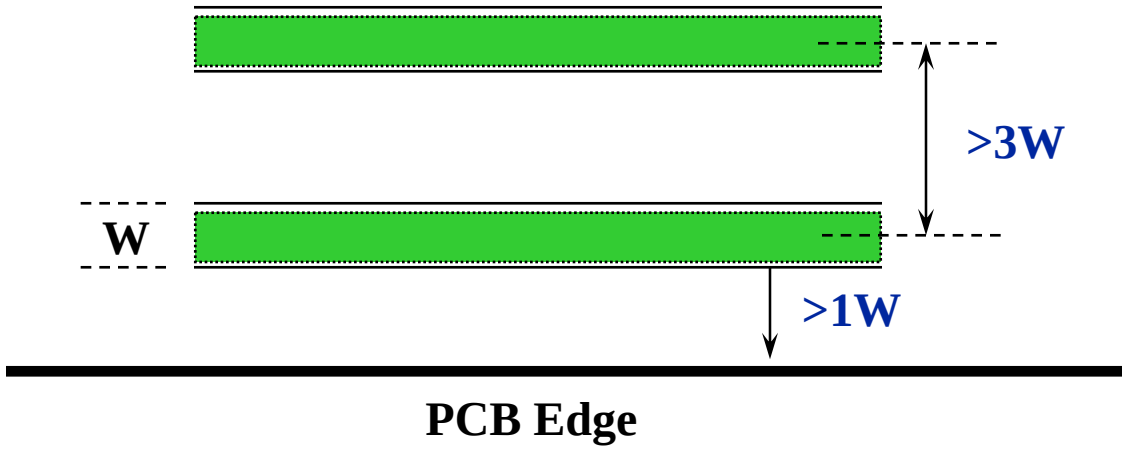


Radiated Noise Corrective Action

- **Keep sensitive signal traces short**
  - Shield sensitive/noisy wires or long traces
- **Terminate signals resistively**
- **Minimize current loop areas**
  - Decouple as locally as possible
  - Minimize clock & oscillator return paths
  - Use ground planes as current return image plane
- **Use an RC or LC low pass filter on all signals entering the cabinet**
  - Filter to cabinet ground
    - Exterior for inputs, interior for outputs
- **Use low impedance drivers to transmit signals over long distances**
- **Match load impedance to source impedance**

The 3-W Rule

- Represents 70% flux boundary
- Removes the need for a guard trace in most cases
- Mandatory only for high threat signals (clocks, analog, reset, differential pairs)



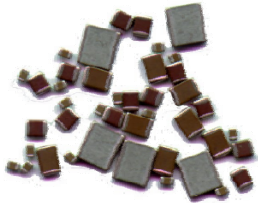
Creating a Power and Ground Distribution Plan

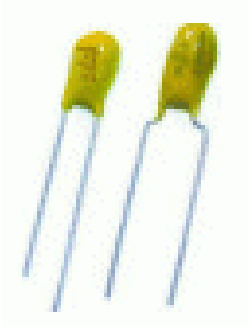
UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

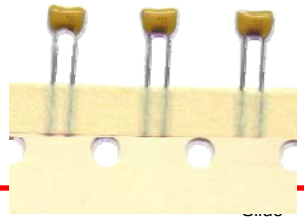
Start with the Right Bypass Capacitor for Digital Sections

- Determine noise frequency
  $f_{noise} = 1 / (\pi * t_{rise})$ or $t_{rise} = 1 / (\pi * f_{noise})$
  [substitute t_{fall} if faster]
- Determine max ripple voltage V_{RIPPLE}
- Approximate surge current
  $I_{SURGE} = I_{AVE} * f_{noise} / f_{clk}$
- Calculate bypass capacitor value

$$C_{BYPASS} = \delta i * \delta t / \delta v$$
$$= I_{SURGE} * t_{rise} / V_{RIPPLE}$$
$$= \{(I_{AVE} * f_{noise} / f_{clk}) * (1 / (\pi * f_{noise})\} / V_{RIPPLE}$$
$$= I_{AVE} / (\pi * f_{clk} * V_{RIPPLE})$$



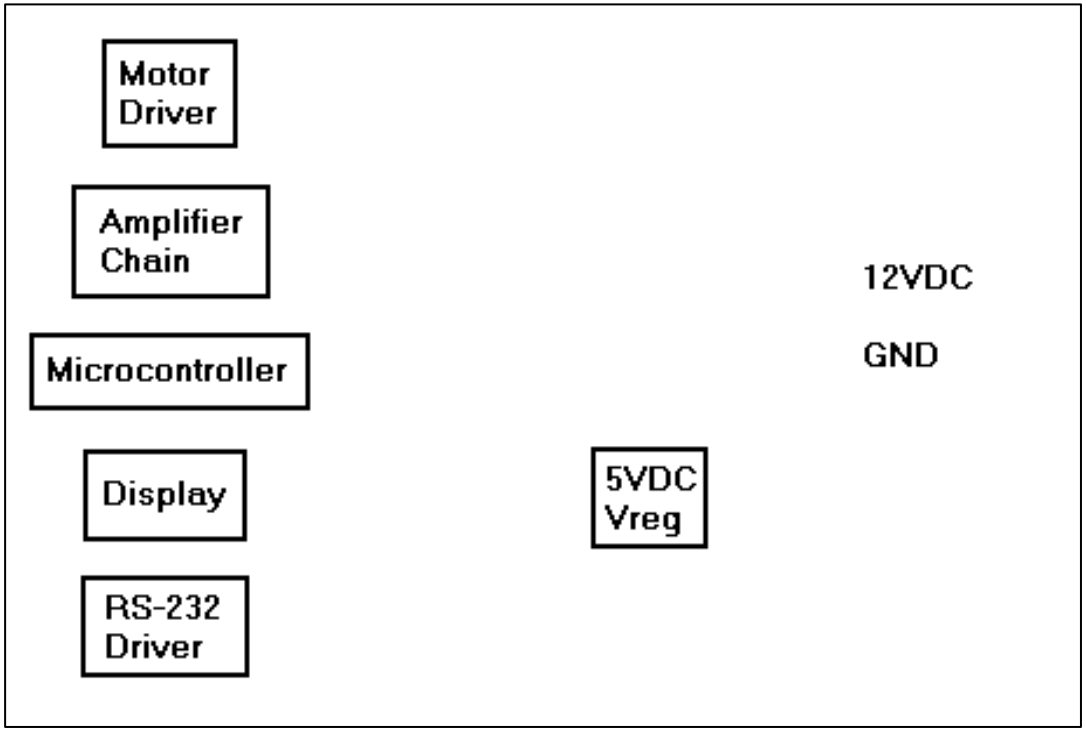




Creating a Power and Ground Distribution Strategy I

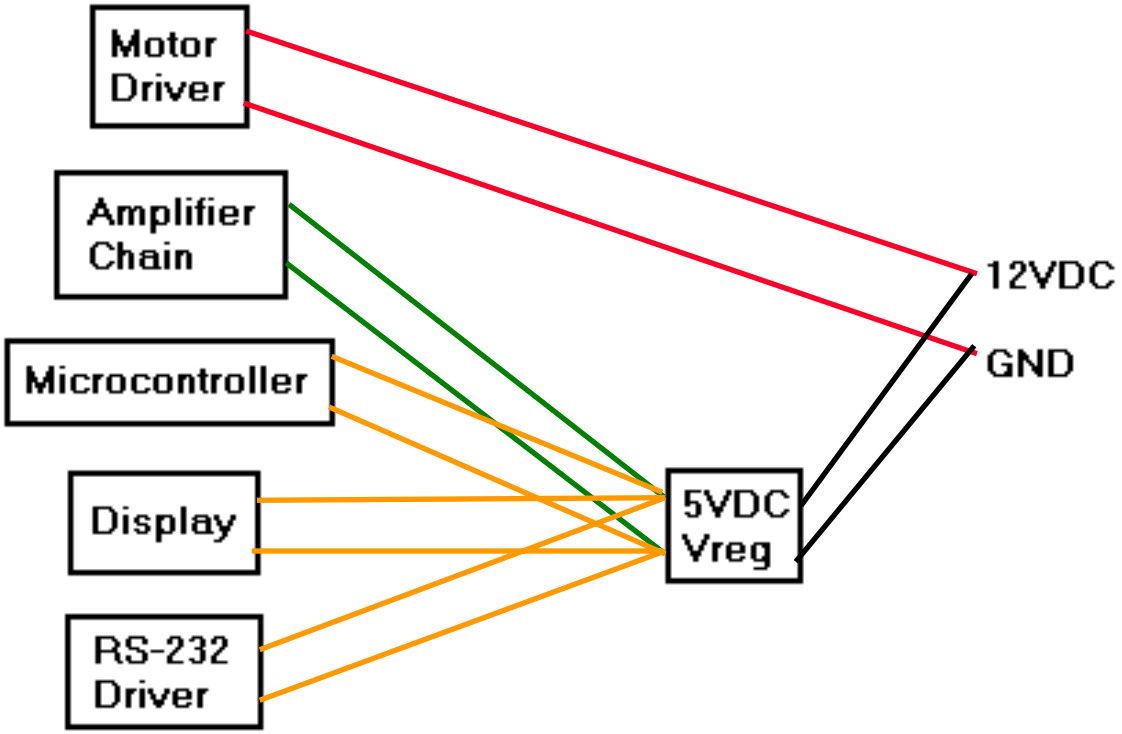
- **Separate, classify and draw the various sections of the design, include the Supplies**

- **Digital section**
  - Clock is <5MHz & $t_{r/f}$ > 5ns so single point ground OK
  - Would require its own digital ground plane if >5MHz, <5ns



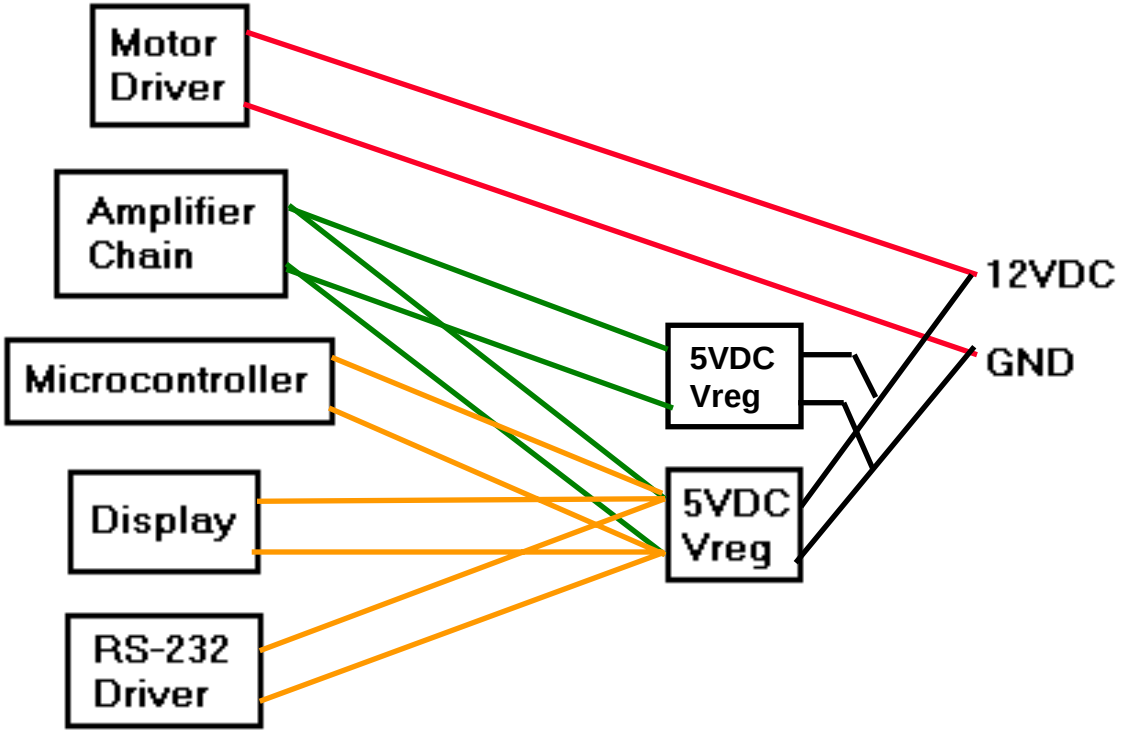
Mapping out the plan

- **Draw the sections of the design, and add the connections**



Revising the plan

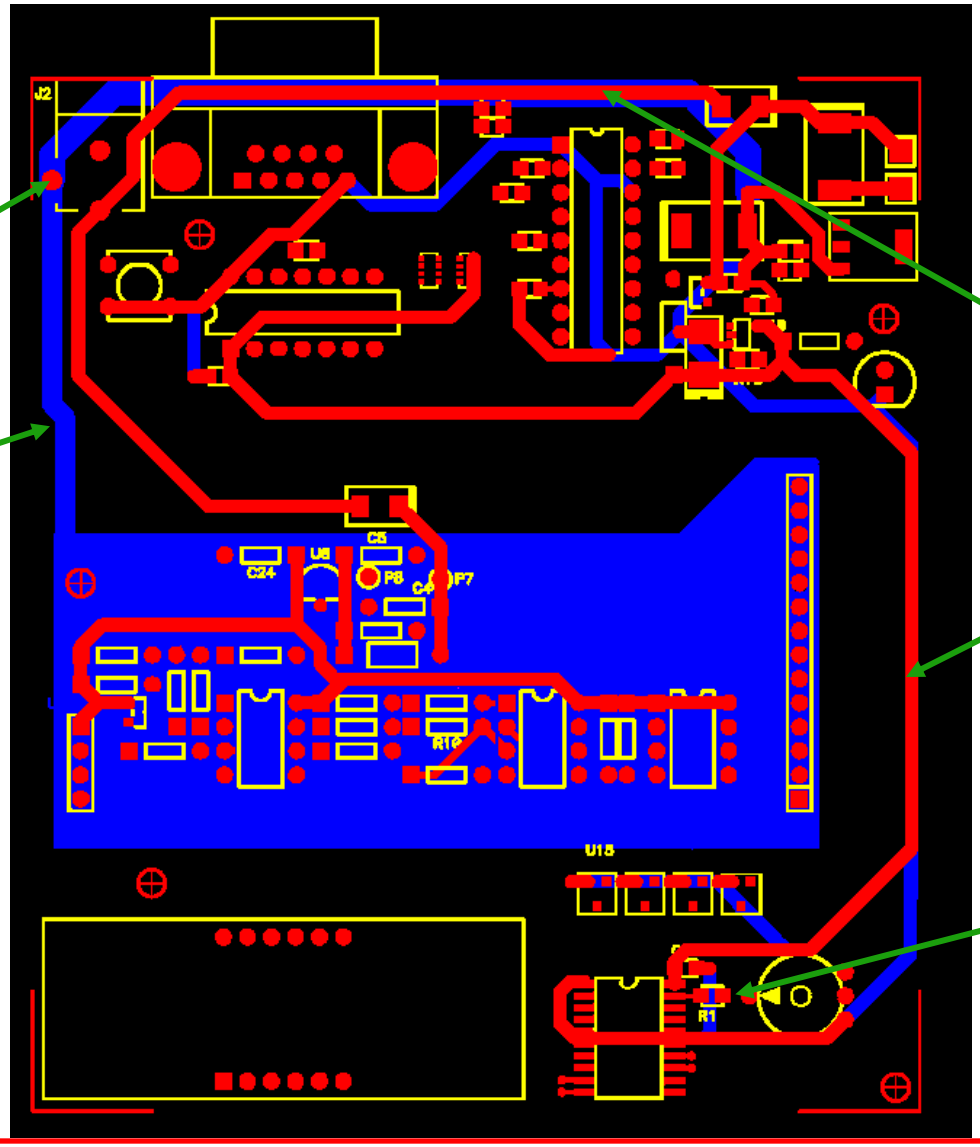
- **Use routing to maximize isolation between noisy and sensitive blocks, while keeping runs short**



Re-layout the Board

- **Layout the board using the plan**
  - Think about isolation when placing each section
  - Think about how to route power and ground for each section
  - Remember to isolate sensitive signals from fast and high current signals
  - Remember which traces have to be wide
  - Remember which traces have to be short and wide

Placement, Power and Ground



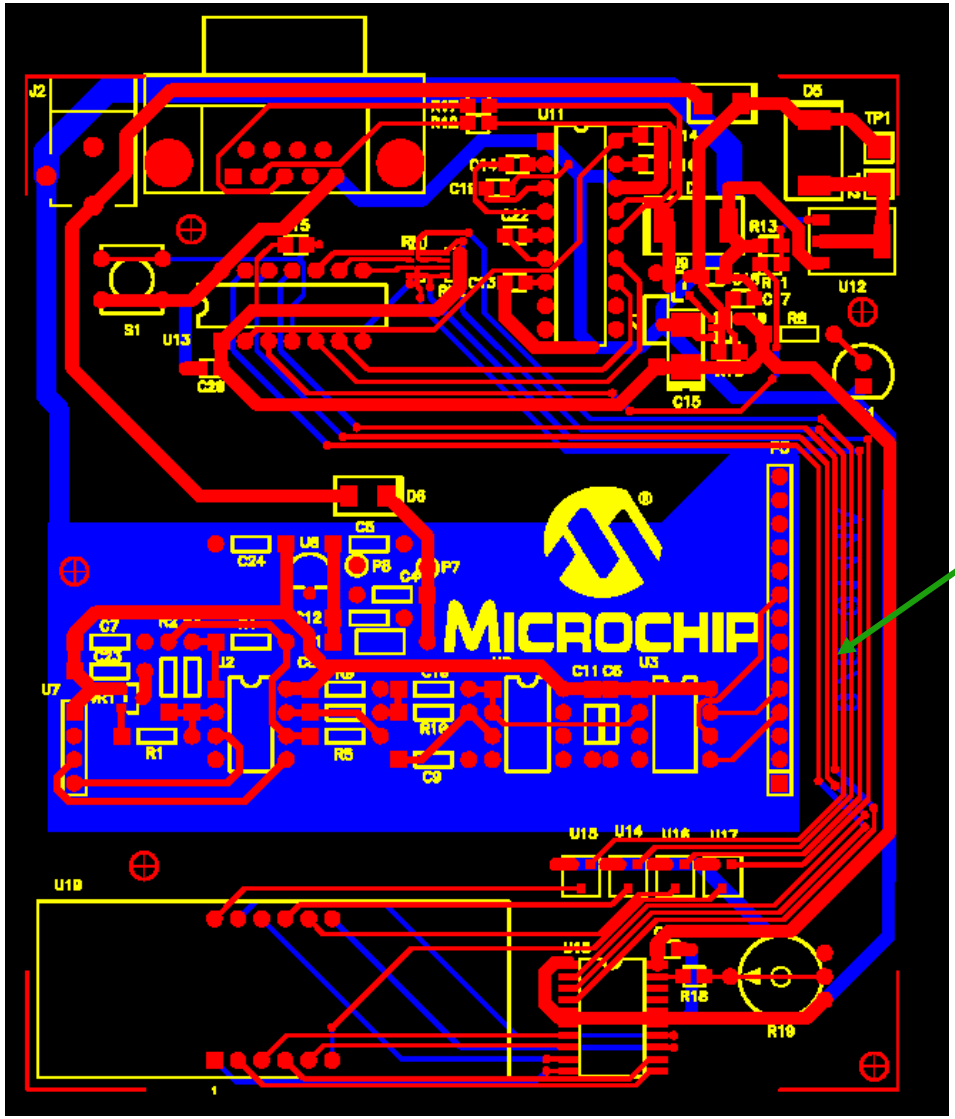
Single point ground connection

Wide traces

Low-Z Power Routing

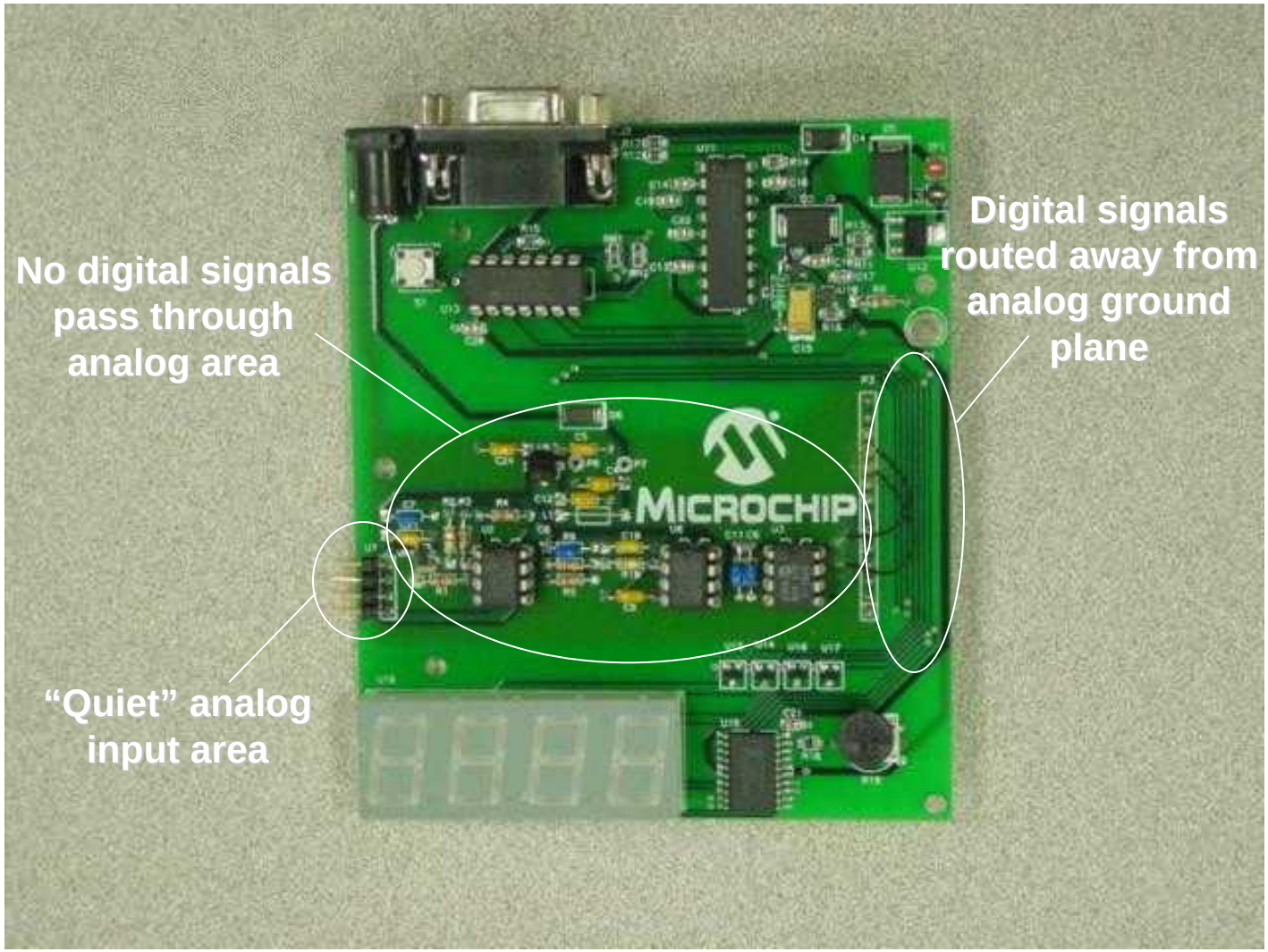
Small decoupling cap loops

Complete Board Layout

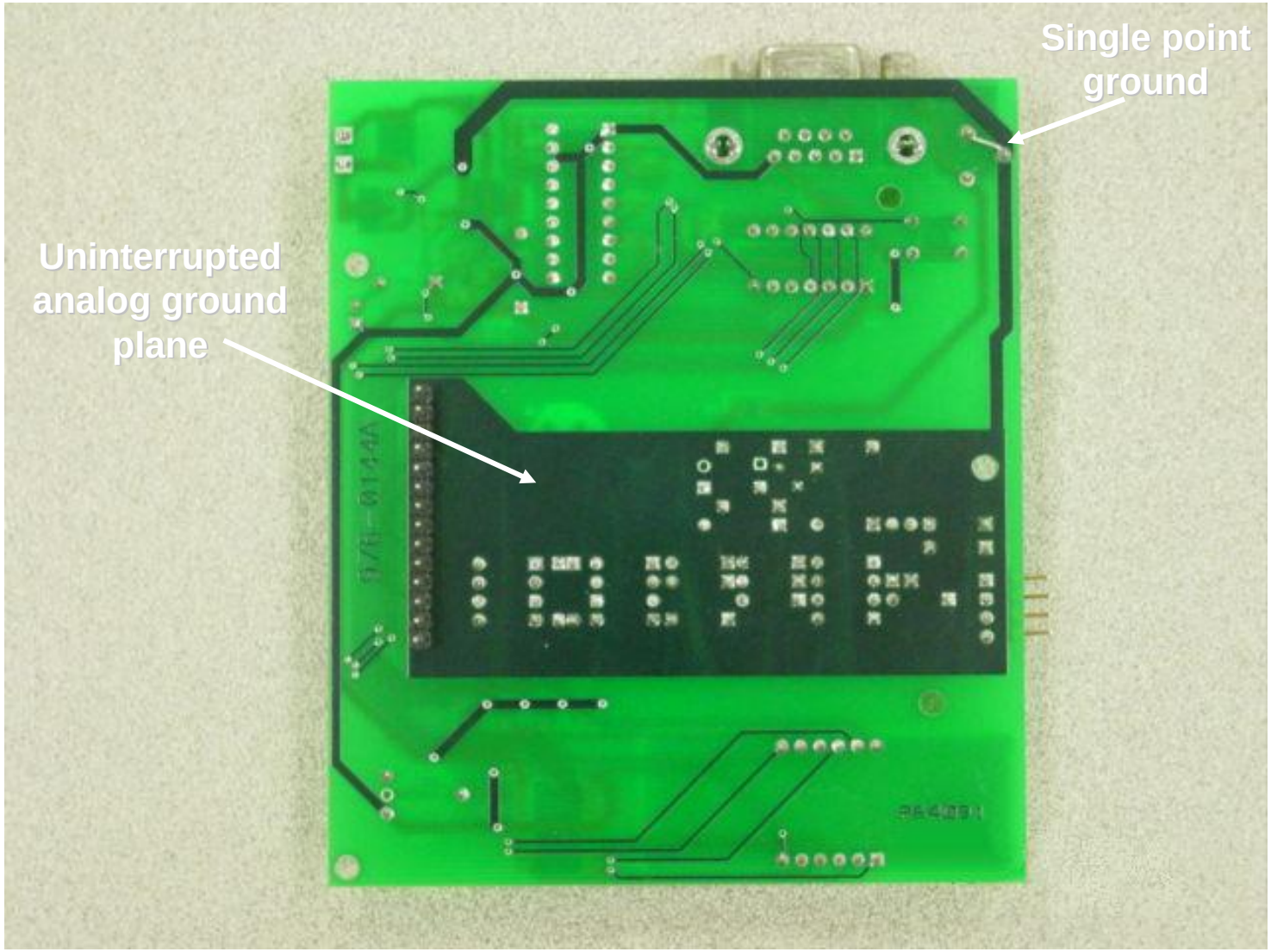


Re-route digital signals around analog area

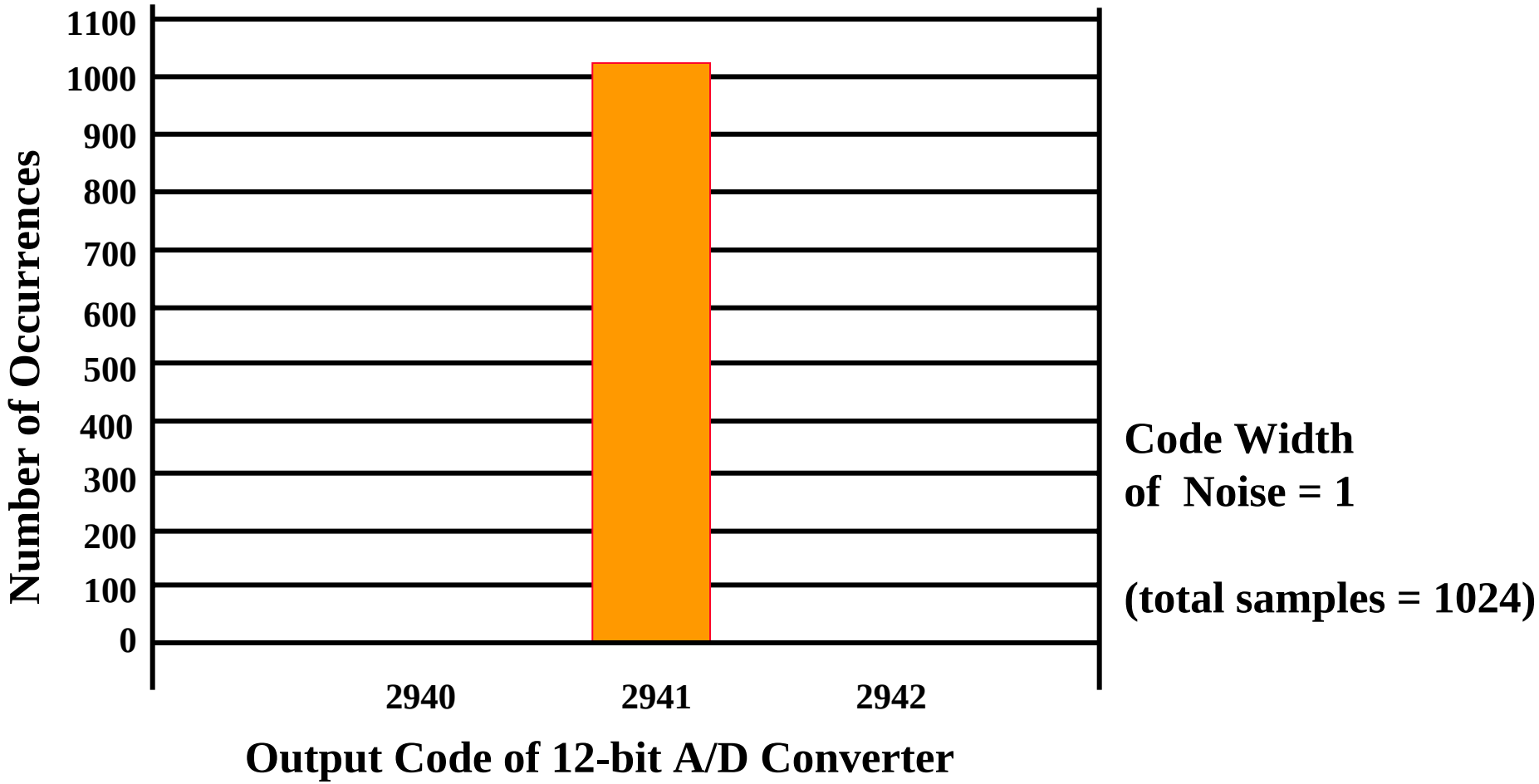
Application Board #5 (top side)



Application Board #5 (bottom side)



New Composite Board Test Results



Summary

- **Use low-noise analog components**
- **Use an uninterrupted ground plane**
  - Separate digital & analog planes using a ‘moat’
- **Filter the ADC with an analog low-pass filter**
- **By-pass all devices properly**
- **Filter your power supply properly**
- **Develop a power and ground plan for the whole circuit**
- **Isolate noisy sections**
- **Minimize noise pathways**

Additional Noise Reduction Techniques

- **Using software to create quiet times for conversions**
- **Move switching power supply inputs to unregulated supplies**
- **Use separate analog and digital voltage regulators**
- **Use two or more bypass capacitors in parallel to extend their frequency range**
  - But be aware of double resonance effects

UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

References

- **Reference Books**
  - High-speed Digital Design: A Handbook of Black Magic, Howard Johnson and Martin Graham, Prentice Hall, 1993.
  - Noise Reduction Techniques in Electronic Systems, (2nd Ed.), Henry Ott, John Wiley, N.Y., 1998.
  - EMC at the Component and PCB Level, Martin O'Hara, Newnes, 1998
  - EMC and the Printed Circuit Board, Mark Montrose, IEEE Press, 1998
  - The RF Capacitor Handbook, from American Technical Ceramics Inc.
  - The Circuit Designer's Companion , by Tim Williams
  - Reference Data for Engineers, 7th edition Edward C. Jordan, Editor in chief
  - ABC's of Transformers & Coils,by Edward J. Bukstein

UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

Additional References

- **Reference Application Notes**
  - *ADN007, Techniques that Reduce System Noise in ADC Circuits*
  - *AN681, Reading and Using Fast Fourier Transforms (FFTs)*
  - *AN699, Anti-Aliasing, Analog Filters for Data Acquisition Systems*
  - *AN695, Interfacing Pressure Sensors to Microchip's Analog Peripherals*
  - *AN688, Layout Tips for 12-Bit A/D Converter Application*
  - *AN823, Analog Design in a digital World using Mixed Signal Controllers*
- **At www.microchip.com under ….**
  - Analog & Interface Products
    - **FilterLab® Active Filter Design Software**
  - EMC Design
    - **EMC 'Webinars'**
    - **EMC Newletter**

UNIVERSITY OF MICROCHIP UOFM MASTERS 2007

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KeeLoq, KeeLoq logo, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, rfPIC and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AmpLab, FilterLab, Linear Active Thermistor, Migratable Memory, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Smart Serial, SmartTel, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.