



# 928 PGN

## Managing Power, Ground, and Noise



# Class Agenda

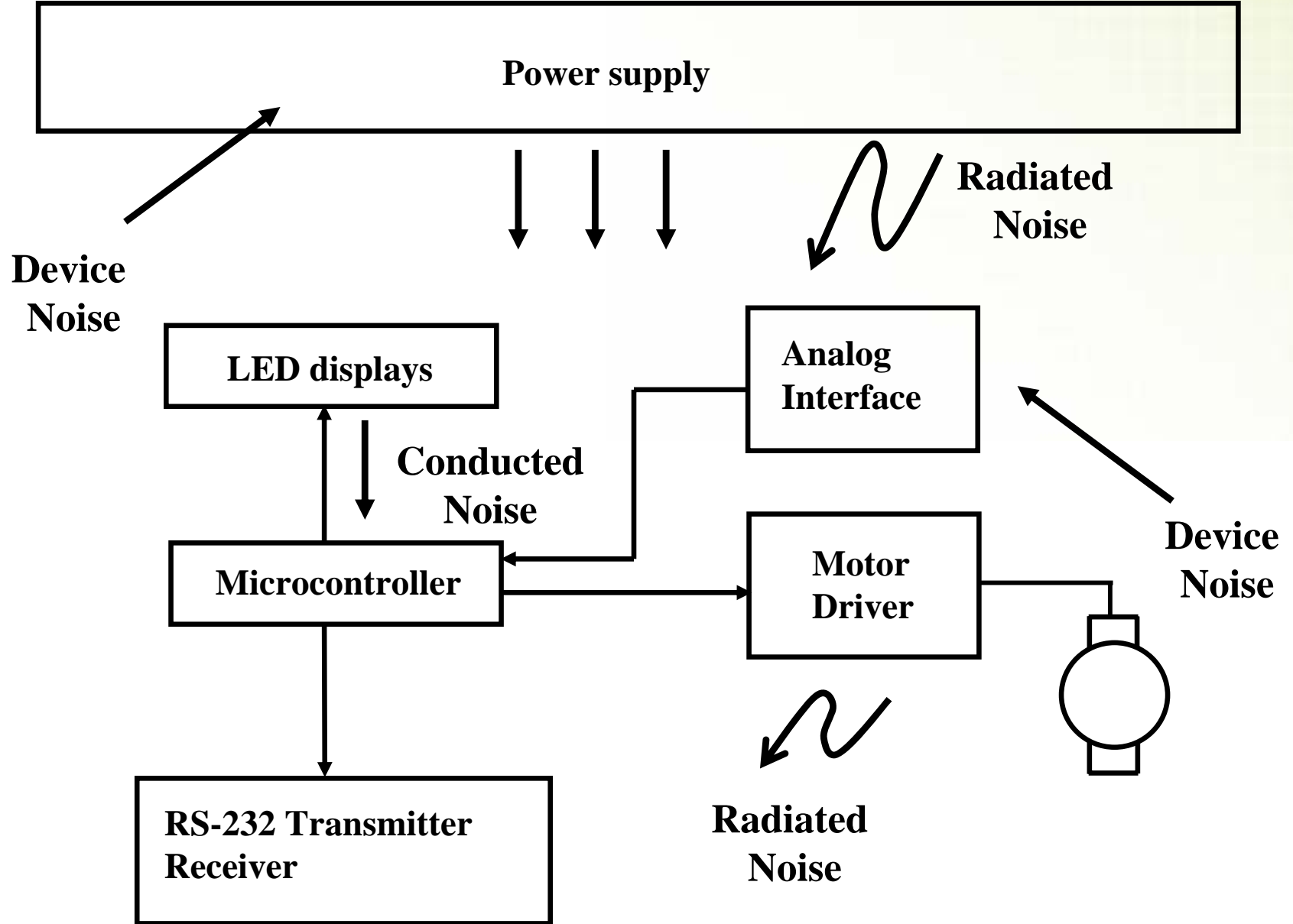
- Project Definition
- Analog Design
- Digital Design
- Pulling it all together



# Definition of Project

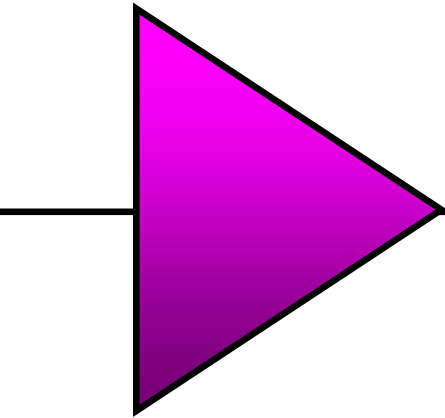
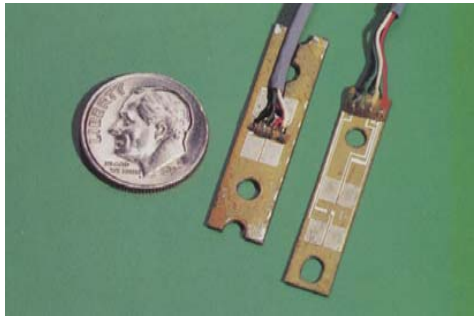
- Has Analog and Digital Content
- Functions:
  - Measures Weight with Specified Load Cell
  - Displays results with LEDs
  - Communication to Computer through RS-232 Interface
  - PWM fan Motor Driver on board

# Analog/Digital System



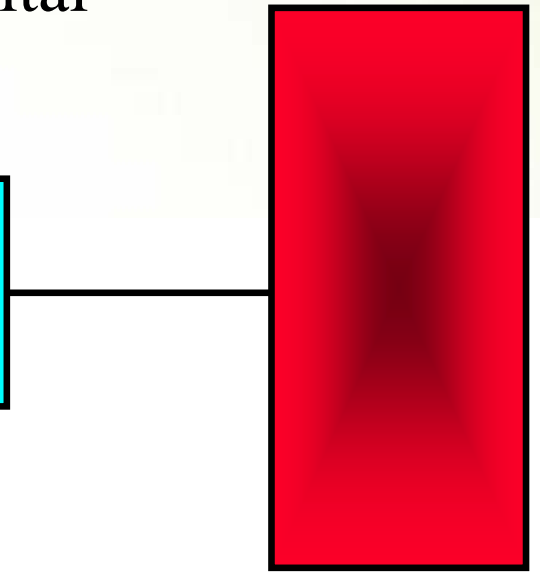
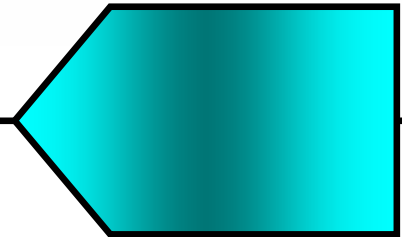
# Analog Section Weigh Scale Circuit

Load  
Cell



Instrumentation  
Amplifier

Analog-to-Digital  
Converter

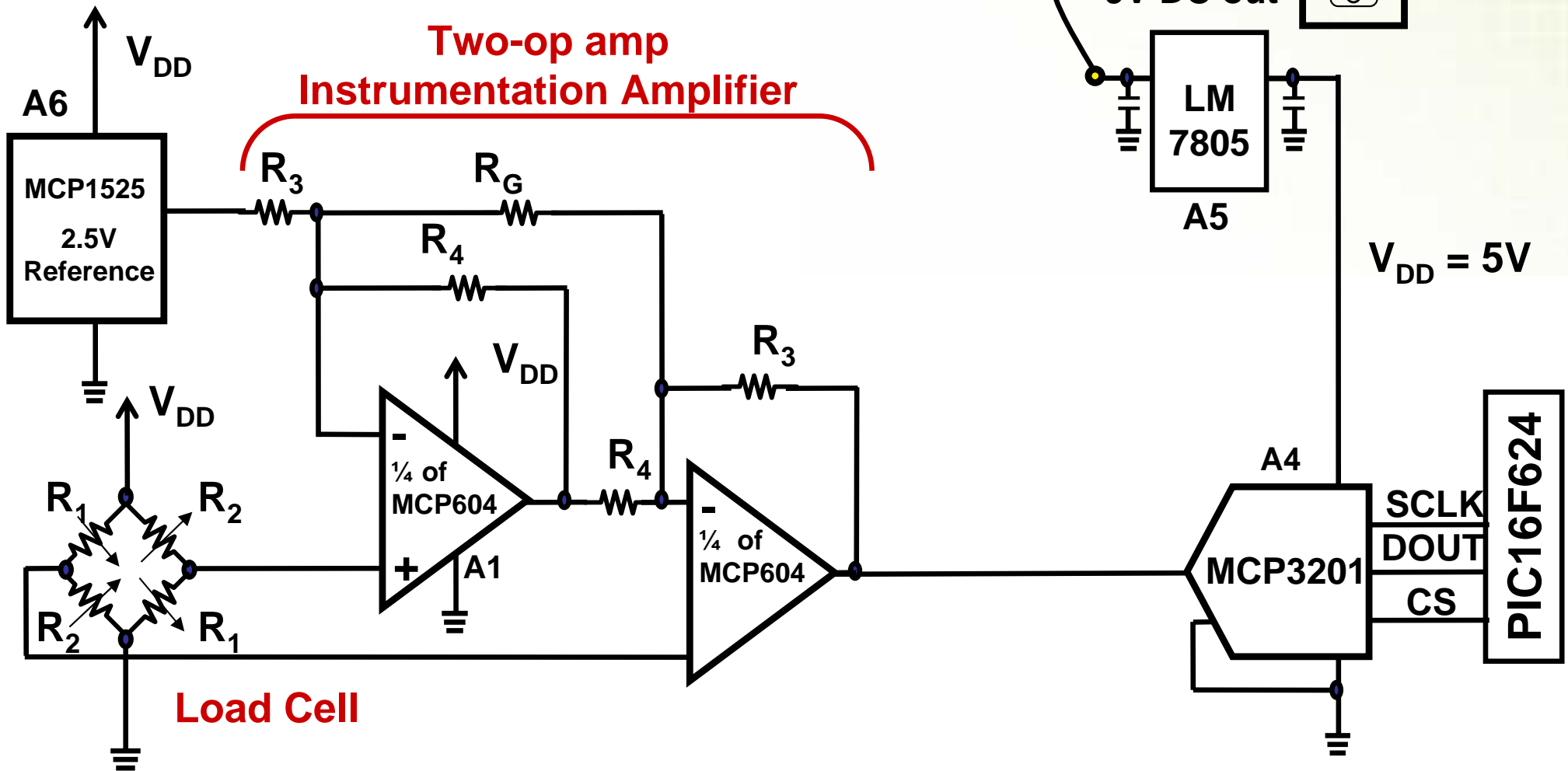


Microcontroller

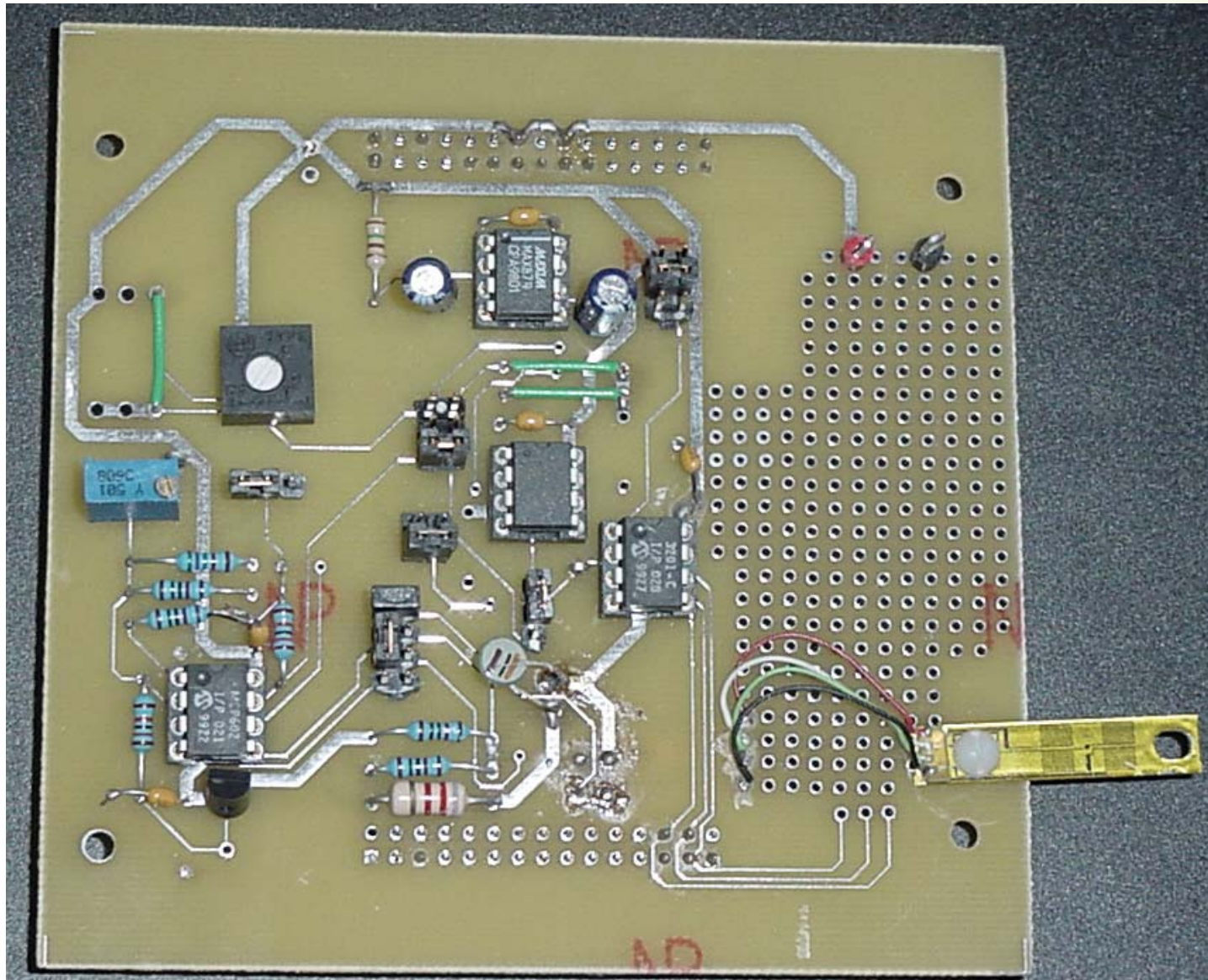
# Schematic of Analog Section

## 12-bit Accurate Circuit Components

- $R_3 = 300 \text{ k}\Omega$ ,  $R_4 = 100 \text{ k}\Omega$ ,  $R_G = 4020 \text{ }\Omega$ , (+/-1%)
- MCP604 = Single Supply, CMOS, quad op amp
- MCP3201 = 12-bit, A/D SAR Converter

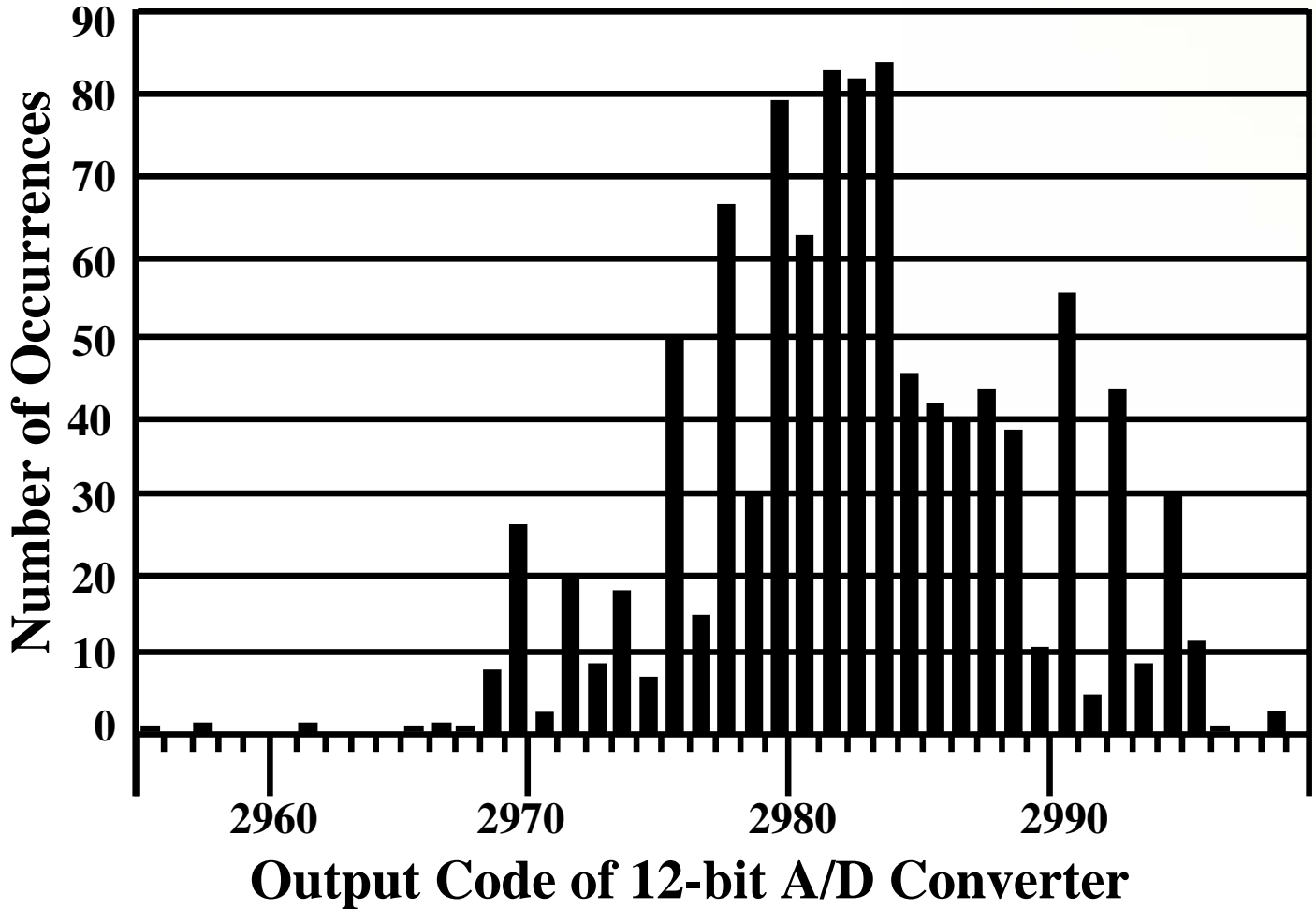


# Analog Layout #1





# Analog Board : First Pass Test Results



**Code Width  
of Noise = 44**  
  
**(total samples = 1024)**

**How many bits?**  
  
**6.54-bits**





# Low-Noise Design

- Device Noise – Created by the devices
  - Resistors – Reduce Values where possible
  - Op amps – Use Lower-Noise Amplifiers
  - Power Supply – Replace or Filter Switching Devices
- Emitted Noise – Externally Injected
  - Layout – Keep analog and digital Separate
  - Environment – Shield or change orientation

# Device Noise

## ● Resistors

- Johnson or Thermal Noise

- $V_{RN} = \sqrt{4KTR(BW)}$  {Vrms}

K = Boltzman's Constant =  $1.38e^{-23}$  JK<sup>-1</sup>

T = Temperature in Kelvin

R = Resistance in Ohms

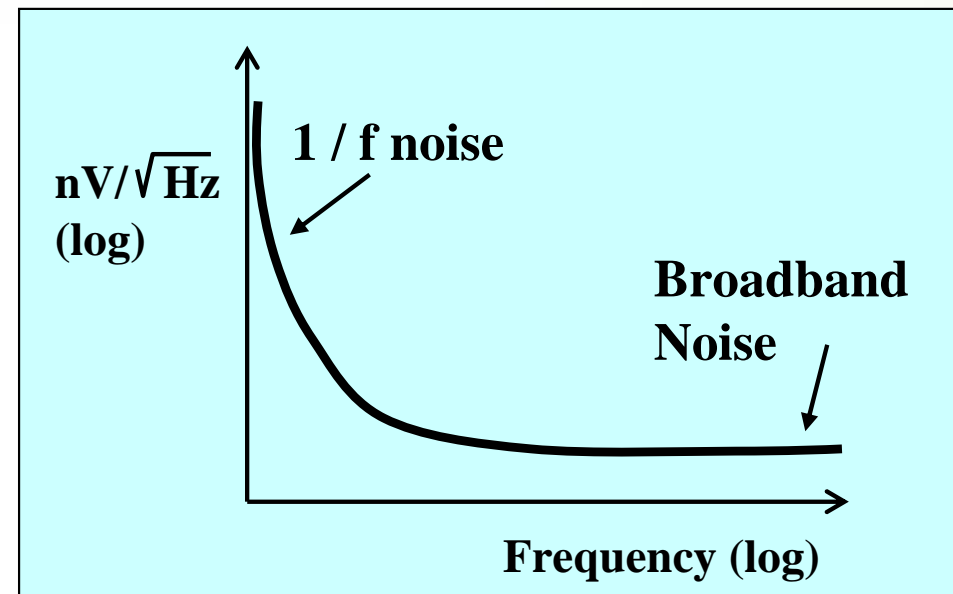
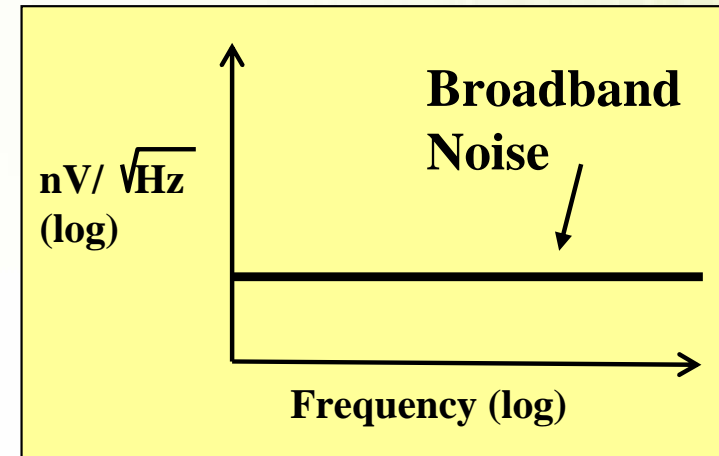
(BW) = Noise Bandwidth in Hz

- $1 \text{ k}\Omega = 4 \text{ nV} / \sqrt{\text{Hz}}$

## ● Amplifiers

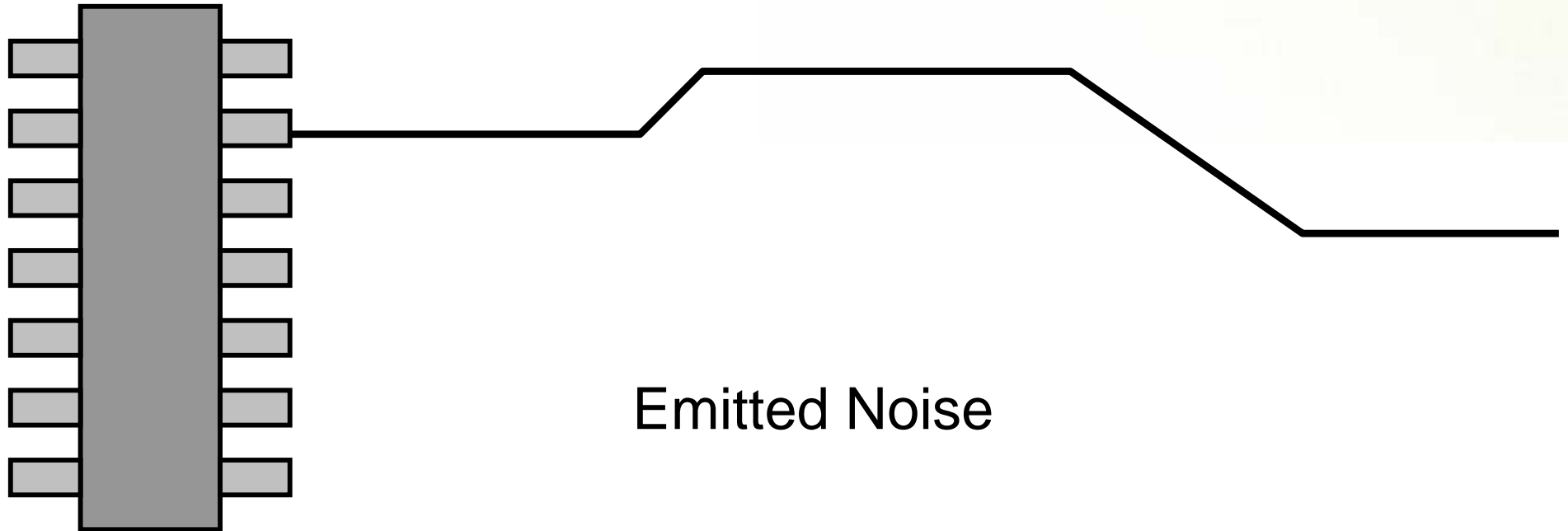
- MCP604 Specification -  
29nV/  $\sqrt{\text{Hz}}$  @ 10 kHz

- MCP6024 Specification -  
10nV/  $\sqrt{\text{Hz}}$  @ 10 kHz



# Long Traces: Antenna

- Trace going into 10-bit or 12-bit ADC input is longer than a few inches



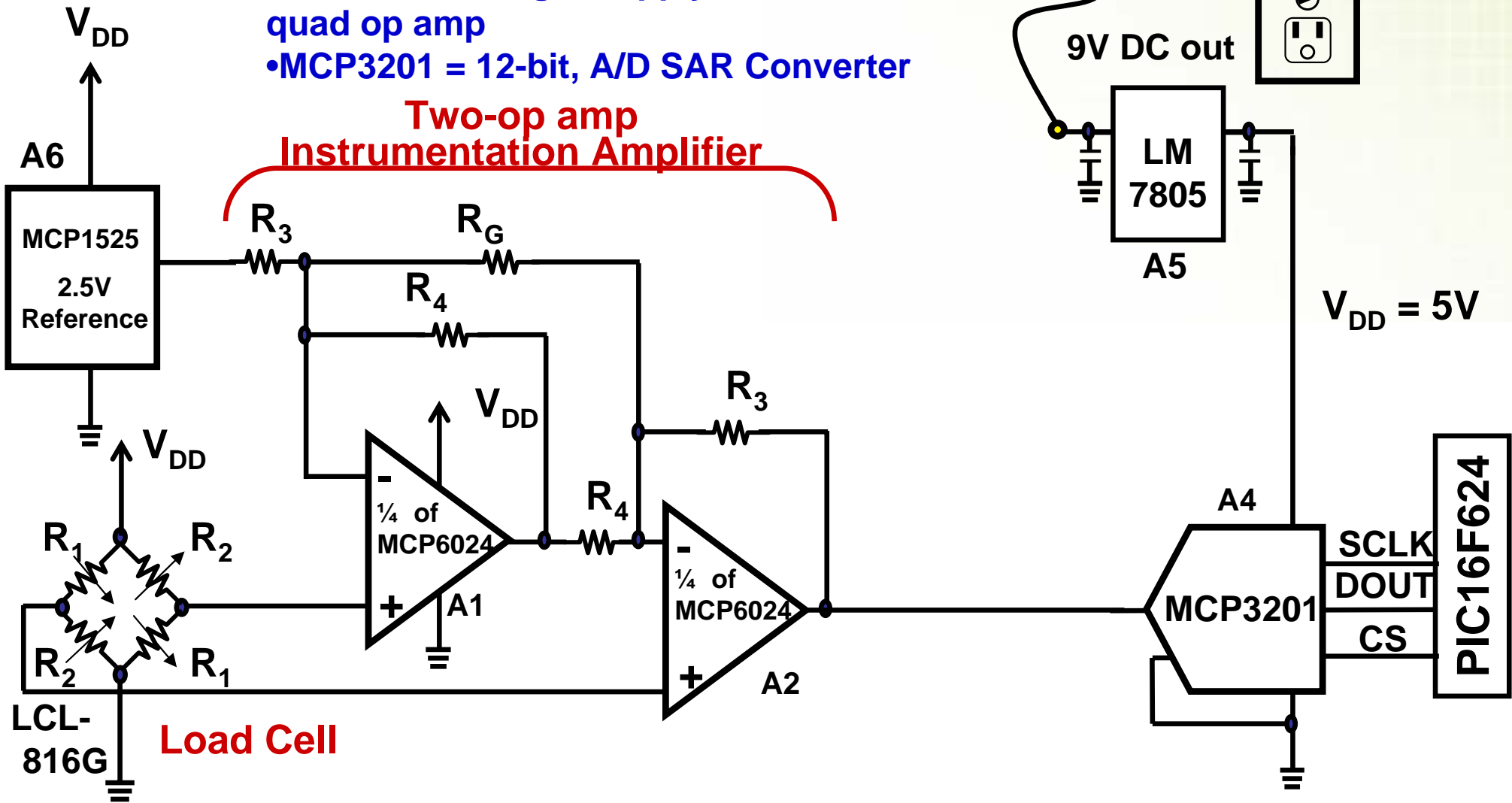
# Analog Application Circuit

Wall Wart

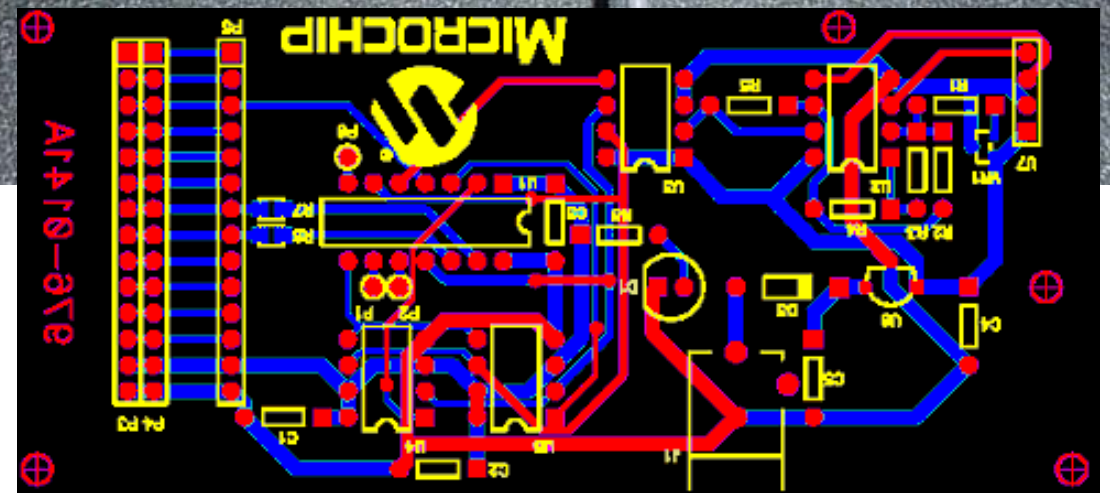
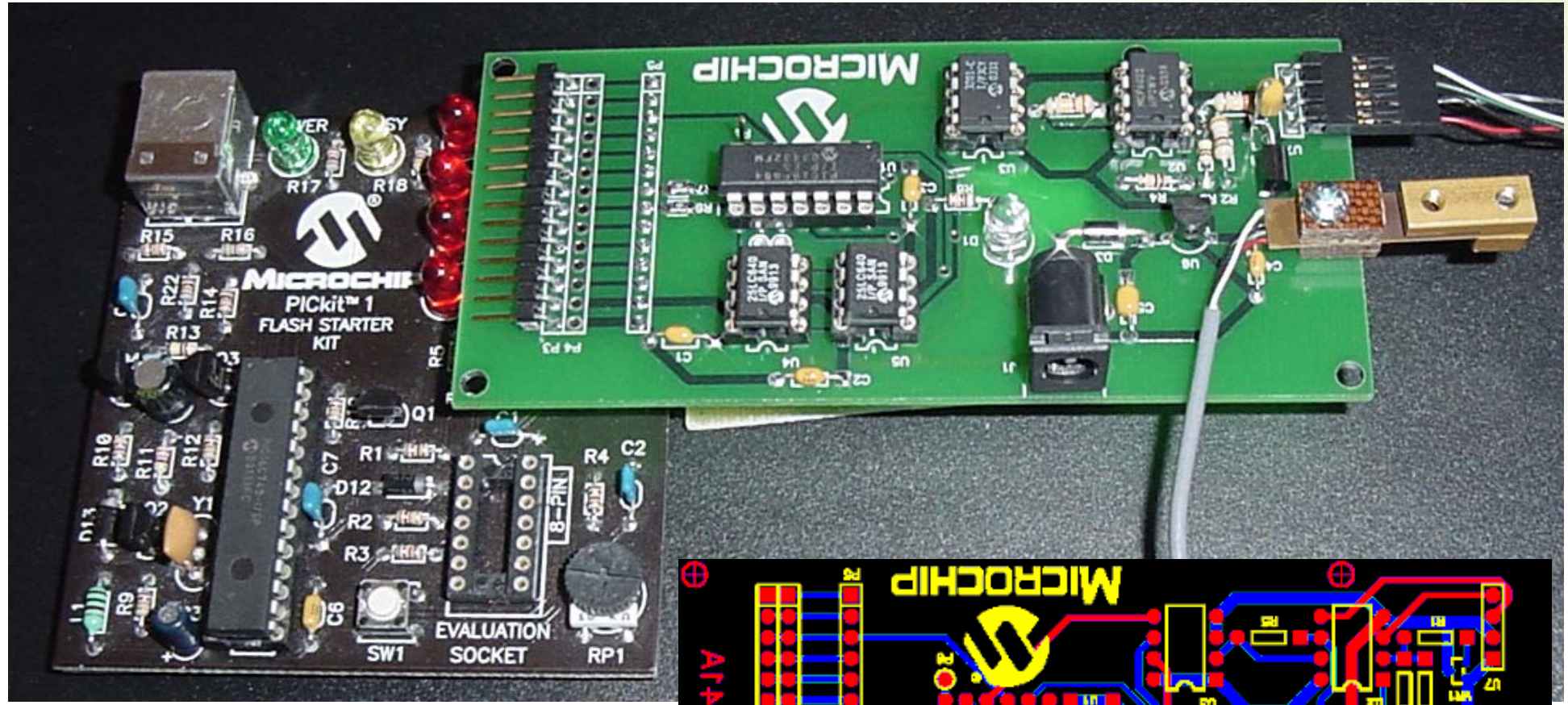
## 12-bit Accurate Circuit Components

- $R_3 = 30k\Omega$ ,  $R_4 = 10k\Omega$ ,  $R_G = 402\Omega$ , (+/-1%)
- MCP6024 = Single Supply, CMOS, low noise, quad op amp
- MCP3201 = 12-bit, A/D SAR Converter

### Two-op amp Instrumentation Amplifier



# Analog Layout #2





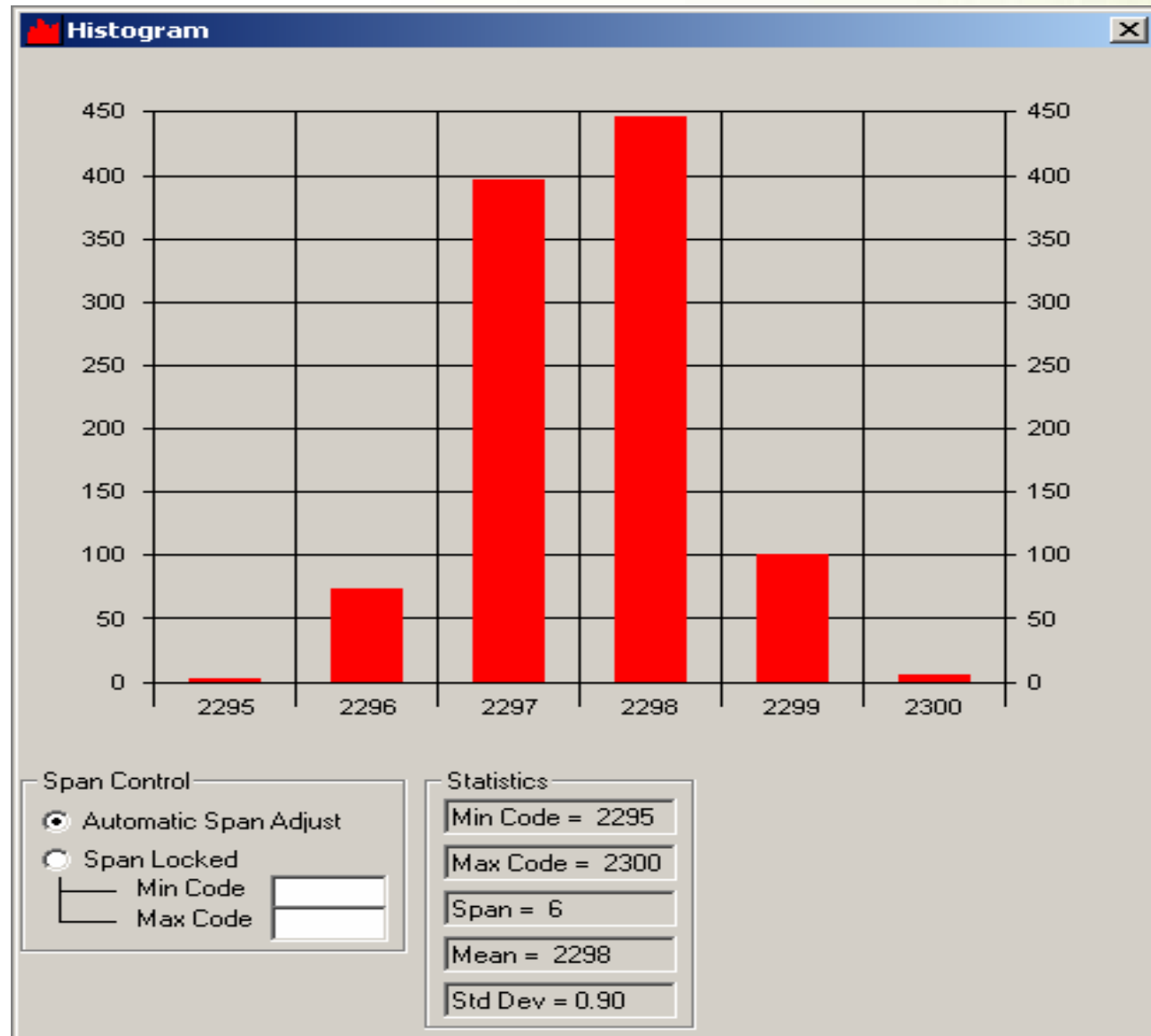
# Analog Application Board #2 Test Results

**Code Width  
of Noise = 6**

**(total samples = 1024)**

**How many bits?**

**9.42-bits**





# Low-Noise Design

- Device Noise - Created by the devices
  - Resistors - Reduce Values where possible
  - Op amps - Use Lower-Noise Amplifiers
  - Power Supply – Replace or Filter Switching Devices
- Emitted Noise - Externally Injected
  - Layout - Keep analog and digital Separate
  - Environment - Shield or change orientation
- Conducted Noise - In the Circuit Traces
  - Use a Continuous Ground Plane
  - Filter Signal traces
  - Filter Supply traces



# Conducted Noise

- Ground and Power
  - 50 Hz or 60 Hz
  - Ground and Supply Current Return Paths
- Solution: By-pass, Choke supply line
  
- Signal Path
  - Digital Switching
  - Noise generated by previous device
- Solution: Analog Filter, Re-layout



# Discontinuous Ground Plane

- Interrupted Ground Plane on the Back Side of the Board



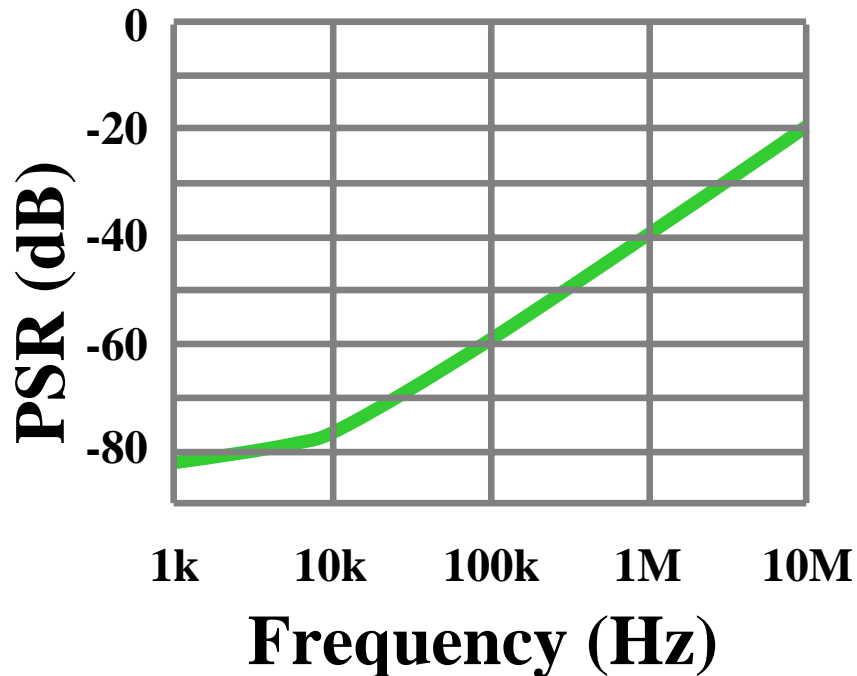


# Bypass Capacitors No Black Magic Here

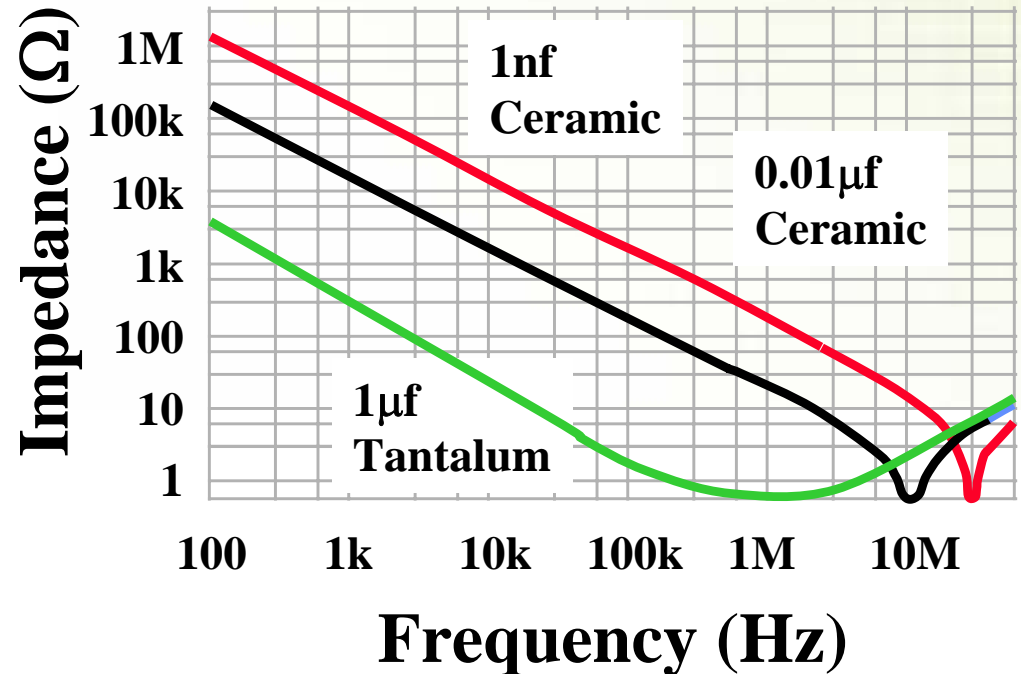
- As close to the device as possible
- Analog Circuits
  - Reduce power supply noise
  - Enhance Chip's Power Supply Rejection (PSR)
- Digital Circuits
  - Low Frequency system clocks have high frequency glitches
  -

# Bypass Capacitors for Analog

## 12-bit A/D Converter



## Capacitor Response



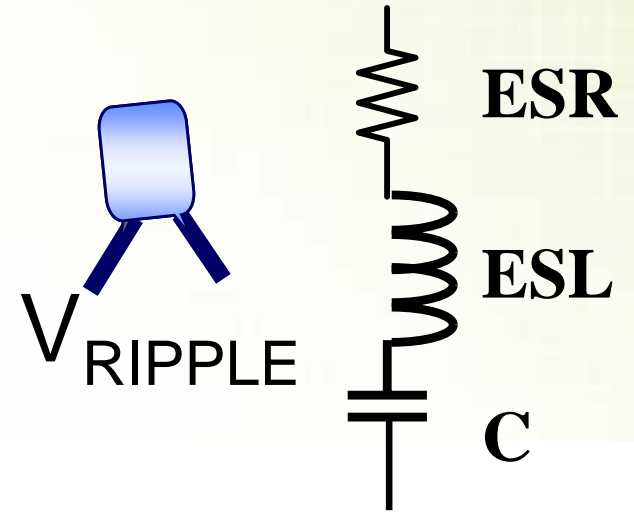
- Assume: Supply =  $5V \pm 20 \text{ mV}$  (all white noise)
  - To bring the noise to  $\pm 1/4 \text{ LSB}$  ( $\pm 0.61 \text{ mV}$ )
  - $\text{PSR} < -30.3 \text{ dB}$

# Bypass Capacitors for Digital

- Determine noise frequency

$$f_{\text{noise}} = 1 / ( 2 * t_{\text{rise}} )$$

- Determine max. ripple voltage

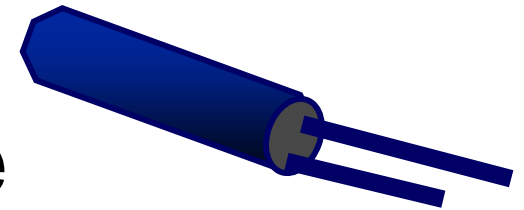


- Approximate surge current

$$I_{\text{SURGE}} = I_{\text{AVE}} * f_{\text{noise}} / f_{\text{MICRO}}$$

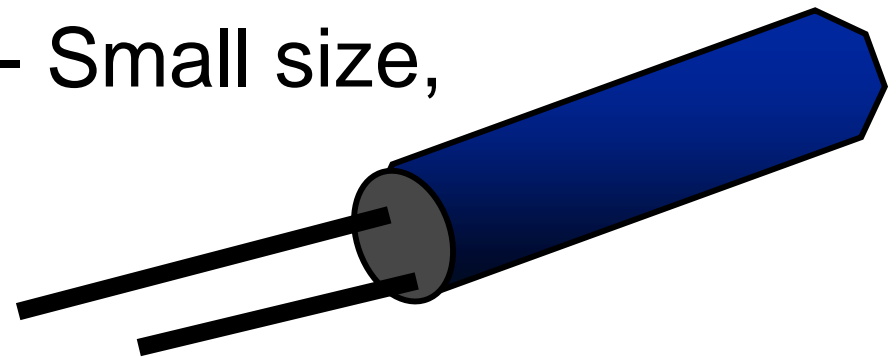
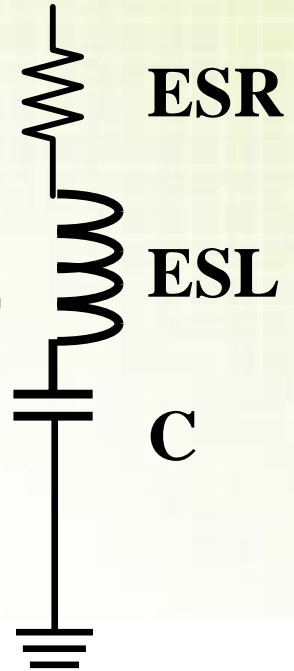
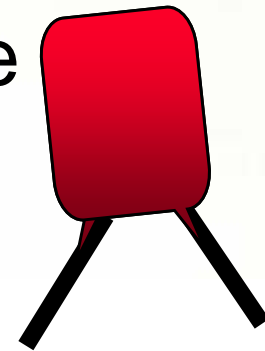
- Calculate bypass capacitor value

$$C_{\text{BYPASS}} = I_{\text{SURGE}} / ( 2 * \pi * f_{\text{noise}} * V_{\text{RIPPLE}} )$$



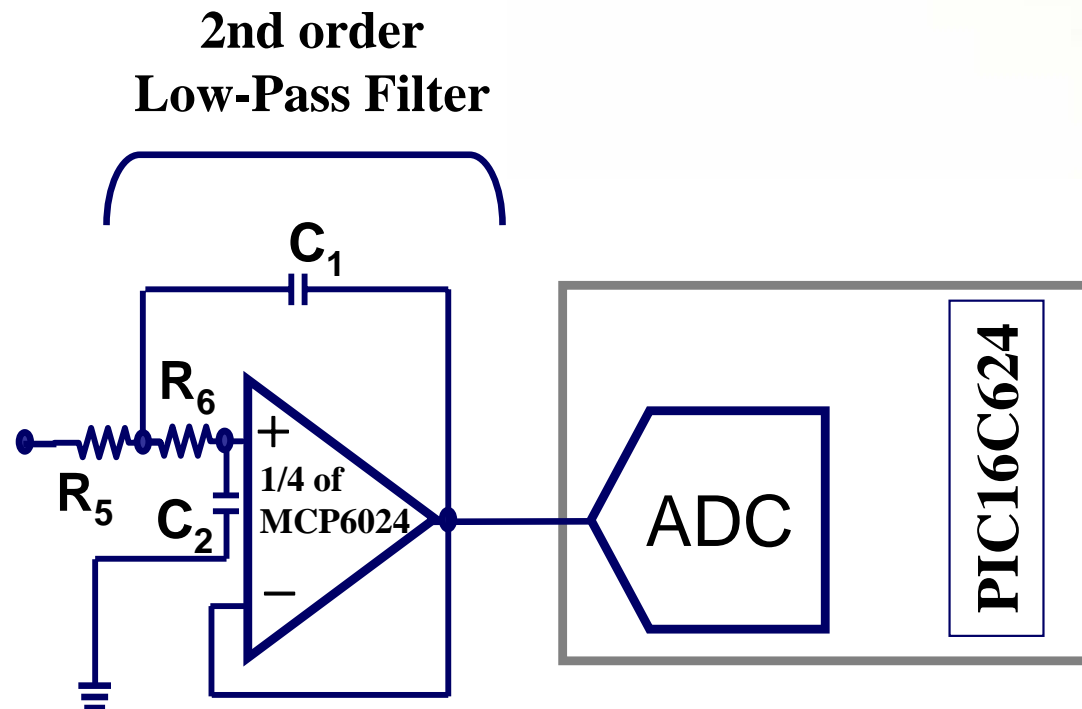
# Bypass Capacitor Types

- Filters Noise at High Frequency
  - Ceramic - Small Case size, Inexpensive, Good Stability, Low Inductance
    - NPO
    - X7R
- Acts as a Charge Reservoir for Fast Changes
  - Tantalum Electrolytic - Small size, Large Values, Medium Inductance



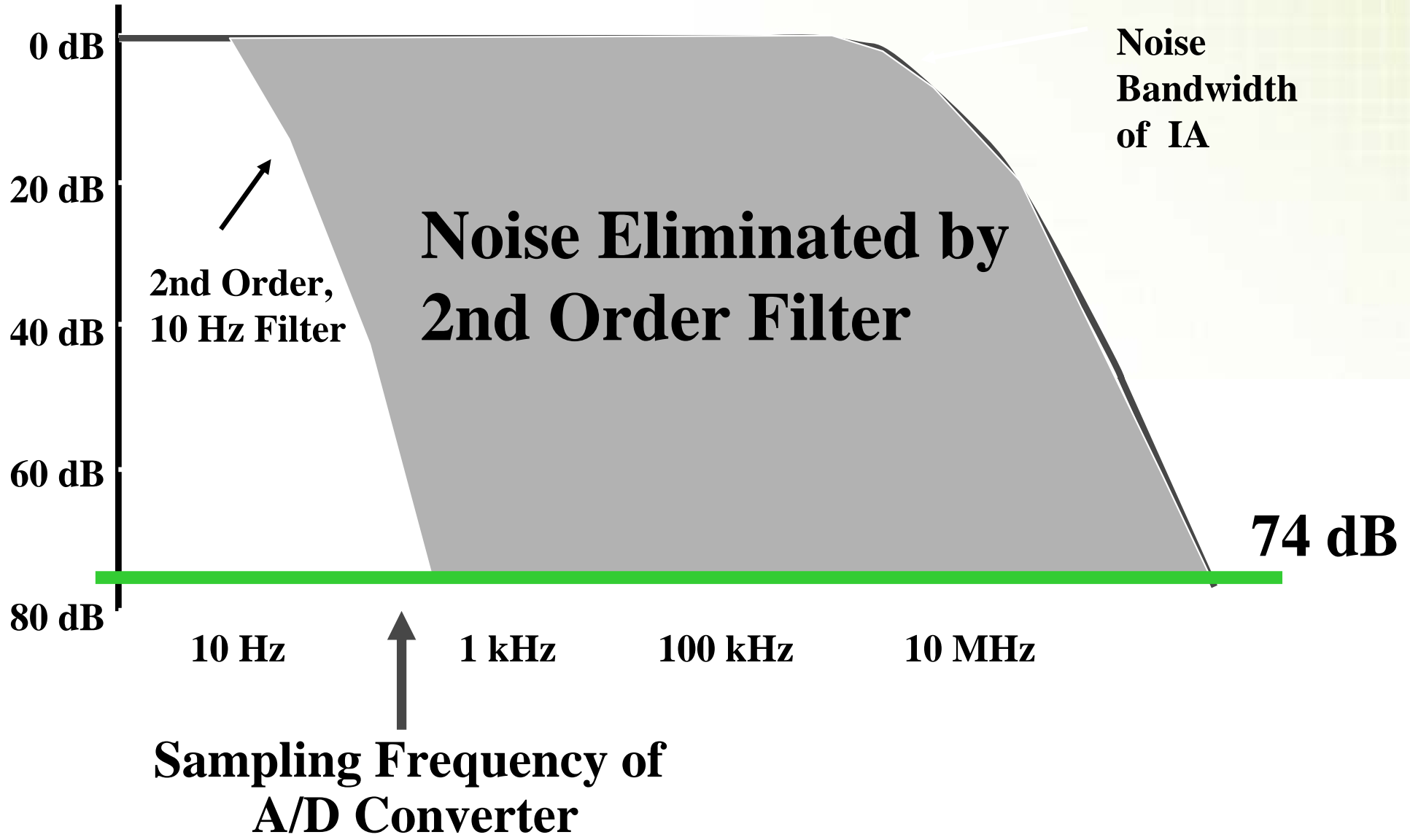
# Low-Pass Filter Missing

- Add anti-aliasing (or Low-Pass) Filter at the input of the ADC





# Noise Reduction with Low-Pass Analog Filter



# Analog Application Circuit

## 12-bit Accurate Circuit Components

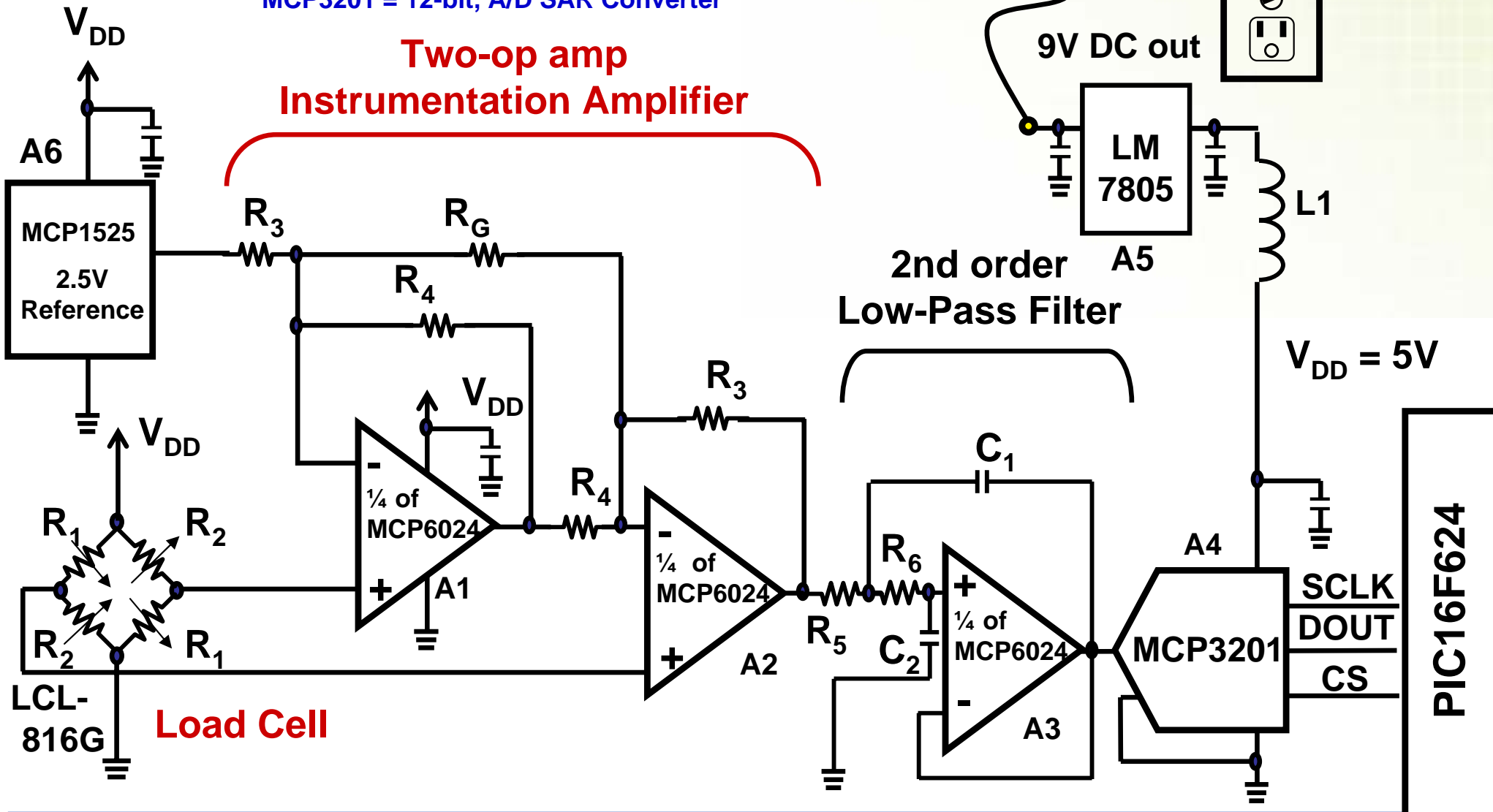
$R_5 = 27.4 \text{ k}\Omega$ ,  $R_6 = 196 \text{ k}\Omega$ ,  $C_1 = 100 \text{ nF}$ ,  $C_2 = 470 \text{ nF}$

Bypass Capacitors

Ground Plane

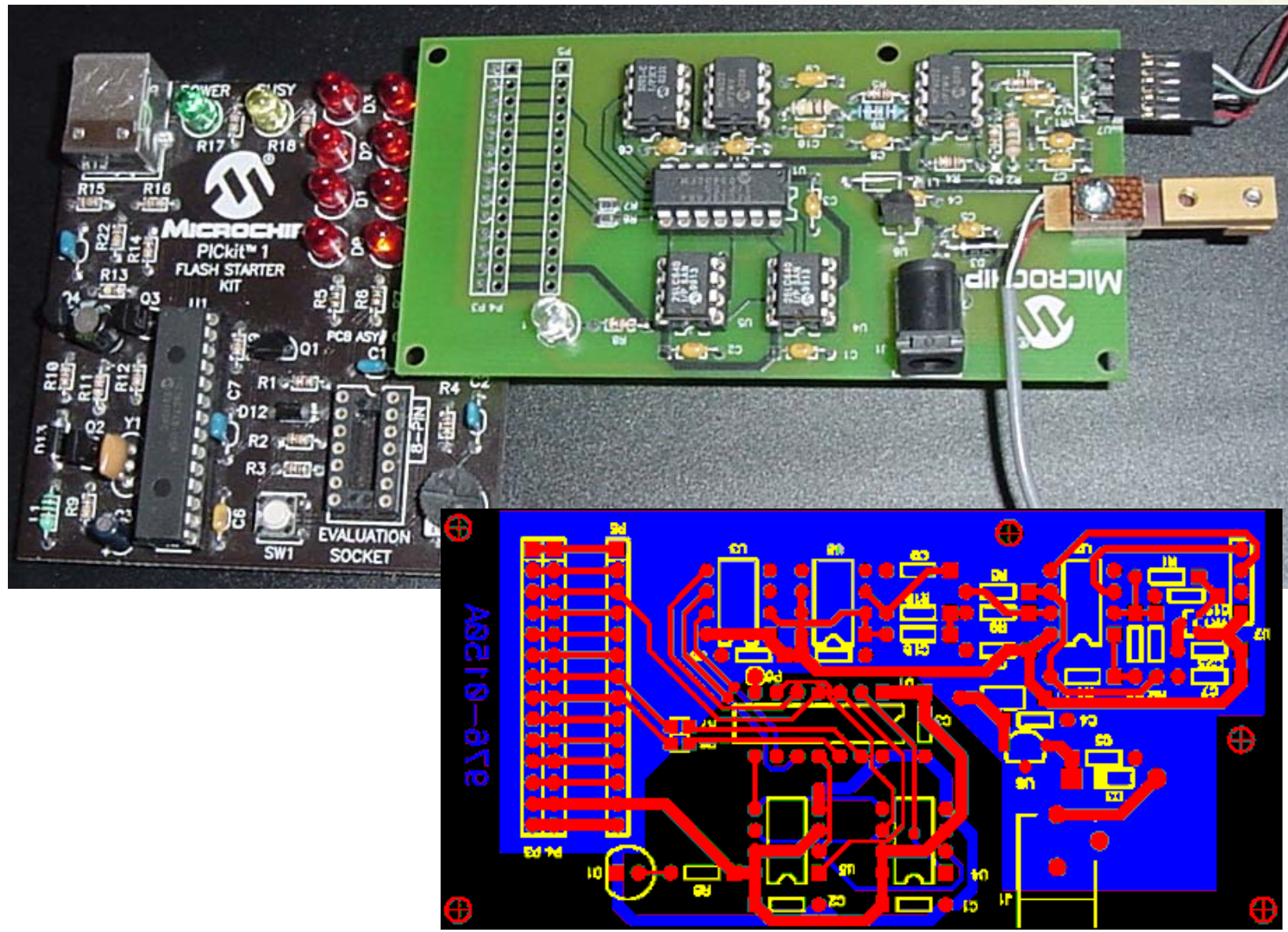
MCP3201 = 12-bit, A/D SAR Converter

**Two-op amp  
Instrumentation Amplifier**





# Analog Layout #3





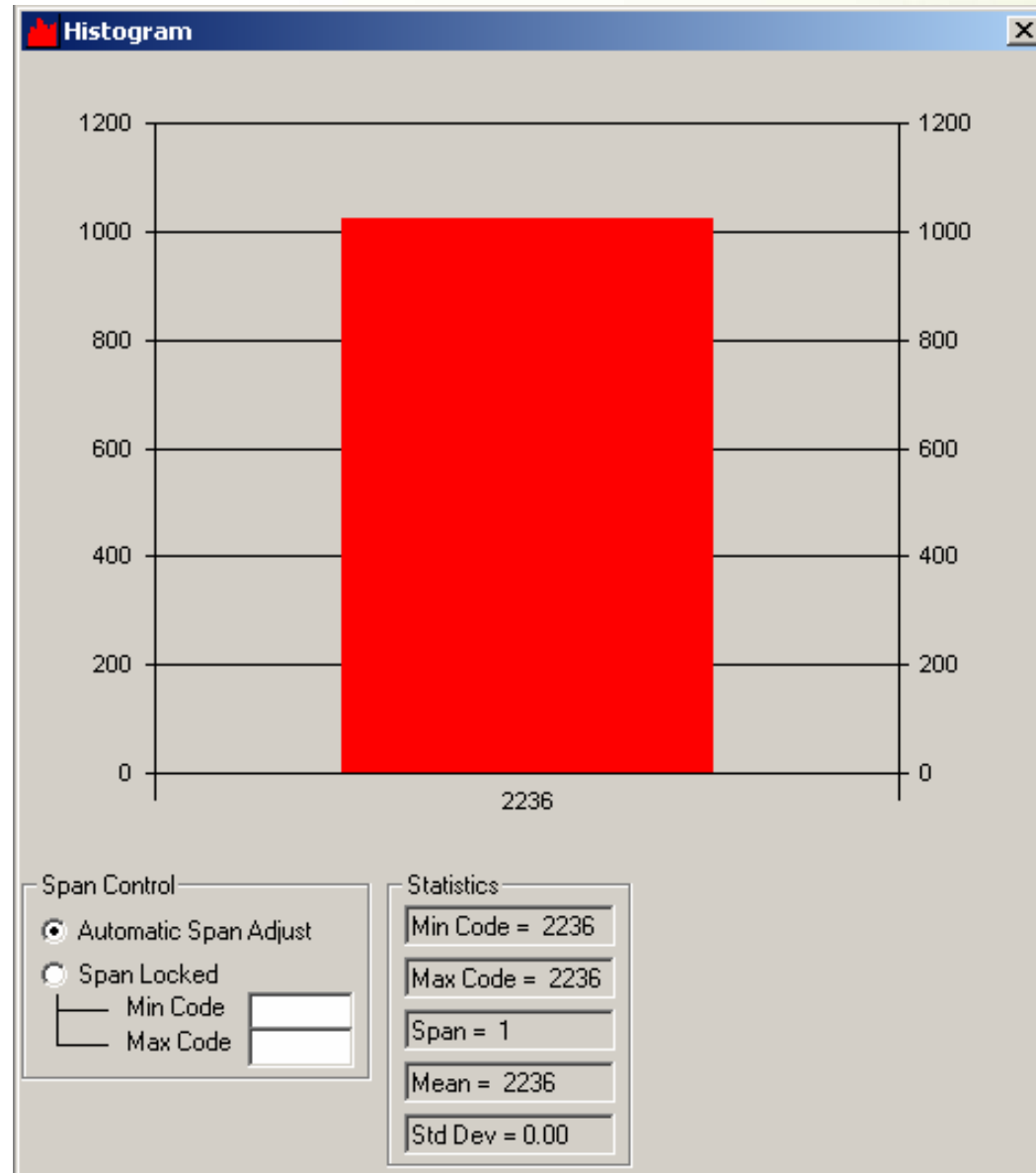
# Analog Application Board #3 Test Results

**Code Width  
of Noise = 1**

**(total samples = 1024)**

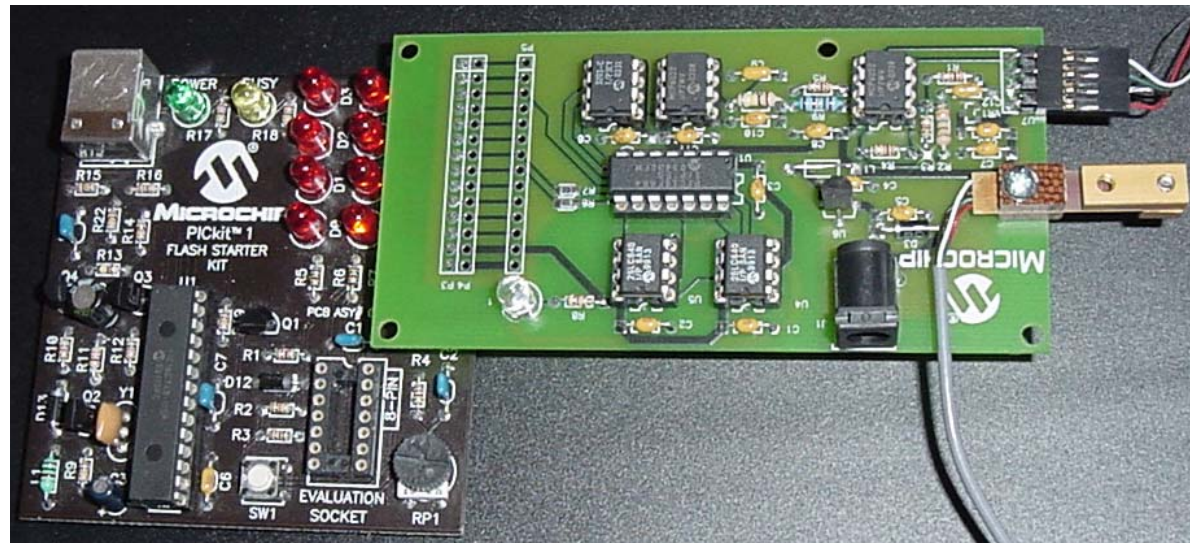
**How many bits?**

**12-bits**

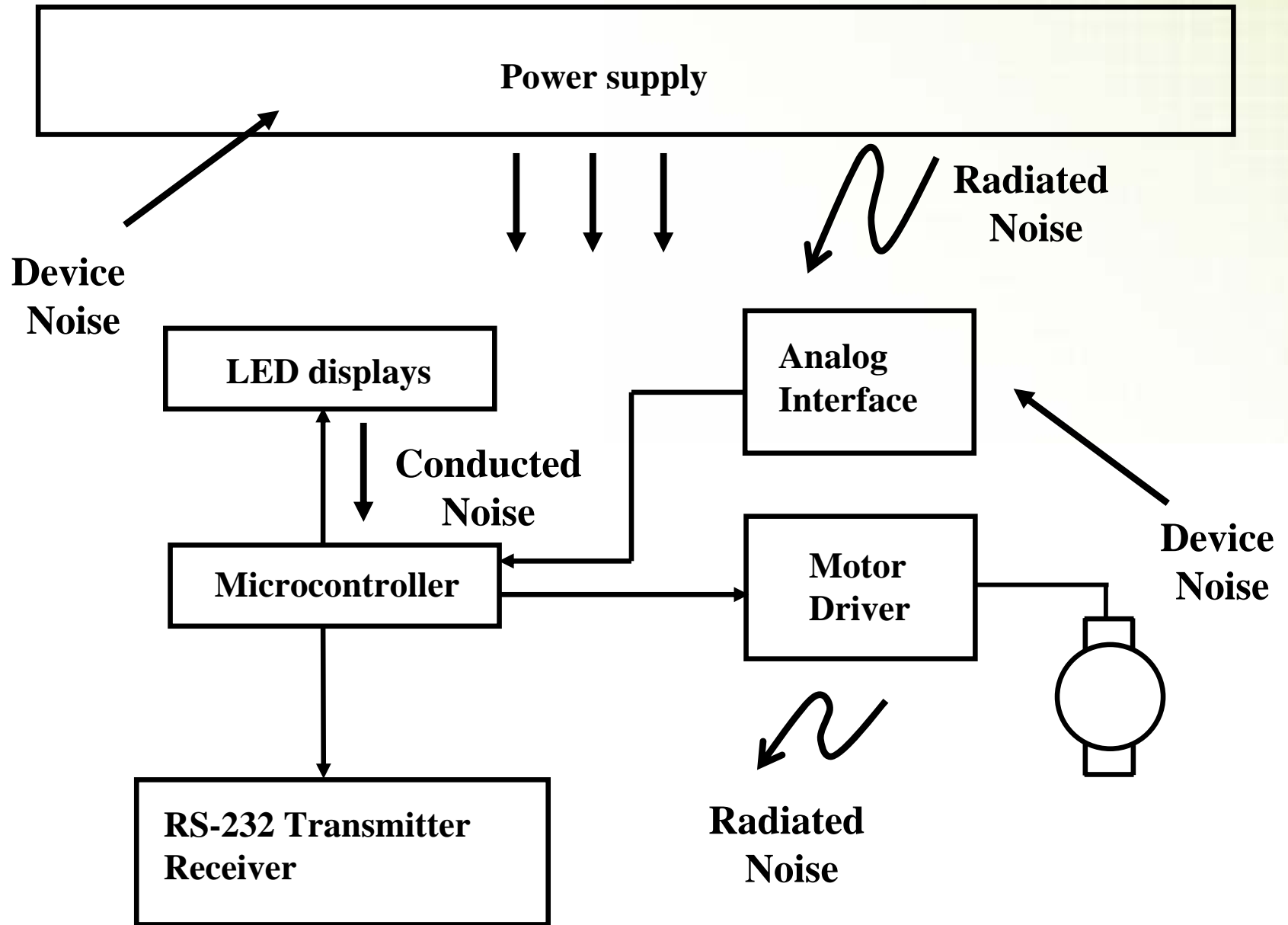


# Analog Design Conclusions

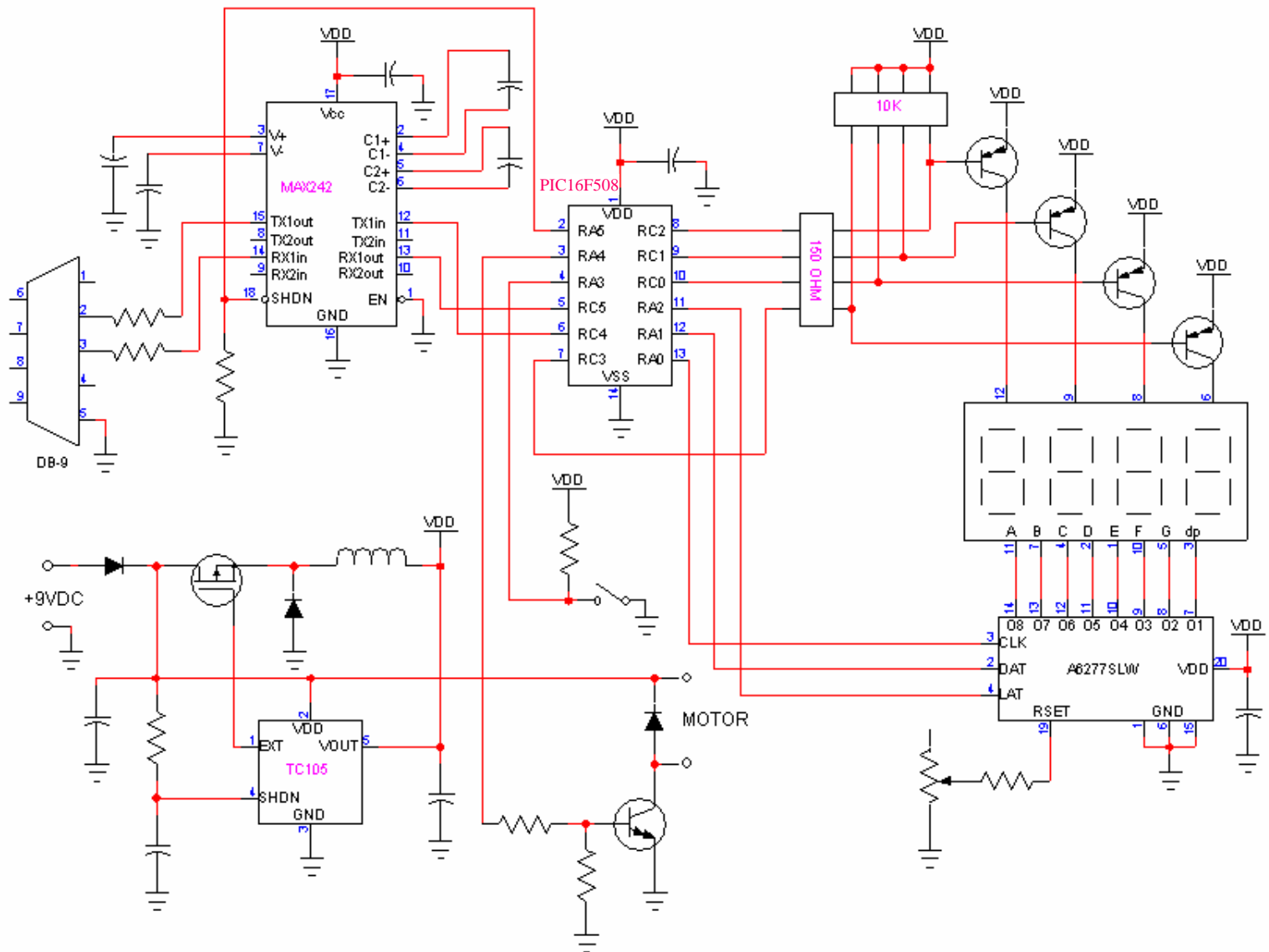
- Use
  - Low-noise devices
  - Uninterrupted ground plane
  - Low-pass anti-aliasing filter
- By-pass all devices
  - Place the capacitors as close to the power pins of the devices as possible.



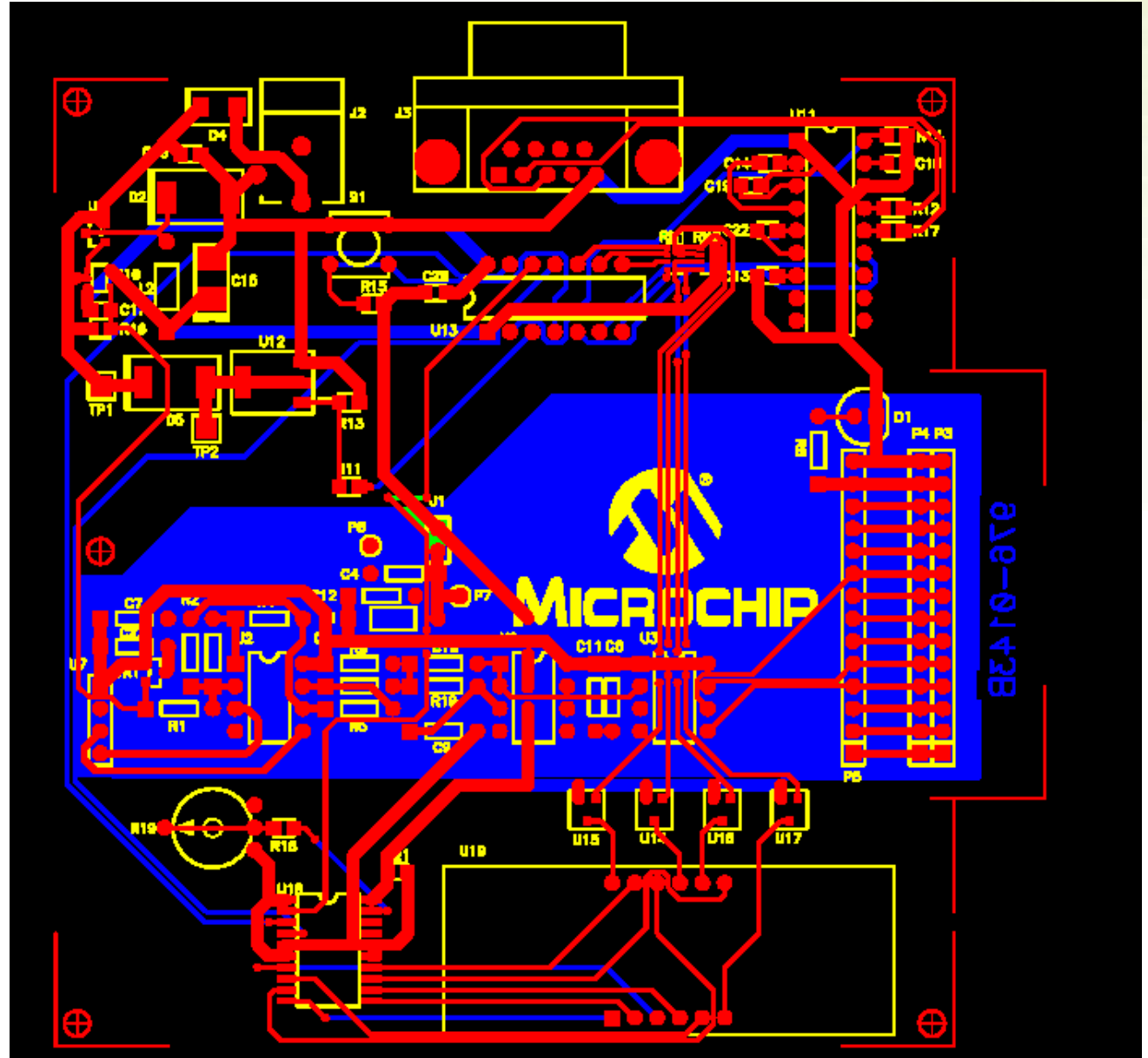
# Adding the Digital System



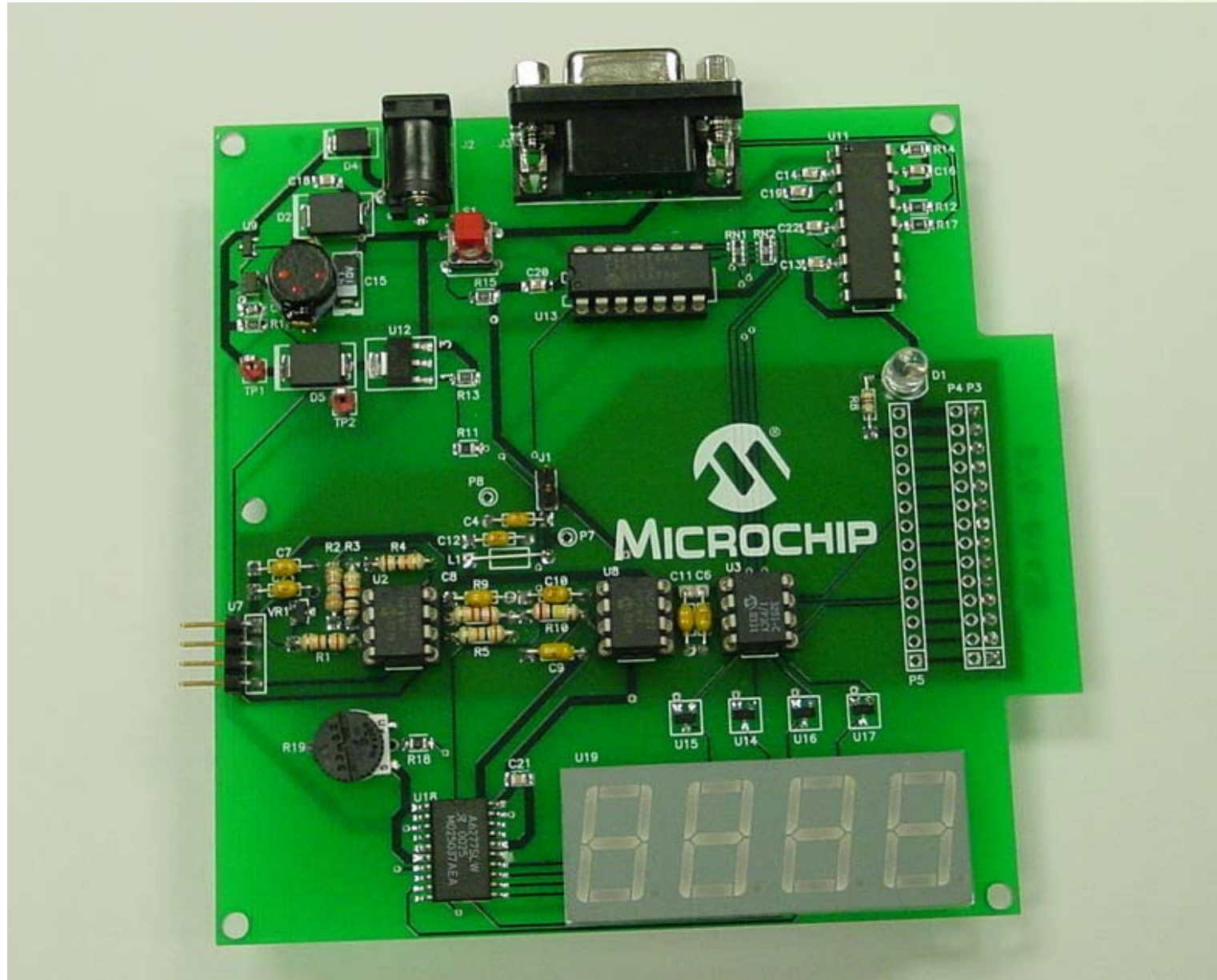
# Schematic of the Digital Section



# First Pass Combined Layout



# Application Board #4

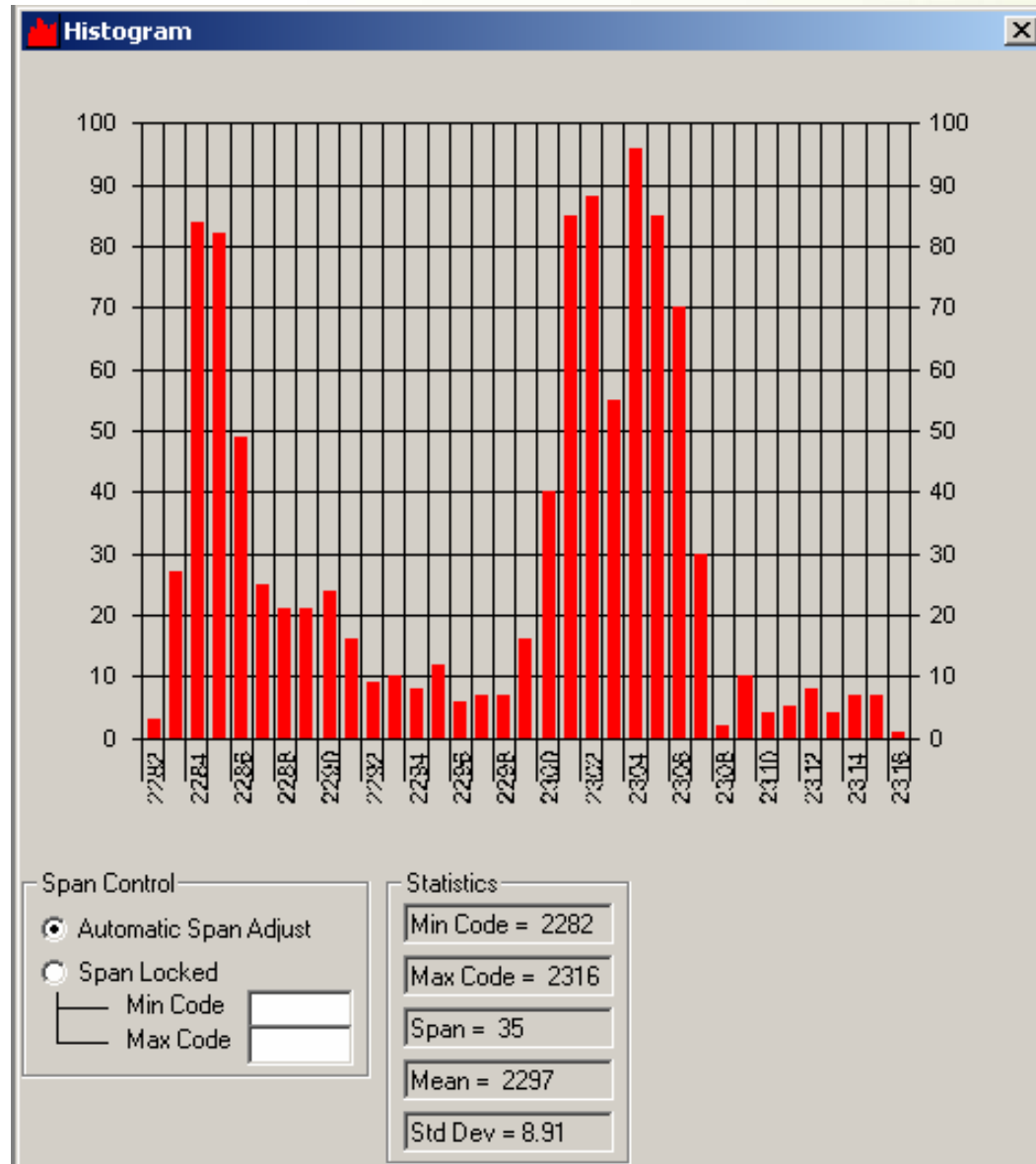




# Combined Analog/Digital Test-Board Results

**Code Width  
of Noise = 35**

**(total samples = 1024)**



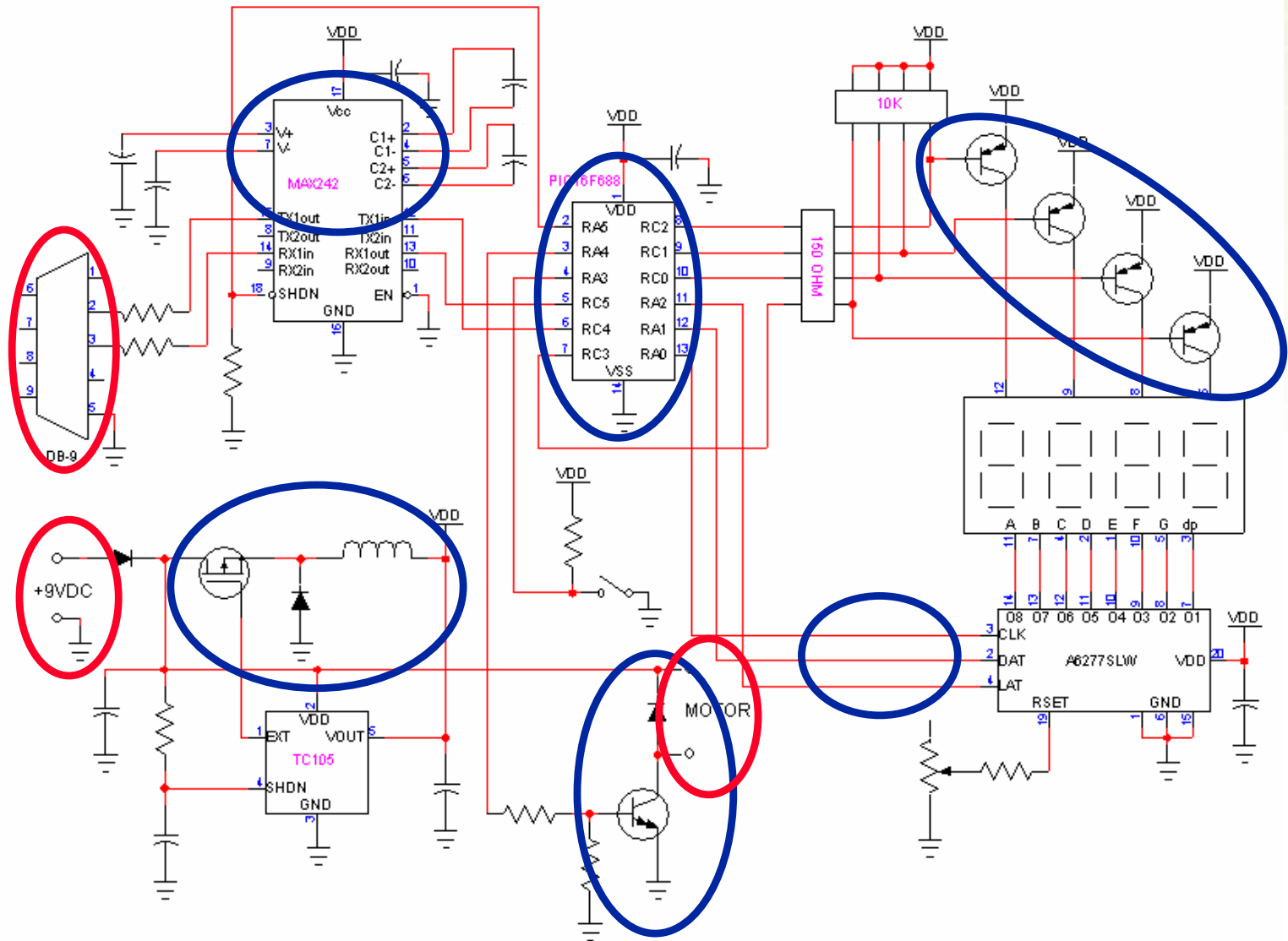




# Identify the Noise Sources

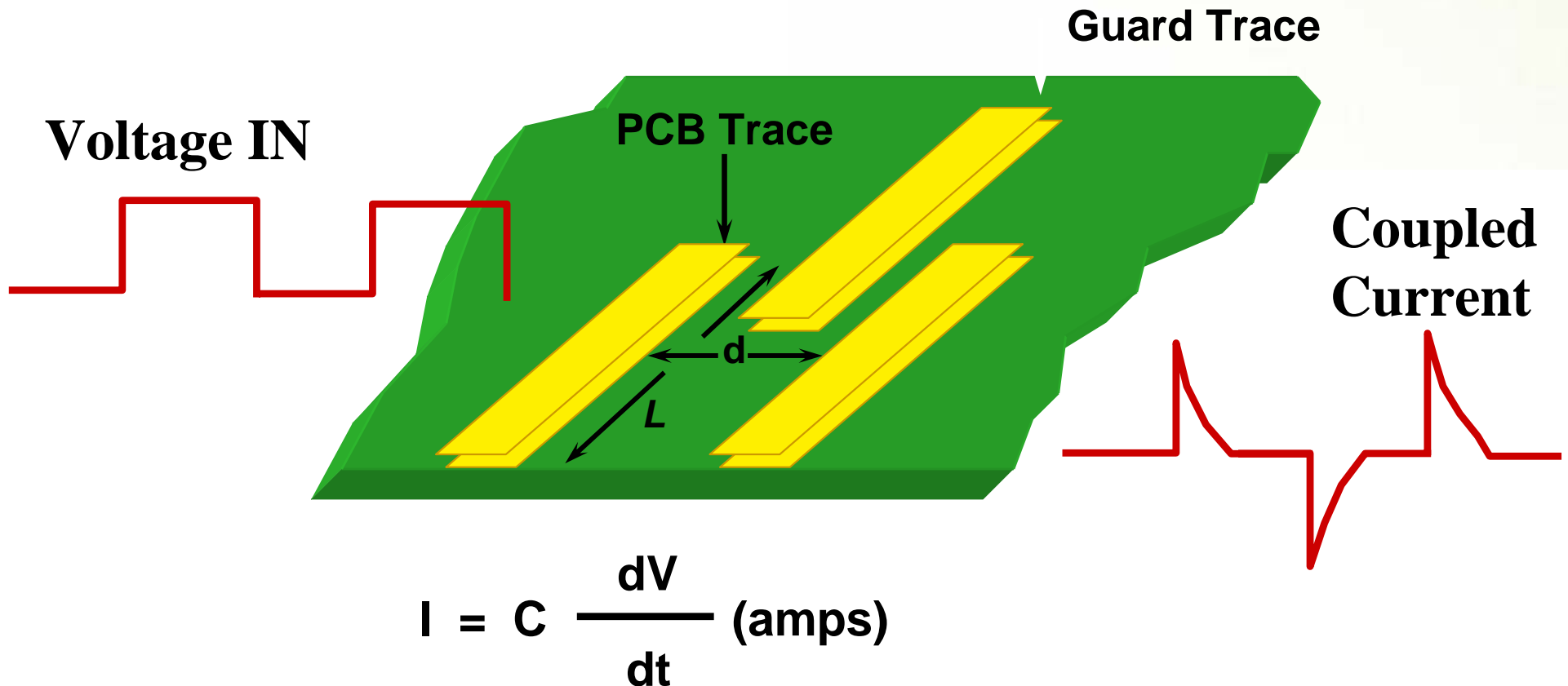
- Device and Conducted noise sources
  - Switching noise generated by fast rise time signals
  - Switching noise generated by high voltage/current switching
- External noise sources
  - Externally generated Electro-Magnetic Interference or EMI
  - Externally generated Radio-Frequency Interference or RFI

# Identify the Noise Sources



# PCB Capacitance

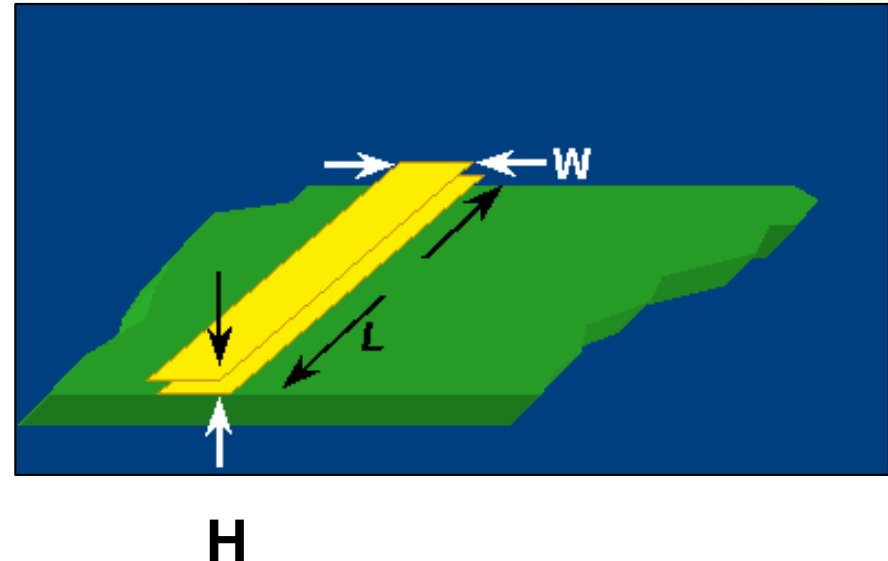
- Decrease “L” or Increase “d”  $C = \frac{w \cdot L \cdot \epsilon_0 \cdot \epsilon_r}{d}$  pF
- Put Ground Guard Between Traces



# PCB Trace Resistance

$$R = \frac{L \cdot \square}{W \cdot H} \quad \Omega$$

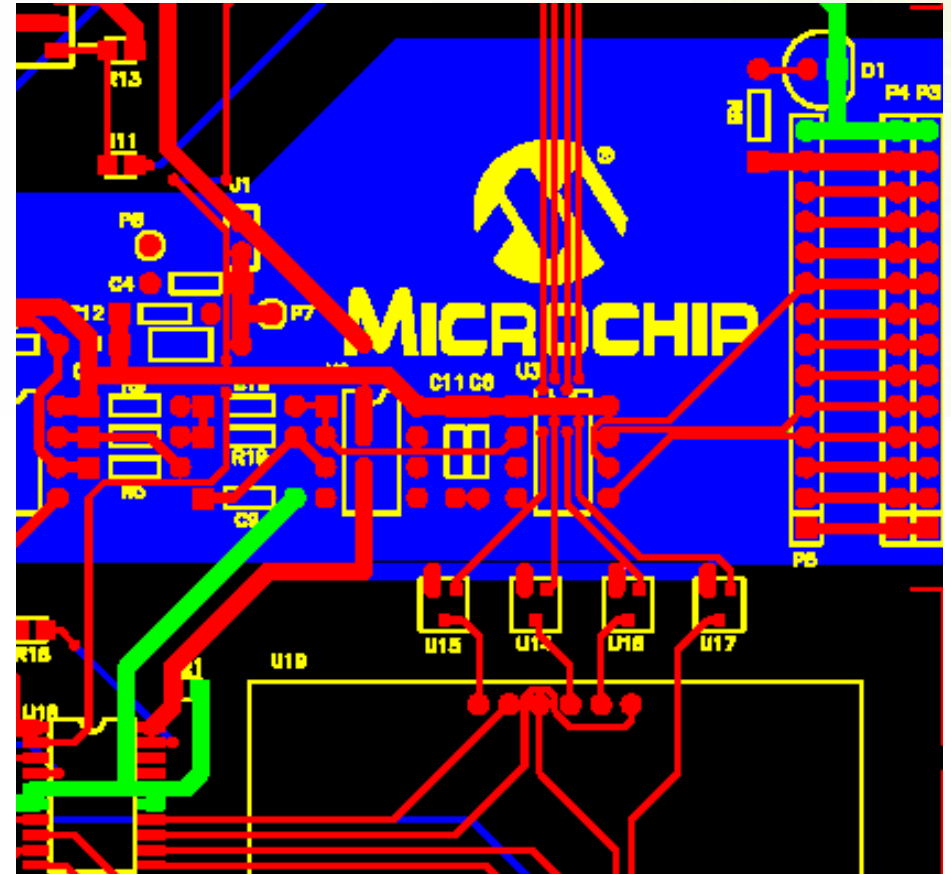
$$I = \frac{V}{R} \quad \text{amps}$$



- Reduce Noise by
  - ↑ W (width of trace)
  - ↓ L (length of trace)
  - ↑ H (thickness of trace)

# Conducted Noise Pathway: Ground

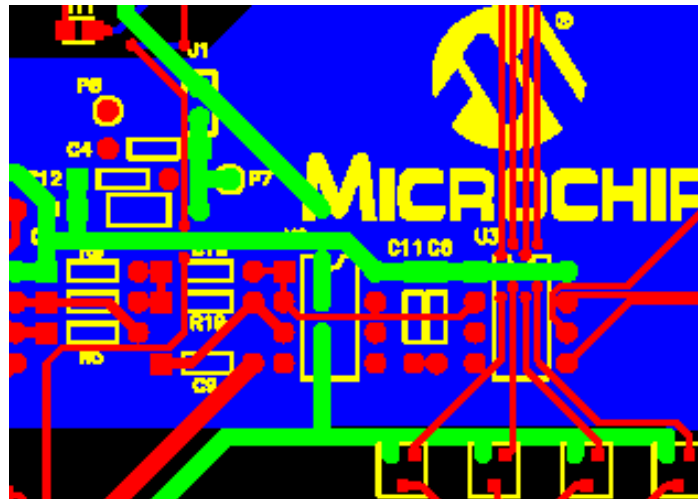
- Pathway:
  - Fast rise time currents react with trace inductance to generate noise voltages
  - High currents react with trace resistance to generate noise voltages





# Conducted Noise Pathway: Power

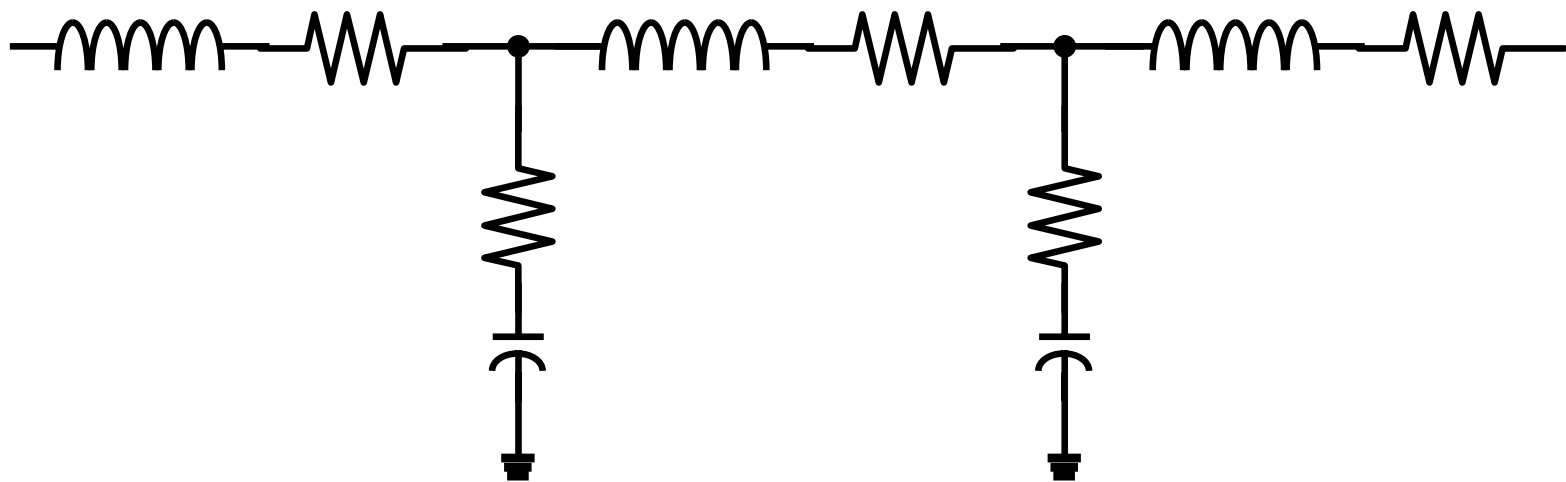
- Pathway:
  - Fast rise time generate noise
  - High currents generate noise



# Conducted Noise

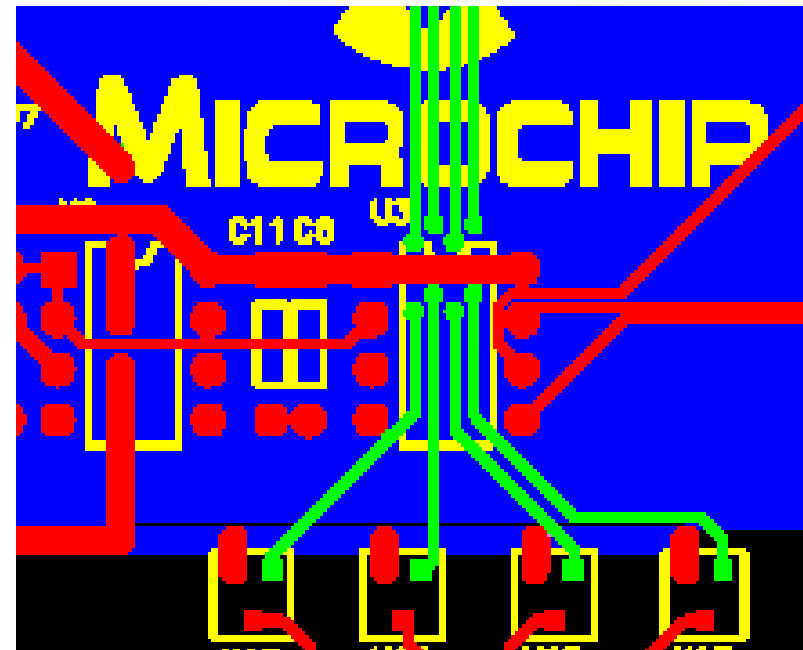
## Corrective Action: Power II

- Use low-pass filtering to isolate noise
  - Circuits on their own power traces
    - Creates higher series impedances
  - Bypass capacitors
    - present a low shunt impedance



# Radiated Noise: EMI

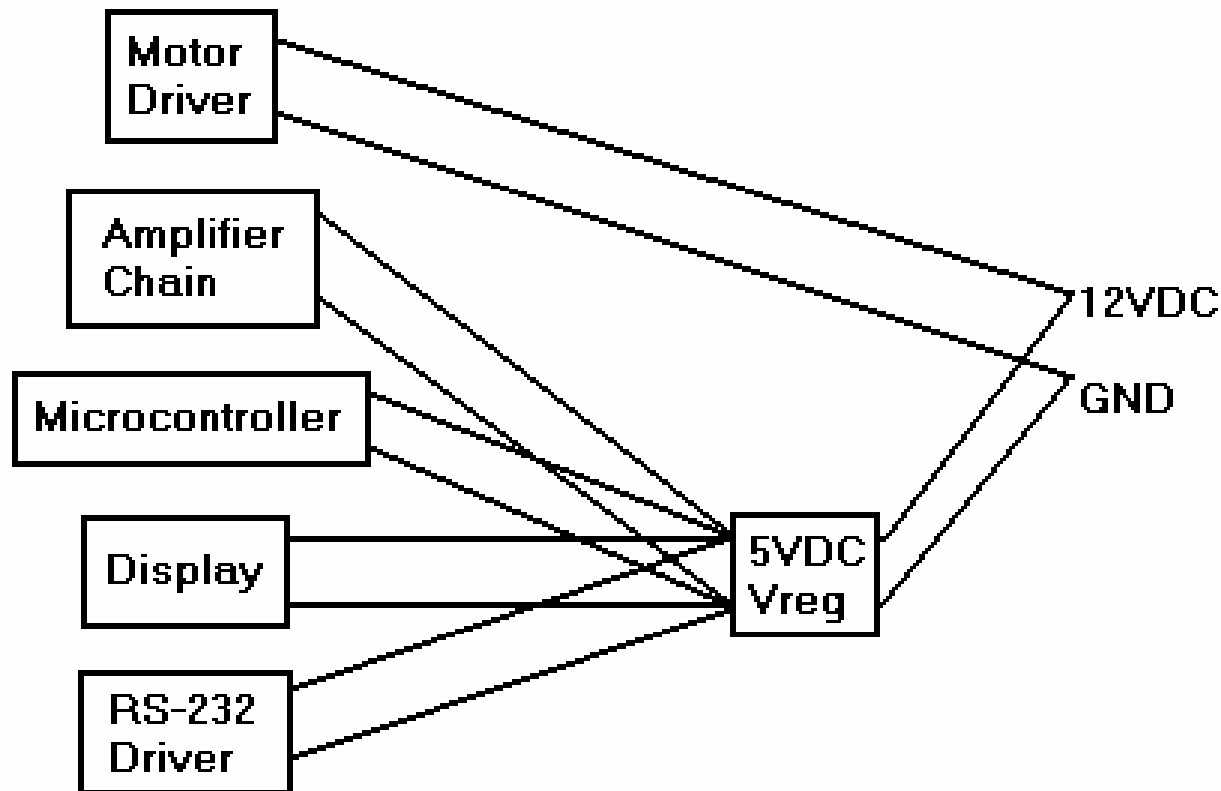
- Pathway: EMI
  - Adjacent traces create unintended capacitors
  - Adjacent traces create unintended transformers
- Corrective Action: EMI
  - Increased distance
  - Decrease common area





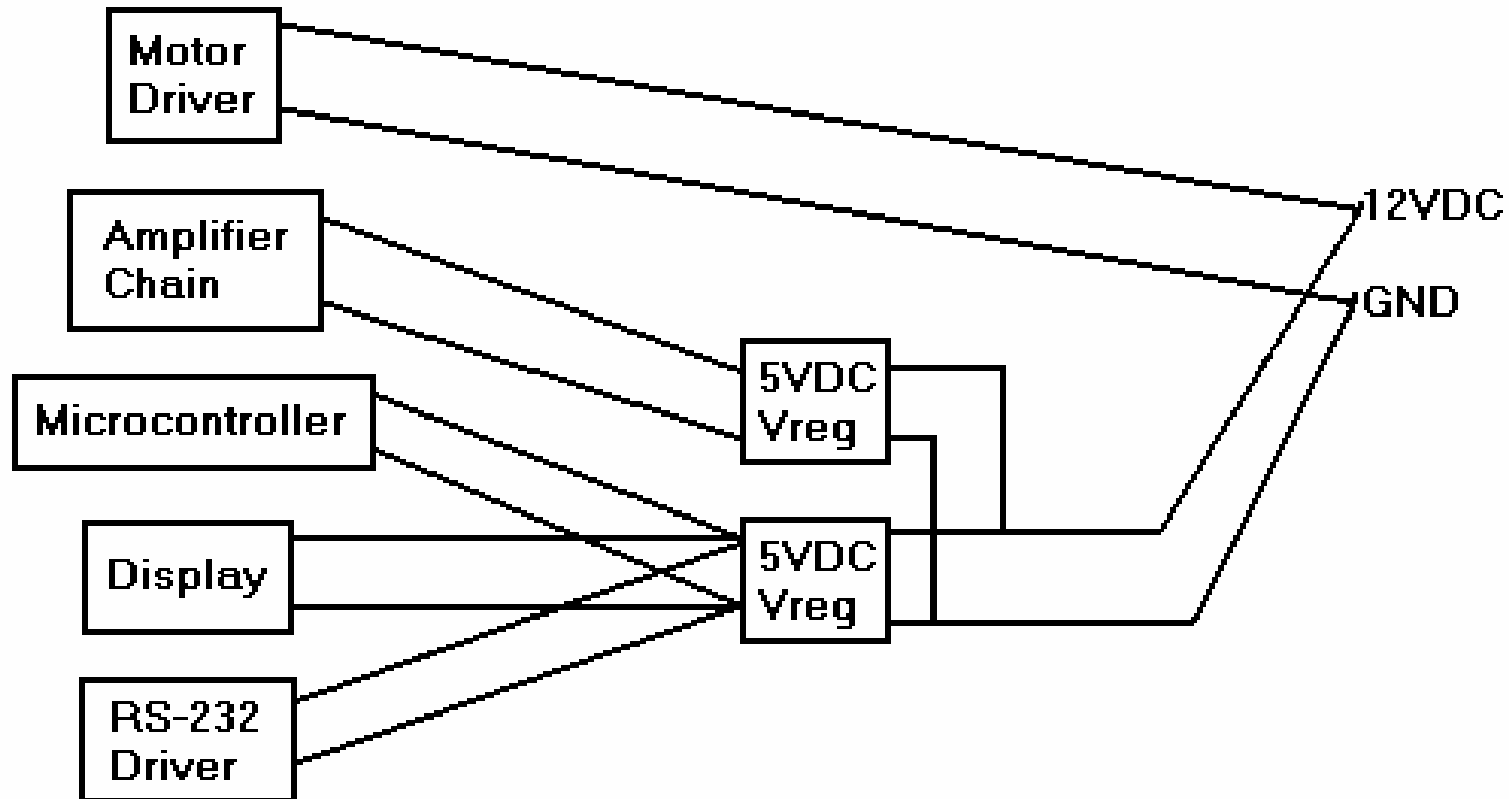
# Mapping Out the Plan

- Draw design sections
- Add the connections



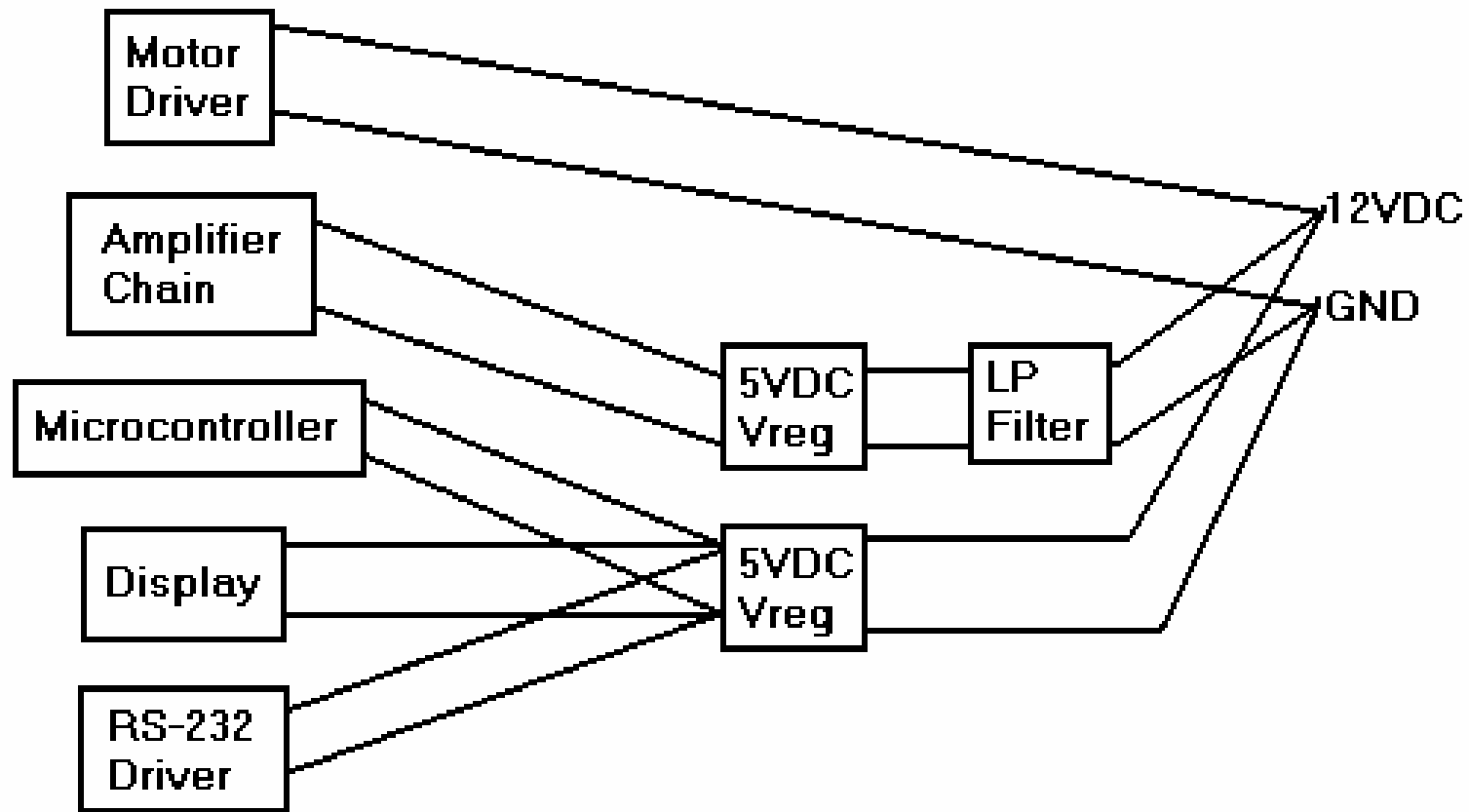
# Revising the Plan

- Route to maximize isolation
  - Between noisy and sensitive blocks
  - Keep runs short



# Revising the Plan Again

- Identify additional isolation requirements

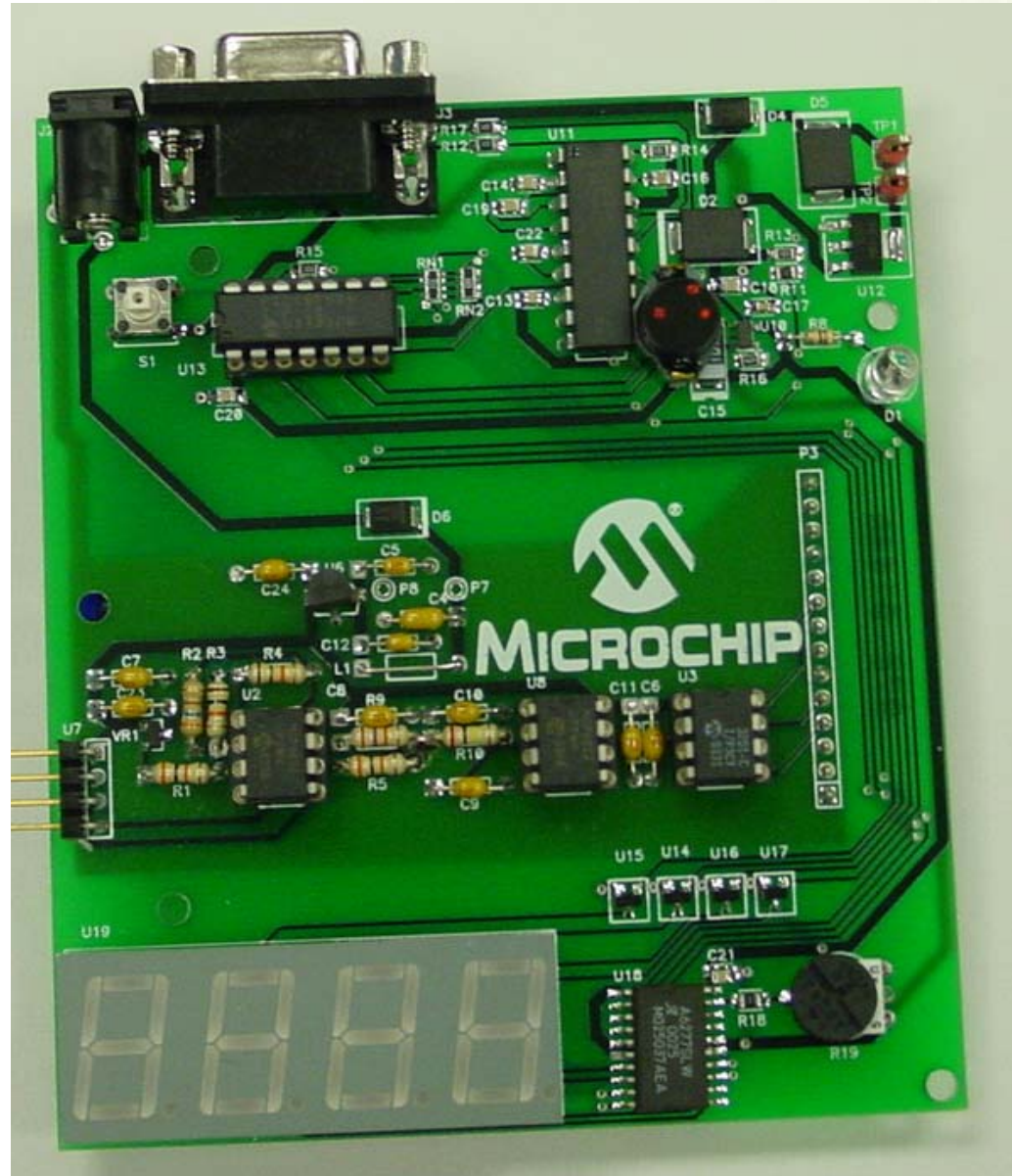




# Re-layout the Board

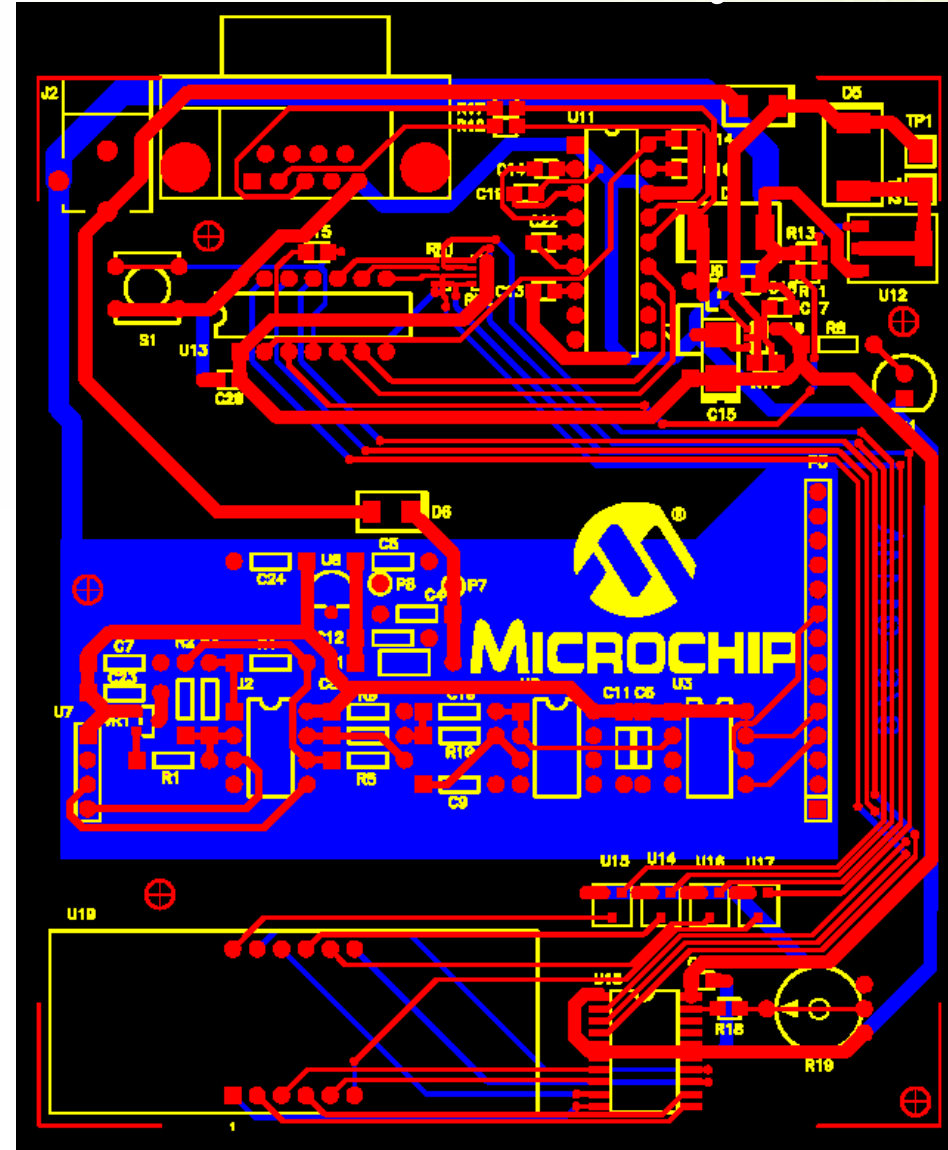
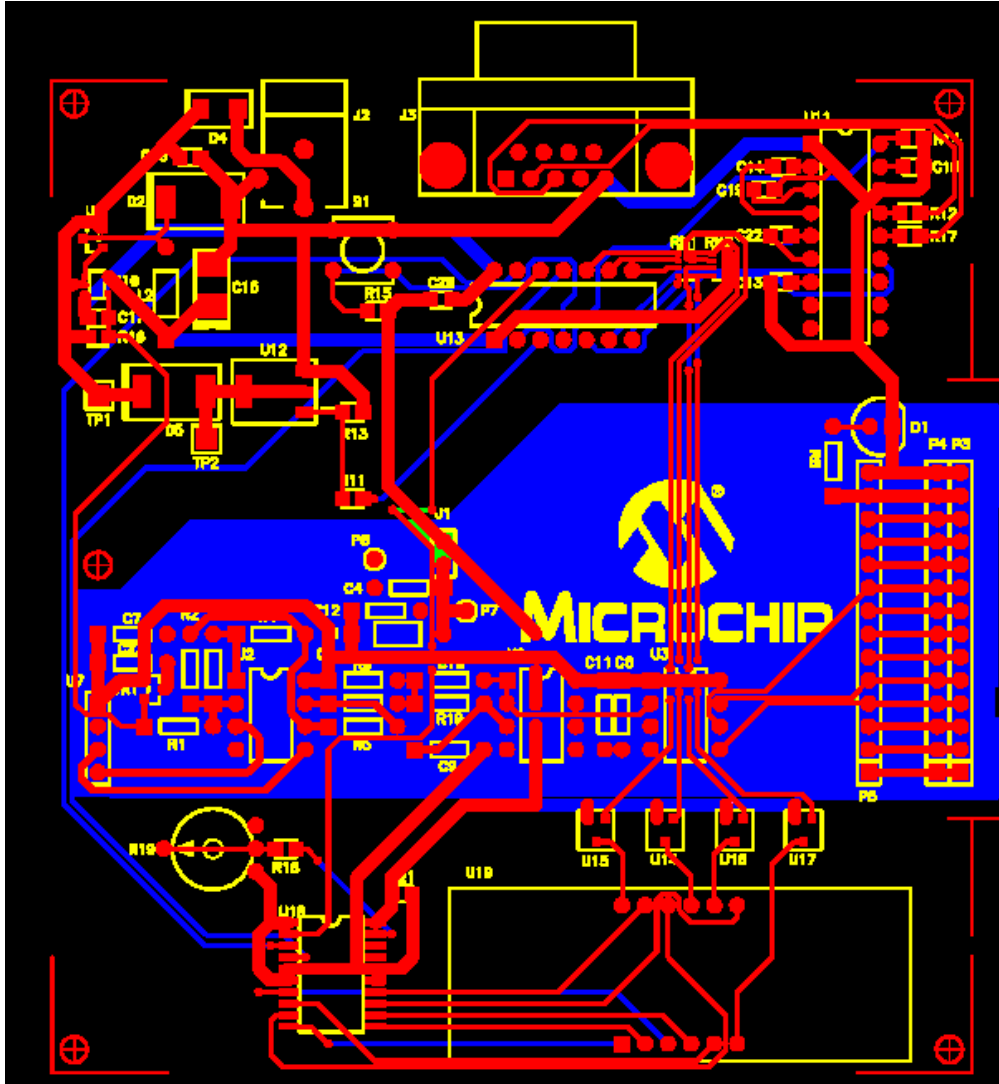
- Layout the board using the plan
  - Isolation each section
  - Plan routing of power and ground for each section
  - Isolate sensitive signals from fast- and high-current signals
  - Identify wide traces
  - Identify short and wide traces

# Application Board #5



# Complete Board Layout

Final Layout

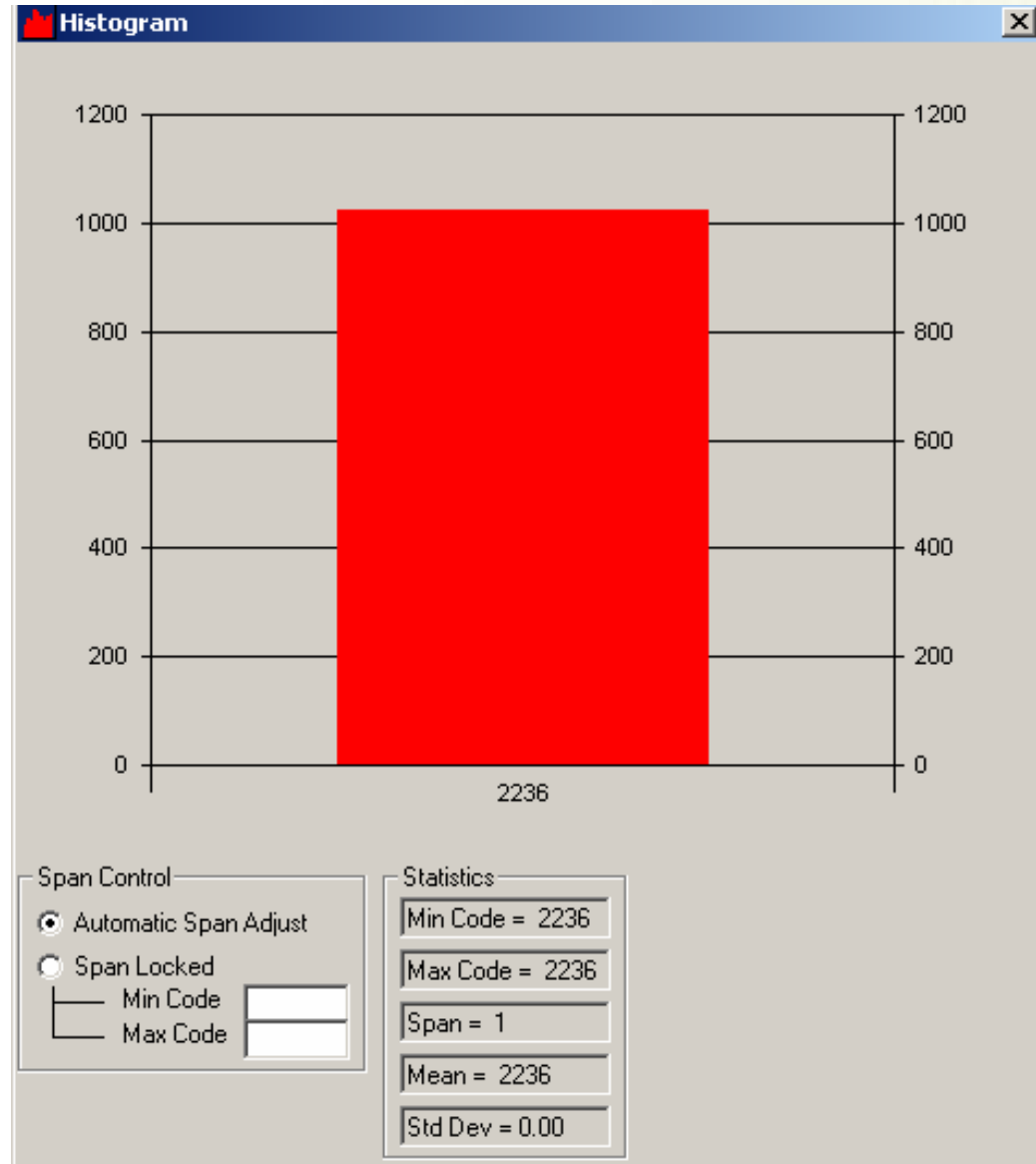




# New Composite Board Test Results

**Code Width  
of Noise = 1**

**(total samples = 1024)**





# System Solution: What You Should Do

- Use low-noise analog parts
- Use an uninterrupted analog ground plane
- Filter the ADC with an analog low-pass filter
- Bypass all devices properly
- Develop a power and ground plan for the whole circuit
- Use software to create quiet times for conversions
- Use separate analog and digital voltage regulators
- Isolate noisy sections





# References

- Reference Books
  - High-speed Digital Design: A Handbook of Black Magic, Howard Johnson and Martin Graham, Prentice Hall, 1993.
  - Noise Reduction Techniques in Electronic Systems, Henry Ott, John Wiley, N.Y., 1998.
  - The RF Capacitor Handbook, from American Technical Ceramics Inc.
  - The Circuit Designer's Companion ,by Tim Williams
  - Reference Data for Engineers, 7th edition  
Edward C. Jordan, Editor in chief
  - ABC's of Transformers & Coils,by Edward J. Bukstein



# Additional References

- Reference Application Notes
  - *ADN 007, Techniques that Reduce System Noise in ADC Circuits*
  - *AN681, Reading and Using Fast Fourier Transforms (FFTs)*
  - *AN699, Anti-Aliasing, Analog Filters for Data Acquisition Systems*
  - *AN695, Interfacing Pressure Sensors to Microchip's Analog Peripherals*
  - *AN688, Layout Tips for 12-Bit A/D Converter Application*
  - *AN823, Analog Design in a digital World using Mixed Signal Controllers*
- Web Addresses
  - <http://www.csee.umbc.edu/~plusquel/650/slides/crosstalk1.html>
- FilterLab<sup>®</sup> Active Filter Design Software
  - Down-loadable at [www.microchip.com](http://www.microchip.com)
  - Active, op amp filters