927 EFB

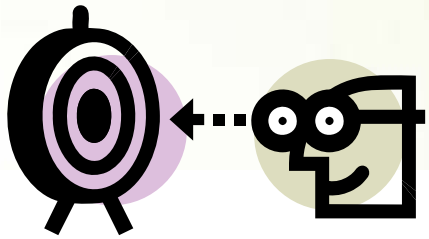
Designing PIC® Microcontroller Circuits for EFT/ESD Compatibility - II

What is EMC?

- EMC- Electromagnetic Compatibility
  - Capability of an electronic system to function compatibly with other electronic systems and not produce or be susceptible to interference
  - A system is electromagnetically compatible if:
    - It does not cause interference with other systems
    - It is not susceptible to emissions from other systems
    - It does not cause interference with itself

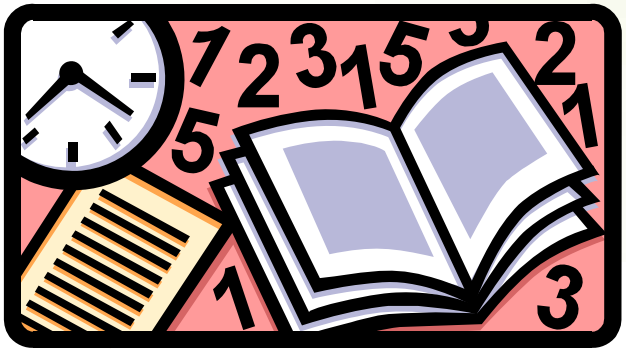
Objectives

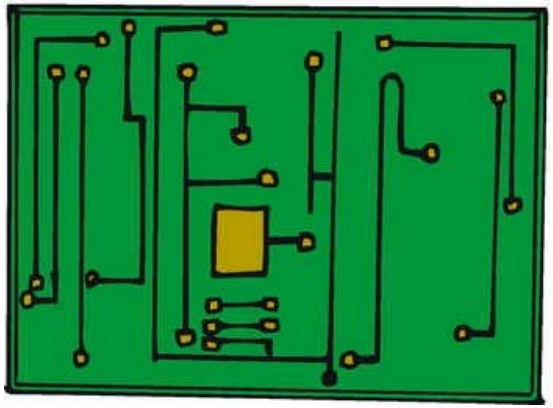
- Focus on EMC subgroups, Discuss PCB layout effect.
  - “It is not susceptible to emissions from other systems”
    - Electrical Fast Transients (EFT)
    - Electro Static Discharge (ESD)
  - “It does not cause interference with itself”
- Explain power and ground planning



Agenda

- PCB layout fundamentals
- Ground (/ Power) Planning
- Case Studies

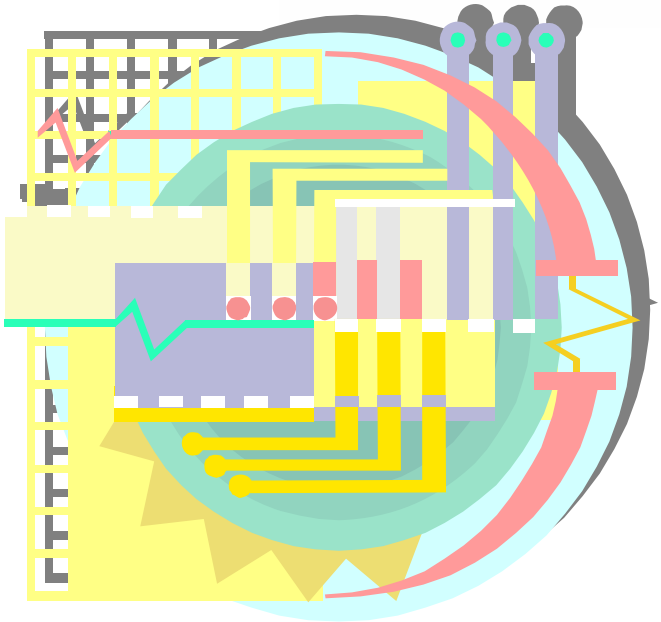




Microchip EMC resources

- EMC Newsletter
  - Available on Appliance and Automotive design center
- EMC Webinars

PCB Layout Fundamentals

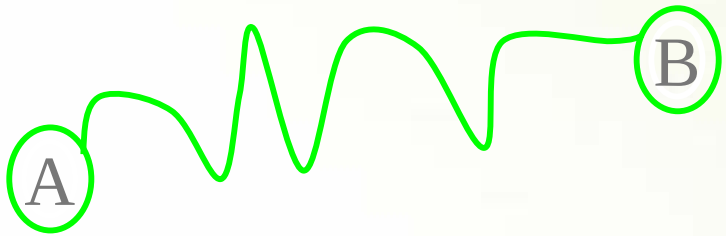


EMC Newsletter

Issue 2

PCB Layout

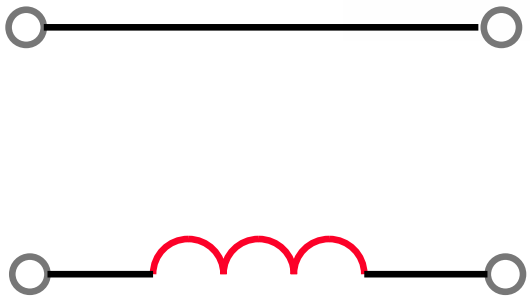
- Main Goal
  - Connect nodes



- For EMC performance
  - Minimize impedance in intended path
  - Maximize impedance in unintended path

PCB Layout
Trace

- Trace
  - Low frequency = wire,
  - High frequency = Inductor



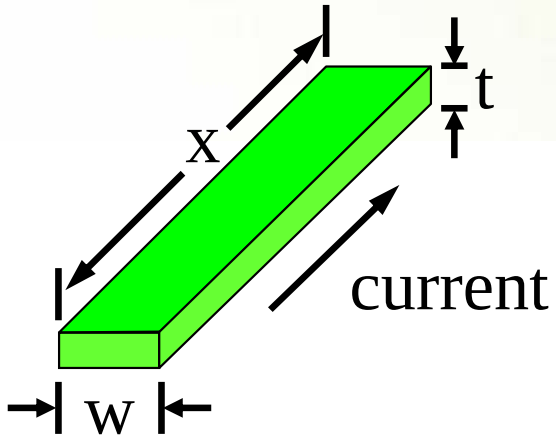
PCB Layout
Trace Resistance

- Trace resistance is based on:
  - Trace length (x)
  - Trace thickness (t)
  - Trace width (w)

ρ = Resistivity
≈ 680 (nΩ-in), Cu (copper)

$t \approx 0.00137$ in/oz, Cu

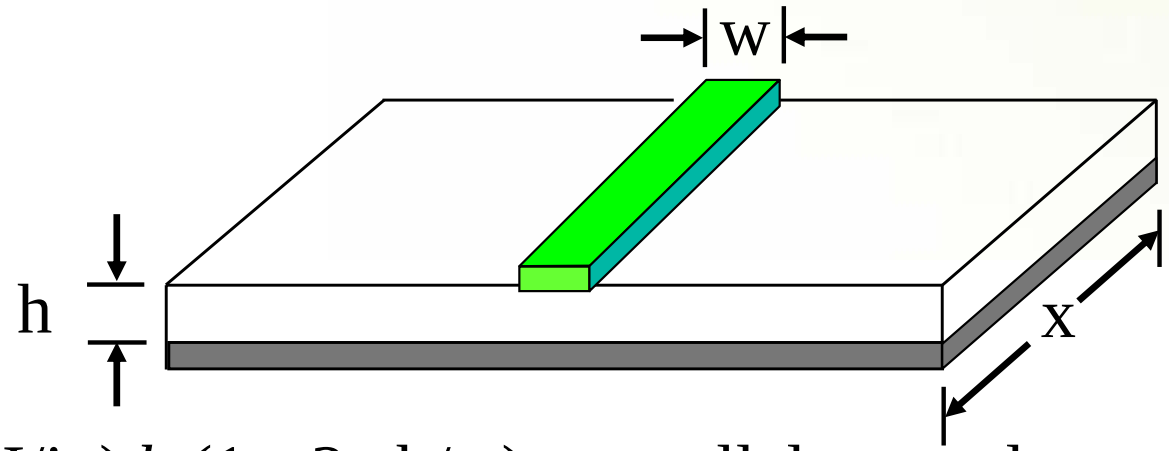
$R \approx \frac{x}{w} \cdot (0.50\ m\Omega/\ \ \ )$, 1 oz Cu



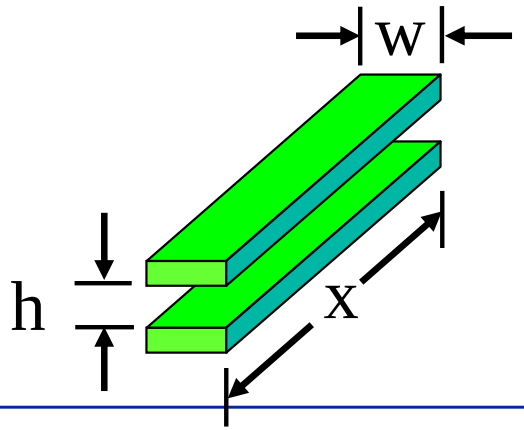
PCB Layout
Trace Inductance

- For PCB traces

$$L \approx x\,(5\ \text{nH/in})\ ln(1 + 2\pi\, h/w), \quad \text{with ground plane}$$

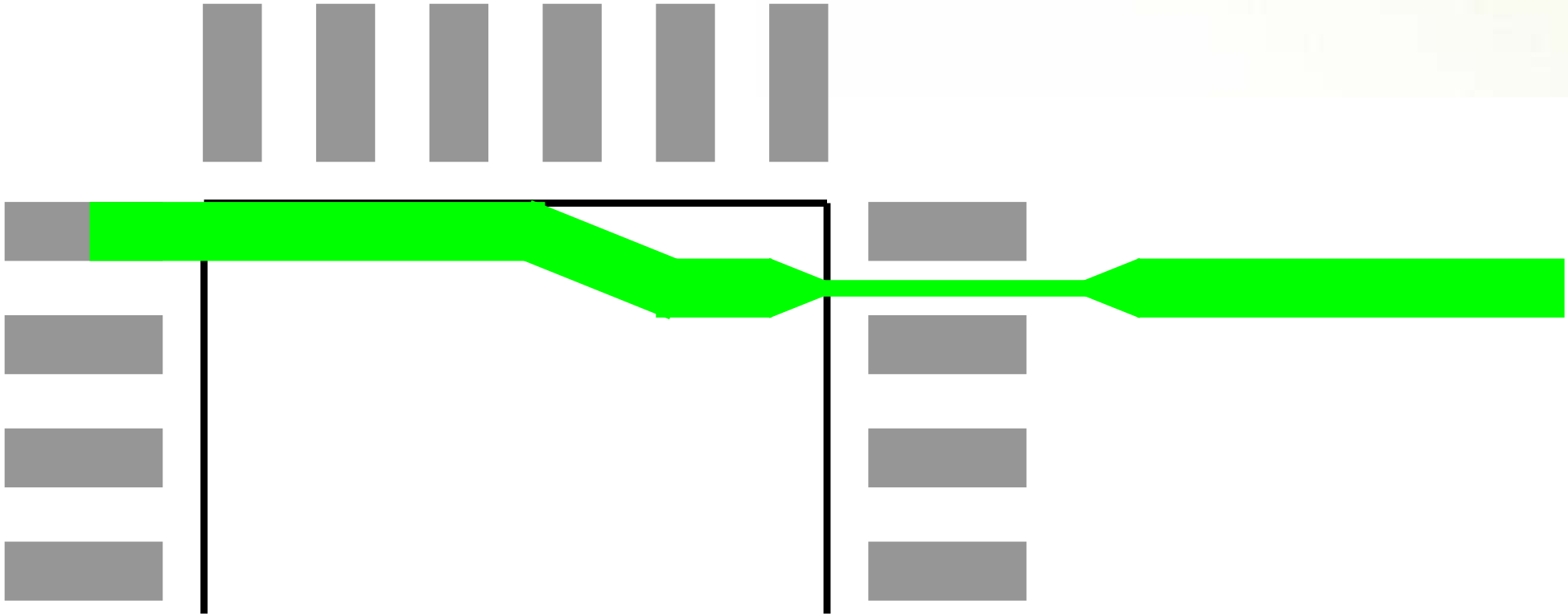


$$L \approx x\,(10\ \text{nH/in})\ ln(1 + 2\pi\, h/w), \quad \text{parallel ground return trace}$$



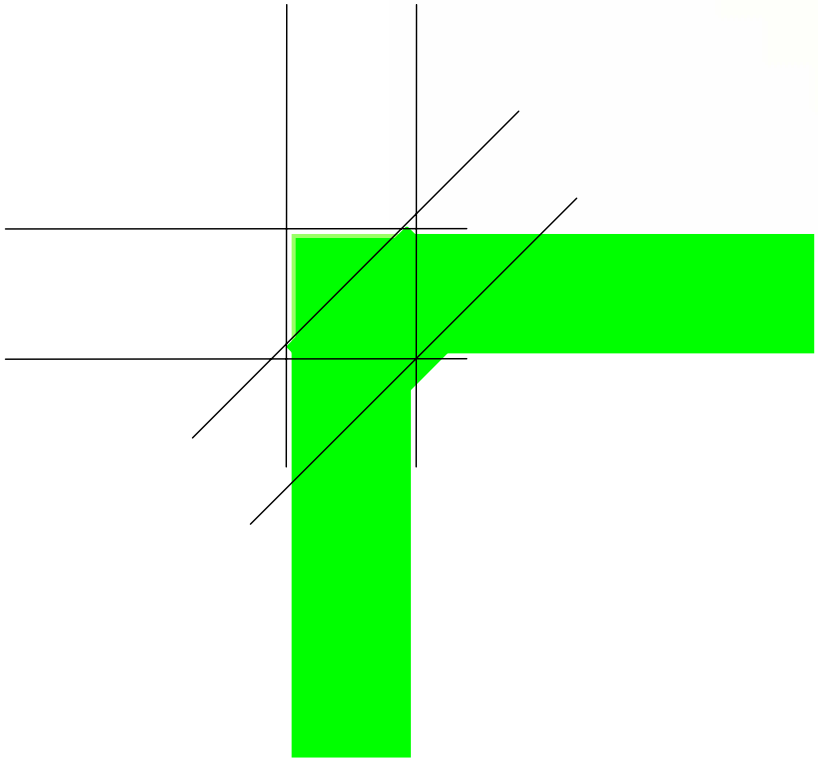
PCB Layout
Trace

- Trace Width Variation?
  - Trace resistance $\propto \frac{1}{w}$
  - Trace inductance $\propto \frac{1}{w}$



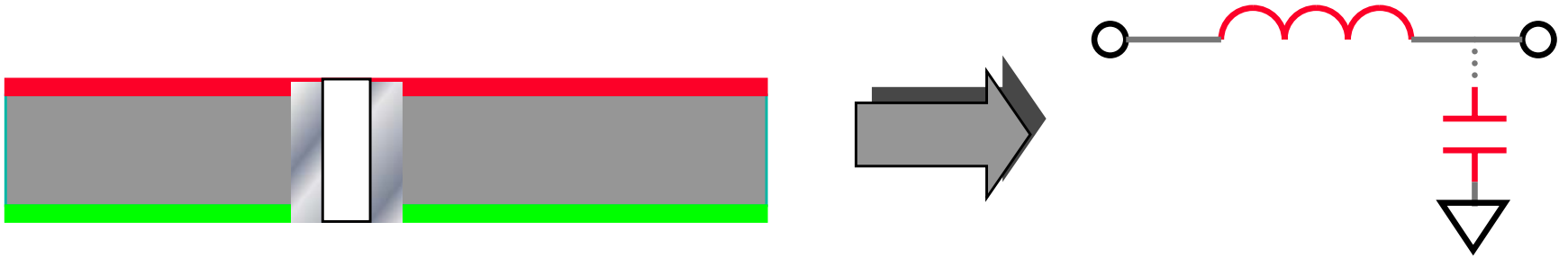
PCB Layout
Trace Corners

- Right angle corners



PCB Layout
Vias

- Vias
  - Each via introduces ~2nH & ~0.5pF
  - Causes impedance mismatches and signal delays



PCB Layout
Vias

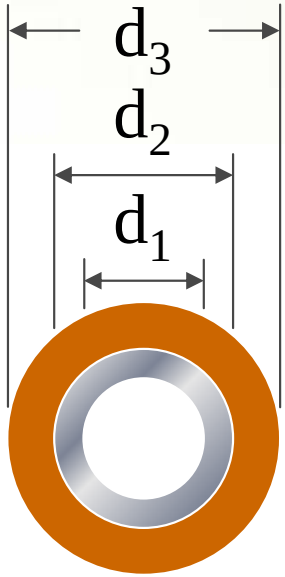
- Via impedances are quite important

d_1 = via diameter
d_2 = via pad diameter
d_3 = ground clearance hole diameter
h = height of via (e.g., board thickness)

$$R \approx \frac{h\,(870\ n\Omega\text{-in})}{d_1^{\,2}}$$

$$C \approx \frac{h\,d_2\,\varepsilon_r\,(1.4\ pF/in)}{d_3 - d_2}$$

$$L \approx h\,(5\ nH/in)\,ln(1 + 4\,h/d_1)$$

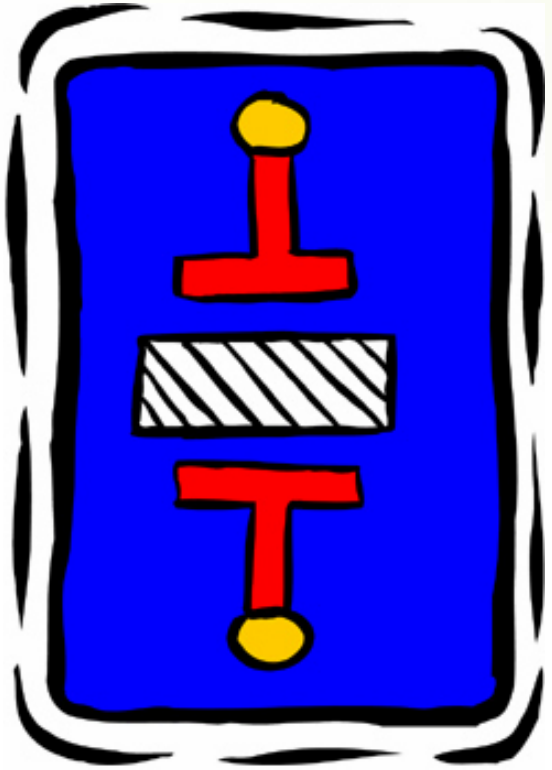


PCB Layout Fundamentals

- PCB Capacitor
  - Two conductors separated by dielectric
  - Low inductance capacitor

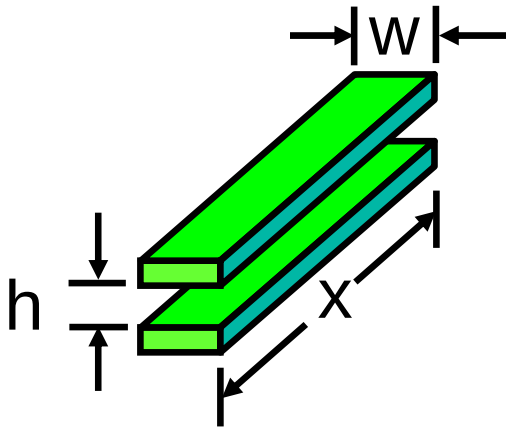
PCB Layout
Trace Capacitance

- Capacitance
  - Is caused by an electric field between two conductors
  - Depends on
    - Geometry
    - Separation
    - Dielectric (εr)

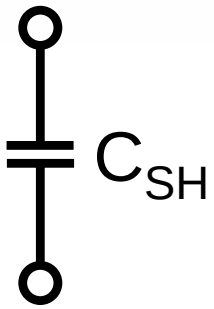


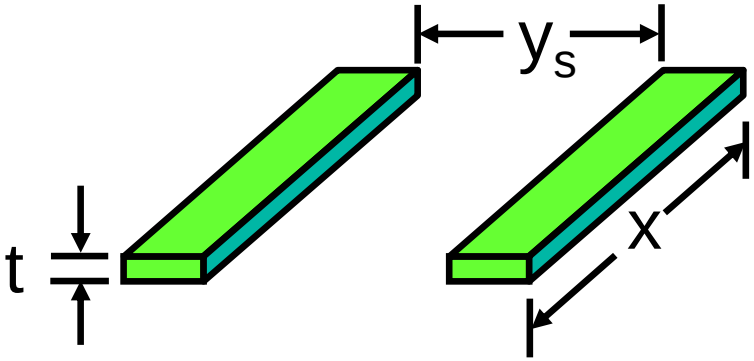
PCB Layout
Trace Capacitance

- Without ground plane



$$C_{SH} \approx \frac{x\,\varepsilon_r\,(0.71\ \text{pF/in})}{ln(1+\pi\,h/w)}, \quad x >> w,h$$

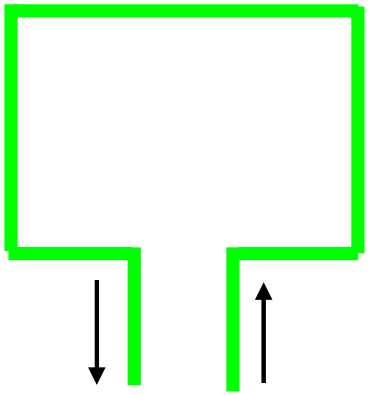




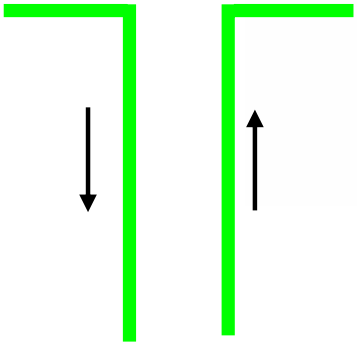
$$C_M \approx \frac{x\,\varepsilon_r\,(0.71\ \text{pF/in})}{ln(1+\pi\,y_s/t)}, \quad x >> t,y_s$$

PCB Layout Fundamentals

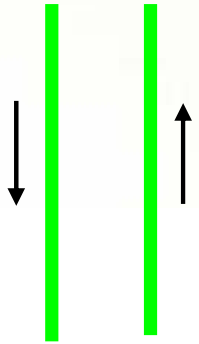
- Watch out for these antennas



Loop antenna



Dipole antenna



Transmission line

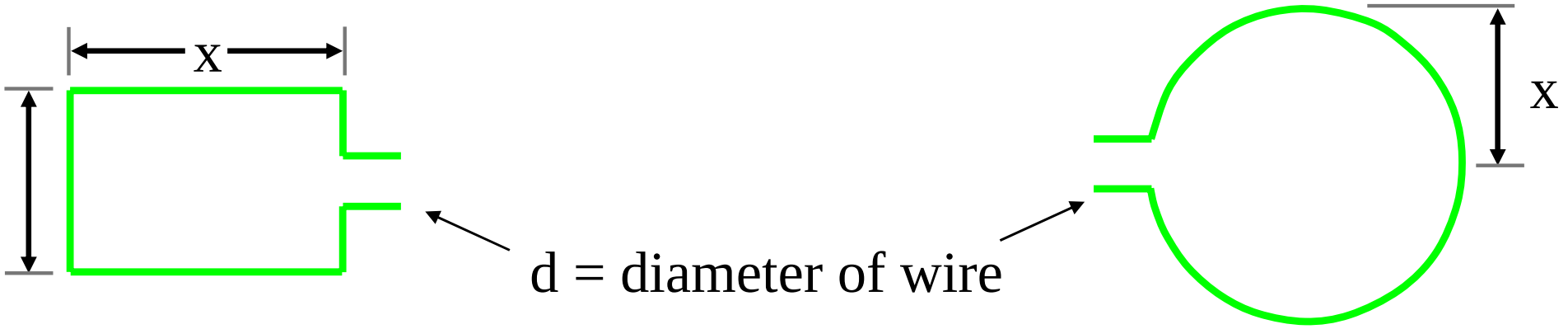
Radiation depends on A, L, I & *f*

PCB Layout
Loop Inductance

- Inductance Is Based on Magnetic Flux
  - Loop Area
  - Geometry

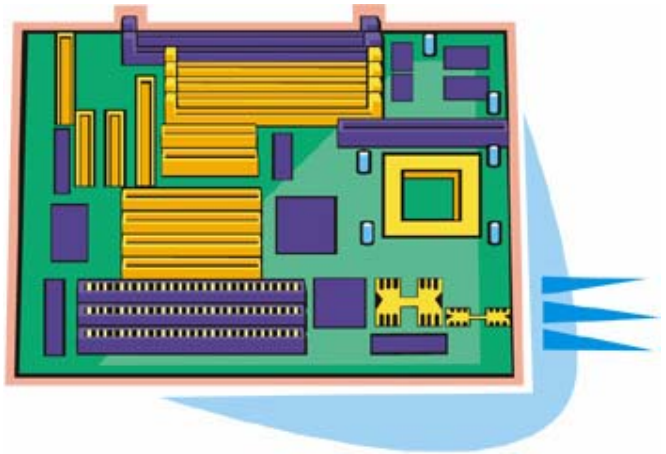
$$L \approx (5\,\text{nH/in})\,(2\,x\,ln(2\,y/d) + 2\,y\,ln(2\,x/d)\,), \quad \text{single rectangular loop}$$

$$L \approx 2\pi\,x\,(5\,\text{nH/in})\,(ln(16\,x/d) - 2), \quad \text{single circular loop}$$



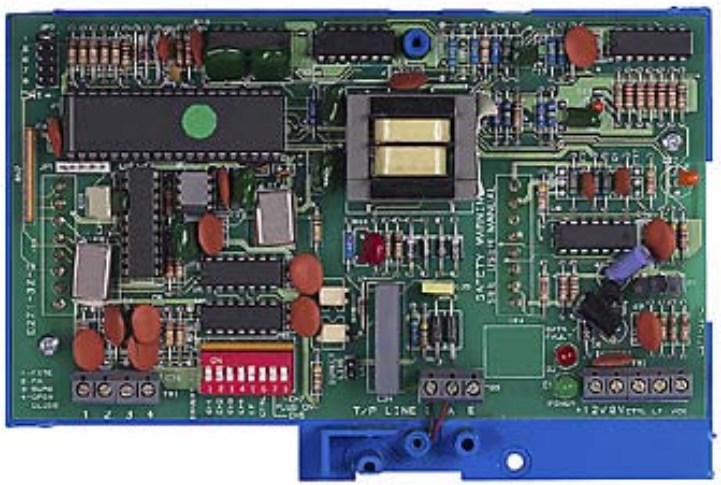
Multi Layer Boards

- Use Multi-layer boards
  - Dedicated surface (s) to power and ground
  - Minimizes loop areas
  - Minimizes signal return path
  - Minimizes cross talk
  - May provide 10x to 1000x improvement



Two Layer Board

- Two layer board can achieve 95% effectiveness of Multi layer board
  - Route GND/ VDD traces carefully
  - Ground plane in selective area
  - Routing of critical signals
    - Return path for critical signals
- May provide optimum Cost to Performance ratio

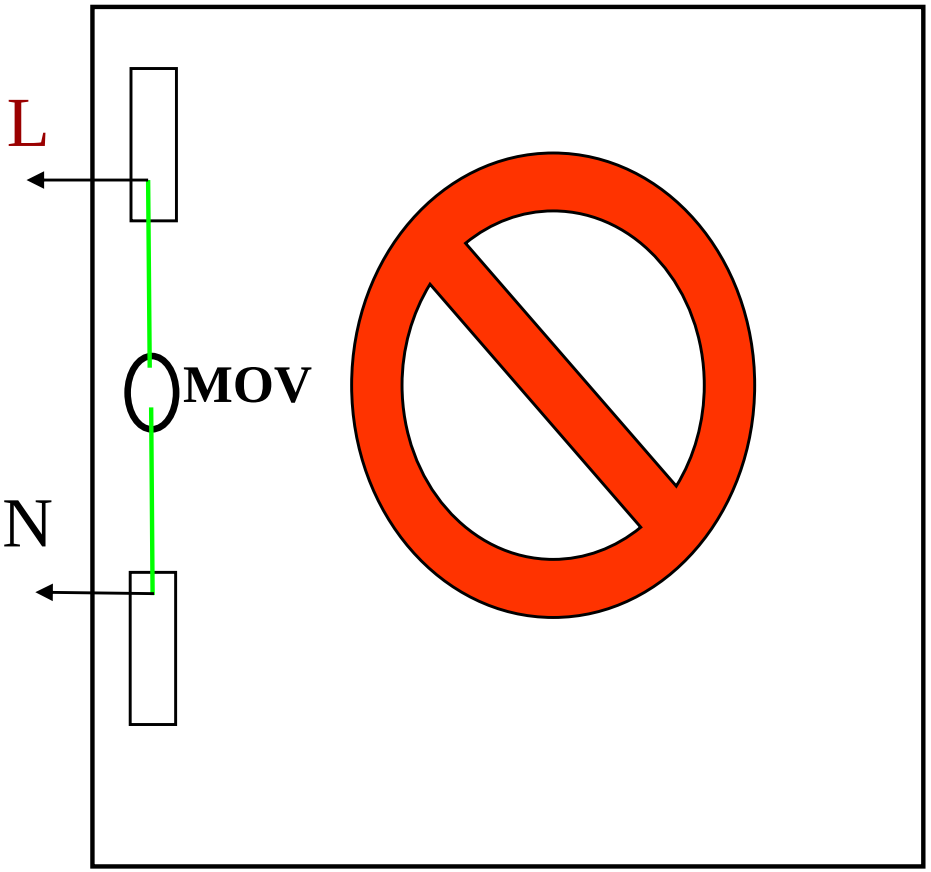


Board Design Approach

- Identify the power/ ground sources and critical signals
- Partition layout into functional blocks
- Position all components with critical signal adjacent to each other
- Route power and ground traces
- Route critical signals and their return paths
- Route rest of the board

Example usage of PCB building blocks

- Power entry & MOV (TS) location



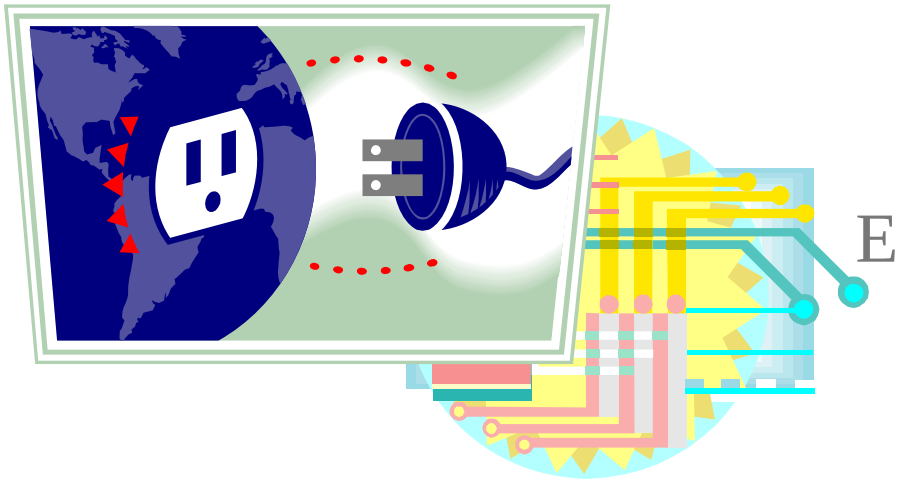
POOR

GOOD

BETTER

Tips & Tricks

Power, Ground & PCB Layout



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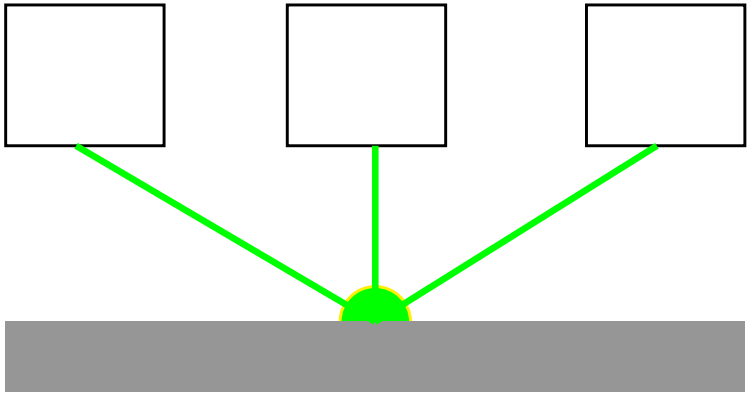
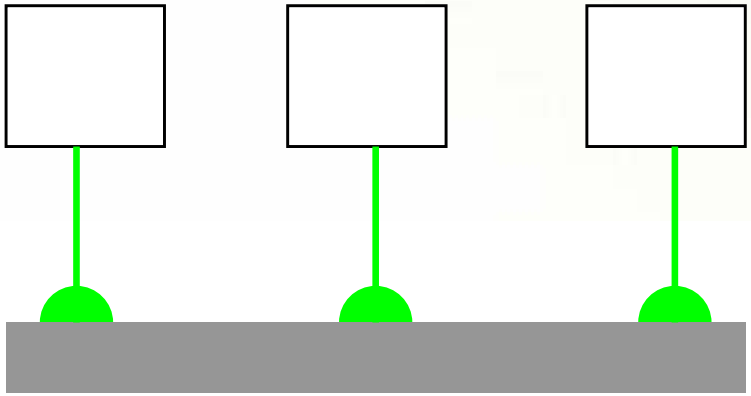
Issue 3

PCB Layout Grounding

- Two most used grounding techniques
  - Single Point
  - Multi Point





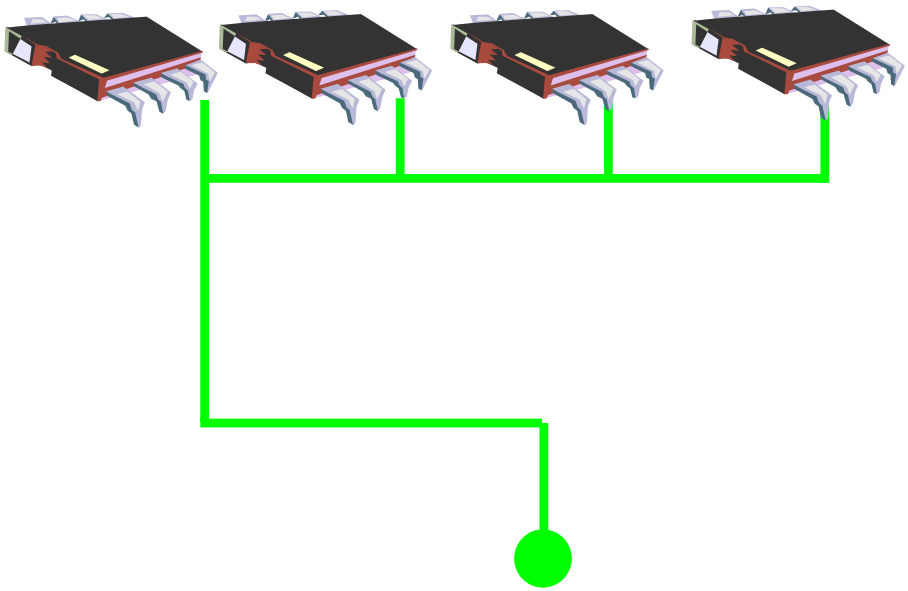
- **Preferred for low frequency**
- **No ground loops**

- **Preferred for high frequency**
- **Lesser parasitic inductance & capacitance**

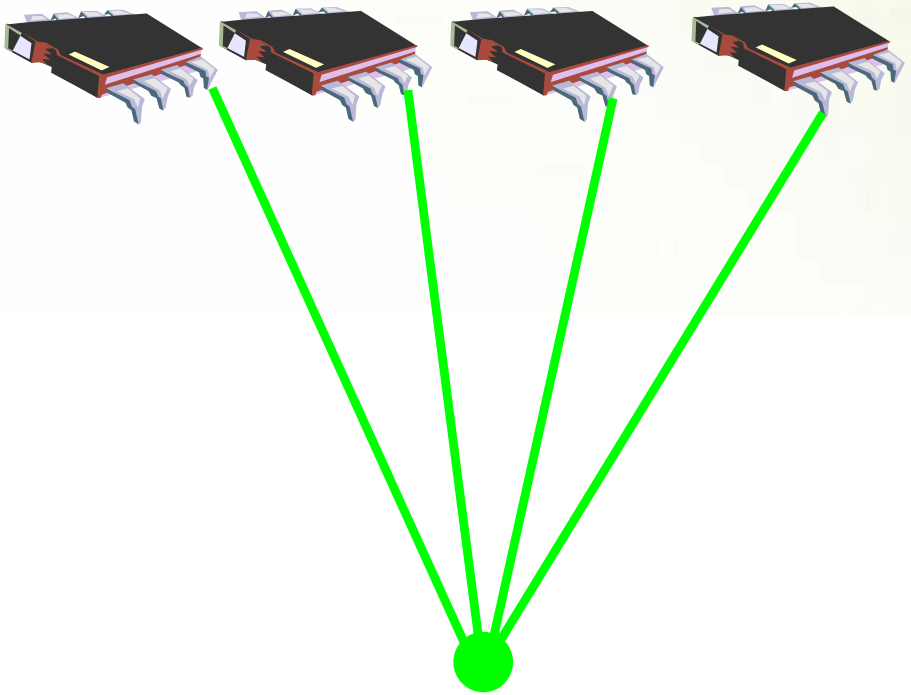
PCB Layout - Hybrid Grounding

- Hybrid Ground
  - Single point ground for analog system
  - Multi-point ground / grid for digital system
  - Capacitor for high frequency only ground
  - Inductor for low frequency only ground

PCB Layout
Power lines



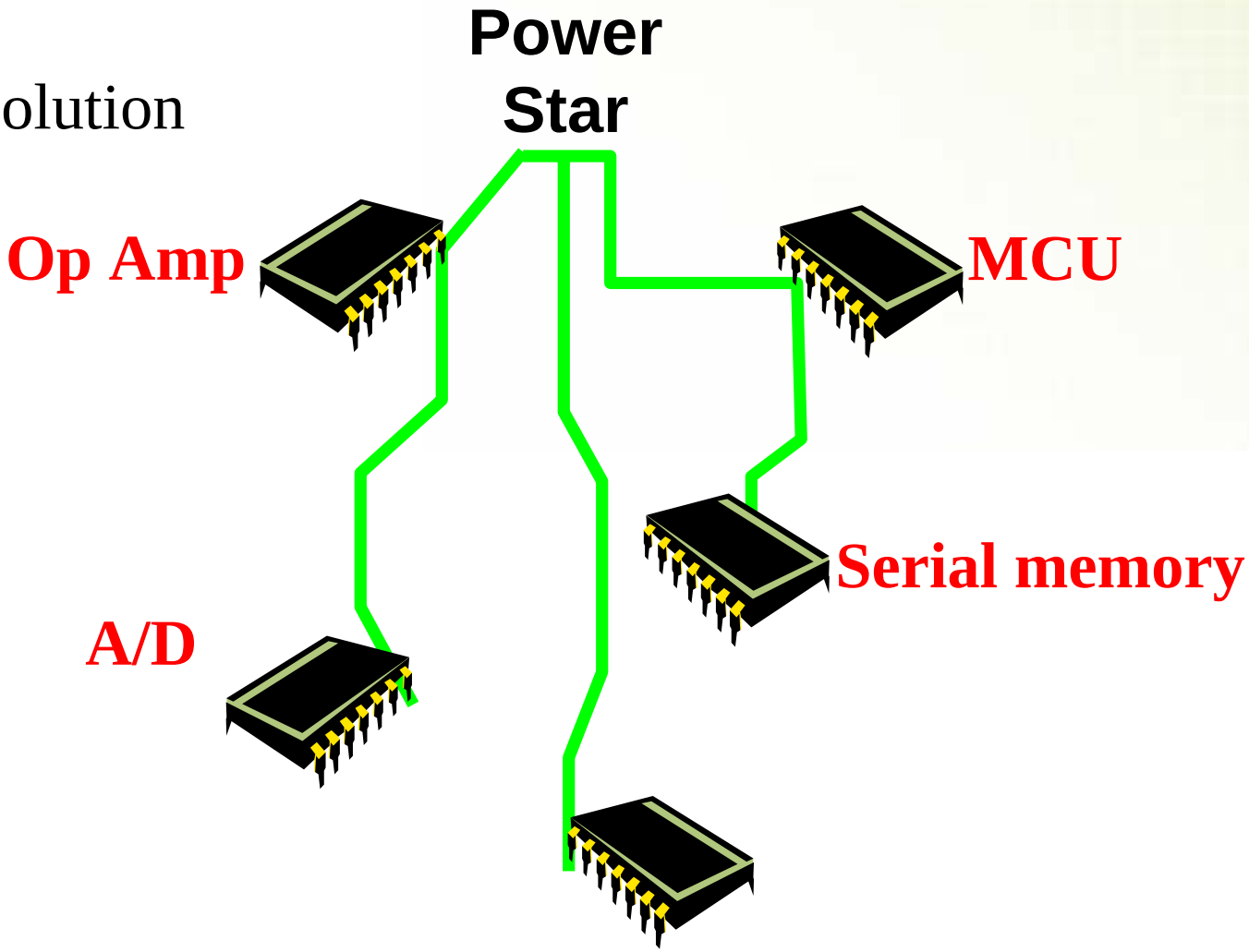
Poor- Daisy Chain



Best- Single Point

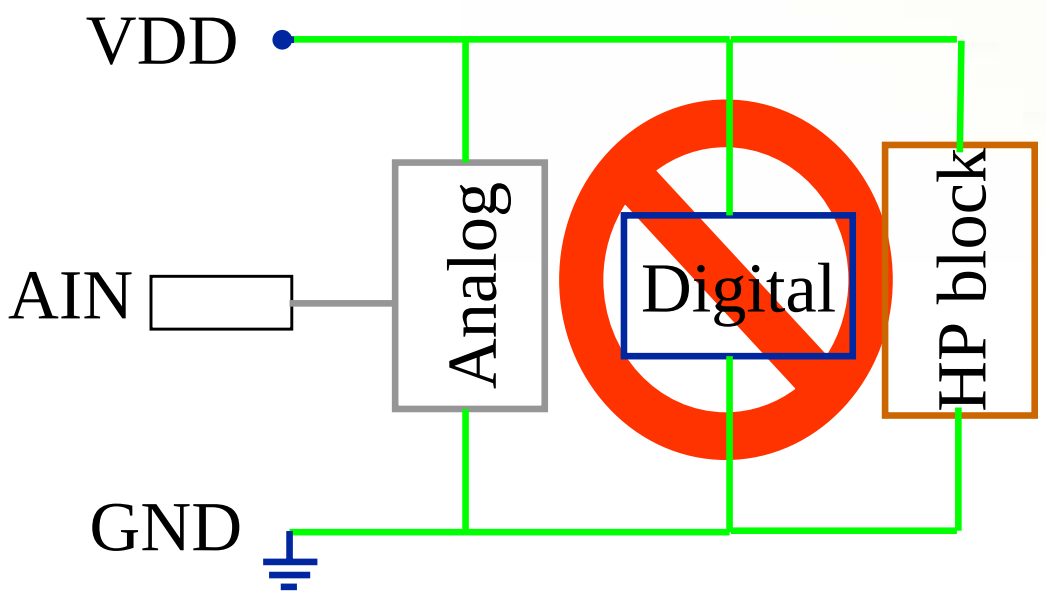
PCB Layout
Power Lines

Better, Practical Solution



PCB Layout - Grounding

- Typical Approach



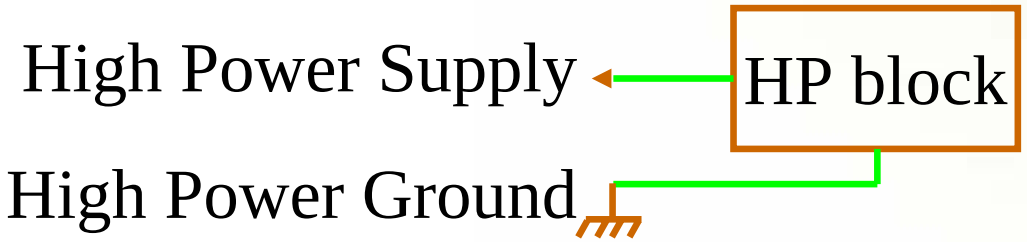
Ground Planning

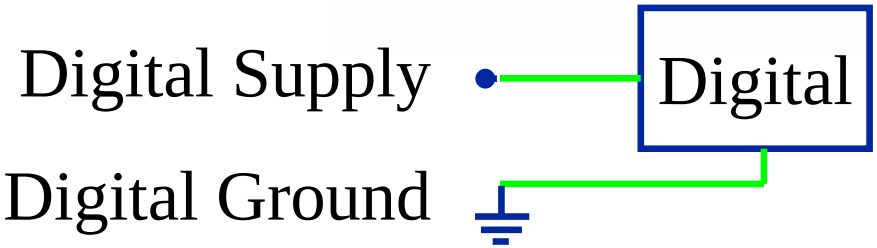
- Identify ground type requirements

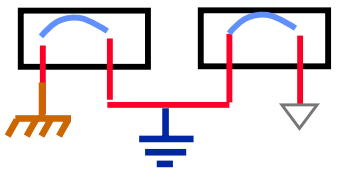
Microcontroller Med-Low noise, Sensitive	Analog Low noise, Very Sensitive
Triac / Relay High noise Low Sensitivity	Seven segment display Med-High noise, Low Sensitivity

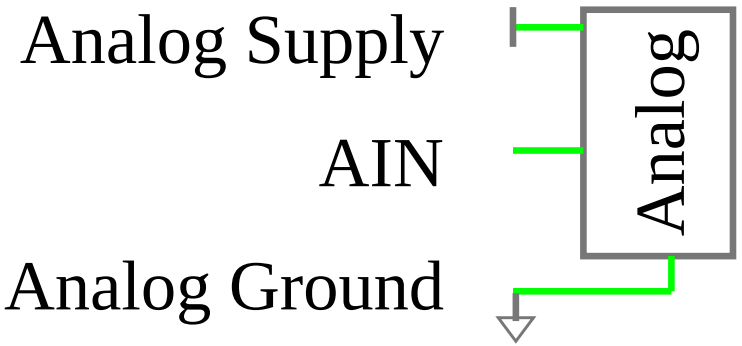
Ground Planning

- Suggested approach



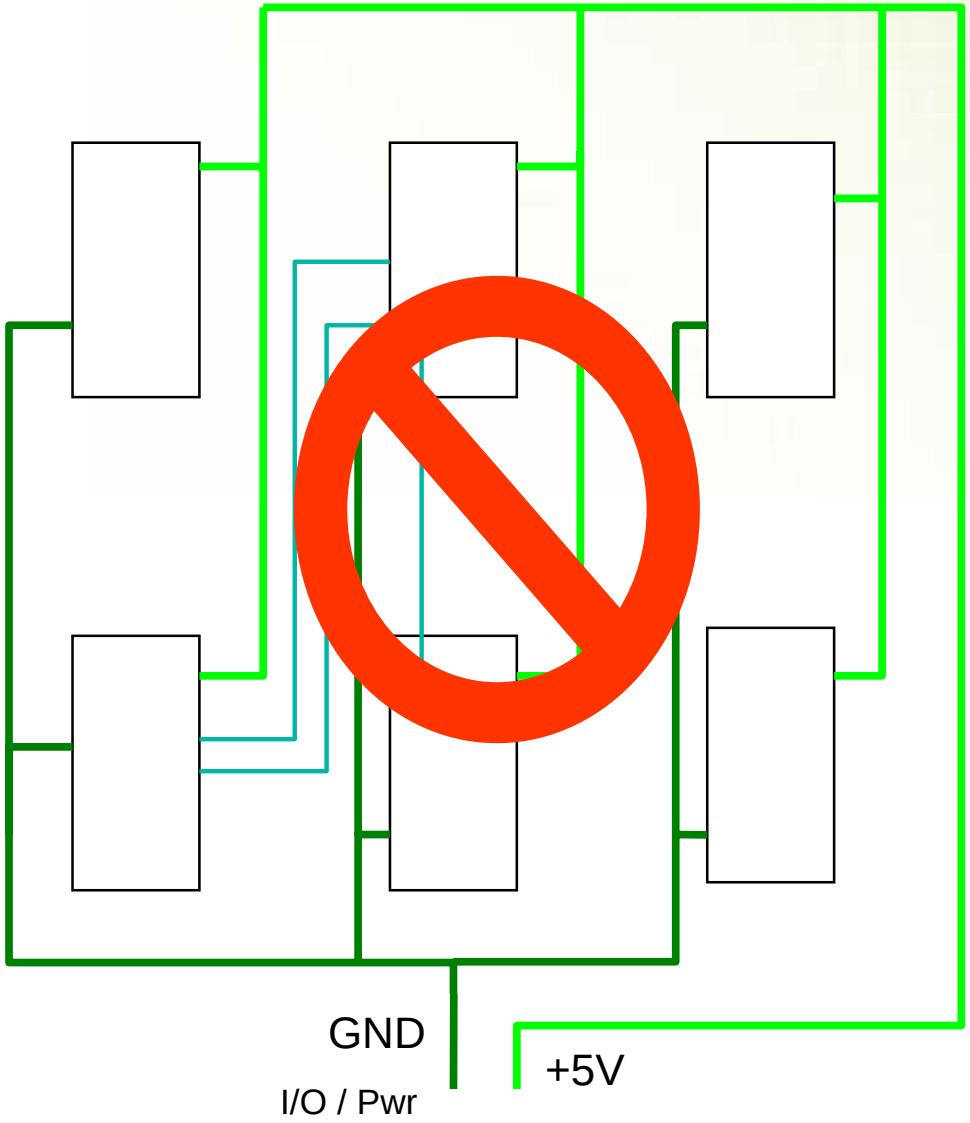




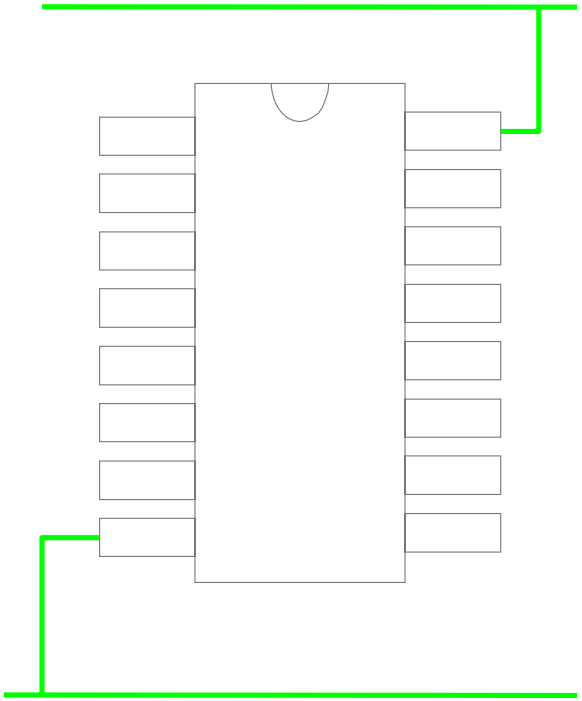


PCB Layout
Power Traces

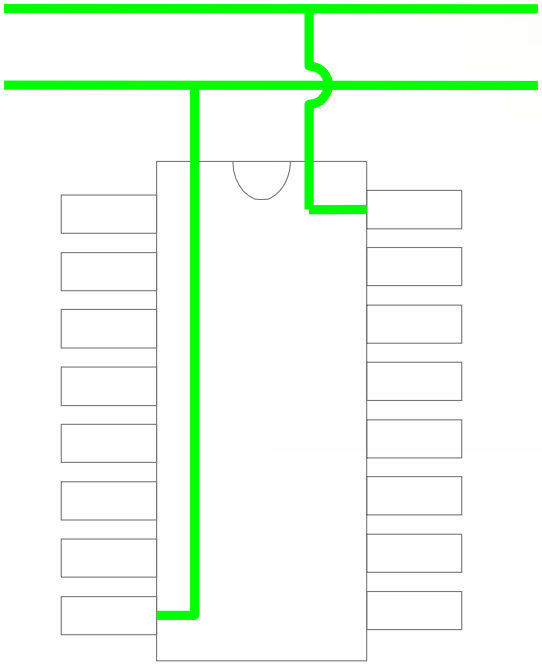
- Power Traces
  - Loop size
  - Verify return paths



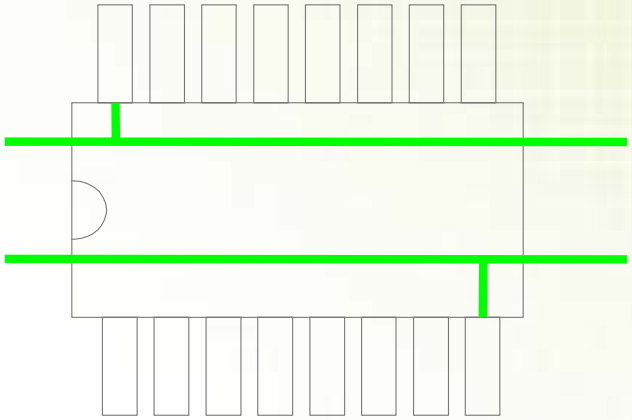
PCB Layout
Power Traces Layout



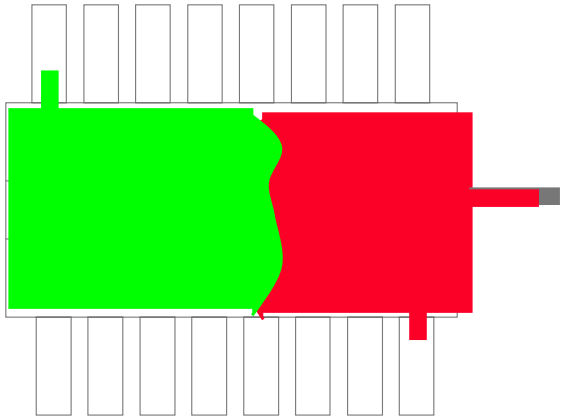
Poor



Good



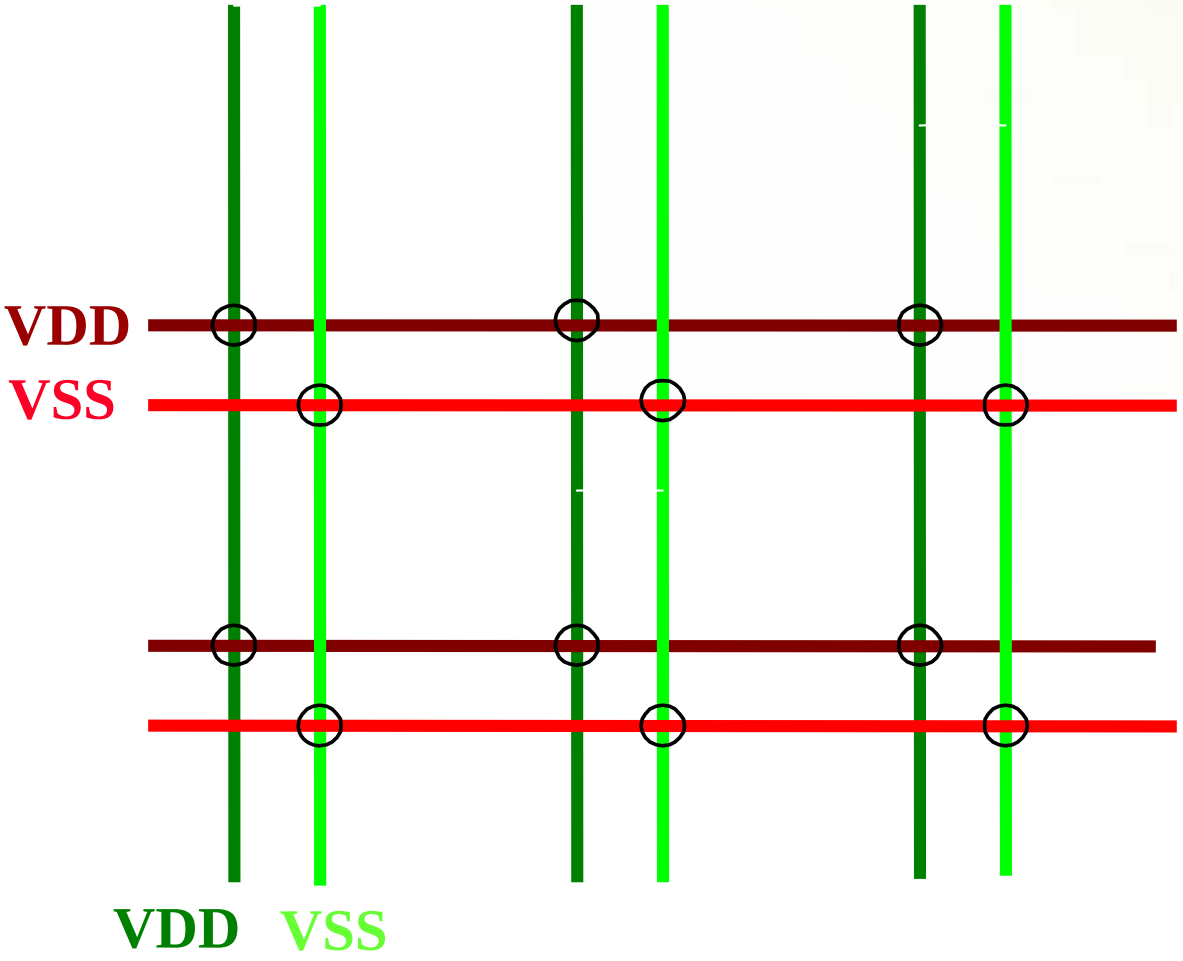
Better



Best

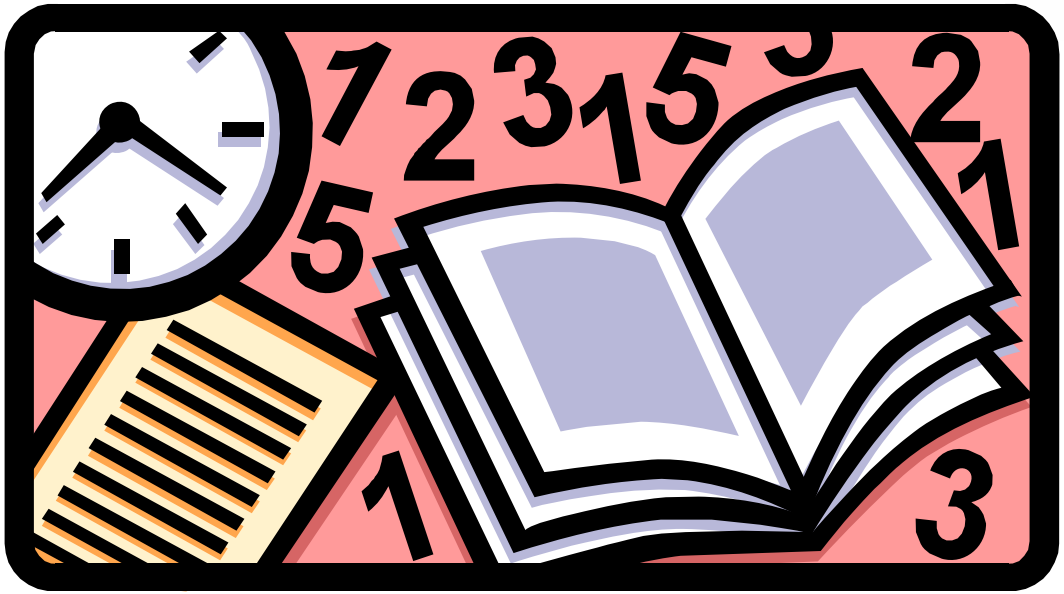
PCB Layout
Power Traces (Grid)

- Alternate (to Planes) routing example



MICROCHIP MASTERs

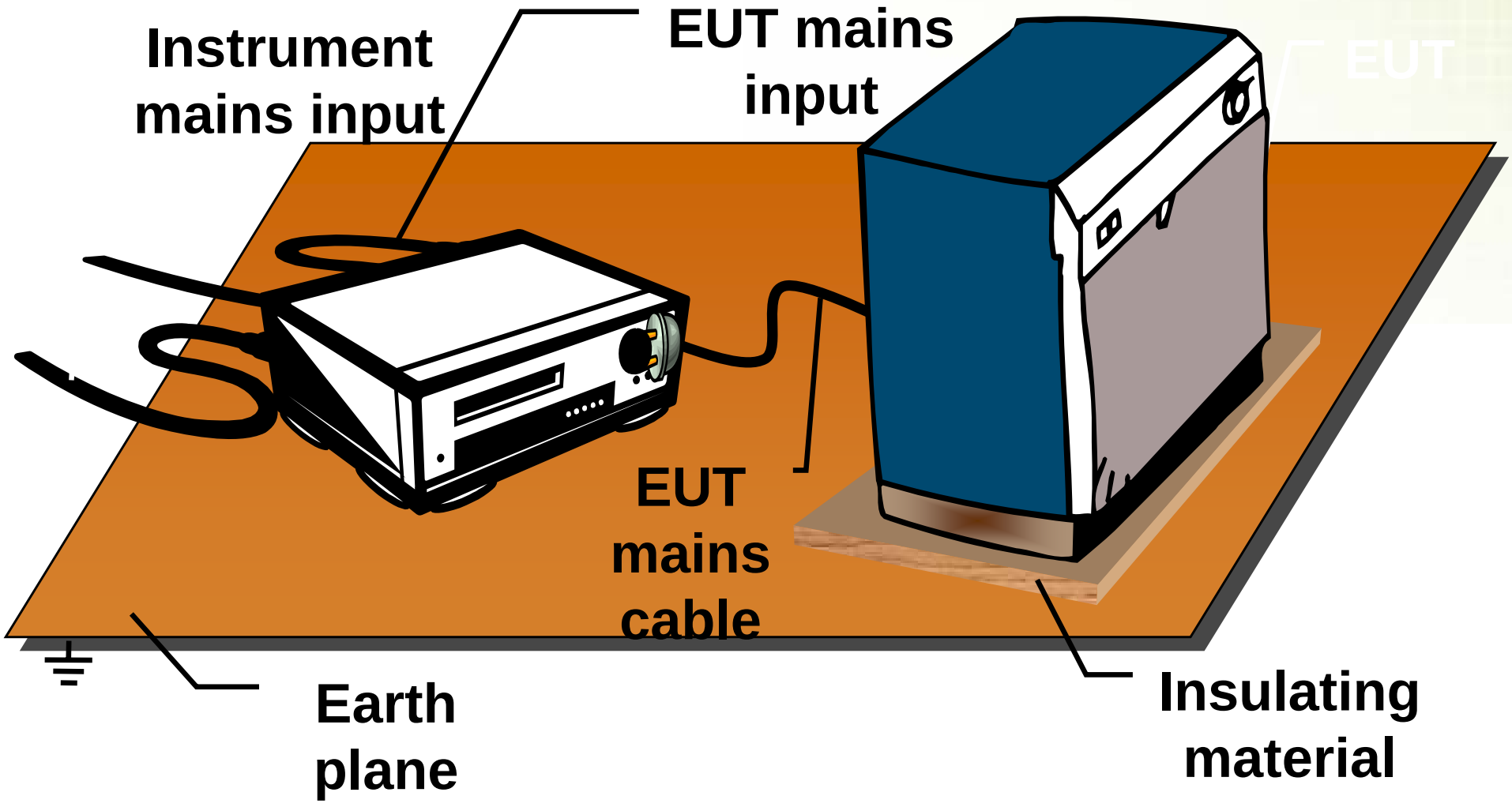
Case Study



Application

- Test Applications
  - Cost Sensitive Applications (Single layer Printed Circuit Boards (PCB))
  - Typical Application
    - Uses microcontroller and some digital glue logic
    - Uses some analog blocks
    - Does power control through Relays / Triacs
    - Uses transformerless power supply

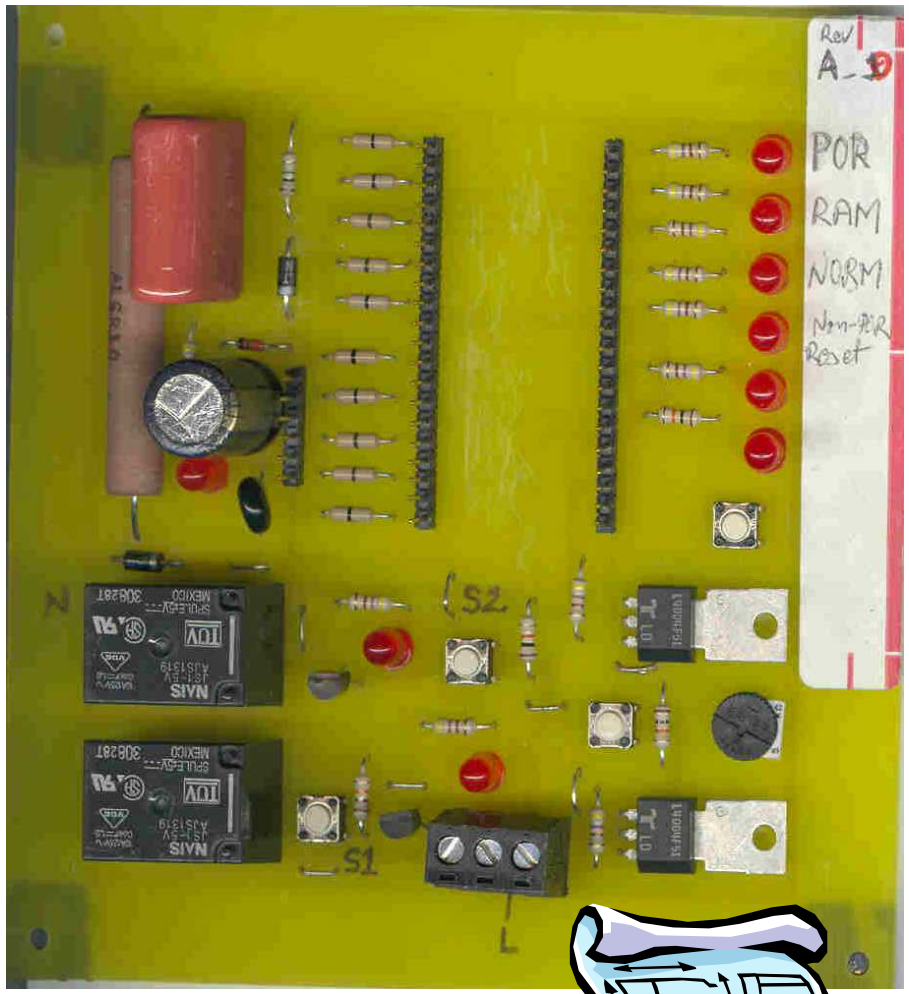
IEC 61000-4-4
Test set-up (Power Supply ports)

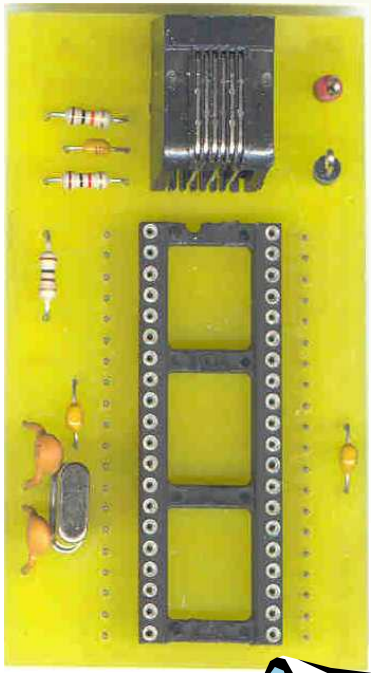


Case Study Data Analysis
Fail code

- (1) - POR reset
- (2) - RAM fail
- (3) - Non POR reset
- (4) - Misexecution
- (5) - Program memory corruption
- (6) - Data EE corruption
- NF - No Fail at 4400V (Max for test equipment)

Case #1

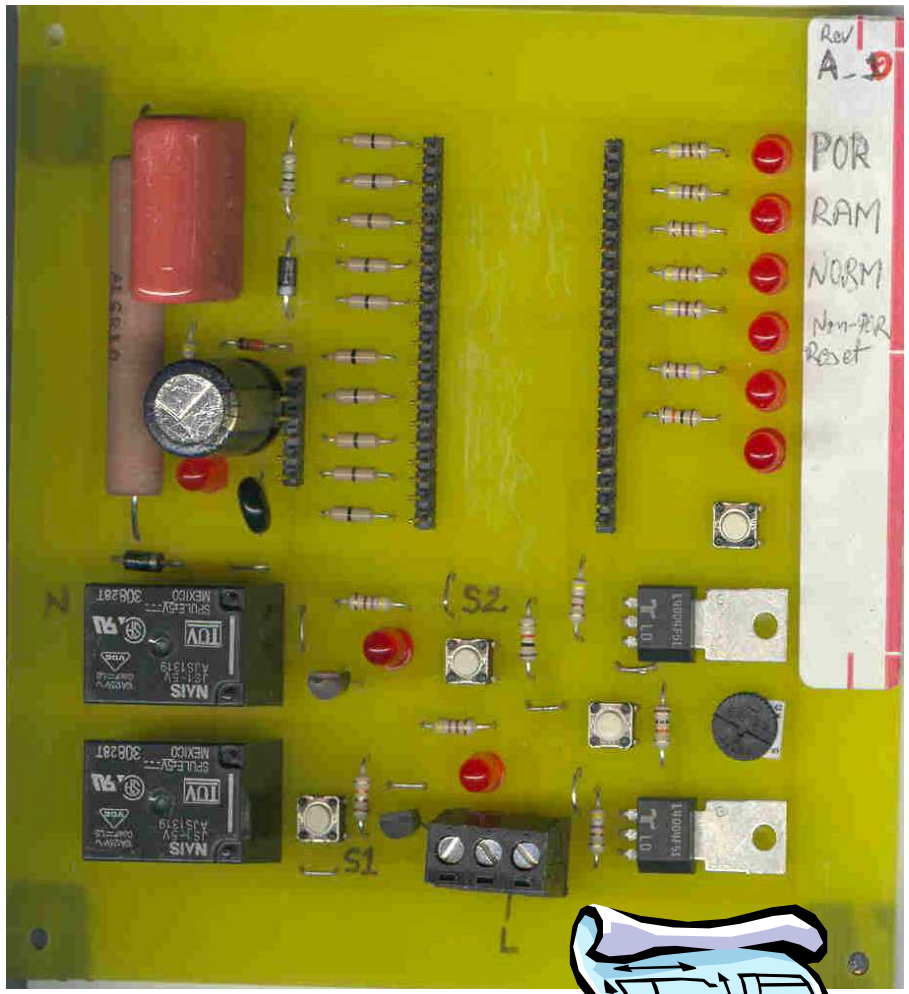


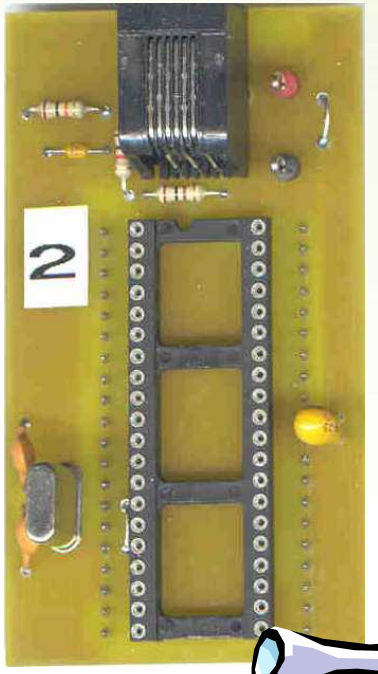


Case #1 Data

Coupling mode	Case #1 FailV
L+	650[2]
L-	900[2]
N+	800[2,3]
N-	450[2,3]
LN+	1400[2]
LN-	900[3]

Case #2





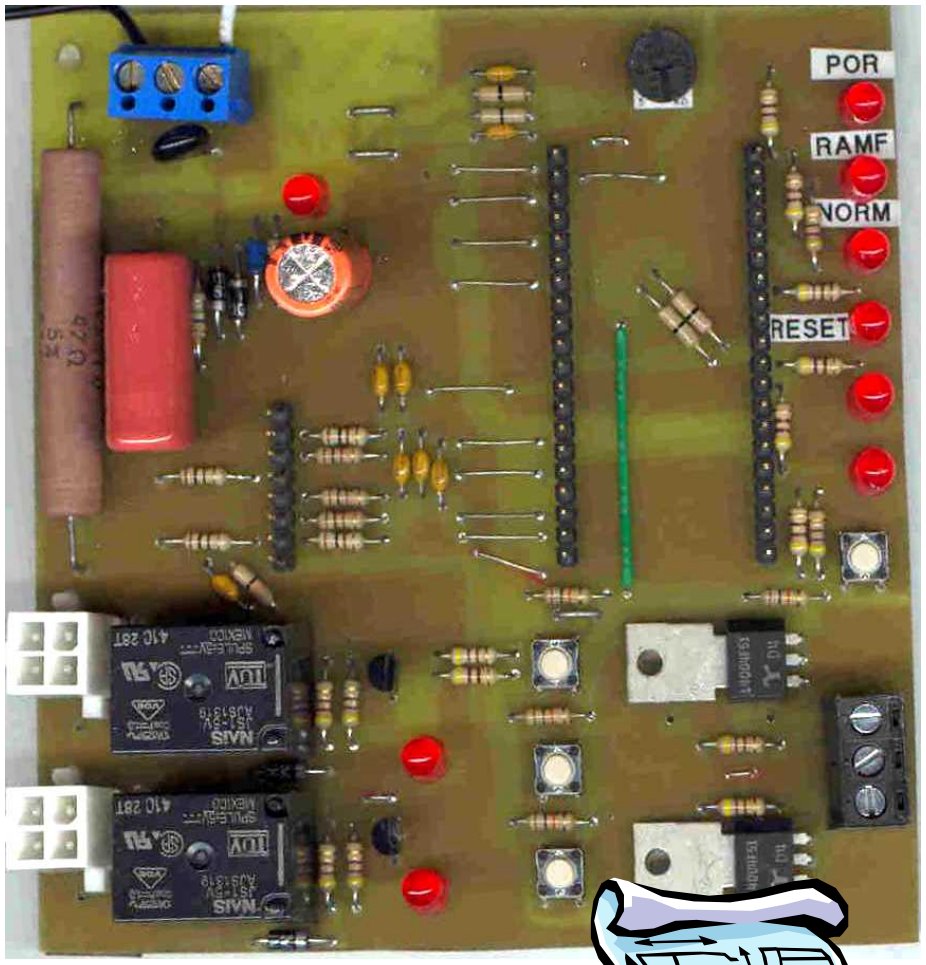
Case #2

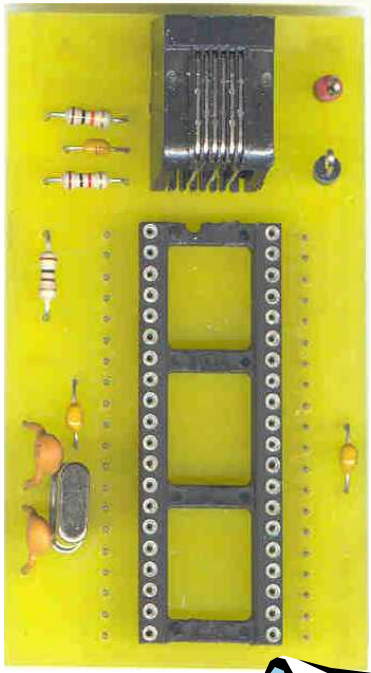
- Daughter board Rev 1 to Rev 2
  - Reset pin layout
  - Power and ground planning
  - PCB capacitor between power and ground
  - Optimized decoupling capacitor

Case #2 Data

Coupling mode	Case #1 FailV	Case #2 FailV
L+	650(2)	4200(3)
L-	900(2)	2100(3)
N+	800(2,3)	3000(2)
N-	450(2,3)	3700(3)
LN+	1400(2)	3100(2,3)
LN-	900(3)	1500(3)

Case #3





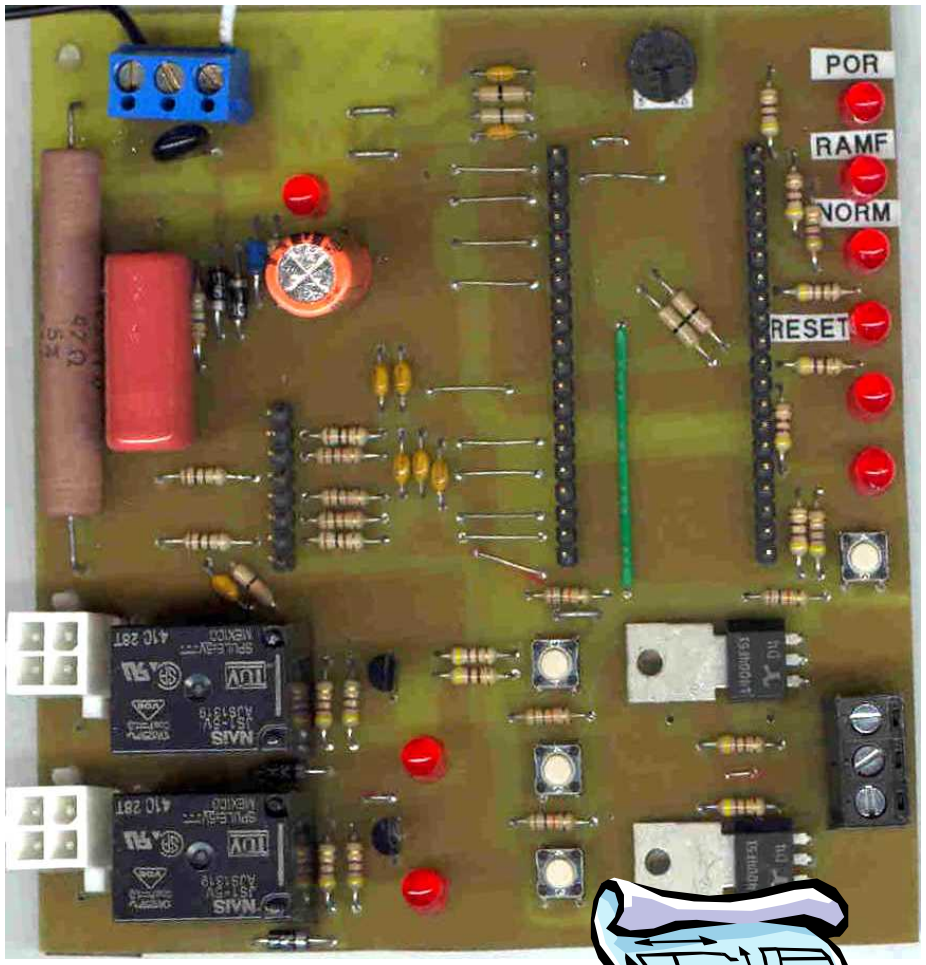
Case #3

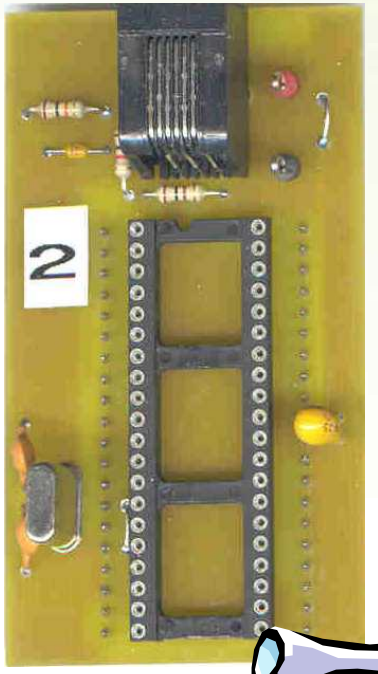
- Mother board Rev 1 to Rev 2
  - Transient suppressor layout and placement
  - Isolated power and ground (Digital, Analog and High power)
  - Power and ground planning
  - PCB capacitor between power and ground
  - Common mode choke (PCB component)
  - Ground ring around sensitive signals

Case #3 Data

Coupling mode	Case #1 FailV	Case #2 FailV	Case #3 FailV
L+	650(2)	4200(3)	2900(2)
L-	900(2)	2100(3)	1500(2)
N+	800(2,3)	3000(2)	1000(2)
N-	450(2,3)	3700(3)	3000(2)
LN+	1400(2)	3100(2,3)	NF
LN-	900(3)	1500(3)	1900(3)

Case #4 & #5





Case #4 Data

Coupling mode	Case #1 FailV	Case #2 FailV	Case #3 FailV	Case #4 FailV
L+	650(2)	4200(3)	2900(2)	NF
L-	900(2)	2100(3)	1500(2)	3400(1,3)
N+	800(2,3)	3000(2)	1000(2)	NF
N-	450(2,3)	3700(3)	3000(2)	NF
LN+	1400(2)	3100(2,3)	NF	NF
LN-	900(3)	1500(3)	1900(3)	2400(1, 3)

Case #5

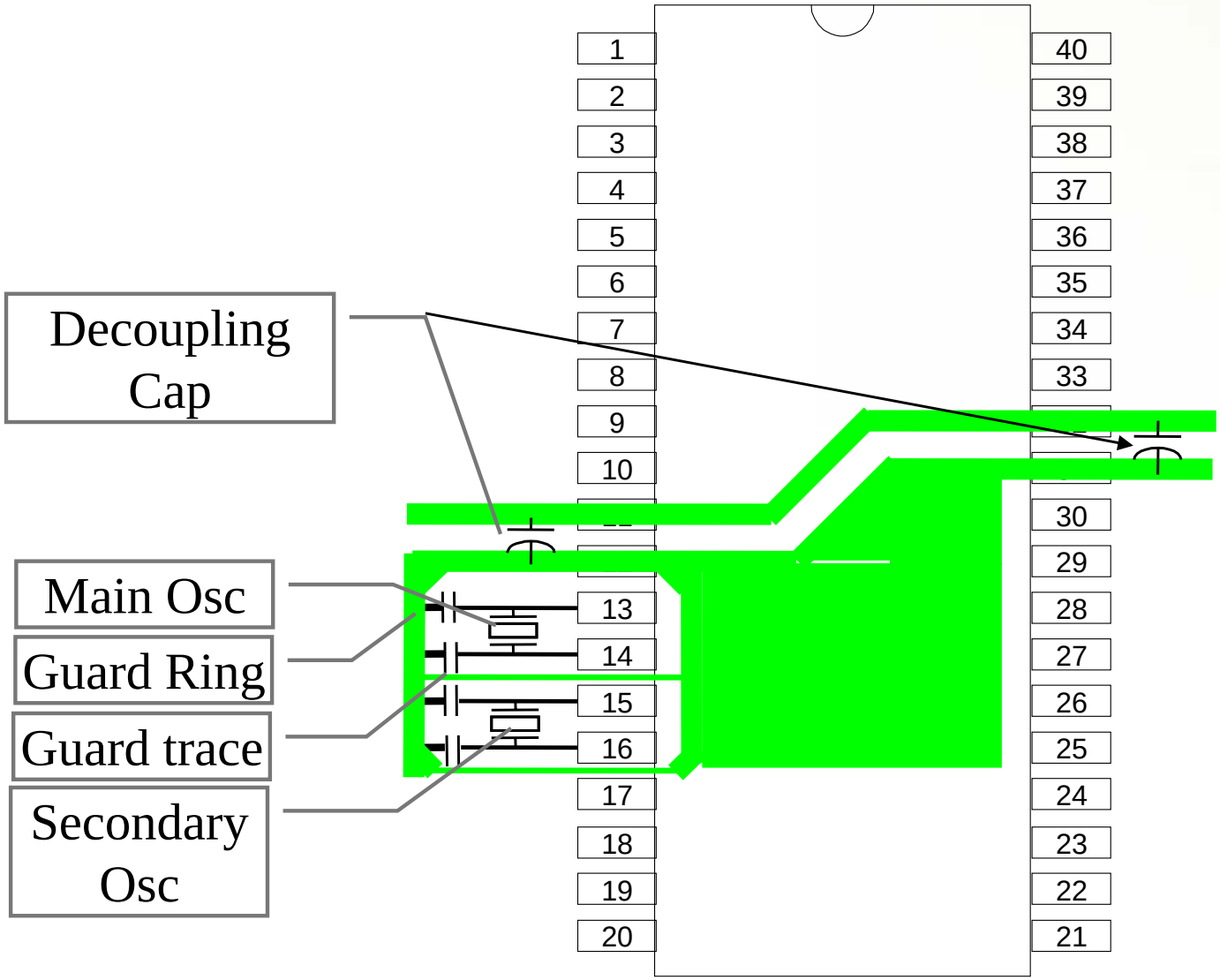
- Case #4 to Case #5 changes
  - Same HW setup as case #4 except
  - Different load on power supply (Relay off)

    Or
  - Modified power supply to support higher load

Case #4 & #5 Data

Coupling mode	Case #1 FailV	Case #2 FailV	Case #3 FailV	Case #4 FailV	Case #5 FailV
L+	650(2)	4200(3)	2900(2)	NF	NF
L-	900(2)	2100(3)	1500(2)	3400(1,3)	NF
N+	800(2,3)	3000(2)	1000(2)	NF	NF
N-	450(2,3)	3700(3)	3000(2)	NF	NF
LN+	1400(2)	3100(2,3)	NF	NF	NF
LN-	900(3)	1500(3)	1900(3)	2400(1, 3)	NF

Suggested Layout for PICmicro

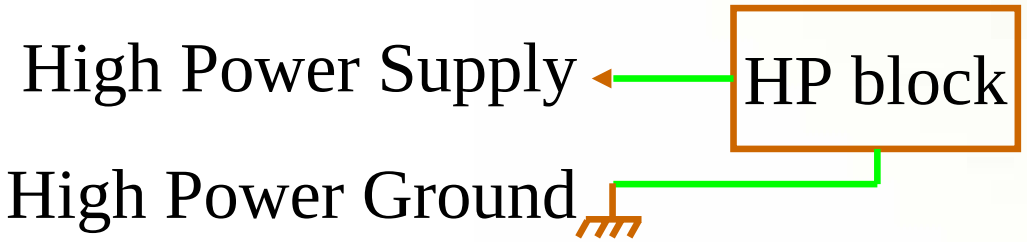


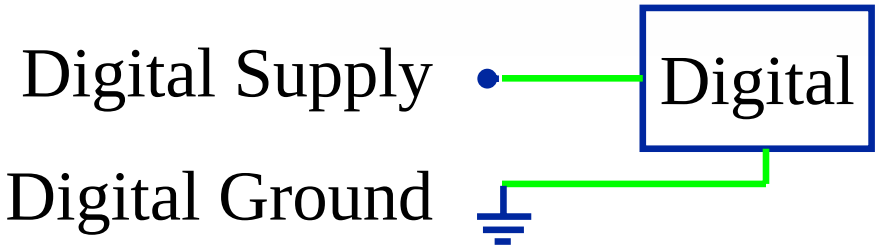
Summary

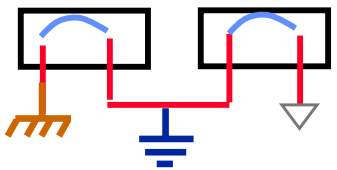
- Reviewed tips & tricks to improve the system susceptibility against EFT/ ESD
- PCB layout and ground planning is very important.
- Hopefully case study will clarify the implementation side
- Many fixes for EFT & ESD helps for other EMC issues

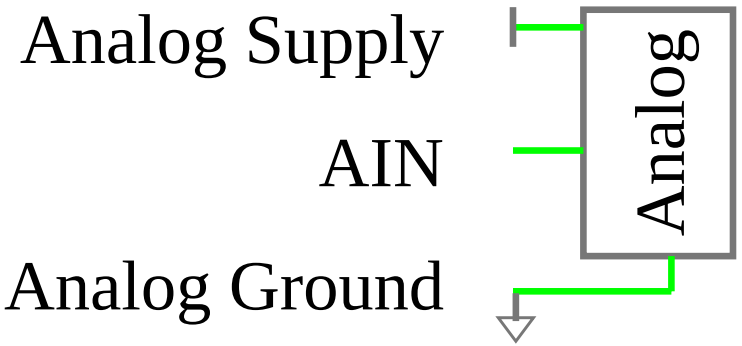
Top Fixes

- Suggested approach

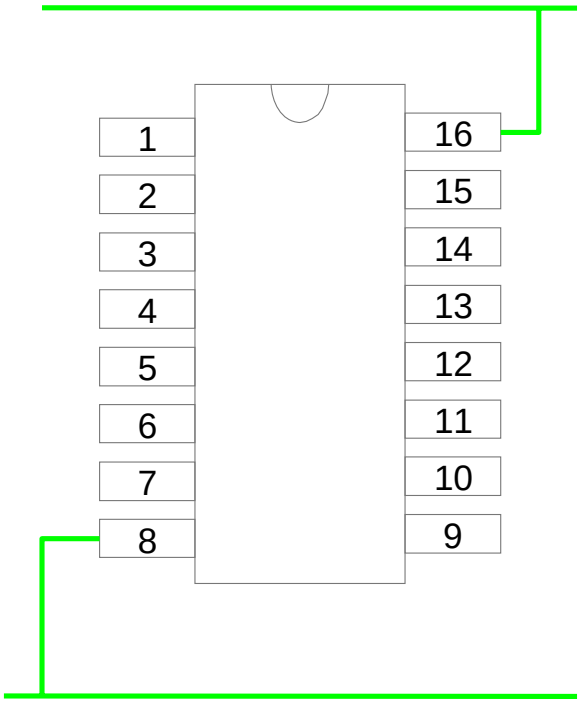




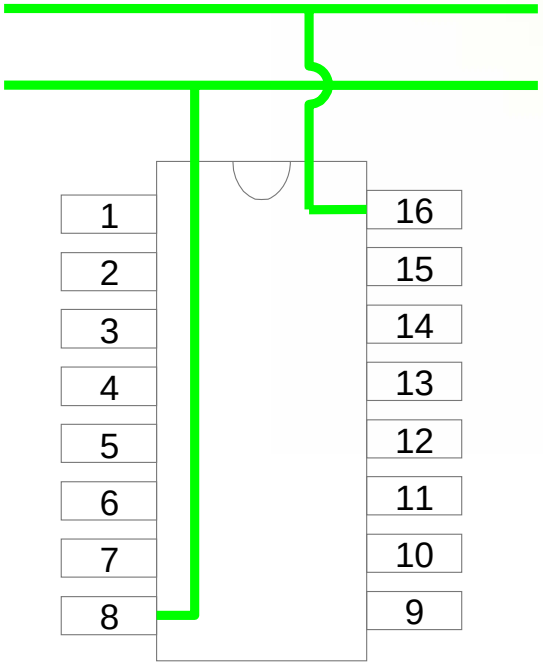




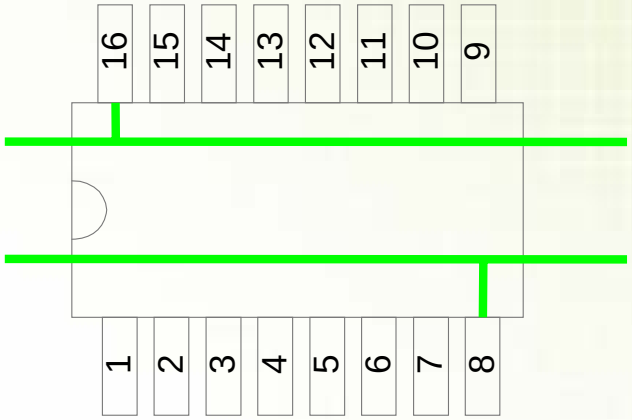
Top Fixes



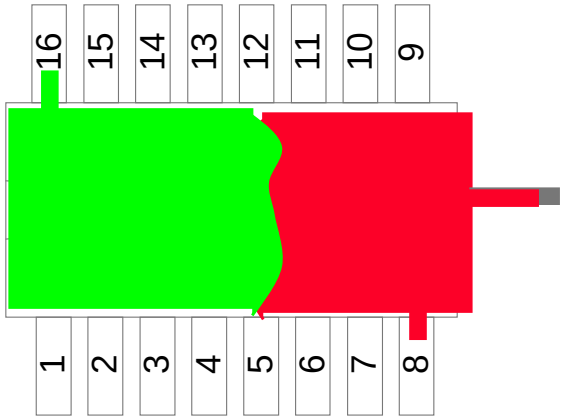
Poor



Good

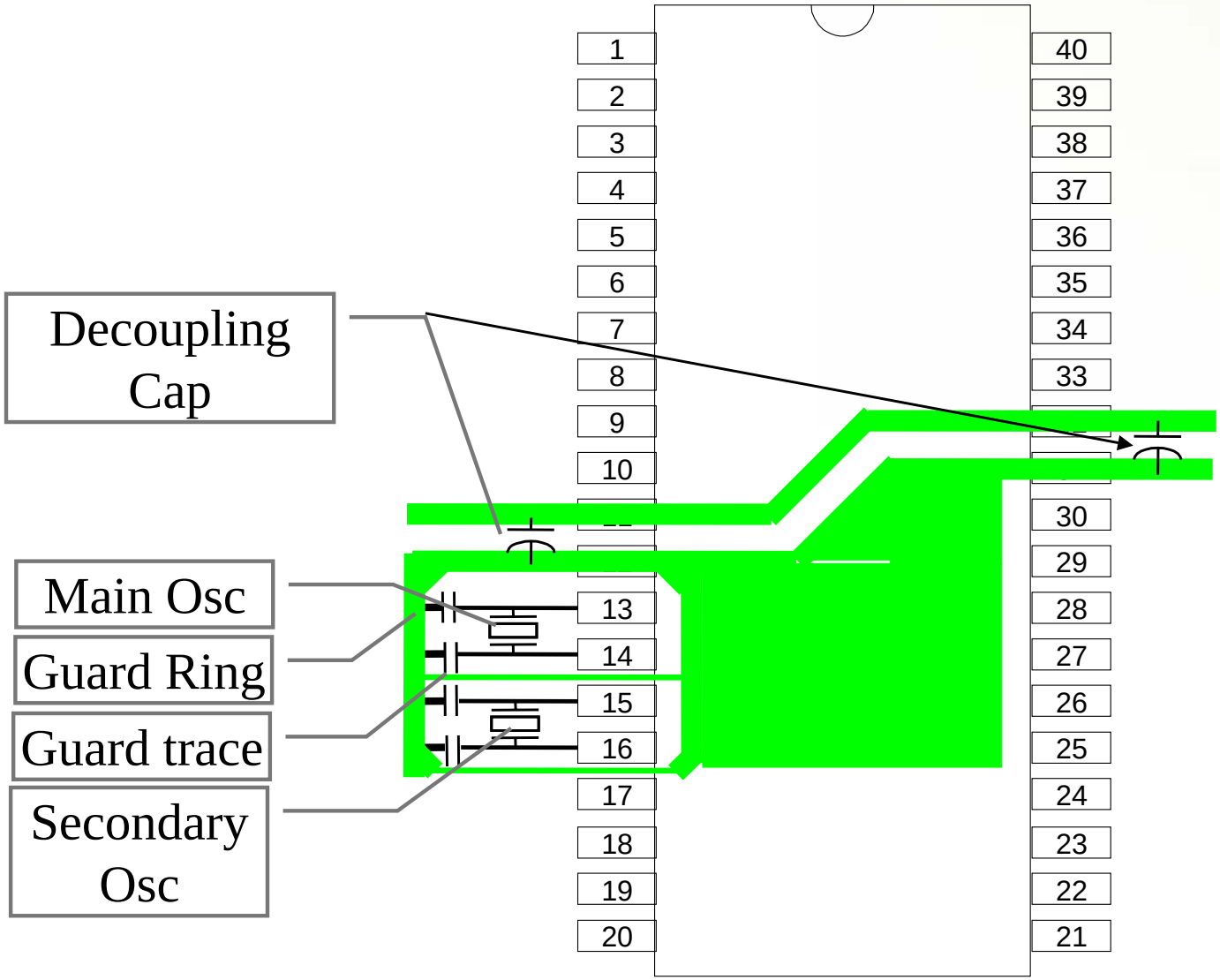


Better



Best

Top Fixes


Decoupling Cap
Main Osc
Guard Ring
Guard trace
Secondary Osc
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