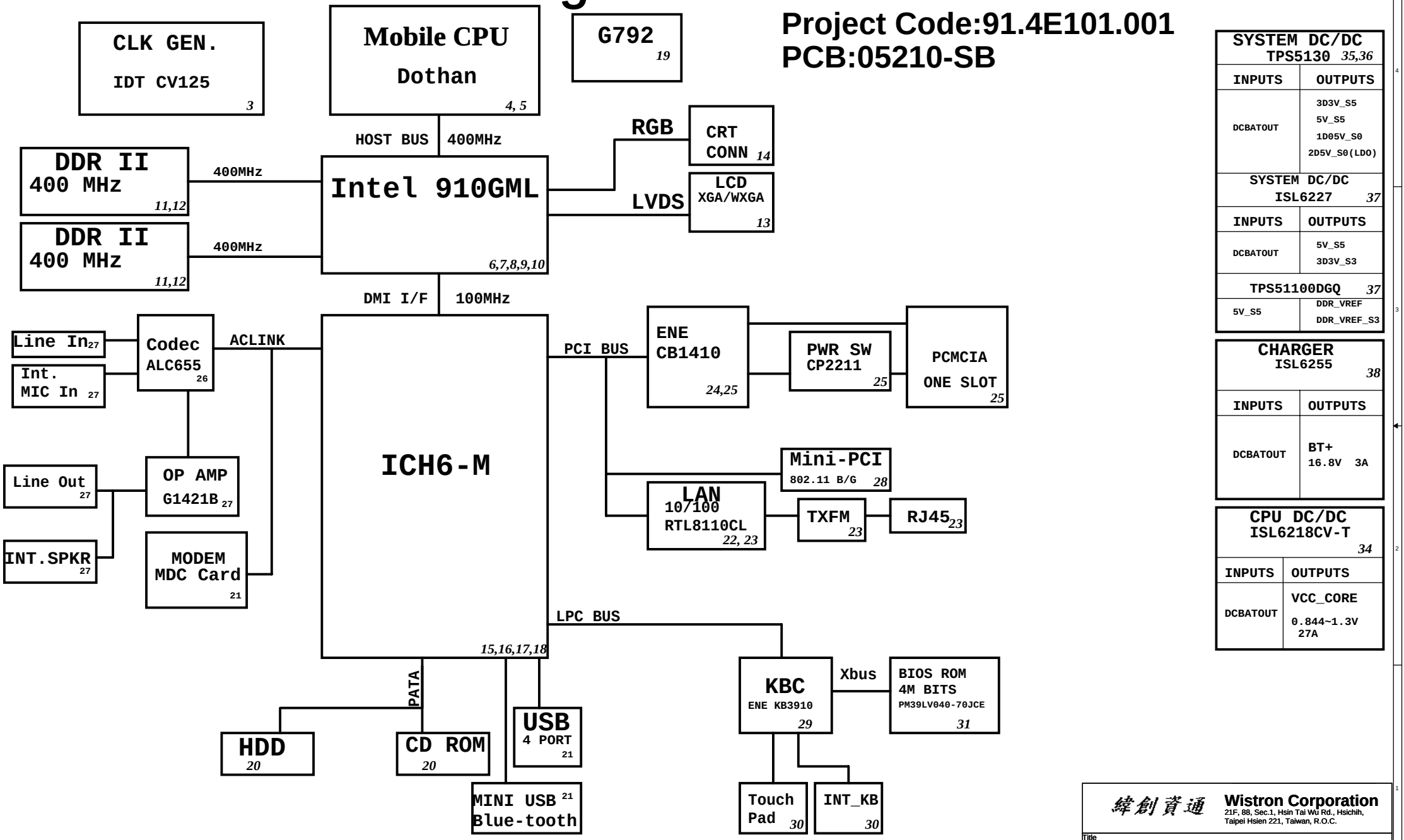
Morar Block Diagram 2005/05/28

Project Code:91.4E101.001
PCB:05210-SB



SYSTEM DC/DC
TPS5130 *35,36*

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5 1D05V_S0 2D5V_S0(LDO)

SYSTEM DC/DC
ISL6227 *37*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DGQ *37*

5V_S5	DDR_VREF DDR_VREF_S3

CHARGER
ISL6255 *38*

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

CPU DC/DC
ISL6218CV-T *34*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

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Title: **BLOCK DIAGRAM**

Size: Custom | Document Number: MORAR | Rev: SB

Date: Thursday, June 09, 2005 | Sheet 1 of 40

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT,ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

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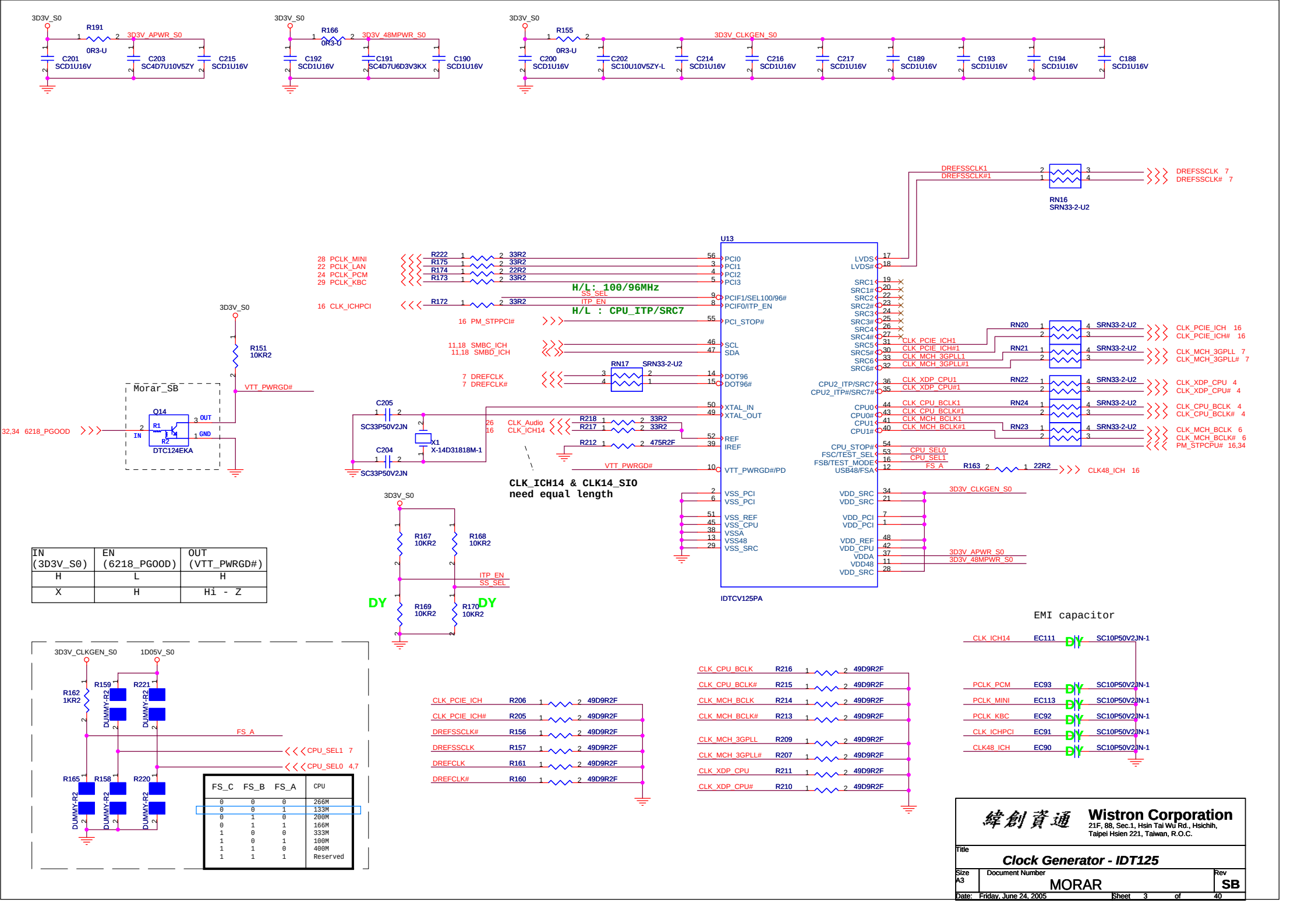
Title: Memo

Size: A3 | Document Number: MORAR | Rev: SB

Date: Saturday, May 28, 2005 | Sheet 2 of 40


3D3V_S0
R191
0R3-U
3D3V_APWR_S0
C201 SCD1U16V
C203 SC4D7U10V5ZY
C215 SCD1U16V
R166
0R3-U
3D3V_48MPWR_S0
C192 SCD1U16V
C191 SC4D7U6D3V3KX
C190 SCD1U16V
R155
0R3-U
3D3V_CLKGEN_S0
C200 SCD1U16V
C202 SC10U10V5ZY-L
C214 SCD1U16V
C216 SCD1U16V
C217 SCD1U16V
C189 SCD1U16V
C193 SCD1U16V
C194 SCD1U16V
C188 SCD1U16V
DREFSSCLK1
DREFSSCLK#1
RN16
SRN33-2-U2
DREFSSCLK 7
DREFSSCLK# 7
U13
28 PCLK_MINI
22 PCLK_LAN
24 PCLK_PCM
29 PCLK_KBC
16 CLK_ICHPCI
R222 33R2
R175 33R2
R174 22R2
R173 33R2
R172 33R2
H/L: 100/96MHz
SS_SEL
ITP_EN
H/L : CPU_ITP/SRC7
16 PM_STPPCI#
11,18 SMBC_ICH
11,18 SMBD_ICH
7 DREFCLK
7 DREFCLK#
RN17 SRN33-2-U2
PCI0
PCI1
PCI2
PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
SCL
SDA
DOT96
DOT96#
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#/PD
VSS_PCI
VSS_PCI
VSS_REF
VSS_CPU
VSSA
VSS48
VSS_SRC
LVDS
LVDS#
SRC1
SRC1#
SRC2
SRC2#
SRC3
SRC3#
SRC4
SRC4#
SRC5
SRC5#
SRC6
SRC6#
CPU2_ITP/SRC7
CPU2_ITP#/SRC7#
CPU0
CPU0#
CPU1
CPU1#
CPU_STOP#
FSC/TEST_SEL
FSB/TEST_MODE
USB48/FSA
VDD_SRC
VDD_SRC
VDD_PCI
VDD_PCI
VDD_REF
VDD_CPU
VDDA
VDD48
VDD_SRC
IDTCV125PA
CLK_PCIE_ICH1
CLK_PCIE_ICH#1
CLK_MCH_3GPLL1
CLK_MCH_3GPLL#1
CLK_XDP_CPU1
CLK_XDP_CPU#1
CLK_CPU_BCLK1
CLK_CPU_BCLK#1
CLK_MCH_BCLK1
CLK_MCH_BCLK#1
CPU_SEL0
CPU_SEL1
FS_A
R163 22R2
CLK48_ICH 16
RN20 SRN33-2-U2
RN21 SRN33-2-U2
RN22 SRN33-2-U2
RN24 SRN33-2-U2
RN23 SRN33-2-U2
CLK_PCIE_ICH 16
CLK_PCIE_ICH# 16
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_XDP_CPU 4
CLK_XDP_CPU# 4
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
PM_STPCPU# 16,34
3D3V_CLKGEN_S0
3D3V_APWR_S0
3D3V_48MPWR_S0
C205 SC33P50V2JN
C204 SC33P50V2JN
X1 X-14D31818M-1
26 CLK_Audio
16 CLK_ICH14
R218 33R2
R217 33R2
R212 475R2F
VTT_PWRGD#
CLK_ICH14 & CLK14_SIO
need equal length
3D3V_S0
R151 10KR2
VTT_PWRGD#
Morar_SB
Q14
R1
R2
DTC124EKA
IN
OUT
GND
32,34 6218_PGOOD
R167 10KR2
R168 10KR2
R169 10KR2
R170 10KR2
ITP_EN
SS_SEL
DY
DY
IN (3D3V_S0) | EN (6218_PGOOD) | OUT (VTT_PWRGD#)
H | L | H
X | H | Hi - Z
3D3V_CLKGEN_S0
1D05V_S0
R162 1KR2
R159 DUMMY-R2
R221 DUMMY-R2
R165 DUMMY-R2
R158 DUMMY-R2
R220 DUMMY-R2
FS_A
CPU_SEL1 7
CPU_SEL0 4,7
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
CLK_PCIE_ICH R206 49D9R2F
CLK_PCIE_ICH# R205 49D9R2F
DREFSSCLK# R156 49D9R2F
DREFSSCLK R157 49D9R2F
DREFCLK R161 49D9R2F
DREFCLK# R160 49D9R2F
CLK_CPU_BCLK R216 49D9R2F
CLK_CPU_BCLK# R215 49D9R2F
CLK_MCH_BCLK R214 49D9R2F
CLK_MCH_BCLK# R213 49D9R2F
CLK_MCH_3GPLL R209 49D9R2F
CLK_MCH_3GPLL# R207 49D9R2F
CLK_XDP_CPU R211 49D9R2F
CLK_XDP_CPU# R210 49D9R2F
EMI capacitor
CLK_ICH14 EC111 DY SC10P50V2JN-1
PCLK_PCM EC93 DY SC10P50V2JN-1
PCLK_MINI EC113 DY SC10P50V2JN-1
PCLK_KBC EC92 DY SC10P50V2JN-1
CLK_ICHPCI EC91 DY SC10P50V2JN-1
CLK48_ICH EC90 DY SC10P50V2JN-1
緯創資通
Wistron Corporation
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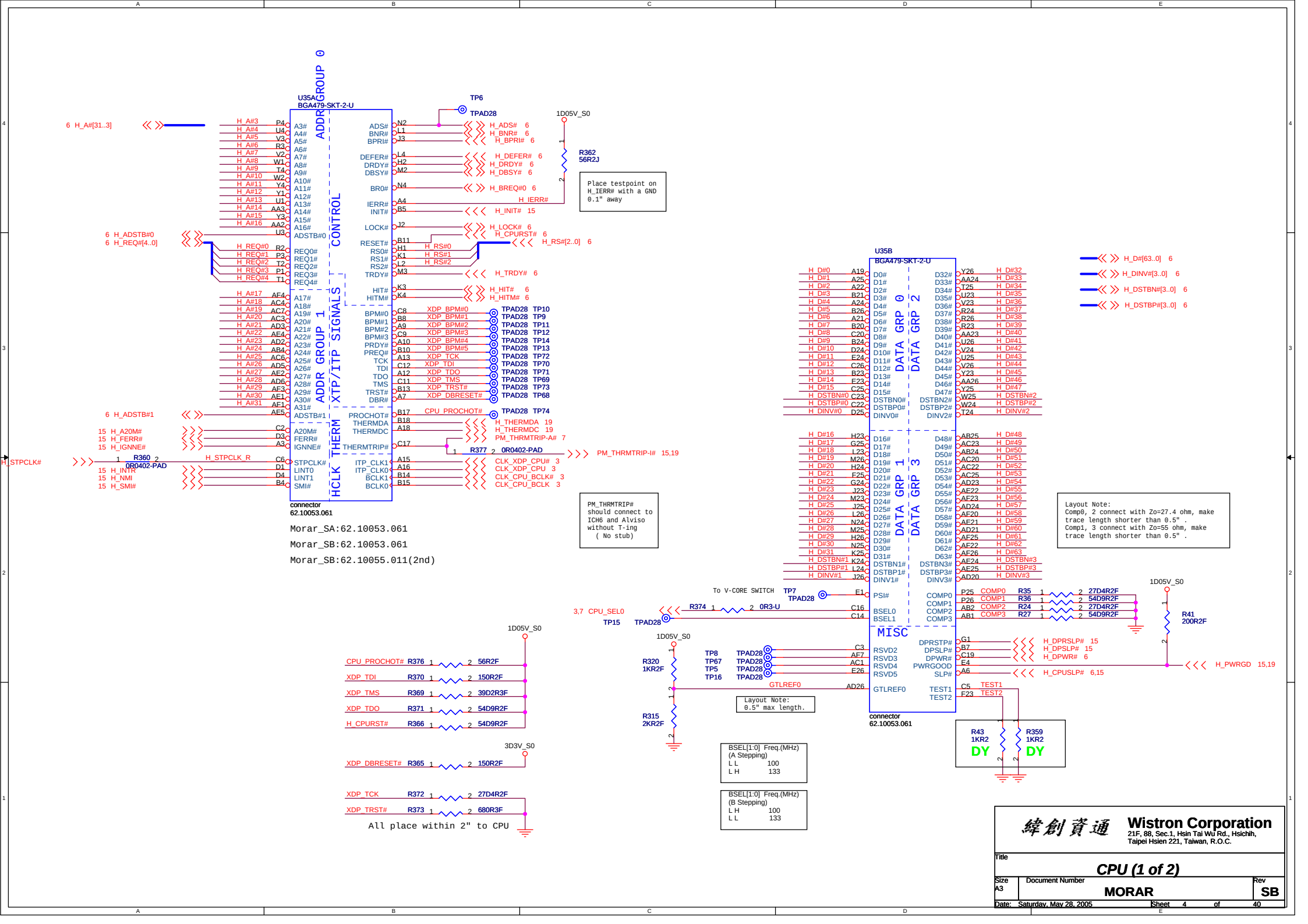
Title
Clock Generator - IDT125
Size A3
Document Number MORAR
Rev SB
Date: Friday, June 24, 2005
Sheet 3 of 40


U35A
BGA479-SKT-2-U
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
CONTROL
HCLK THERM
connector
62.10053.061
TP6
TPAD28
1D05V_S0
R362
56R2J
Place testpoint on
H_IERR# with a GND
0.1" away
R360
0R0402-PAD
R377
0R0402-PAD
PM_THRMTRIP-I# 15,19
PM_THRMTRIP#
should connect to
ICH6 and Alviso
without T-ing
(No stub)
Morar_SA:62.10053.061
Morar_SB:62.10053.061
Morar_SB:62.10055.011(2nd)
U35B
BGA479-SKT-2-U
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
connector
62.10053.061
To V-CORE SWITCH
TP7
TPAD28
R374
0R3-U
3,7 CPU_SEL0
TP15
R320
1KR2F
R315
2KR2F
GTLREF0
Layout Note:
0.5" max length.
R41
200R2F
R43
1KR2
DY
R359
1KR2
DY
BSEL[1:0] Freq.(MHz)
(A Stepping)
L L 100
L H 133
BSEL[1:0] Freq.(MHz)
(B Stepping)
L H 100
L L 133
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5" .
CPU_PROCHOT# R376 56R2F
XDP_TDI R370 150R2F
XDP_TMS R369 39D2R3F
XDP_TDO R371 54D9R2F
H_CPURST# R366 54D9R2F
3D3V_S0
XDP_DBRESET# R365 150R2F
XDP_TCK R372 27D4R2F
XDP_TRST# R373 680R3F
All place within 2" to CPU
緯創資通
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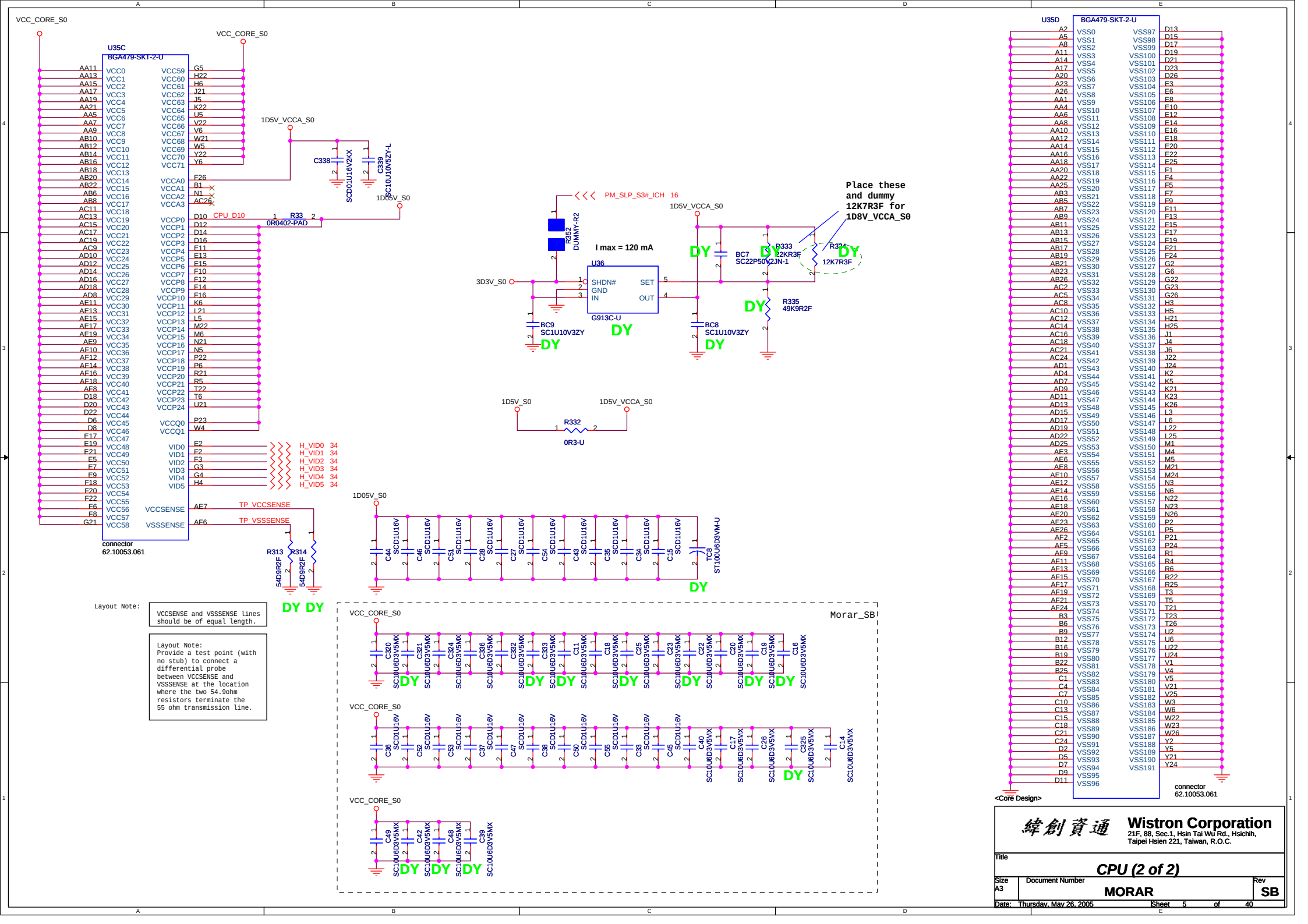
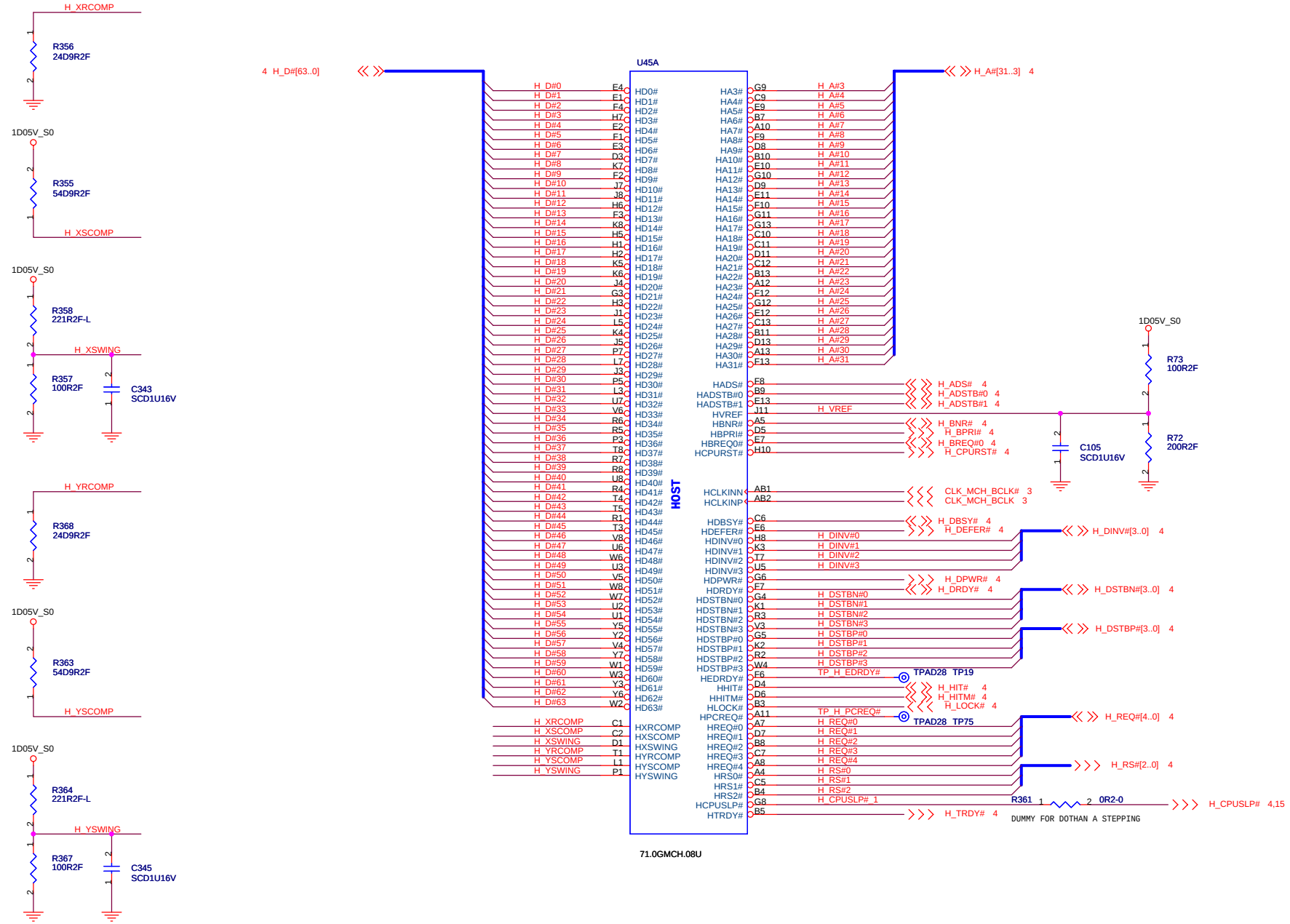
Title
CPU (1 of 2)
Size A3
Document Number
MORAR
Rev SB
Date: Saturday, May 28, 2005
Sheet 4 of 40


VCC_CORE_S0
U35C
BGA479-SKT-2-U
connector
62.10053.061
1D5V_VCCA_S0
C338
SCD01U16V2KX
C339
SC10U10V5ZY-L
1D05V_S0
CPU_D10
R33
0R0402-PAD
PM_SLP_S3#_ICH 16
R352
DUMMY-R2
I max = 120 mA
U36
SHDN#
GND
IN
SET
OUT
G913C-U
3D3V_S0
BC9
SC1U10V3ZY
BC8
SC1U10V3ZY
BC7
SC22P50V2JN-1
R333
22KR3F
R334
12K7R3F
R335
49K9R2F
Place these and dummy 12K7R3F for 1D8V_VCCA_S0
DY
R332
0R3-U
H_VID0 34
H_VID1 34
H_VID2 34
H_VID3 34
H_VID4 34
H_VID5 34
TP_VCCSENSE
TP_VSSSENSE
R313
R314
54D9R2F
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
Morar_SB
U35D
BGA479-SKT-2-U
connector
62.10053.061
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size
A3
Document Number
MORAR
Rev
SB
Date: Thursday, May 26, 2005
Sheet 5 of 40



Place them near to the chip

<Core Design>

緯創資通 **Wistron Corporation**
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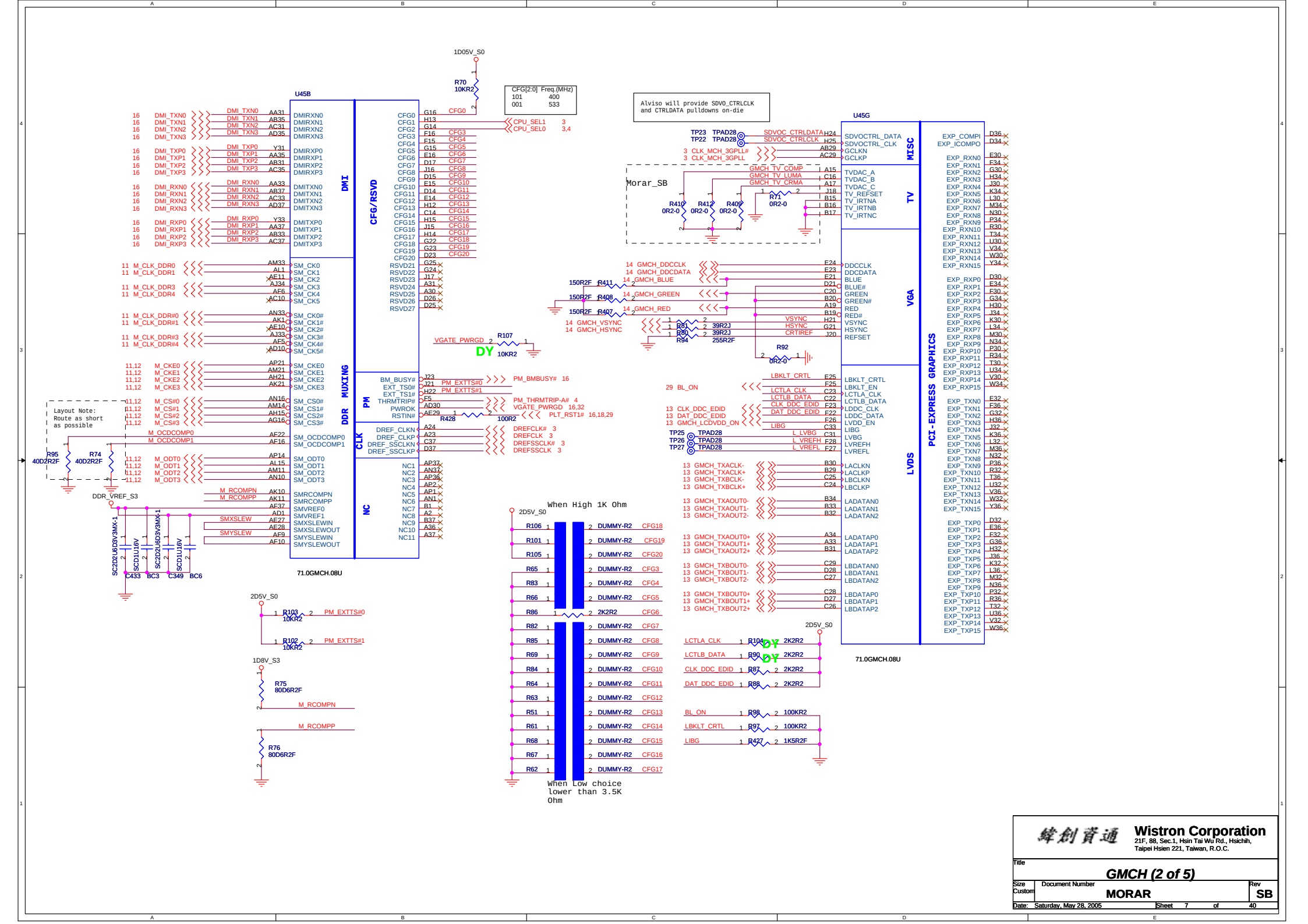
Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	MORAR	SB

Date: Friday, June 24, 2005 Sheet 6 of 40



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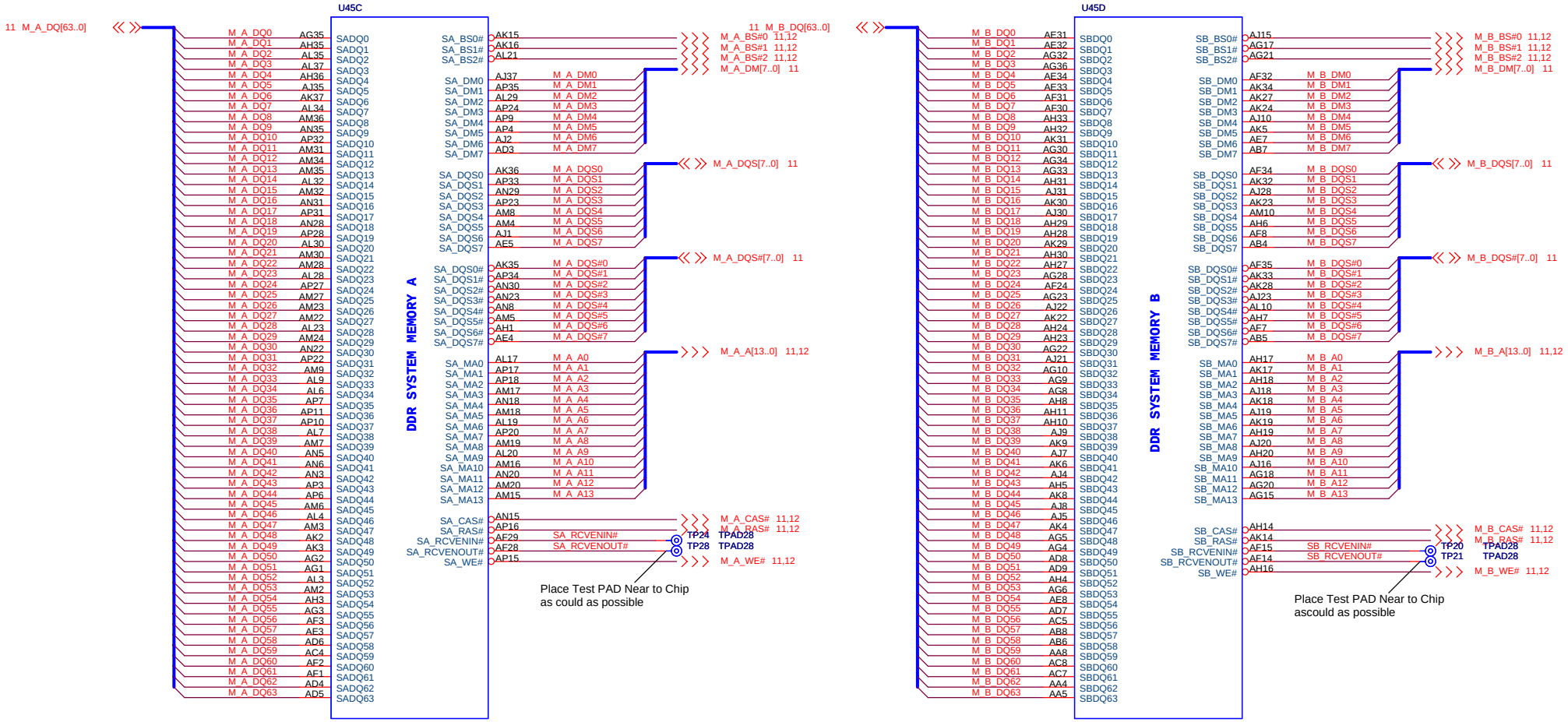
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (2 of 5)**

Size: Custom | Document Number: MORAR | Rev: SB

Date: Saturday, May 28, 2005 | Sheet 7 of 40



<Core Design>

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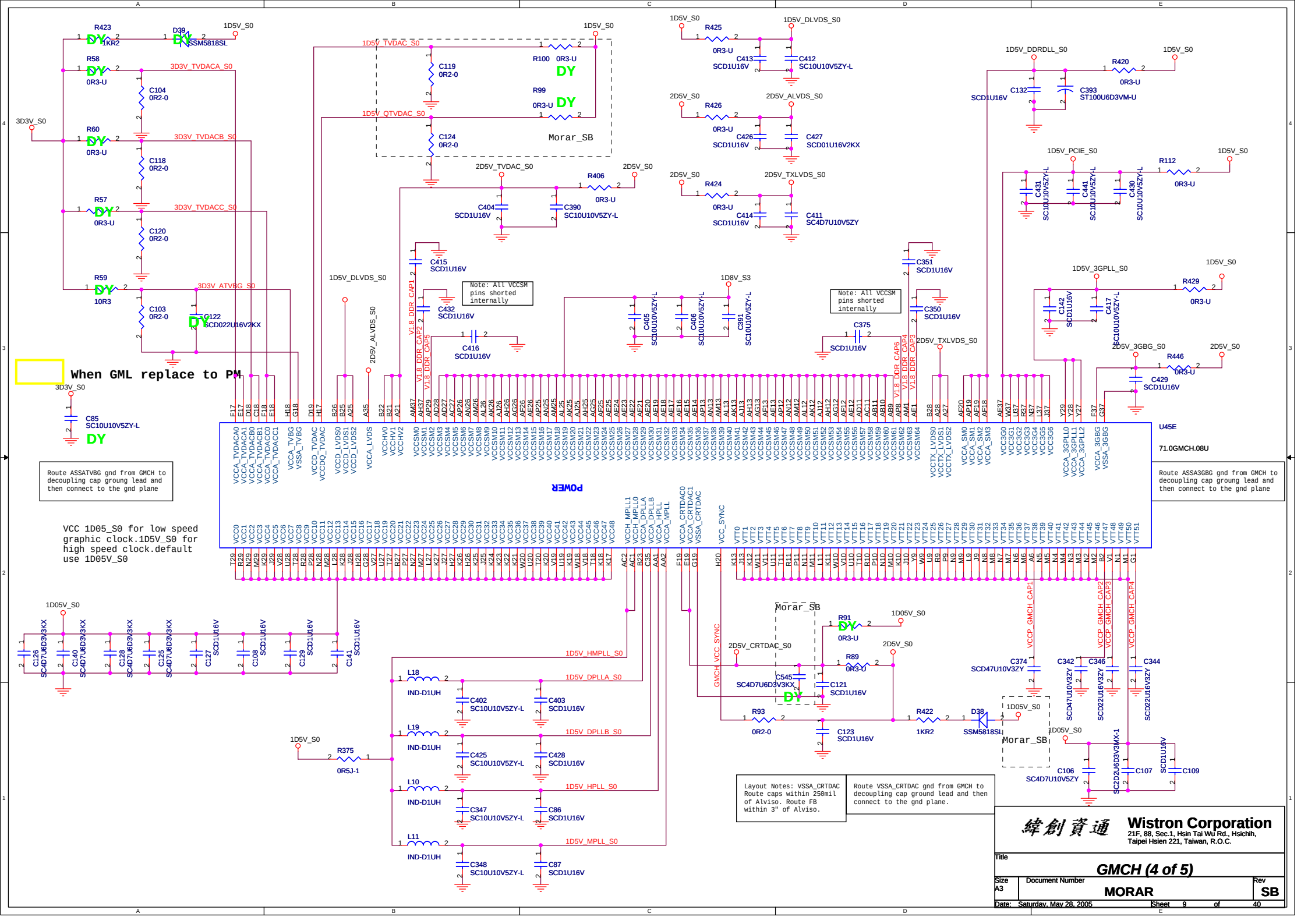
Title: GMCH (3 of 5)

Size	Document Number	Rev
A3	MORAR	SB

Date: Friday, June 24, 2005 Sheet 8 of 40


When GML replace to PM
U45E
71.0GMCH.08U
POWER
Morar_SB
Note: All VCCSM pins shorted internally
Route ASSATVBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
Route ASSA3GBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
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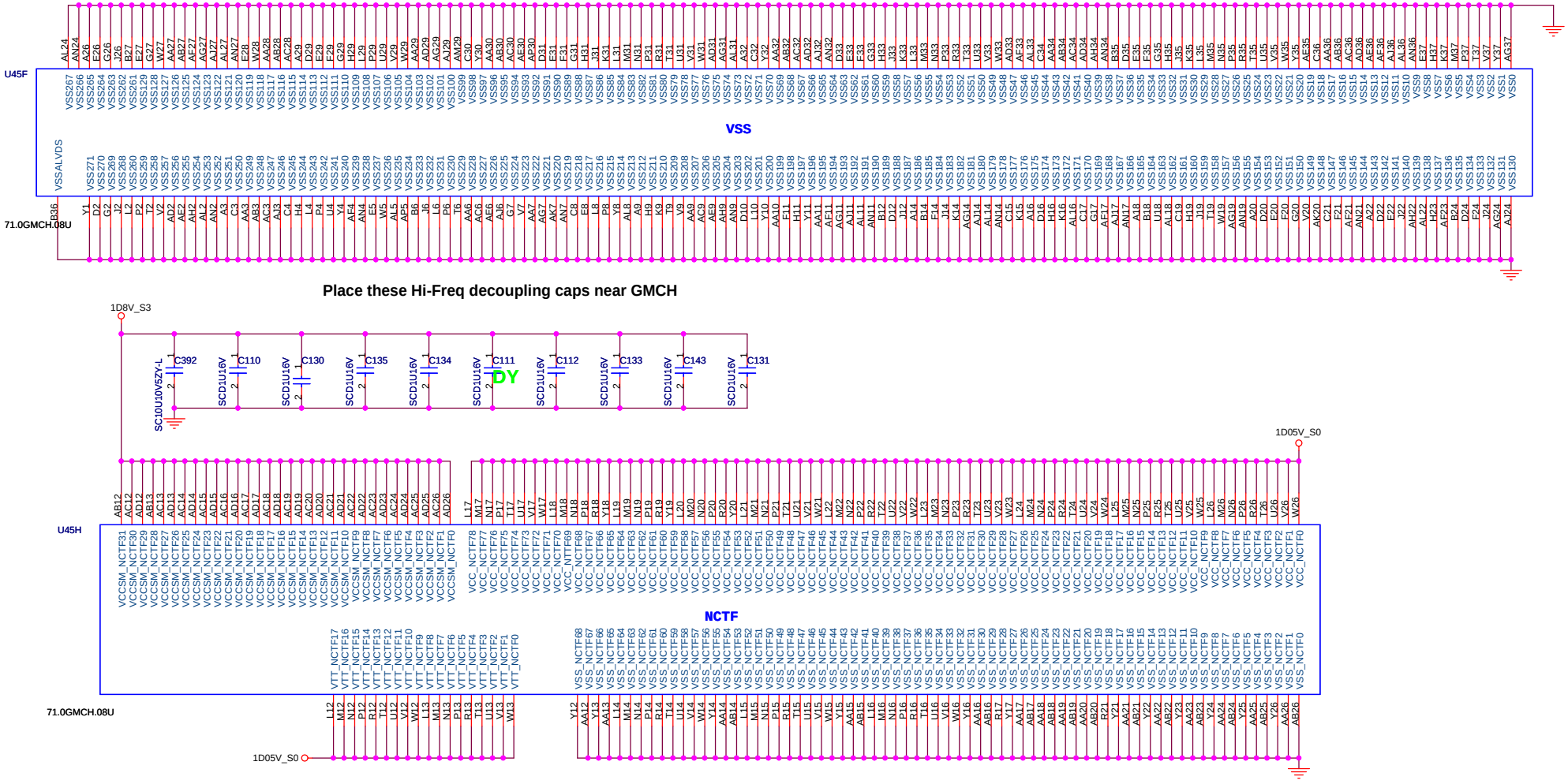
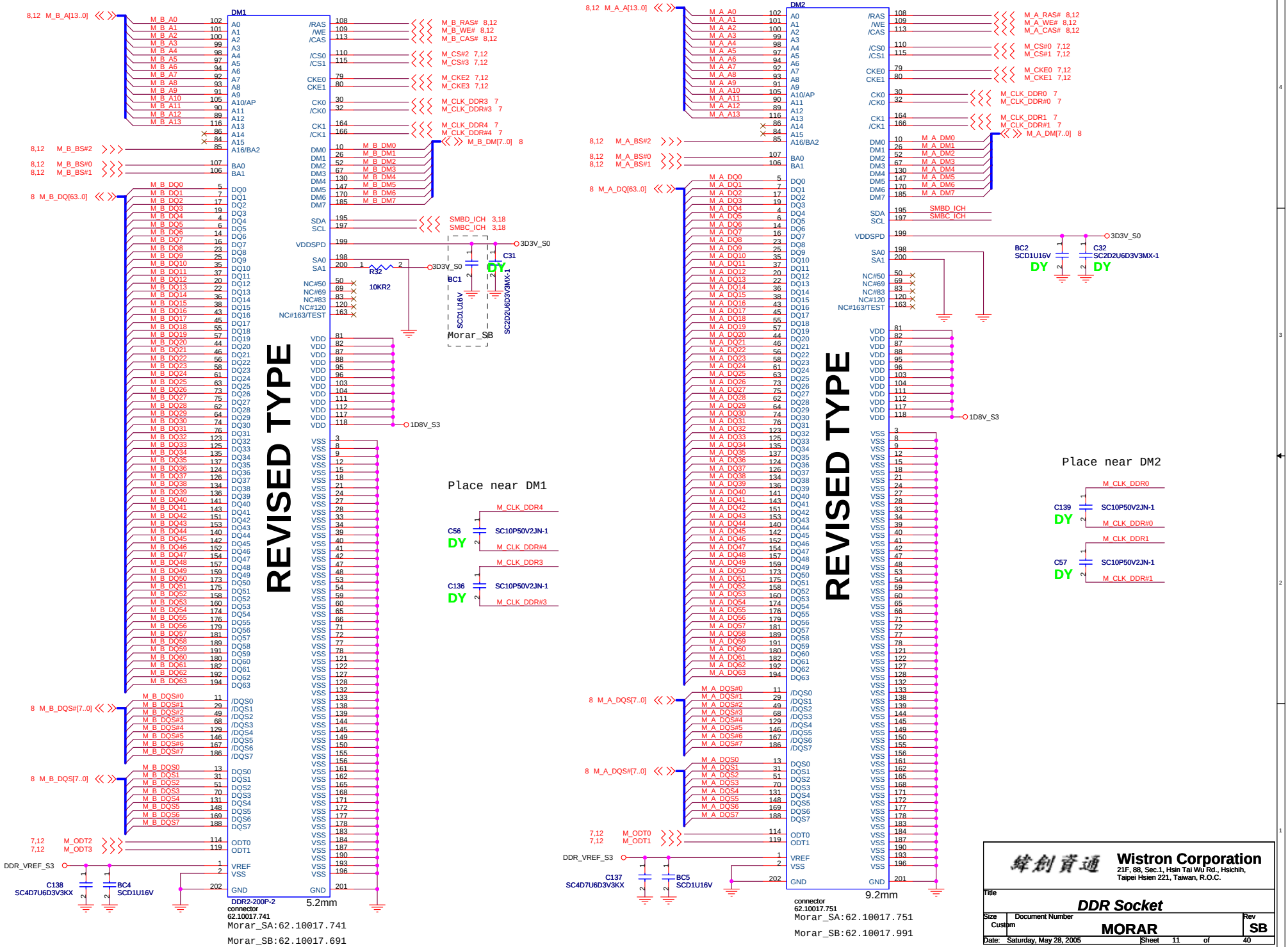
Title
GMCH (4 of 5)
Size A3
Document Number MORAR
Rev SB
Date: Saturday, May 28, 2005
Sheet 9 of 40



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	***GMCH (5 of 5)***			
Size A3	Document Number **MORAR**			Rev **SB**
Date: Friday, June 24, 2005		Sheet 10 of 40		


DM1
REVISED TYPE
DDR2-200P-2
connector
62.10017.741
5.2mm
Morar_SA:62.10017.741
Morar_SB:62.10017.691
Morar_SB
Place near DM1
C56 SC10P50V2JN-1 DY
C136 SC10P50V2JN-1 DY
C31
BC1
R32 10KR2
C138 SC4D7U6D3V3KX
BC4 SCD1U16V
DM2
REVISED TYPE
connector
62.10017.751
9.2mm
Morar_SA:62.10017.751
Morar_SB:62.10017.991
Place near DM2
C139 SC10P50V2JN-1 DY
C57 SC10P50V2JN-1 DY
BC2 SCD1U16V DY
C32 SC2D2U6D3V3MX-1 DY
C137 SC4D7U6D3V3KX
BC5 SCD1U16V
Wistron Corporation
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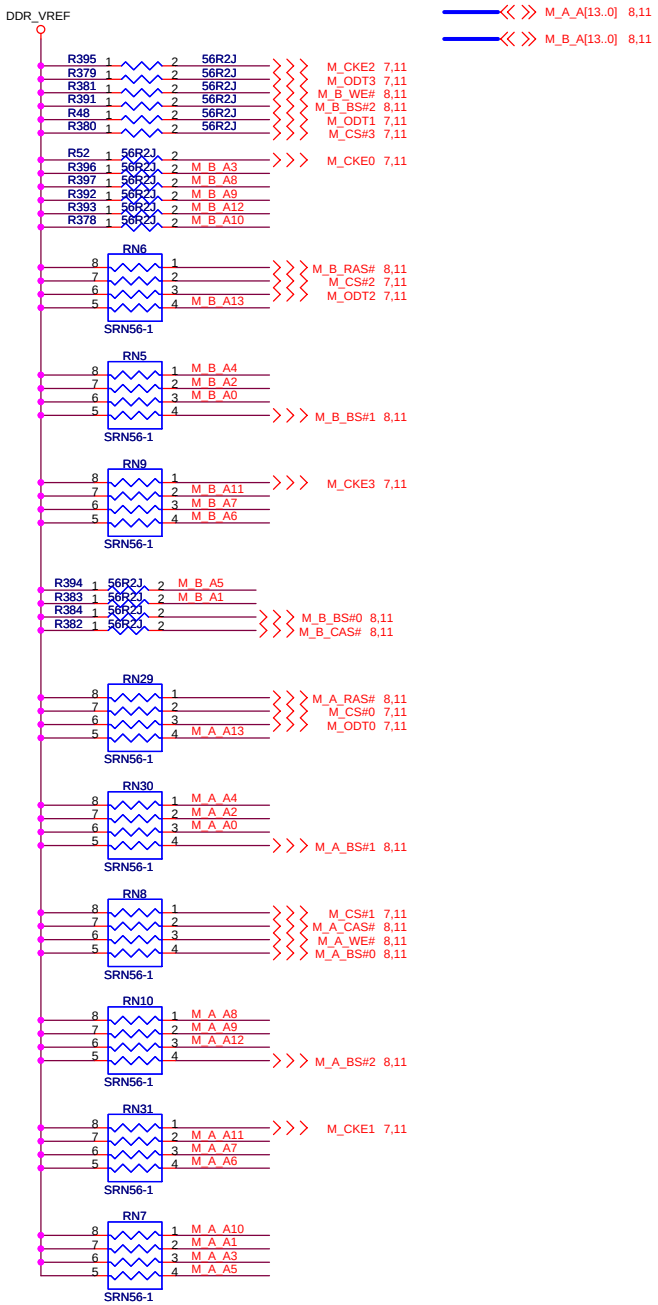
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR Socket
Size Custom
Document Number MORAR
Rev SB
Date: Saturday, May 28, 2005
Sheet 11 of 40

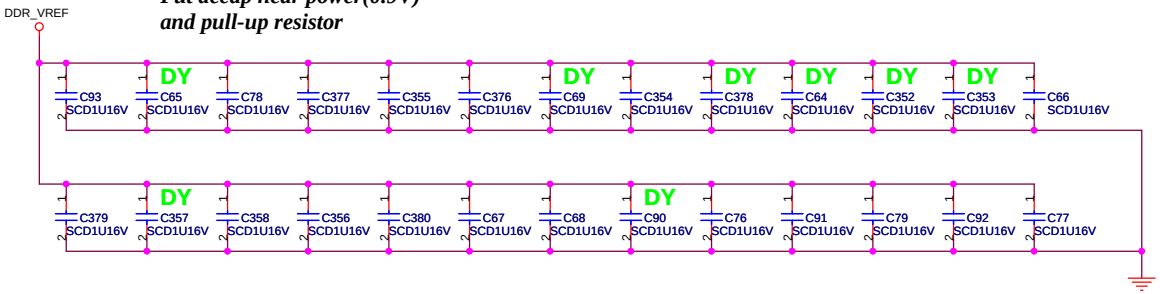
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

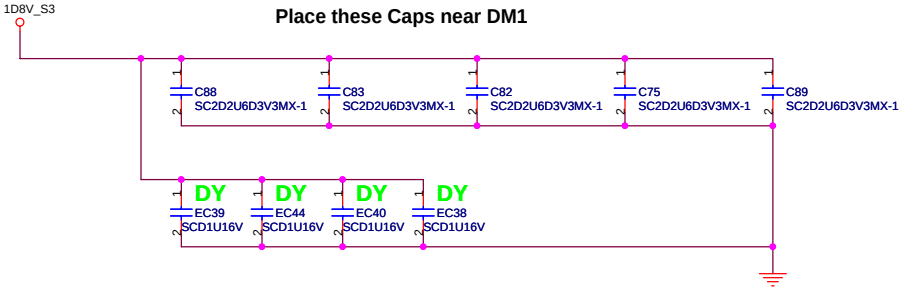


Decoupling Capacitor

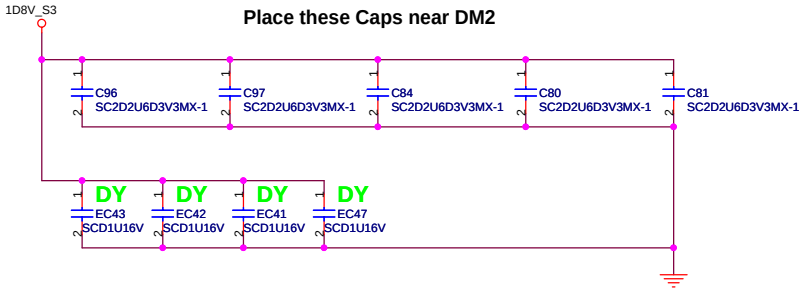
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



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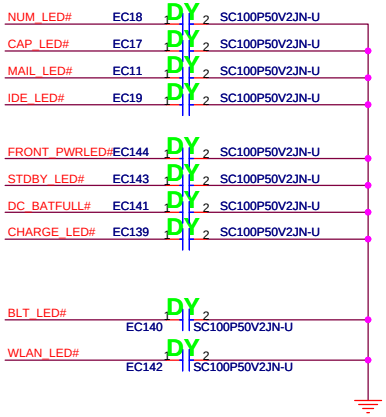
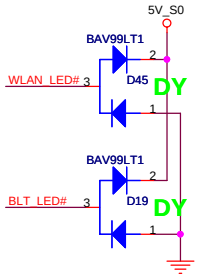
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	MORAR	SB

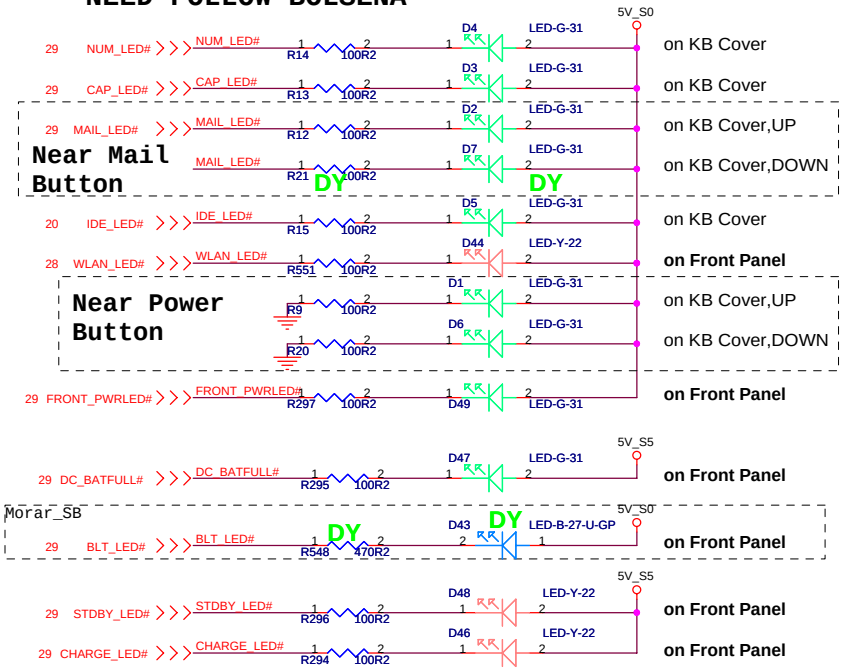
Date: Friday, June 24, 2005 Sheet 12 of 40

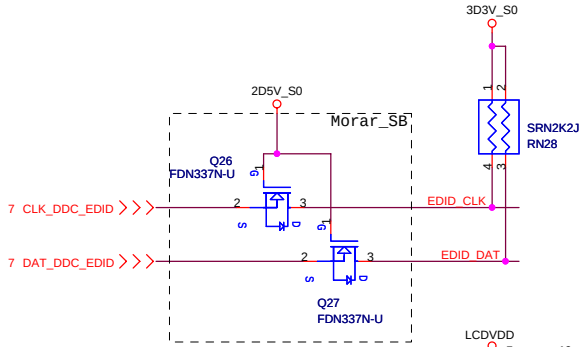
LED

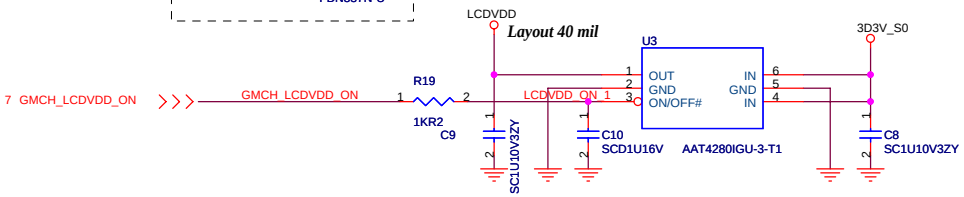




NEED FOLLOW BOLSENA







on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

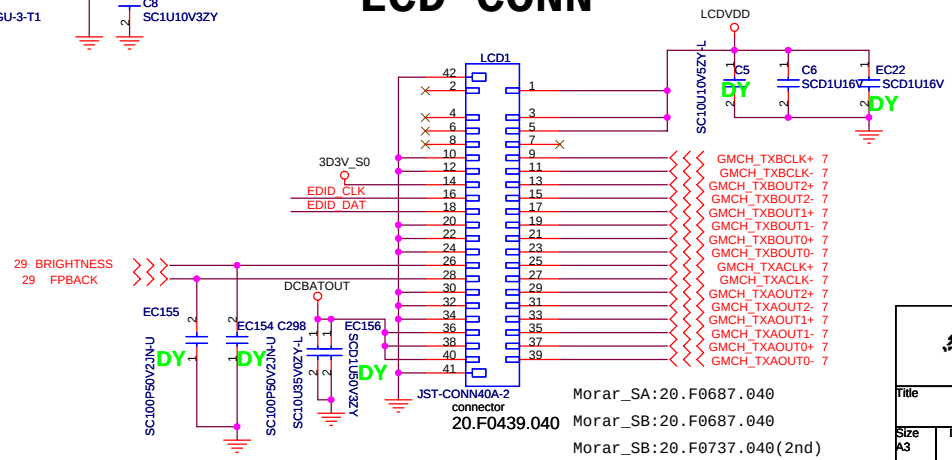
LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

Charger:
Green : DC only or Battery full with DC
Orange : Charging
Orange Blink : Battery low

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

LCD CONN



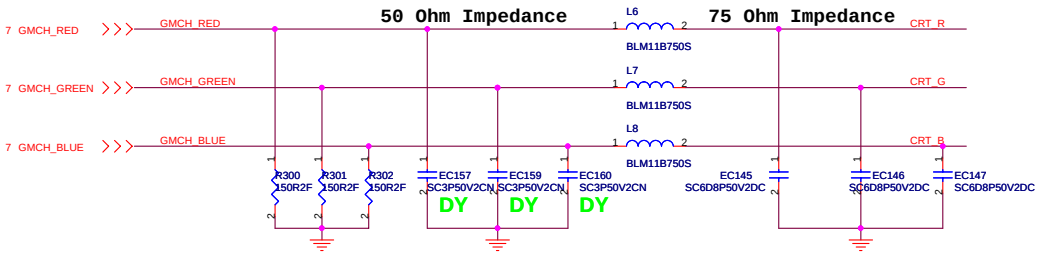
Morar_SA:20.F0687.040
Morar_SB:20.F0687.040
Morar_SB:20.F0737.040(2nd)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

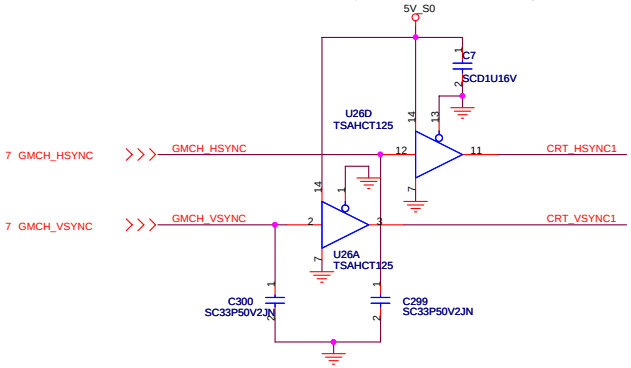
Title	LCD CONN & LED		
Size A3	Document Number MORAR		Rev SB
Date: Saturday, May 28, 2005	Sheet 13	of	40

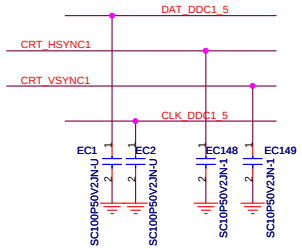
CRT CONNECTOR

Ferrite bead impedance: 75ohm@100MHz

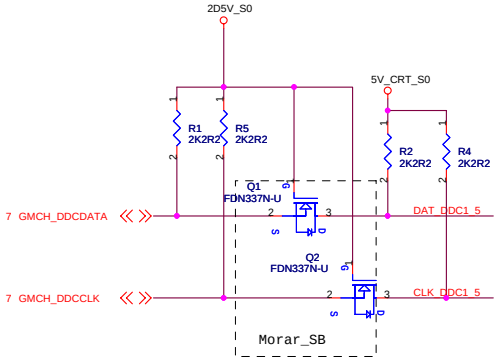


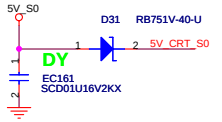
Hsync & Vsync level shift

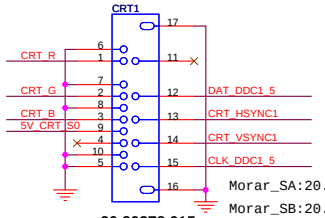




DDC_CLK & DATA level shift



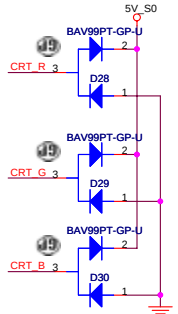




Morar_SA:20.20378.015
Morar_SB:20.20378.015

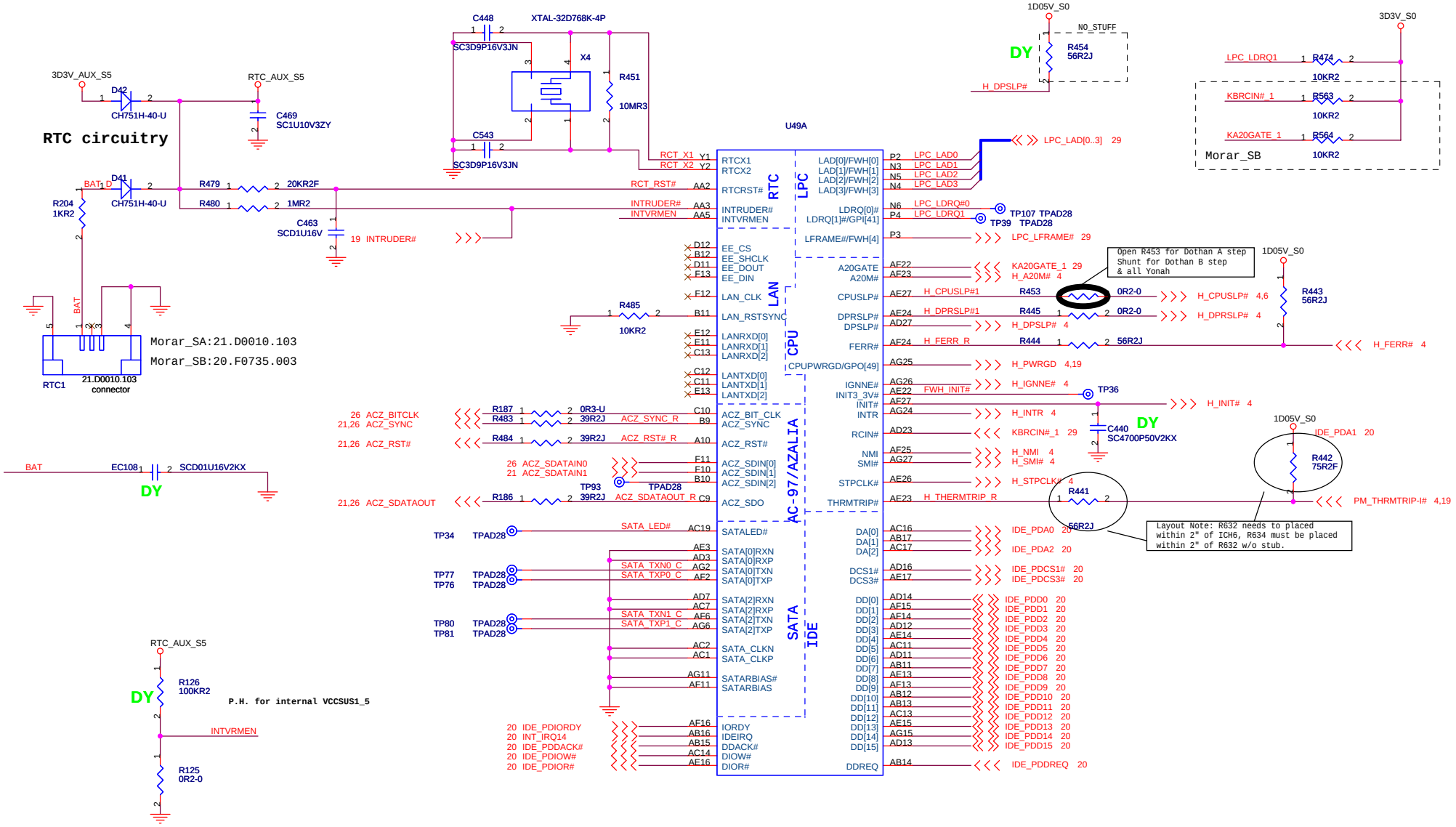
20.20378.015
VIDEO-15-42
connector

ESD Protection Diode

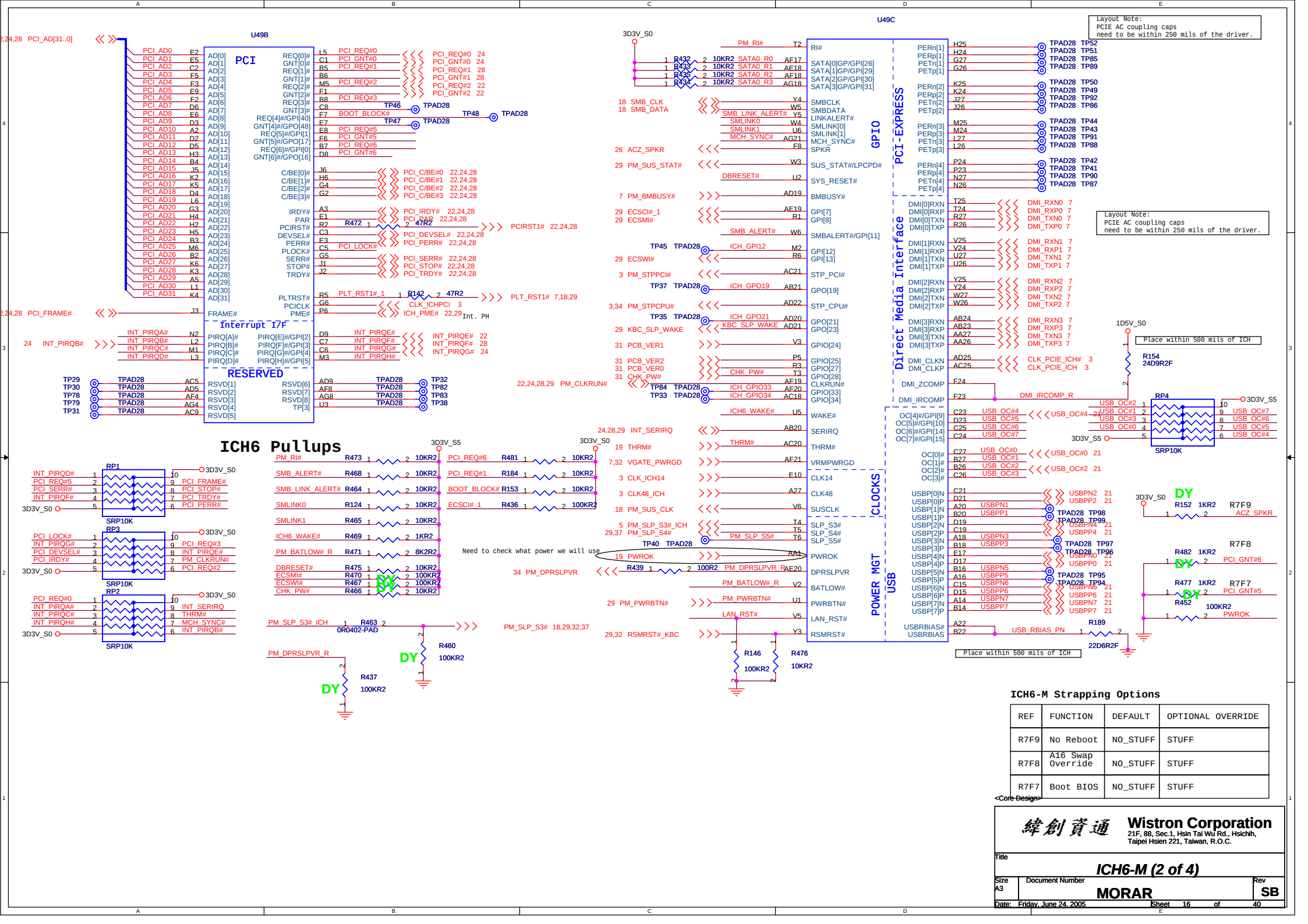


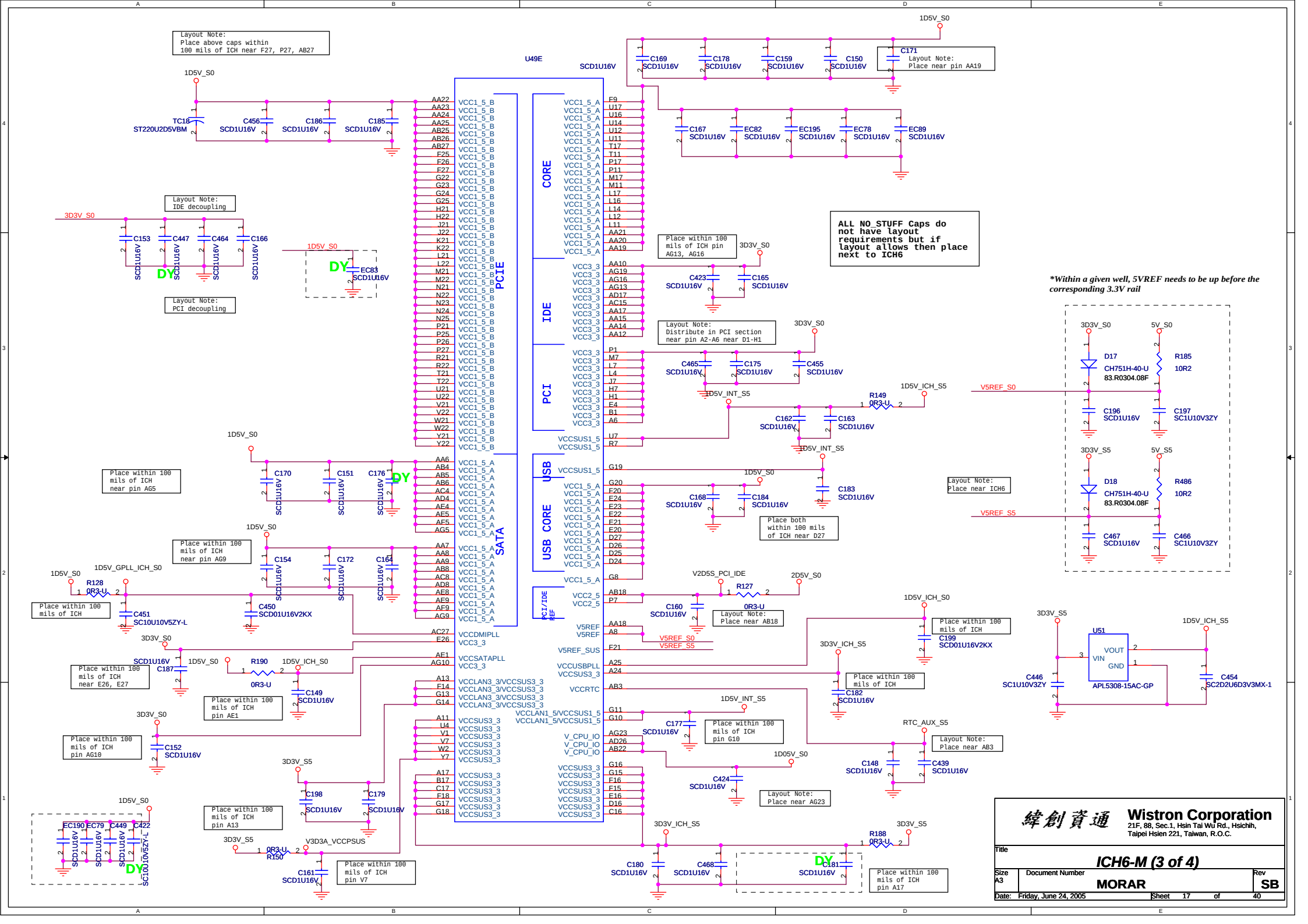
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT Connector*		
Size: Custom	Document Number: MORAR	Rev: SB
Date: Saturday, May 28, 2005	Sheet 14 of 40	

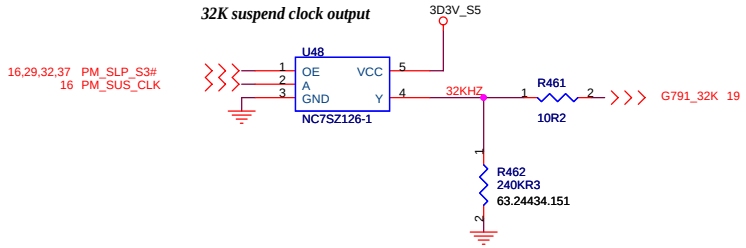


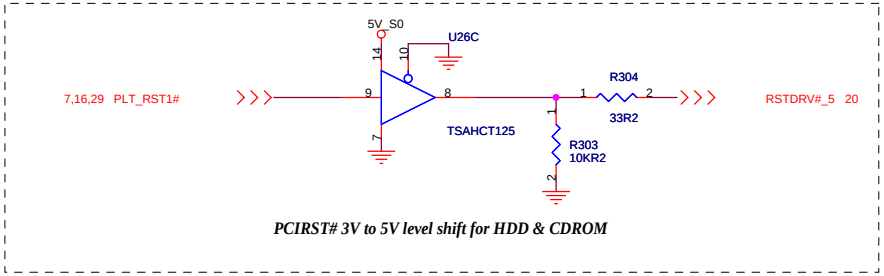
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*ICH6-M (1 of 4)*	
Size A3	Document Number **MORAR**	Rev **SB**
Date: Saturday, May 28, 2005	Sheet 15 of 40	


U49B
PCI
Interrupt I/F
RESERVED
U49C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
USB
POWER MGT
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
ICH6 Pullups
Need to check what power we will use
ICH6-M Strapping Options
REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE
R7F9 | No Reboot | NO_STUFF | STUFF
R7F8 | A16 Swap Override | NO_STUFF | STUFF
R7F7 | Boot BIOS | NO_STUFF | STUFF
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (2 of 4)
Size A3
Document Number
MORAR
Rev SB
Date: Friday, June 24, 2005
Sheet 16 of 40


U49E
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Place within 100 mils of ICH pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin A17
Place both within 100 mils of ICH near D27
Layout Note: Place near AB18
Layout Note: Place near AG23
Layout Note: Place near AB3
Layout Note: Place near pin AA19
Layout Note: Place near ICH6
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
Document Number MORAR
Rev SB
Date: Friday, June 24, 2005
Sheet 17 of 40

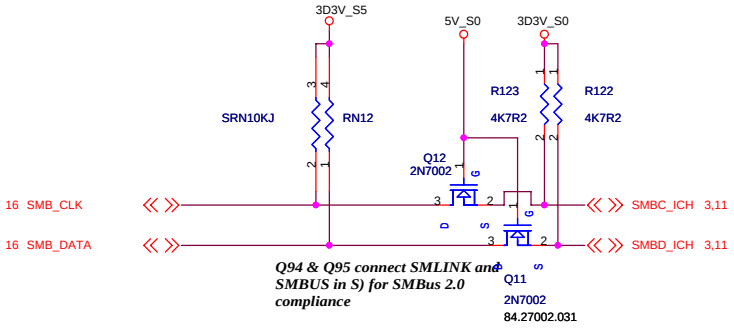
32K suspend clock output





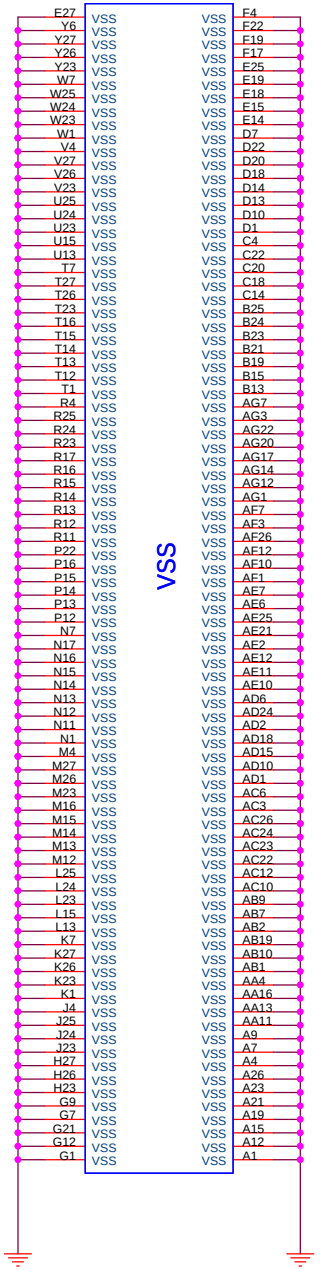
PCIRST# 3V to 5V level shift for HDD & CDROM

SMBUS



Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

U49D



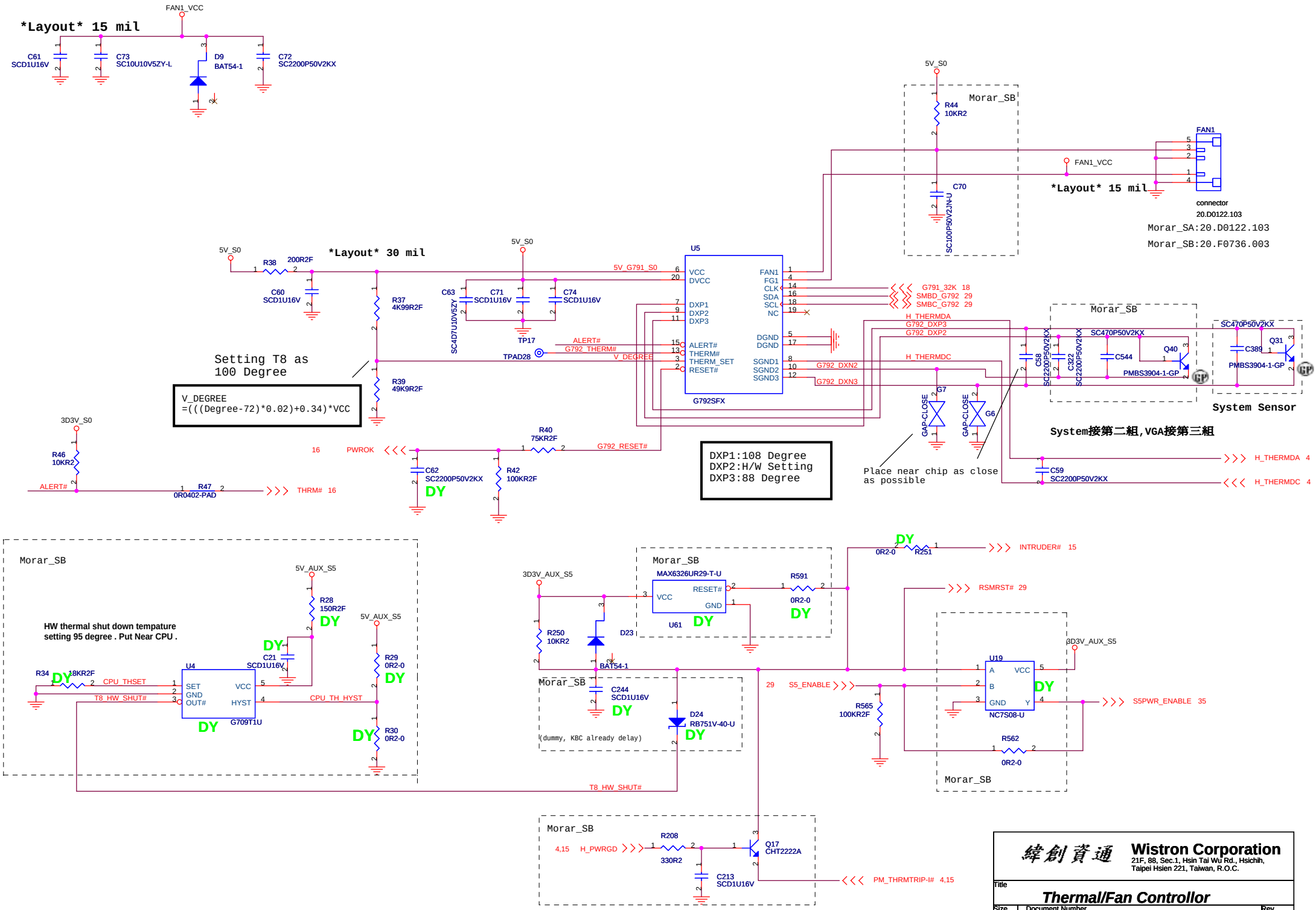
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

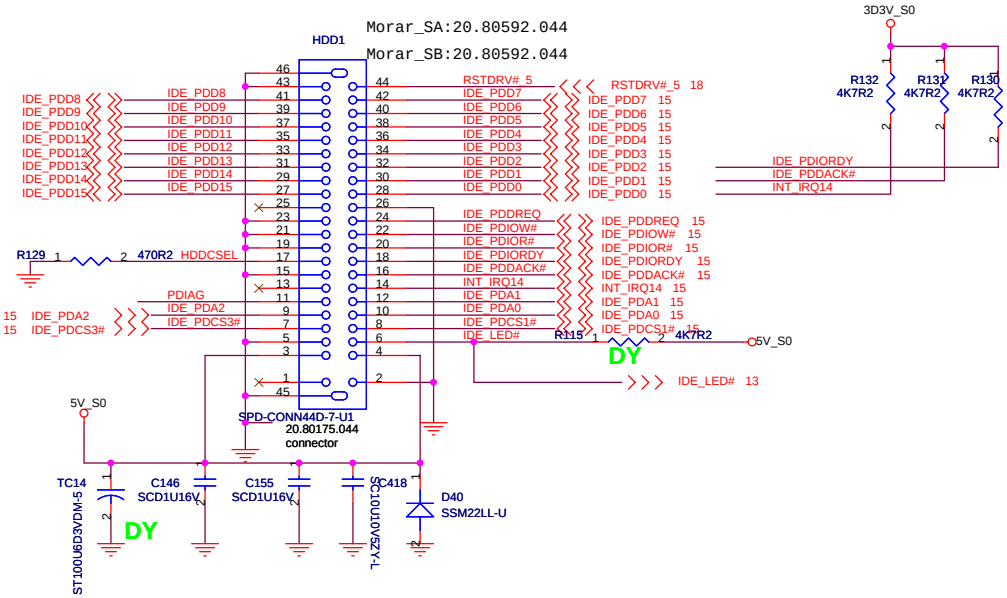
Title: ICH6-M (4 of 4)

Size: A3 | Document Number: MORAR | Rev: SB

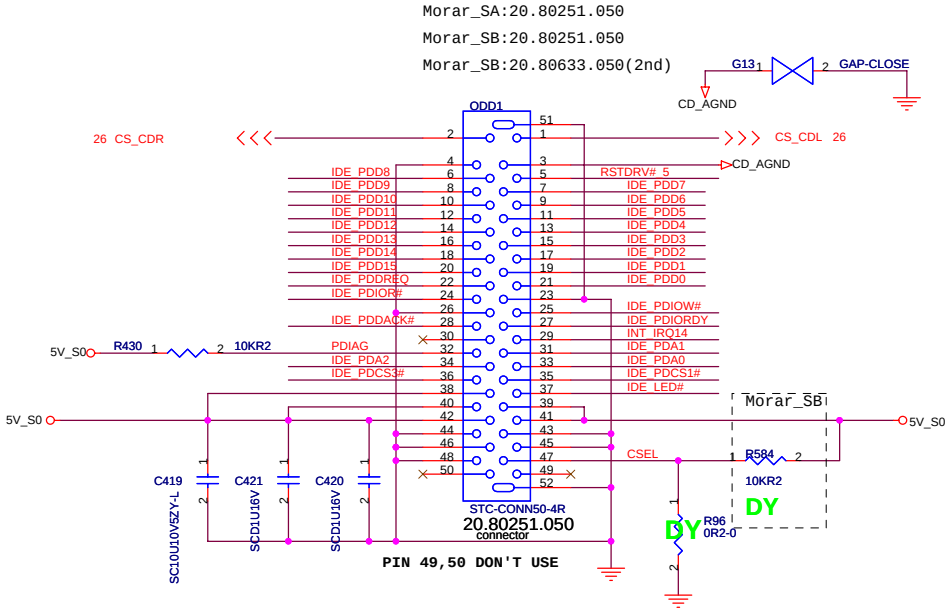
Date: Friday, June 24, 2005 | Sheet 18 of 40


Layout 15 mil
FAN1_VCC
C61 SCD1U16V
C73 SC10U10V5ZY-L
D9 BAT54-1
C72 SC2200P50V2KX
5V_S0
Morar_SB
R44 10KR2
C70 SC100P50V2JN-U
FAN1
FAN1_VCC
Layout 15 mil
connector
20.D0122.103
Morar_SA:20.D0122.103
Morar_SB:20.F0736.003
Layout 30 mil
R38 200R2F
C60 SCD1U16V
R37 4K99R2F
R39 49K9R2F
C63 SC4D7U10V5ZY
C71 SCD1U16V
C74 SCD1U16V
TP17
TPAD28
5V_G791_S0
U5
G792SFX
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC
DGND
SGND1
SGND2
SGND3
G791_32K 18
SMBD_G792 29
SMBC_G792 29
H_THERMDA
G792_DXP3
G792_DXP2
H_THERMDC
G792_DXN2
G792_DXN3
ALERT#
G792_THERM#
V_DEGREE
Setting T8 as 100 Degree
V_DEGREE =(((Degree-72)*0.02)+0.34)*VCC
3D3V_S0
R46 10KR2
ALERT#
R47 0R0402-PAD
THRM# 16
16 PWROK
R40 75KR2F
G792_RESET#
C62 SC2200P50V2KX
DY
R42 100KR2F
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
G7 GAP-CLOSE
G6 GAP-CLOSE
Morar_SB
C58 SC2200P50V2KX
C322 SC2200P50V2KX
SC470P50V2KX
C544
Q40 PMBS3904-1-GP
SC470P50V2KX
C389
Q31 PMBS3904-1-GP
System Sensor
System接第二組,VGA接第三組
C59 SC2200P50V2KX
H_THERMDA 4
H_THERMDC 4
Morar_SB
HW thermal shut down tempature setting 95 degree . Put Near CPU .
5V_AUX_S5
R28 150R2F
DY
C21 SCD1U16V
U4
G709T1U
SET
GND
OUT#
VCC
HYST
R34 18KR2F
CPU_THSET
T8_HW_SHUT#
CPU_TH_HYST
R29 0R2-0
R30 0R2-0
3D3V_AUX_S5
Morar_SB
MAX6326UR29-T-U
U61
RESET#
VCC
GND
R591 0R2-0
R250 10KR2
D23 BAT54-1
C244 SCD1U16V
(dummy, KBC already delay)
D24 RB751V-40-U
R251 0R2-0
INTRUDER# 15
RSMRST# 29
29 S5_ENABLE
R565 100KR2F
U19
NC7S08-U
A
B
GND
VCC
Y
3D3V_AUX_S5
S5PWR_ENABLE 35
R562 0R2-0
Morar_SB
T8_HW_SHUT#
Morar_SB
4,15 H_PWRGD
R208 330R2
Q17 CHT2222A
C213 SCD1U16V
PM_THRMTRIP-I# 4,15
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size Custom
Document Number MORAR
Rev SB
Date: Saturday, May 28, 2005
Sheet 19 of 40

HDD Connector

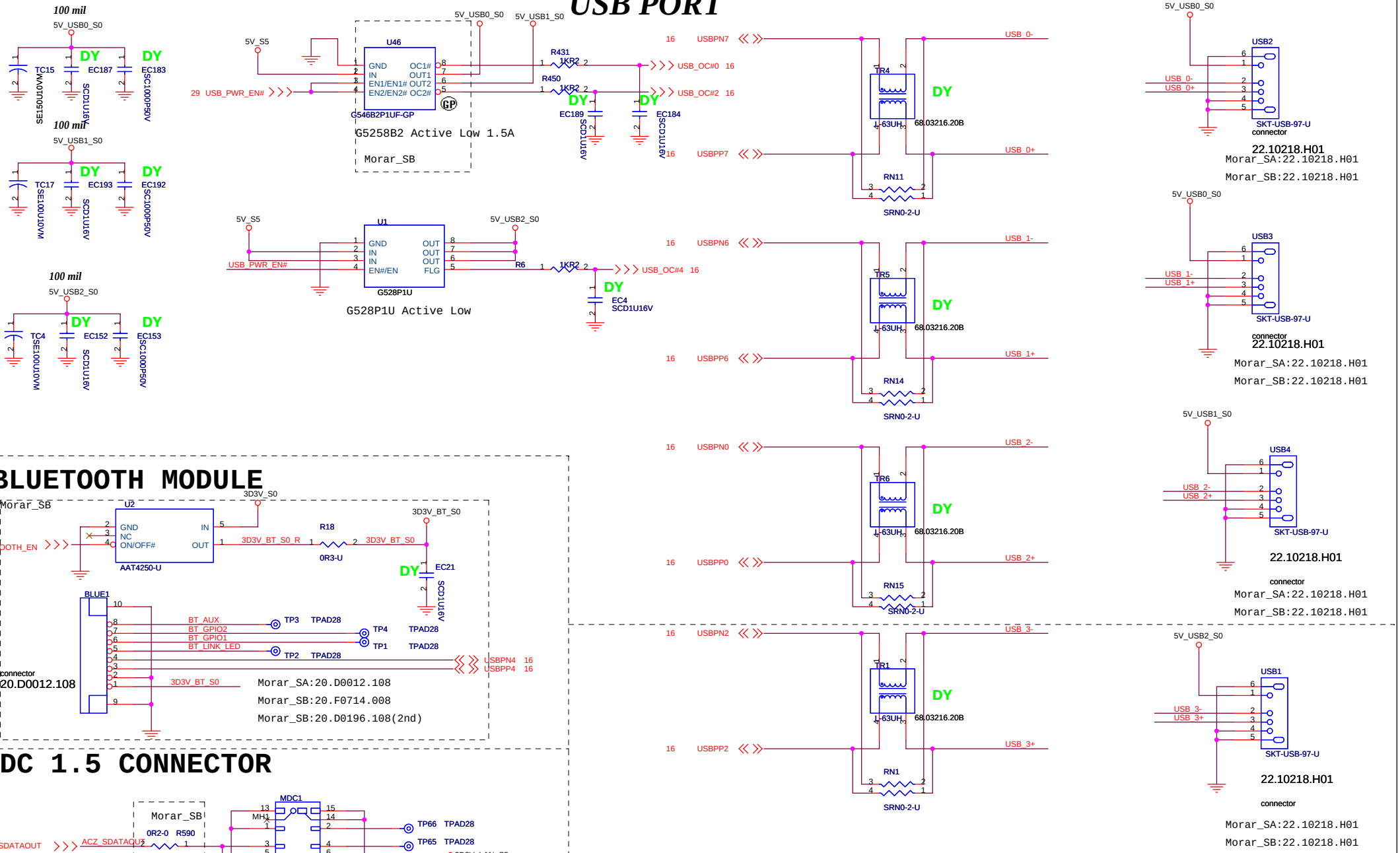


CD-ROM Connector



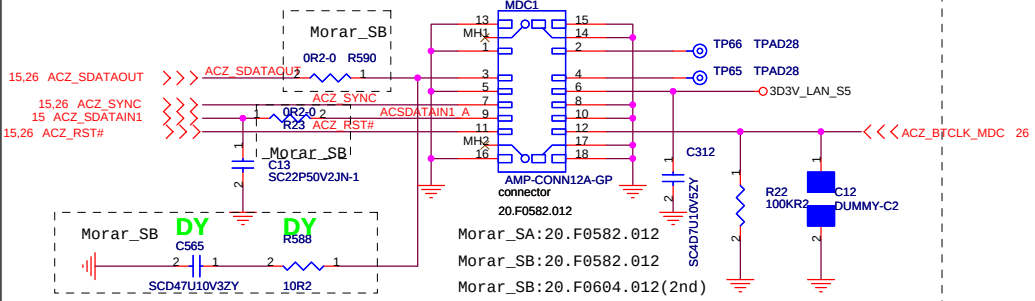
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD and CDROM		
Size: A3	Document Number: MORAR	Rev: SB
Date: Saturday, May 28, 2005	Sheet 20 of 40	

USB PORT

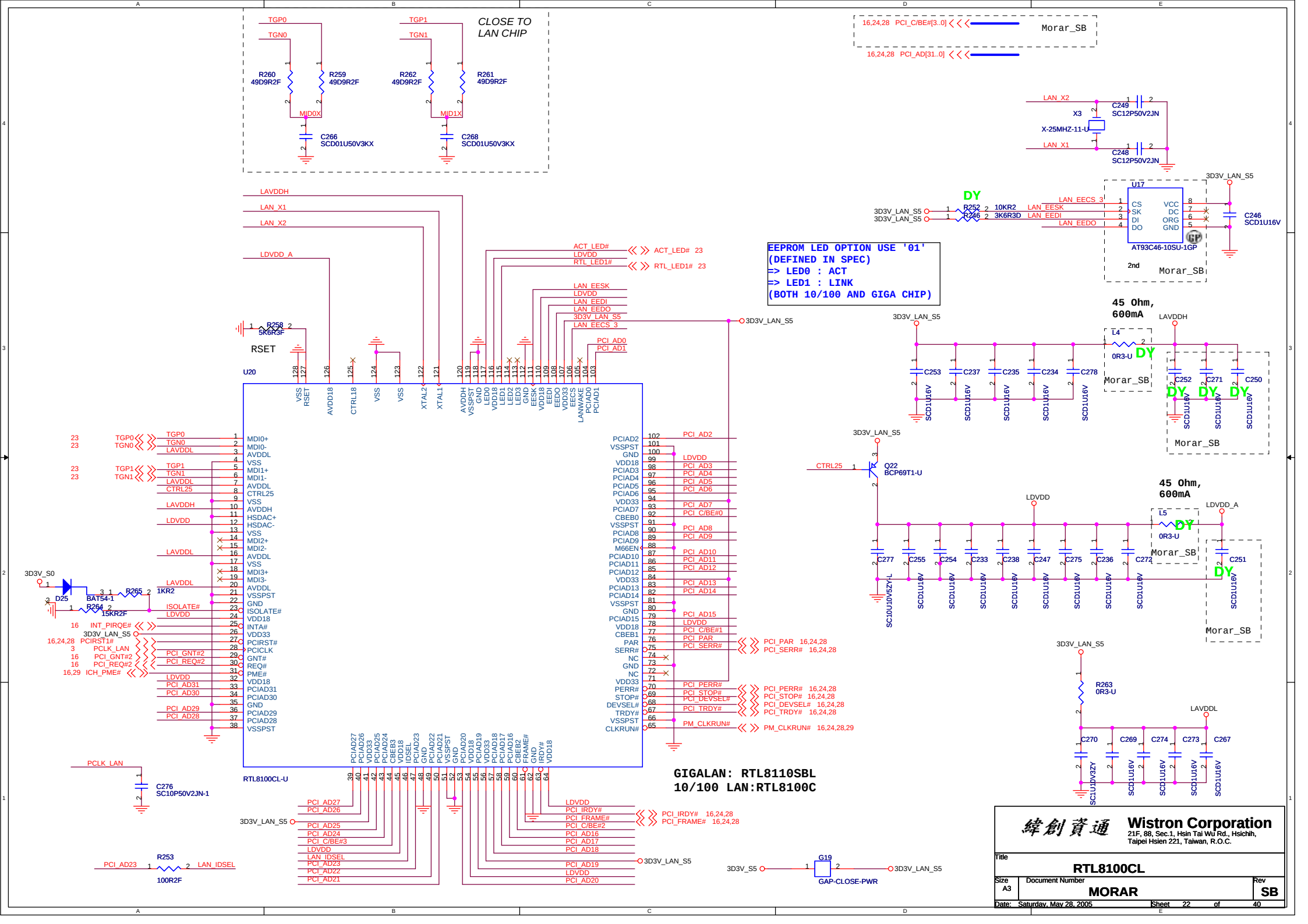


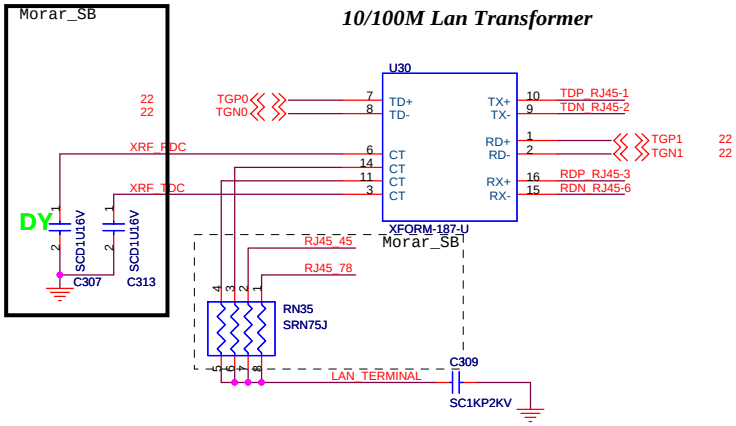
BLUETOOTH MODULE

MDC 1.5 CONNECTOR

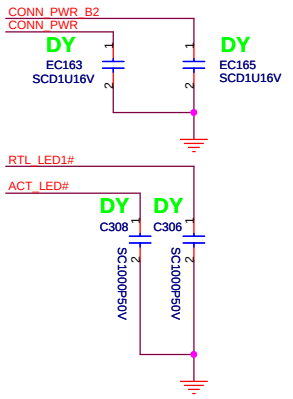


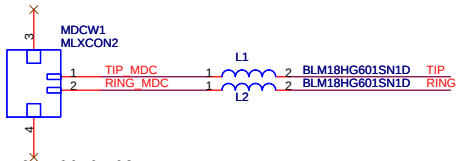
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB / MDC / BLUETOOTH**	
Size A3	Document Number **MORAR**	Rev **SB**
Date: Saturday, May 28, 2005	Sheet 21 of 40	


CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
R260 49D9R2F
R259 49D9R2F
R262 49D9R2F
R261 49D9R2F
MID0X
MID1X
C266 SCD01U50V3KX
C268 SCD01U50V3KX
16,24,28 PCI_C/BE#[3..0]
16,24,28 PCI_AD[31..0]
Morar_SB
LAN_X2
X3
X-25MHZ-11-U
LAN_X1
C249 SC12P50V2JN
C248 SC12P50V2JN
U17
AT93C46-10SU-1GP
2nd
3D3V_LAN_S5
DY
R252 10KR2
R246 3K6R3D
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
C246 SCD1U16V
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
45 Ohm, 600mA
L4
0R3-U
LAVDDH
C253 C237 C235 C234 C278
C252 C271 C250
SCD1U16V
LAVDD
LDVDD
LDVDD_A
L5
Q22 BCP69T1-U
CTRL25
C277 C255 C254 C233 C238 C247 C275 C236 C272
C251
SC10U10V5ZY-L
R263 0R3-U
C270 C269 C274 C273 C267
SC1U10V3ZY
LAVDDH
LAN_X1
LAN_X2
LDVDD_A
RSET
R258 5K6R3F
U20
RTL8100CL-U
ACT_LED#
RTL_LED1#
PCI_AD0
PCI_AD1
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
HSDAC+
HSDAC-
ISOLATE#
INT_PIRQE#
PCIRST#
PCICLK
GNT#
REQ#
PME#
PCIAD31
PCIAD30
PCIAD29
PCIAD28
PCIAD27
PCIAD26
PCIAD25
PCIAD24
PCIAD23
PCIAD22
PCIAD21
PCIAD20
PCIAD19
PCIAD18
PCIAD17
PCIAD16
PCIAD15
PCIAD14
PCIAD13
PCIAD12
PCIAD10
PCIAD2
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_C/BE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_C/BE#1
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN#
PCI_C/BE#2
PCI_FRAME#
PCI_IRDY#
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
LAN_IDSEL
R253 100R2F
D25 BAT54-1
R265 1KR2
R264 15KR2F
3D3V_S0
C276 SC10P50V2JN-1
PCLK_LAN
G19 GAP-CLOSE-PWR
3D3V_S5
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8100CL
Size A3
Document Number MORAR
Rev SB
Date: Saturday, May 28, 2005
Sheet 22 of 40



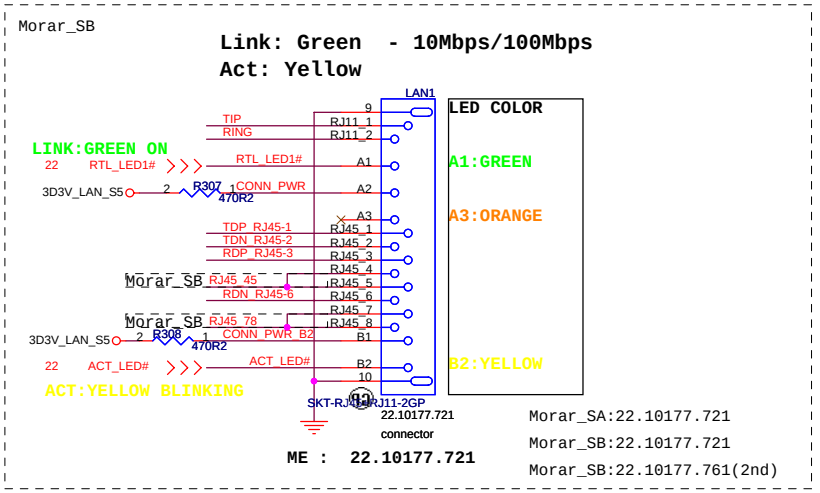
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.





21.D0010.102
connector

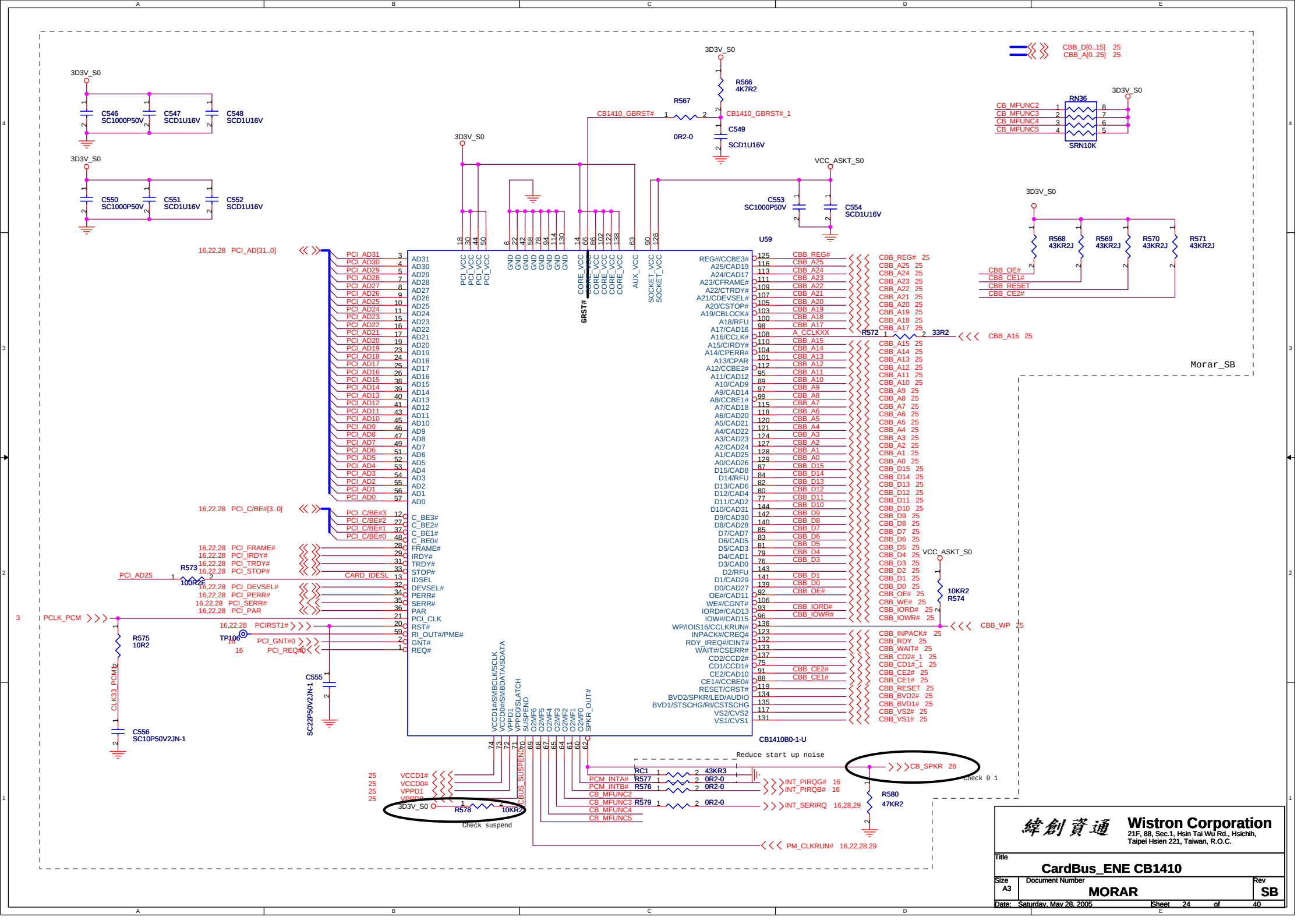
Morar_SA:21.D0010.102
Morar_SB:20.F0714.002
Morar_SB:20.D0196.102(2nd)



Morar_SA:22.10177.721
Morar_SB:22.10177.721
Morar_SB:22.10177.761(2nd)

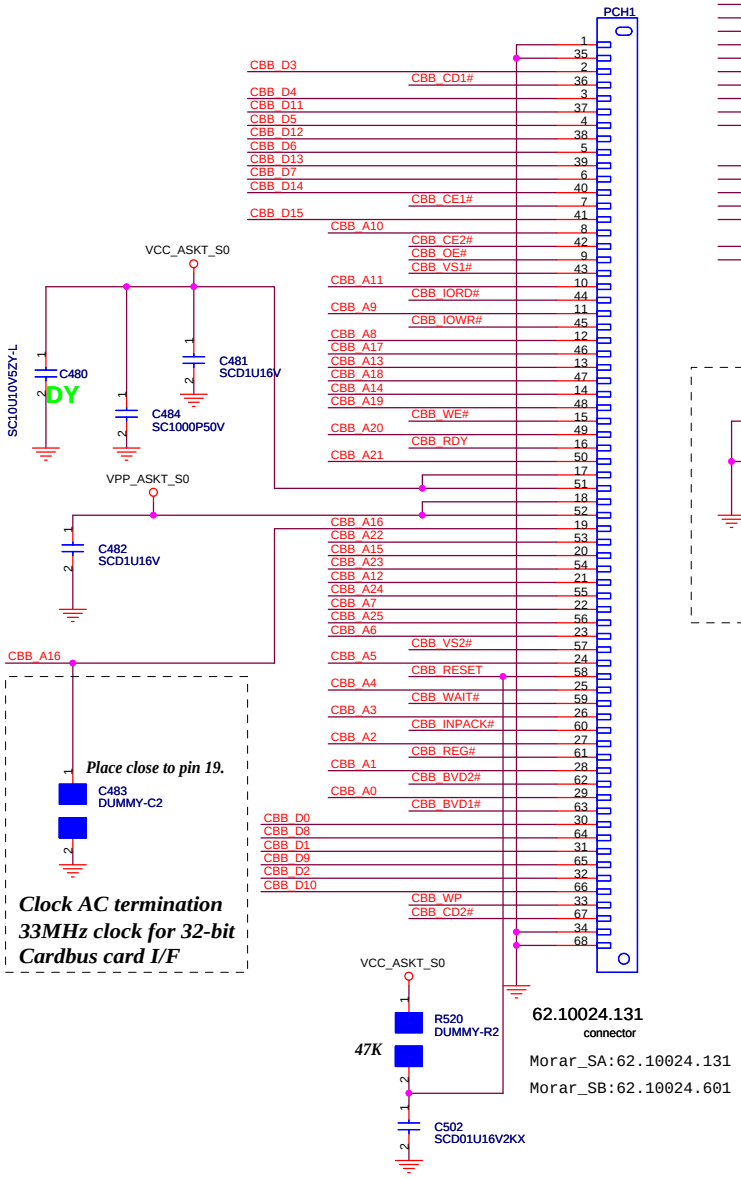
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number MORAR	Rev SB
Date: Saturday, May 28, 2005	Sheet 23 of 40	



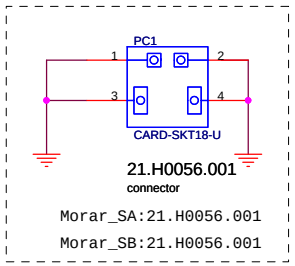
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CardBus_ENE CB1410**	
Size A3	Document Number **MORAR**	Rev **SB**
Date: Saturday, May 28, 2005	Sheet 24 of 40	

PCMCIA Socket

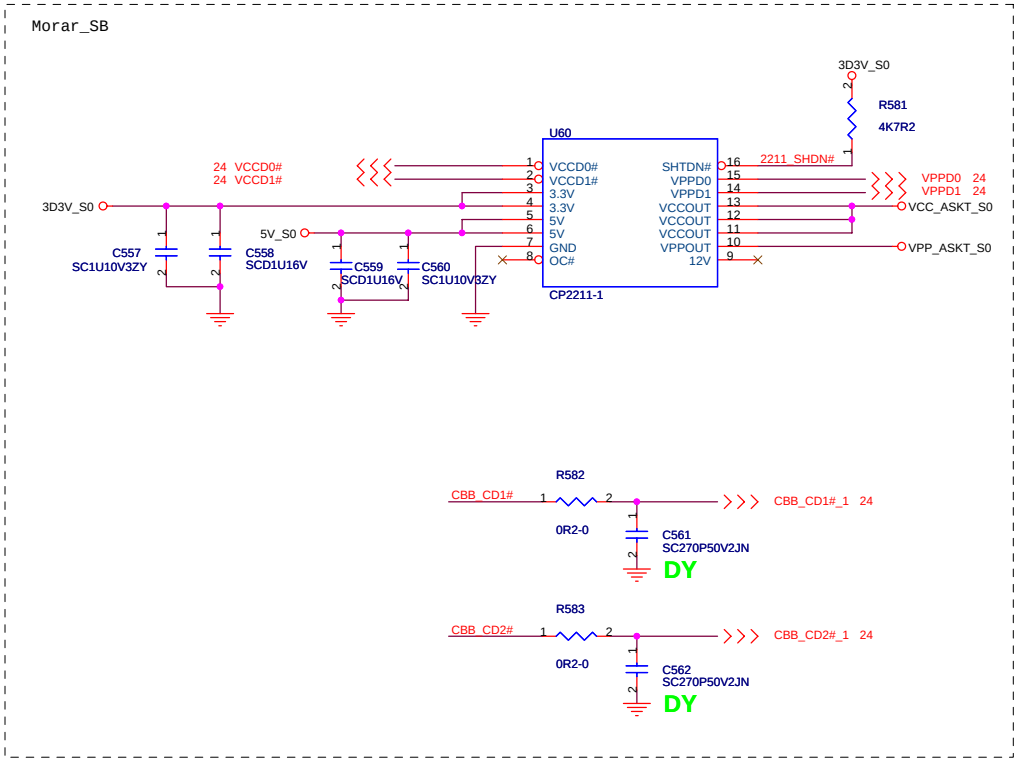


Cardbus I/F

CBB_D[0..15] 24
CBB_A[0..25] 24
CBB_IORD# 24
CBB_IOWR# 24
CBB_OE# 24
CBB_WE# 24
CBB_REG# 24
CBB_RDY 24
CBB_WP 24
CBB_RESET 24
CBB_WAIT# 24
CBB_INPACK# 24
CBB_CE1# 24
CBB_CE2# 24
CBB_BVD1# 24
CBB_BVD2# 24
CBB_VS1# 24
CBB_VS2# 24

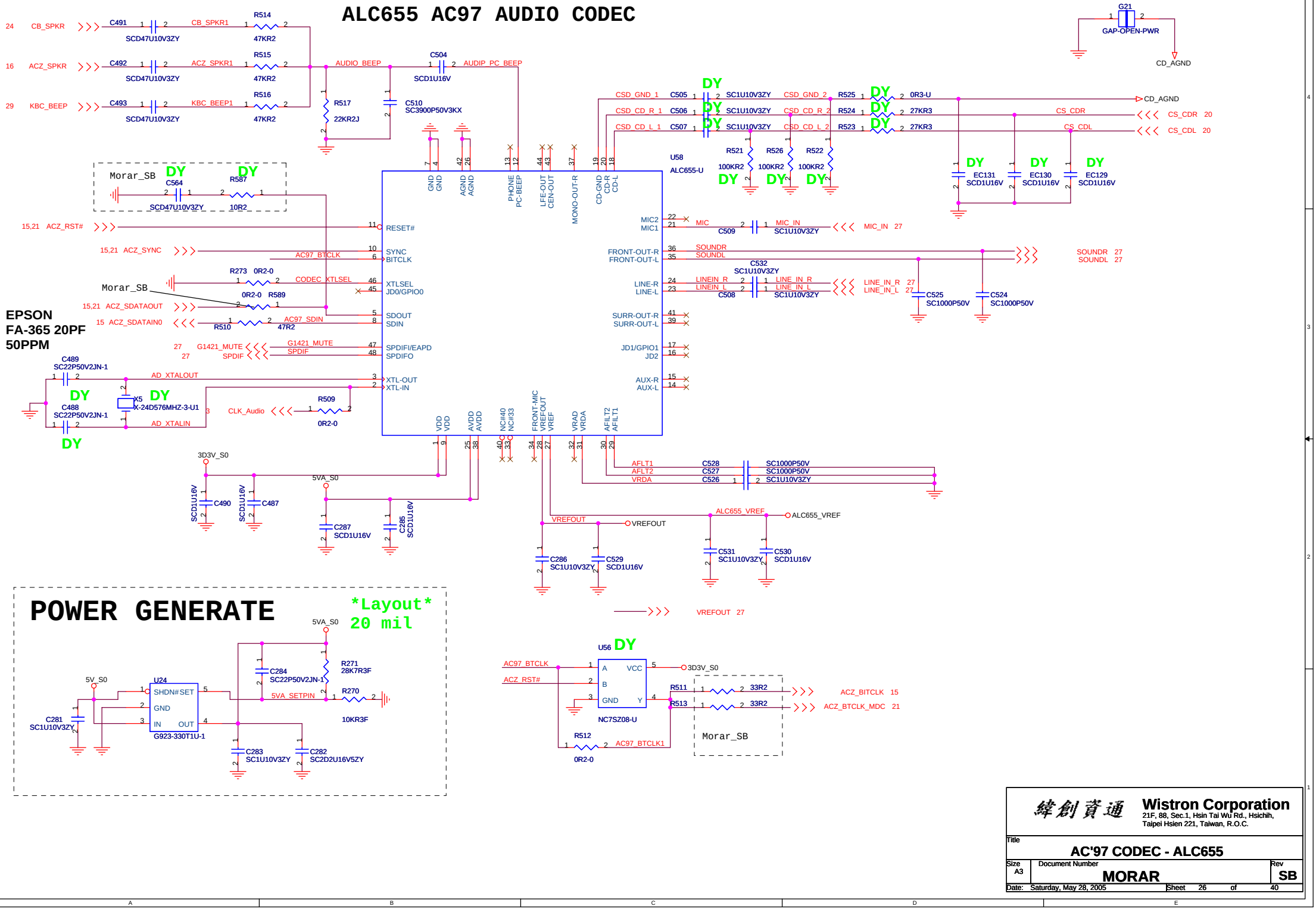


Power switch



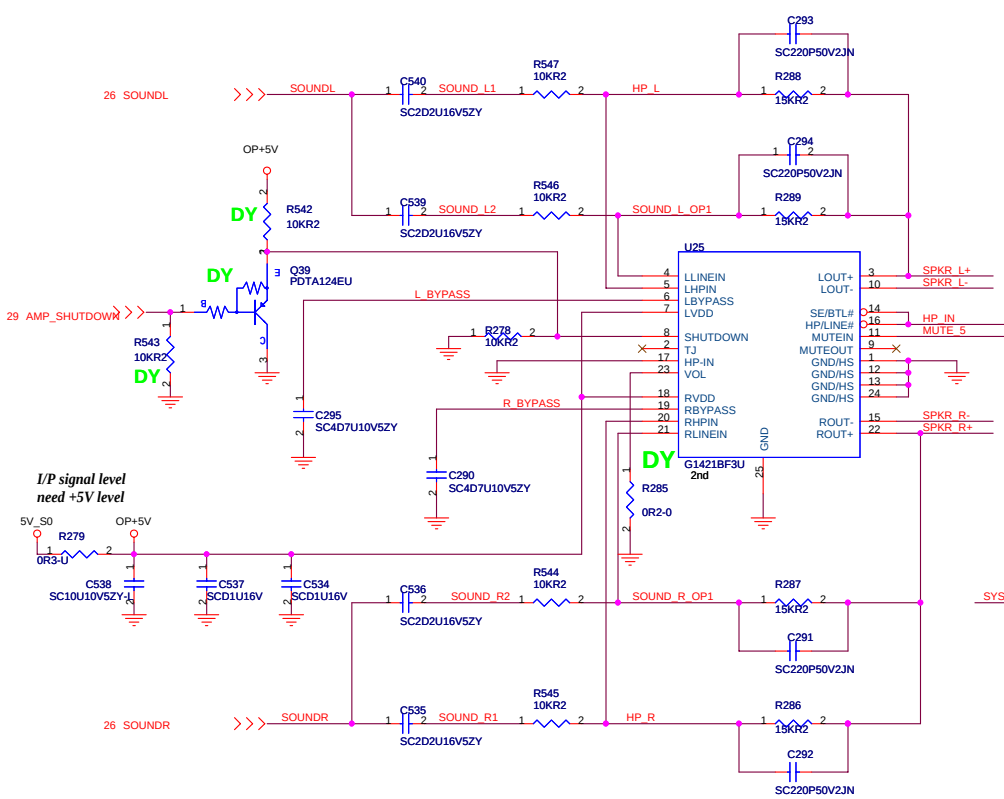
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCMCA	
Size A3	Document Number MORAR	Rev SB
Date: Saturday, May 28, 2005	Sheet 25 of 40	

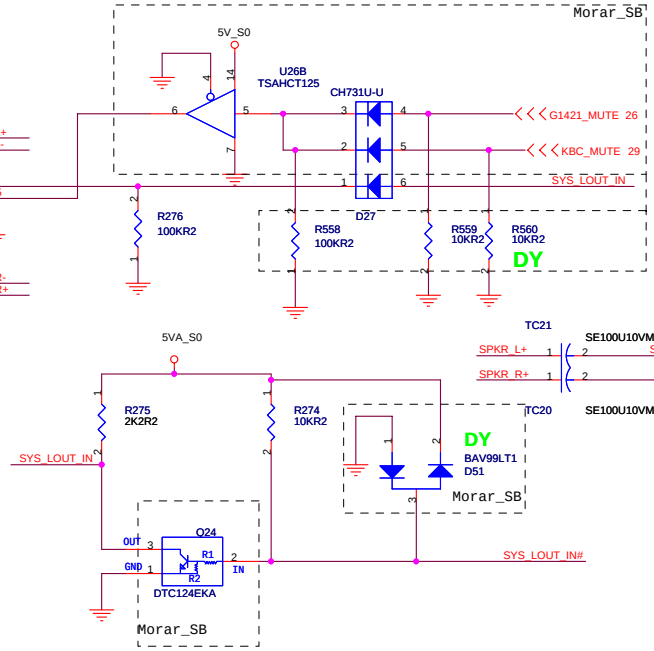
ALC655 AC97 AUDIO CODEC

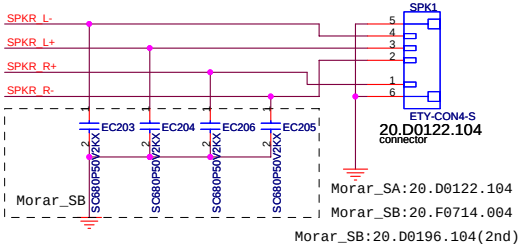


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AC'97 CODEC - ALC655	
Size: A3	Document Number: MORAR
Rev: SB	
Date: Saturday, May 28, 2005	Sheet 26 of 40

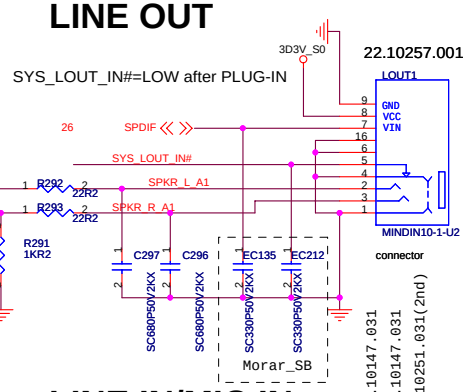
AUDIO OP AMPLIFIER



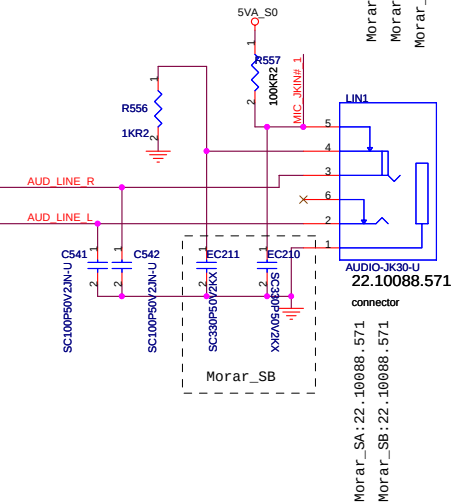


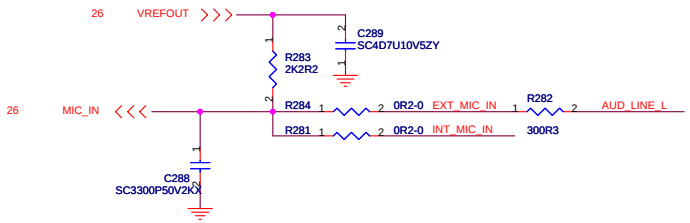


LINE OUT

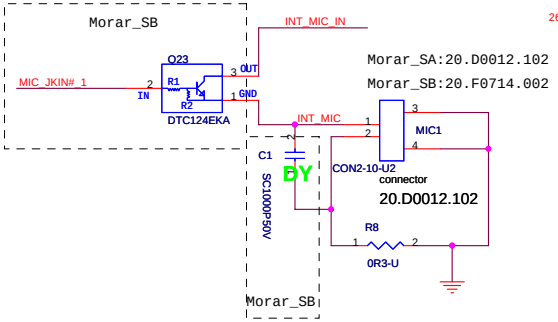


LINE IN/MIC IN





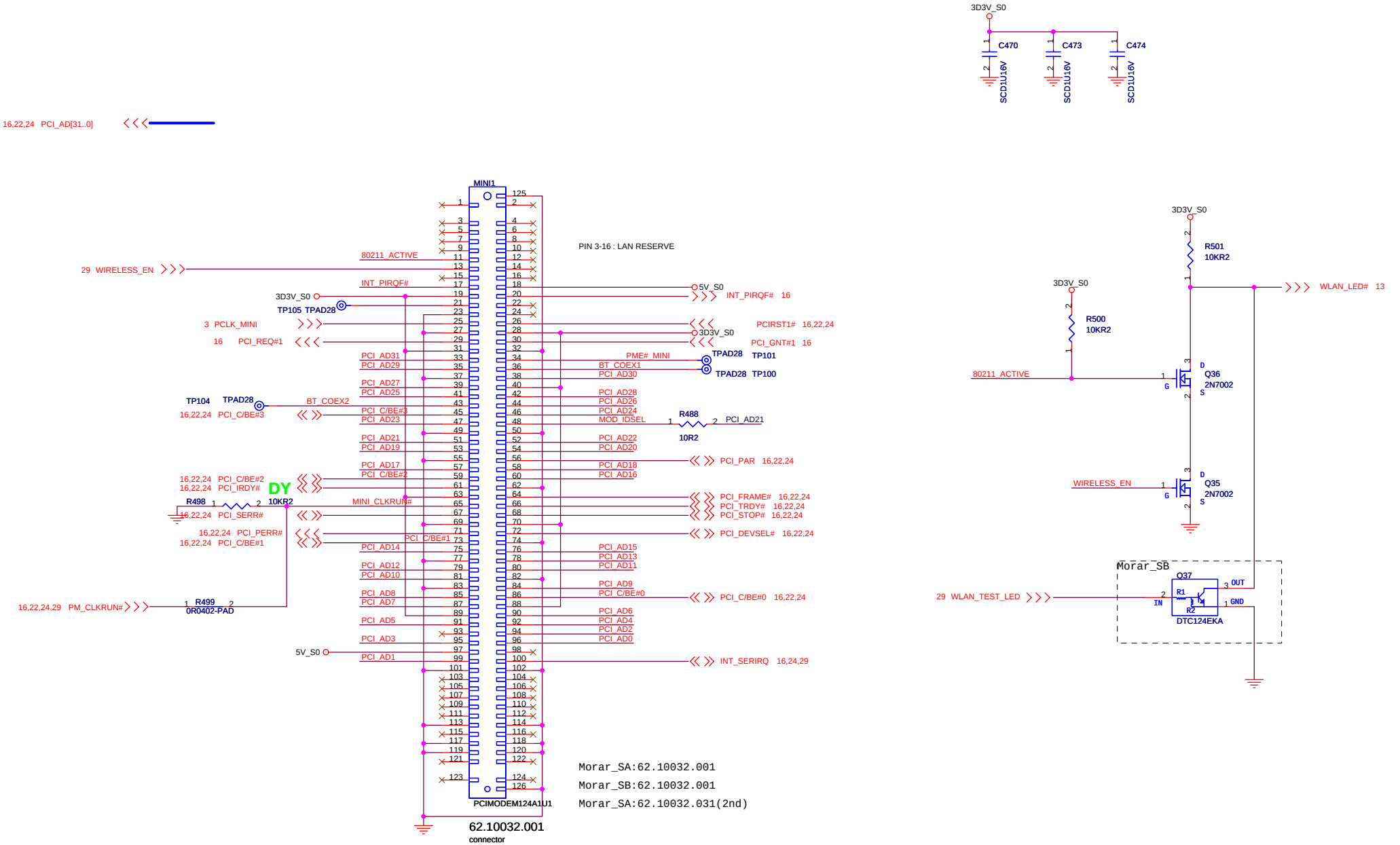
Internal Mic



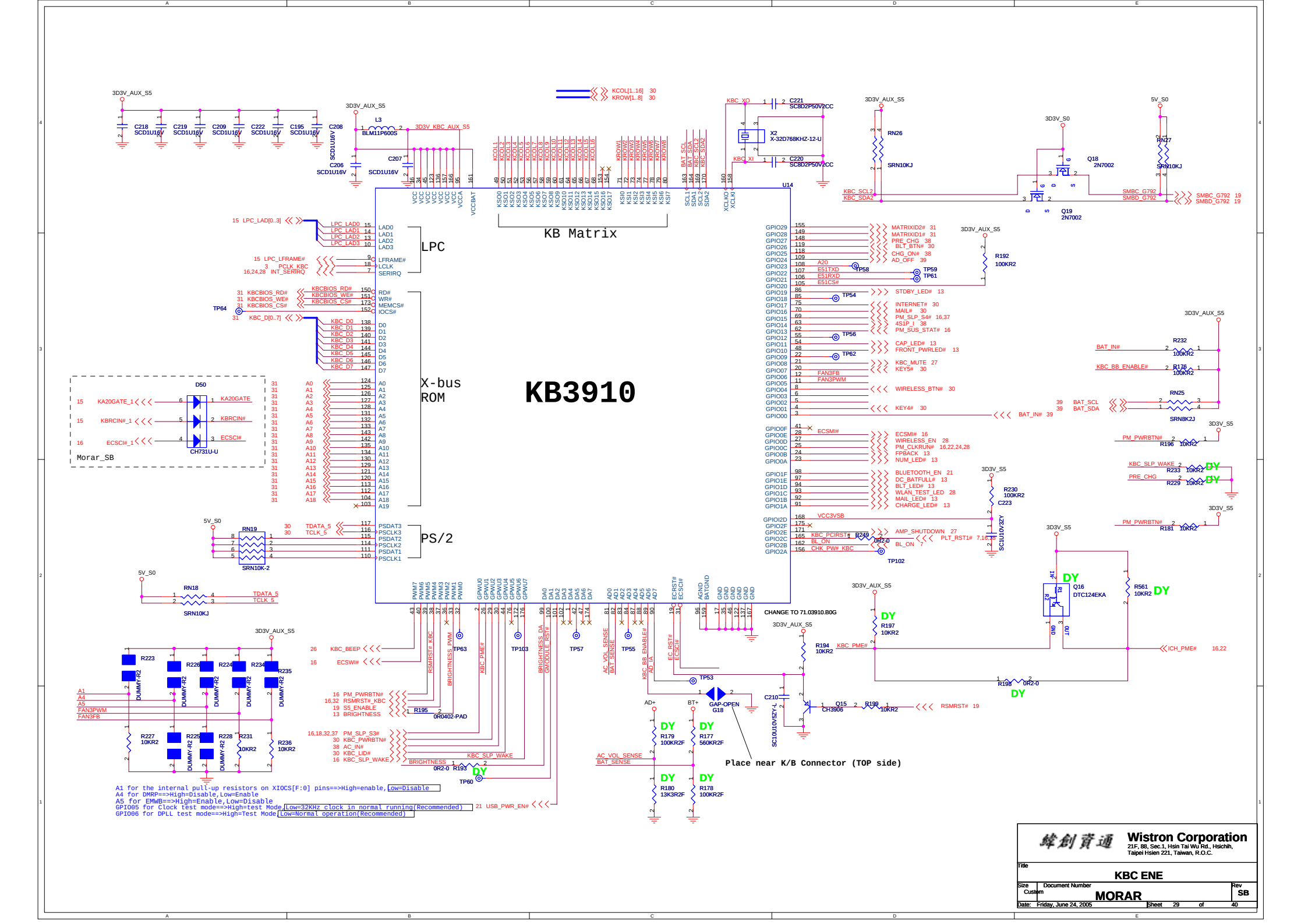
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

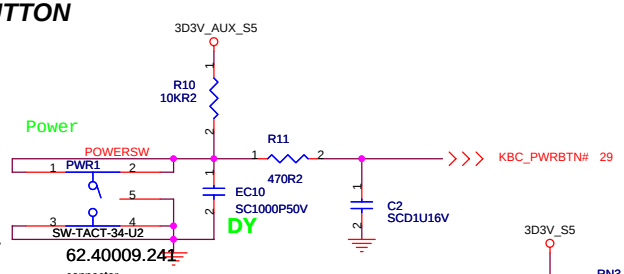
Title	Audio AMP and Jack	
Size	Document Number: MORAR	Rev: SB
Date: Saturday, May 28, 2005	Sheet 27 of 40	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number **MORAR**	Rev **SB**
Date: Saturday, May 28, 2005	Sheet 28 of 40	

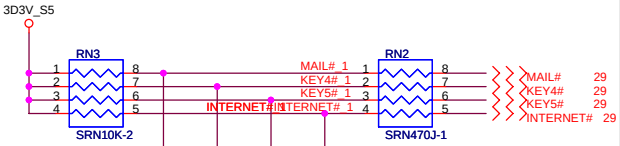

KB3910
KB Matrix
LPC
X-bus ROM
PS/2
Morar_SB
Place near K/B Connector (TOP side)
CHANGE TO 71.03910.B0G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ENE
MORAR
Date: Friday, June 24, 2005
Sheet 29 of 40

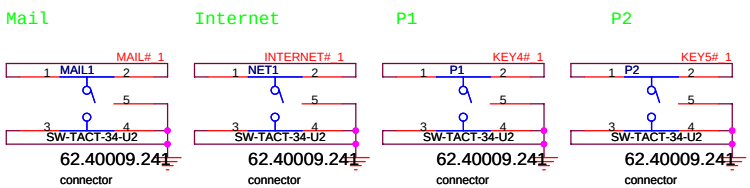
POWER BUTTON

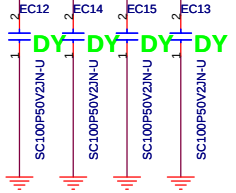


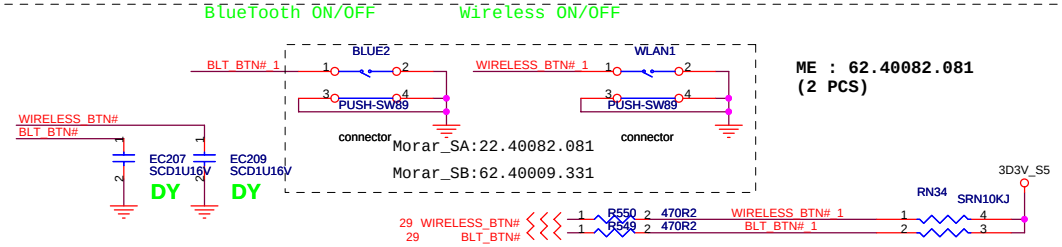
ME : 62.40009.241
(ALL 11 PCS)

Buttons



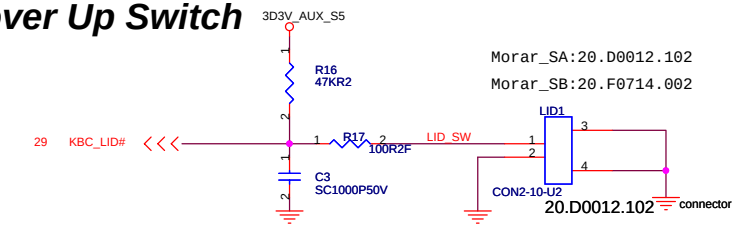




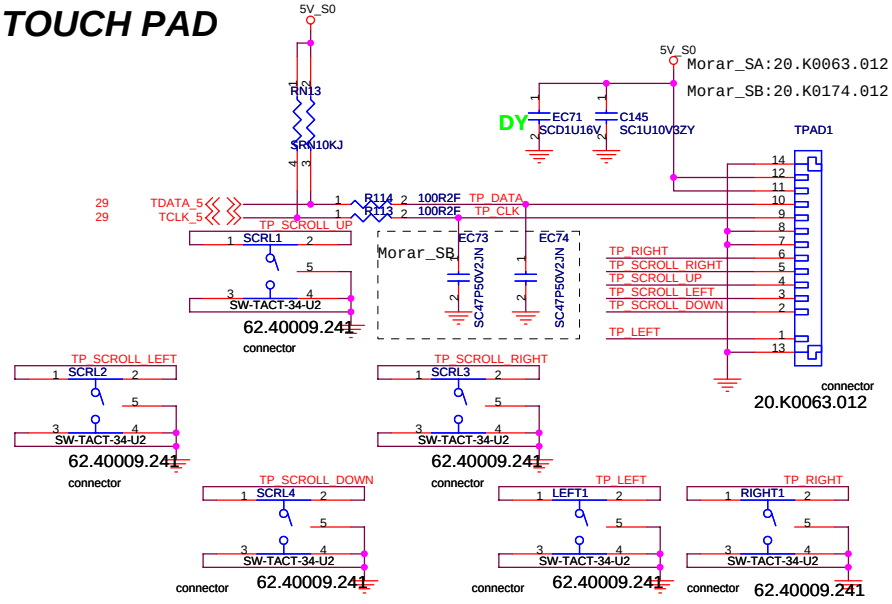


ME : 62.40082.081
(2 PCS)

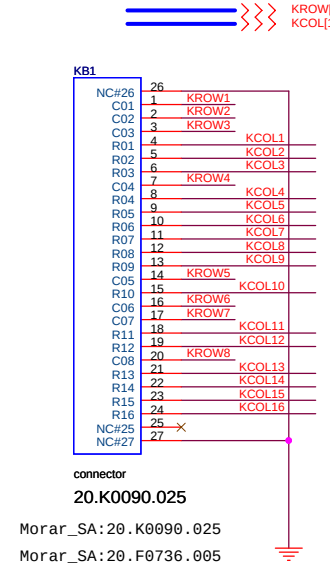
Cover Up Switch



TOUCH PAD

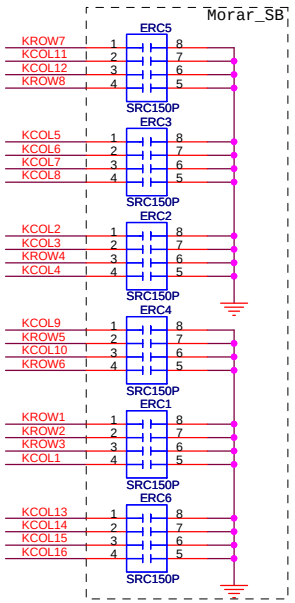


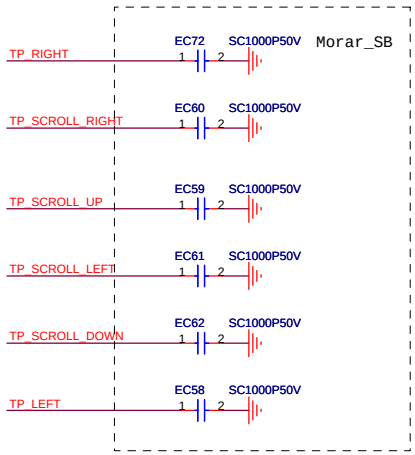
Internal KeyBoard CONN



Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.





緯創資通 Wistron Corporation
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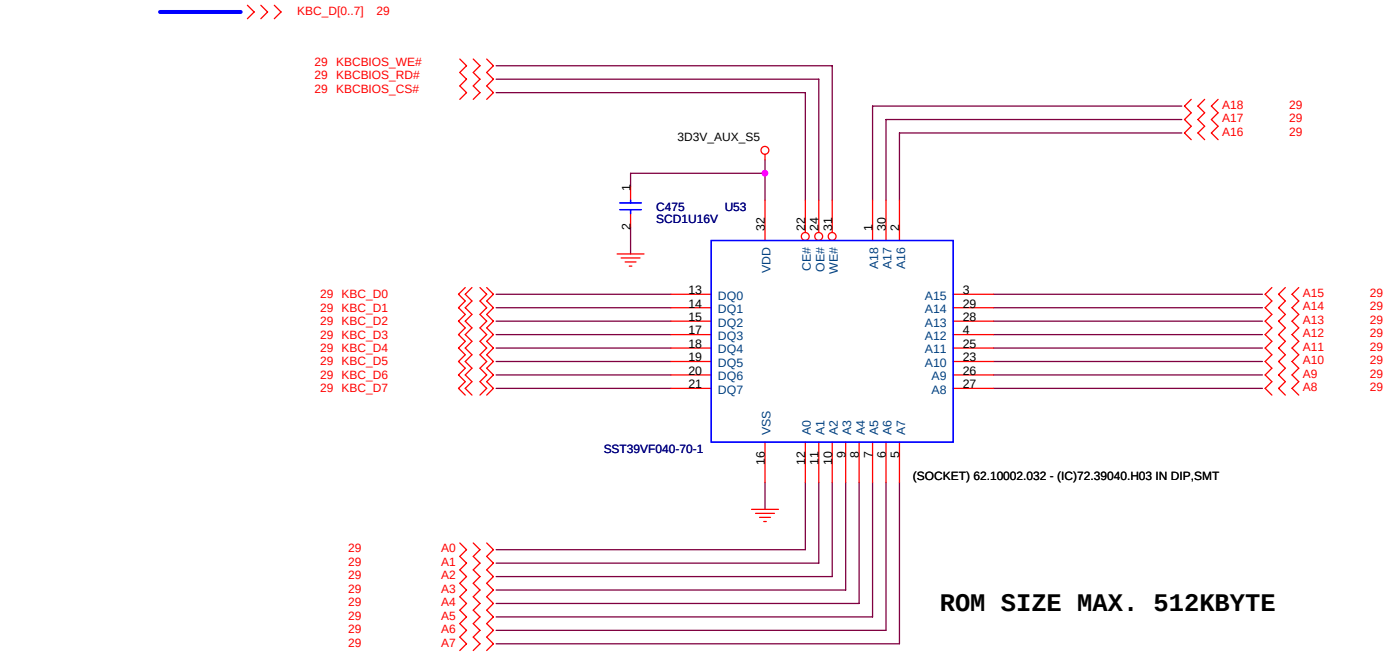
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

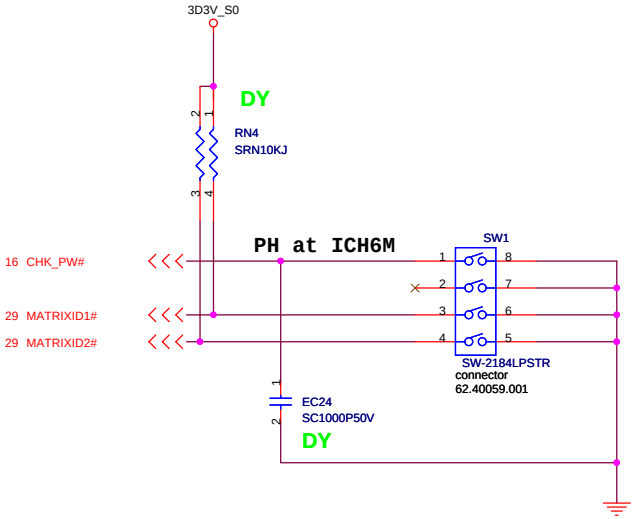
Size	Document Number	Rev
A3	MORAR	SB

Date: Saturday, May 28, 2005 Sheet 30 of 40



ROM SIZE MAX. 512KBYTE

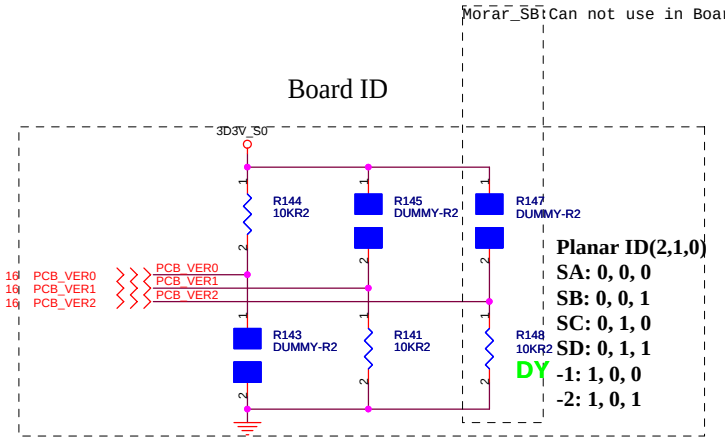
PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

Morar_SB:Can not use in Board ID



Planar ID(2,1,0)
SA: 0, 0, 0
SB: 0, 0, 1
SC: 0, 1, 0
SD: 0, 1, 1
-1: 1, 0, 0
-2: 1, 0, 1

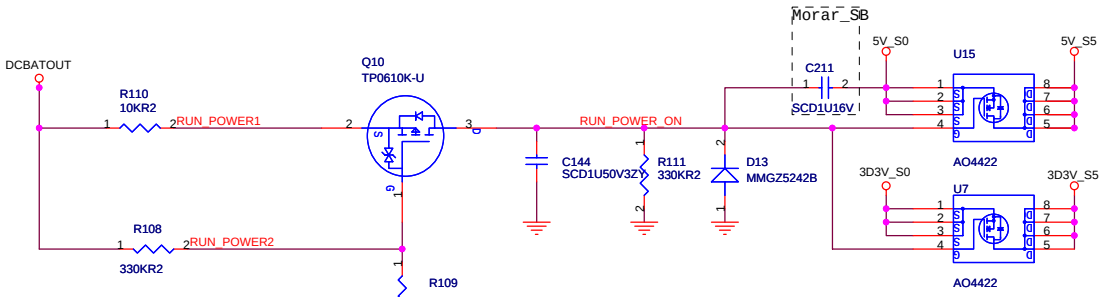
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

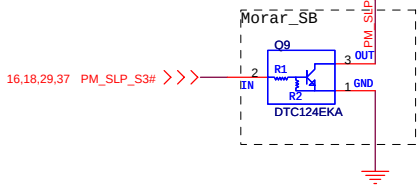
Title: **BIOS ROM**

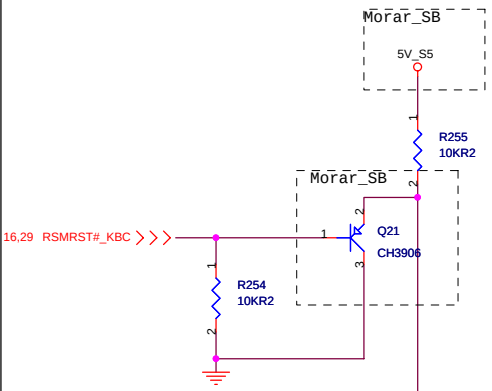
Size: A3 | Document Number: **MORAR** | Rev: **SB**

Date: Saturday, May 28, 2005 | Sheet 31 of 40

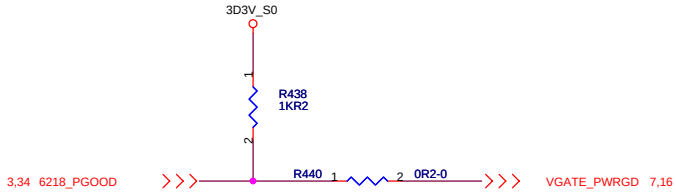
Run Power



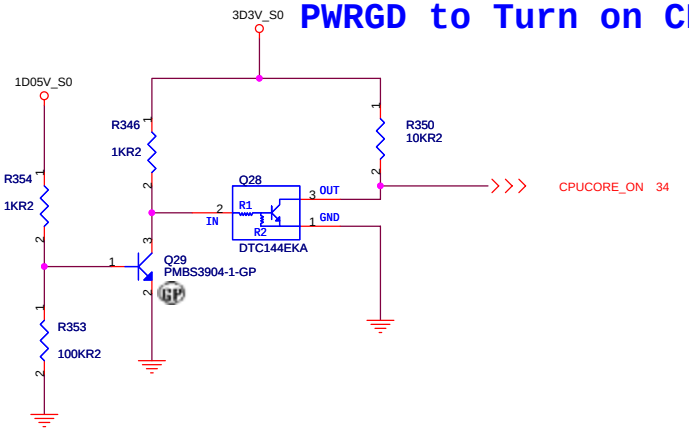




PWRGD for NB and SB

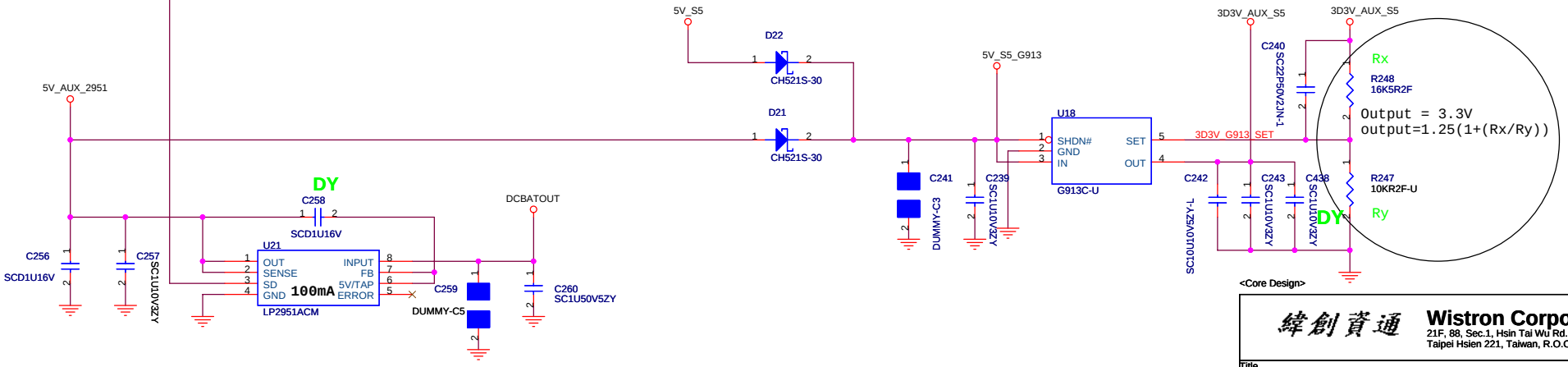


PWRGD to Turn on CPU_Core_Power



Aux Power

3D3V_AUX_S5



<Core Design>

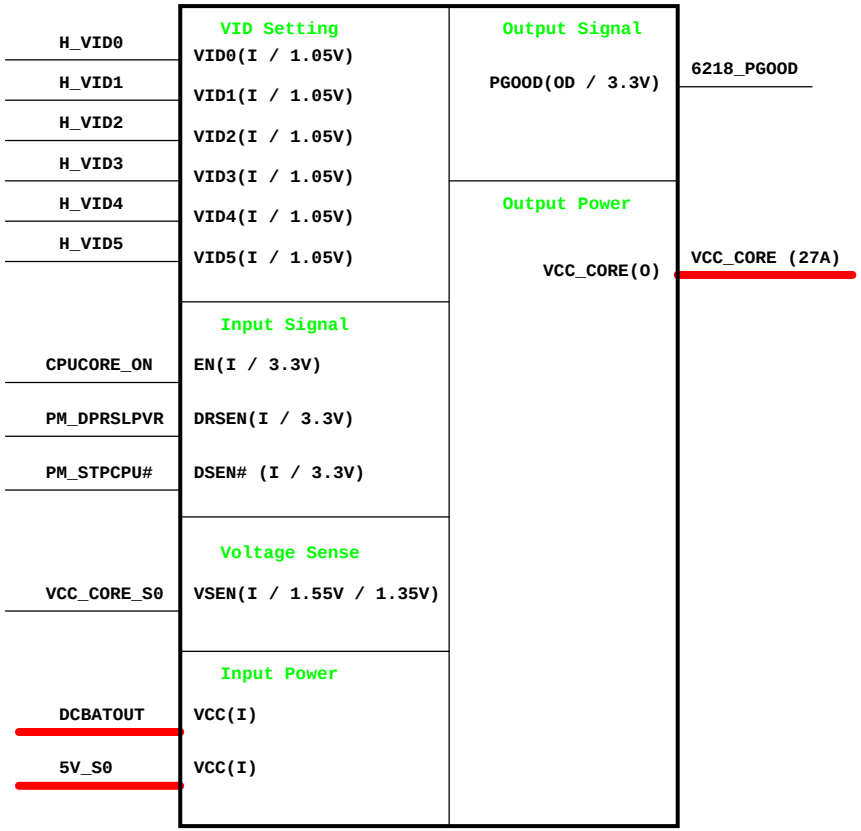
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RUN POWER and 3D3V_AUX_S5***

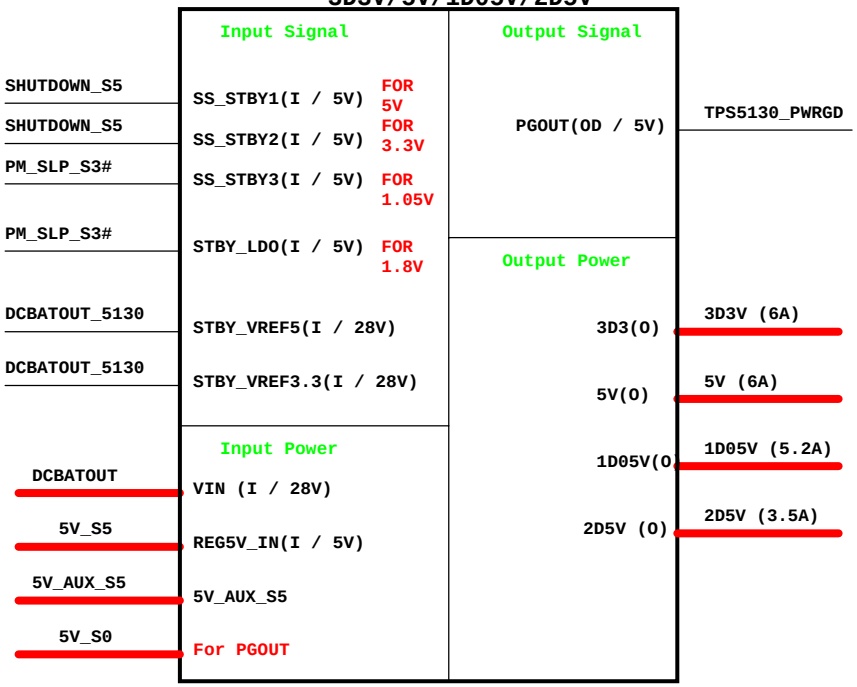
Size	Document Number	Rev
A3	MORAR	SB

Date: Saturday, May 28, 2005 Sheet 32 of 40

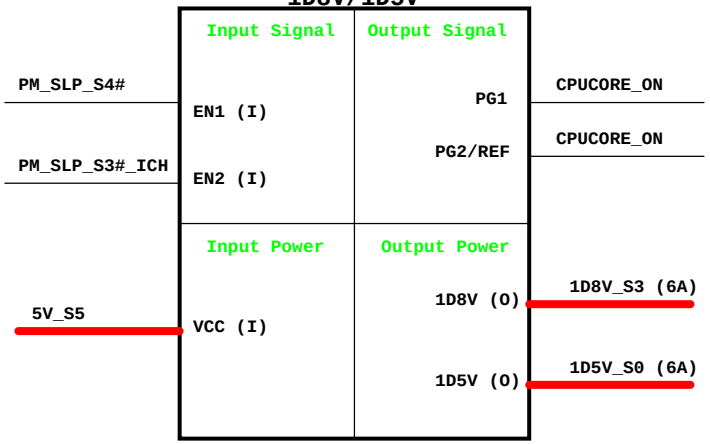
CPU_CORE ISL6218CV



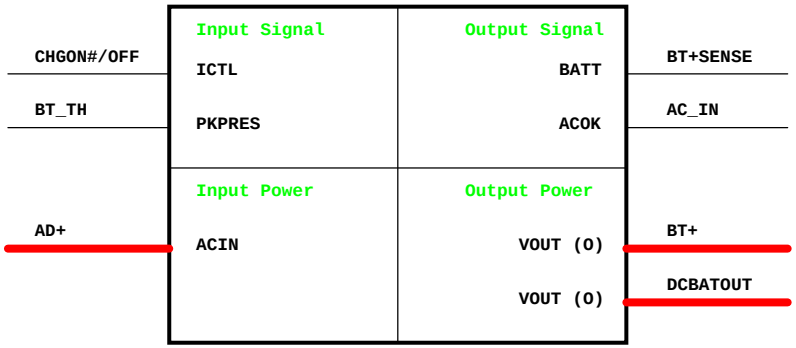
TPS5130 3D3V/5V/1D05V/2D5V



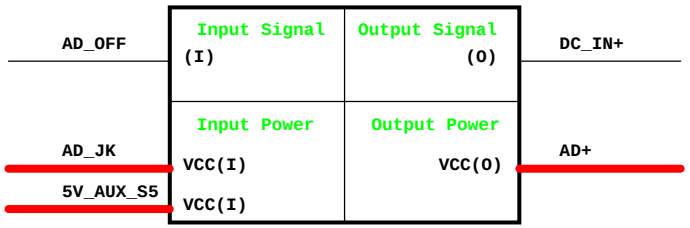
ISL6227 1D8V/1D5V



Charger Max8725



Adapter



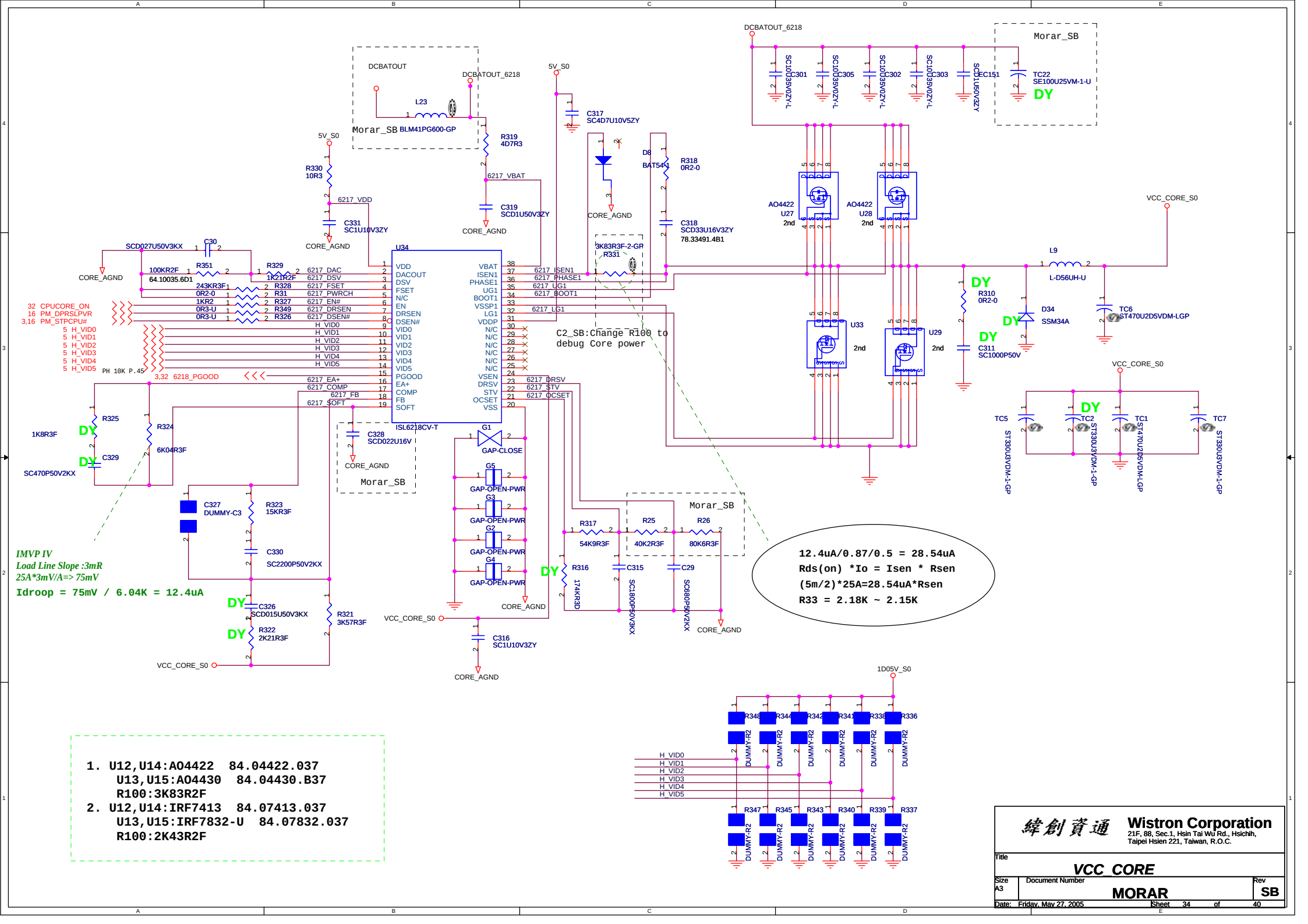
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Diagram**

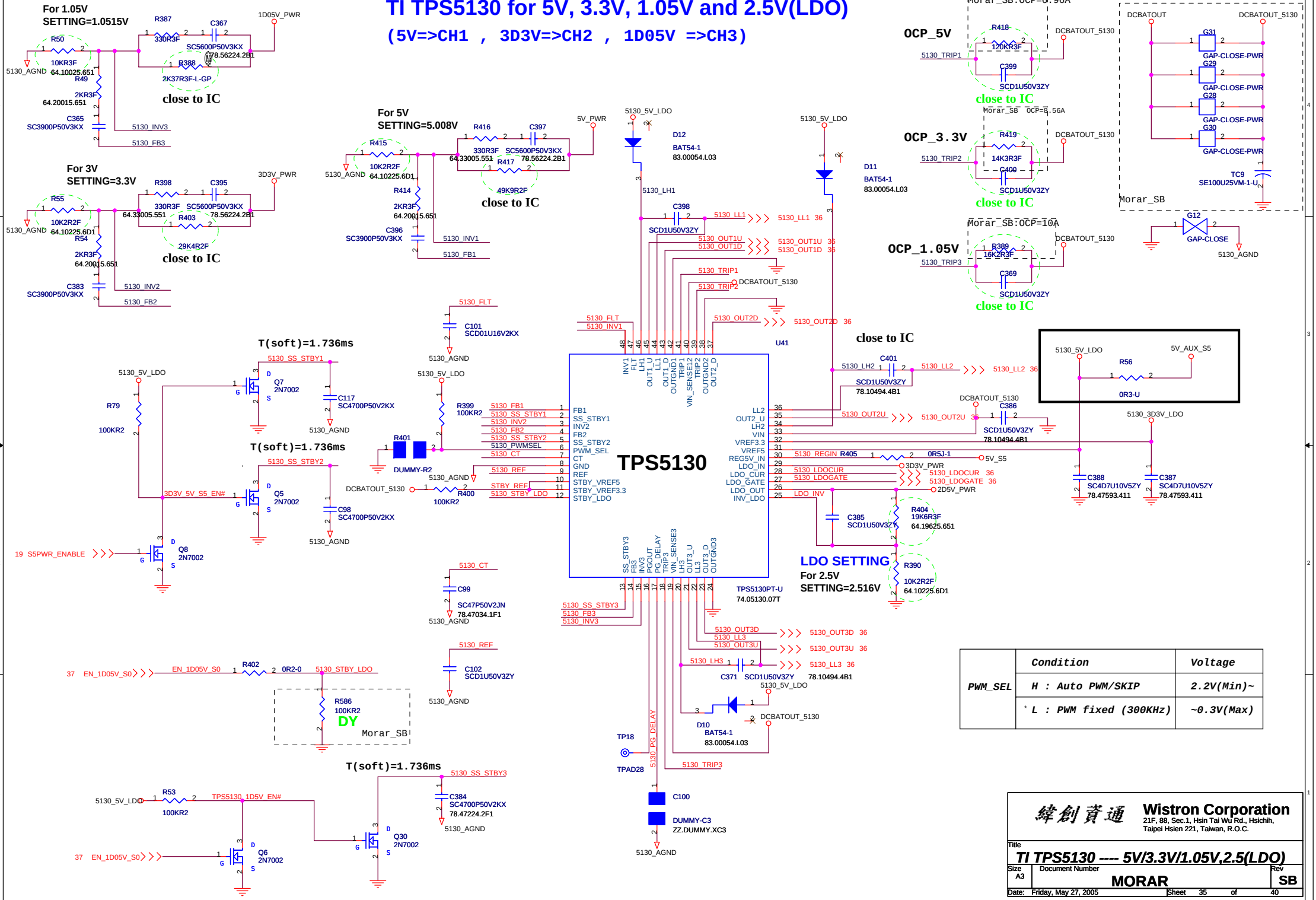
Size	Document Number	Rev
A3	MORAR	SB

Date: Friday, June 24, 2005 Sheet 33 of 40


DCBATOUT_6218
Morar_SB
DCBATOUT
L23
Morar_SB BLM41PG600-GP
5V_S0
R319 4D7R3
R330 10R3
6217_VBAT
6217_VDD
C319 SCD1U50V3ZY
C331 SC1U10V3ZY
CORE_AGND
C317 SC4D7U10V5ZY
D8 BAT54-1
R318 0R2-0
C318 SCD33U16V3ZY 78.33491.4B1
3K83R3F-2-GR R331
AO4422 U27 2nd
AO4422 U28 2nd
U33 2nd
U29 2nd
SC10U35V2ZY-L C301
SC10U35V2ZY-L C305
SC10U35V2ZY-L C302
SC10U35V2ZY-L C303
SC1U50V2ZY C151
TC22 SE100U25VM-1-U
DY
VCC_CORE_S0
L9 L-D56UH-U
R310 0R2-0
D34 SSM34A
TC6 ST470U2D5VDM-LGP
SC1000P50V C311
TC5 ST330U3VDM-1-GP
TC2 ST330U3VDM-1-GP
TC1 ST470U2D5VDM-LGP
TC7 ST330U3VDM-1-GP
U34
ISL6218CV-T
VDD DACOUT DSV FSET N/C EN DRSEN DSEN# VID0 VID1 VID2 VID3 VID4 VID5 PGOOD EA+ COMP FB SOFT
VBAT ISEN1 PHASE1 UG1 BOOT1 VSSP1 LG1 VDDP N/C N/C N/C N/C N/C N/C VSEN DRSV STV OCSET VSS
6217_ISEN1 6217_PHASE1 6217_UG1 6217_BOOT1 6217_LG1 6217_DRSV 6217_STV 6217_OCSET
SCD027U50V3KX C30
100KR2F R351
64.10035.6D1
R329 1K21R2F
243KR3F R328
0R2-0 R31
1KR2 R327
0R3-U R349
0R3-U R326
6217_DAC 6217_DSV 6217_FSET 6217_PWRCH 6217_EN# 6217_DRSEN 6217_DSEN#
32 CPUCORE_ON
16 PM_DPRSLPVR
3,16 PM_STPCPU#
5 H_VID0
5 H_VID1
5 H_VID2
5 H_VID3
5 H_VID4
5 H_VID5
PH 10K P.45
3,32 6218_PGOOD
6217_EA+
6217_COMP
6217_FB
6217_SOFT
C328 SCD022U16V
R325 1K8R3F
R324 6K04R3F
C329 SC470P50V2KX
C327 DUMMY-C3
R323 15KR3F
C330 SC2200P50V2KX
C326 SCD015U50V3KX
R322 2K21R3F
R321 3K57R3F
C316 SC1U10V3ZY
G1 GAP-CLOSE
G5 GAP-OPEN-PWR
G3 GAP-OPEN-PWR
G2 GAP-OPEN-PWR
G4 GAP-OPEN-PWR
R317 54K9R3F
R25 40K2R3F
R26 80K6R3F
R316 174KR3D
C315 SC1800P50V3KX
C29 SC680P50V2KX
C2_SB:Change R100 to debug Core power
IMVP IV
Load Line Slope :3mR
25A*3mV/A=> 75mV
Idroop = 75mV / 6.04K = 12.4uA
12.4uA/0.87/0.5 = 28.54uA
Rds(on) *Io = Isen * Rsen
(5m/2)*25A=28.54uA*Rsen
R33 = 2.18K ~ 2.15K
1D05V_S0
R348 R344 R342 R341 R338 R336
R347 R345 R343 R340 R339 R337
DUMMY-R2
H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5
1. U12,U14:AO4422 84.04422.037
U13,U15:AO4430 84.04430.B37
R100:3K83R2F
2. U12,U14:IRF7413 84.07413.037
U13,U15:IRF7832-U 84.07832.037
R100:2K43R2F
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE
Size A3
Document Number
MORAR
Rev SB
Date: Friday, May 27, 2005
Sheet 34 of 40

TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(5V=>CH1 , 3D3V=>CH2 , 1D05V =>CH3)



PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

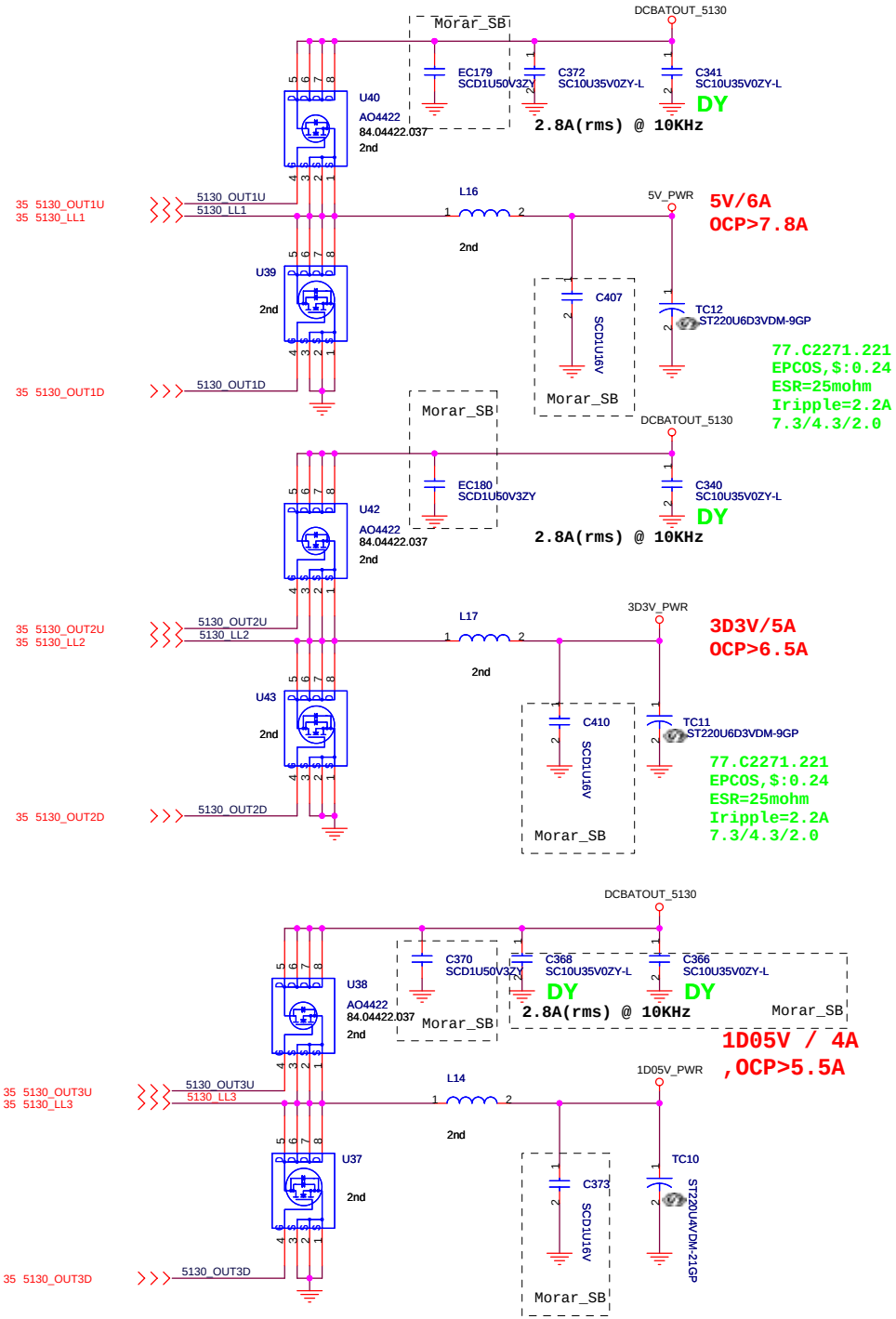
Title: *TI TPS5130 ---- 5V/3.3V/1.05V,2.5(LDO)*

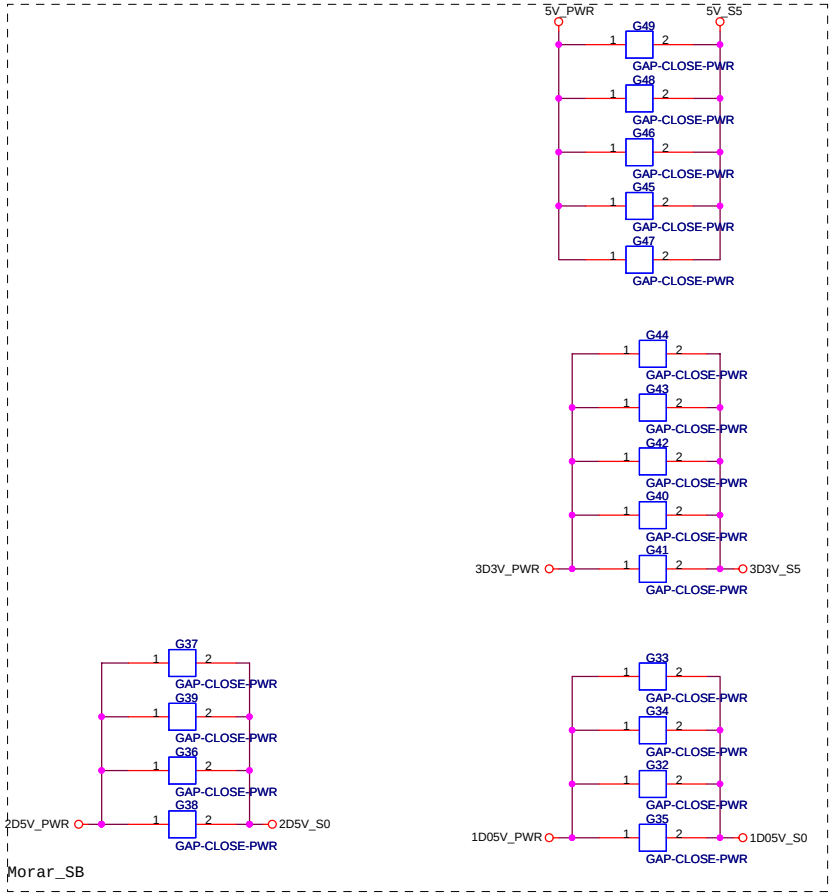
Size: A3 | Document Number: MORAR | Rev: SB

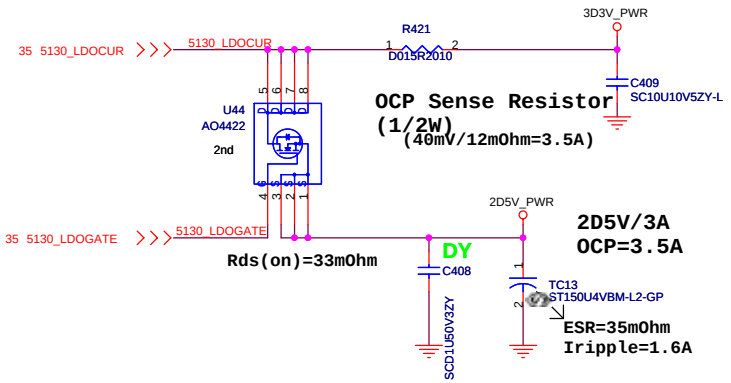
Date: Friday, May 27, 2005 | Sheet 35 of 40

TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

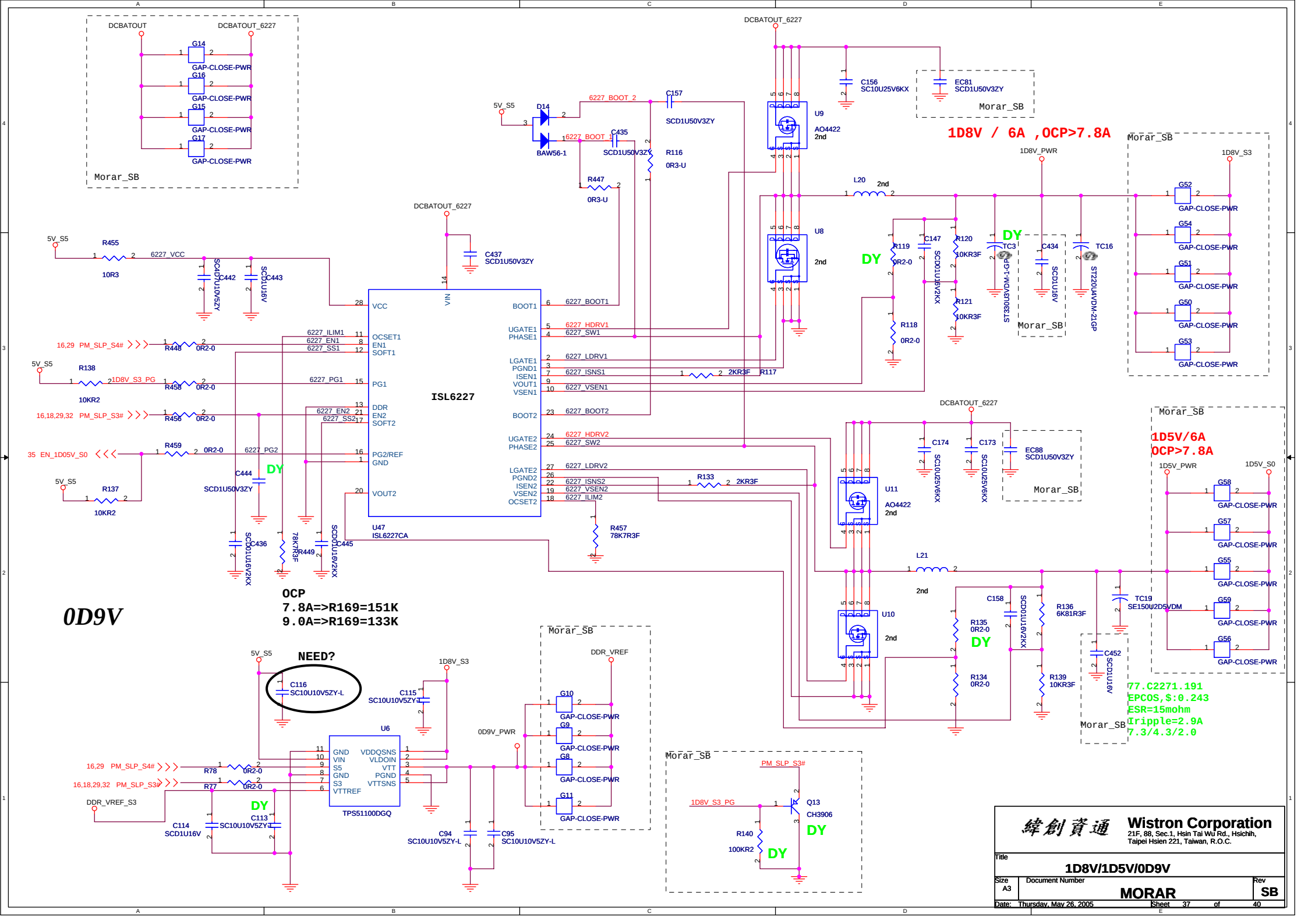
(5V=>CH1 , 3D3V=>CH2 , 1D05V =>CH3)

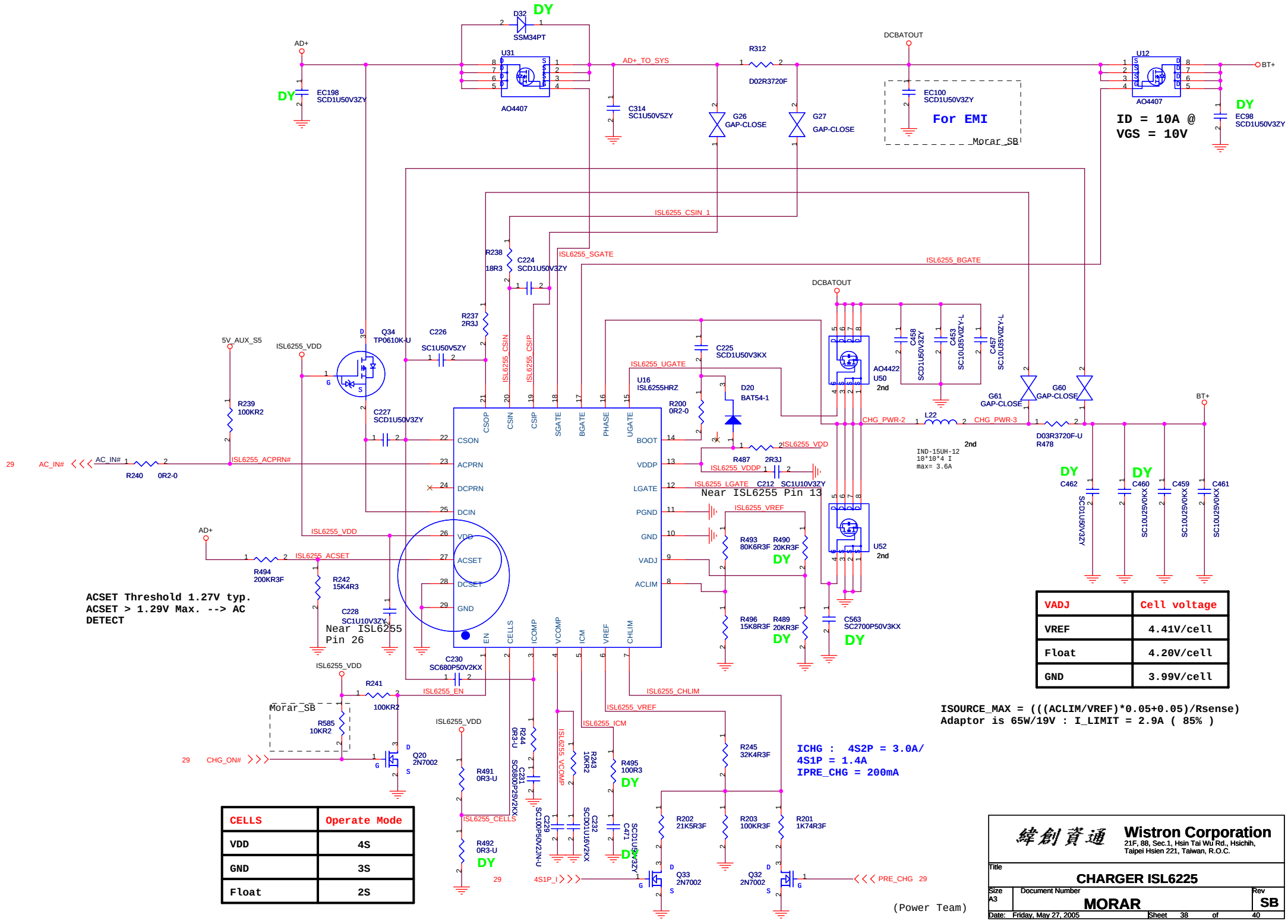






緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*TI TPS5130 ---- 5V/3.3V/1.05V,2.5(LDO)*	
Size A3	Document Number **MORAR**	Rev **SB**
Date: Friday, May 27, 2005	Sheet 36 of 40	


DCBATOUT
DCBATOUT_6227
G14
GAP-CLOSE-PWR
G16
GAP-CLOSE-PWR
G15
GAP-CLOSE-PWR
G17
GAP-CLOSE-PWR
Morar_SB
1D8V / 6A ,OCP>7.8A
U9
AO4422
2nd
U8
2nd
C156
SC10U25V6KX
EC81
SCD1U50V3ZY
D14
BAW56-1
C157
SCD1U50V3ZY
C435
SCD1U50V3ZY
R116
0R3-U
R447
0R3-U
6227_BOOT_2
6227_BOOT_1
L20
2nd
1D8V_PWR
1D8V_S3
G52
G54
G51
G50
G53
R119
0R2-0
C147
SCD1U25V2KX
R120
10KR3F
R121
10KR3F
R118
0R2-0
TC3
ST330U3VDM-1-GP
C434
SCD1U16V
TC16
ST220U4VDM-21GP
DY
5V_S5
R455
10R3
6227_VCC
C442
SC47U10V5ZY
C443
SCD1U16V
C437
SCD1U50V3ZY
VIN
ISL6227
VCC
OCSET1
EN1
SOFT1
PG1
DDR
EN2
SOFT2
PG2/REF
GND
VOUT2
BOOT1
UGATE1
PHASE1
LGATE1
PGND1
ISEN1
VOUT1
VSEN1
BOOT2
UGATE2
PHASE2
LGATE2
PGND2
ISEN2
VSEN2
OCSET2
6227_ILIM1
6227_EN1
6227_SS1
6227_PG1
6227_EN2
6227_SS2
6227_PG2
6227_HDRV1
6227_SW1
6227_LDRV1
6227_ISNS1
6227_VSEN1
6227_BOOT2
6227_HDRV2
6227_SW2
6227_LDRV2
6227_ISNS2
6227_VSEN2
6227_ILIM2
R117
2KR3F
R133
2KR3F
R457
78K7R3F
U47
ISL6227CA
16,29 PM_SLP_S4#
R448
0R2-0
5V_S5
R138
10KR2
1D8V_S3_PG
R458
0R2-0
16,18,29,32 PM_SLP_S3#
R456
0R2-0
35 EN_1D05V_S0
R459
0R2-0
5V_S5
R137
10KR2
C444
SCD1U50V3ZY
C436
SCD1U16V2KX
78K7R3F
R449
C445
SCD1U16V2KX
0D9V
OCP
7.8A=>R169=151K
9.0A=>R169=133K
U11
AO4422
2nd
C174
SC10U25V6KX
C173
SC10U25V6KX
EC88
SCD1U50V3ZY
1D5V/6A
OCP>7.8A
1D5V_PWR
1D5V_S0
G58
G57
G55
G59
G56
L21
2nd
U10
2nd
C158
SCD1U16V2KX
R135
0R2-0
R134
0R2-0
R136
6K81R3F
R139
10KR3F
TC19
SE150U2D5VDM
C452
SCD1U16V
77.C2271.191
EPCOS,$:0.243
ESR=15mohm
Iripple=2.9A
7.3/4.3/2.0
5V_S5
NEED?
C116
SC10U10V5ZY-L
C115
SC10U10V5ZY-L
1D8V_S3
U6
TPS51100DGQ
GND
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
0D9V_PWR
DDR_VREF
G10
G9
G8
G11
16,29 PM_SLP_S4#
R78
0R2-0
16,18,29,32 PM_SLP_S3#
R77
0R2-0
DDR_VREF_S3
C114
SCD1U16V
C113
SC10U10V5ZY-L
C94
SC10U10V5ZY-L
C95
SC10U10V5ZY-L
PM_SLP_S3#
1D8V_S3_PG
Q13
CH3906
R140
100KR2
DY
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1D8V/1D5V/0D9V
Size
A3
Document Number
MORAR
Rev
SB
Date: Thursday, May 26, 2005
Sheet 37 of 40



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

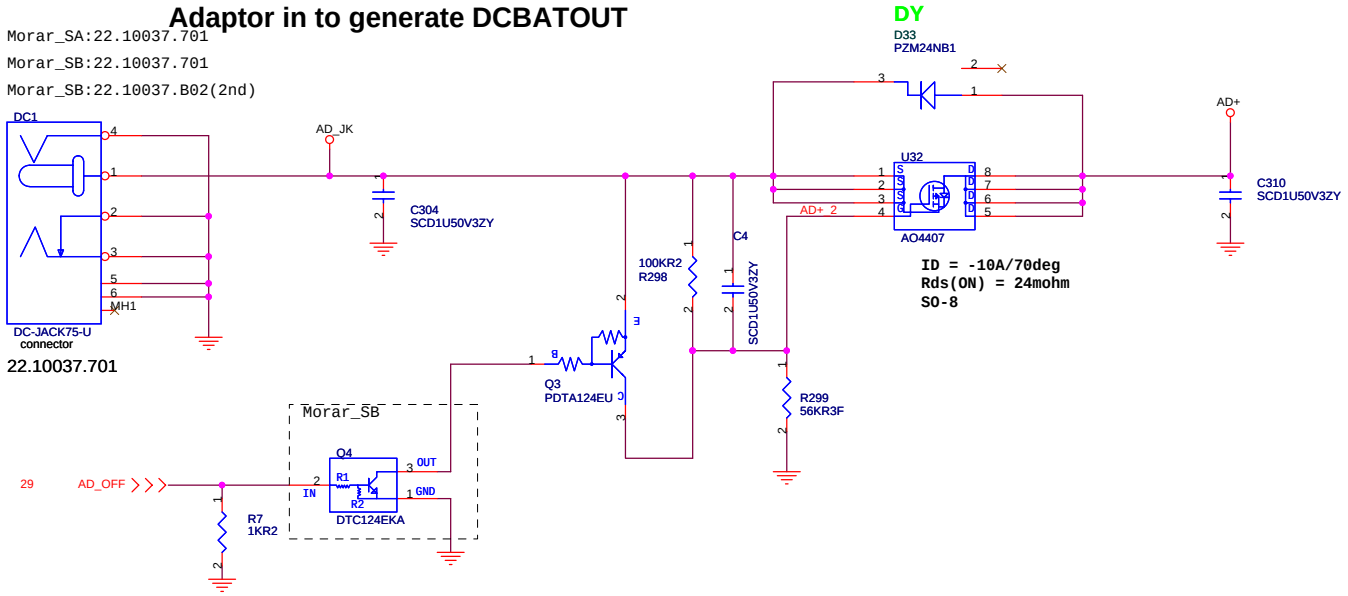
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHARGER ISL6225
Size A3 / Document Number	MORAR / Rev SB
Date: Friday, May 27, 2005	Sheet 38 of 40

Adaptor in to generate DCBATOUT

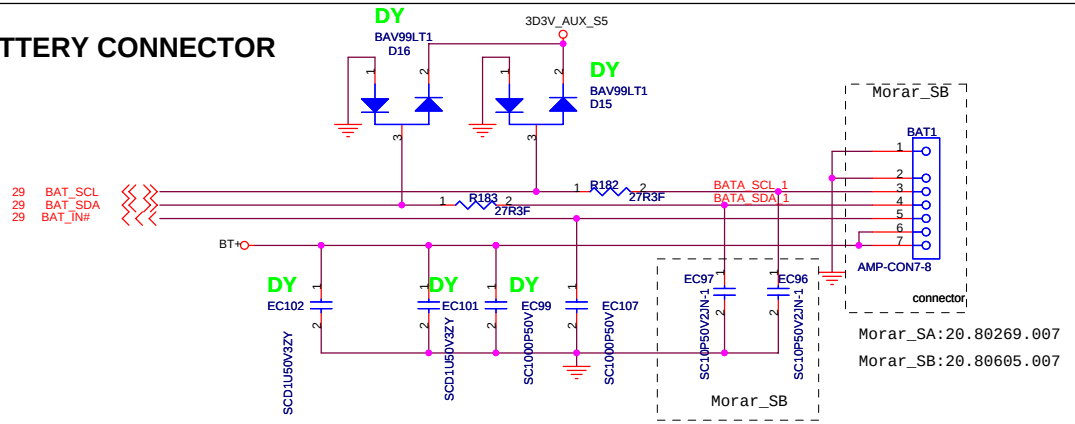
Morar_SA:22.10037.701

Morar_SB:22.10037.701

Morar_SB:22.10037.B02(2nd)

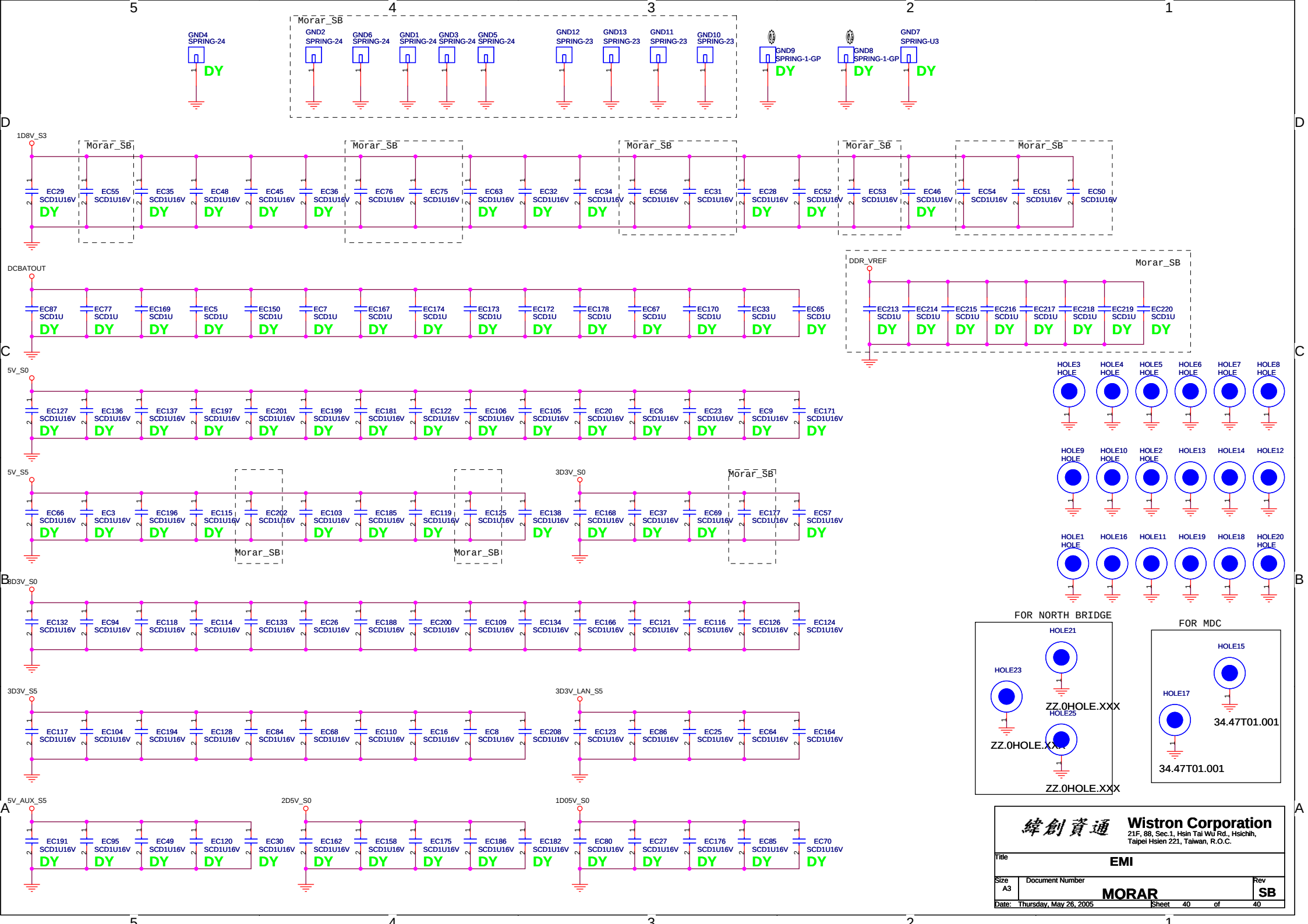


BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD/BATT CONN		
Size: A3	Document Number: MORAR	Rev: SB
Date: Saturday, May 28, 2005	Sheet 39 of 40	


GND4 SPRING-24
Morar_SB
GND2 SPRING-24
GND6 SPRING-24
GND1 SPRING-24
GND3 SPRING-24
GND5 SPRING-24
GND12 SPRING-23
GND13 SPRING-23
GND11 SPRING-23
GND10 SPRING-23
GND9 SPRING-1-GP
GND8 SPRING-1-GP
GND7 SPRING-U3
DY
1D8V_S3
EC29 SCD1U16V
EC55 SCD1U16V
EC35 SCD1U16V
EC48 SCD1U16V
EC45 SCD1U16V
EC36 SCD1U16V
EC76 SCD1U16V
EC75 SCD1U16V
EC63 SCD1U16V
EC32 SCD1U16V
EC34 SCD1U16V
EC56 SCD1U16V
EC31 SCD1U16V
EC28 SCD1U16V
EC52 SCD1U16V
EC53 SCD1U16V
EC46 SCD1U16V
EC54 SCD1U16V
EC51 SCD1U16V
EC50 SCD1U16V
DCBATOUT
EC87 SCD1U
EC77 SCD1U
EC169 SCD1U
EC5 SCD1U
EC150 SCD1U
EC7 SCD1U
EC167 SCD1U
EC174 SCD1U
EC173 SCD1U
EC172 SCD1U
EC178 SCD1U
EC67 SCD1U
EC170 SCD1U
EC33 SCD1U
EC65 SCD1U
DDR_VREF
EC213 SCD1U
EC214 SCD1U
EC215 SCD1U
EC216 SCD1U
EC217 SCD1U
EC218 SCD1U
EC219 SCD1U
EC220 SCD1U
5V_S0
EC127 SCD1U16V
EC136 SCD1U16V
EC137 SCD1U16V
EC197 SCD1U16V
EC201 SCD1U16V
EC199 SCD1U16V
EC181 SCD1U16V
EC122 SCD1U16V
EC106 SCD1U16V
EC105 SCD1U16V
EC20 SCD1U16V
EC6 SCD1U16V
EC23 SCD1U16V
EC9 SCD1U16V
EC171 SCD1U16V
5V_S5
EC66 SCD1U16V
EC3 SCD1U16V
EC196 SCD1U16V
EC115 SCD1U16V
EC202 SCD1U16V
EC103 SCD1U16V
EC185 SCD1U16V
EC119 SCD1U16V
EC125 SCD1U16V
EC138 SCD1U16V
3D3V_S0
EC168 SCD1U16V
EC37 SCD1U16V
EC69 SCD1U16V
EC177 SCD1U16V
EC57 SCD1U16V
HOLE3 HOLE
HOLE4 HOLE
HOLE5 HOLE
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HOLE9 HOLE
HOLE10 HOLE
HOLE2 HOLE
HOLE13 HOLE
HOLE14 HOLE
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HOLE16 HOLE
HOLE11 HOLE
HOLE19 HOLE
HOLE18 HOLE
HOLE20 HOLE
FOR NORTH BRIDGE
HOLE21
HOLE23
HOLE25
ZZ.0HOLE.XXX
FOR MDC
HOLE15
HOLE17
34.47T01.001
EC132 SCD1U16V
EC94 SCD1U16V
EC118 SCD1U16V
EC114 SCD1U16V
EC133 SCD1U16V
EC26 SCD1U16V
EC188 SCD1U16V
EC200 SCD1U16V
EC109 SCD1U16V
EC134 SCD1U16V
EC166 SCD1U16V
EC121 SCD1U16V
EC116 SCD1U16V
EC126 SCD1U16V
EC124 SCD1U16V
3D3V_S5
EC117 SCD1U16V
EC104 SCD1U16V
EC194 SCD1U16V
EC128 SCD1U16V
EC84 SCD1U16V
EC68 SCD1U16V
EC110 SCD1U16V
EC16 SCD1U16V
EC8 SCD1U16V
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3D3V_LAN_S5
EC123 SCD1U16V
EC86 SCD1U16V
EC25 SCD1U16V
EC64 SCD1U16V
EC164 SCD1U16V
5V_AUX_S5
EC191 SCD1U16V
EC95 SCD1U16V
EC49 SCD1U16V
EC120 SCD1U16V
EC30 SCD1U16V
2D5V_S0
EC162 SCD1U16V
EC158 SCD1U16V
EC175 SCD1U16V
EC186 SCD1U16V
EC182 SCD1U16V
1D05V_S0
EC80 SCD1U16V
EC27 SCD1U16V
EC176 SCD1U16V
EC85 SCD1U16V
EC70 SCD1U16V
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI
Size A3
Document Number
MORAR
Rev SB
Date: Thursday, May 26, 2005
Sheet 40 of 40