GLASSMAN HIGH VOLTAGE, INC.
Route 22 East, Salem Industrial Park
Whitehouse Station, NJ 08889

Our Glassman is a
Model SP/WG-10N30
SN M348220-02BC900718

INSTRUCTION MANUAL

WG SERIES

Model PS/WG-10N30

Serial M308480-05

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TABLE OF CONTENTS

WG SERIES

TABLE OF CONTENTS (Cont'd.)

SECTION II - APPLICATIONS INFORMATION

THIS EQUIPMENT EMPLOYS VOLTAGES THAT ARE DANGEROUS. EXTREME CAUTION MUST BE EXERCISED WHEN WORKING WITH THIS EQUIPMENT

A. Unpacking and Inspection

First inspect package exterior(s) for evidence of rough handling in transit. If none, proceed to unpack... carefully. After removing the supply from its shipping container(s), remove the top dust cover(s) and inspect thoroughly for damage. In some models the high voltage assembly is shipped in its own container and should also be thoroughly inspected.

IMPORTANT

In cases of damage due to rough handling in transit, notify the carrier immediately if damage is evident from appearance of package. Do not destroy or remove any of the packing material used in a damaged shipment. Carrier companies will usually not accept claims for damaged material unless they can inspect the damaged item and its associated packing material. Claims must be made promptly - certainly within five days of receipt of shipment.

Check out the power supply operation and performance as outlined below.

B. Installation and Operation

The following procedure should be followed to connect and operate the equipment, after it has been placed or mounted in position.

WARNING

THIS EQUIPMENT EMPLOYS VOLTAGES THAT ARE DANGEROUS. EXTREME CAUTION MUST BE EXERCISED WHEN WORKING WITH THIS EQUIPMENT.

A 3-PRONG GROUNDED PLUG IS PROVIDED FOR CONNECTION TO AC LINE. IF A GROUNDED RECEPTACLE IS NOT AVAILABLE, USE AN ADAPTER AND CONNECT THE THIRD WIRE TO A GOOD GROUND - PREFERABLY A WATER SYSTEM GROUND.

ALWAYS MAKE CERTAIN THAT THE RETURN LINE FROM THE LOAD IS CONNECTED TO THE GROUND STUD AT THE REAR OF THE UNIT. A GOOD EXTERNAL WATER SYSTEM GROUND SHOULD ALSO BE CONNECTED TO THIS STUD.

1. Check the input voltage rating on the nameplate of the supply and make certain that this is the rating of the available power source.

2. Connect the input cable to the power source.

3. In models in which the high voltage assembly is physically not contained within the control assembly, interconnection cabling is provided and must be attached between the main control assembly and the high voltage assembly.

    a. For models with an output voltage of greater than 60kV, the high voltage assembly is contained in a polyethylene enclosure which is mounted in a separate 5-¼" high rack chassis.

        The control and high voltage assembly chassis are both 5-¼" high and are intended to be mounted one above the other to use 10-½" of rack space. Normally the control chassis is mounted above the high voltage chassis, but this is arbitrary.

    b. A control cable with circular connectors (plugs) on both ends is provided to interconnect between the control assembly and the high voltage assembly. The connectors mate with a receptacle on the rear of the control chassis and on the rear of the high voltage assembly chassis.

c. Note that there is a "jumper" connection in the wires attached to the high voltage assembly chassis receptacle. This is an interlock connection which prevents the power supply from operating unless both connectors are plugged into their respective receptacles.

d. A high voltage RF connection is also required between the control and high voltage assembly chassis. This is supplied in a short length with plugs on each end of the high voltage lead so that a short loop between the pair of corresponding high voltage receptacles on the rear of the chassis can be achieved. This wire carries high voltage AC (5kV peak) and should not make contact with any ground surfaces or other low voltage elements. It should be an "air borne" lead.

4. Connect the high voltage output cable and ground return lead to the load. Insert the high voltage output cable into the receptacle on the rear panel. Spring action should be felt as the probe reaches the bottom of the receptacle. Hold the cable pressed down against the spring as the locking nut is screwed onto the receptacle.

5. Rotate OUTPUT VOLTAGE control to fully counter-clockwise position. (This is optional, but desirable to prevent damage to external equipment caused by inadvertent overvoltage setting. Not required if correct setting has already been determined.)

6. Rotate OUTPUT CURRENT control to approximately mid-scale (a setting of 5 on the 10-turn control).

7. Apply input power to the supply by depressing the POWER ON/OFF pushbutton. The indicator should light.

8. Energize high voltage by depressing the HV ON push-button. The indicator should light.

9. Rotate the OUTPUT VOLTAGE control clockwise and observe that both the voltmeter and the ammeter rise. The ammeter reading is a function of the load connected to the supply, and will not read if a load is not connected. The output end of the high voltage output cable, if connected to the supply, must be prevented from coming too close to ground, or high voltage breakdowns may occur.

10. The mode indicators on the front panel indicate whether the supply is operating in a voltage regulated or current regulated mode.

11. To shut down, press the POWER ON/OFF pushbutton.

WARNING: DO NOT HANDLE THE LOAD UNTIL IT HAS BEEN DISCHARGED - CHECK KILOVOLTMETER!!! AN UNLOADED SUPPLY MAY TAKE UP TO 15 SECONDS TO FULLY DISCHARGE.

C. Polarity Reversal

Models 60kV and below

For reversible polarity models 60kV and below, the power supply has been shipped with two high voltage assemblies, one positive and one negative. The serial label on the high voltage assembly indicates its polarity. To reverse the polarity of the power supply, it is necessary to interchange the high voltage modules. First remove the dust cover from the unit. Then remove the electrical connector that is mounted on the rear of the unit, noting where it is, so you will know how to replace it. Next, remove the assembly from its mechanical constraint. Install the other high voltage assembly by reversing your steps.

Models above 60kV

For reversible polarity models above 60kV, the power supply has been shipped with two high voltage chassis, one positive and one negative. The serial label on the rear of the chassis indicates its polarity. To reverse the polarity of the power supply, simply interchange the high voltage chassis.

D. Remote Control Connections and Applications

Terminal board TB1 is mounted on the rear panel of the control chassis and has the following functions:

TB1-1: Ground. This is an auxiliary instrumentation ground terminal. The main ground terminal is a "stud", E1, located near the high voltage output connector.

TB1-2: Common. This terminal is the instrumentation/measurement circuit return. It is "DC" connected to ground, internally, by a pair of back-to-back diodes. If left floating, this point will clamp at approximately 500 millivolts. The power supply

is shipped from the factory with a barrier jumper across TB1-1 and TB1-2, so that, normally, the common is operated at ground potential. If desired, the user may lift this jumper and allow the common to "float". This may be done for the purpose of inserting a current monitoring circuit which will measure "true" load current, with no internal drain included in the measurement. When attempting this, it should be remembered that the inserted drop must not exceed the 500 millivolt clamping voltage, or erroneous readings will be obtained.*

TB1-3: External Interlock. This terminal must be connected to common, TB1-2, to enable the power supply control circuits. These terminals have been shorted by a barrier jumper terminal at the factory to assure start-up. When desired, the jumper may be removed and replaced by an external switch device which must be closed to make the supply operable. When the external switch is open, the power supply output will drop to zero. Consult GLASSMAN Engineering Department for alternate interlock configurations, such as TTL enable logic.

TB1-4: Voltage Monitor. A 0-10 volt, positive with respect to common/ground, signal in direct proportion to output voltage is available at this terminal. A 10 K ohm limiting impedance protects the internal circuitry, so that a digital voltmeter with greater than 10 megohms input impedance should be used to monitor this terminal. It is also acceptable to use a 1 milliampere DC full scale instrument for monitor purposes.

TB1-5: Voltage Program. To operate with remote voltage programming, first remove the barrier jumper between TB1-5 and TB1-6. A 0-10 volt, positive with respect to common/ground, signal will control the output from zero to rated voltage. The user may provide his own external programming control signal, or may use an external potentiometer across the reference to derive a programming voltage. The preferred value for an external potentiometer is 10 K ohms, although values from 5 K through 50 K ohms will be satisfactory. When inserting an external programming signal, the negative end should be connected to the common/ground terminal TB1-1/2. The positive end should be connected to terminal TB1-5.

When connecting an external potentiometer using the power supply internal reference, connect as follows:

Clockwise terminal to TB1-10 (reference voltage)

Counter-clockwise terminal to TB1-1/2 (common)

Slider terminal to TB1-5 (program input)

In this mode of operation, the front panel control serves as an overvoltage limit for the remote control. As an example, if the front panel control is set to 50%, then the remote control is capable of adjustment from 0 to 50% only, which corresponds to a signal voltage of 0 to 5 volts DC. If full range control is desired, the front panel control must be set to maximum. In any case, the power supply will "clamp" the programming input at the front panel control setting, and thereby protect against inadvertent overvoltage programming signals up to 50 volts DC.

TB1-6: Local Voltage Control. This terminal is normally used as the voltage source for the voltage program input. As such, the power supply is shipped with a barrier jumper connecting TB1-5 and TB1-6. To operate with remote voltage programming, the jumper must be removed and proceed as described in TB1-5 above.

TB1-7: Current Monitor. A 0-10 volt, positive with respect to common/ground, signal in direct proportion to output current is available at this terminal. Use an instrument with at least 10 megohm input impedance to monitor this terminal.

TB1-8: Current Program. To operate with remote current programming, first remove the barrier jumper between TB1-8 and TB1-9. A 0-10 volt, positive with respect to common/ground, signal will control the output from zero to rated current. The user may provide his own external programming control signal, or may use an external potentiometer across the reference to derive a programming voltage. The preferred value for an external potentiometer is 10K ohms, although values from 5K through 50K ohms will be satisfactory.

When inserting an external programming signal, the negative end should be connected to the common/ground terminal, TB1-1/2. The positive end should be connected to terminal TB1-8.

When connecting an external potentiometer using the power supply internal reference, connect as follows:

Clockwise terminal to TB1-10 (reference voltage)

Counter-clockwise terminal to TB1-1/2 (common)

Slider terminal to TB1-8 (program input)

In this mode of operation, the front panel current control serves as an overcurrent limit for the remote control. It works analogously to the overvoltage clamp action of the front panel voltage control as described in TB1-5 above.

TB1-9: Local Current Control. This terminal is normally used as the voltage source for the current program input. As such, the power supply is shipped with a barrier jumper connecting TB1-8 and TB1-9. To operate with remote current programming, the jumper must be removed and proceed as described in TB1-8 above.

TB1-10: Reference. An ultra-stable, 10 volt, positive with respect to common (terminal TB1-2), reference is supplied for user programming applications. Remember that the common is normally at ground potential, so that external circuitry may be returned directly to ground. Maximum current drain from this reference should be limited to 3 milliamperes to maintain normal operation, although no damage will be done even with a severe overload at this terminal.

* NOTE: When operating the power supply with jumper between common (TB1-2) and ground (TB1-1) removed, any equipment connected to the common terminal (TB1-2) must not be grounded.

E. Correspondence and Ordering Spare Parts

1. Each Glassman power supply has an identification label on the rear of the chassis that bears its model and serial number.

2. When requesting engineering or applications information, reference should be made to this model and serial number, as well as to the component symbol number(s) shown on the applicable schematic diagram, if specific components or circuit sections are involved in the inquiry.

3. When ordering spare parts, the information described in Paragraph 2 should be given, in addition to the Glassman part number that appears on the parts list.

Examples: 1. When requesting engineering data:

"...voltage across capacitor C2, for serial no. M020670 of model PS/WG-30P10 power supply."

2. When requesting that component:

"...one (1) Glassman part no. CFH1-10.0-0.015 capacitor C2 for serial no. M020670 of model PS/WG-30P10 power supply."

SECTION III - THEORY OF OPERATION

A. Main Assembly

Refer to the WG Series Main Assembly schematic at the rear of this book. AC input enters the power supply on an input line cord. This is ordinarily 115 volts RMS, 50 - 60 Hz, with a grounded third wire connection. Optional input voltages, as described in the catalog, are available. Power enters through fuse F1 on the rear panel, and then through component FL1, which is an RFI conducted noise filter. The wiring of FL1 physically gounds the third wire to the chassis of the power supply. Power continues to the front panel POWER ON/OFF pushbutton switch, S1. When this switch is in the ON position, the amber pilot light (part of S1) is illuminated, since the low end of the pilot light is returned directly to the low side of the power line. Observe that the "hot" side of the line is also brought to the primary side of transformer T1, and fan B1. These components are not energized since the return to the common side of the line is not yet made. The next action is to close momentary pushbutton switch S2, HV ON. The momentary closure of pushbutton S2 returns components T1, B1, and relay coil K1 to the common side of the power line.

When the coil of contactor/relay K1 is energized, its contacts K1a and K1b, close. This causes K1 coil to go into a self-holding mode, and the HV ON pushbutton S2 may be released. AC power is now applied to the red pilot light (part of S2), as well as to transformer T1, and fan B1. The AC power continues through current limiting resistor R2, to the voltage surge limiting semiconductor CR2, and then to bridge rectifier CR1. The rectified voltage is applied to bleed resistor R1 and capacitor C1, which are in parallel, to develop the main B+ source. The B+ voltage is applied to sub-assembly A3 via terminals 1 and 5 by passing it through surge current sensing sub-assembly A5. Action of these sub-assemblies will be described in subsequent paragraphs.

The balance of the circuitry shown on the main assembly schematic consists essentially of the front panel and rear panel control elements and the interconnecting wiring between the various sub-assemblies. Included among these components are the following:

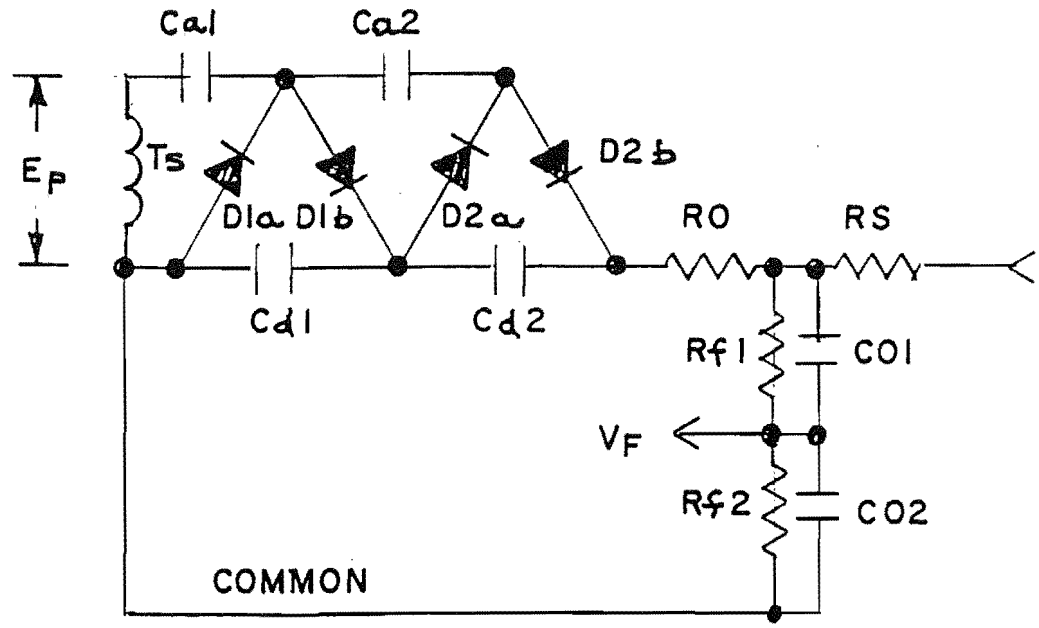
R1 and R2 are the ten-turn front panel control potentiometers for current and voltage, respectively. Voltage applied across these potientiometers is derived from the A1 internal reference J1-13, which will be described later. Sliders of the potentiometers are connected to the rear terminals TB1-9 and TB1-6 respectively, as well as being returned internally to J1-14 and

J1-11 (on sub-assembly A1) respectively, to be described later. Functions of the terminal connections at TB1 on the rear panel are fully described under application information in Section II, Paragraph D, above.

M1 is the front panel kilovoltmeter, and M2 is the front panel milliammeter.

The LED CR2 is the front panel voltage mode indicator, and LED CR1 is the front panel current mode indicator. All of these components will be described subsequently in conjunction with sub-assembly A1.

B. High Voltage Assembly



A simplified diagram of the high voltage generating and output circuit is shown above. The circuit is a cascade voltage multiplier, frequently referred to as a Cockroft-Walton generator. For a complete technical discussion of the circuit, numerous articles exist in the literature, of which we have listed several for reference.[1]

A brief description of the multiplier action is as follows: When Ts is at its negative peak, capacitor Ca1 charges through diode D1a to Ep, the transformer peak voltage. When the transformer polarity reverses, so that its output is positive with respect to common, the transformer voltage, Ep, is then in the same direction as the voltage on the capacitor Ca1, and the two voltages add arithmetically. Thus, 2Ep is the driving voltage which charges capacitor Cd1 through diode D1b, and the voltage developed across the capacitor Cd1 is equal to 2Ep.

[1] "Factors Controlling the Performance of Cascade Rectifier Circuits"- R.E. Jones, R.T. Waters, Proc IEE, Vol. III, 5, May 64.

Cockcroft-Walton Voltage Multiplier Circuit, Everhart, Lorrain, Rev Sci Instrum, 1953, 24, p.221.

Continuing up the multiplier string, and considering again the negative swing of the transformer to Ep, it is easy to see that a net driving voltage of 2Ep is available to charge capacitor Ca2 to 2Ep volts, through diode D2a. Similarly, when the transformer once again drives to its positive peak, Ep, a quick calculation will show that capacitor Cd2 also will charge to a value of 2Ep through diode D2b.

Note that capacitors Cd1 and Cd2 are both charged to a voltage 2Ep. This process would continue for any additional voltage multiplier stages. Also note that capacitor Ca1 is charged to Ep, but capacitor Ca2, and all additional capacitors on this side of the voltage multiplier network, charge to 2Ep. All diodes are subjected to a peak inverse voltage of 2Ep.

Thus, in the voltage multiplier network, it is seen that each stage, consisting of an AC capacitor Ca, a DC capacitor Cd, and two diodes, D1a and D1b, develops a voltage across the DC capacitor which is equal to twice the peak voltage of the transformer. It is for this reason that the stages of the voltage multiplier network are frequently referred to as voltage doubler stages. The total output voltage of the voltage multiplier is therefore seen to be 2nEp, in which n is the number of doubler stages.

In the above discussion, we have ignored the effects of regulation and component impedances. The voltage 2nEp is the output voltage in the perfect case in which all impedances are zero and the load current is zero. Inherent regulation and ripple can be calculated from the following formulas taken from the reference article by Jones and Waters on the previous page.

$$\text{Ripple Volts (p-p)} = In(n+1)/2fC$$
$$\text{Regulation Volts} = I(2n/3 + n/4 + n/12)/fC$$

I = DC load current (amperes)
n = number of doubler stages
f = operating frequency (Hz)
C = capacitance per stage (farads)

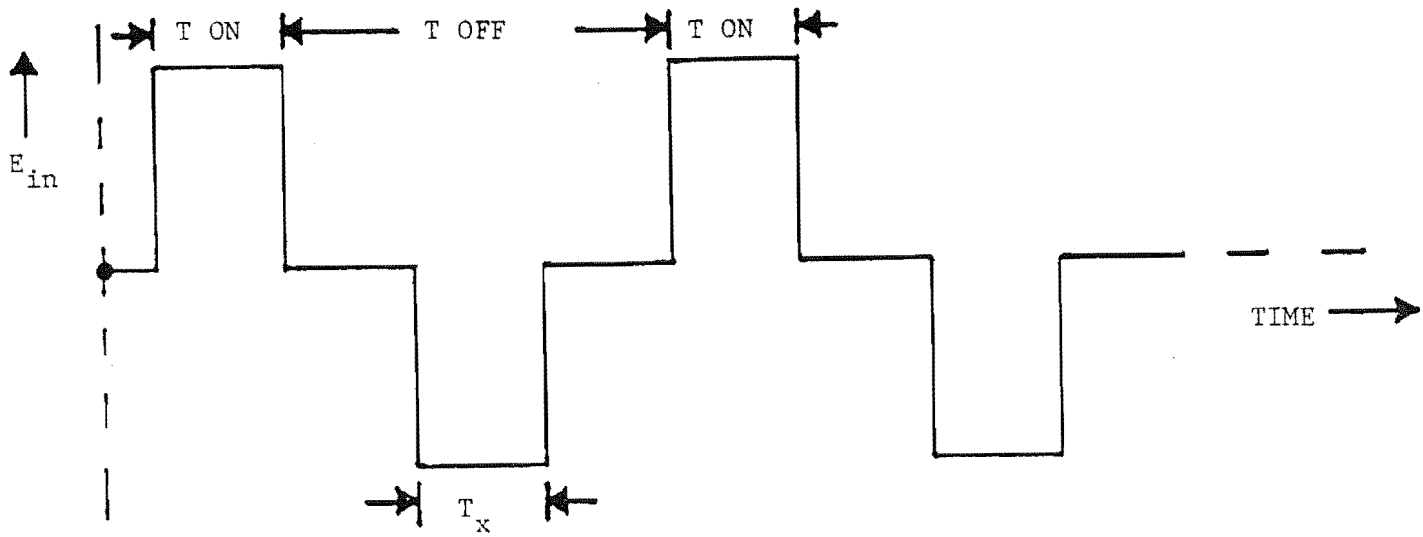
The schematic shows a resistor Ro, feeding the output feedback network, consisting of resistor divider Co1 and Co2. The resistor divider generates feedback voltage Vf, which is used to control the regulating loop. Capacitor divider Co1 and Co2 serve as stabilizing elements for the feedback loop, as well as an output filter capacitor in conjunction with the output resistor Ro. To be specific, the ripple voltage across the voltage multiplying capacitor network consisting of Cd1 and Cd2, etc., is attenuated by the RC network consisting of Ro and the series combination of Co1 and Co2. Rs is a final surge limiting resistor which is a

protective device in the event of sudden, severe,overload conditions on the power supply.

The high voltage transformer secondary Ts, which is shown in this schematic, is not physically within the sub-assembly A2. Actually it is a part of the Driver Assembly, A1.

C. Transformer Primary, and Power Transistor Collector Drive Circuitry

Refer to the Power Module Schematic (AP-WG) at the rear of this manual. This schematic is applicable to the power module shown on the Main Assembly Schematic, which is designated as A3. Observe that the main power transistors Q1 and Q2 are connected in series across the B+/B- power source. The center junction of the two transistors, i.e., the emitter of Q1 and the collector of Q2, are AC coupled through capacitor C1 to the primary of the main high voltage power transformer coil, T2. The drive system, to be described below, is such that Q1 and Q2 are never on simultaneously. Furthermore, the switching system is such that when a transistor is turned on, it is driven to full saturation. Therefore, the circuit may be viewed as a switching system, in which Q1 is on for some portion of the cycle that Q2 is off, followed by a period during which both Q1 and Q2 are off, then followed by a period during which Q2 is on and Q1 is off. When Q1 is on, the full DC voltage is applied across the series combination of C1 and T2 primary. When Q2 is on, and Q1 is off, a short circuit is applied across the series combination of C1 and T2 primary. By this arrangement, the applied DC B+/B- voltage is "chopped" to a peak-to-peak AC voltage equal to the applied DC voltage, at a frequency which is dependent on the input drive system.



The voltage wave shape shown above is typical for the applied voltage to the base circuitry of Q1 and Q2. The shape shown is

for the voltage of each of the secondary windings of transformer T1, which are applied to the bases of transistors Q1 and Q2. Observe, however, that the two secondary windings are 180° out of phase, so that when a positive pulse is applied to Q1, a negative pulse is simultaneously applied to Q2, and vice versa, Note that the pulse has both a positive and a negative half cycle. However, actual drive to each of the individual transistors Q1 and Q2 occurs only on the positive pulse of the drive transformer wave shape. Thus, during the period T on, let us say that transistor Q1 is on. During the rest of the period until the next positive pulse occurs, the diagram is marked as T off, and transistor Q1 is off. The negative pulse Tx occurs during the off time. It is during this period, Tx, when the other transistor Q2 is actually on.

The pulse width control is such that average voltage applied to the primary of transformer T2 is a function of the on- and off-times of the input voltage, Ein. As the on-time is reduced, the average voltage applied to the primary of T2 is reduced, and the output voltage is correspondingly and proportionally reduced. Similarly, as the on-time is increased, the output voltage is proportionally increased.

This method of duty cycle control permits the transistors to operate with extreme efficiency, since the transistors are driven to saturation during the period when current is permitted to flow in the particular transistor, and the collector voltage rises only when the primary current is turned off.

Diodes CR1 and CR2 are "catch" clamps, which prevent the transistor collector voltages from rising above the B+/B- level. Capacitor C1 prevents any DC component from flowing in the primary of T2, which prevents DC saturation of the power transformer. The components C2 and R6 serve for dynamic damping during the period when both transistors are off.

The function of L1 is to improve the drive circuit efficiency of the primary system.

We now discuss the base drive circuit of the power transistors. In the discussion which follows, we will use the reference designators for the base drive of transistor Q1. Note that the circuitry is exactly analogous to transistor Q2. When the pulse drive is positive, current flows around the main loop consisting of diode CR3, base to emitter of Q1, and resistor R3. During this period of time, transistor Q1 is driven to saturation, and is turned on. Also during this period, capacitor C3 is charged essentially to the peak pulse voltage of the drive transformer through diode CR4. During the off-time of the pulse, which includes both the period of zero drive voltage, as well as negative pulse voltage, the stored energy in capacitor C3 instantly

turns the cutoff transistor Q3 on, providing a sharp cutoff voltage for the main power transistor Q1, reinforcing the removal of base drive current and base charge in transistor Q1. This cutoff circuit is a vital part of the efficient switching of the main power transistors Q1 and Q2.

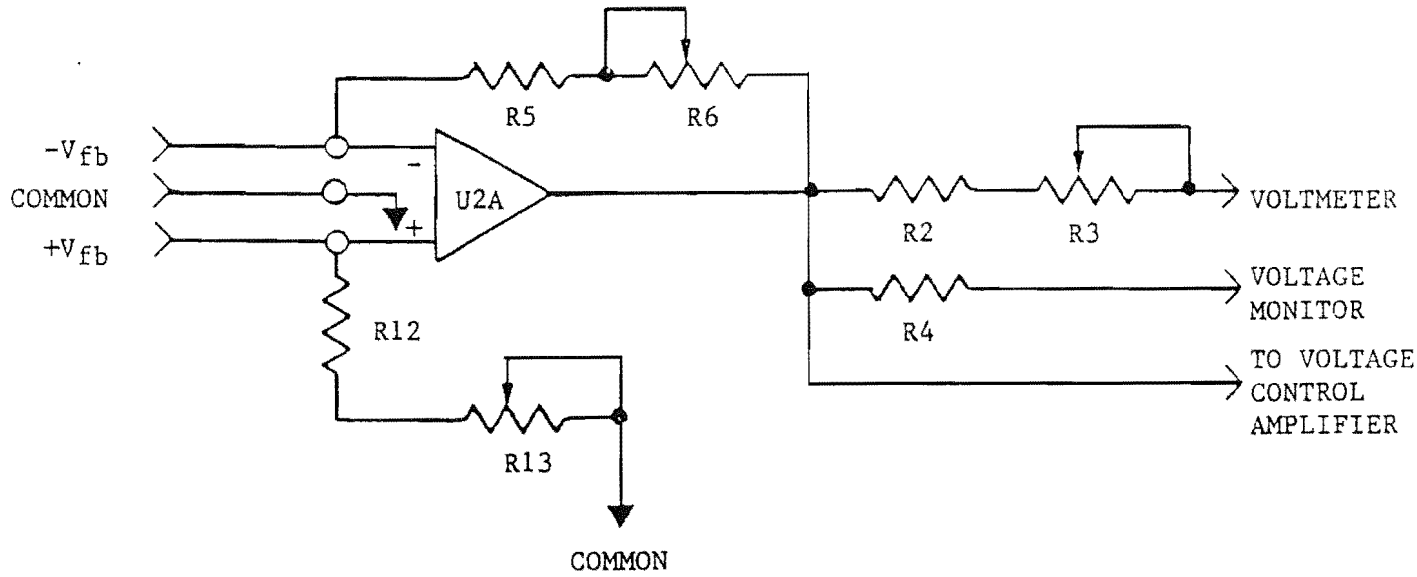
We now consider the pulse drive applied to the primaries of transformer T1 in the power module. The transformer primary is a tapped winding with the center tap connected to +25 volts via terminal J2. The collector drive windings are designated as CD1 and CD2, and are terminated at terminals J4 and J3, respectively. To see the various interconnections, refer to the Main Assembly schematic. The power module is shown as A3 on the Main Assembly schematic.

D. Bias Voltages

Refer again to the Main Assembly schematic and observe that the center-tapped secondary of transformer T1 is connected to the Driver Assembly (A1) through terminals J2-13, -14, and -15. Now refer to the Driver Assembly schematic. J2-14 is connected to common, and J2-13 and -15 are the AC input voltages from the main assembly transformer T1. The AC voltage is applied to the full wave bridge rectifier D16, which develops a pulsating +25V and -25V with respect to common. This is applied to capacitors C21 and C20 to develop filtered +25VDC and -25VDC, respectively. The +25VDC and -25VDC sources are applied to the voltage regulators U8 and U7 to produce regulated +15VDC and -8VDC, respectively. These regulated voltages are applied to the various amplifiers used in the main assembly, to be described below. The regulated +15VDC is applied to the main assembly reference element U6, which develops an extremely stable and well-regulated +10VDC source. Some adjustability is available from this reference by means of adjusting resistor R1. The +15VDC is also used to provide power for the front panel LED pilot lamps, which are VOLTAGE MODE or CURRENT MODE indicators. This function will be described later.

A separate +25VDC source is developed by rectifiers D17, D18, and filter capacitor C38. This source is used to provide B+ voltage for the drive transformer on the power module (A3).

E. Voltage Feedback Input Amplifier, Polarity Reversal, and Voltage Monitor Circuits.



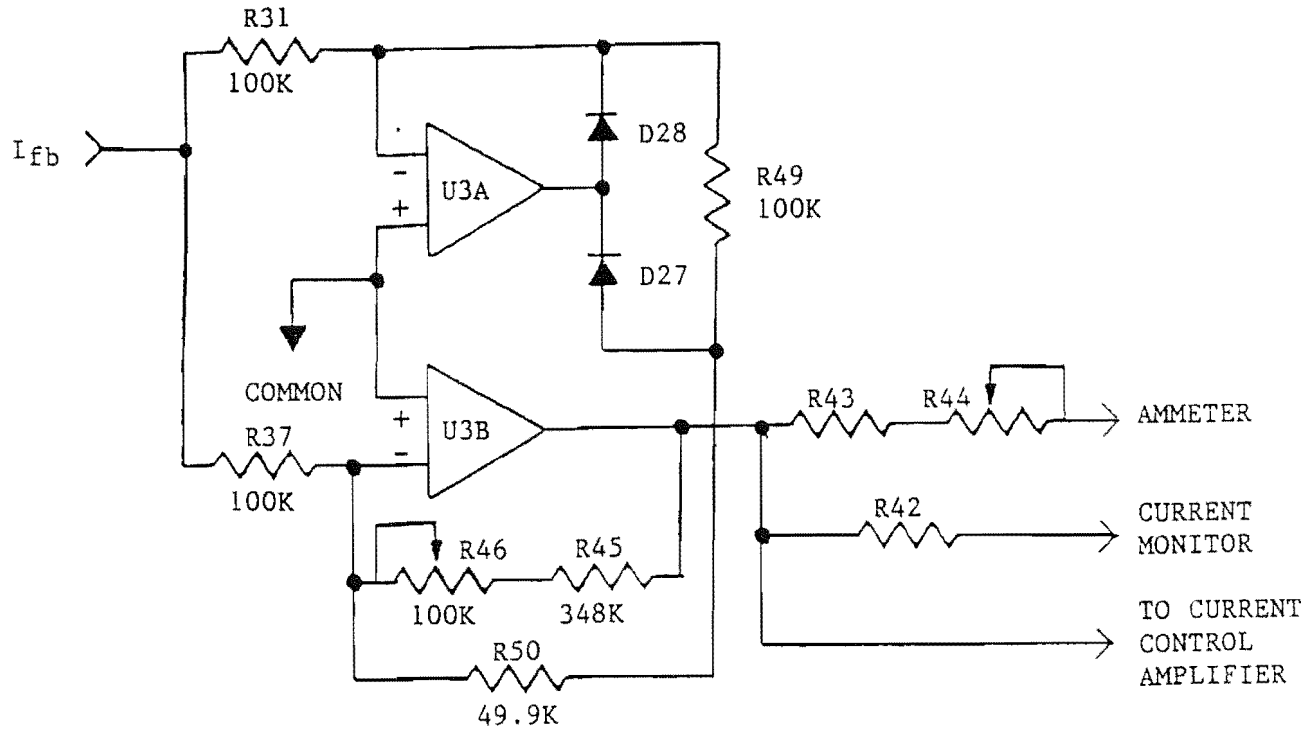
The above simplified schematic of the Driver Assembly shows the essential components involved in this portion of the circuitry. Consider first the case of a positive high voltage output power supply. In this instance, high voltage feedback current flows in through the terminal marked +Vfb and flows through resistors R12 and R13 (in series) to common, developing a positive voltage across these resistors. R13 is adjusted so that at the rated power supply output voltage, exactly 10 volts is developed across the pair of resistors. This voltage is applied to the non-inverting terminal of U2A, which is connected as a follower, with R5 in series with R6, connected between the inverting input terminal and the output terminal of U2A. Thus, the high impedance input configuration is converted to a low impedance output by amplifier U2A. Since the amplifier is connected as a simple follower, the output is exactly equal to the input, and is therefore directly proportional to the high voltage output of the power supply as derived from the voltage feedback current. The output of the amplifier is fed to the front panel voltmeter through resistors R2 and calibrating resistor R3. R3 is used to compensate for any minor inaccuracies in the meter, thereby permitting the meter to be set exactly to full scale for rated output voltage. The amplifier output is also fed to the voltage monitor terminal through resistor R4. R4 is used simply as a protective resistor to protect the power supply in the event that the user inadvertently short circuits or overloads the voltage monitor terminal. Finally, the output of U2A is applied to the

main voltage control feedback amplifier, which will be described below.

When the output of the high voltage power supply is negative, feedback current flows into the terminal marked -Vfb. In this arrangement, U2A acts as an inverting amplifier, in which the non-inverting terminal is connected to common via R12 and R13 in series. The inverting amplifier now forces the inverting terminal of U2A to a virtual ground potential. Thus, current flows from the output of U2A, through resistors R5 and R6 in series, through the inverting input terminal of the amplifier, and finally out through the Vfb terminal to the negative high voltage output, providing the feedback current to the high voltage system. In this polarity, R6 is adjusted so that the output of U2A is exactly 10 volts at the rated output voltage of the power supply.

Therefore, regardless of the high voltage output polarity, the output of the amplifier U2A is always positive and directly proportional to the output voltage. To repeat, the output of U2A is always +10 volts at rated output voltage of the high voltage system, regardless of the polarity. It follows that the voltmeter, voltage monitor, and voltage control amplifiers are the same for this polarity as described above.

F. Current Feedback Input Amplifier, Polarity Reversal, and Current Monitor Circuits



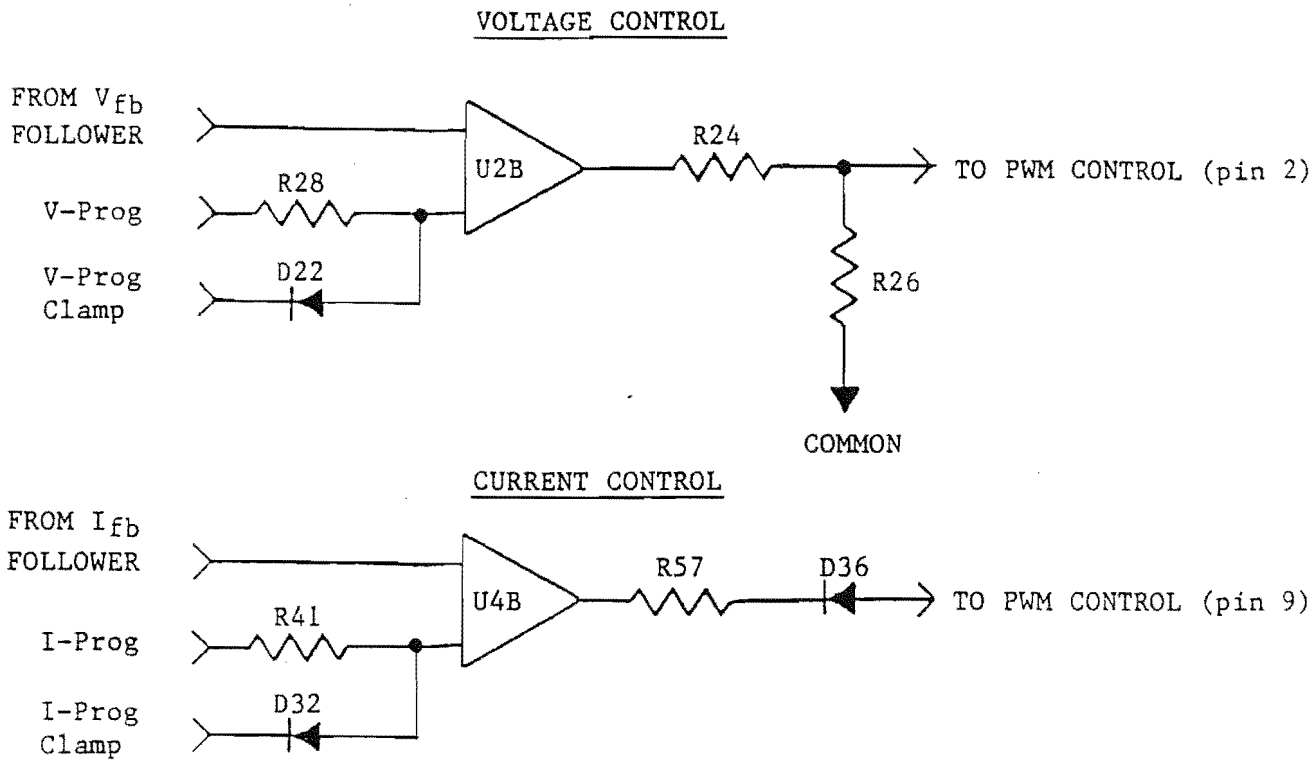
The above simplified schematic of the Driver Assembly shows the basic elements used in the current feedback input amplifier and

the technique used to automatically sense the specific polarity of the power supply output voltage. The terminal marked Ifb is actually a voltage source derived from the high voltage assembly when load current flows through the sensing resistor Rx, which was described above in Paragraph B. The polarity of the voltage developed across Rx is either positive or negative, depending on whether the high voltage output polarity is negative or positive, respectively. Referring to the simplified schematic of the high voltage assembly in Paragraph B, note that the high voltage diodes are drawn for a positive high voltage polarity condition. In this case, current flows from ground or common through resistor Rx into the high voltage diodes D1a, D1b, D2a, and D2b to the high voltage output terminal. Thus, the voltage developed at terminal Ifb is negative with respect to ground. Refer again to the above simplified schematic. If the input source voltage is negative, observe that the output of amplifier U3B is positive, so that current flows through resistors R46 and R45 in series, to resistor R37, and then into the current source. The design is such that R46 is adjusted to make the series combination of resistors R46 and R45 exactly four times the value of resistor R37. Thus, if the output of U3B is to be the design value of 10 volts, the drop across the current sensing resistor will be -2.5 volts, i.e., a four-to-one ratio. Observe that the output of amplifier U3A must supply current through D28 to the virtual ground inverting input terminal of U3A, and will feed current through R31 to the current source. Also note that since D27 is reverse biased, no current flows through R50 and R49, since there is no potential difference across these resistors.

For the other polarity, the Ifb terminal will be +2.5 volts at rated load current. In this case, current flows from the source through R31 and through R37 to the virtual ground at the inverting input terminals of U3A and U3B. Current in R31 is sinked through resistor R49 and diode D27 to amplifier output U3A. In this case, D28 is reverse biased. Now the output of U3B is again positive and provides the necessary current through R45 and R46 to produce the virtual ground at the inverting input terminal of U3B. The two components of current, i.e., the one through R37 and the one through the series combination of R45 and R46, exit the inverting input junction terminal of U3B through resistor R50 and are also sinked by the output terminal of amplifier U3A.

It is thus seen that the output of U3B is designed to be +10 volts for either a positive or a negative current source input of 2.5 volts from the high voltage current feedback system. The output voltage of U3B is applied to the front panel milliammeter through resistors R43 and R44 in series, R44 being used as an adjustment to calibrate for any meter inaccuracies. The output voltage is also applied to the current monitor terminal through R42. The function of R42 is to prevent overload of the amplifier in the inadvertent short circuiting or overloading of the current monitor terminal. Finally, the output of U3B is applied to the current control amplifier to be described on the following page.

G. Feedback Control Amplifiers and Programming, Voltage and Current Regulators



The simplified schematic above shows the basic circuit elements of the voltage control and current control amplifier systems. Complete details for these circuits can be found by referring to the Driver Assembly schematic at the rear of this manual. The schematic reference designators shown in the above sketches correspond to the equivalent parts on the complete schematic. Only the key components are included in these sketches. The two circuits, voltage and current control, are quite analogous. We will describe only the voltage control amplifier in the following discussion. The voltage program and current program signals may be selected optionally by the user in several different manners, all of which have been described previously in Section II, Paragraph D.

The feedback loop is closed at the input of control amplifier U2B in a conventional comparator configuration. The programming voltage signal is applied through resistor R28 to the non-inverting input terminal of the amplifier. The output information from the voltage feedback follower amplifier is applied to the inverting input terminal of the control amplifier.

The circuit is similar to most closed loop configurations. The input signal, obtained as a portion of the reference voltage and referred to as programming voltage, is applied to one input of the control amplifier. The loop then drives the output voltage of the power supply to a level such that the signal returned from the feedback divider and follower amplifiers described in an earlier paragraph, and applied to the other input of the control amplifier, "nulls" the amplifier and balances the applied program voltage. The output of the control amplifier is used to control the pulse width modulator main driver, to be described below.

D22 is connected from the positive amplifier input terminal (after the voltage programming input resistor) to the voltage program clamp. Normally, this connection is made to the slider of the front panel ten-turn voltage control. Thus, if an external programming signal is applied to the power supply, it can be clamped by the front panel ten-turn control, thereby permitting this control to be used as an overvoltage limit. In other words, the setting of the front panel voltage adjust clamps the remote program signal, and limits the output voltage to a level corresponding to the setting on the front panel control.

In the current control amplifier, diode D36 in the output is the "crossover" element which permits the power supply to automatically change from a voltage mode to a current mode of operation. Thus, as long as the current programming input signal is greater than the actual output current feedback information, the output of amplifier U4B is "high", and diode D36 is back biased, and decoupled. When the load current, and the subsequent feedback follower information reaches the level of the current program signal, U4B amplifier goes into its dynamic range. Diode D36 is forward biased and the pulse width modulator control overrides that of the voltage amplifier.

Not shown on the simplified sketches above are the numerous protective diode clamps required to protect the circuitry under transient conditions. Also not shown is the automatic gain circuit, consisting of transistor Q3 and photocell U5. The gain is increased as the power supply load current increases, to achieve fast loop response and an improved ripple characteristic. The gain is reduced at light load, to stabilize the feedback loop under these operating conditions.

H. Pulse Width Modulator

U1 on the Driver Assembly is an integrated circuit which provides all the controls required to establish the pulse width modulator drive system. The next few pages of this instruction manual contain copies of the manufacturer's data sheets for the part used in this power supply. It is recommended that if this part needs replacement, the same manufacturer and manufacturer's part number be used. Any substitutions should be checked with the Glassman Engineering Department.

LINEAR INTEGRATED CIRCUITS

Advanced Regulating Pulse Width Modulators

UC1524A
UC2524A
UC3524A

FEATURES

- Fully interchangeable with standard UC1524 family
- Precision reference internally trimmed to ±1%
- High-Performance current limit function
- Under-voltage lockout with hysteretic turn-on
- Start-up supply current less than 4mA
- Output current to 200mA
- 60V output capability
- Wide common-mode input range for both error and current limit amplifiers
- PWM latch insures single pulse per period
- 200ns shutdown through PWM latch
- Guaranteed frequency accuracy

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

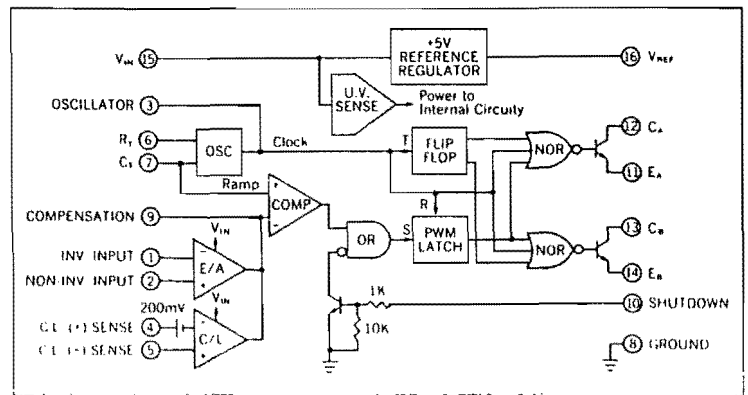
Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period even in noisy environments and a shutdown circuit feeding directly to the latch which will disable the outputs within 200ns. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from −55°C to +125°C. The UC2524A and UC3524A are available in either ceramic or plastic packages and are rated for operation from −25°C to +85°C and 0°C to 70°C, respectively.

ABSOLUTE MAXIMUM RATINGS

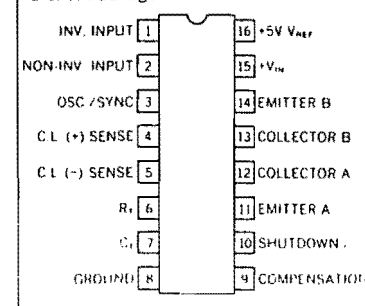
Supply Voltage (V_{IN})	40V
Collector Supply Voltage (V_C)	
UC1524A, UC2524A	60V
UC3524A	50V
Output Current (Each Output)	200mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T_A = +25°C	1000mW
Derate above +50°C	10mW/°C
Power Dissipation at T_C = +25°C	2000mW
Derate for Case Temperature above +25°C	16mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N Package



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25°C to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V_{IN} = V_C = 20V.)

PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Turn-on Characteristics								
Input Voltage	Operating range after Turn-on	8		40	8		40	V
Turn-on Threshold		6	7.5	8.5	6	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.6			0.6		V
Reference Section								
Output Voltage	T_j = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability*	Over Operating Range		20	50		20	50	mV
Short Circuit Current	V_{REF} = 0, T_j = 25°C		80	100		80	100	mA
Output Noise Voltage*	10hz ≤ f ≤ 10kHz, T_j = 25°C		40			40		μVrms
Long Term Stability*	T_j = 125°C, 1000 Hrs.		20	50		20	50	mV
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_j = 25°C	40	43	46		43		kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1 mfd			120			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470 pF	500			500			kHz
Output Amplitude*	T_j = 25°C		3.5			3.5		V
Output Pulse Width*	T_j = 25°C		0.5			0.5		μs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley		0.7	0.9	1.0	0.7	0.9	1.0	V
Error Amplifier Section (Unles otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current			.05	1		0.5	1	μA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	60	75		60	75		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
Open Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10 Meg Ω	72	80		60	80		dB
Gain-Bandwidth*	T_j = 25°C, A_V = 0dB		3			3		MHz

* These parameters are guaranteed by design but not 100% tested in production.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1524A, −25°C to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V_{IN} = V_C = 20V.)

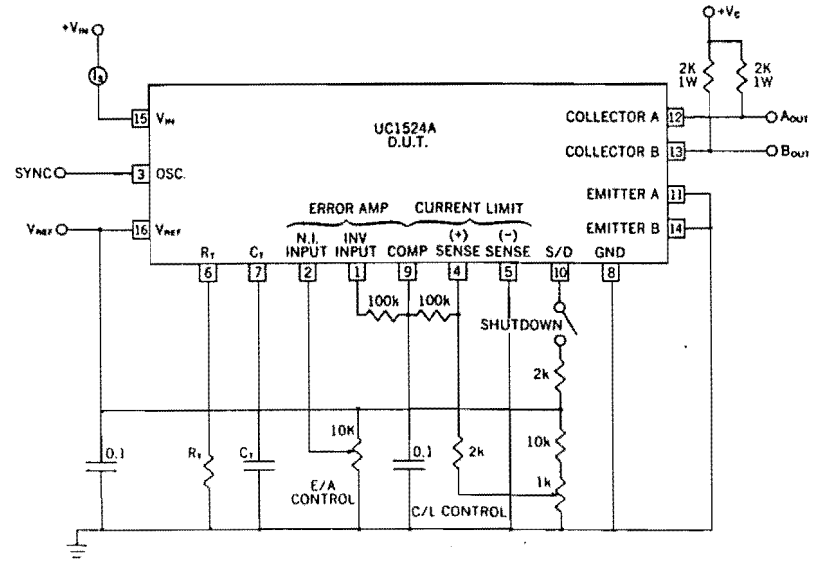
PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Amplifier (Unless otherwise specified, Pin 5 =0V)								
Input Offset Voltage	T_j = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
Input Offset Voltage	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	μA
Common Mode Rejection Ratio	$V_{(Pin\ 5)}$ = −0.3V to +5.5V	50	60		50	60		dB
Power Supply Rejection Ration	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
Open Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10 Meg Ω	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100μA	60	80		50	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	μA
Saturation Voltage	I_C = 20mA I_C = 200mA		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_j = 25°C, R = 2K Ω		200			200		ns
Fall Time*	T_j = 25°C, R = 2K Ω		100			100		ns
Comparator Delay*	T_j = 25°C, Pin 9 to Output		300			300		ns
Shutdown Delay*	T_j = 25°C, Pin 10 to Output		200			200		ns
Shutdown Threshold	T_j = 25°C, R_C = 2K Ω	0.5	.7	1.0	0.5	.7	1.0	V

* These parameters are guaranteed by design but not 100% tested in production.

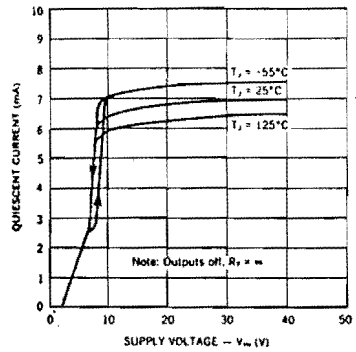
OPEN-LOOP TEST CIRCUIT

Note: The UC1524A should be able to be tested in any 1524 test circuit with two possible exceptions:
1. The higher gain-bandwidth of the current limit amplifier in the UC1524A may cause oscillations in an uncompensated 1524 test circuit.
2. The effect of the shutdown, pin 10, cannot be seen at the compensation terminal, pin 9, but must be observed at the outputs.

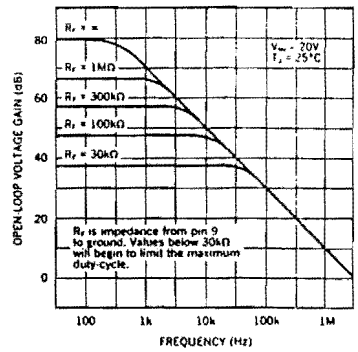
The circuit below will allow all UC1524A functions to be evaluated.



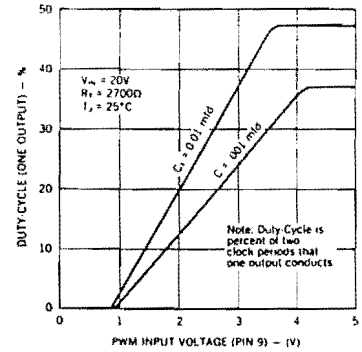
Supply Current vs Voltage



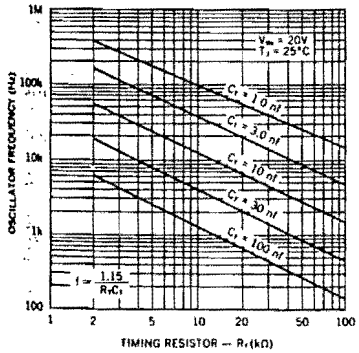
Error Amplifier Voltage Gain vs Frequency



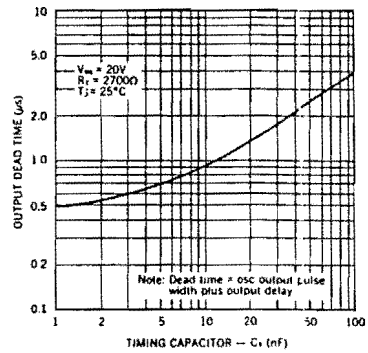
Pulse Width Modulator Transfer Function



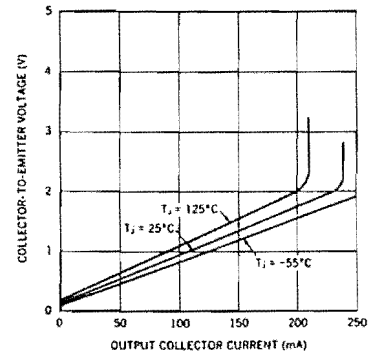
Oscillator Frequency vs Timing Components



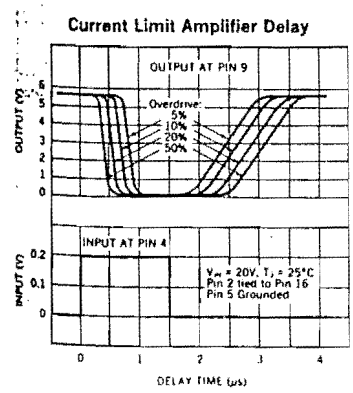
Output Dead Time vs Timing Capacitor Value



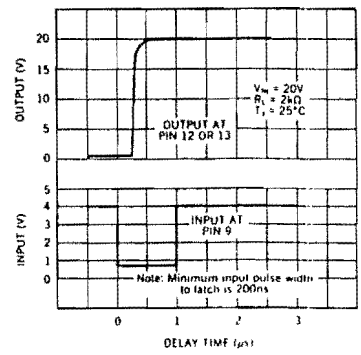
Output Saturation Voltage



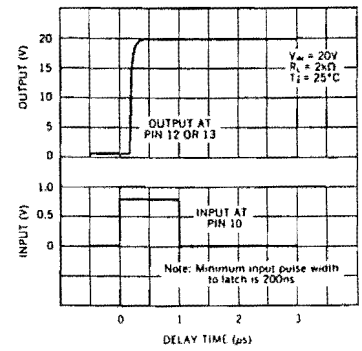
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator — Pin 9



Turn-Off Delay From Shutdown — Pin 10



Recent Advances in IC Switching Power Supply Controllers Reach New Performance Levels While Reducing System Costs

by
Robert Mammano, Vice President of Engineering
Unitrode Integrated Circuits Corporation

High frequencies, more output power, easier interfacing, better fault sensing, lower internal power losses, greater accuracy, increased predictability, and more self-contained features: These are the improvements power supply designers have been demanding of IC technology in order to reduce their overall system costs. Efforts toward accomplishing these goals have been directed both toward improving existing products as well as developing new devices to significantly extend the state of the art. This article introduces the results of this activity by describing a newly redesigned IC controller and illustrating its benefit to the power supply engineer.

Building a successful switching power supply has always represented a battle against cost. It was the high cost of implementing switching technology which most often dictated linear power supplies in the past. While tremendous strides have been made in improving performance and reducing costs of components, the battle is far from over. Every time a designer sits down to develop a new power system, his major task is usually not how to solve a technical problem but how to implement the design in a cost-effective manner. The designer only wins if his resultant power supply is competitive in the marketplace, regardless of whether it's a stand-alone power source or part of a larger system.

The introduction of integrated circuit pulse-width modulator (PWM) controllers has made significant contribution to lowering switching power supply costs by reducing much of the regulator circuit complexity to a single chip. There have been so many developments in this area that one might suspect all potential gains have already been achieved. However, open any switching power supply on the market today and one will still see a fairly large P.C. board containing a multitude of discrete control components. Although significant improvements have been made, the ultimate IC controller chip has yet to be defined.

IC CONTROLLERS

The application of IC technology to the switching power supply began with the introduction of the SG1524 in 1976. This device, whose block diagram is shown in Figure 1, was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straightforward approach to the classic PWM architecture gave it wide acceptance, and it has become the most widely used IC controller today.

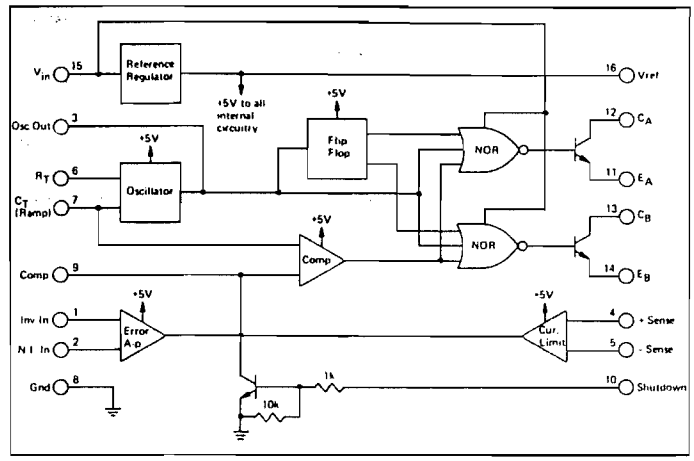


FIGURE 1. The UC1524 Pulse Width Modulator Block Diagram

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times cursed the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real world of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

The TL494 was introduced to provide better analog instrumentation for voltage and current sensing and increased output power, and it won many converts. But it also suffered from a need for external support and protection circuitry to incorporate it within a practical power supply.

A second generation circuit, the SG1525A was developed for more optimum utilization in specialized applications. This part was the first IC controller circuit to incorporate a trimmed 1% reference and a PWM latch for jitter-free operation in noisy environments. The 1525A also featured totem-pole outputs for turn-off, as well as turn-on commands. While this improved interfacing in some applications, it sacrificed some of the flexibility offered by the 1524s uncommitted outputs.

A third generation circuit, the SG1526, provided further improvements such as more internal protection circuitry and a wide-range current limiting amplifier at the cost of considerable complexity and increased internal power losses.

(please turn to page 16)

Recent Advances in IC Switching

(continued from page 14)

Another choice offered power supply designers was the NE5560, whose major advantage was the capability for input voltage sensing for constant volt-second operation. While greatly improving line regulation, this device offered only a single, low-current output.

With the availability of all the above devices, plus several other "also-rans", design engineers now have a wide range of choices from which to select the IC which results in the lowest system cost for their particular application. In an attempt to understand more about these decisions, an independent survey was conducted last October, with 122 individuals from 97 different companies, representing both power supply manufacturers and captive design groups within OEM companies. The survey asked, among other questions, which is the preferred IC controller chip. The results of this survey are shown in Figure 2.

With some 42% of the users preferring the 1524 family, it seemed appropriate to take a closer look at the reasons. A key factor in the 1524s acceptance appeared to be the wide versatility offered by its easy-to-understand PWM architecture. From this study it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. Thus, Unitrode undertook this task. The result is the UC1524A.

THE UC1524A PWM CONTROLLER

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be a cost advantage in using the UC1524A in new designs. The block diagram of the UC1524A is shown in Figure 3, which, by intent, looks very similar to the diagram of Figure 1.

The list of improvements, however, is considerable and includes the following:

•The 5V reference is now internally trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments.

•The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.

•A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.

•An under voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.

•A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds directly to this latch which will disable the outputs within 200nsec of activation.

•The oscillator circuit is usable to frequencies beyond 500kHz and is easier to synchronize with an external clock pulse.

•The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

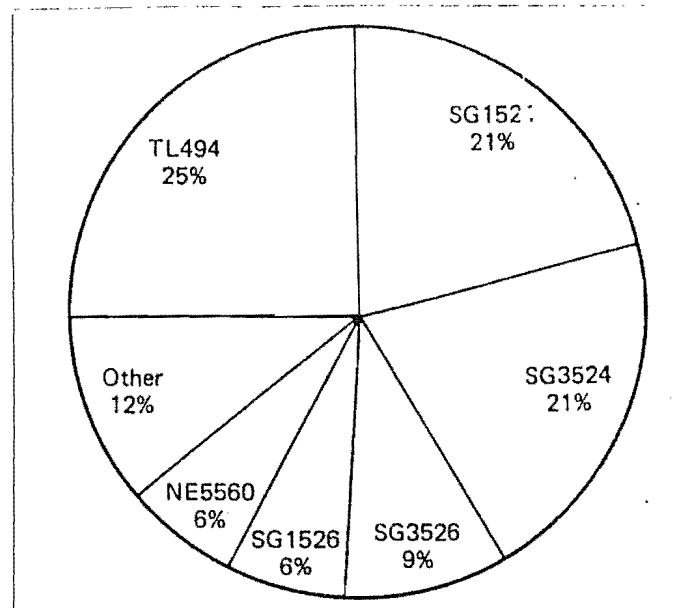


FIGURE 2. Results of a 1981 Survey of Control IC Usage by Part Number Shown by Percent of Engineer Responses

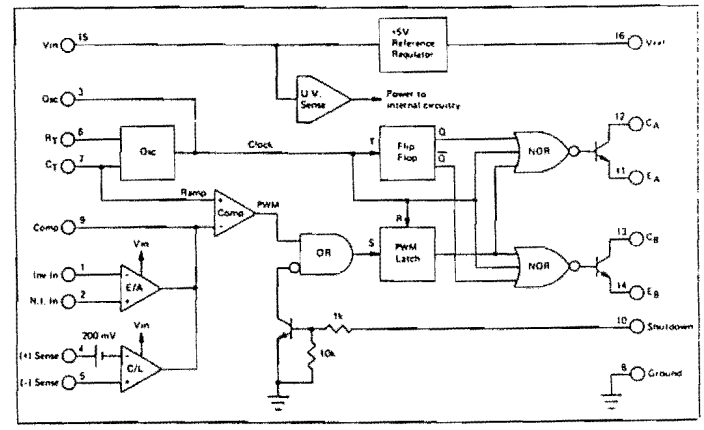


FIGURE 3. The UC1524A Block Diagram follows the same Architecture as the UC1524 but with Several Significant Differences

INTERNAL POWER TURN-ON CIRCUIT

The undervoltage lockout and turn-on hysteresis circuit is shown in Figure 4. This circuit requires approximately 2V for activation; and, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_{in} rises above 2V, R1 begins to conduct saturating Q3 and holding the base of Q5 too low to allow any of the current sources to conduct. The current through R3 flows through Q3 and R2, developing a 600mV drop across R2 when Vref reaches 5V. At this level, the only current

flowing is that used by the reference regulator and R1 and R3, a total of approximately 2.5mA at turn-on threshold.

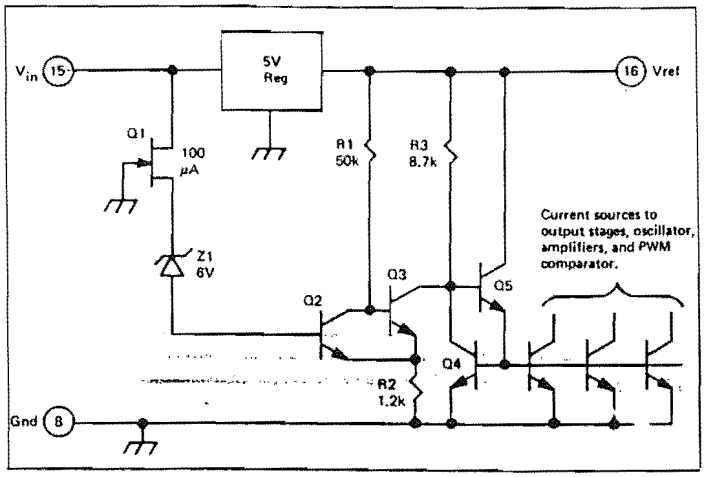


FIGURE 4. The Undervoltage Lockout and Power Turn-On Circuitry within the UC1524A

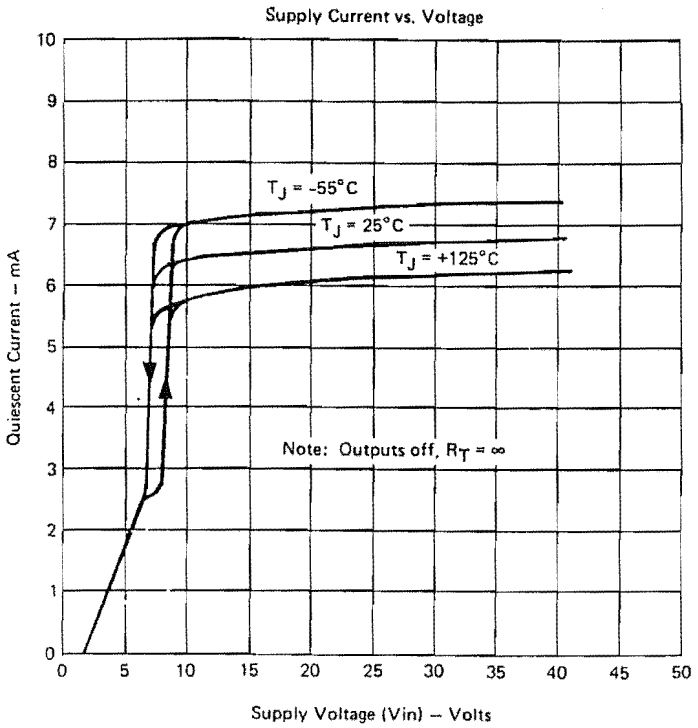


FIGURE 5. Supply Current for the UC1524A vs Input Voltage

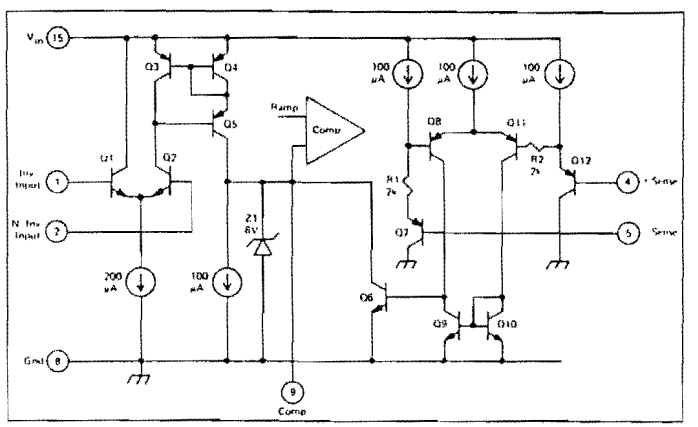


FIGURE 6. Voltage and Current Sensing Amplifiers have a Common Output at the Input to the PWM Comparator

When the input voltage reaches approximately 8V, Z1 begins to conduct turning on Q2 which turns off Q3 and allows the current sources to activate. Since the current through Q2 is much less than through Q3, the voltage across R2 drops providing positive feedback. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 5 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with bootstrapped operation after turn on.

A NEW CURRENT LIMIT AMPLIFIER

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 6. Since the error amplifier, consisting of transistors Q1 through Q5, must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524A with one exception: It is now powered by V_{in} instead of Vref, so that the input common-mode range extends to within 2V of either rail. Zener diode, Z1, is used on the output to keep the input level to the PWM comparator below 6V.

The error amplifier's output can be considered a 100µA current source or sink (0 - 200µA source with 100µA constant sink). When the current limit circuit activates, Q6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

The current limit circuit consists of Q6 through Q12. Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within 2V of V_{in}. Its threshold, or offset, of 200mV is established by the 100µA current source through R1, with R2 added to null out the effect of any base current from Q8.

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600nsec. This can be decreased substantially with additional overdirve. Use of the current sensing block as a comparator is usually preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the 100µA pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stablization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 7.

An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 8. If R1 is made 100k, there will be minimal effect upon the error amplifier gain.

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Recent Advances in IC Switching

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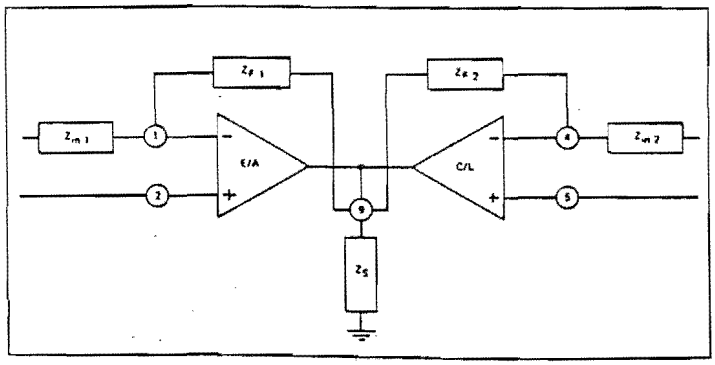


FIGURE 7. Various Compensation Options which are Possible when both Amplifiers are Operated in the Linear Mode.

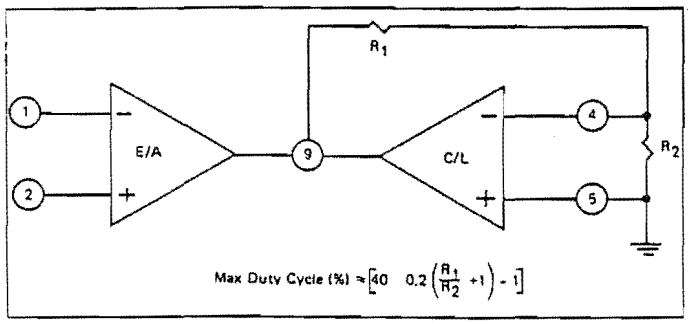


FIGURE 8. The Fixed 200mV Threshold of the Current Limit Amplifier can be Multiplied to form a Duty-Cycle Clamp, or Dead-Band Control

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin 10. While the input threshold of this circuit is not as accurately controlled, has a negative temperature coefficient of −2mV/°C and is internally ground referenced; it does feed directly into the PWM latch with only 200nsec delay from activation of pin 10 to shutdown of the outputs.

PWM COMPARATOR AND LATCH

The PWM latch insures only a single pulse is allowed to the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to blank the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

There are several significant advantages to this circuit. First, the latch completely eliminates multiple outputs of the PWM comparator because of noise or ringing on the output of the error amplifier causing multiple crossings of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

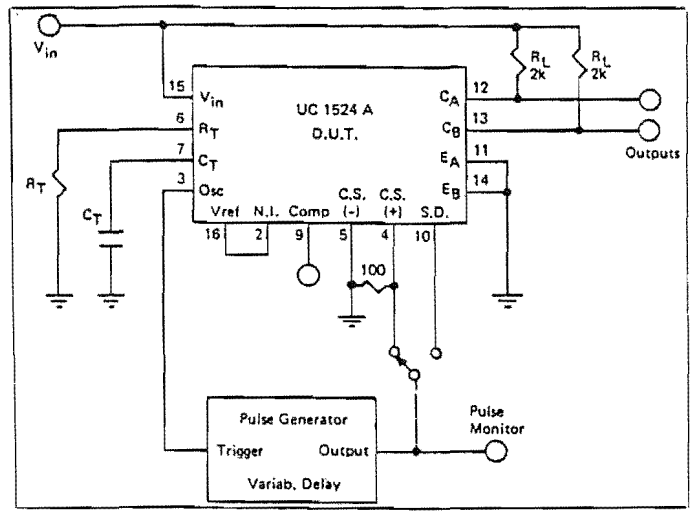
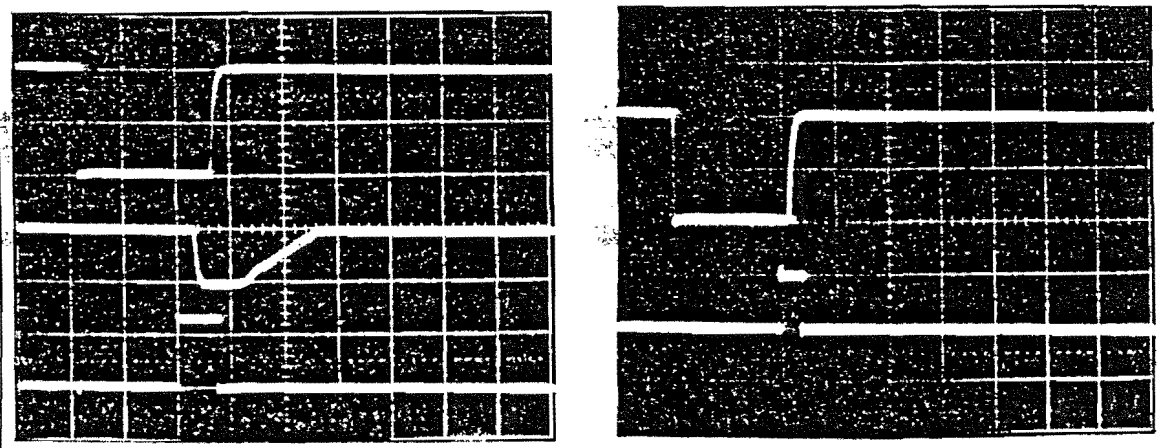


FIGURE 9. Evaluating the Turn-Off Delays of the UC1524A with the aid of a Triggerable Pulse Generator with Variable Delay

The performance of this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, setup as shown in Figure 9. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The



Lower — Current sense input, 200 mV/div
Middle — Comp output, 5V/div
Top — Output, 10V/div
Time — 1 μsec/div

Lower — Shutdown input, 1V/div
Upper — Output, 10V/div
Time — 1 μsec/div

FIGURE 10. Typical Turn-Off Response from both the Current Sense and Shutdown Inputs

output pulse width must be at least 200nsec and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 10.

HIGHER POWER OUTPUT SWITCHES

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirements, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay. Saturation voltage as a function of current is shown in Figure 11.

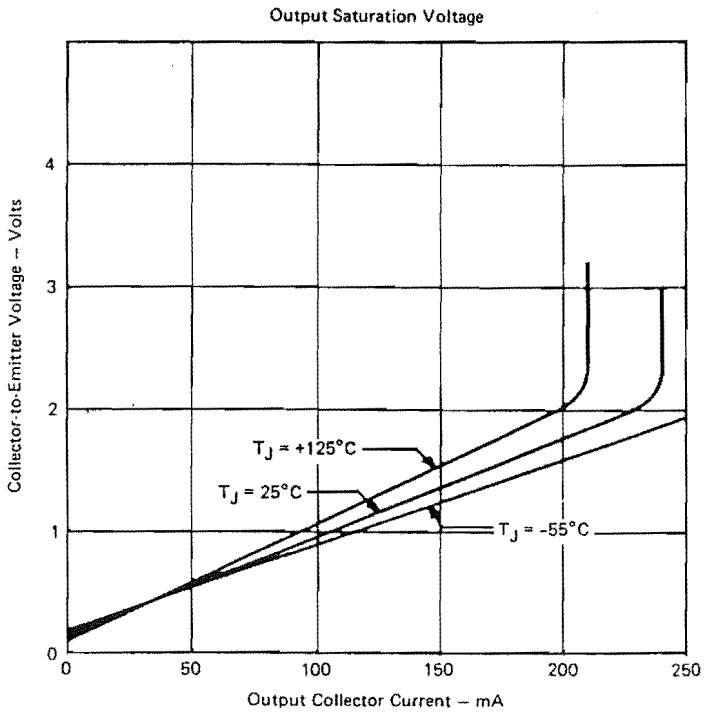


FIGURE 11. Output Saturation Characteristics for each of the UC1524A's Outputs

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful configuration for enhanced turn-off is shown in Figure 12. The signal appearing at the drive current limiting resistor, R1, is capacitively coupled to saturate an external transistor, Q2, greatly reducing the turn-off delay of Q3. Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

FREQUENCY SYNCHRONIZATION

The oscillator circuit within the UC1524A, shown in Figure 13, has been improved over that of the 1524 with the addition of C2. Without this component, a synchronizing pulse externally applied to pin 3 had to do all the

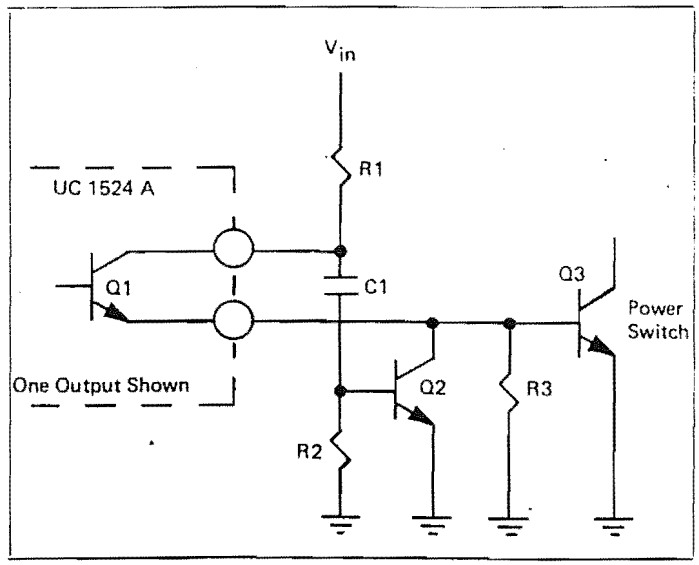


FIGURE 12. The Addition of C1 and Q2 uses the Collector Signal of the UC1524A to generate an Enhanced Turn-Off Command for Q3

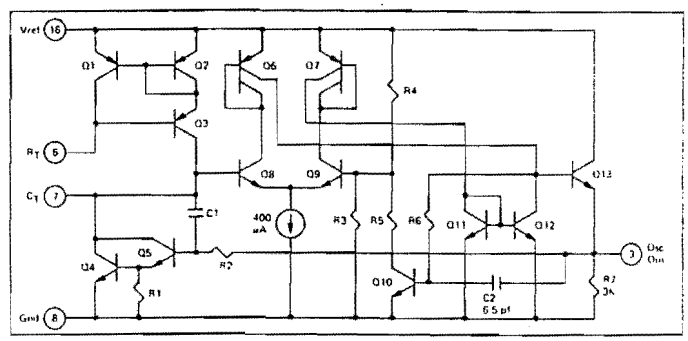


FIGURE 13. The Oscillator Circuit of the UC1524A allows both High Frequency Operation and Ease of External Synchronization

work of discharging the timing capacitor through Q4 and Q5. The simple addition of C2 couples a positive pulse from pin 3 to the base of Q10, momentarily reducing the threshold of comparator Q8-Q9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

As with the 1524, synchronization to an external clock should be done with the R_TC_T time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the components. For synchronizing multiple UC1524A devices, all R_T, C_T, and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pf from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load from pin 3 to ground of 1 kohm minimum will reduce the pulse width.

A SIMPLE BUCK REGULATOR CIRCUIT

The application of Figure 14 demonstrates the utility of the UC1524A used with a PIC600 hybrid switch. This combination greatly simplifies the design of switching regulators, since the only other active device required is a small-signal 2N2222 which serves to provide a constant

Recent Advances in IC Switching

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drive current to the output switch, regardless of the input voltage level. With the UC1524A, current sensing does not have to be done in the ground line, but will still function when the regulator output is shorted to ground.

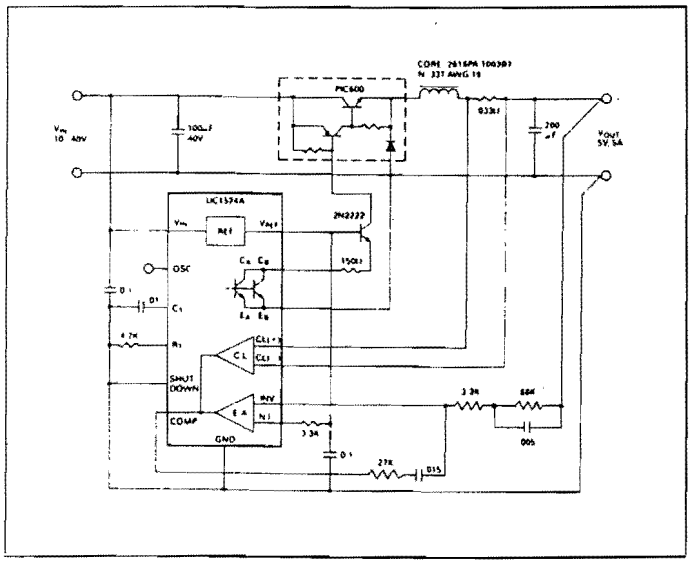


FIGURE 14. The UC1524A combines with the PCI 600 Hybrid Switch to for a simple but powerful Buck Regulator

The waveforms of Figure 15 demonstrate the performance of the current limiting comparator, showing that from the onset of current limiting to a complete short circuit, the peak input current increases from 5.2A to only 5.9A.

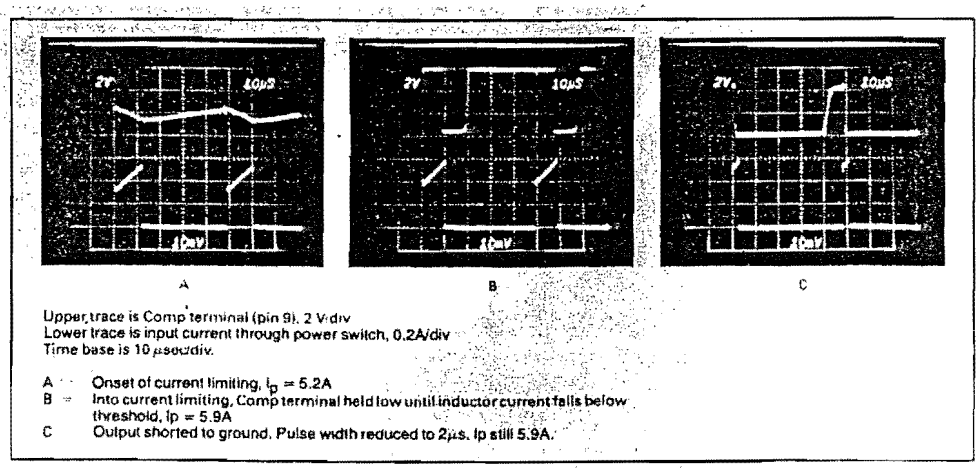


FIGURE 15. Performance Data for Figure 14's Regulator shows the Tight Control of Peak Current, even under Shorted Output Conditions

AN OFF-LINE FLYBACK APPLICATION

The circuit of Figure 16 demonstrates several of the new features of the UC1524A. Since this IC needs less than 4mA prior to turn on, capacitor C2 is charged through a relatively high-value R1 until the start voltage is reached. At that time, C2 provides the energy to activate the switching circuitry. Feedback winding N2 then picks up the drive power with R1 retaining less than 2W of steady-state power loss.

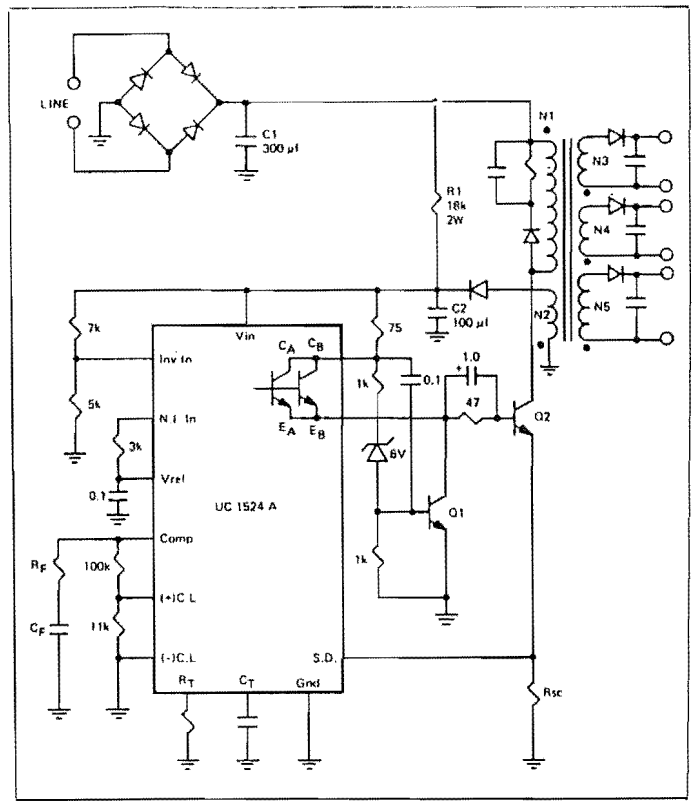


FIGURE 16. An Off-Line, Primary-Side Control for a 50W Flyback Converter

Since this is a flyback application, the duty cycle must be less than 50%, and the current limit amplifier is used as a clamp, with current sensing being performed by the shutdown pin. The added interface circuitry is provided for high-speed turn-off of the main power switch, Q2, as described earlier.

With the voltage feedback loop closed to the feedback winding, N2, regulation will only be as good as the coupling between N2 and the other output windings. While at least 10% regulation can be achieved in this manner, an added optical coupler to provide isolated feedback from the high-current output could improve regulation to better than 1%.

CONCLUSION

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it never hurts to review older ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement: providing greater performance and versatility while reducing system costs.

η

I. Protection and Other Miscellaneous Circuits

1. External Interlock

This circuit takes advantage of the interlock feature of the pulse width modulator. Note that pin 10 of U1 is connected to the external interlock terminal through connector J1-18. If this terminal is open, then pin 10 of U1 is connected to the internal 5 volt reference at U1 pin 16 through resistor R61. This configuration overrides all internal functions of U1 and prevents any output drive. When pin 10 is connected to common, U1 can go into its normal operating mode. The user may wish to have a remote safety switch for a test cage or other control purpose. The rear panel barrier terminal board jumper may be removed and replaced by a switch located at a remote point. The switch must be rated to make and break 50VDC at 50mA resistive load. The switch must be in the closed or shorted position to enable the power supply.

For models above 60kV, an additional interlock feature is added to assure that the interconnection cable between the control chassis and the high voltage chassis is in place. In this circuit, pin 10 of U1 is connected (via J1-18 of the Drive Assembly) to J1-E, through the interconnection cable to J1-E of the High Voltage Assembly. A jumper connection between J1-E and J1-D of the High Voltage Assembly allows the circuit to continue from J1-D of the High Voltage Assembly back to J1-D of the control chassis and then to TB1-3.

Pin 10 of U1 is also connected to J2-1 through resistor R75. As noted on the Driver Assembly schematic, this line is used for TTL logic control when this option is specified.

2. Slow Start Circuit

The RC network of R21 and C13 is charged by a 15VDC regulated supply when power is initially applied. The voltage programming signal at pin 5 of U2B is clamped to the slowly rising voltage at C13 by the forward bias action of D11, allowing the voltage at pin 5 to increase as a function of the time constant in the RC network. When the voltage at the slow start capacitor C13 reaches the voltage programming level, D11 becomes reverse biased, and the capacitor is decoupled from the voltage programming.

3. SCR Cutoff Protection Circuits

D43 is an SCR which, when gated and latched, disables the power supply output voltage by removing the drive signal from the pulse width modulator controller U1. This is accomplished as follows:

When D43 is turned on, the base drive current provided by

R22 and through diode D46 is sinked by the SCR. This action releases R23 to provide base drive through D48 to Q5, turning on transistor Q5. This removes the drive signal to U1 pin 2 by sinking the current in R24,thereby preventing the pulse width modulator from delivering any output pulses, and maintaining the power supply in an off state.

The SCR can be triggered by any of the following possibilities.

a. Current Trip Option

When specified by the user's order, this option is included by adding the circuitry enclosed in the dotted box labeled CURRENT TRIP on the Driver Assembly schematic. The circuit functions exactly the same as the standard "current limit" feature, except that when current amplifier U4B switches "down" in response to an over-current condition, transistor Q7 turns on and provides current to trigger the gate of SCR D43. The SCR latches and must be reset by removing AC input power and then re-energizing.

b. Overcurrent Protection/B+ Current Sensing

The B+ current sensing circuit prevents damage to the main power drive module, A3, due to excessive loads or short circuits. Observe on the Driver Assembly schematic that the base of Q5 is connected to terminal J1-17 through diodes D38 and D29. The Main Assembly schematic shows that this connection is transformer-coupled to the current source feeding the main power drive module. Thus, pulse voltage is developed which is proportional to the peak input current of the power module. When this current is excessive, the calibrated voltage, determined by the transformer-coupled signal and resistance divider information in sub-assembly A5, is sufficient to turn on Q5. With Q5 on, the voltage level at pin 2 of U1 is low, and the pulse width modulator output is turned off. The output of U1 remains off until the base voltage on Q5 is released.

Some models are provided with a remote reset through J1-16, which bypasses the SCR holding current to common.

4. Mode Indicating Lights

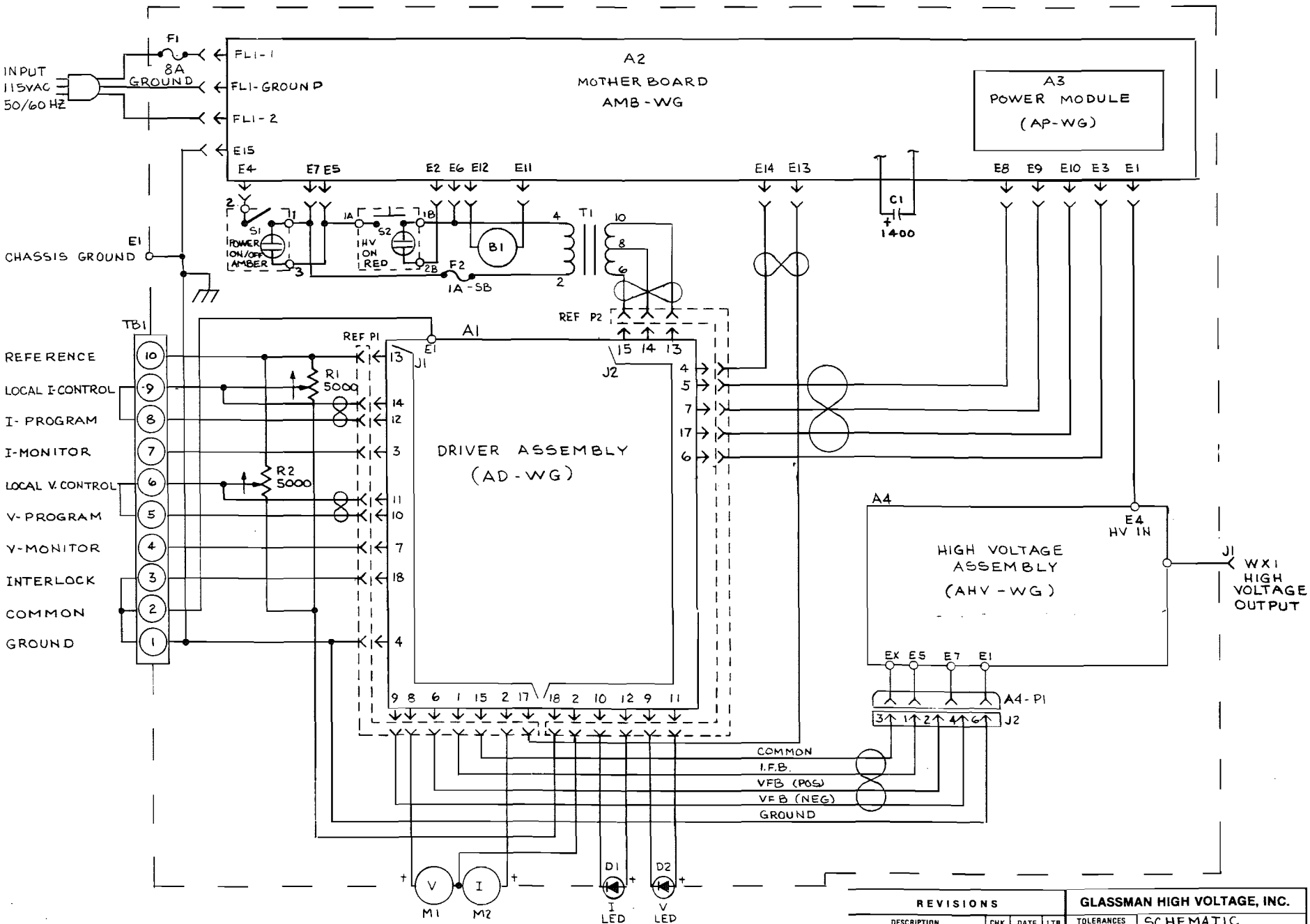
In an earlier paragraph, we have noted that the +15 volt source is used to provide power to the mode indicators. This is accomplished through dropping resistor R65 for the current lamp via terminal J2-12 and through R66 and D21 for the voltage lamp through J2-11. The operation of the lamps

is as follows. Normally, let us assume that the power supply is in a voltage mode. In this case, the voltage lamp is energized by the current flowing through R66, D21, terminal J2-11, the positive terminal of the voltage LED CR4, and terminal J2-9 (common). The current pilot lamp is not drawing current in this mode. The circuit path includes R65, to J2-12, to the lamp, returning to J2-10, and finally returning to common through transistor Q8. No current flows because the base of transistor Q8 is not forward biased.

Now consider the circuit changes when the power supply goes into a current mode. The output of the voltage amplifier U2B goes full positive. In this condition, base drive is provided to transistor Q8 through R67 and zener diode D19, turning on transistor Q8. When this occurs, the current pilot lamp conducts and is illuminated. Simultaneously, it will be observed that the collector of Q8 removes the current source from the voltage pilot lamp by back-biasing diode D21 through the conduction of R66 and D20 into the collector of Q8, so that the voltage mode pilot lamp turns off.

5. AC Line Overvoltage

When AC input exceeds approximately 130 volts RMS, the output of pulse width modulator U1 is cut off. This is accomplished when zener diode D14 removes drive from U1 pin 1 because the -25VDC unregulated source has increased in magnitude.



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GLASSMAN HIGH VOLTAGE, INC.

TOLERANCES DEC ± FRAC ±		SCHEMATIC MAIN ASSEMBLY WG SERIES AM-WG-01	
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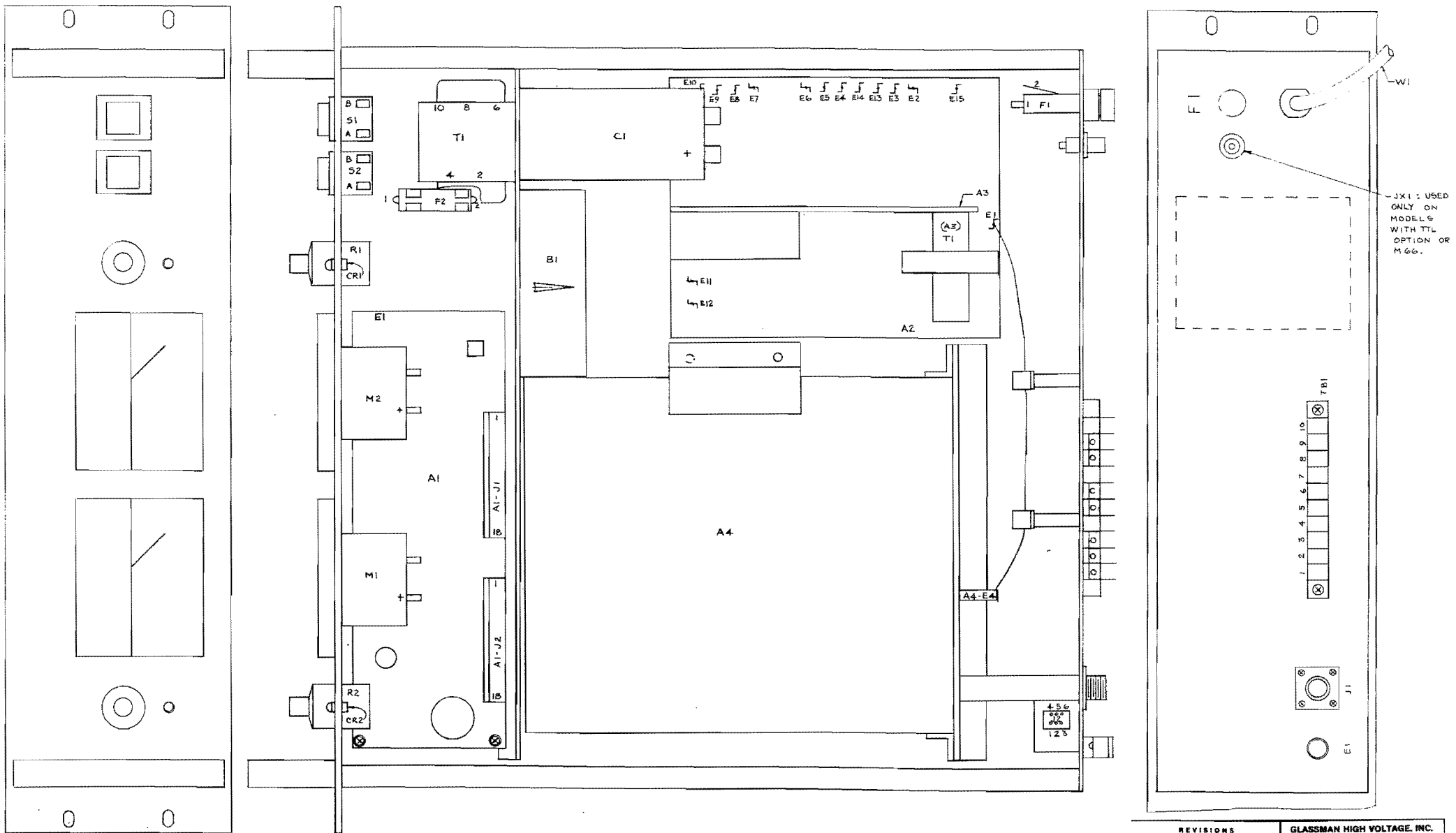
	12-1-86		



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MAIN ASSEMBLY
WG SERIES
(AM-WG-01)

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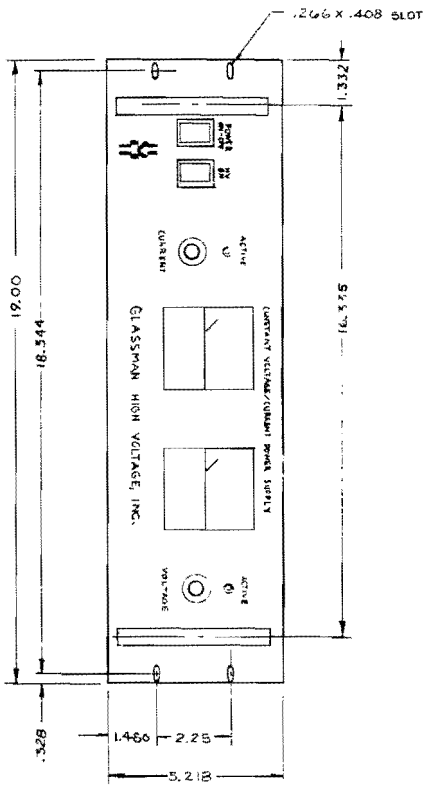

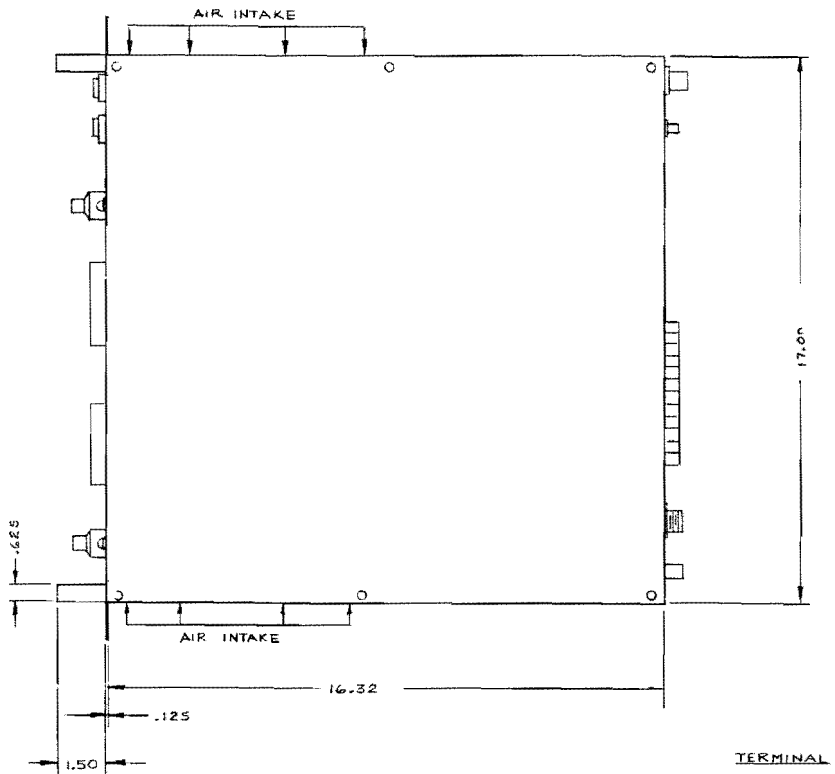

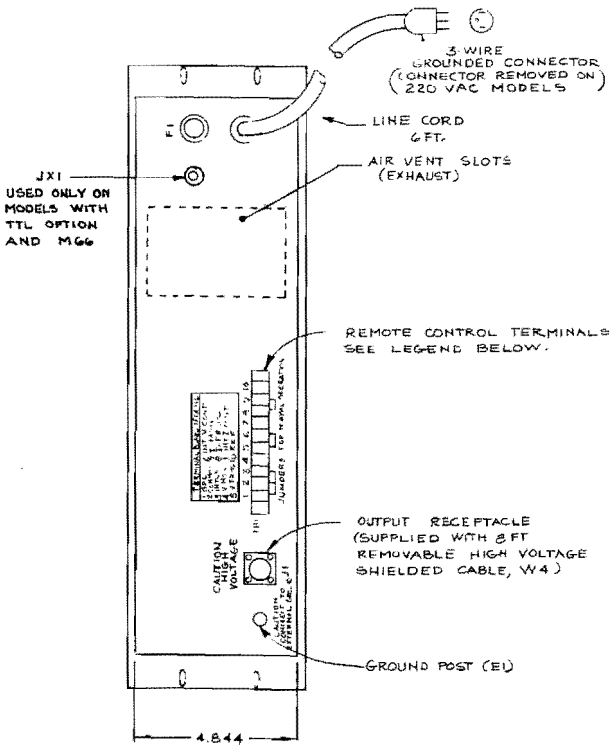

TERMINAL BOARD LEGEND

1 GROUND	6 INTERNAL VOLTAGE CONTROL
2 COMMON	7 I-MONITOR
3 INTERLOCK	8 I-PROGRAM
4 V-MONITOR	9 INTERNAL CURRENT CONTROL
5 V-PROGRAM	10 REFERENCE

NOTE:
FOR NORMAL OPERATION, JUMPER 1-2-3, 5-6, 8-9. SEE INSTRUCTION MANUAL FOR ADDITIONAL DETAILS.

REVISIONS			
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ECN 1977; FLOW WAS 16.875	MES	8-3-89	C

GLASSMAN HIGH VOLTAGE, INC.

TOLERANCES: DEC ± , FRAC ±

OUTLINE & INTERFACE MODEL WG SERIES SINGLE CHASSIS DESIGNS (AM-WG-01)

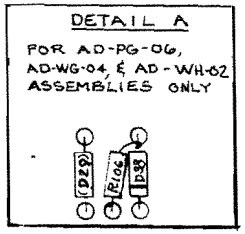
Drawn: MES 8-23-89 | Check: | Date:

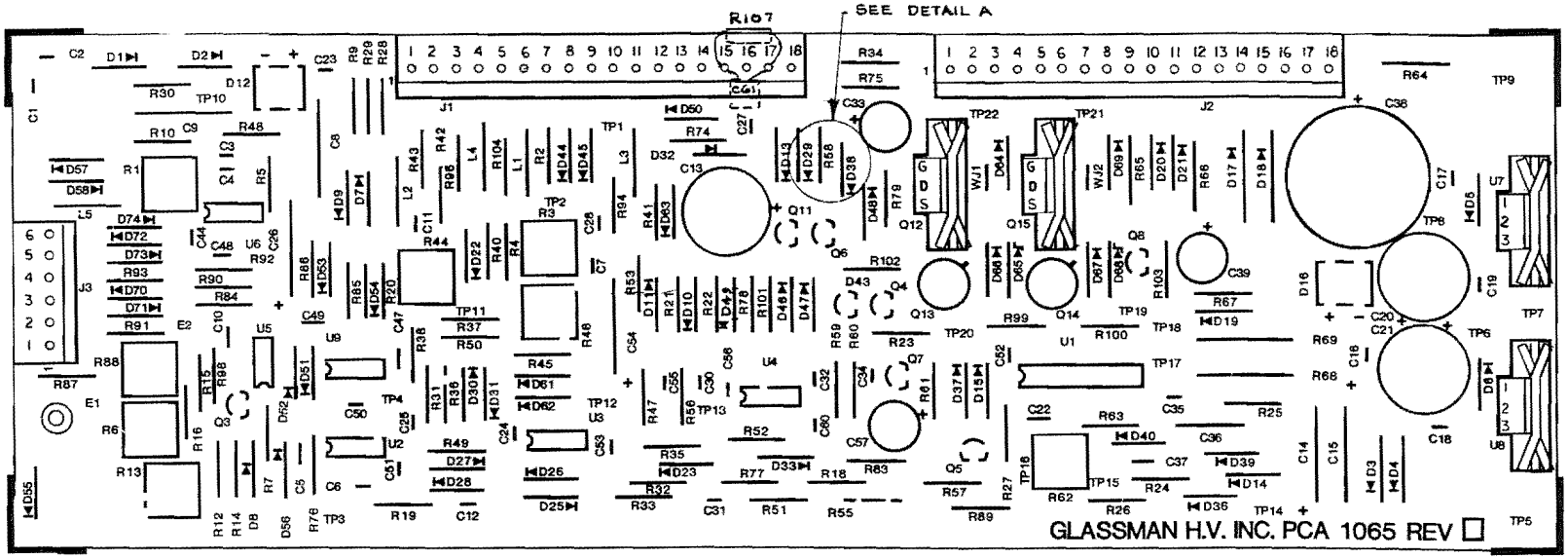
DRAWING NO. 401126-001 | REV C

SIZE HALF | Sheet 1 of 1

DETAIL A

FOR AD-PG-06, AD-WG-04, & AD-WH-62 ASSEMBLIES ONLY





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GLASSMAN HIGH VOLTAGE, INC.

TOLERANCES: DEC ±, FRAC ±

PARTS PLACEMENT DRIVER BOARD PG, WG, WH SERIES AD-PG-05, PG-06, WG-03, WG-04, WH-02

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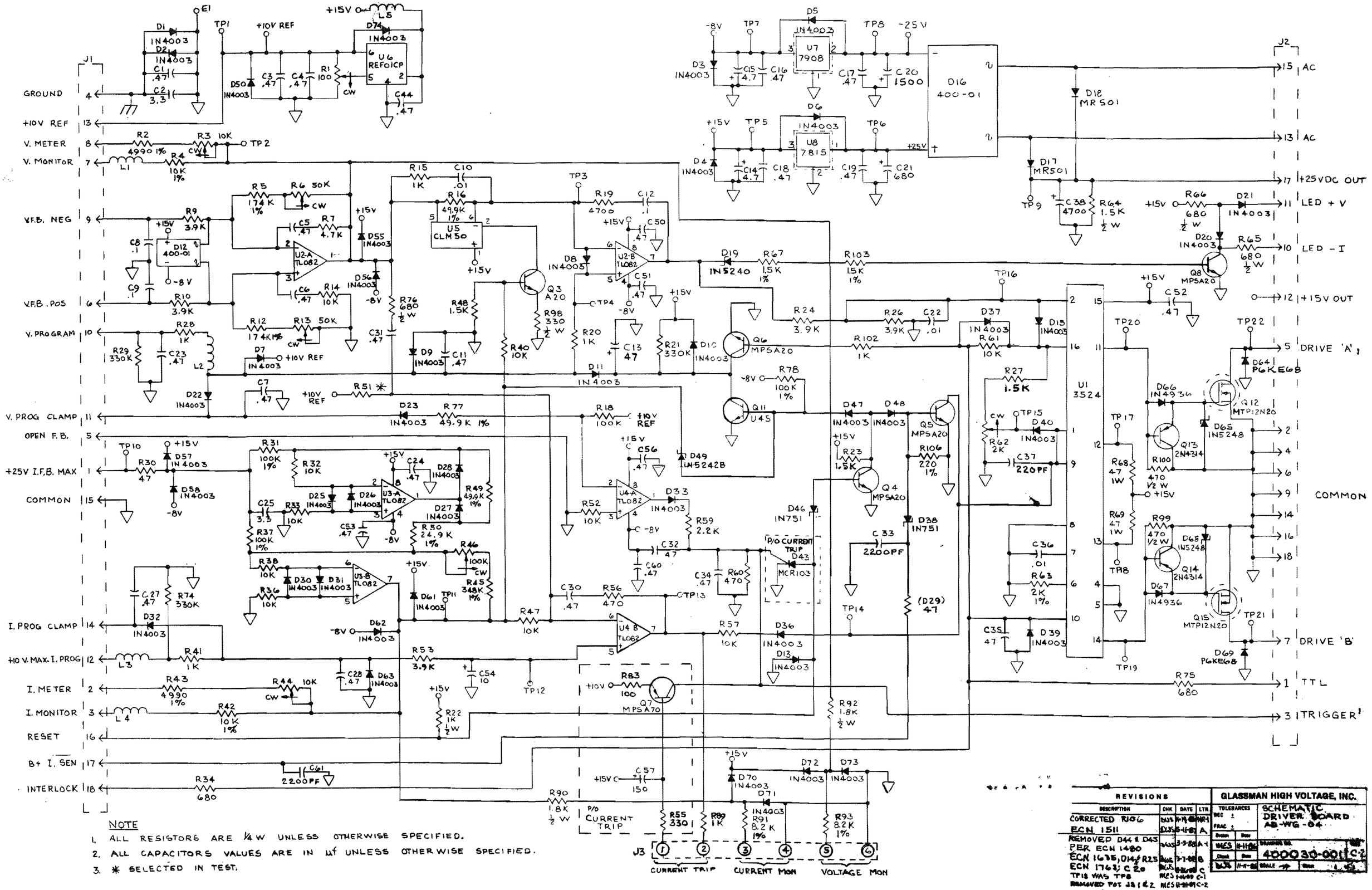
SCALE: Sheet 1 of 1



NOTE

1. ALL RESISTORS ARE ¼ W UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS VALUES ARE IN µf UNLESS OTHERWISE SPECIFIED.
3. * SELECTED IN TEST.

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ECN 1635, D14, R25	MES	7-7-88	B
ECN 1763; C 20	MES	8-26-88	C
TP18 WAS TP8	MES	11-09	C-1
REMOVED POT J3 & 2	MES	11-29-91	C-2

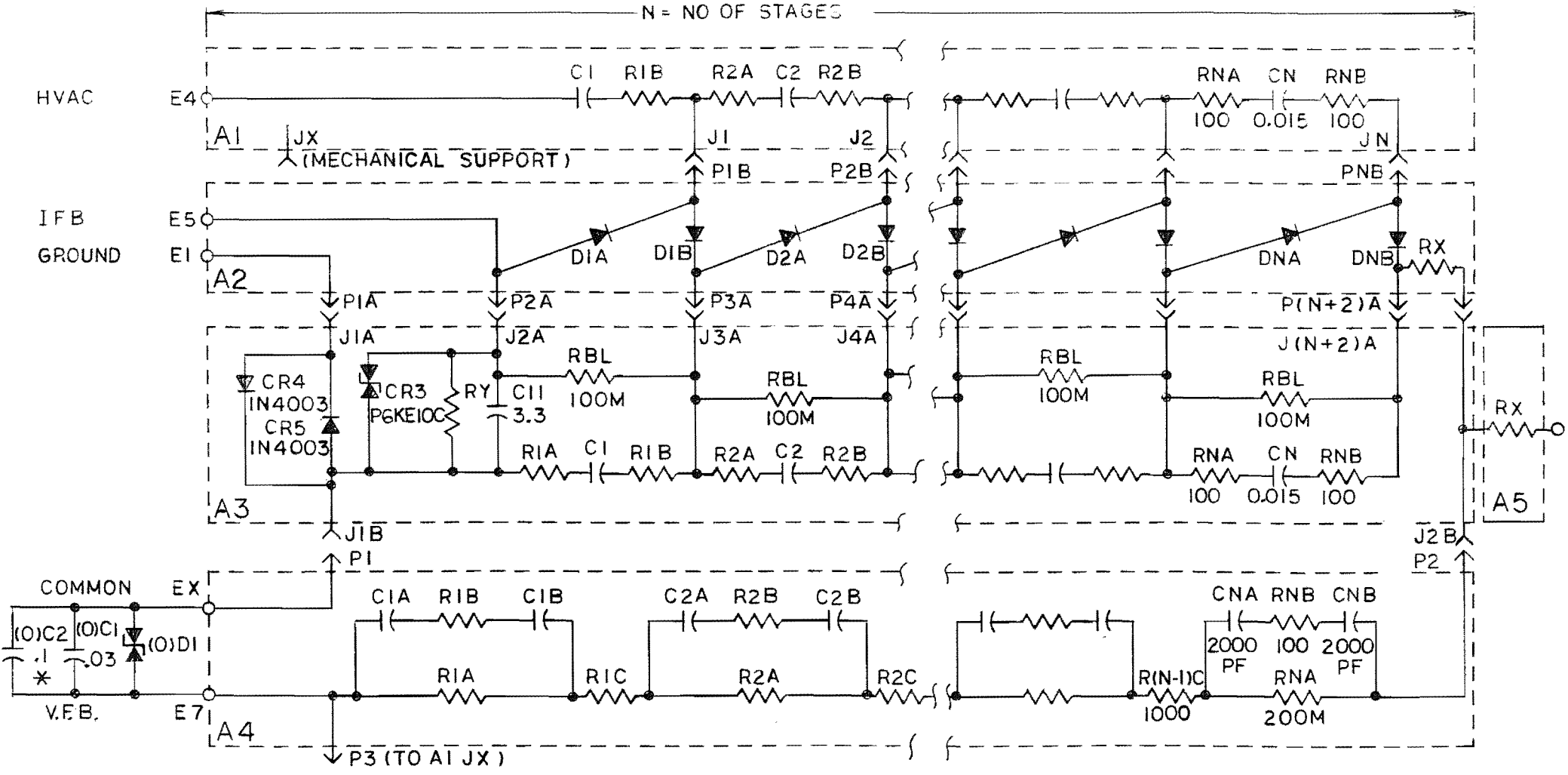
GLASSMAN HIGH VOLTAGE, INC.

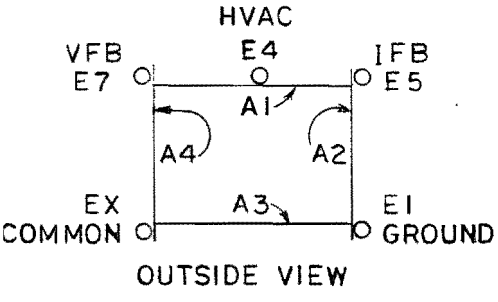
TOLERANCES DEC ± FRAC ±

SCHEMATIC DRIVER BOARD AB-WG-04

DRAWING NO. 400030-001 REV C-2

DRAWN MES 11-11-86 SCALE NONE SHEET 1 OF 1





NOTES:

1 - DIODES SHOWN FOR POSITIVE POLARITY; REVERSE FOR NEGATIVE POLARITY.

2 - * (0)C2 USED ONLY ON 5KV UNITS.

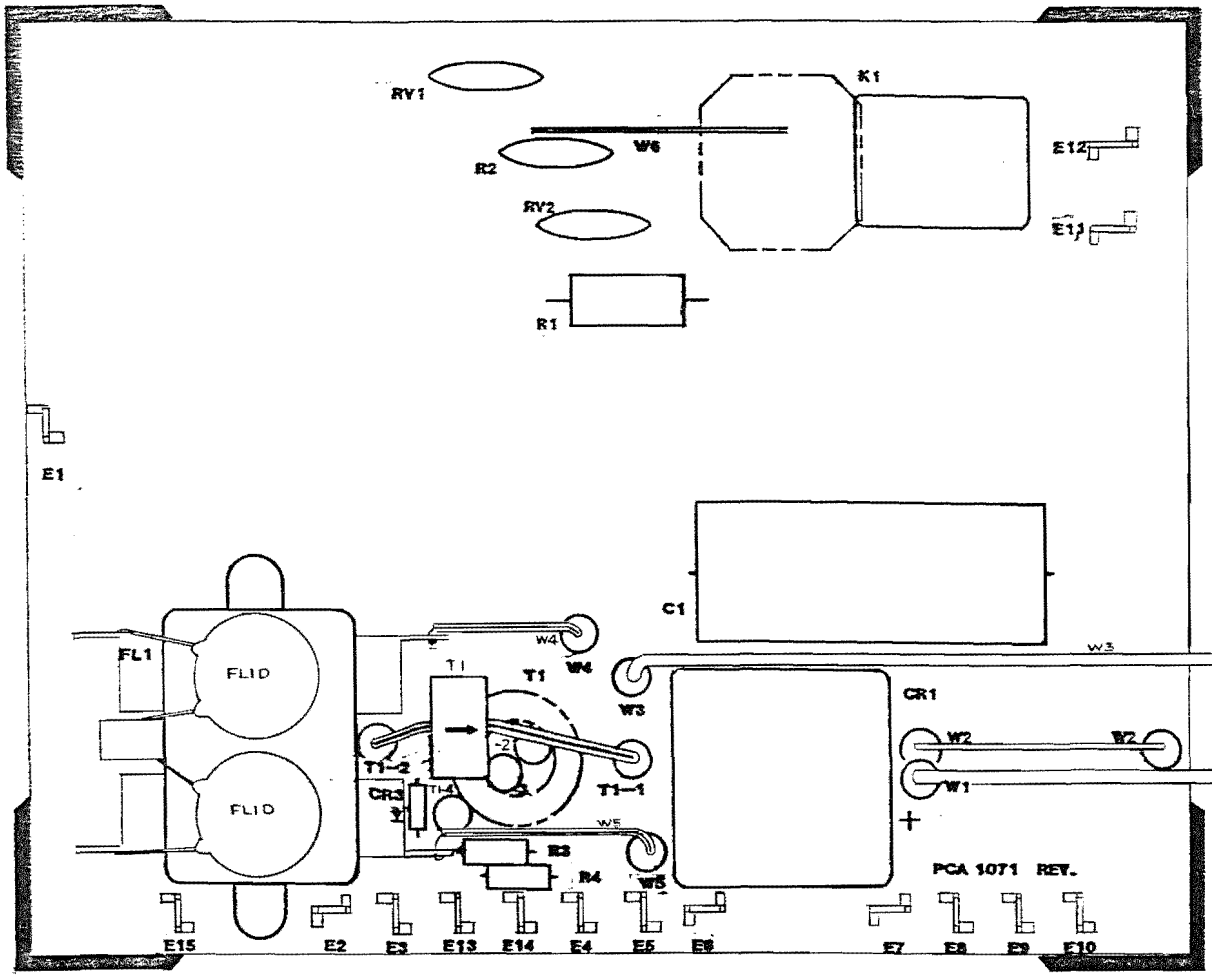
REVISIONS			
DESCRIPTION	CHK	DATE	LTR
SEE OBSOLETE			A/E-2
REDRAWN	Dws	3-29-89	E-3
ECN 2310; 2RX WAS ON A3	jm	12-21-89	F

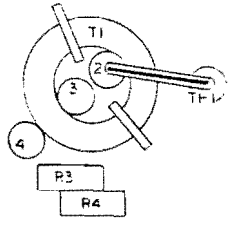
GLASSMAN HIGH VOLTAGE, INC.

TOLERANCES: DEC XXX ± / XX ±; FRAC ±

SCHEMATIC
HIGH VOLTAGE ASSY
WG SERIES (AHV WG)

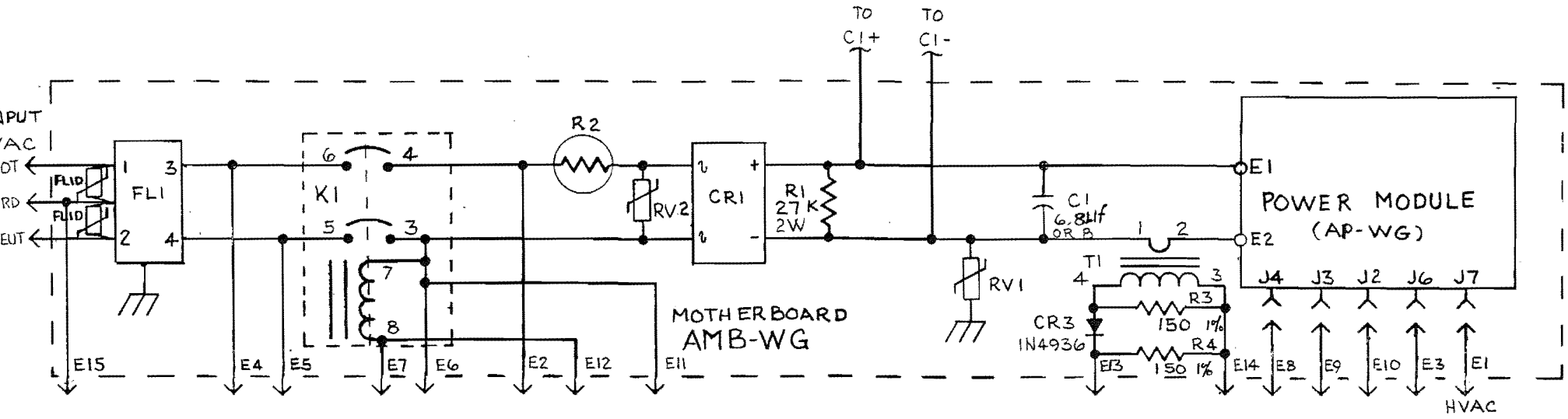
Drawn	Date	DRAWING NO.	REV.
MSC	9-15-83	200021-005	F
Check	Date		
		SCALE NA	Sheet 1 of 1





ALTERNATE T1
(TWX846T250-06)

REVISIONS				GLASSMAN HIGH VOLTAGE, INC.	
DESCRIPTION	ECN	DATE	LTR	TOLERANCES DEC : FRAC :	PARTS PLACEMENT MOTHERBOARD WG SERIES AMB-WG-02
				Drawn WCS 1-19-87	DRAWING NO PCA1071-002 REV N.R.
				Check	
				ENG 3-16-87	SCALE Sheet 1 of 1



NOTE:

ALL RESISTORS ARE $\frac{1}{4}$W U.O.S.

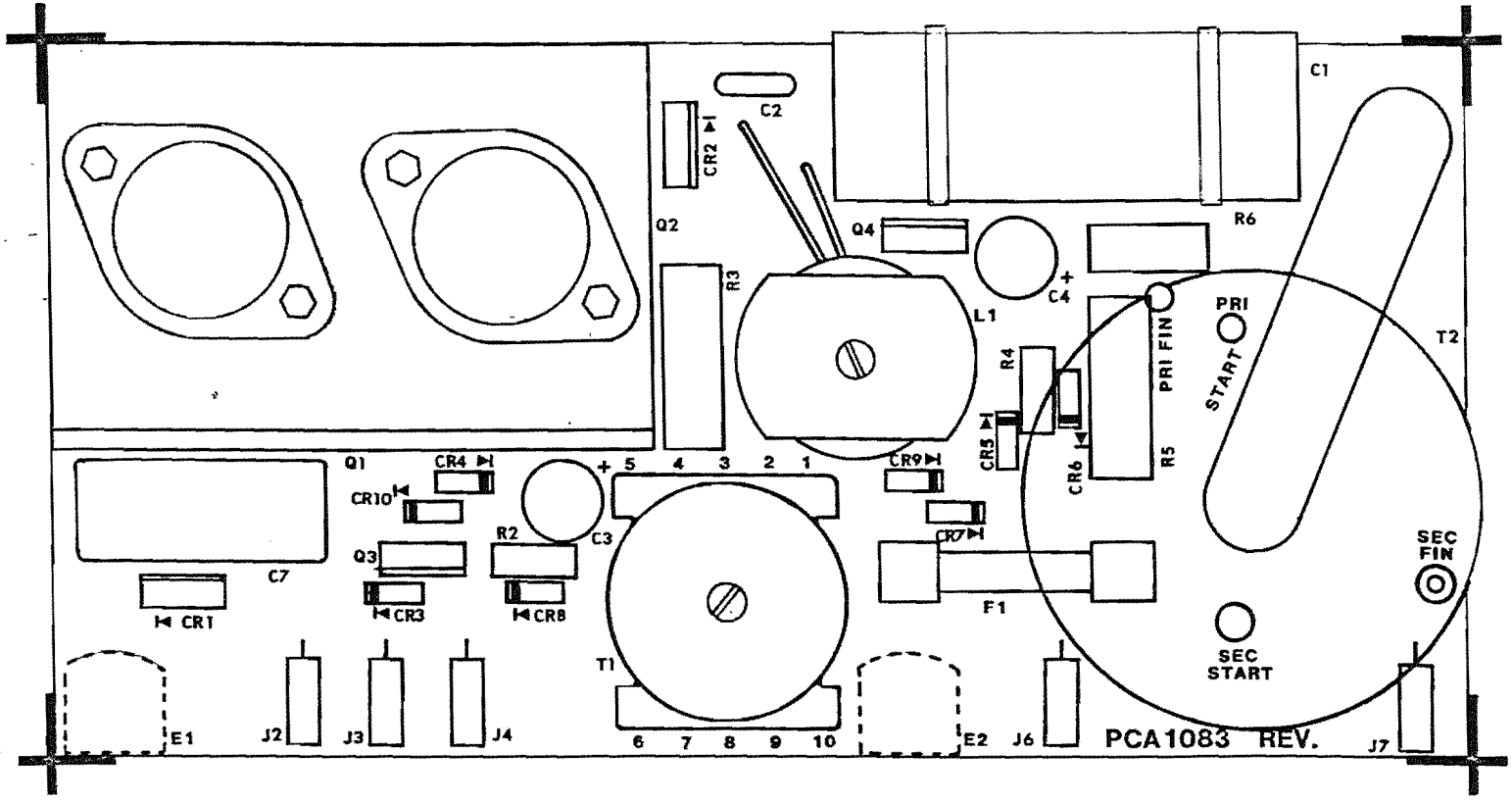
REVISIONS			
DESCRIPTION	CHK	DATE	LTR
C1 TRANSFERED TO AM SCHEMATIC ECN 1A01 C1=8MF REPLACED BY 6.8MF	DWL RK	4-28-87 9-18-87	NR-1 NR-2

GLASSMAN HIGH VOLTAGE, INC.

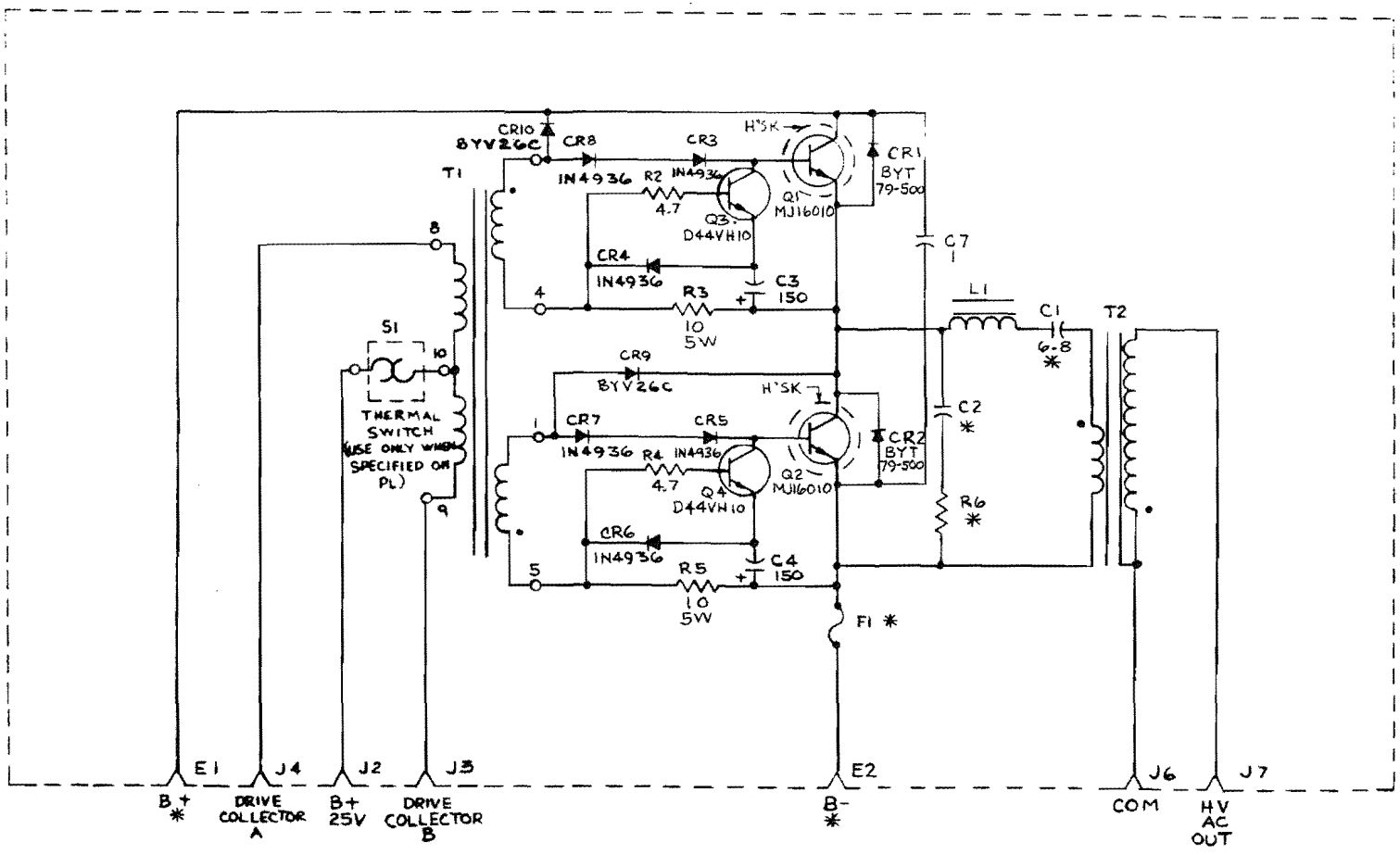
TOLERANCES DEC ± FRAC ±

SCHEMATIC MOTHERBOARD WG SERIES (AMB-WG-02)

Drawn	Date	DRAWING NO.	REV.
MES	11-24-86	200043-001	NR-2
Check	Date		
J.M.	12-2-86	SCALE NTS	Sheet 1 of 1



REVISIONS				GLASSMAN HIGH VOLTAGE, INC.			
DESCRIPTION	CHK	DATE	LTR	TOLERANCES DEC ± FRAC ±	PARTS PLACEMENT POWER MODULE AP-PG-04, AP-WG-02		
ECN 2094; CI TIE WRAPS	PL	6-2-89	A	Drawn: MES Date: 6-1-87	DRAWING NO. PCA1083-002	REV. A	
				Check: DWS Date: 6-2-89	SCALE: 3/4	Sheet 1 of 1	



*

INPUT	F1	REF VOLTAGE B+	REF VOLTAGE B-	R6	C1 ALT.	C2
115V	8A	160V	–	470 ½W	8 µf	.001µF
220V	5A	320V	–	1000 1W	5 µf	220 PF
100V	8A	140V	–	470 ½W	8 µf	.001µF

REVISIONS			
DESCRIPTION	CHK	DATE	LTR
ECN 1443	MW	9-11-86	NR
ECN 1477	DWS	10-17-86	A
ECN 1401		9-15-87	A-1
ECN 1660, C2 WAS .001	DWS	4-21-88	B
ECN 1718, CR9 & CR10	DWS	6-22-88	C

GLASSMAN HIGH VOLTAGE, INC.

SCHEMATIC
POWER MODULE
AP-PG-04
AP-WG-02

TOLERANCES	
DEC ±	
FRAC ±	
Drawn	Date
MES	9-11-86
Check	Date

DRAWING NO. 300030-010 REV. C

SCALE | Sheet 1 of 1