Linear FET combines advantages of planar and trench MOSFETs

About this document

Scope and purpose

OptiMOS™ Linear FET offers the advantages of both the wide SOA of planar MOSFETs and the industry's lowest $R_{DS(on)}$ of modern trench MOSFETs. It provides the perfect solution for hot-swap e-fuse, and battery protection applications, where low conduction loss is a must and high start-up currents have to be handled without degradation or destruction of the device.

In this application note the technical principle of OptiMOS™ Linear FET is explained in details and the key differences from the standard trench MOSFETs are discussed.

Intended audience

Power supply designers

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1 Introduction

From generation to generation, power MOSFETs have been optimized to reduce conduction and switching losses. As a result, the traditional planar MOSFETs evolved into the modern trench MOSFETs. Trench technology enables a significantly smaller $R_{DS(on)}$ in the same chip area and significantly reduces the overall conduction losses. Trench MOSFETs also have substantially steeper transfer characteristics, which enables faster switching - a small change in the gate-source voltage results in a much higher drain-source current.

However, modern trench MOSFETs have limitations that are undesirable for some applications. One important characteristic is the narrowing of the safe operating area (SOA), which exhibits clear limitations in the millisecond range. For example, hot swap application in particular requires MOSFET to slowly turn on in the 1 ~ 10 millisecond range with currents as high as the MOSFET can withstand, i.e. wide SOA capable. It also requires low $R_{DS(on)}$ for the normally-on operating condition. Infineon's new OptiMOS™ Linear FET combines the low $R_{DS(on)}$ of a modern trench MOSFET with the broad safe operating area (SOA) of a planar MOSFET.

2 Clarification between “linear mode” and “linear region”

The diagram below describes the output characteristics of a power MOSFET.

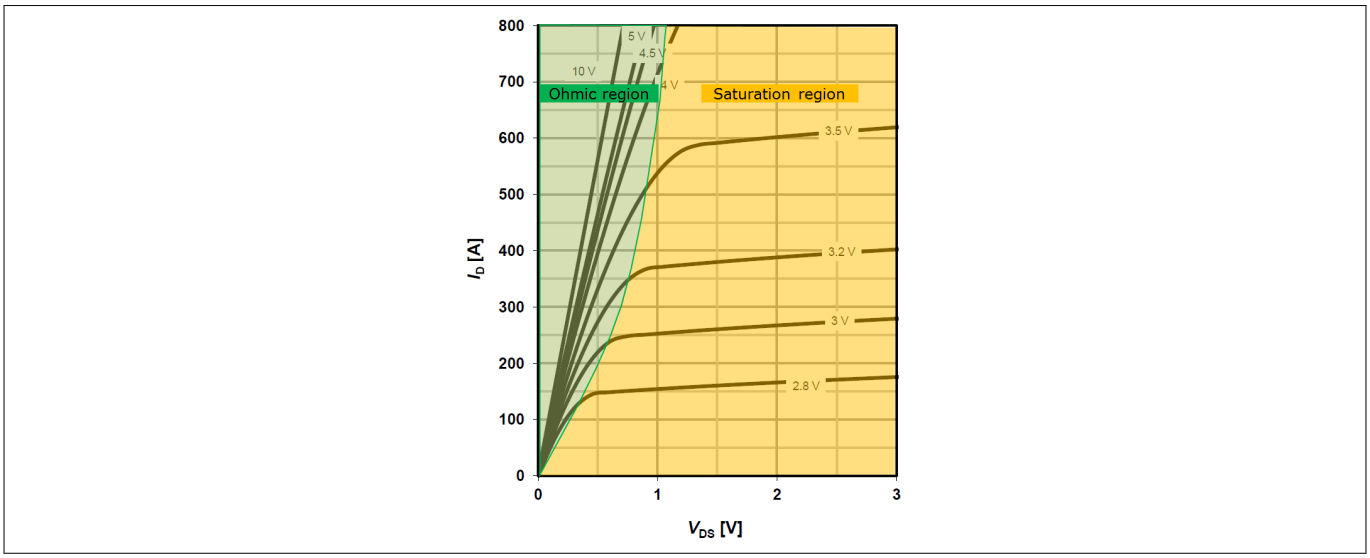

Figure 1 Ohmic and saturation region, diagram “Typ. output characteristics”, BSC010N04LSI

The ohmic region (green, left) is often also referred to as linear region because the characteristic curves in this area have a roughly linear relationship between I_D and V_{DS} similar to a resistor. Both terms are used synonymously in the literature. In this region, a MOSFET behaves like a resistor. As the drain-source voltage increases, the current also increases in a linear manner.

As V_{DS} continues to increase, the current starts to saturate and the device enters the so-called "saturation region” (yellow, right). In this region, the current is controlled by the applied gate-source voltage and has little dependency on the drain-source voltage. The transfer characteristics in the datasheet ***Figure 2*** illustrates the linear relationship between V_{GS} and I_D.

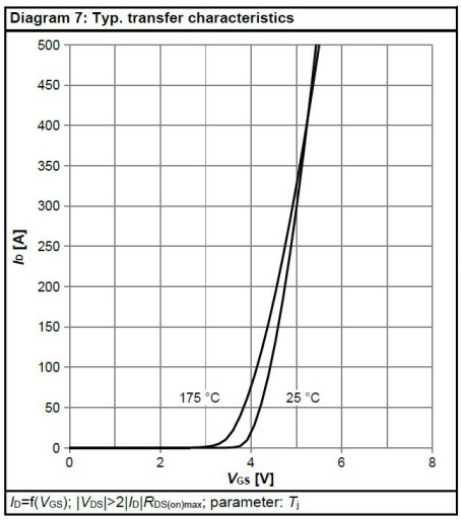

Figure 2 “Typ. transfer characteristic” of a trench MOSFET, IPB017N10N5

In addition, one can also see this as an analogy, where the MOSFET works similar to a linear regulator. Increasing the drain-source voltage only results in an insignificant increase of the current.

In most applications, the MOSFET runs through the saturation region in a very short time (a few tenths to several hundred nanoseconds) during turn-on and turn-off of each switching event, and spends most of the time in the ohmic region.

3 Safe operating area (SOA) planar versus trench MOSFET

Figure 3 shows the safe operating area (SOA) diagrams on an older planar and a modern trench MOSFET.

Optimized for fast switching and a much lower $R_{DS(on)}$, the trench MOSFET shows a much weaker behavior for longer power pulses, typical for hot-swap and battery management applications.

In ***Figure 3*** typical operating points (54 V, 10 ms) are marked in both diagrams showing the current of the devices and handle during this power pulse. The planar MOSFETs (left diagram) is 4.2 A. The trench MOSFET withstands only 0.5 A.

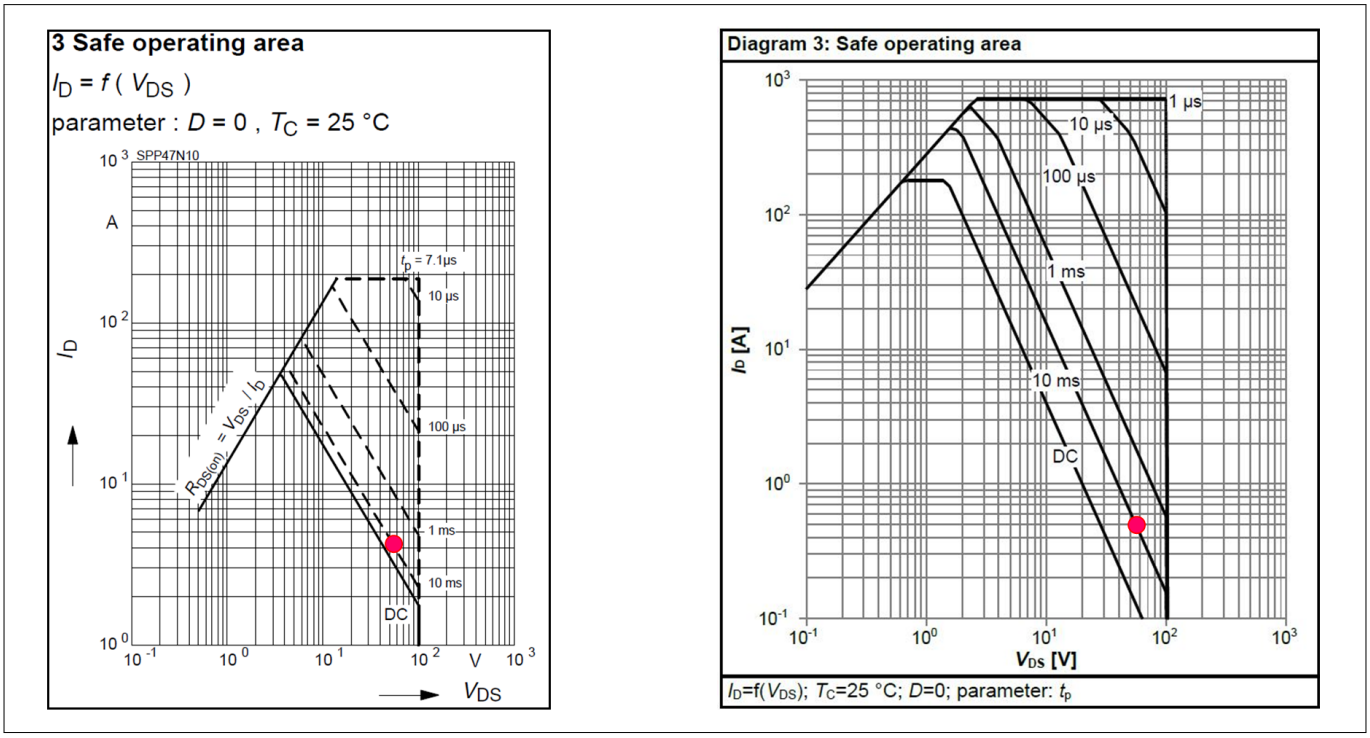

Figure 3 SOA diagrams of a planar (left) and a modern trench MOSFET (right)

4 Application description

In most applications, it is ideal to operate the MOSFET either in the off-state or in the on-state only in the ohmic region. Passing through the saturation region is undesirable during the turn-on and turn off, but cannot be avoided. In a few special cases, however, one wants to utilize specifically the current-limiting behavior in the saturation region. A classic use case can be found in telecom systems. ***Figure 4*** demonstrates the system block diagram.

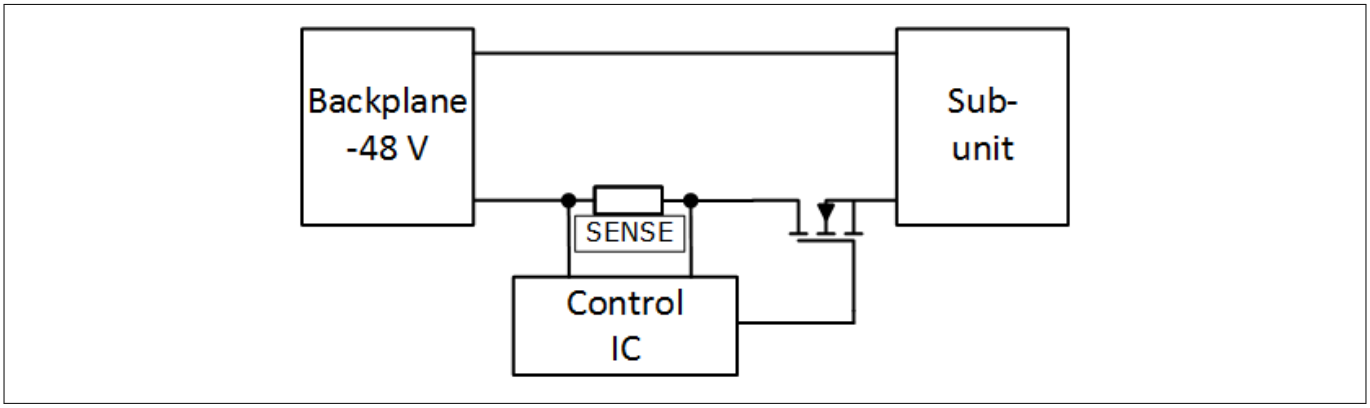

Figure 4 Block diagram “Hot-Swap”

If a sub-unit must be replaced, the central power supply (e.g. 48 V) must not be turned off.

The input stage of the new sub-unit contains several initially uncharged (electrolytic) capacitors. Without any control, during first contact, these capacitors would experience a high surge current similar to a short circuit event. The current is only limited by the PCB parasitic components, such as resistances and inductances, and can easily reach several hundred amperes. Although the energy is mainly drawn out from the capacitor bank, the central power supply might collapse below a permissible level during this in-rush phase. To prevent this, the in-rush current to the sub-unit must be limited to an acceptable level. An effective current limitation with an instant hot swap function can be achieved by interposing a power MOSFET, which operates in the saturation region during this few-millisecond event. The MOSFET is controlled by increasing the gate-source voltage slowly (normally with the help of a specific hot swap controller IC) so that the drain-source current (the capacitor charging current) is capped by a configured constant current limit.

Due to heterogeneous current distribution common in a power MOSFET with large area, some parts of the chip may become overloaded, resulting in a hot spot. This reduces lifespan of the component or could potentially cause destruction of the system.

One way to tackle this problem is to use two devices in parallel where one device is selected according to the required SOA behavior for the in-rush phase and the other with newest generation low-resistance MOSFETs, such as OptiMOS™ 5 series, for the continuous conduction phase. This approach combines the benefit of both worlds; however, the bill of material is increased due to the use of two device types instead of one, and additional control circuit is needed to switch between the two.

The ideal device for this application would be one that behaves like a planar MOSFET with a broad safe operating area allowing high current during the in-rush phase and has low $R_{DS(on)}$ like a modern trench MOSFET during the continuous normal operation without additional control efforts. Infineon’s OptiMOS™ Linear FET is optimized exactly for this type of application, resulting in wide SOA similar to that of a planar MOSFET and low $R_{DS(on)}$ of state-of-the-art trench MOSFET.

5 OptiMOS™ Linear FET versus standard OptiMOS™ power MOSFET

This section compares side by side some of the key datasheet characteristics of an OptiMOS™ Linear FET and a standard OptiMOS™ power MOSFET.

OptiMOS™ Linear FET IPB017N10N5LF (shown on the right) and the OptiMOS™ 5 IPB017N10N5 (shown on the left) are used as examples. Both D²PAK 7pin devices come with the capability to block 100 V and industry's lowest 1.7 mΩ on-state resistance $R_{DS(on)}$.

5.1 Safe operating area (SOA)

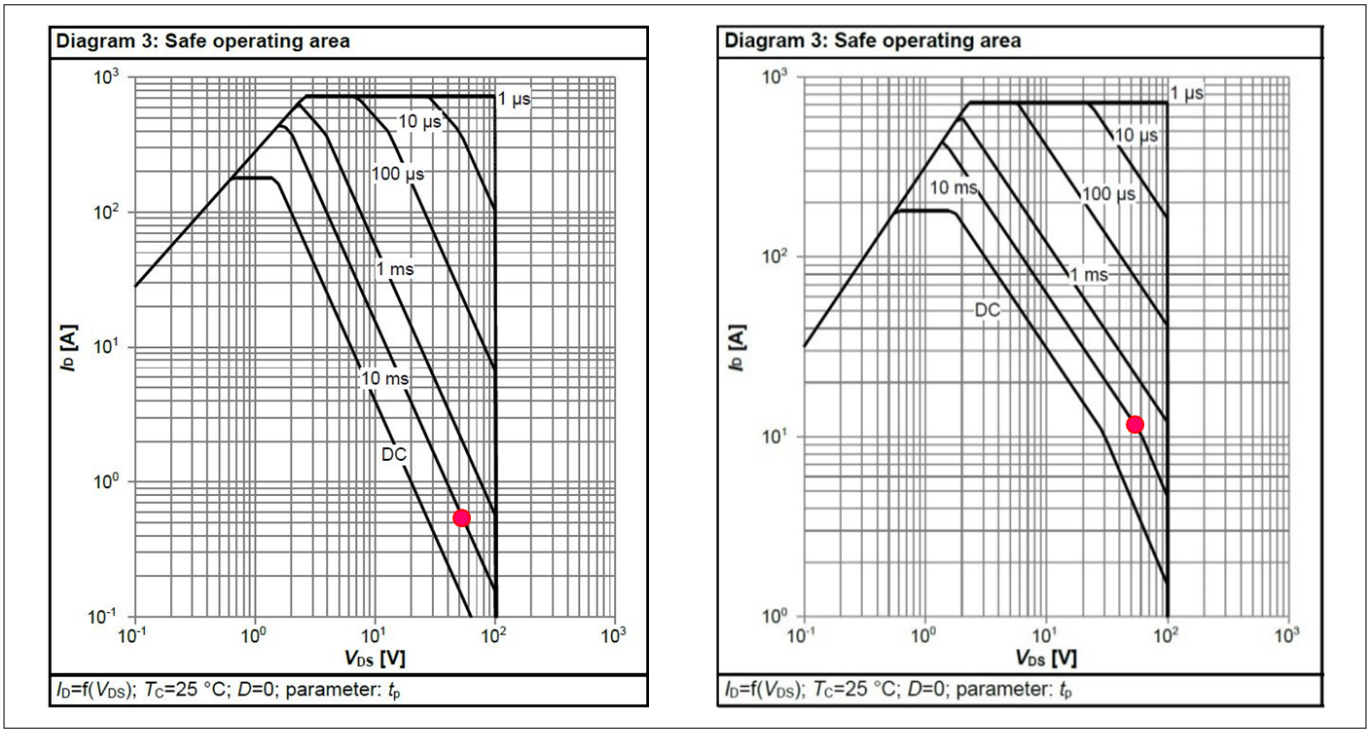

Figure 5 Safe operating area IPB017N10N5 (left) and IPB017N10N5LF (right)

Despite the same $R_{DS(on)}$, the SOA diagrams show significant differences between the two devices. A typical operating condition for telecom hot swap conditions with input voltage of 54 V and in-rush period of 10 ms can be used as an example. Based on the datasheet SOA, the standard OptiMOS™ IPB017N10N5 can allow only 0.5 A of 10 ms current, whereas OptiMOS™ Linear FET IPB017N10N5LF can withstand up to 11.5 A which is more than 20 times higher than the standard MOSFET.

Therefore, with Linear FET, it is possible to charge a much larger capacitor bank in the same amount of time without damaging or destroying the MOSFET. Alternatively, the same capacitor bank can be charged at higher currents in a shorter duration.

OptiMOS™ Linear FET versus standard OptiMOS™ power MOSFET

5.2 Typ. transfer characteristics

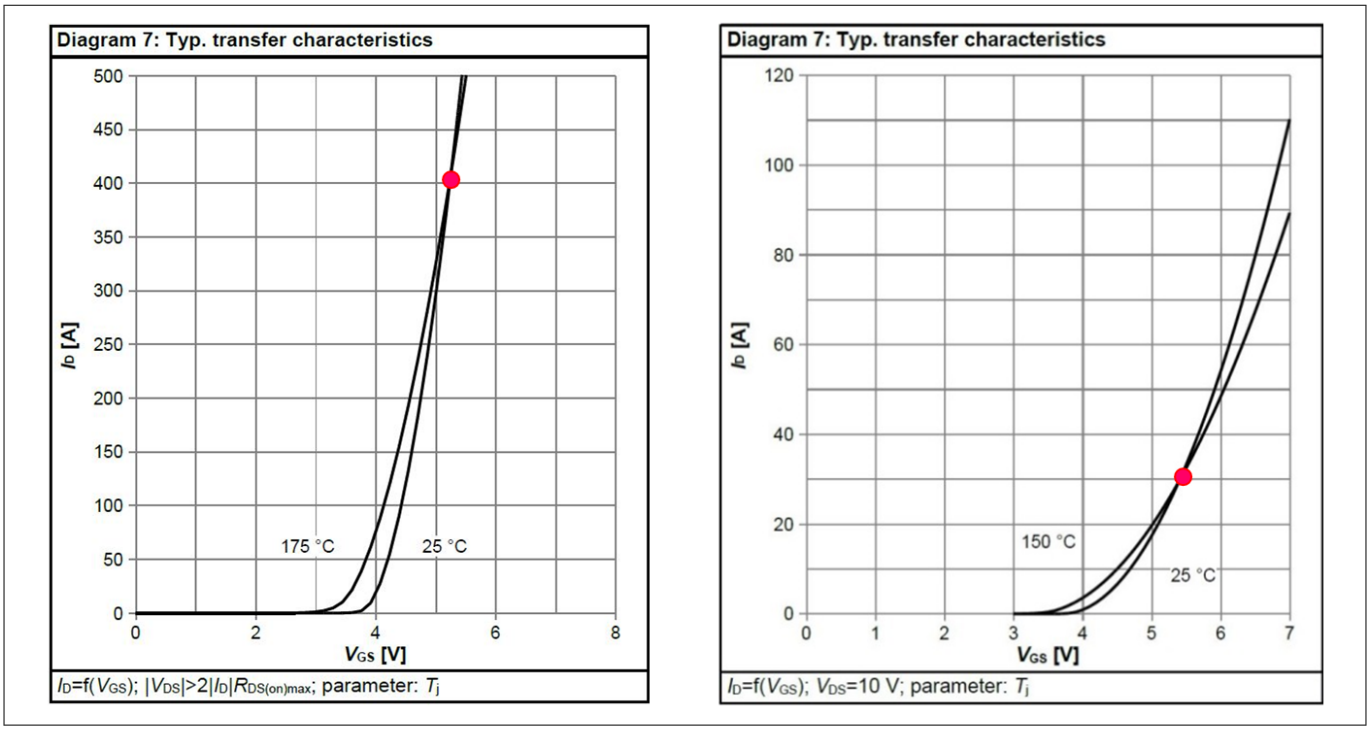

Figure 6 ”Typ. transfer characteristis” IPB017N10N5 (left) and IPB017N10N5LF (right)

In comparison with the standard OptiMOS™ MOSFET (***Figure 6*** left-side), the characteristic transfer curve of the OptiMOS™ Linear FET IPB017N10N5 (***Figure 6*** right-side) is less steep. The gate-source voltage, therefore, must be significantly increased to get the same current when compared with the standard MOSFET. This behavior is similar to that of a planar MOSFET.

It is very important to understand the intersection between the two transfer curves at different temperatures (respectively at 25°C and 150°/175°C). This intersection marks an important threshold and is called the zero temperature coefficient (ZTC) point. Operating below this point is unwanted due to the positive feedback coupling with positive temperature coefficient (PTC). It means with the same operating gate-source voltage and drain-source voltage, the hotter areas of the chip tend to conduct higher current than the colder areas. Due to higher power dissipation (P_{loss}=i(t)*v(t)), the hotter areas get hotter and hotter, potentially leading to destruction due to thermal run away. Above the ZTC point, the MOSFET stabilizes itself as warmer areas naturally get current reduced due to negative temperature coefficient (NTC).

It can be seen as a clear advantage when the ZTC point happens at a current as low as possible. For OptiMOS™ Linear FET, the intersection is at around 30 A, which is much lower than the ~400 A of the standard OptiMOS™. OptiMOS™ Linear FET has much less chances to operate in the conditions which could run into thermal runaway. This is exactly the reason why the permitted SOA of the OptiMOS™ Linear FET is much larger and wider than that of the standard OptiMOS™.

OptiMOS™ Linear FET versus standard OptiMOS™ power MOSFET

5.3 Typ. gate charge

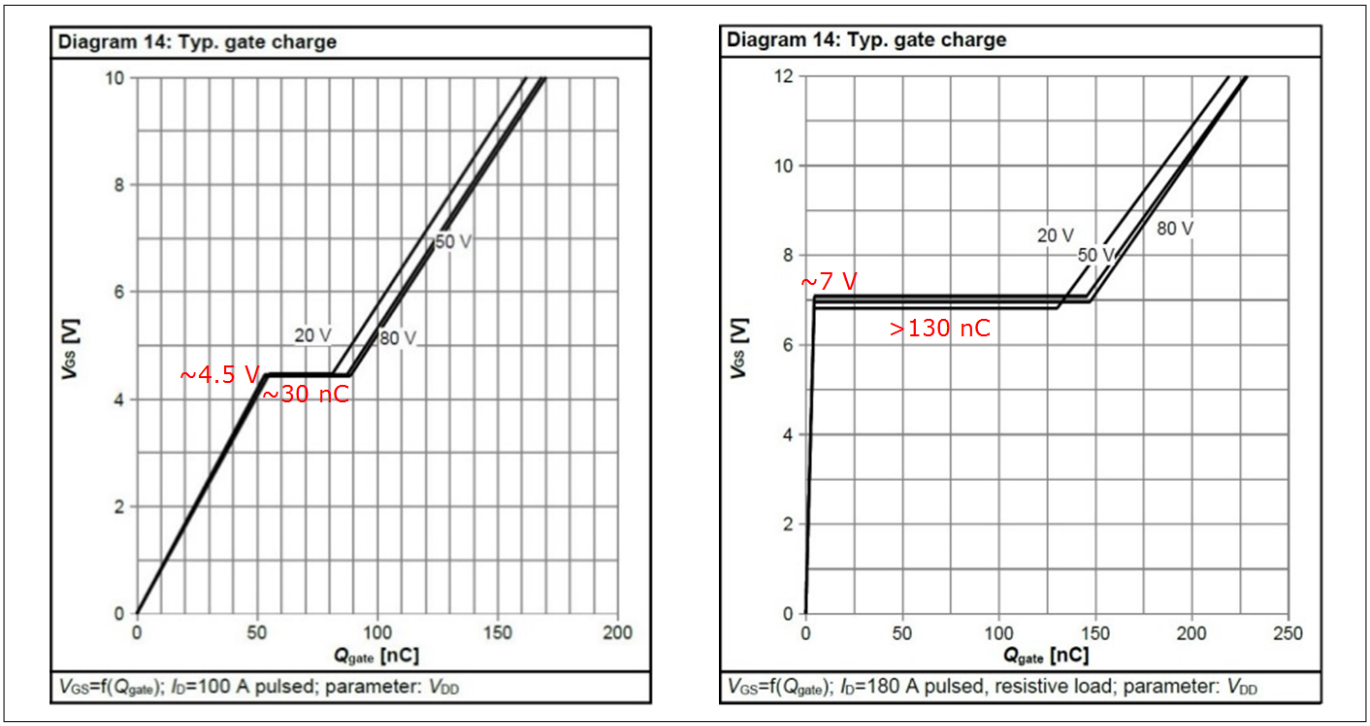

Figure 7 ”Typ. gate charge” IPB017N10N5 (left) and IPB017N10N5LF (right)

Another key characteristic to explain the differences between OptiMOS™ Linear FET and the standard one is to look at the gate-charge behavior (***Figure 7***).

While the standard MOSFET optimizes for lowest total Q_g and Q_{gd}, Linear FET on the other hand has much larger turn-on gate charge. The Miller plateau can be reached with a much lower charge (approx. 10 nC vs. approx. 55 nC), and enters linear mode more effortlessly. It then stays in plateau longer due to higher charge needed to completely charge the MOSFET (more than 130 nC vs. approx. 30 nC). This is the desired behavior for hot-swap applications, because in-rush current can be sufficiently limited.

Another significant difference can be seen in the position of the Miller plateau.

Here, the plateau of Linear FET is typically at V_{GS}~7 V (at 180 A) compared to the ~4.5 V (at 100 A) plateau of the standard FET.

5.4 Typ. output characteristics

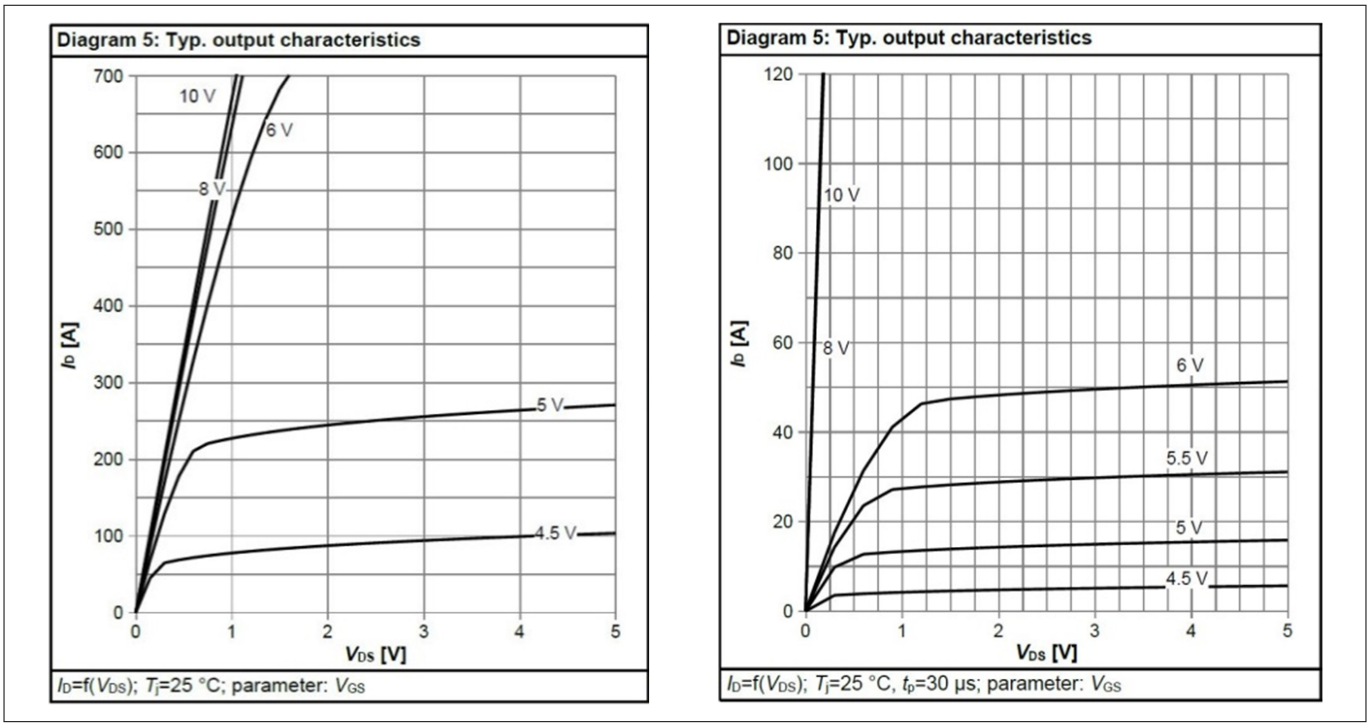

Figure 8 ”Typ. output characteristics” IPB017N10N5 (left) and IPB017N10N5LF (right)

The output characteristic comparison between OptiMOS™ Linear FET and standard device is shown in ***Figure 8***. For Linear FET, the gate-source voltage must be significantly higher than 6 V so that the MOSFET switches on completely when the currents are higher than around 50 A. With the aforementioned ~7 V plateau voltage, an operation with at least 8 V gate drive is needed; 10 V gate driving voltage is highly recommended.

5.5 Typ. drain-source on-resistance

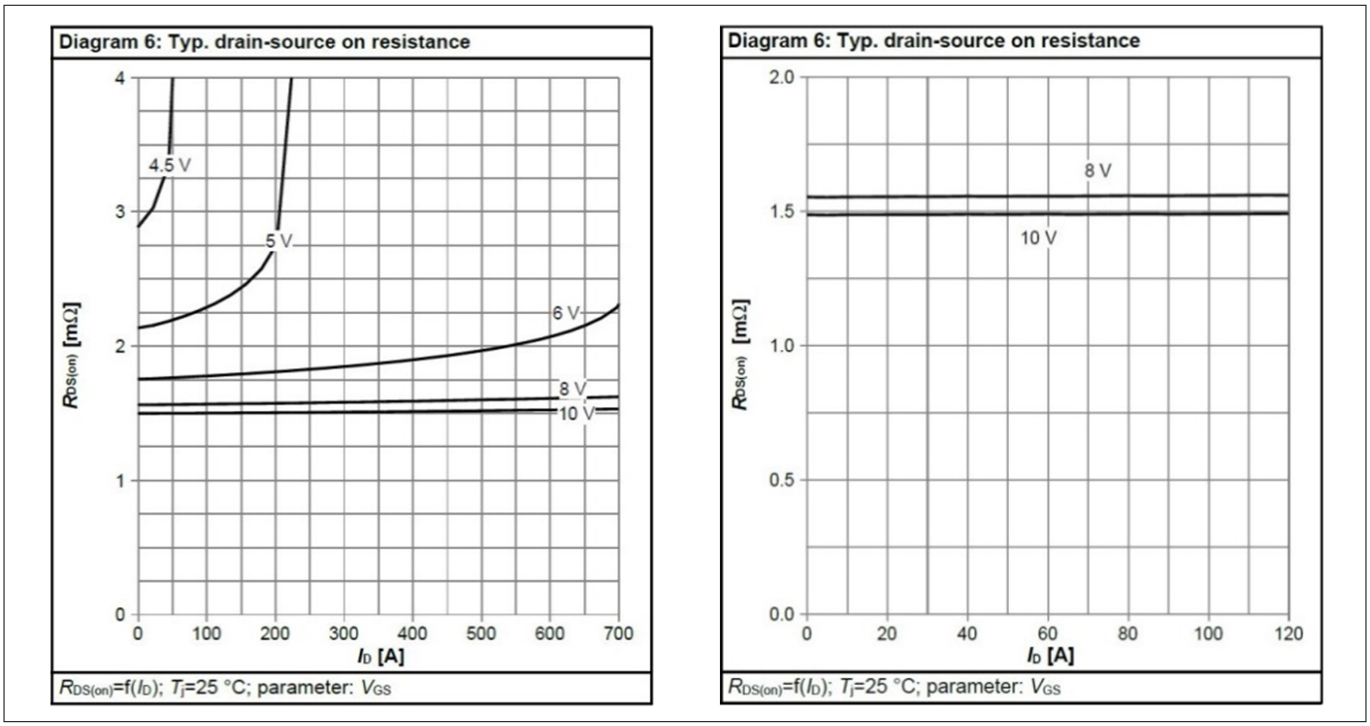

Figure 9 ”Typ. drain-source-on-resistance” IPB017N10N5 (left) and IPB017N10N5LF (right)

In contrast to IPB017N10N5, OptiMOS™ Linear FET leaves the saturation region only at levels significantly above 6 V, which is why $R_{DS(on)}$ is only specified at 8 V and above. ***Figure 9*** also shows that an increase in the gate-source voltage from 8 V to 10 V again results in a considerable reduction of $R_{DS(on)}$, resulting in lower conduction losses (another reason to use higher driving voltages).

6 Summary

The OptiMOS™ Linear FET is the ideal solution for hot-swap, e-fuse, and battery protection applications. It combines the advantages of a wide safe operating area (SOA) such as a planar MOSFFET and low $R_{DS(on)}$ of a modern trench MOSFET. It increases system robustness and at the same time enables best efficiency.

Revision history

Document version	Date of release	Description of changes

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