Evaluating the Reliability of Power MOSFETs

By **Carl Blake**, **Tim McDonald**, **Dan Kinzer**, **Joe Cao**, **Alex Kwan** and **Aram Arzumanyan**, International Rectifier, El Segundo, Calif.

Device junction temperature and other operating conditions are critical in determining the avalanche current capability and forward bias safe operating area for MOSFETs designed in different processes.

Power device performance continues to advance at a high rate. Each generation is also becoming more optimized and more specialized to particular application conditions. At the same time, a high value continues to be placed on devices that are extremely rugged, capable of withstanding current, voltage and temperature conditions well in excess of their nominal continuous ratings. With the continuous drive for higher power density and lower cost, newer technologies achieve much higher channel densities than ever before, while keeping gate capacitance in check with innovative structures that minimize all nonessential gate overlaps with source and drain.

Trench technologies are becoming commonplace and dominant in applications where a high premium is placed on dc or on pulsed-current density, while planar technologies still find application where low thermal resistance and maximum forward bias safe operating area (FBSOA) is a dominant concern. To meet the system design goals in power switch applications, designers should understand ruggedness tradeoffs of each MOSFET device type as they apply to the target application.

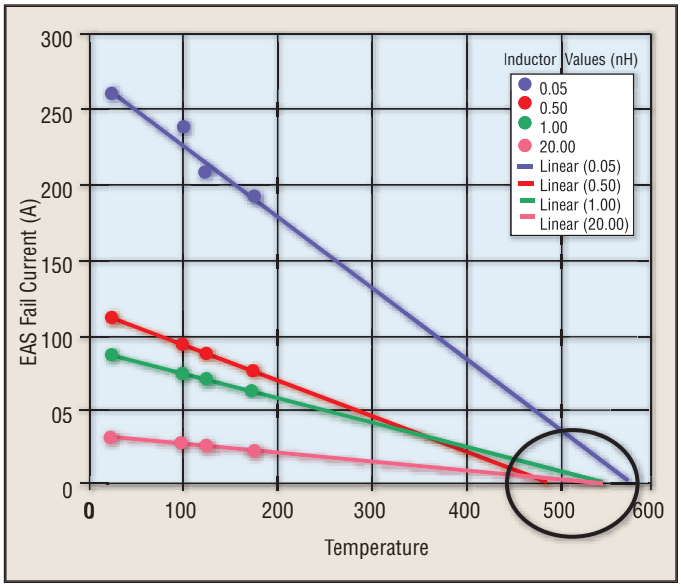


Fig. 1. *The characteristic curves for a robust 40-V trench MOSFET show average avalanche failure energy versus starting junction temperature for various inductor sizes.*

Avalanche Ruggedness in Trench Power MOSFETs

One important feature of the new devices optimizes the design by forcing the avalanche breakdown site to occur directly under the source metal contact. At this location the hole current does not create a bias voltage to the source, thus improving EAS capability.

For many applications, the ability of a device to drive unclamped inductive loads is a critical success criterion. A

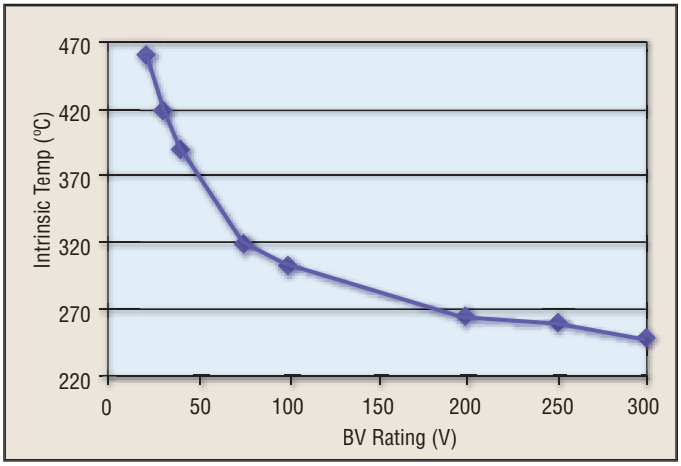


Fig. 2. *The intrinsic temperature of a power device is calculated at various breakdown voltages, assuming a background concentration close to that of a plane junction.*

well-designed and fabrication defect-free MOSFET will share current uniformly across the active area during avalanche, due to the positive temperature coefficient of breakdown voltage. When the device fails, it will not do so because of bipolar device mechanism activation. It will fail because the temperature and current have reached a point at which the thermally generated carrier concentration is too high for the device to support the applied voltage.

Such a device will have a characteristic family of curves as shown in **Fig. 1**, where an extrapolation of lines fit to the average failure points at various starting temperatures will intersect the x-axis at or above the intrinsic temperature of the device. The intrinsic temperature is above 500°C and will be true for a large range of values of inductor. The data in **Fig. 1** was obtained from a rugged 40-V trench MOSFET design. **Fig. 2** shows a calculation of the intrinsic temperature, i.e. the temperature where the intrinsic carrier concentration is equal to the background doping, according to the formula:

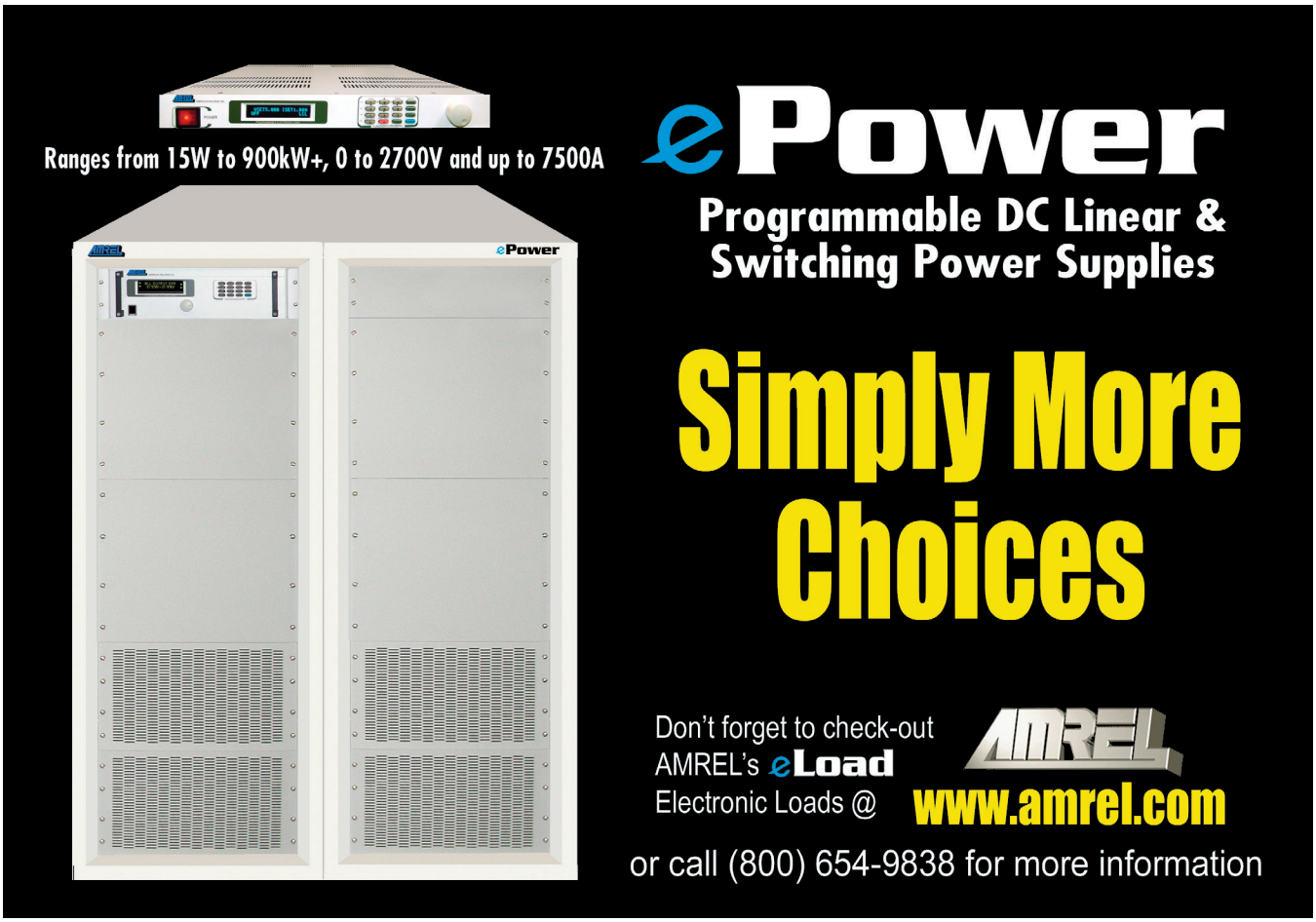
$Ni = 3.88e16T^{1.5}\exp(-7000/T)$, where T is temperature in degrees Kelvin.

Ensuring the ruggedness of a MOSFET design requires a very thorough evaluation of the device, and the acquisition of a statistically large sample of failure currents and energies. The population should be free as much as possible from maverick devices that fail at lower energies, and the mavericks that do exist must be removed through 100% testing of the entire product population. Testing for a tight distribution even at elevated temperatures gives confidence that there isn't a significant population of mavericks, and the room temperature screens that are applied should take the device close enough to its failure level to remove them.

Knowing the intrinsic temperature, the inductor value, the actual breakdown voltage at temperature and the transient thermal impedance, one can calculate the expected current that will result in the device "going intrinsic." For a 100-V device, the calculation yields IAS = 149 A at 25°C and IAS = 110 A at 150°C, for active area (AA) = 10.4 mm^2 with L = 100 µH. The actual performance of several technologies is shown in **Fig. 3**.

The comparison of technologies gives some insight into the way different devices perform. The highest performance technology for handling unclamped avalanche is the advanced planar design. It has unclamped avalanche failure points that exceed 80% of the ideal calculated value, and the standard deviation at both 25°C and 125°C is in the range of 1% to 2% with no mavericks or non-normal distribution.

The conventional planar technology fails at 25% lower current, with a standard deviation of 2% to 3%, and again no evidence of mavericks. The advanced trench devices perform similarly to the conventional planar, with one or two maverick parts in evidence. The conventional trench,



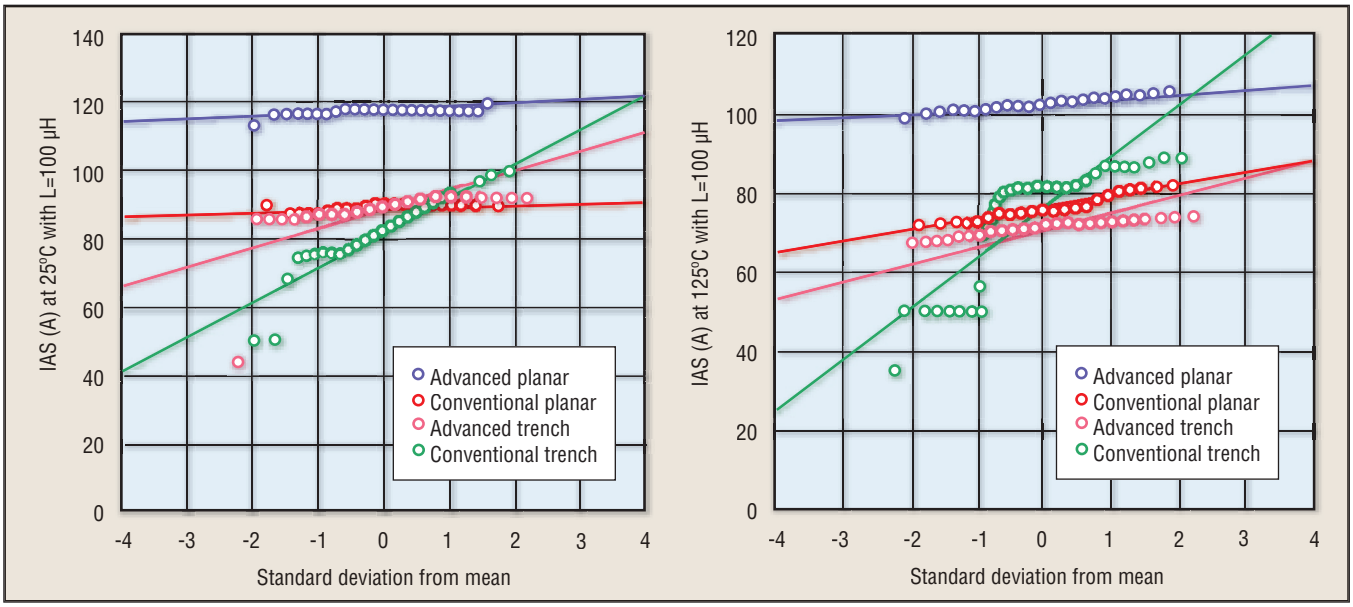


Fig. 3. *A comparison of the statistics of samples (individual lot distributions) of various generations of planar and trench MOSFET technology at junction temperatures of 25°C (left) and 125°C (right). The value at 0 gives the mean avalanche failure current, while the slope gives the standard deviation.*

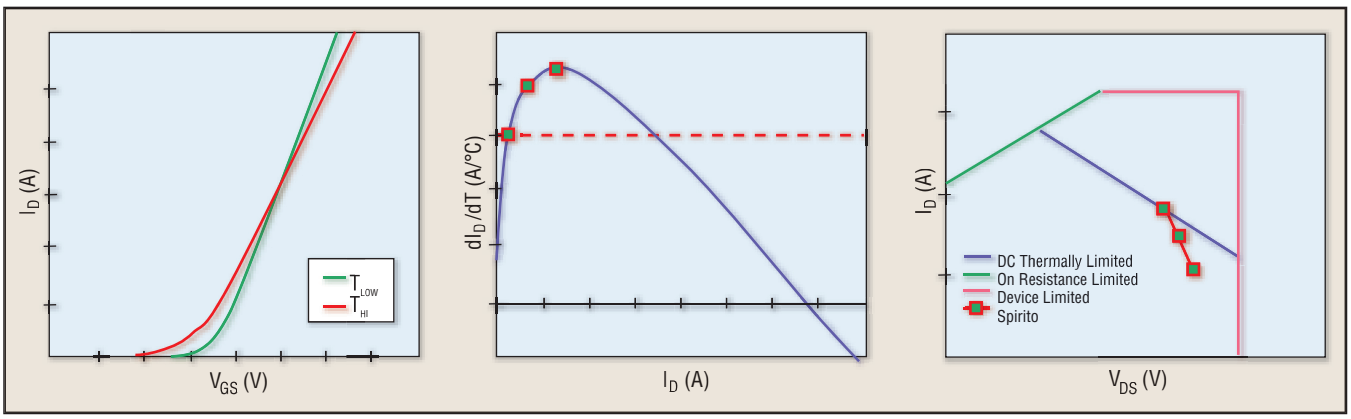


Fig. 4. *Shown here are a MOSFET I_D versus V_{GS} transfer curve (left), the associated dI_D/dT curve showing drain current temperature dependence (middle), and the resulting derating curve (safe operating area) (right).*

while it has a similar mean failure level, has a much larger variation, and evidence of a bimodal distribution at elevated temperature.

Forward Bias Safe Operating Area

A number of applications require power MOSFETs to operate under the simultaneous application of high voltage and current. Linear power supplies and amplifiers are still in use for low dropout and highly noise-sensitive applications. Automotive linear fan control is another such application. Some switching applications have surge requirements that will pull the device into a "linear" mode where the gate voltage is controlling the current with high voltage applied (for example, hot swap in a Netcom converter).

A typical MOSFET transfer curve has a crossover current below which the temperature coefficient of I_D is positive, as shown in **Fig. 4**. The dI_D/dV_{GS} curve has a peak at low currents and gradually falls. This characteristic leads to thermal instability at higher voltage according to the equation:

$$\frac{dI_D}{dT} > \frac{1}{(V_{DS} \times Z\theta(t))}$$

as described in Spirito and other references[1-4]. The constant power current derating curve that is often used for short pulses becomes invalid for longer pulses, and the maximum allowable current falls off as shown. High-density MOSFET designs have higher transconductance, the crossover current is much higher, and the peak dI_D/dT is higher. **Fig. 5** shows a comparison of the transfer characteristics of three technologies.

In **Fig. 6**, MOSFET devices are swept up in voltage at constant power, and the maximum T_J was measured with a thermal imaging camera. The lower transconductance device is able to be swept up to nearly the rated voltage with

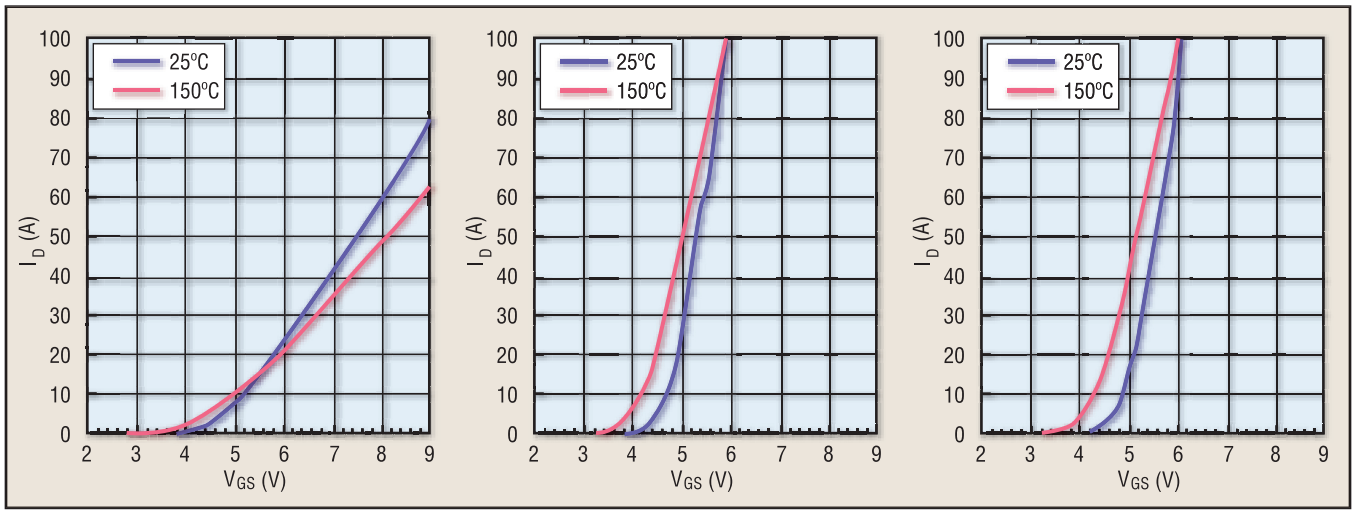


Fig. 5. *A comparison of transfer curves of early planar (left), recent planar (middle) and recent trench (right) MOSFET technology illustrates the higher transconductance associated with the higher density MOSFET designs.*

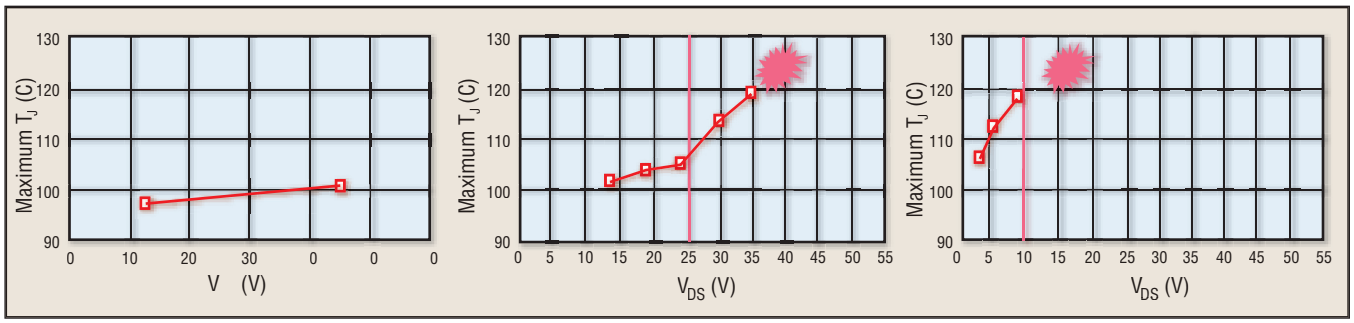


Fig. 6. *In these measurements, the voltage across the MOSFETs was swept while maintaining constant power. The maximum T_J was then measured with a thermal imaging camera, revealing the thermal limits of early planar (left), recent planar (middle) and recent trench technology (right).*

little change in T_J, while the newer technologies develop hot spots and thermal failure shortly after exceeding the thermal instability criterion. This points out the serious limitations of traditional FBSOA curves and is an extremely important factor in choosing the right technology and design for applications that require this type of operation. When a linear load is involved, designers should take care to use power MOSFETs whose ratings comprehend this effect[5]: planar devices fit the bill.

Ensuring Reliability of New Process Technology

High performance and robust power semiconductors must be designed with attention to specific application requirements and with capability to withstand a variety of normal and overload conditions. Power MOSFETs are the transistor of choice in the 20-V to 200-V range, and new generations of devices are available combining high-density process techniques.

New technology platforms must be carefully designed and characterized to make sure they are capable of reliable unclamped inductive load performance and linear operation. **PETech**

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Editor's Note

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