Low Voltage MOSFET's Behavior in FBSOA

Power MOSFETs working in linear mode need to be correctly designed at the Silicon level in order to improve ruggedness to thermal instability phenomena. In particular, modern Silicon technologies, optimized for high current and high switching frequency environments, could be less safe in linear mode than previous planar technologies, optimized for linear mode. **Filadelfo Fusillo, Senior Market and Application Engineer, and Filippo Scrimizzi, Low Power Market and Application Manager, STMicroelectronics, Catania, Italy**

Many systems use Power MOSFETs operating mainly in linear mode (or active region): for example, in a fan controller, the MOSFET works permanently as constant current source, with the fan connected in High Side position. The fan speed can be adjusted by varying the current value and therefore the MOSFET gate-source voltage (V_{GS}). In other applications, the device can work in linear mode for short time intervals, passing from ON state to OFF state condition and vice versa. The slower this transition, the more critical the device power dissipation; so, high power capability is required for MOSFETs working in linear mode. With new MOSFET technologies, huge enhancements in conduction and switching losses have been reached thanks to drastic specific R_{DSon} and Q_g reduction, linked to smaller and smaller device die size. These features enable considerable efficiency gain in high switching frequency applications. On the other hand, they could be very risky when the MOSFET works in linear mode because of the reduced power capability.

Linear mode operation and safe operating area

There are basically two main operation modes for a Power MOSFET working in ON state:

- Ohmic (or triode) region: linear relationship between drain current $\left(I_D = \frac{V_{DS}}{R_{DSon}}\right)$ and drain-source voltage (V_{DS}) ; this is a constant resistance region;
- Saturation (or linear) region: the drain current $\left(I_D = k\left(V_{GS} - V_{TH}\right)^2\right)$ is nearly independent of the drain-source voltage (V_{DS}), while it can be adjusted by varying properly the gate-source voltage (V_{GS}).

MOSFETs working in linear mode can withstand very high power dissipation levels, due to simultaneous high current (I_D) and voltage across it (V_{DS}). When a MOSFET works as a switch, it passes continuously from OFF state (high V_{DS} but zero current) to ON state (ohmic or R_{DSon} region). During these transients, the device stays in linear mode for a short time interval; eventually, if these transitions become slower (i.e. high R_G in the gate driving circuit), the device could dissipate high amount of energy. For a power MOSFET, the SOA curve (or Safe Operating Area) defines the maximum value of drain-source voltage (V_{DS}) and drain current (I_D) for a correct device working. Figure 1 shows an idealized SOA curve for a

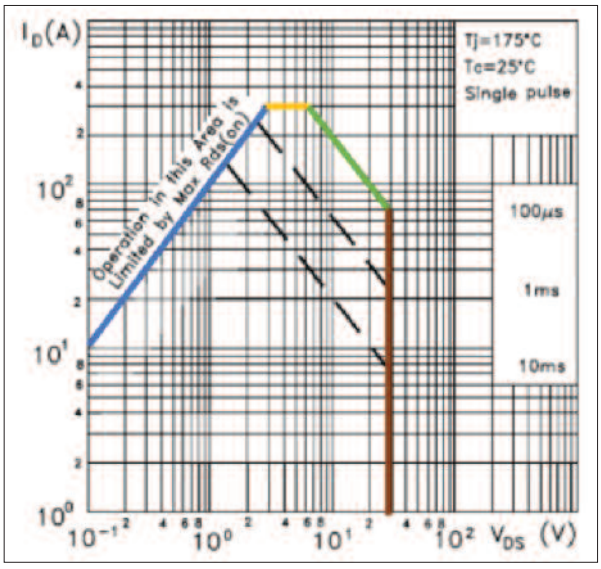


Figure 1: Idealized MOSFET SOA curve

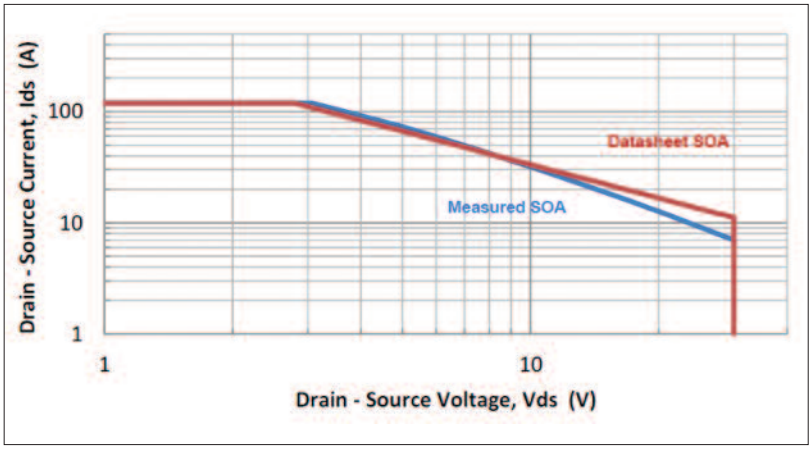


Figure 2: Measured SOA curve

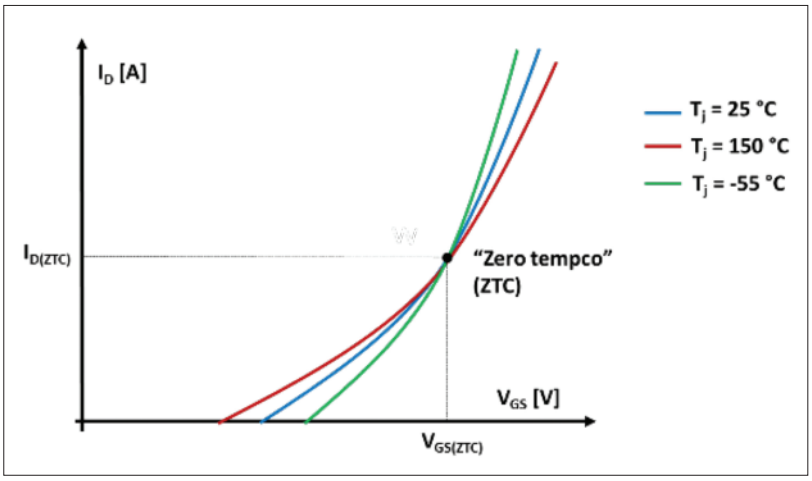


Figure 3: **MOSFET transfer curves and ZTC identification**

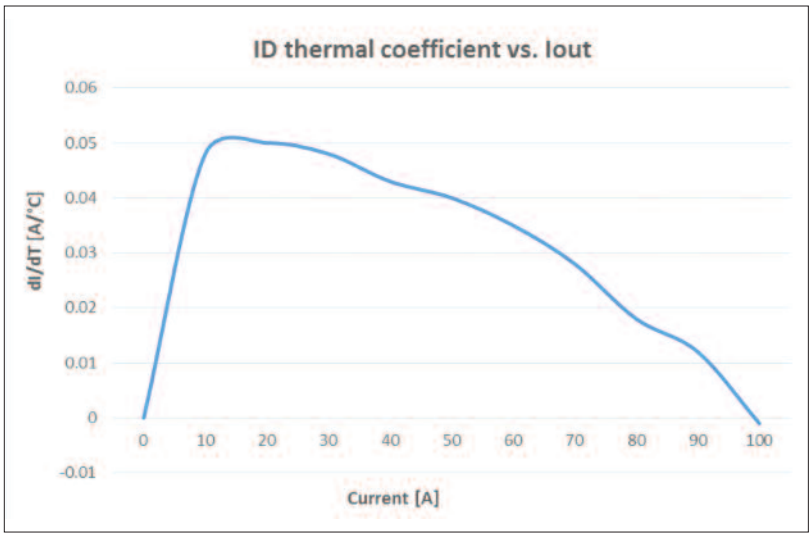


Figure 4: **ID temperature coefficient at T = 25°C**

30 V Power MOSFET, colored lines represent the SOA limits:

- R_{DSon} limit (blue line): for a given V_{DS}, I_D value is limited by the maximum R_{DSon};
- Maximum I_D limit (yellow line): maximum current value that the package can manage;
- Maximum power limit (green line): maximum power level allowed for T_J=T_{Jmax};
- Maximum V_{DS} limit (brown line): SOA limit defined by device breakdown voltage.

Unfortunately, real devices show different behaviors in the "maximum power" zone of the SOA at high drain-source voltage. This is linked to the "thermal instability" phenomenon, which affects Power MOSFETs working in linear mode. In fact, when the electric power generated into the device is higher than the power dissipated, the device is not able to sustain the power pulse any longer. This failure mechanism can happen even inside the idealized or theoretical SOA curve and also at low drain current values [1]. The difference between theoretical and measured SOA, for a 30V device, is explained in Figure 2.

Thermal coefficient of drain current

The transfer characteristic of a Power MOSFET shows the drain current (I_D) as a function of gate-source voltage (V_{GS}) at a fixed junction temperature (T_J); this curve is a common datasheet parameter. Considering the negative temperature coefficient of the threshold voltage $\left(\frac{\Delta V_{GS(th)}}{\Delta T}\right)$, the transfer characteristics at three different junction temperatures (-55°C, 25°C and 150°C) are plotted in Figure 3.

The three curves intersect at a cross-over point called zero temperature coefficient (or "zero tempco", ZTC); in other words, for $V_{GS} = V_{GS(ZTC)}$, the device current remains stable with the temperature. For $V_{GS} > V_{GS(ZTC)}$, when the device temperature rises up, the drain current tends to decrease, reaching thermal stability conditions. And vice versa: for $V_{GS} < V_{GS(ZTC)}$, the drain current thermal coefficient is positive; when a small die zone becomes hotter than adjacent area, it conducts more drain current, creating more heat. This, in turn, allows more current to flow, due to a lower threshold voltage (negative $V_{GS(th)}$ temperature coefficient). Finally, this die area can conduct a huge amount of current, which can push the device to failure (thermal runaway) if appropriate limitations haven't been fixed up. Lower voltage and current values of ZTC reduce the zone with a positive temperature coefficient thus increasing the device thermal stability. Deep analysis on MOSFET technologies and Silicon characteristics highlight that there is a strict link between ZTC and MOSFET transconductance (g_{fs}): the higher gfs the higher the ZTC. Consequently, the device could work more likely in an unstable zone [2]

Modern MOSFET technologies, which guarantee excellent performances in high switching frequency and high power applications, show ever growing g_{fs} values and tend to be inherently less robust to

	Technology	BV_{DSS} [V]	$R_{DSon,typ}$ [mΩ]
Device #1	Std. trench	>40	1.7
Device #2	Optimized planar (for lin. Mode)	>40	3.6
Device #3	New advanced trench	>100	2.3
Device #4	Advanced planar	>100	4.5

Figure 5: **ST DUT main features**

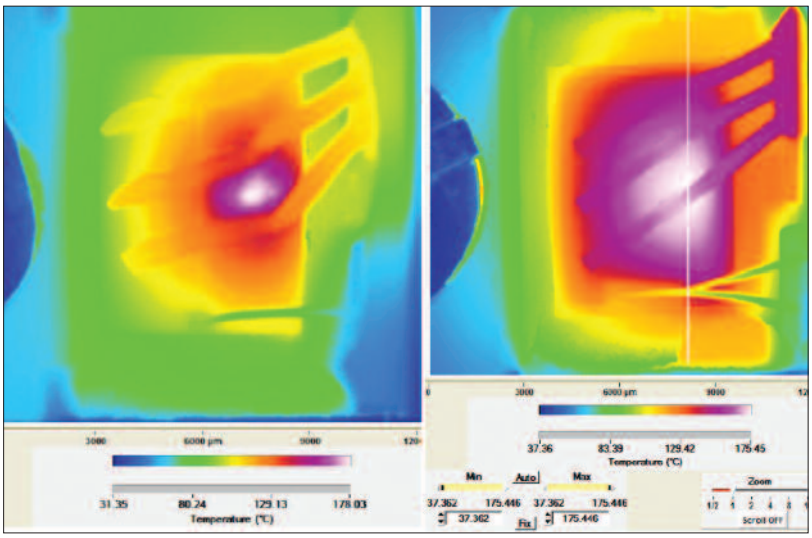


Figure 6: **Die temperature at VDS = 10 V (std. trench tech. on the left, optimized planar tech. on the right)**

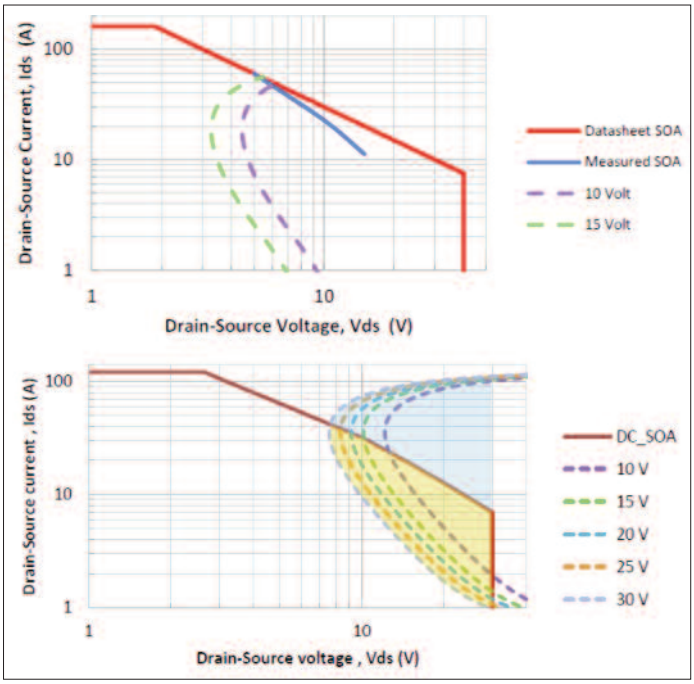


Figure 7: **Standard trench (upper) and optimized technology for linear mode (lower) thermal runaway boundaries**

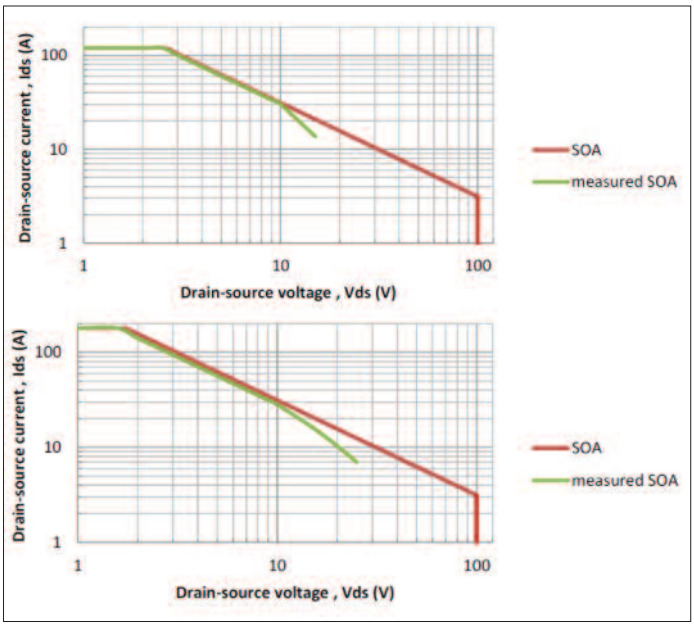


Figure 8: **Measured SOA for advanced planar (upper) and new advanced trench technology device (lower)**

thermal runaway or hot spot phenomena. In Figure 4 the drain current temperature coefficient is depicted as a function of the drain current (T = 25°C).

Thermal instability phenomenon occurs when the device cannot dissipate all the electric power generated. In other words, if P_G is the electrical (or generated) power and P_D is the thermally dissipated power.

ST's MOSFET characterization

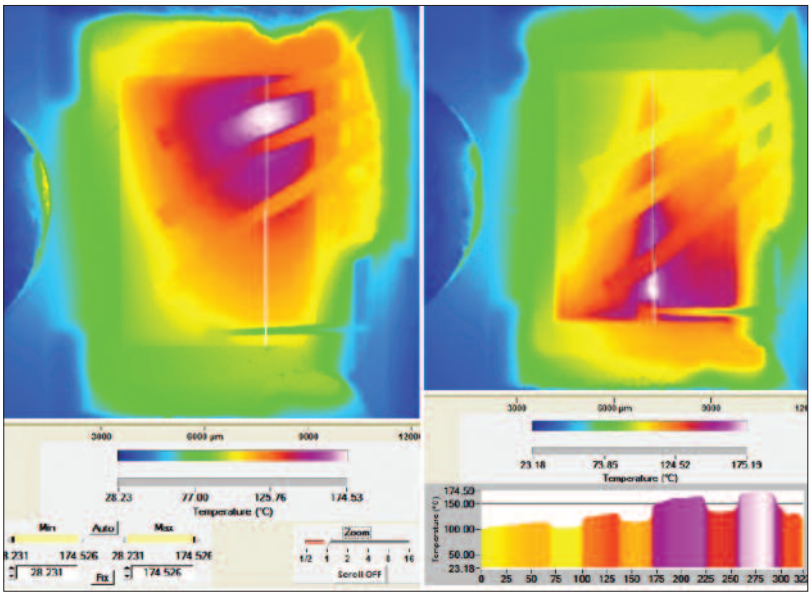
There is a strict correlation between Silicon technology features and MOSFET performances in linear mode. The device ruggedness to thermal runaway and resulting failure can be evaluated by properly combining the SOA curve and drain current thermal coefficient. Furthermore, the R_{th} trend with V_{DS} and junction temperature gives additional information about device performances in linear mode. We performed two different technology comparisons between ST MOSFETs: in the first one, standard trench technology is compared with optimized planar technology for linear mode working (BV_{DSS} = 40 V). In the second comparison, the 100 V device realized in the new advanced trench technology is compared with an advanced planar device (Figure 5).

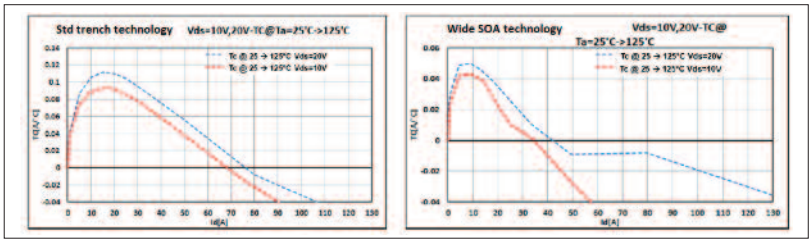
The Standard trench device shows noticeable current focusing phenomena at V_{DS} > 10 V (Figure 6, left image). The reduction of the die active area implies an increase of the device's R_{th} and worse power management. On the other hand, the planar technology optimized for linear mode device shows more uniform die temperature (Figure 6, right image) and a softer Rth trend when VDS increases, with better power dissipation capability. The area between the DC SOA and thermal coefficient curve is the thermal instability zone (Figure 7). The larger this area is (inside the SOA), the less robust the device is in linear mode.

Standard trench technology is able to work without failure in linear mode only at low V_{DS} and I_D; it's not possible to test above V_{DS} = 15 V (T > $T_{j,max}$ = 175 °C). On the other hand, optimized planar technology guarantees better performance and higher power dissipation capabilities in linear mode at higher voltages as well as at lower voltages.

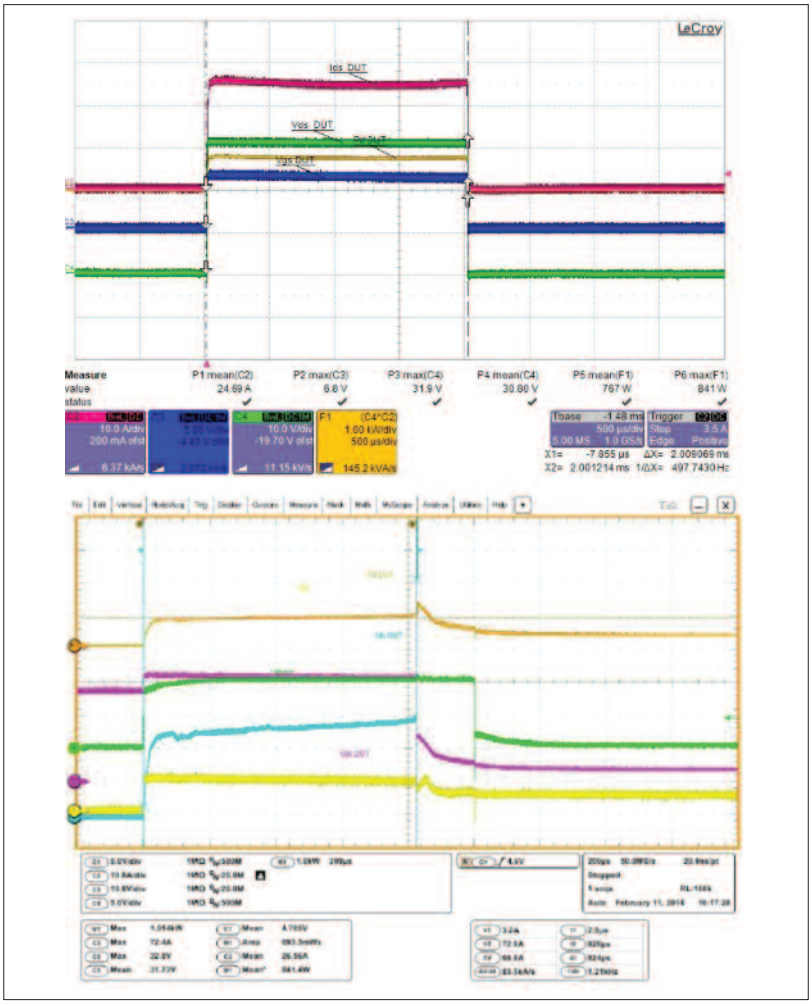
The new advanced trench technology outperforms advanced planar technology in linear mode operation because it is thermally stable for a wider range of operating conditions inside the SOA. Figure 8 illustrates the measured SOA curves for the two technologies.

The new advanced trench device is able to pass the linear mode test up to 25 V, while the advanced planar one fails for V_{DS} > 15 V. Figure 9 shows the relevant





ABOVE Figure 10: **Standard trench (left) and wide SOA (right) thermal coefficient curves**



LEFT Figure 11: **Wide SOA (upper) and standard trench (lower) waveforms in hot swap applications**

LEFT Figure 9: **Thermal picture at VDS = 15 V (left) and VDS= 25 V (right)**

thermal pictures at V_{DS} = 15 V (advanced planar device, left image) and V_{DS} = 25 V (new advanced trench, right image).

Another reason the new advanced trench technology device achieves better performances in linear mode is because of its slightly higher threshold voltage (V_{TH}), ensuring quicker device turn-off and hence more ruggedness when biased in linear mode. In order to further improve linear mode ruggedness, ST has introduced a technology able to meet a wider SOA capability together with very low R_{DSon}. Figure 10 shows the comparison in terms of thermal coefficients between a standard low R_{DSon} trench technology and its equivalent die-size wide SOA.

The wide SOA device has lower maximum thermal coefficient and narrower positive coefficient area (thermal instability zone for MOSFET); this means higher robustness in linear mode operation. As shown in Figure 11, when the device works in hot swap configuration with V_{DS} = 30 V and I_D = 25 A (typical working condition in a telecom environment), the wide SOA device is able to survive at least 2 ms, which is the minimum time gap required by primary customers. On the other hand, a standard trench FET fails after 800 µs.

Conclusions

Modern Silicon technologies, optimized for high current and high switching frequency environments, could be less safe in linear mode than previous planar technologies, optimized for linear mode, due to high values of g_{fs} and ZTC. So, it takes a dedicated device design, especially for new advanced trench technologies, to enhance the performances in linear mode, especially in the worst operating conditions (low I_D and high V_{DS}), and when in higher V_{DS} and R_{th} such a dedicated design can create the right conditions for current focusing and hot spot events.

Literature

[1]. "Thermal instability of low voltage Power MOSFETs," A.Consoli, F.Gennaro, A.Testa, G.Consentino, F.Frisina, R.Letor, A.Magri' – IEEE Transactions on Power Electronics, Vol.15, N.3, May 2000.

[2]. AN-4161, "Practical considerations of Trench MOSFET stability when operating in linear mode," Fairchild Semiconductor.