TSC101A-B-C High side current sense amplifiers

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Abstract

Analog macromodels, for Spice-like simulators, were implemented for TSC101/A/B/C high side current sense amplifiers matching the measured DC, Transient and AC behavior specifications. After a brief introduction to the macromodeling paradigm the simulation results of the implemented macromodels are introduced.

Contents

1 Macromodeling paradigm

Macromodeling of IC is useful for two reason.

The first reason is reduced computational complexity: a full integrated circuit simulation in SPICE could take hours and even days, which is unacceptably slow; the circuit simulation time is proportional to the number of non-linear devices, transistors and diodes, in the circuit and since a large IC could have hundreds and thousands of transistors, there needed to be a way to simulate faster. Verifying a complete analog system via transistor-level simulation is an extremely difficult process and can often become infeasible due to the limitation of simulation capacity. A similar difficulty is encountered when high-level design analysis is performed for the whole system. For these reasons, compact macromodels of analog blocks are desired which can be substituted in place of the real transistor-level netlist to speedup the simulation *with sufficiently high accuracy.*

The second reason for macromodeling is the preservation of proprietary information, Intellectual Property Encryption (IPE): a macromodel *describes the observable behavior but not necessarily the implementation of a device.* Often transistor-level schematics for integrated circuits are not released to the customer therefore, if a customer wants to simulate a given device for evaluation, there is no way for them to know for sure exactly what there is in the circuit; however, the customer can often get a macromodel that replies the device behavior and, *with a good understanding of the model limitations*, can use it for simulation of the device.

2 TSC101A-B-C real features

The TSC101 measures a small differential voltage on a high-side shunt resistor and translates it into a ground-referenced output voltage. The gain is internally fixed: 20V/V for TSC101A, 50V/V for TSC101B and 100V/V for TSC101C.

Current consumption lower than 300μA and wide supply voltage range allow to connect the power supply to either side of the current measurement shunt with minimal error.

The TSC101 high-side current-sense amplifier features a wide input common-mode range $\in$ [2.8V,30V] that is independent of supply voltage Vcc $\in$ [4V,24V], as shown in fig. 1: the main advantage of this feature is to allow high-side current sensing at voltages much greater than the supply voltage Vcc.

The TSC101A/B/C output is buffered so it has a very low output resistance in order to offer the same voltage gain independently of the resistive load.

These features make the TSC101 ideal for automotive current monitoring, notebook computers, dc motor control, photovoltaic systems, battery chargers, precision current sources.

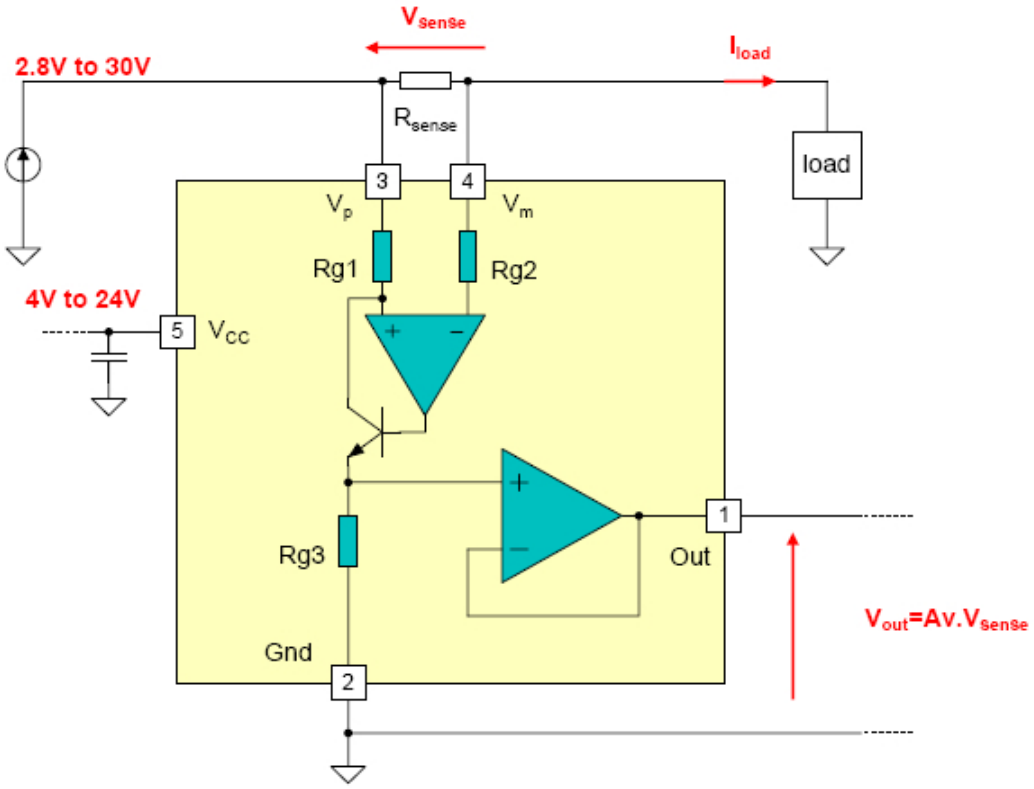

Figure 1: TSC101 high-side current-sense amplifier: the input common-mode range $\in$ [2.8V,30V] is independent of supply voltage Vcc $\in$ [4V,24V].

3 TSC101A-B-C macromodels

The TSC101A-B-C macromodels have a common schematic and they differ in some components values: in fig. 2 3 the macromodel schematic (top and opamp-sr) is shown (schematic notes are only for author's convenience).

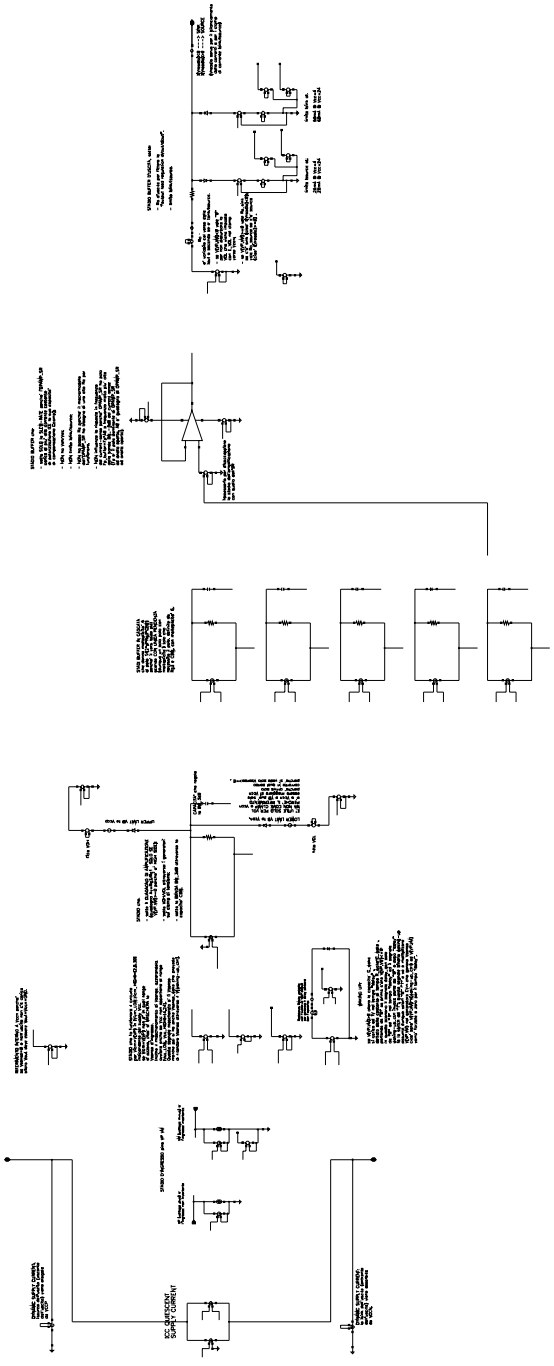

Figure 2: Macromodel top schematic.

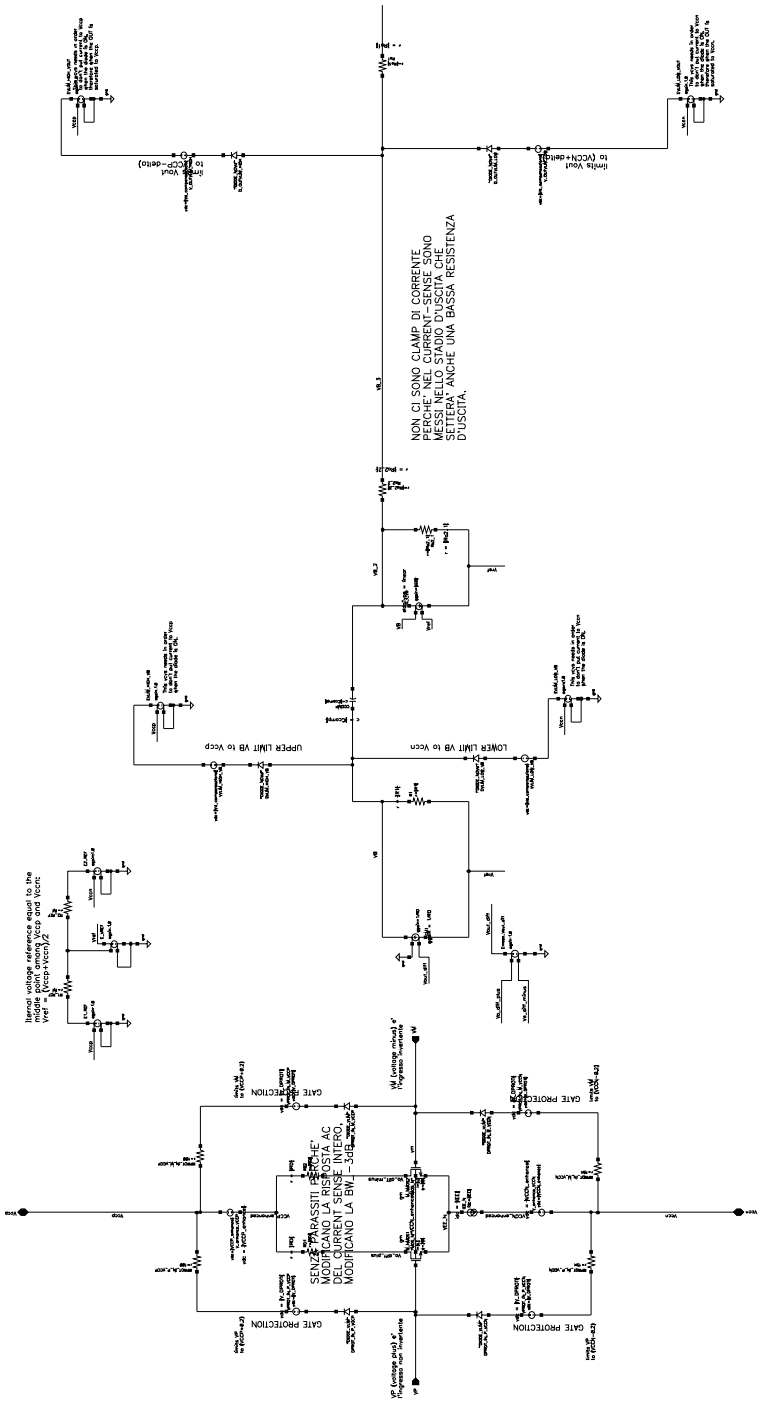

Figure 3: Macromodel opamp-sr schematic.

3.1 TSC101-A-B-C macromodels Library netlists for Spice simulators

The TSC101-A-B-C macromodels subcircuits netlists were collected in a unique Spice compatible syntax library (tested with Cadence Orcad PSpice v10.3.0 and Linear Technology LTSpice v2.22d) as follows:

```
**************************************************************************
*
* WARNING : please consider following remarks before usage
*
* 1) All models are a tradeoff between accuracy and complexity (ie. simulation
*    time).
*
* 2) Macromodels are not a substitute to breadboarding, they rather confirm the
*    validity of a design approach and help to select surrounding component values.
*
* 3) A macromodel emulates the NOMINAL performance of a TYPICAL device within
*    SPECIFIED OPERATING CONDITIONS (ie. temperature, supply voltage, etc.).
*    Thus the macromodel is often not as exhaustive as the datasheet, its goal
*    is to illustrate the main parameters of the product.
*
* 4) Data issued from macromodels used outside of its specified conditions
*    (Vcc, Temperature, etc) or even worse: outside of the device operating
*    conditions (Vcc, Vicm, etc) are not reliable in any way.
*

**************************************************************************
****
***  TSC101A  Spice macromodel subckt
***  September 2008
****
************ CONNECTIONS:
****              INVERTING INPUT
****               |  NON-INVERTING INPUT
****               |   |  OUTPUT
****               |   |   |  POSITIVE POWER SUPPLY
****               |   |   |   |  NEGATIVE POWER SUPPLY
****               |   |   |   |   |
****               |   |   |   |   |
.SUBCKT TSC101A  VM  VP  VS  VCCP VCCN
*
* change all the "IF" ctrl statements with "IF" if you need to use Eldo.
*
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET185 NET257 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 4.32u
    VREADI_ROUT NET191 NET225 DC 0
    VREADI_RWAKE NET282 DELAY_GEN DC 0
```

```
    VVLIM_LOW_VRG3 NET246 NET196 DC {Vd_compensazione}
    VREADIO VB_3 VS DC 0
    VVLIM_HIGH_VRG3 NET206 NET200 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET206 DIODE_NOVd
    DVLIM_LOW_VRG3 NET196 VRG3 DIODE_NOVd
    C86 VRG3_5 VCCN_REF {CBW_A}
    C87 VRG3_6 VCCN_REF {CBW_A}
    C_WAKE DELAY_GEN 0 60p
    C84 VRG3_3 VCCN_REF {CBW_A}
    C79 VRG3_2 VCCN_REF {CBW_A}
    C85 VRG3_4 VCCN_REF {CBW_A}
    CBW VRG3 VCCN_REF {CBW_A}
    E_ROUT NET225 NET249 VALUE={ IF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VRG3_6 0 1.0
    E59 VCCN_REF 0 VCCN 0 1.0
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET185 0 VCCP 0 1.0
    E_VOL NET245 NET246 VALUE={ IF(I(VreadIo)<0 , 24.8*I(VreadIo) , 0 )
+}
    EOUT NET249 0 VRG3_SR 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={IF( V(Vsense)<= -100m , (8.68e-6 -
+4.32e-6) , (-43e-6)*V(Vsense) )}
    E65 NET257 0 VCCN 0 1.0
    E_VOH NET261 NET200 VALUE={ IF(I(VreadIo)<5m , 640m , -0.031 +
+134.2*I(VreadIo) ) }
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0

* Eldo:
*    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 81k ) (3m , 60k)
*+(4m , 48k) ( 5m , 40.5k ) (7m , 32k) ( 9m , 27.1k ) (12m 22.7k) ( 15m ,
*+20k ) (17m 18.75k) ( 20m , 17.5k ) ( 25m , 15.7k ) ( 30m , 14.5k ) ( 35m
*+, 13.7k ) ( 40m , 13.2k ) ( 50m , 12.4k ) ( 60m , 11.7k ) ( 70m , 11.35k
*+) ( 80m , 11k ) ( 90m , 10.8k ) ( 100m , 10.61k ) ( 120m , 10.35k ) (
*+150m , 10.15k )
*
* PSpice:
    E_RWAKE_VAL RWAKE_VAL 0 VALUE={TABLE( V(VP,VM), 2m , 81k , 3m , 60k ,
+ 4m , 48k , 5m , 40.5k , 7m , 32k , 9m , 27.1k , 12m , 22.7k , 15m ,
+ 20k , 17m , 18.75k , 20m , 17.5k , 25m , 15.7k , 30m , 14.5k , 35m ,
+ 13.7k , 40m , 13.2k , 50m , 12.4k , 60m , 11.7k , 70m , 11.35k ,
+ 80m , 11k , 90m , 10.8k , 100m , 10.61k , 120m , 10.35k , 150m , 10.15k )}

    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={IF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET277 0 VALUE={IF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET277 NET282 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
```

```
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={IF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={IF( (V(VP)>=Vicm_LOW) & (V(VP)<=Vicm_HIGH) &
+(V(Vccp,Vccn)>=Vcc_LOW) & (V(Vccp,Vccn)<=Vcc_HIGH) , V(VP,VM) , 0)}
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET261 0 VCCP 0 1.0
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={IF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    EVLIM_LOW_VRG3 NET245 0 VCCN 0 1.0
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -299.5 -5000*I(VreadIo)}
    R144 VCCN_REF VRG3_6 {Rg3_A}
    R136 VCCN_REF VRG3_2 {Rg3_A}
    R142 VCCN_REF VRG3_4 {Rg3_A}
    RO2_2 NET191 VB_3 {Ro2_2}
    R143 VCCN_REF VRG3_5 {Rg3_A}
    R141 VCCN_REF VRG3_3 {Rg3_A}
    R1 VCCN_REF VRG3 {Rg3_A}
    G_ICC_VSENSE VCCP VCCN VALUE={IF( V(Vsense)>0 , 3.5e-5 +
+0.0015*V(Vsense) , 0 )}
    G_IIB-VP_VSENSE VP 0 VALUE={IF( V(Vsense)>0 , V(Vsense)/Rg1 , 0 )}
    G70 VCCN_REF VRG3_6 VRG3_5 VCCN_REF {1/Rg3_A}
    G67 VCCN_REF VRG3_3 VRG3_2 VCCN_REF {1/Rg3_A}
    G60 VM 0 VALUE={IF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G68 VCCN_REF VRG3_4 VRG3_3 VCCN_REF {1/Rg3_A}
    G62 VCCN_REF VRG3_2 VRG3 VCCN_REF {1/Rg3_A}
    G69 VCCN_REF VRG3_5 VRG3_4 VCCN_REF {1/Rg3_A}
    G_IOUT_SOURCED VCCP 0 VALUE={IF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 VCCN_REF VRG3 VALUE={IF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0
+)}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP VCCN 1.26e-4 3.25e-6
    G_IOUT_SINKED VCCN 0 VALUE={IF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.



********************************************************************************
****
***  TSC101B  Spice macromodel subckt
***  September 2008
****
************ CONNECTIONS:
****              INVERTING INPUT
****               |  NON-INVERTING INPUT
****               |   |  OUTPUT
****               |   |   |  POSITIVE POWER SUPPLY
```

```
****              |   |   |   |  NEGATIVE POWER SUPPLY
****              |   |   |   |   |
****              |   |   |   |   |
.SUBCKT TSC101B  VM  VP  VS  VCCP VCCN
*
* change all the "IF" ctrl statements with "IF" if you need to use Eldo.
*
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET185 NET257 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 4.32u
    VREADI_ROUT NET191 NET225 DC 0
    VREADI_RWAKE NET282 DELAY_GEN DC 0
    VVLIM_LOW_VRG3 NET246 NET196 DC {Vd_compensazione}
    VREADIO VB_3 VS DC 0
    VVLIM_HIGH_VRG3 NET206 NET200 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET206 DIODE_NOVd
    DVLIM_LOW_VRG3 NET196 VRG3 DIODE_NOVd
    C86 VRG3_5 VCCN_REF {CBW_B}
    C87 VRG3_6 VCCN_REF {CBW_B}
    C_WAKE DELAY_GEN 0 60p
    C84 VRG3_3 VCCN_REF {CBW_B}
    C79 VRG3_2 VCCN_REF {CBW_B}
    C85 VRG3_4 VCCN_REF {CBW_B}
    CBW VRG3 VCCN_REF {CBW_B}
    E_ROUT NET225 NET249 VALUE={ IF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VRG3_6 0 1.0
    E59 VCCN_REF 0 VCCN 0 1.0
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET185 0 VCCP 0 1.0
    E_VOL NET245 NET246 VALUE={ IF(I(VreadIo)<0 , 24.8*I(VreadIo) , 0 )
+}
    EOUT NET249 0 VRG3_SR 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={IF( V(Vsense)<= -100m , (8.68e-6 -
+4.32e-6) , (-43e-6)*V(Vsense) )}
    E65 NET257 0 VCCN 0 1.0
    E_VOH NET261 NET200 VALUE={ IF(I(VreadIo)<5m , 640m , -0.031 +
+134.2*I(VreadIo) ) }
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0

* Eldo:
*    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 81k ) (3m , 60k)
*+(4m , 48k) ( 5m , 40.5k ) (7m , 32k) ( 9m , 27.1k ) (12m 22.7k) ( 15m ,
*+20k ) (17m 18.75k) ( 20m , 17.5k ) ( 25m , 15.7k ) ( 30m , 14.5k ) ( 35m
*+, 13.7k ) ( 40m , 13.2k ) ( 50m , 12.4k ) ( 60m , 11.7k ) ( 70m , 11.35k
*+) ( 80m , 11k ) ( 90m , 10.8k ) ( 100m , 10.61k ) ( 120m , 10.35k ) (
*+150m , 10.15k )
*
```

```
* PSpice:
    E_RWAKE_VAL RWAKE_VAL 0 VALUE={TABLE( V(VP,VM), 2m , 81k , 3m , 60k ,
+ 4m , 48k , 5m , 40.5k , 7m , 32k , 9m , 27.1k , 12m , 22.7k , 15m ,
+ 20k , 17m , 18.75k , 20m , 17.5k , 25m , 15.7k , 30m , 14.5k , 35m ,
+ 13.7k , 40m , 13.2k , 50m , 12.4k , 60m , 11.7k , 70m , 11.35k ,
+ 80m , 11k , 90m , 10.8k , 100m , 10.61k , 120m , 10.35k , 150m , 10.15k )}

    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={IF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET277 0 VALUE={IF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET277 NET282 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={IF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={IF( (V(VP)>=Vicm_LOW) & (V(VP)<=Vicm_HIGH) &
+(V(Vccp,Vccn)>=Vcc_LOW) & (V(Vccp,Vccn)<=Vcc_HIGH) , V(VP,VM) , 0)}
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET261 0 VCCP 0 1.0
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={IF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    EVLIM_LOW_VRG3 NET245 0 VCCN 0 1.0
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -299.5 -5000*I(VreadIo)}
    R144 VCCN_REF VRG3_6 {Rg3_B}
    R136 VCCN_REF VRG3_2 {Rg3_B}
    R142 VCCN_REF VRG3_4 {Rg3_B}
    RO2_2 NET191 VB_3 {Ro2_2}
    R143 VCCN_REF VRG3_5 {Rg3_B}
    R141 VCCN_REF VRG3_3 {Rg3_B}
    R1 VCCN_REF VRG3 {Rg3_B}
    G_ICC_VSENSE VCCP VCCN VALUE={IF( V(Vsense)>0 , 3.5e-5 +
+0.0015*V(Vsense) , 0 )}
    G_IIB-VP_VSENSE VP 0 VALUE={IF( V(Vsense)>0 , V(Vsense)/Rg1 , 0 )}
    G70 VCCN_REF VRG3_6 VRG3_5 VCCN_REF {1/Rg3_B}
    G67 VCCN_REF VRG3_3 VRG3_2 VCCN_REF {1/Rg3_B}
    G60 VM 0 VALUE={IF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G68 VCCN_REF VRG3_4 VRG3_3 VCCN_REF {1/Rg3_B}
    G62 VCCN_REF VRG3_2 VRG3 VCCN_REF {1/Rg3_B}
    G69 VCCN_REF VRG3_5 VRG3_4 VCCN_REF {1/Rg3_B}
    G_IOUT_SOURCED VCCP 0 VALUE={IF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 VCCN_REF VRG3 VALUE={IF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0
+)}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP VCCN 1.26e-4 3.25e-6
    G_IOUT_SINKED VCCN 0 VALUE={IF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.
```

```
*********************************************************************************
****
***  TSC101C  Spice macromodel subckt
***  September 2008
****
************ CONNECTIONS:
****              INVERTING INPUT
****               |  NON-INVERTING INPUT
****               |   |  OUTPUT
****               |   |   |  POSITIVE POWER SUPPLY
****               |   |   |   |  NEGATIVE POWER SUPPLY
****               |   |   |   |   |
****               |   |   |   |   |
.SUBCKT TSC101C  VM  VP  VS  VCCP VCCN
*
* change all the "IF" ctrl statements with "IF" if you need to use Eldo.
*
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET185 NET257 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 4.32u
    VREADI_ROUT NET191 NET225 DC 0
    VREADI_RWAKE NET282 DELAY_GEN DC 0
    VVLIM_LOW_VRG3 NET246 NET196 DC {Vd_compensazione}
    VREADIO VB_3 VS DC 0
    VVLIM_HIGH_VRG3 NET206 NET200 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET206 DIODE_NOVd
    DVLIM_LOW_VRG3 NET196 VRG3 DIODE_NOVd
    C86 VRG3_5 VCCN_REF {CBW_C}
    C87 VRG3_6 VCCN_REF {CBW_C}
    C_WAKE DELAY_GEN 0 60p
    C84 VRG3_3 VCCN_REF {CBW_C}
    C79 VRG3_2 VCCN_REF {CBW_C}
    C85 VRG3_4 VCCN_REF {CBW_C}
    CBW VRG3 VCCN_REF {CBW_C}
    E_ROUT NET225 NET249 VALUE={ IF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VRG3_6 0 1.0
    E59 VCCN_REF 0 VCCN 0 1.0
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET185 0 VCCP 0 1.0
    E_VOL NET245 NET246 VALUE={ IF(I(VreadIo)<0 , 24.8*I(VreadIo) , 0 )
+}
    EOUT NET249 0 VRG3_SR 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={IF( V(Vsense)<= -100m , (8.68e-6 -
+4.32e-6) , (-43e-6)*V(Vsense) )}
    E65 NET257 0 VCCN 0 1.0
```

```
    E_VOH NET261 NET200 VALUE={ IF(I(VreadIo)<5m , 640m , -0.031 +
+134.2*I(VreadIo) ) }
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0

* Eldo:
*    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 81k ) (3m , 60k)
*+(4m , 48k) ( 5m , 40.5k ) (7m , 32k) ( 9m , 27.1k ) (12m 22.7k) ( 15m ,
*+20k ) (17m 18.75k) ( 20m , 17.5k ) ( 25m , 15.7k ) ( 30m , 14.5k ) ( 35m
*+, 13.7k ) ( 40m , 13.2k ) ( 50m , 12.4k ) ( 60m , 11.7k ) ( 70m , 11.35k
*+) ( 80m , 11k ) ( 90m , 10.8k ) ( 100m , 10.61k ) ( 120m , 10.35k ) (
*+150m , 10.15k )
*
* PSpice:
    E_RWAKE_VAL RWAKE_VAL 0 VALUE={TABLE( V(VP,VM), 2m , 81k , 3m , 60k ,
+ 4m , 48k , 5m , 40.5k , 7m , 32k , 9m , 27.1k , 12m , 22.7k , 15m ,
+ 20k , 17m , 18.75k , 20m , 17.5k , 25m , 15.7k , 30m , 14.5k , 35m ,
+ 13.7k , 40m , 13.2k , 50m , 12.4k , 60m , 11.7k , 70m , 11.35k ,
+ 80m , 11k , 90m , 10.8k , 100m , 10.61k , 120m , 10.35k , 150m , 10.15k )}

    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={IF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET277 0 VALUE={IF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET277 NET282 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={IF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={IF( (V(VP)>=Vicm_LOW) & (V(VP)<=Vicm_HIGH) &
+(V(Vccp,Vccn)>=Vcc_LOW) & (V(Vccp,Vccn)<=Vcc_HIGH) , V(VP,VM) , 0)}
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET261 0 VCCP 0 1.0
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={IF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    EVLIM_LOW_VRG3 NET245 0 VCCN 0 1.0
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -299.5 -5000*I(VreadIo)}
    R144 VCCN_REF VRG3_6 {Rg3_C}
    R136 VCCN_REF VRG3_2 {Rg3_C}
    R142 VCCN_REF VRG3_4 {Rg3_C}
    RO2_2 NET191 VB_3 {Ro2_2}
    R143 VCCN_REF VRG3_5 {Rg3_C}
    R141 VCCN_REF VRG3_3 {Rg3_C}
    R1 VCCN_REF VRG3 {Rg3_C}
    G_ICC_VSENSE VCCP VCCN VALUE={IF( V(Vsense)>0 , 3.5e-5 +
+0.0015*V(Vsense) , 0 )}
    G_IIB-VP_VSENSE VP 0 VALUE={IF( V(Vsense)>0 , V(Vsense)/Rg1 , 0 )}
    G70 VCCN_REF VRG3_6 VRG3_5 VCCN_REF {1/Rg3_C}
    G67 VCCN_REF VRG3_3 VRG3_2 VCCN_REF {1/Rg3_C}
```

```
    G60 VM 0 VALUE={IF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G68 VCCN_REF VRG3_4 VRG3_3 VCCN_REF {1/Rg3_C}
    G62 VCCN_REF VRG3_2 VRG3 VCCN_REF {1/Rg3_C}
    G69 VCCN_REF VRG3_5 VRG3_4 VCCN_REF {1/Rg3_C}
    G_IOUT_SOURCED VCCP 0 VALUE={IF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 VCCN_REF VRG3 VALUE={IF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0
+)}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP VCCN 1.26e-4 3.25e-6
    G_IOUT_SINKED VCCN 0 VALUE={IF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.



********************************************************************************
*
* MODELS/SUBCKTS and PARAMS used by TSC101A-B-C subckt:
*

.SUBCKT OPAMP_SR VM VP VS VCCP VCCN
    M_NMOS2 VO_DIFF_MINUS VM VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    M_NMOS1 VO_DIFF_PLUS VP VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    IEE_N VEE_N VCCN_ENHANCED DC {IEE}
    VVLIM_LOW_VB NET0109 NET0110 DC {Vd_compensazione}
    VPROT_IN_P_VCCP NET0123 NET0134 DC {V_DPROT}
    V_ENHANCE_VCCN VCCN_ENHANCED VCCN DC {VCCN_enhance}
    VVLIM_HIGH_VB NET0187 NET0153 DC {Vd_compensazione}
    V_ENHANCE_VCCP VCCP_ENHANCED VCCP DC {VCCP_enhance}
    V_OUTVLIM_LOW NET0224 NET125 DC {Vd_compensazione}
    VPROT_IN_M_VCCN NET0116 NET0192 DC {V_DPROT}
    V_OUTVLIM_HIGH NET0201 NET0131 DC {Vd_compensazione}
    VPROT_IN_P_VCCN NET0115 NET096 DC {V_DPROT}
    VPROT_IN_M_VCCP NET0190 NET0135 DC {V_DPROT}
    DVLIM_HIGH_VB VB NET0187 DIODE_NOVd
    DPROT_IN_M_VCCP VM NET0135 DIODE_VLIM
    DVLIM_LOW_VB NET0110 VB DIODE_NOVd
    DPROT_IN_M_VCCN NET0116 VM DIODE_VLIM
    D_OUTVLIM_LOW NET125 VB_3 DIODE_NOVd
    DPROT_IN_P_VCCP VP NET0134 DIODE_VLIM
    DPROT_IN_P_VCCN NET0115 VP DIODE_VLIM
    D_OUTVLIM_HIGH VB_3 NET0201 DIODE_NOVd
    CCOMP VB VB_2 {Ccomp}
    EMEAS_VOUT_DIFF VOUT_DIFF 0 VO_DIFF_PLUS VO_DIFF_MINUS 1.0
    EVLIM_HIGH_VB NET0153 0 VCCP 0 1.0
    EVLIM_HIGH_VOUT NET0131 0 VCCP 0 1.0
    EVLIM_LOW_VB NET0109 0 VCCN 0 1.0
    E2_REF NET0238 0 VCCN 0 1.0
    E_VREF VREF 0 NET0250 0 1.0
    E1_REF NET0210 0 VCCP 0 1.0
    EVLIM_LOW_VOUT NET0224 0 VCCN 0 1.0
    RO2_2 VB_3 VB_2 {Ro2_2}
```

```
    RPROT_IN_P_VCCP NET0123 VCCP 100
    RPROT_IN_M_VCCP VCCP NET0190 100
    RO1 VS VB_3 {Ro1}
    RD1 VCCP_ENHANCED VO_DIFF_PLUS {RD}
    RD2 VCCP_ENHANCED VO_DIFF_MINUS {RD}
    RO2_1 VREF VB_2 {Ro2_1}
    R1_REF NET0210 NET0250 1Meg
    R1 VB VREF {R1}
    RPROT_IN_M_VCCN VCCN NET0192 15K
    R2_REF NET0250 NET0238 1Meg
    RPROT_IN_P_VCCN NET096 VCCN 15K
    G_I_VB VB_2 VREF VB VREF {GB}
    GM1 VREF VB VOUT_DIFF 0 {1/RD}
.ENDS
*** End of subcircuit definition.


.PARAM Vicm_LOW  = 2.8
.PARAM Vicm_HIGH = 30
.PARAM Vcc_LOW  = 4
.PARAM Vcc_HIGH = 24
.PARAM Iib = 5.5e-6
.PARAM Rg1 = 5k
.PARAM Av_A  = 20
.PARAM Av_B  = 50
.PARAM Av_C  = 100
.PARAM Rg3_A = {Av_A*Rg1}
.PARAM Rg3_B = {Av_B*Rg1}
.PARAM Rg3_C = {Av_C*Rg1}
.PARAM Ro_sink = 1m
.PARAM Ro_source = 3
.PARAM Ro_off = 0.82
.PARAM alpha_switch_Ro = 1e4
.PARAM CBW_A = 1.08p
.PARAM CBW_B = 0.32p
.PARAM CBW_C = 0.243p
.PARAM RD=1k
.PARAM VCCP_enhance=-100m
.PARAM VCCN_enhance=-700m
.PARAM Ccomp=11p
.PARAM IEE=10u
.PARAM A0=97.93103448E3
.PARAM Ro=17587.2
.PARAM W=11u
.PARAM L=1u
.PARAM gm_mos=0.0002348021861505248
.PARAM GB=10m
.PARAM Ro1=1
.PARAM Ro2_2=1e-3
.PARAM Ro2_1={Ro - Ro2_2 - Ro1}
.PARAM R1={A0/(gm_mos*GB*Ro2_1)}
```

```
.PARAM V_DPROT=0.6
.PARAM Vd_compensazione=-245.4u

* Eldo:
*.MODEL MOS_N  NMOS LEVEL=1 MODTYPE=ELDO VTO=+0.65  KP=500E-6
*.MODEL DIODE_NOVd D LEVEL=1 MODTYPE=ELDO IS=10E-15 N=0.001
*.MODEL DIODE_VLIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
*.MODEL DIODE_ILIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
*.MODEL DX D LEVEL=1 MODTYPE=ELDO IS=1E-14
*
* PSpice:
.MODEL MOS_N  NMOS LEVEL=1  VTO=+0.65  KP=500E-6
.MODEL DIODE_NOVd D LEVEL=1  IS=10E-15 N=0.001
.MODEL DIODE_VLIM D LEVEL=1  IS=0.8E-15
.MODEL DIODE_ILIM D LEVEL=1  IS=0.8E-15
.MODEL DX D LEVEL=1  IS=1E-14
*
**********************************************************************************
```

3.2 TSC101-A-B-C macromodels Library netlists for Eldo simulator

The TSC101-A-B-C macromodels subcircuits netlists were collected in a unique Eldo (Mentor Graphics) compatible syntax library as follows: (N.B.: simulating it the user has not to use the -stver option running Eldo simulator, because the TSC101 macromodel netlist uses basic standard analog devices, not STMicroelectronics version instead used in real TSC101 netlist)

```
*****************************************************************************
*
* WARNING : please consider following remarks before usage
*
* 1) All models are a tradeoff between accuracy and complexity (ie. simulation
*    time).
*
* 2) Macromodels are not a substitute to breadboarding, they rather confirm the
*    validity of a design approach and help to select surrounding component values.
*
* 3) A macromodel emulates the NOMINAL performance of a TYPICAL device within
*    SPECIFIED OPERATING CONDITIONS (ie. temperature, supply voltage, etc.).
*    Thus the macromodel is often not as exhaustive as the datasheet, its goal
*    is to illustrate the main parameters of the product.
*
* 4) Data issued from macromodels used outside of its specified conditions
*    (Vcc, Temperature, etc) or even worse: outside of the device operating
*    conditions (Vcc, Vicm, etc) are not reliable in any way.
*


*****************************************************************************
****
***  TSC101A  Eldo macromodel subckt
***  September 2008
****
************ CONNECTIONS:
****              INVERTING INPUT
****               |  NON-INVERTING INPUT
****               |   |  OUTPUT
****               |   |   |  POSITIVE POWER SUPPLY
****               |   |   |   |  NEGATIVE POWER SUPPLY
****               |   |   |   |   |
****               |   |   |   |   |
.SUBCKT TSC101A  VM  VP  VS  VCCP VCCN
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET185 NET257 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 4.32u
    VREADI_ROUT NET191 NET225 DC 0
```

```
    VREADI_RWAKE NET282 DELAY_GEN DC 0
    VVLIM_LOW_VRG3 NET246 NET196 DC {Vd_compensazione}
    VREADIO VB_3 VS DC 0
    VVLIM_HIGH_VRG3 NET206 NET200 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET206 DIODE_NOVd
    DVLIM_LOW_VRG3 NET196 VRG3 DIODE_NOVd
    C86 VRG3_5 VCCN_REF {CBW_A}
    C87 VRG3_6 VCCN_REF {CBW_A}
    C_WAKE DELAY_GEN 0 60p
    C84 VRG3_3 VCCN_REF {CBW_A}
    C79 VRG3_2 VCCN_REF {CBW_A}
    C85 VRG3_4 VCCN_REF {CBW_A}
    CBW VRG3 VCCN_REF {CBW_A}
    E_ROUT NET225 NET249 VALUE={ VALIF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VRG3_6 0 1.0
    E59 VCCN_REF 0 VCCN 0 1.0
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET185 0 VCCP 0 1.0
    E_VOL NET245 NET246 VALUE={ VALIF(I(VreadIo)<0 , 24.8*I(VreadIo) , 0 )
+}
    EOUT NET249 0 VRG3_SR 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={VALIF( V(Vsense)<= -100m , (8.68e-6 -
+4.32e-6) , (-43e-6)*V(Vsense) )}
    E65 NET257 0 VCCN 0 1.0
    E_VOH NET261 NET200 VALUE={ VALIF(I(VreadIo)<5m , 640m , -0.031 +
+134.2*I(VreadIo) ) }
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0
    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 81k ) (3m , 60k)
+(4m , 48k) ( 5m , 40.5k ) (7m , 32k) ( 9m , 27.1k ) (12m 22.7k) ( 15m ,
+20k ) (17m 18.75k) ( 20m , 17.5k ) ( 25m , 15.7k ) ( 30m , 14.5k ) ( 35m
+, 13.7k ) ( 40m , 13.2k ) ( 50m , 12.4k ) ( 60m , 11.7k ) ( 70m , 11.35k
+) ( 80m , 11k ) ( 90m , 10.8k ) ( 100m , 10.61k ) ( 120m , 10.35k ) (
+150m , 10.15k )
    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={VALIF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET277 0 VALUE={VALIF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET277 NET282 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={VALIF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={VALIF( (V(VP)>=Vicm_LOW) & (V(VP)<=Vicm_HIGH) &
+(V(Vccp,Vccn)>=Vcc_LOW) & (V(Vccp,Vccn)<=Vcc_HIGH) , V(VP,VM) , 0)}
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
```

```
    EVLIM_HIGH_VRG3 NET261 0 VCCP 0 1.0
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={VALIF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    EVLIM_LOW_VRG3 NET245 0 VCCN 0 1.0
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -299.5 -5000*I(VreadIo)}
    R144 VCCN_REF VRG3_6 {Rg3_A}
    R136 VCCN_REF VRG3_2 {Rg3_A}
    R142 VCCN_REF VRG3_4 {Rg3_A}
    RO2_2 NET191 VB_3 {Ro2_2}
    R143 VCCN_REF VRG3_5 {Rg3_A}
    R141 VCCN_REF VRG3_3 {Rg3_A}
    R1 VCCN_REF VRG3 {Rg3_A}
    G_ICC_VSENSE VCCP VCCN VALUE={VALIF( V(Vsense)>0 , 3.5e-5 +
+0.0015*V(Vsense) , 0 )}
    G_IIB-VP_VSENSE VP 0 VALUE={VALIF( V(Vsense)>0 , V(Vsense)/Rg1 , 0 )}
    G70 VCCN_REF VRG3_6 VRG3_5 VCCN_REF {1/Rg3_A}
    G67 VCCN_REF VRG3_3 VRG3_2 VCCN_REF {1/Rg3_A}
    G60 VM 0 VALUE={VALIF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G68 VCCN_REF VRG3_4 VRG3_3 VCCN_REF {1/Rg3_A}
    G62 VCCN_REF VRG3_2 VRG3 VCCN_REF {1/Rg3_A}
    G69 VCCN_REF VRG3_5 VRG3_4 VCCN_REF {1/Rg3_A}
    G_IOUT_SOURCED VCCP 0 VALUE={VALIF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 VCCN_REF VRG3 VALUE={VALIF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0
+)}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP VCCN 1.26e-4 3.25e-6
    G_IOUT_SINKED VCCN 0 VALUE={VALIF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.


********************************************************************************
****
***  TSC101B  Eldo macromodel subckt
***  September 2008
****
************ CONNECTIONS:
****              INVERTING INPUT
****               |  NON-INVERTING INPUT
****               |   |  OUTPUT
****               |   |   |  POSITIVE POWER SUPPLY
****               |   |   |   |  NEGATIVE POWER SUPPLY
****               |   |   |   |   |
****               |   |   |   |   |
.SUBCKT TSC101B  VM  VP  VS  VCCP VCCN
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET185 NET257 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 4.32u
    VREADI_ROUT NET191 NET225 DC 0
    VREADI_RWAKE NET282 DELAY_GEN DC 0
    VVLIM_LOW_VRG3 NET246 NET196 DC {Vd_compensazione}
```

```
    VREADIO VB_3 VS DC 0
    VVLIM_HIGH_VRG3 NET206 NET200 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET206 DIODE_NOVd
    DVLIM_LOW_VRG3 NET196 VRG3 DIODE_NOVd
    C86 VRG3_5 VCCN_REF {CBW_B}
    C87 VRG3_6 VCCN_REF {CBW_B}
    C_WAKE DELAY_GEN 0 60p
    C84 VRG3_3 VCCN_REF {CBW_B}
    C79 VRG3_2 VCCN_REF {CBW_B}
    C85 VRG3_4 VCCN_REF {CBW_B}
    CBW VRG3 VCCN_REF {CBW_B}
    E_ROUT NET225 NET249 VALUE={ VALIF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VRG3_6 0 1.0
    E59 VCCN_REF 0 VCCN 0 1.0
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET185 0 VCCP 0 1.0
    E_VOL NET245 NET246 VALUE={ VALIF(I(VreadIo)<0 , 24.8*I(VreadIo) , 0 )
+}
    EOUT NET249 0 VRG3_SR 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={VALIF( V(Vsense)<= -100m , (8.68e-6 -
+4.32e-6) , (-43e-6)*V(Vsense) )}
    E65 NET257 0 VCCN 0 1.0
    E_VOH NET261 NET200 VALUE={ VALIF(I(VreadIo)<5m , 640m , -0.031 +
+134.2*I(VreadIo) ) }
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0
    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 81k ) (3m , 60k)
+(4m , 48k) ( 5m , 40.5k ) (7m , 32k) ( 9m , 27.1k ) (12m 22.7k) ( 15m ,
+20k ) (17m 18.75k) ( 20m , 17.5k ) ( 25m , 15.7k ) ( 30m , 14.5k ) ( 35m
+, 13.7k ) ( 40m , 13.2k ) ( 50m , 12.4k ) ( 60m , 11.7k ) ( 70m , 11.35k
+) ( 80m , 11k ) ( 90m , 10.8k ) ( 100m , 10.61k ) ( 120m , 10.35k ) (
+150m , 10.15k )
    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={VALIF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET277 0 VALUE={VALIF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET277 NET282 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={VALIF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={VALIF( (V(VP)>=Vicm_LOW) & (V(VP)<=Vicm_HIGH) &
+(V(Vccp,Vccn)>=Vcc_LOW) & (V(Vccp,Vccn)<=Vcc_HIGH) , V(VP,VM) , 0)}
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET261 0 VCCP 0 1.0
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
```

```
+VALUE={VALIF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    EVLIM_LOW_VRG3 NET245 0 VCCN 0 1.0
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -299.5 -5000*I(VreadIo)}
    R144 VCCN_REF VRG3_6 {Rg3_B}
    R136 VCCN_REF VRG3_2 {Rg3_B}
    R142 VCCN_REF VRG3_4 {Rg3_B}
    RO2_2 NET191 VB_3 {Ro2_2}
    R143 VCCN_REF VRG3_5 {Rg3_B}
    R141 VCCN_REF VRG3_3 {Rg3_B}
    R1 VCCN_REF VRG3 {Rg3_B}
    G_ICC_VSENSE VCCP VCCN VALUE={VALIF( V(Vsense)>0 , 3.5e-5 +
+0.0015*V(Vsense) , 0 )}
    G_IIB-VP_VSENSE VP 0 VALUE={VALIF( V(Vsense)>0 , V(Vsense)/Rg1 , 0 )}
    G70 VCCN_REF VRG3_6 VRG3_5 VCCN_REF {1/Rg3_B}
    G67 VCCN_REF VRG3_3 VRG3_2 VCCN_REF {1/Rg3_B}
    G60 VM 0 VALUE={VALIF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G68 VCCN_REF VRG3_4 VRG3_3 VCCN_REF {1/Rg3_B}
    G62 VCCN_REF VRG3_2 VRG3 VCCN_REF {1/Rg3_B}
    G69 VCCN_REF VRG3_5 VRG3_4 VCCN_REF {1/Rg3_B}
    G_IOUT_SOURCED VCCP 0 VALUE={VALIF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 VCCN_REF VRG3 VALUE={VALIF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0
+)}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP VCCN 1.26e-4 3.25e-6
    G_IOUT_SINKED VCCN 0 VALUE={VALIF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.


********************************************************************************
****
***  TSC101C  Eldo macromodel subckt
***  September 2008
****
************ CONNECTIONS:
****              INVERTING INPUT
****               |  NON-INVERTING INPUT
****               |   |  OUTPUT
****               |   |   |  POSITIVE POWER SUPPLY
****               |   |   |   |  NEGATIVE POWER SUPPLY
****               |   |   |   |   |
****               |   |   |   |   |
.SUBCKT TSC101C  VM  VP  VS  VCCP VCCN
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET185 NET257 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 4.32u
    VREADI_ROUT NET191 NET225 DC 0
    VREADI_RWAKE NET282 DELAY_GEN DC 0
    VVLIM_LOW_VRG3 NET246 NET196 DC {Vd_compensazione}
    VREADIO VB_3 VS DC 0
    VVLIM_HIGH_VRG3 NET206 NET200 DC {Vd_compensazione}
```

```
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET206 DIODE_NOVd
    DVLIM_LOW_VRG3 NET196 VRG3 DIODE_NOVd
    C86 VRG3_5 VCCN_REF {CBW_C}
    C87 VRG3_6 VCCN_REF {CBW_C}
    C_WAKE DELAY_GEN 0 60p
    C84 VRG3_3 VCCN_REF {CBW_C}
    C79 VRG3_2 VCCN_REF {CBW_C}
    C85 VRG3_4 VCCN_REF {CBW_C}
    CBW VRG3 VCCN_REF {CBW_C}
    E_ROUT NET225 NET249 VALUE={ VALIF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VRG3_6 0 1.0
    E59 VCCN_REF 0 VCCN 0 1.0
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET185 0 VCCP 0 1.0
    E_VOL NET245 NET246 VALUE={ VALIF(I(VreadIo)<0 , 24.8*I(VreadIo) , 0 )
+}
    EOUT NET249 0 VRG3_SR 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={VALIF( V(Vsense)<= -100m , (8.68e-6 -
+4.32e-6) , (-43e-6)*V(Vsense) )}
    E65 NET257 0 VCCN 0 1.0
    E_VOH NET261 NET200 VALUE={ VALIF(I(VreadIo)<5m , 640m , -0.031 +
+134.2*I(VreadIo) ) }
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0
    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 81k ) (3m , 60k)
+(4m , 48k) ( 5m , 40.5k ) (7m , 32k) ( 9m , 27.1k ) (12m 22.7k) ( 15m ,
+20k ) (17m 18.75k) ( 20m , 17.5k ) ( 25m , 15.7k ) ( 30m , 14.5k ) ( 35m
+, 13.7k ) ( 40m , 13.2k ) ( 50m , 12.4k ) ( 60m , 11.7k ) ( 70m , 11.35k
+) ( 80m , 11k ) ( 90m , 10.8k ) ( 100m , 10.61k ) ( 120m , 10.35k ) (
+150m , 10.15k )
    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={VALIF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET277 0 VALUE={VALIF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET277 NET282 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={VALIF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={VALIF( (V(VP)>=Vicm_LOW) & (V(VP)<=Vicm_HIGH) &
+(V(Vccp,Vccn)>=Vcc_LOW) & (V(Vccp,Vccn)<=Vcc_HIGH) , V(VP,VM) , 0)}
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET261 0 VCCP 0 1.0
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={VALIF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    EVLIM_LOW_VRG3 NET245 0 VCCN 0 1.0
```

```
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -299.5 -5000*I(VreadIo)}
    R144 VCCN_REF VRG3_6 {Rg3_C}
    R136 VCCN_REF VRG3_2 {Rg3_C}
    R142 VCCN_REF VRG3_4 {Rg3_C}
    RO2_2 NET191 VB_3 {Ro2_2}
    R143 VCCN_REF VRG3_5 {Rg3_C}
    R141 VCCN_REF VRG3_3 {Rg3_C}
    R1 VCCN_REF VRG3 {Rg3_C}
    G_ICC_VSENSE VCCP VCCN VALUE={VALIF( V(Vsense)>0 , 3.5e-5 +
+0.0015*V(Vsense) , 0 )}
    G_IIB-VP_VSENSE VP 0 VALUE={VALIF( V(Vsense)>0 , V(Vsense)/Rg1 , 0 )}
    G70 VCCN_REF VRG3_6 VRG3_5 VCCN_REF {1/Rg3_C}
    G67 VCCN_REF VRG3_3 VRG3_2 VCCN_REF {1/Rg3_C}
    G60 VM 0 VALUE={VALIF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G68 VCCN_REF VRG3_4 VRG3_3 VCCN_REF {1/Rg3_C}
    G62 VCCN_REF VRG3_2 VRG3 VCCN_REF {1/Rg3_C}
    G69 VCCN_REF VRG3_5 VRG3_4 VCCN_REF {1/Rg3_C}
    G_IOUT_SOURCED VCCP 0 VALUE={VALIF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 VCCN_REF VRG3 VALUE={VALIF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0
+)}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP VCCN 1.26e-4 3.25e-6
    G_IOUT_SINKED VCCN 0 VALUE={VALIF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.



********************************************************************************
*
* MODELS/SUBCKTS and PARAMS used by TSC101A-B-C subckt:
*

.SUBCKT OPAMP_SR VM VP VS VCCP VCCN
    M_NMOS2 VO_DIFF_MINUS VM VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    M_NMOS1 VO_DIFF_PLUS VP VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    IEE_N VEE_N VCCN_ENHANCED DC {IEE}
    VVLIM_LOW_VB NET0109 NET0110 DC {Vd_compensazione}
    VPROT_IN_P_VCCP NET0123 NET0134 DC {V_DPROT}
    V_ENHANCE_VCCN VCCN_ENHANCED VCCN DC {VCCN_enhance}
    VVLIM_HIGH_VB NET0187 NET0153 DC {Vd_compensazione}
    V_ENHANCE_VCCP VCCP_ENHANCED VCCP DC {VCCP_enhance}
    V_OUTVLIM_LOW NET0224 NET125 DC {Vd_compensazione}
    VPROT_IN_M_VCCN NET0116 NET0192 DC {V_DPROT}
    V_OUTVLIM_HIGH NET0201 NET0131 DC {Vd_compensazione}
    VPROT_IN_P_VCCN NET0115 NET096 DC {V_DPROT}
    VPROT_IN_M_VCCP NET0190 NET0135 DC {V_DPROT}
    DVLIM_HIGH_VB VB NET0187 DIODE_NOVd
    DPROT_IN_M_VCCP VM NET0135 DIODE_VLIM
    DVLIM_LOW_VB NET0110 VB DIODE_NOVd
    DPROT_IN_M_VCCN NET0116 VM DIODE_VLIM
```

```
    D_OUTVLIM_LOW NET125 VB_3 DIODE_NOVd
    DPROT_IN_P_VCCP VP NET0134 DIODE_VLIM
    DPROT_IN_P_VCCN NET0115 VP DIODE_VLIM
    D_OUTVLIM_HIGH VB_3 NET0201 DIODE_NOVd
    CCOMP VB VB_2 {Ccomp}
    EMEAS_VOUT_DIFF VOUT_DIFF 0 VO_DIFF_PLUS VO_DIFF_MINUS 1.0
    EVLIM_HIGH_VB NET0153 0 VCCP 0 1.0
    EVLIM_HIGH_VOUT NET0131 0 VCCP 0 1.0
    EVLIM_LOW_VB NET0109 0 VCCN 0 1.0
    E2_REF NET0238 0 VCCN 0 1.0
    E_VREF VREF 0 NET0250 0 1.0
    E1_REF NET0210 0 VCCP 0 1.0
    EVLIM_LOW_VOUT NET0224 0 VCCN 0 1.0
    RO2_2 VB_3 VB_2 {Ro2_2}
    RPROT_IN_P_VCCP NET0123 VCCP 100
    RPROT_IN_M_VCCP VCCP NET0190 100
    RO1 VS VB_3 {Ro1}
    RD1 VCCP_ENHANCED VO_DIFF_PLUS {RD}
    RD2 VCCP_ENHANCED VO_DIFF_MINUS {RD}
    RO2_1 VREF VB_2 {Ro2_1}
    R1_REF NET0210 NET0250 1Meg
    R1 VB VREF {R1}
    RPROT_IN_M_VCCN VCCN NET0192 15K
    R2_REF NET0250 NET0238 1Meg
    RPROT_IN_P_VCCN NET096 VCCN 15K
    G_I_VB VB_2 VREF VB VREF {GB}
    GM1 VREF VB VOUT_DIFF 0 {1/RD}
.ENDS
*** End of subcircuit definition.


.PARAM Vicm_LOW  = 2.8
.PARAM Vicm_HIGH = 30
.PARAM Vcc_LOW  = 4
.PARAM Vcc_HIGH = 24
.PARAM Iib = 5.5e-6
.PARAM Rg1 = 5k
.PARAM Av_A  = 20
.PARAM Av_B  = 50
.PARAM Av_C  = 100
.PARAM Rg3_A = {Av_A*Rg1}
.PARAM Rg3_B = {Av_B*Rg1}
.PARAM Rg3_C = {Av_C*Rg1}
.PARAM Ro_sink = 1m
.PARAM Ro_source = 3
.PARAM Ro_off = 0.82
.PARAM alpha_switch_Ro = 1e4
.PARAM CBW_A = 1.08p
.PARAM CBW_B = 0.32p
.PARAM CBW_C = 0.243p
.PARAM RD=1k
```

```
.PARAM VCCP_enhance=-100m
.PARAM VCCN_enhance=-700m
.PARAM Ccomp=11p
.PARAM IEE=10u
.PARAM A0=97.93103448E3
.PARAM Ro=17587.2
.PARAM W=11u
.PARAM L=1u
.PARAM gm_mos=0.0002348021861505248
.PARAM GB=10m
.PARAM Ro1=1
.PARAM Ro2_2=1e-3
.PARAM Ro2_1={Ro - Ro2_2 - Ro1}
.PARAM R1={A0/(gm_mos*GB*Ro2_1)}
.PARAM V_DPROT=0.6
.PARAM Vd_compensazione=-245.4u

.MODEL MOS_N  NMOS LEVEL=1 MODTYPE=ELDO VTO=+0.65  KP=500E-6
.MODEL DIODE_NOVd D LEVEL=1 MODTYPE=ELDO IS=10E-15 N=0.001
.MODEL DIODE_VLIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
.MODEL DIODE_ILIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
.MODEL DX D LEVEL=1 MODTYPE=ELDO IS=1E-14
*
*********************************************************************************
```

4 Macromodel behavior: DC simulations

The macromodel matches the real TSC101 DC behavior: the following sections explain how the macromodel fits each DC specification.

4.1 Transfer function: output voltage vs. Vsense

Fig. 4 shows the circuit used to simulate the transfer function, output voltage vs. Vsense:

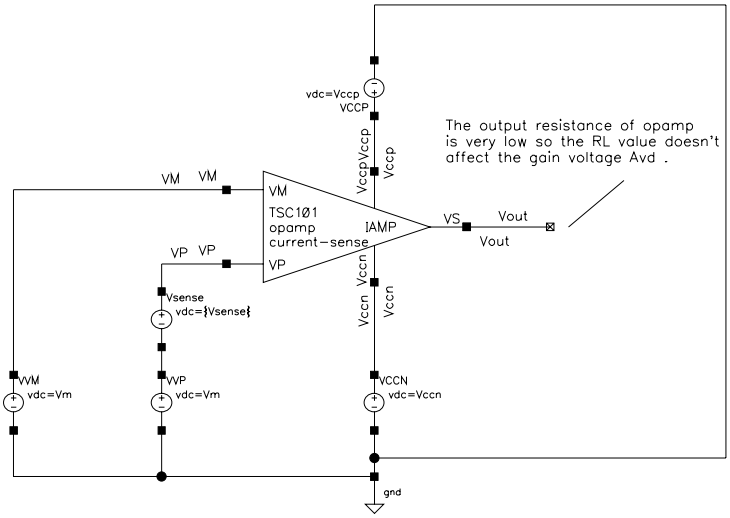

Figure 4: Transfer function, output voltage vs. Vsense: simulation schematic.

The macromodel Avd (Large signal voltage gain) follows in table 1, simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc, Vccn=0, Vm=12V, Vcc=12V, no load on out.

Device	Macromodel	Datasheet (Typ.)
TSC101A	20 V/V	20 V/V
TSC101B	50 V/V	50 V/V
TSC101C	100 V/V	100 V/V

Table 1: Avd (Large signal voltage gain): macromodel simulations vs datasheet .

Fig. 5 shows the entire Vout vs. Vsense curves simulation considering each TSC101A/B/C macromodel compared with its measure.

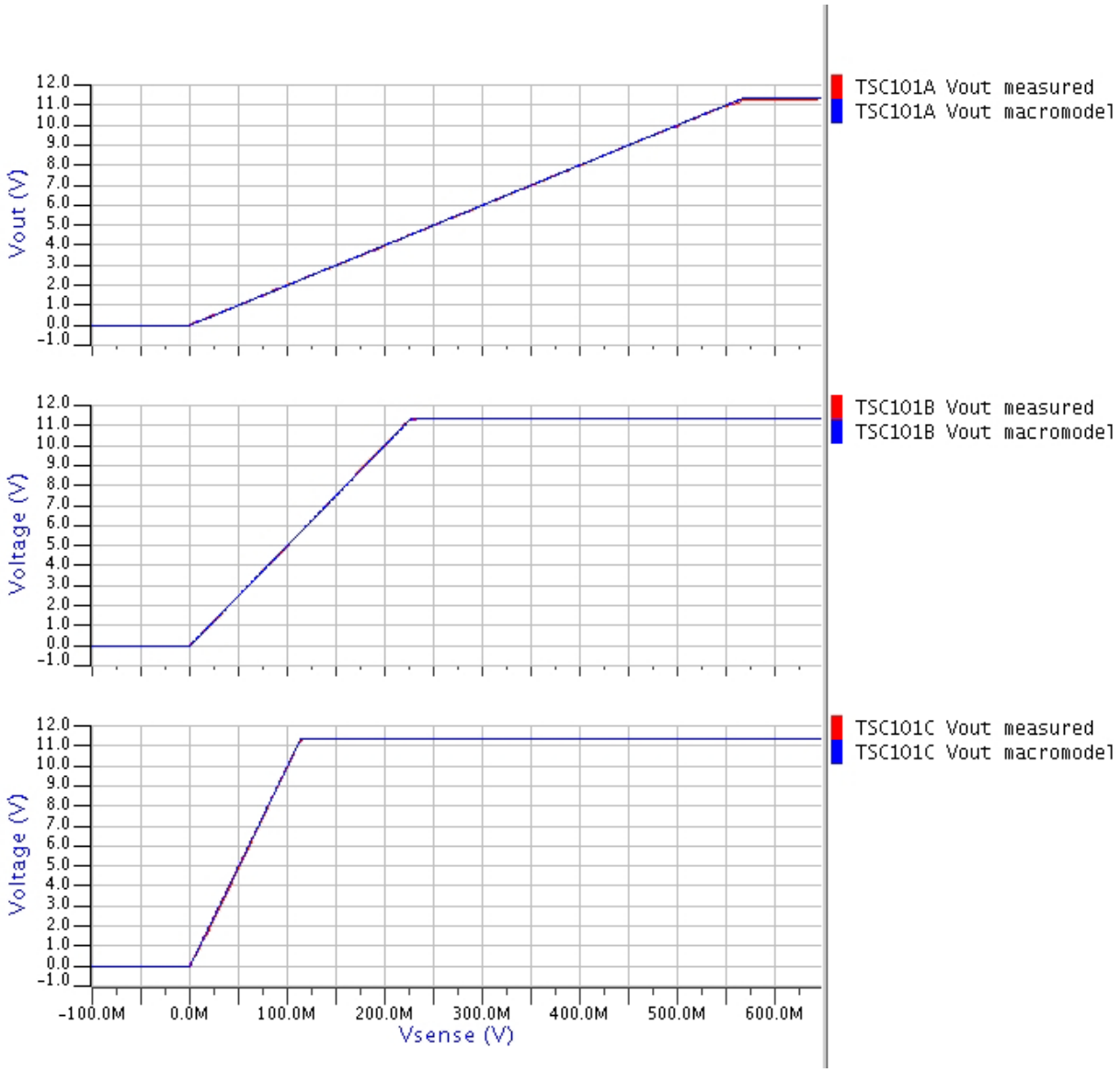

Figure 5: Output voltage (Vout) vs. Vsense: macromodel simulation result vs. measure.

Fig. 6 shows, for low Vsense values (<20mV), the Vout vs. Vsense curves simulation considering each TSC101A/B/C macromodel.

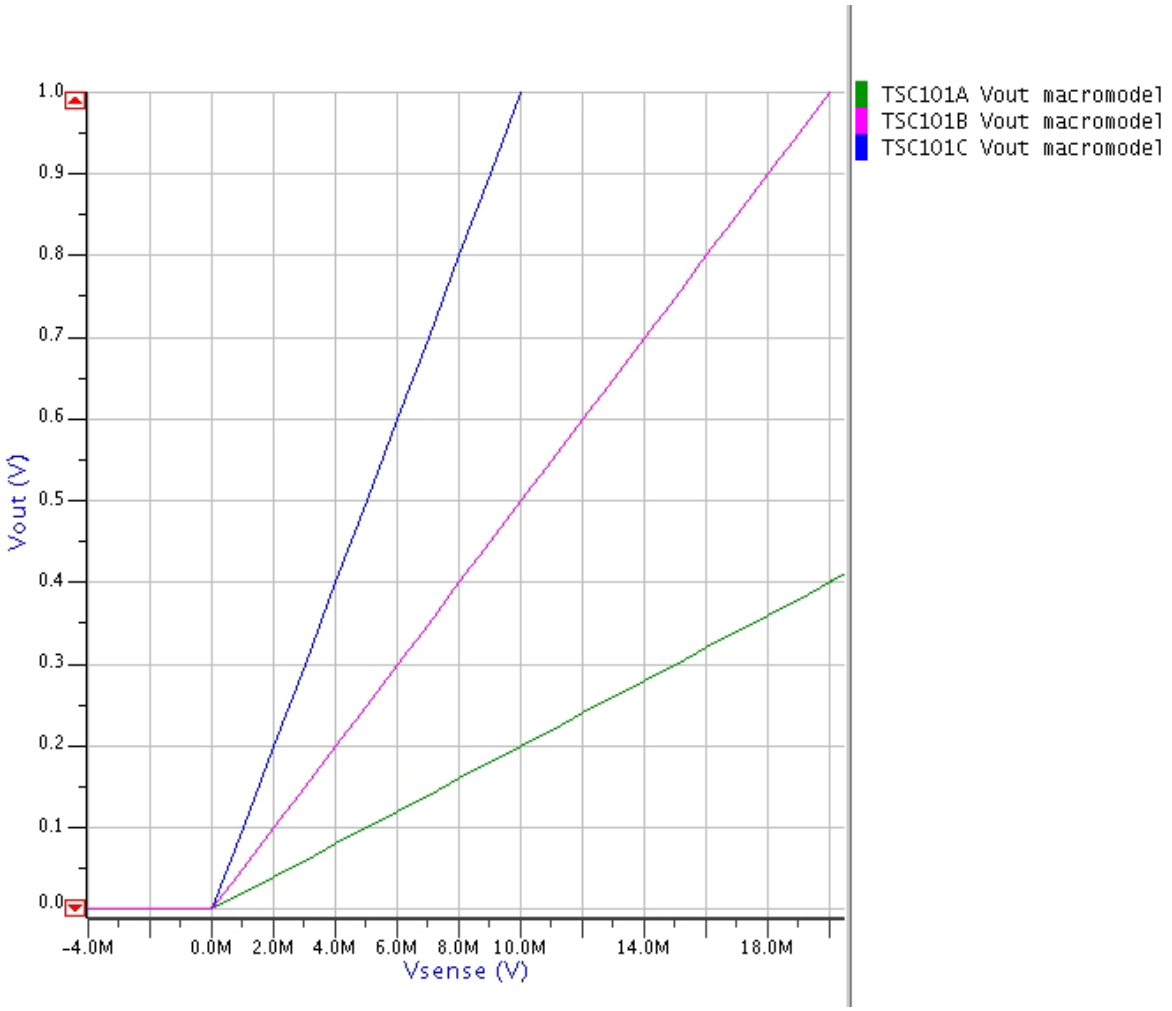

Figure 6: Output voltage (Vout) versus Vsense for low Vsense: macromodel simulation result vs. measure.

4.2 Common mode input voltage (Vicm)

The TSC101A-B-C macromodels match the real behavior regarding the input common-mode explained in sec. 2, so the macromodels have a wide input common-mode range $\in$ [2.8V,30V] that is independent of supply voltage Vcc $\in$ [4V,24V].

4.3 Consumption supply current (Icc) and input bias current (Iib)

Fig. 7 shows the circuit used to simulate it.

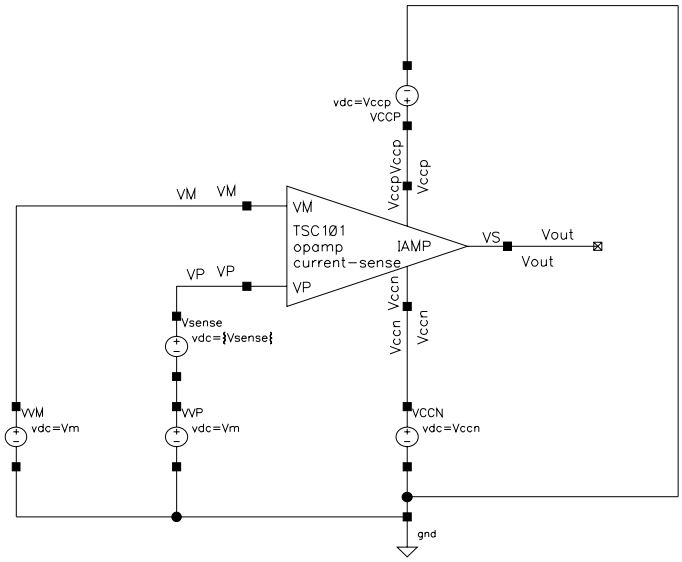

Figure 7: Consumption current (Icc): simulation schematic.

Fig. 8 shows the macromodel Icc (consumption supply current) simulation compared with the measured one shown in datasheet, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc, Vccn=0, Vm=12V, **fixing Vsense=Vp-Vm=0V and varying Vcc in** $[4V, 24V]$.

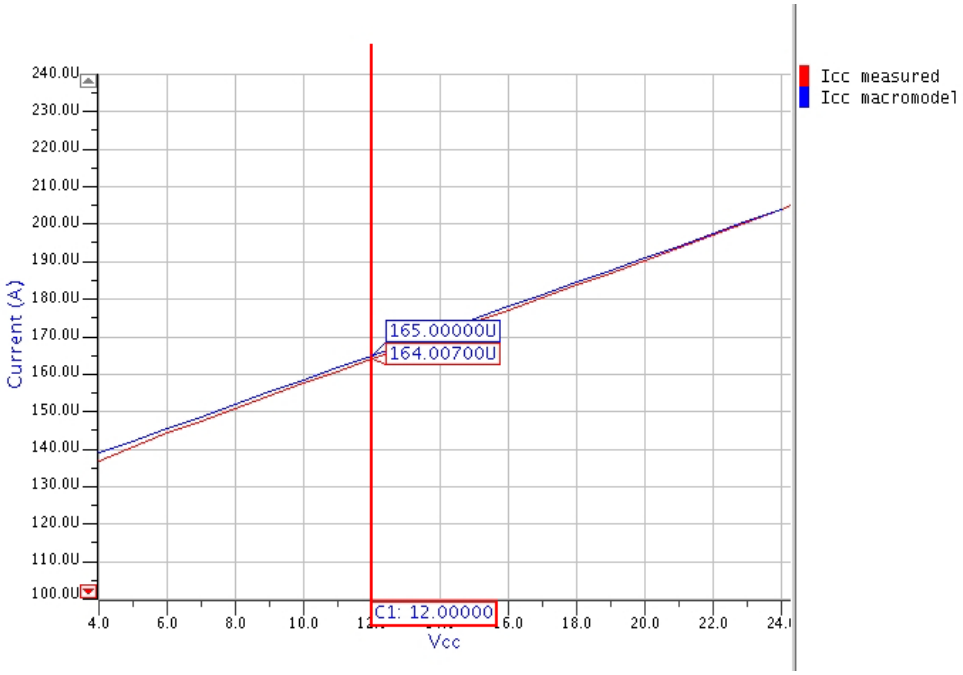

Figure 8: Supply current (Icc) vs. supply voltage (Vcc) (@ Vsense=0V): macromodel simulation result vs. measure.

The macromodel fits well the measured Icc over the full Vcc range $[4V, 24V]$: the tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

Fig. 9 shows the macromodel Icc (consumption supply current) simulation compared with the measured one shown in datasheet, considering the following test conditions: T_{amb} = 25^oC, Vccp=Vcc=12V, Vccn=0, Vm=12V and **varying Vsense=(Vp-Vm) in** $[-120mV, +120mV]$.

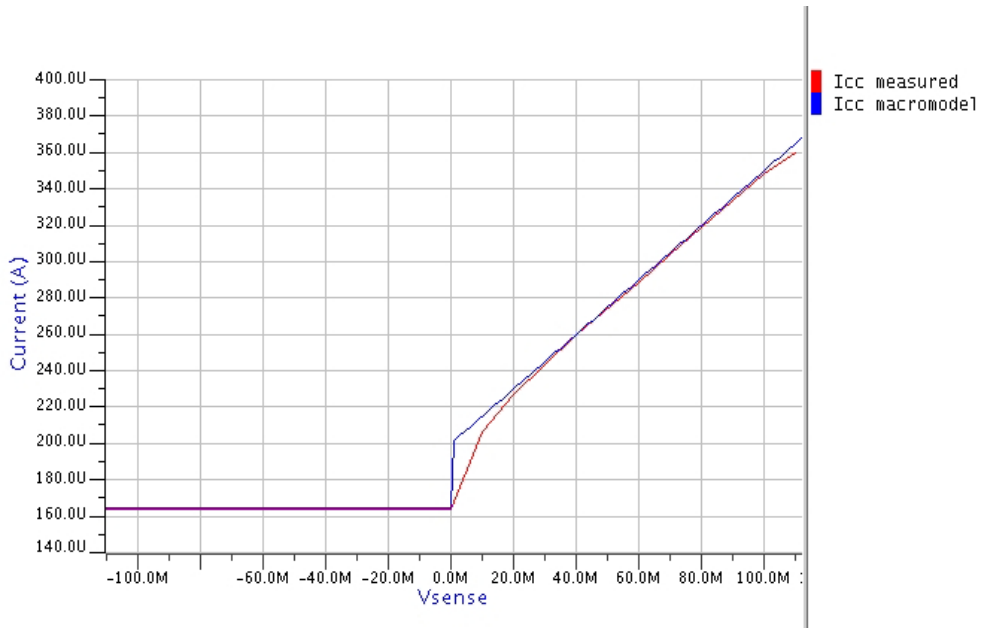

Figure 9: Supply current (Icc) vs. Vsense: macromodel simulation result vs. measure.

The macromodel fits well the measured Icc, varying Vsense: the tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

Fig. 10 shows the macromodel Vp pin input bias current simulation compared with the measured one shown in datasheet, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V and **varying Vsense=(Vp-Vm) in** $[-120mV, +120mV]$.

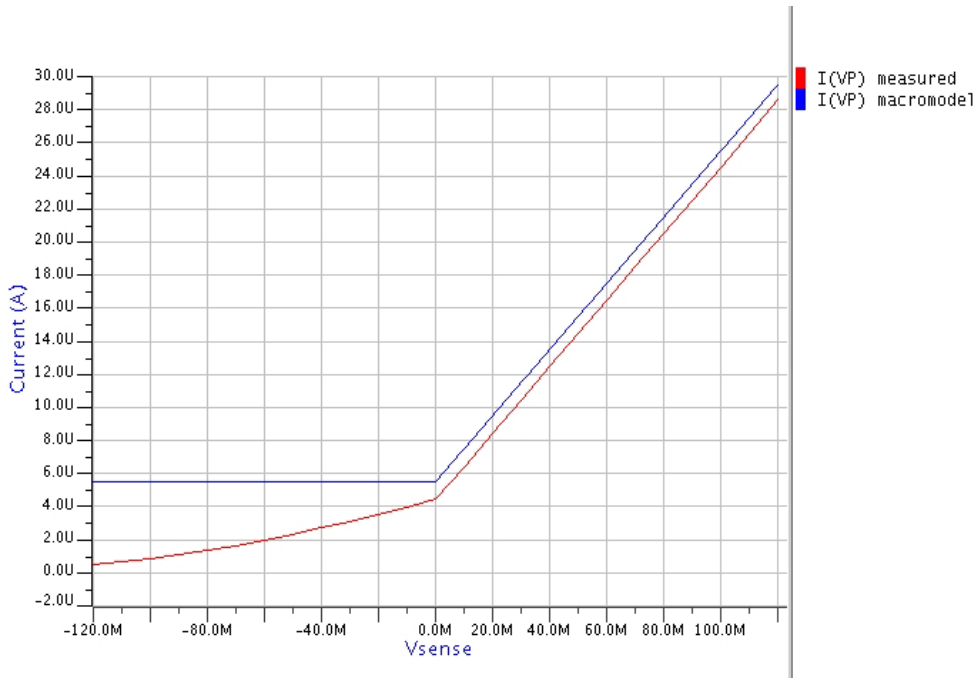

Figure 10: Vp pin input bias current vs. Vsense: macromodel simulation result vs. measure.

The macromodel fits well the measured Vp pin input bias, varying Vsense: the tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

Fig. 11 shows the macromodel Vm pin input bias current simulation compared with the measured one shown in datasheet, considering the following test conditions: T_{amb} = 25^oC, Vccp=Vcc=12V, Vccn=0, Vm=12V and **varying Vsense=(Vp-Vm) in** $[-120mV, +120mV]$.

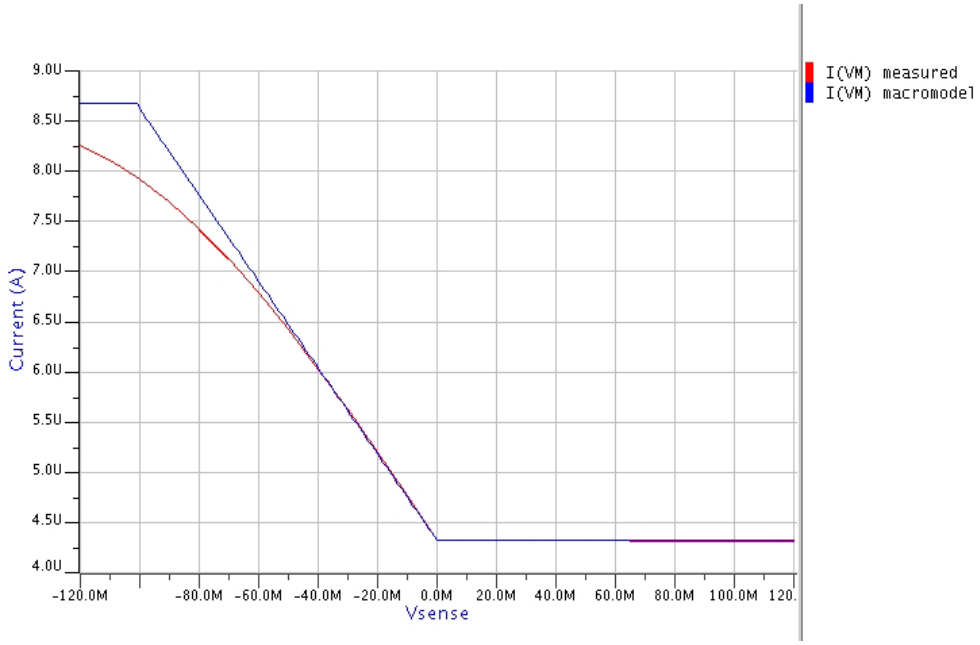

Figure 11: Vm pin input bias current vs. Vsense: macromodel simulation result vs. measure.

The macromodel fits well the measured Vm pin input bias, varying Vsense: the tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

4.4 Low level output voltage (Vol)

Fig. 12 shows the circuit used to simulate it.

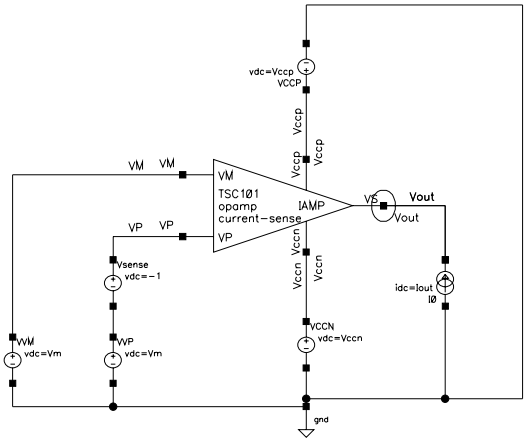

Figure 12: Vol (Low level output voltage): simulation schematic.

Fig. 13 shows the macromodel output stage low-state saturation voltage (Vol) simulation compared with the measured one shown in datasheet, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V, Vsense=(Vp-Vm)=-1V and **varying Iout in** $[-10mV, +10mV]$.

The macromodel fits well the measured Vol vs. Iout: the tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

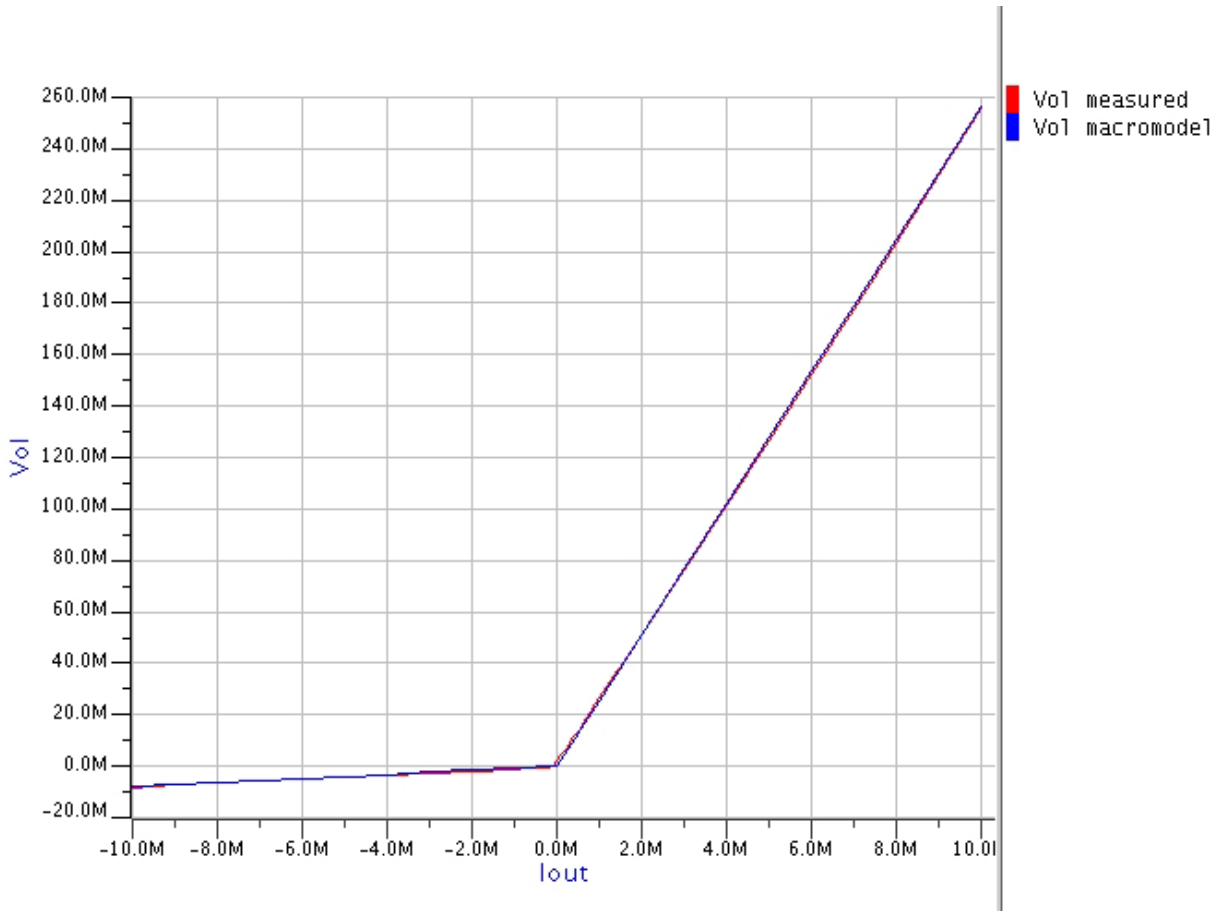

Figure 13: Vol vs. Iout: macromodel simulation result vs. measure.

4.5 High level output voltage (Voh)

Fig. 14 shows the circuit used to simulate it.

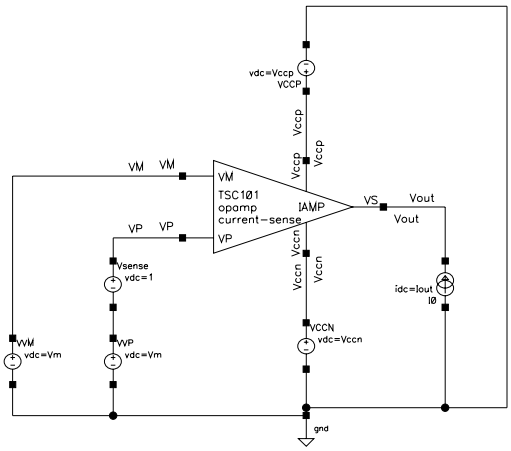

Figure 14: Voh (High level output voltage): simulation schematic.

Fig. 15 shows the macromodel output stage high-state saturation voltage (Voh) simulation compared with the measured one shown in datasheet, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V, Vsense=(Vp-Vm)=+1V and **varying Iout in** $[-10mV, +10mV]$.

The macromodel fits well the measured Voh vs. Iout: the tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

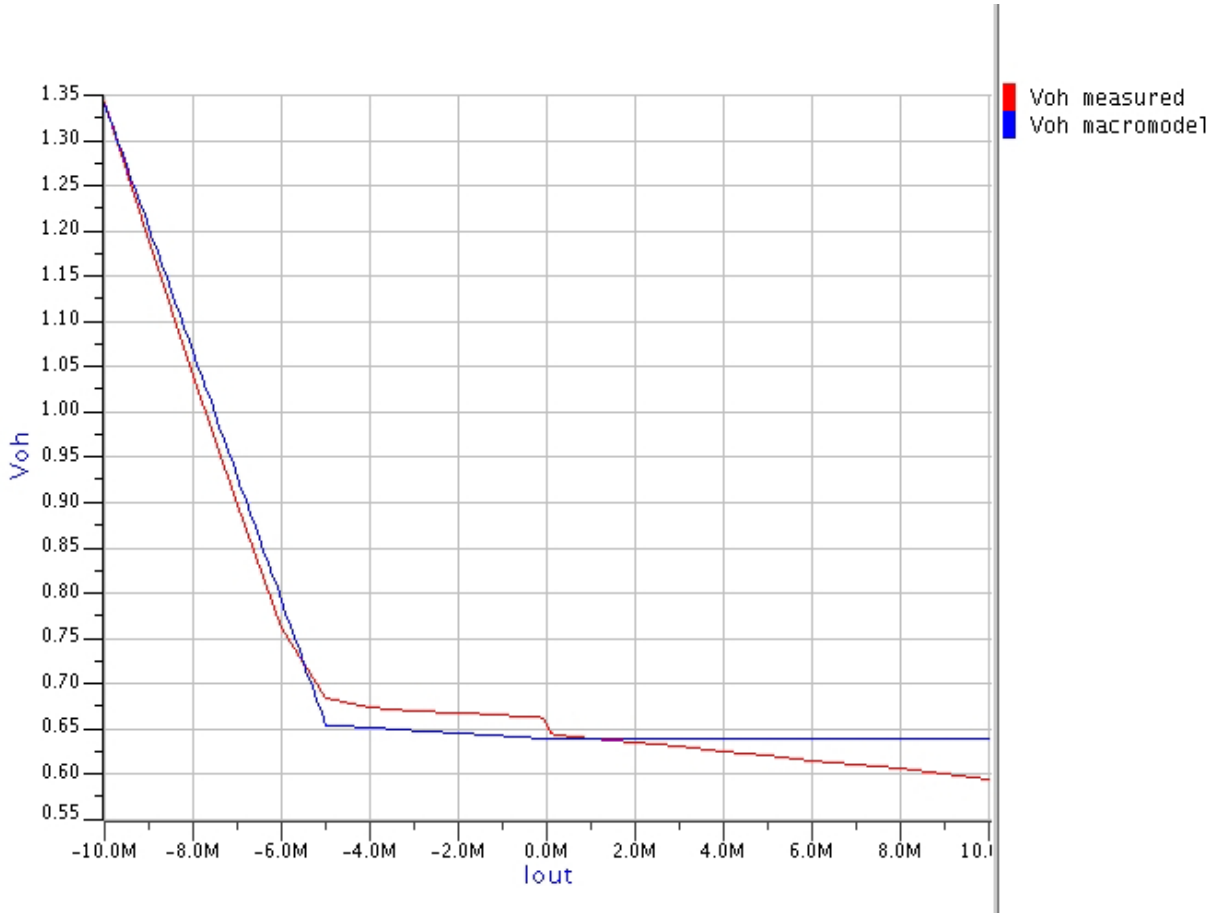

Figure 15: Voh vs. Iout: macromodel simulation result vs. measure.

4.6 Isource short-circuit current

Fig. 16 shows the circuit used to simulate it.

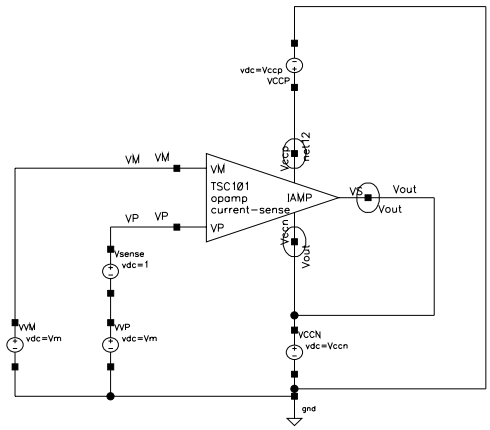

Figure 16: Isource short-circuit current: simulation schematic.

Follows the macromodel max source current simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V, Vsense=(Vp-Vm)=+1V and out connected to gnd:

Macromodel	Datasheet (Typ.)
26.09 mA	26 mA

Table 2: Isource (Max source current): macromodel simulations vs datasheet.

Fig. 17 shows I(Vout), I(Vccp) and I(Vccn) varying Vcc in $[4V, 24V]$.

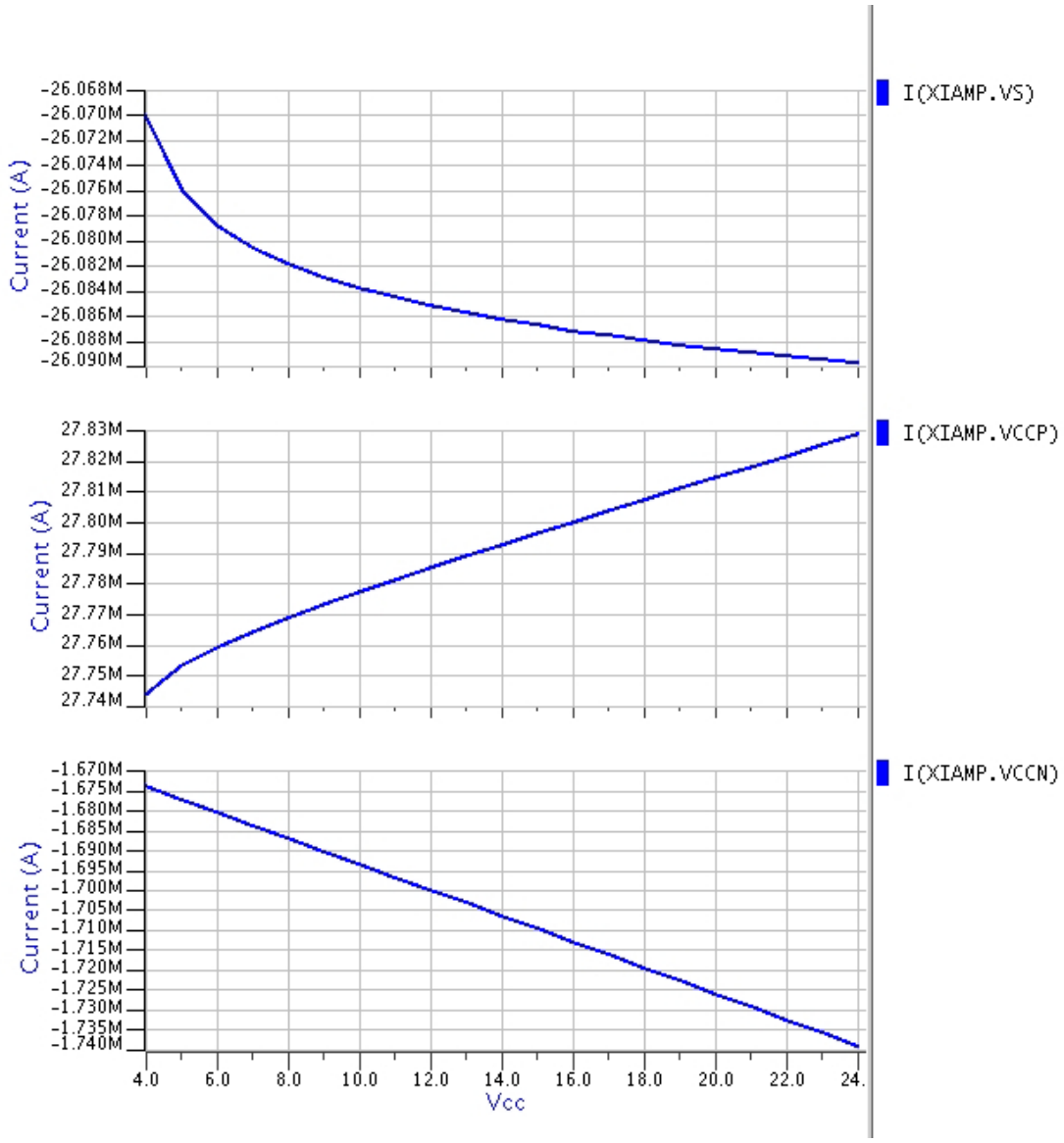

Figure 17: Isource short-circuit current: simulation results.

4.7 Isink short-circuit current

Fig. 18 shows the circuit used to simulate it.

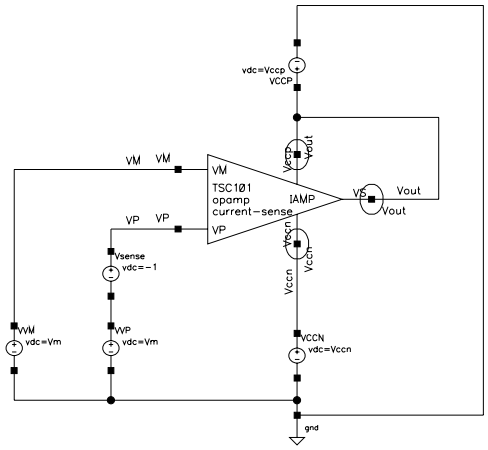

Figure 18: Isink short-circuit current: simulation schematic.

Follows the macromodel max sink current simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V, Vsense=(Vp-Vm)=-1V and out connected to Vcc:

Macromodel	Datasheet (Typ.)
60.09 mA	60 mA

Table 3: Isink (Max sink current): macromodel simulations vs datasheet.

Fig. 19 shows I(Vout), I(Vccp) and I(Vccn) varying Vcc in $[4V, 24V]$.

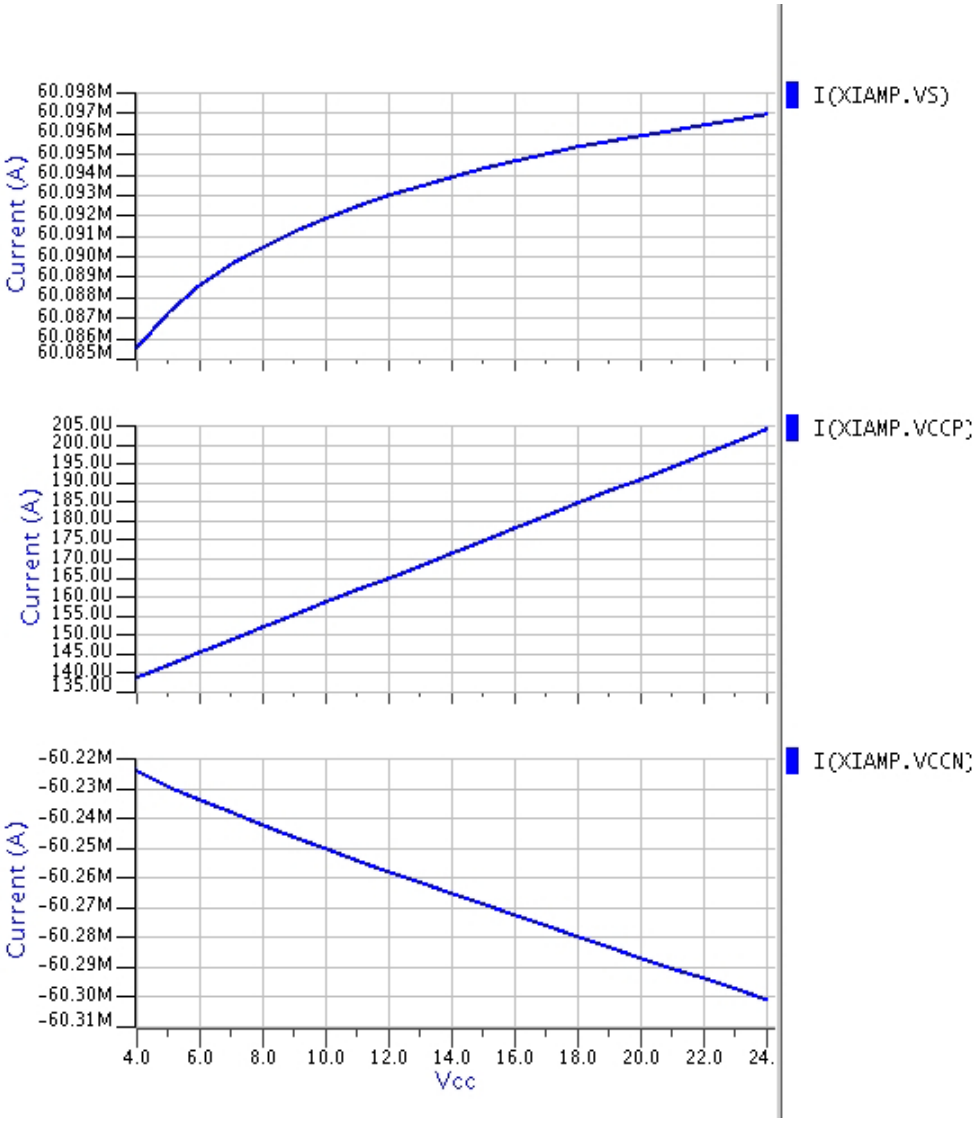

Figure 19: Isink short-circuit current: simulation results.

4.8 Output stage load regulation ($R_{out} = \Delta V_{out}/\Delta I_{out}$)

Fig. 20 shows the circuit used to simulate it.

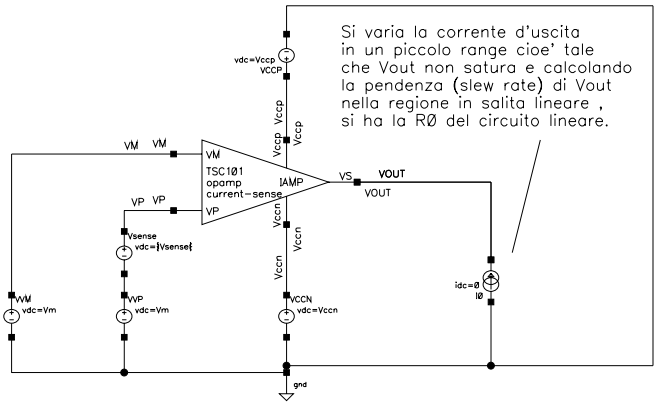

Figure 20: Output stage load regulation: simulation schematic.

Fig. 21 shows the macromodel output stage load regulation (Vout-Vout0 vs. Iout , Vout0 is Vout @ Iout=0) simulation compared with the measured one shown in datasheet, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V, Vsense=(Vp-Vm)=50mV and **varying Iout in** $[-10mV, +10mV]$

The macromodel fits well the measured $\Delta V_{out}/\Delta I_{out}$: as shown in fig. 22, the macromodel has a $R_{out} = \Delta V_{out}/\Delta I_{out} \simeq 3$ for output stage source current and a very low $R_{out} = \Delta V_{out}/\Delta I_{out} \simeq 0.002$ for output stage sink current.

The tested device is TSC101-C but this result is valid for TSC101-A TSC101-B too.

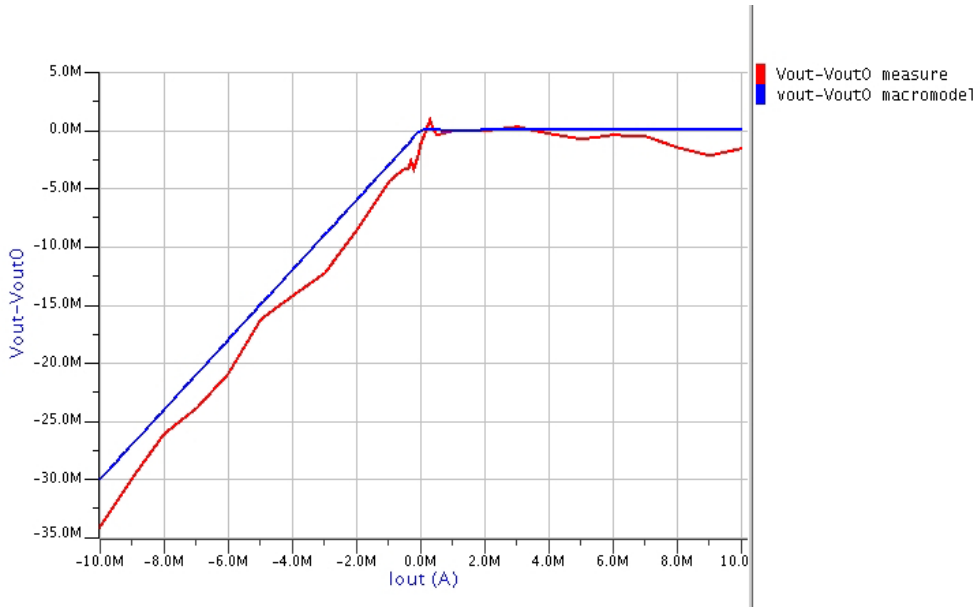

Figure 21: Output stage load regulation: macromodel simulation result vs. measure.

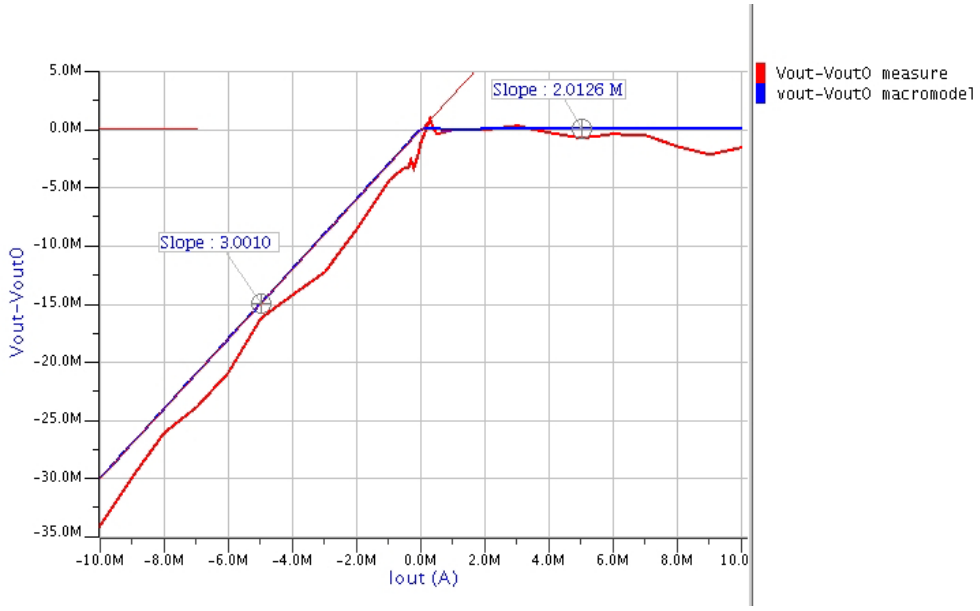

Figure 22: Output stage load regulation: slopes.

5 Macromodel behavior: TRANSIENT simulations

The macromodel matches the real TSC101 transient behavior: the following sections explain how the macromodel fits each transient specification.

5.1 Slew rate

Fig. 23 shows the circuit used to simulate it.

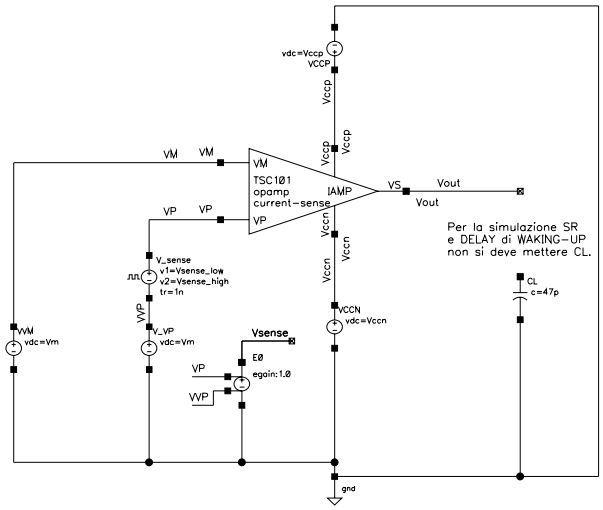

Figure 23: Slew rate: simulation schematic.

Table 4 shows the TSC101A-B-C macromodels slew rate simulated in the same datasheet test conditions: T_{amb} = 25^oC, Vccp=Vcc=12V, Vccn=0, Vm=12V and with an input step starting from Vsense_low=10mV to Vsense_high=100mV.

Fig. 24 shows the entire step response for TSC101A-B-C macromodels.

The TSC101A-B-C macromodels match well the datasheet slew rate specification .

Device	Macromodel	Datasheet (Typ.)
TSC101A	$0.905V/\mu s$	$0.9V/\mu s$
TSC101B	$0.904V/\mu s$	$0.9V/\mu s$
TSC101C	$0.904V/\mu s$	$0.9V/\mu s$

Table 4: Slew rate: macromodel simulations vs datasheet.

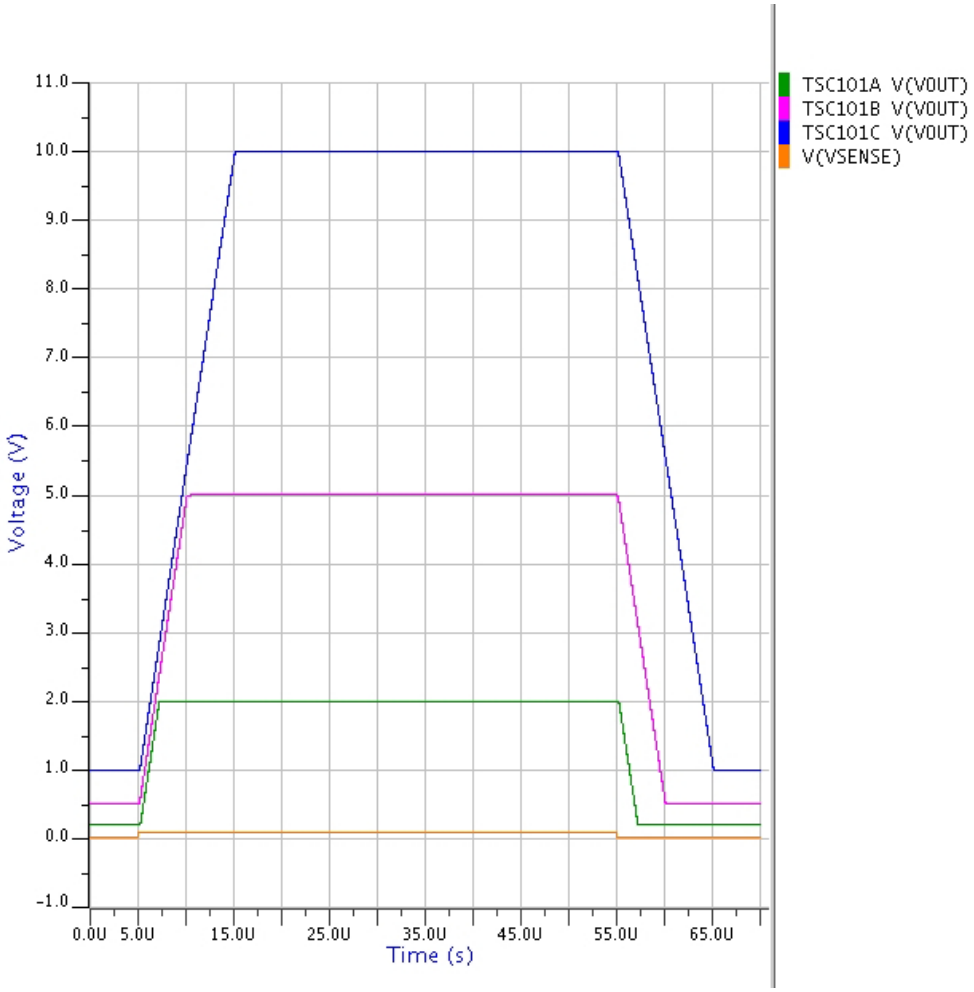

Figure 24: Sler rate: simulation results.

5.2 Waking-up effect

In the previous section 5.1 the TSC101A-B-C output voltage isn't delayed respect the input step stimulus starting from Vsense_low=10mV to Vsense_high=100mV.

If this input step signal starts from a Vsense_low > 0 then the output voltage doesn't show any delay therefore the device is immediately ready to respond to the input step signal: instead if this input step signal starts from a Vsense_low < 0 then the output voltage is delayed respect it; this effect is called waking-up.

The waking-up delay depend of the input overdrive voltage (Vsense_high value): the delay decreases increasing the input overdrive voltage.

Considering the TSC101C device, the schematic shown in fig. 23 was simulated in the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V and with an input step starting from **Vsense_low= -1mV** to **Vsense_high** $\in$ **[2mV , 160mV]**.

Fig.25 shows the entire TSC101C macromodel output voltage response varying **Vsense_high** $\in$ **[2mV , 160mV]**.

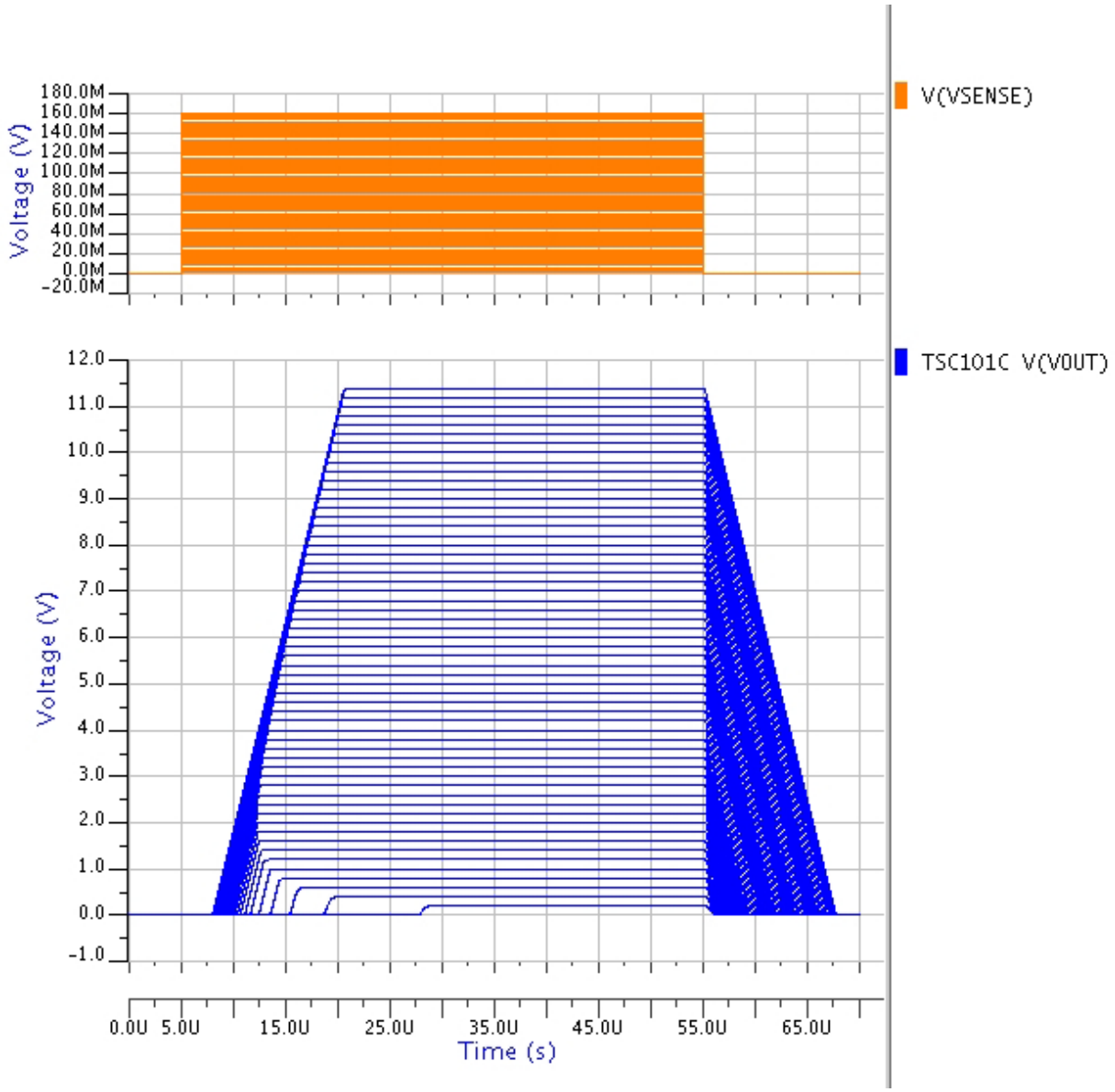

Figure 25: Waking-up, entire step response: simulation results.

Fig.26 shows the TSC101C macromodel delay compared with that extracted simulating the real TSC101C designer netlist.

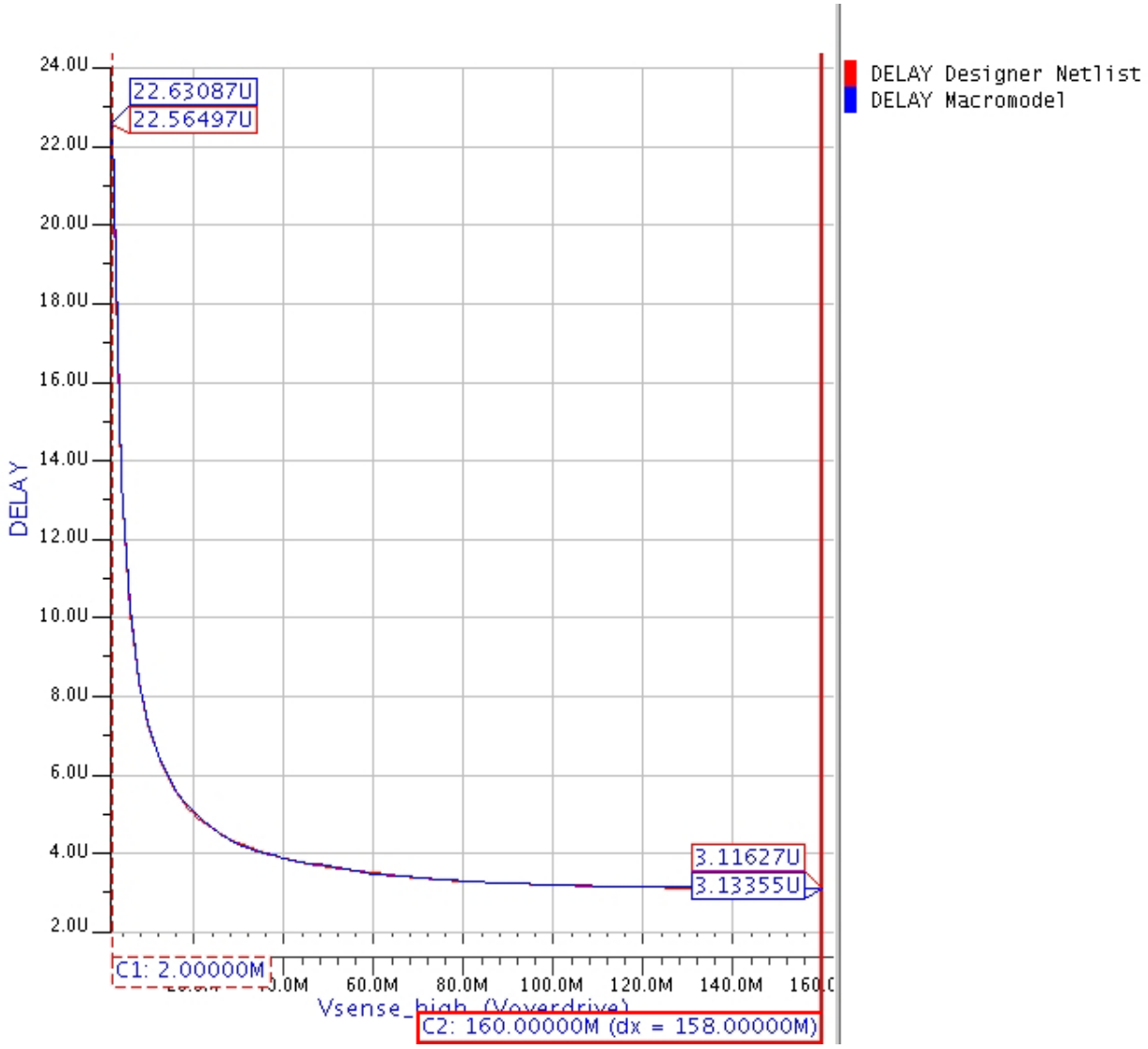

Figure 26: Waking-up, delay: TSC101C macromodel simulation vs designer netlist simulation.

This result is valid for TSC101-A TSC101-B too, as shown in fig. 27 that compares the TSC101A-B-C delay.

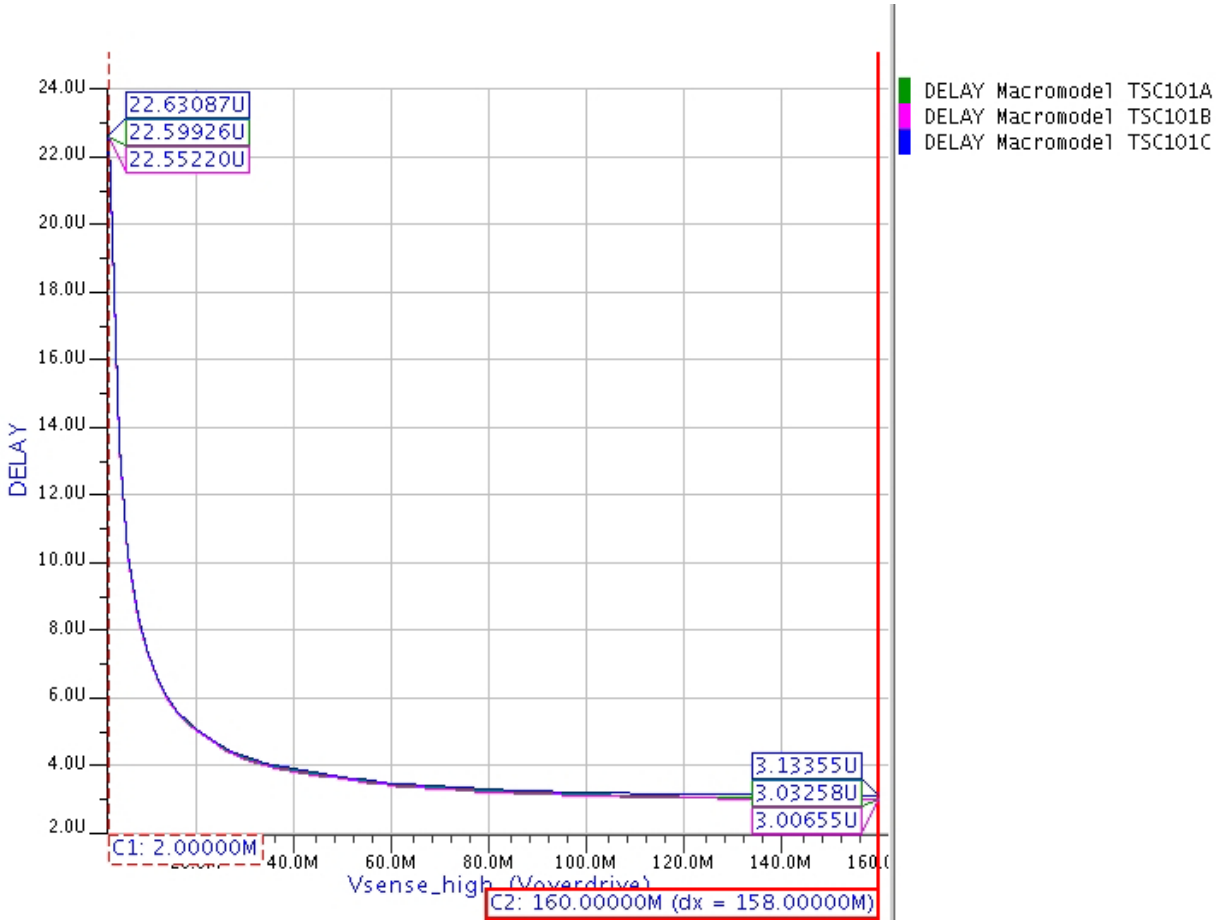

Figure 27: Waking-up, delay: TSC101A-B-C macromodel simulation.

6 Macromodel behavior: AC simulations

The macromodel matches the real TSC101 AC behavior: the following sections explain how the macromodel fits each AC specification.

6.1 AC open-loop response

Fig. 28 shows the circuit used to simulate the open-loop AC response:

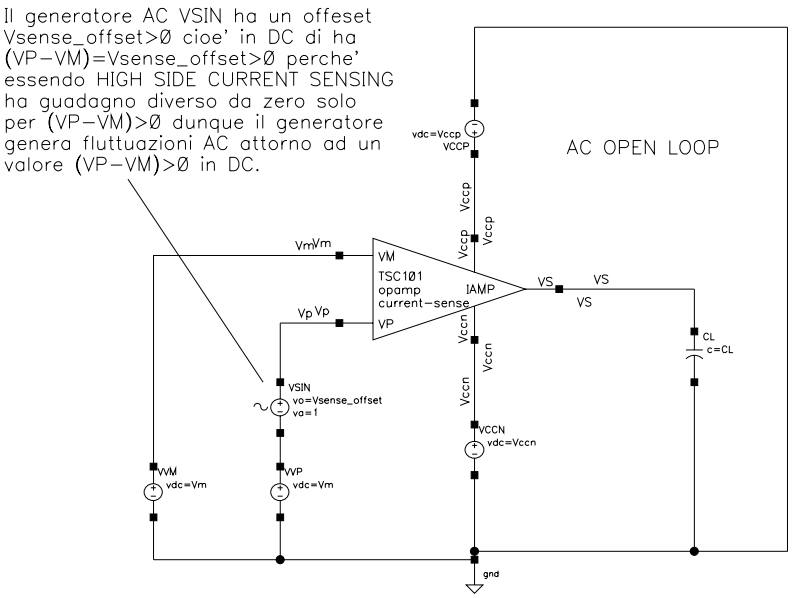

Figure 28: AC response in open-loop: simulation schematic.

Table 5 shows the TSC101A-B-C macromodels 3dB bandwidth simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=12V, Vccn=0, Vm=12V , $Vsense_{dc}$=100mV, Cload=47pF.

Device	Macromodel	Datasheet (Typ.)
TSC101A	506	500
TSC101B	674	670
TSC101C	451	450

Table 5: BW_{3dB} (kHz): macromodel simulations vs datasheet.

In the same test conditions the following figures compare the TSC101A-B-C macromodel Bode plot with the measured one.

Fig. 29 shows the entire TSC101A ac open loop response (mag and phase) compared with the measured one.

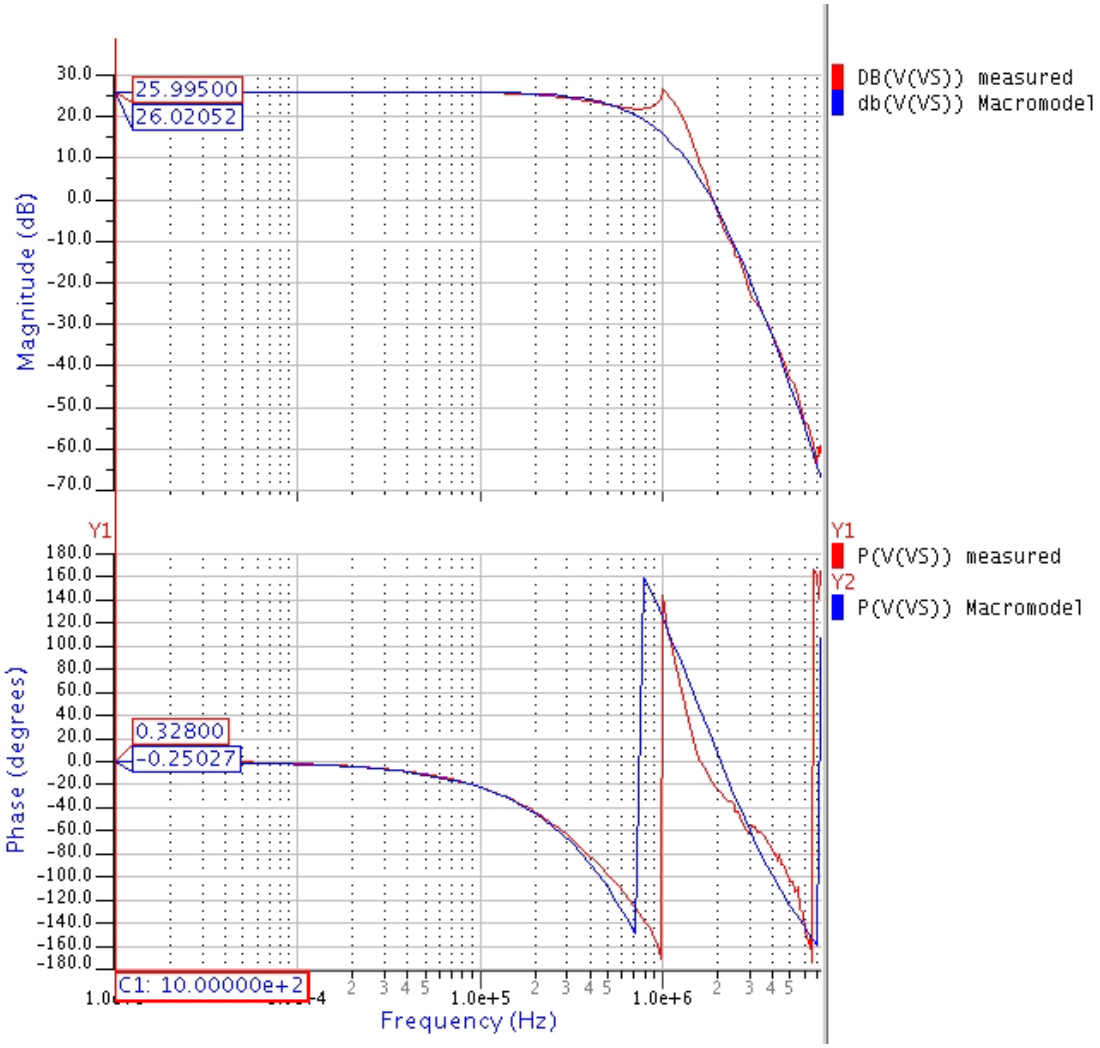

Figure 29: AC open loop response: TSC101A macromodel simulation result vs. TSC101A measure.

Fig. 30 shows the entire TSC101B ac open loop response (mag and phase) compared with the measured one.

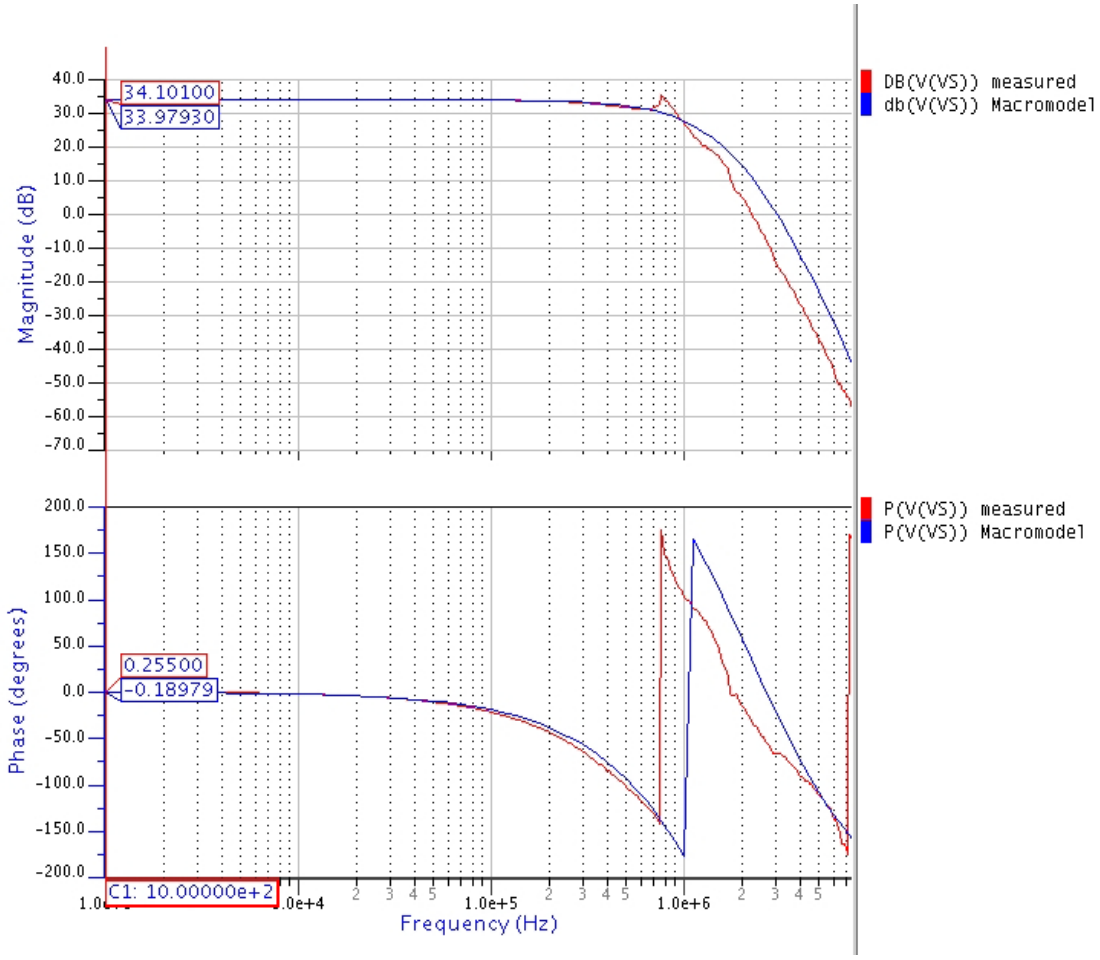

Figure 30: AC open loop response: TSC101B macromodel simulation result vs. TSC101B measure.

Fig. 31 shows the entire TSC101C ac open loop response (mag and phase) compared with the measured one.

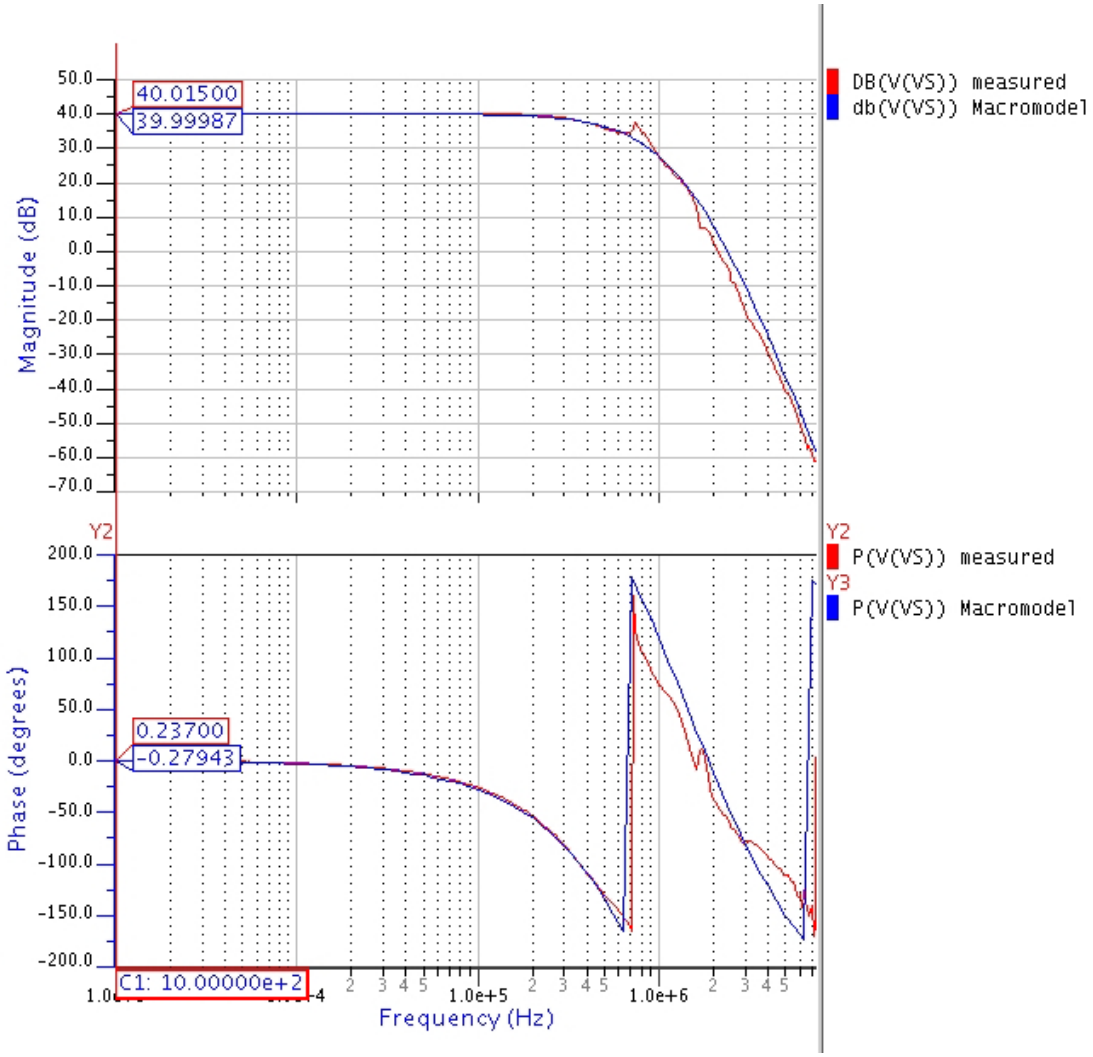

Figure 31: AC open loop response: TSC101C macromodel simulation result vs. TSC101C measure.

7 Conclusion

Analog macromodels, for Spice-like simulators, were implemented for TSC101/A/B/C high side current sense amplifiers matching the measured DC, Transient and AC behavior specifications: the macromodels guarantees the real design IP encryption and, containing a smaller number of non linear devices, allows faster simulations.

As shown in the previous sections, the implemented macromodels has a **good fitness** of the given DC, Transient and AC specifications datasheet and of the laboratory measures.

List of Figures

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