# Analog Macromodel for TSC1031 high-voltage high side current sense amplifier

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May 2009

**Abstract**

An analog macromodel, for Spice-like simulators, was implemented for the TSC1031, high-voltage high side current sense amplifier, matching the datasheet DC, Transient and AC behaviour specifications. After a brief introduction to the macromodeling paradigm the simulation results of the implemented macromodel are introduced.

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# 1 Macromodeling paradigm

***Macromodeling of IC is useful for two reason.***

***The first reason*** is reduced computational complexity: a full integrated circuit simulation in SPICE could take hours and even days, which is unacceptably slow; the circuit simulation time is proportional to the number of non-linear devices, transistors and diodes, in the circuit and since a large IC could have hundreds and thousands of transistors, there needed to be a way to simulate faster. Verifying a complete analog system via transistor-level simulation is an extremely difficult process and can often become infeasible due to the limitation of simulation capacity. A similar difficulty is encountered when high-level design analysis is performed for the whole system. For these reasons, compact macromodels of analog blocks are desired which can be substituted in place of the real transistor-level netlist to speedup the simulation *with sufficiently high accuracy*.

***The second reason*** for macromodeling is the preservation of proprietary information, Intellectual Property Encryption (IPE): a macromodel *describes the observable behaviour but not necessarily the implementation of a device*. Often transistor-level schematics for integrated circuits are not released to the customer therefore, if a customer wants to simulate a given device for evaluation, there is no way for them to know for sure exactly what there is in the circuit; however, the customer can often get a macromodel that replies the device behaviour and, *with a good understanding of the model limitations*, can use it for simulation of the device.

# 2 TSC1031 real features

The TSC1031 measures a small differential voltage on a high-side shunt resistor and translates it into a ground-referenced output voltage. The gain is adjustable to 50V/V or 100V/V by a selection pin. Wide input common-mode voltage range, low quiescent current enable use in a wide variety of applications.

Input common-mode and power supply voltages are independent. Common-mode voltage can range from 2.9V to 75V in the single-supply configuration or be offset by an adjustable voltage supplied on Vcc- pin in dual-supply configuration.

The real TSC1031 device schematic is shown in fig. 1

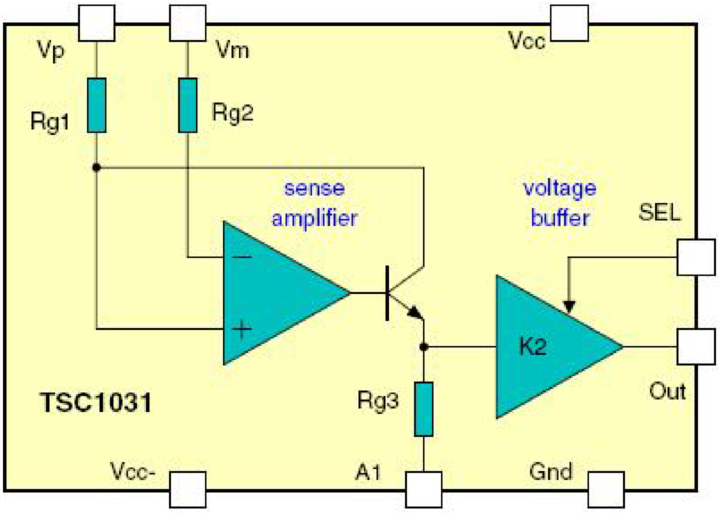


Figure 1: TSC1031 real device schematic.

| Symbol | Function |
|---|---|
| Out | The out voltage is proportional to the magnitude of the sense voltage Vp-Vm. |
| Gnd | Ground line |
| Vcc (Vccp) | Positive power supply line |
| Vcc- (Vccn) | Negative power supply line |
| Vp | Connection for the external sense resistor<br>The measured current enters the shunt on the Vp side |
| Vm | Connection for the external sense resistor<br>The measured current exits the shunt on the Vm side |
| SEL | Gain-select pin |
| A1 | Connection to the output resistor |

Table 1: Pin description.

# 3 TSC1031 macromodel

The TSC1031 macromodel schematic is shown in fig. 2.

(Schematic notes are only for author's convenience).

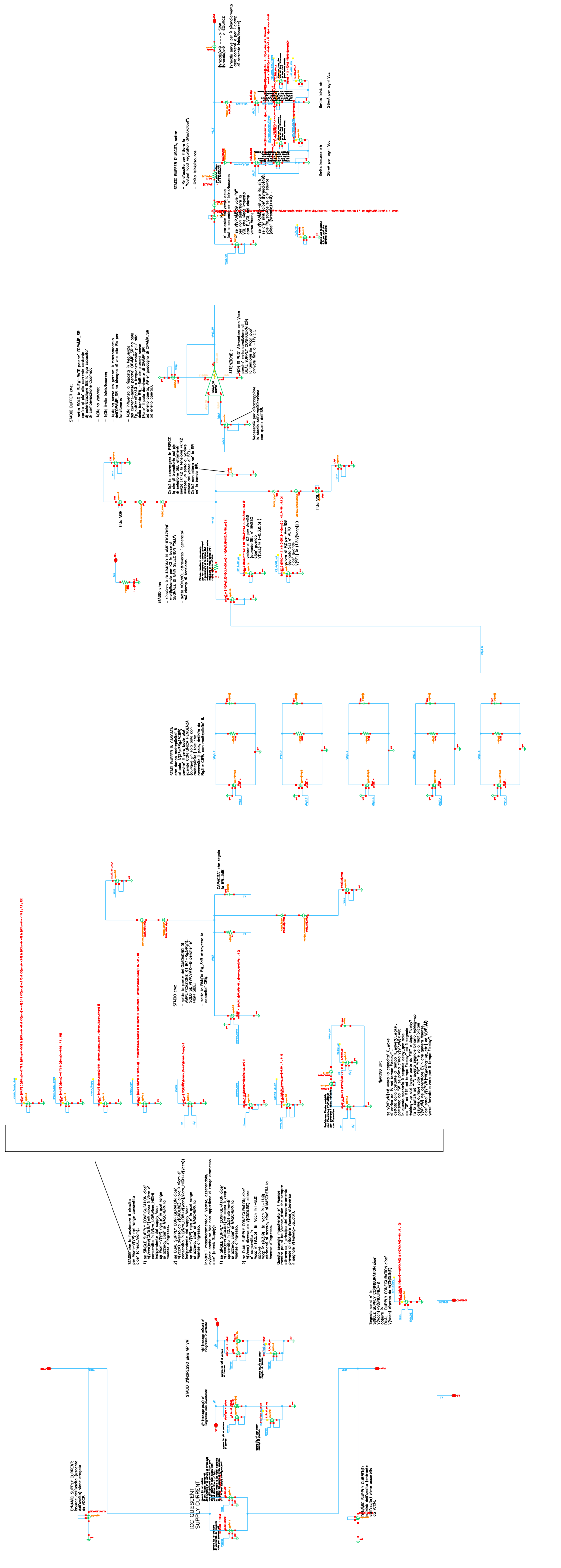

Figure 2: TSC1031 Macromodel schematic.

## 3.1 TSC1031 macromodel Library netlist for Spice simulators

The macromodel netlist in Spice compatible syntax (tested with Cadence Orcad PSpice v16.0 and Linear Technology LTSpice v2.25c) follows:

```
****************************************************************************
*
* WARNING : please consider following remarks before usage
*
* 1) All models are a tradeoff between accuracy and complexity (ie. simulation
*    time).
*
* 2) Macromodels are not a substitute to breadboarding, they rather confirm the
*    validity of a design approach and help to select surrounding component values.
*
* 3) A macromodel emulates the NOMINAL performance of a TYPICAL device within
*    SPECIFIED OPERATING CONDITIONS (ie. temperature, supply voltage, etc.).
*    Thus the macromodel is often not as exhaustive as the datasheet, its goal
*    is to illustrate the main parameters of the product.
*
* 4) Data issued from macromodels used outside of its specified conditions
*    (Vcc, Temperature, etc) or even worse: outside of the device operating
*    conditions (Vcc, Vicm, etc) are not reliable in any way.
*
****************************************************************************
****
***  TSC1031  Spice macromodel subckt
***  May 2009
****
**** CONNECTIONS:
****           INVERTING INPUT: MEASURED CURRENT EXITS THE SHUNT ON THE VM SIDE
****             |
****             | NON-INVERTING INPUT: MEASURED CURRENT ENTERS THE SHUNT ON THE VP SIDE
****             |   |
****             |   |  OUTPUT VOLTAGE
****             |   |   |
****             |   |   |  POSITIVE POWER SUPPLY LINE
****             |   |   |   |
****             |   |   |   |     NEGATIVE POWER SUPPLY LINE
****             |   |   |   |      |
****             |   |   |   |      |     GROUND LINE
****             |   |   |   |      |      |
****             |   |   |   |      |      |     CONNECTION TO THE OUTPUT RESISTOR
****             |   |   |   |      |      |      |
****             |   |   |   |      |      |      |   GAIN-SELECT PIN
****             |   |   |   |      |      |      |    |
.SUBCKT TSC1031  VM  VP  OUT VCCP VCCN GNDLINE  A1  SEL
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET0313 0 OPAMP_SR
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 10u
    VREADI_ROUT NET254 NET308 DC 0
```

```
    VREADI_RWAKE NET357 DELAY_GEN DC 0
    V63 NET297 NET251 DC {Vd_compensazione}
    VVLIM_LOW_VRG3 NET258 NET259 DC {Vd_compensazione}
    VREADIO VB_3 OUT DC 0
    V62 NET267 NET253 DC {Vd_compensazione}
    VVLIM_HIGH_VRG3 NET273 NET263 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET273 DIODE_NOVd
    D38 VK1K2 NET267 DIODE_NOVd
    DVLIM_LOW_VRG3 NET259 VRG3 DIODE_NOVd
    D39 NET251 VK1K2 DIODE_NOVd
    C86 VRG3_5 0 {CBW}
    C87 VRG3_6 0 {CBW}
    C84 VRG3_3 0 {CBW}
    C79 VRG3_2 0 {CBW}
    C85 VRG3_4 0 {CBW}
    C_WAKE DELAY_GEN 0 60p
    CBW VRG3 A1 {CBW}
    E_ROUT NET308 NET328 VALUE={ IF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VK1K2 0 1.0
    E83 K2_AV100_VAL 0 VALUE={IF( ( V(SEL)>=1.2 ) & ( V(SEL)<=V(Vccp) )
+, K2_Av100 , 0.0 )}
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET0313 0 VCCP 0 1.0
    EOUT NET328 0 VRG3_SR 0 1.0
    E_IIB_VP_VAL_NEG IIB_VP_VAL_NEG 0 VALUE={IF( V(Vsense)<-180m ,
+(56u)*(-180m) , (56u)*V(Vsense) )}
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0

*Eldo:
*    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 18k ) (3m ,
*+13.04k) (4m , 10.9k) ( 5m , 9.4k ) (7m , 7.65k) ( 8m , 7.18k ) ( 9m ,
*+6.9k ) (10.5m 6.615k) (12m 6.45k) ( 15m , 6.32k ) (17m 6.27k) ( 20m ,
*+6.19k ) ( 25m , 6.055k ) ( 30m , 5.944k ) ( 35m , 5.845k ) ( 40m , 5.76k
*+) ( 50m , 5.62k ) ( 60m , 5.505k ) ( 70m , 5.417k ) ( 80m , 5.345k ) (
*+90m , 5.29k ) ( 100m , 5.25k ) ( 120m , 5.2k ) ( 150m , 5.15k )
*PSpice:
    E_RWAKE_VAL RWAKE_VAL 0 VALUE={ TABLE( V(VP,VM) , 2m , 18k , 3m ,
+ 13.04k , 4m , 10.9k , 5m , 9.4k , 7m , 7.65k , 8m , 7.18k , 9m ,
+ 6.9k , 10.5m , 6.615k , 12m , 6.45k , 15m , 6.32k , 17m , 6.27k , 20m ,
+ 6.19k , 25m , 6.055k , 30m , 5.944k , 35m , 5.845k , 40m , 5.76k ,
+ 50m , 5.62k , 60m , 5.505k , 70m , 5.417k , 80m , 5.345k ,
+ 90m , 5.29k , 100m , 5.25k , 120m , 5.2k , 150m , 5.15k )}

    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={IF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET352 0 VALUE={IF( V(VP,VM)>0 , 1 , 0 )}
```

```
    E_RWAKE NET352 NET357 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E81 NET360 0 VALUE={ V(VRg3_6)*V(K2_Av50_val) +
+V(VRg3_6)*V(K2_Av100_val) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={IF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={ V(VP,VM)*V(check_Vicm)*V(check_Supply) }
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={IF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET263 0 VCCP 0 1.0
    E79 CHECK_SUPPLY_DUAL 0 VALUE={IF( ( (V(Vccp)>=2.7) & (V(Vccp)<=5.5)
+& (V(Vccn)<=0) & (V(Vccn)>=-8) ) | ( (V(Vccp)>=2.7) & (V(Vccp)<=3.0) &
+(V(Vccn)<=0) & (V(Vccn)>=-11) ) , 1.0 , 0)}
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={IF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    E78 CHECK_SUPPLY_SINGLE 0 VALUE={IF( (V(Vccp)>=2.7) &
+(V(Vccp)<=5.5) , 1.0 , 0)}
    EVLIM_LOW_VRG3 NET258 0 VCCN 0 1.0
    E75 CHECK_VICM 0 VALUE={IF( (V(VP)>=( Vicm_LOW +
+V(Vccn)*V(dual_supply) )) & (V(VP)<=( Vicm_HIGH + V(Vccn)*V(dual_supply)
+)) , 1.0 , 0)}
    E76 CHECK_SUPPLY 0 VALUE={IF( V(dual_supply)>0.9 ,
+V(check_Supply_dual) , V(check_Supply_single) )}
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    EDUAL_SUPPLY DUAL_SUPPLY 0 VALUE={IF( (V(Vccn)==V(GNDLINE)) &
+(V(GNDLINE)==0) , 0 , 1)}
    E82 K2_AV50_VAL 0 VALUE={IF( ( V(SEL)>=-0.3 ) & ( V(SEL)<=0.5 ) ,
+K2_Av50 , 0.0 )}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -129.5 -5000*I(VreadIo)}
    E100 NET296 NET297 VALUE={ IF(I(VreadIo)<0 , 49.0*I(VreadIo) , 0 )
+}
    E98 NET304 NET253 VALUE={ 58.0*I(VreadIo) }
    E101 NET296 0 VCCN 0 1.0
    E99 NET304 0 VCCP 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={IF( V(Vsense)<= -160m ,
+(-56u)*(-160m) , (-56u)*V(Vsense) )}
    RSEL 0 SEL  {RSEL}
    R144 0 VRG3_6 {Rg3}
    R136 0 VRG3_2 {Rg3}
    R142 0 VRG3_4 {Rg3}
    R143 0 VRG3_5 {Rg3}
    R141 0 VRG3_3 {Rg3}
    RO2_2 NET254 VB_3 {Ro2_2}
    R1 A1 VRG3 {Rg3}
    R147 NET360 VK1K2 1e-3
    CK1K2 VK1K2 0 10n
    G_ICC_VSENSE VCCP VCCN VALUE={IF( V(Vsense)>0 , 0.14625E-4 +
+0.0013075*V(Vsense) , 0 )}
    G70 0 VRG3_6 VRG3_5 0 {1/Rg3}
```

```
    G67 0 VRG3_3 VRG3_2 0 {1/Rg3}
    G68 0 VRG3_4 VRG3_3 0 {1/Rg3}
    G62 0 VRG3_2 VRG3 0 {1/Rg3}
    G69 0 VRG3_5 VRG3_4 0 {1/Rg3}
    G_IIB-VP_VSENSE VP 0 VALUE={IF( V(Vsense)>0 , V(Vsense)/Rg1 ,
+V(Iib_VP_val_neg) )}
    G60 VM 0 VALUE={IF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
    G_IOUT_SOURCED VCCP 0 VALUE={IF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 0 VRG3 VALUE={IF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0 )}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP 0 2.4565217391304354E-4
+1.0869565217391281E-5
    G_IOUT_SINKED VCCN 0 VALUE={IF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.


********************************************************************************
*
* MODELS/SUBCKTS and PARAMS used by TSC1031 subckt:
*

.SUBCKT OPAMP_SR VM VP VS VCCP VCCN
    M_NMOS2 VO_DIFF_MINUS VM VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    M_NMOS1 VO_DIFF_PLUS VP VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    IEE_N VEE_N VCCN_ENHANCED DC {IEE}
    VVLIM_LOW_VB NET0109 NET0110 DC {Vd_compensazione}
    VPROT_IN_P_VCCP NET0123 NET0134 DC {V_DPROT}
    V_ENHANCE_VCCN VCCN_ENHANCED VCCN DC {VCCN_enhance}
    VVLIM_HIGH_VB NET0187 NET0153 DC {Vd_compensazione}
    V_ENHANCE_VCCP VCCP_ENHANCED VCCP DC {VCCP_enhance}
    V_OUTVLIM_LOW NET0224 NET125 DC {Vd_compensazione}
    VPROT_IN_M_VCCN NET0116 NET0192 DC {V_DPROT}
    V_OUTVLIM_HIGH NET0201 NET0131 DC {Vd_compensazione}
    VPROT_IN_P_VCCN NET0115 NET096 DC {V_DPROT}
    VPROT_IN_M_VCCP NET0190 NET0135 DC {V_DPROT}
    DVLIM_HIGH_VB VB NET0187 DIODE_NOVd
    DPROT_IN_M_VCCP VM NET0135 DIODE_VLIM
    DVLIM_LOW_VB NET0110 VB DIODE_NOVd
    DPROT_IN_M_VCCN NET0116 VM DIODE_VLIM
    D_OUTVLIM_LOW NET125 VB_3 DIODE_NOVd
    DPROT_IN_P_VCCP VP NET0134 DIODE_VLIM
    DPROT_IN_P_VCCN NET0115 VP DIODE_VLIM
    D_OUTVLIM_HIGH VB_3 NET0201 DIODE_NOVd
    CCOMP VB VB_2 {Ccomp}
    EMEAS_VOUT_DIFF VOUT_DIFF 0 VO_DIFF_PLUS VO_DIFF_MINUS 1.0
    EVLIM_HIGH_VB NET0153 0 VCCP 0 1.0
    EVLIM_HIGH_VOUT NET0131 0 VCCP 0 1.0
    EVLIM_LOW_VB NET0109 0 VCCN 0 1.0
    E2_REF NET0238 0 VCCN 0 1.0
    E_VREF VREF 0 NET0250 0 1.0
    E1_REF NET0210 0 VCCP 0 1.0
```

```
    EVLIM_LOW_VOUT NET0224 0 VCCN 0 1.0
    RO2_2 VB_3 VB_2 {Ro2_2}
    RPROT_IN_P_VCCP NET0123 VCCP {RPROT_VCCP}
    RPROT_IN_M_VCCP VCCP NET0190 {RPROT_VCCP}
    RO1 VS VB_3 {Ro1}
    RD1 VCCP_ENHANCED VO_DIFF_PLUS {RD}
    RD2 VCCP_ENHANCED VO_DIFF_MINUS {RD}
    RO2_1 VREF VB_2 {Ro2_1}
    R1_REF NET0210 NET0250 1Meg
    R1 VB VREF {R1}
    RPROT_IN_M_VCCN VCCN NET0192 {RPROT_VCCN}
    R2_REF NET0250 NET0238 1Meg
    RPROT_IN_P_VCCN NET096 VCCN {RPROT_VCCN}
    G_I_VB VB_2 VREF VB VREF {GB}
    GM1 VREF VB VOUT_DIFF 0 {1/RD}
.ENDS
*** End of subcircuit definition.

.PARAM RSEL = 5.5e6
.PARAM Vicm_LOW  = 2.9
.PARAM Vicm_HIGH = 75
.PARAM Iib = 10e-6
.PARAM Rg1 = 5k
.PARAM K1       = 25
.PARAM Rg3      = {K1*Rg1}
.PARAM K2_Av50  = 2
.PARAm K2_Av100 = 4
.PARAM Ro_sink = 2
.PARAM Ro_source = 2
.PARAM Ro_off = 1.05
.PARAM alpha_switch_Ro = 1e4
.PARAM CBW = 0.533p
.PARAM RD=1k
.PARAM VCCP_enhance=150m
.PARAM VCCN_enhance=-1100m
.PARAM Ccomp=11p
.PARAM IEE=10u
.PARAM A0=97.93103448E3
.PARAM Ro=17587.2
.PARAM W=11u
.PARAM L=1u
.PARAM gm_mos=0.0002347956532101469
.PARAM GB=10m
.PARAM Ro1=1
.PARAM Ro2_2=1e-3
.PARAM Ro2_1={Ro - Ro2_2 - Ro1}
.PARAM R1={A0/(gm_mos*GB*Ro2_1)}
.PARAM V_DPROT=150m
.PARAM RPROT_VCCP=100
.PARAM RPROT_VCCN=15k
.PARAM Vd_compensazione=-788.4u
```

```
*Eldo:
*.MODEL MOS_N  NMOS LEVEL=1 MODTYPE=ELDO VTO=+0.65  KP=500E-6
*.MODEL DIODE_NOVd D LEVEL=1 MODTYPE=ELDO IS=10E-15 N=0.001
*.MODEL DIODE_VLIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
*.MODEL DIODE_ILIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
*.MODEL DX D LEVEL=1 MODTYPE=ELDO IS=1E-14
*PSpice:
.MODEL MOS_N  NMOS LEVEL=1 VTO=+0.65  KP=500E-6
.MODEL DIODE_NOVd D LEVEL=1 IS=10E-15 N=0.001
.MODEL DIODE_VLIM D LEVEL=1 IS=0.8E-15
.MODEL DIODE_ILIM D LEVEL=1 IS=0.8E-15
.MODEL DX D LEVEL=1 IS=1E-14
*
********************************************************************************
```

## 3.2 TSC1031 macromodel Library netlist for Eldo simulator

The macromodel netlist in Mentor Graphics Eldo compatible syntax follows: (N.B.: simulating it the user has not to use the -stver option running Eldo simulator, because the TSC1031 macromodel netlist uses basic standard analog devices, not STMicroelectronics version instead used in real TSC1031 netlist)

```
****************************************************************************
*
* WARNING : please consider following remarks before usage
*
* 1) All models are a tradeoff between accuracy and complexity (ie. simulation
*    time).
*
* 2) Macromodels are not a substitute to breadboarding, they rather confirm the
*    validity of a design approach and help to select surrounding component values.
*
* 3) A macromodel emulates the NOMINAL performance of a TYPICAL device within
*    SPECIFIED OPERATING CONDITIONS (ie. temperature, supply voltage, etc.).
*    Thus the macromodel is often not as exhaustive as the datasheet, its goal
*    is to illustrate the main parameters of the product.
*
* 4) Data issued from macromodels used outside of its specified conditions
*    (Vcc, Temperature, etc) or even worse: outside of the device operating
*    conditions (Vcc, Vicm, etc) are not reliable in any way.
*
****************************************************************************
****
***  TSC1031  Eldo macromodel subckt
***  May 2009
****
**** CONNECTIONS:
****           INVERTING INPUT: MEASURED CURRENT EXITS THE SHUNT ON THE VM SIDE
****             |
****             | NON-INVERTING INPUT: MEASURED CURRENT ENTERS THE SHUNT ON THE VP SIDE
****             |   |
****             |   |  OUTPUT VOLTAGE
****             |   |   |
****             |   |   |  POSITIVE POWER SUPPLY LINE
****             |   |   |   |
****             |   |   |   |     NEGATIVE POWER SUPPLY LINE
****             |   |   |   |      |
****             |   |   |   |      |     GROUND LINE
****             |   |   |   |      |      |
****             |   |   |   |      |      |     CONNECTION TO THE OUTPUT RESISTOR
****             |   |   |   |      |      |      |
****             |   |   |   |      |      |      |    GAIN-SELECT PIN
****             |   |   |   |      |      |      |     |
.SUBCKT TSC1031  VM  VP  OUT VCCP VCCN GNDLINE  A1  SEL
    XIAMP_SR VRG3_SR INBUF VRG3_SR NET0313 0 OPAMP_SR
```

```
    IIB_VP VP 0 DC {Iib}
    IIB_VM VM 0 DC 10u
    VREADI_ROUT NET254 NET308 DC 0
    VREADI_RWAKE NET357 DELAY_GEN DC 0
    V63 NET297 NET251 DC {Vd_compensazione}
    VVLIM_LOW_VRG3 NET258 NET259 DC {Vd_compensazione}
    VREADIO VB_3 OUT DC 0
    V62 NET267 NET253 DC {Vd_compensazione}
    VVLIM_HIGH_VRG3 NET273 NET263 DC {Vd_compensazione}
    DILIM_SINK VB_3_SINK VB_3 DIODE_ILIM
    DILIM_SOURCE VB_3 VB_3_SOURCE DIODE_ILIM
    DVLIM_HIGH_VRG3 VRG3 NET273 DIODE_NOVd
    D38 VK1K2 NET267 DIODE_NOVd
    DVLIM_LOW_VRG3 NET259 VRG3 DIODE_NOVd
    D39 NET251 VK1K2 DIODE_NOVd
    C86 VRG3_5 0 {CBW}
    C87 VRG3_6 0 {CBW}
    C84 VRG3_3 0 {CBW}
    C79 VRG3_2 0 {CBW}
    C85 VRG3_4 0 {CBW}
    C_WAKE DELAY_GEN 0 60p
    CBW VRG3 A1 {CBW}
    E_ROUT NET308 NET328 VALUE={ VALIF( V(VP,VM)>=0  , ( Ro_sink
++(Ro_source - Ro_sink)*1/(1+exp( -alpha_switch_Ro*V(V_Io_val) ) )
+)*I(VreadI_ROUT)  , Ro_OFF*I(VreadI_ROUT) )}
    E67 INBUF 0 VK1K2 0 1.0
    E83 K2_AV100_VAL 0 VALUE={VALIF( ( V(SEL)>=1.2 ) & ( V(SEL)<=V(Vccp) )
+, K2_Av100 , 0.0 )}
    E_READIO V_IO_VAL 0 VALUE={I(VreadIo)}
    E64 NET0313 0 VCCP 0 1.0
    EOUT NET328 0 VRG3_SR 0 1.0
    E_IIB_VP_VAL_NEG IIB_VP_VAL_NEG 0 VALUE={VALIF( V(Vsense)<-180m ,
+(56u)*(-180m) , (56u)*V(Vsense) )}
    EILIM_SOURCE VB_3_SOURCE VDEP_SOURCE VB_3 0 1.0
    E_RWAKE_VAL RWAKE_VAL 0 TABLE { V(VP,VM) } = ( 2m , 18k ) (3m ,
+13.04k) (4m , 10.9k) ( 5m , 9.4k ) (7m , 7.65k) ( 8m , 7.18k ) ( 9m ,
+6.9k ) (10.5m 6.615k) (12m 6.45k) ( 15m , 6.32k ) (17m 6.27k) ( 20m ,
+6.19k ) ( 25m , 6.055k ) ( 30m , 5.944k ) ( 35m , 5.845k ) ( 40m , 5.76k
+) ( 50m , 5.62k ) ( 60m , 5.505k ) ( 70m , 5.417k ) ( 80m , 5.345k ) (
+90m , 5.29k ) ( 100m , 5.25k ) ( 120m , 5.2k ) ( 150m , 5.15k )
    E_VDEP_SOURCE_2 VAL_VDEP_SOURCE_FILTERED 0
+VALUE={VALIF(V(val_vdep_source)>=0, 0, V(val_vdep_source))}
    EVIN_WAKE VSENSE_WAKE 0 VALUE={ V(Vsense)*V(waking-up_ctrl) }
    E_WAKE NET352 0 VALUE={VALIF( V(VP,VM)>0 , 1 , 0 )}
    E_RWAKE NET352 NET357 VALUE={ V(Rwake_val)*I(VreadI_Rwake) }
    E81 NET360 0 VALUE={ V(VRg3_6)*V(K2_Av50_val) +
+V(VRg3_6)*V(K2_Av100_val) }
    E_WAKING-UP_CTRL WAKING-UP_CTRL 0 VALUE={VALIF( V(delay_gen)>0.99 , 1
+, 0 )}
    EILIM_SINK VB_3_SINK VDEP_SINK VB_3 0 1.0
    E_VDEP_SINK_3 VDEP_SINK 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
```

```
+V(val_vdep_sink_filtered))}
    EVIN VSENSE 0 VALUE={ V(VP,VM)*V(check_Vicm)*V(check_Supply) }
    E_VDEP_SOURCE_3 VDEP_SOURCE 0 VALUE={VALIF( abs(I(VreadIo))<1m , 0 ,
+V(val_vdep_source_filtered))}
    EVLIM_HIGH_VRG3 NET263 0 VCCP 0 1.0
    E79 CHECK_SUPPLY_DUAL 0 VALUE={VALIF( ( (V(Vccp)>=2.7) & (V(Vccp)<=5.5)
+& (V(Vccn)<=0) & (V(Vccn)>=-8) ) | ( (V(Vccp)>=2.7) & (V(Vccp)<=3.0) &
+(V(Vccn)<=0) & (V(Vccn)>=-11) ) , 1.0 , 0)}
    E_VDEP_SINK_2 VAL_VDEP_SINK_FILTERED 0
+VALUE={VALIF(V(val_vdep_sink)<=0 , 0 , V(val_vdep_sink))}
    E78 CHECK_SUPPLY_SINGLE 0 VALUE={VALIF( (V(Vccp)>=2.7) &
+(V(Vccp)<=5.5) , 1.0 , 0)}
    EVLIM_LOW_VRG3 NET258 0 VCCN 0 1.0
    E75 CHECK_VICM 0 VALUE={VALIF( (V(VP)>=( Vicm_LOW +
+V(Vccn)*V(dual_supply) )) & (V(VP)<=( Vicm_HIGH + V(Vccn)*V(dual_supply)
+)) , 1.0 , 0)}
    E76 CHECK_SUPPLY 0 VALUE={VALIF( V(dual_supply)>0.9 ,
+V(check_Supply_dual) , V(check_Supply_single) )}
    E_VDEP_SOURCE_1 VAL_VDEP_SOURCE 0 VALUE={ 129.5  -5000*I(VreadIo)}
    EDUAL_SUPPLY DUAL_SUPPLY 0 VALUE={VALIF( (V(Vccn)==V(GNDLINE)) &
+(V(GNDLINE)==0) , 0 , 1)}
    E82 K2_AV50_VAL 0 VALUE={VALIF( ( V(SEL)>=-0.3 ) & ( V(SEL)<=0.5 ) ,
+K2_Av50 , 0.0 )}
    E_VDEP_SINK_1 VAL_VDEP_SINK 0 VALUE={ -129.5 -5000*I(VreadIo)}
    E100 NET296 NET297 VALUE={ VALIF(I(VreadIo)<0 , 49.0*I(VreadIo) , 0 )
+}
    E98 NET304 NET253 VALUE={ 58.0*I(VreadIo) }
    E101 NET296 0 VCCN 0 1.0
    E99 NET304 0 VCCP 0 1.0
    E_IIB_VM_VAL IIB_VM_VAL 0 VALUE={VALIF( V(Vsense)<= -160m ,
+(-56u)*(-160m) , (-56u)*V(Vsense) )}
    RSEL 0 SEL  {RSEL}
    R144 0 VRG3_6 {Rg3}
    R136 0 VRG3_2 {Rg3}
    R142 0 VRG3_4 {Rg3}
    R143 0 VRG3_5 {Rg3}
    R141 0 VRG3_3 {Rg3}
    RO2_2 NET254 VB_3 {Ro2_2}
    R1 A1 VRG3 {Rg3}
    R147 NET360 VK1K2 1e-3
    CK1K2 VK1K2 0 10n
    G_ICC_VSENSE VCCP VCCN VALUE={VALIF( V(Vsense)>0 , 0.14625E-4 +
+0.0013075*V(Vsense) , 0 )}
    G70 0 VRG3_6 VRG3_5 0 {1/Rg3}
    G67 0 VRG3_3 VRG3_2 0 {1/Rg3}
    G68 0 VRG3_4 VRG3_3 0 {1/Rg3}
    G62 0 VRG3_2 VRG3 0 {1/Rg3}
    G69 0 VRG3_5 VRG3_4 0 {1/Rg3}
    G_IIB-VP_VSENSE VP 0 VALUE={VALIF( V(Vsense)>0 , V(Vsense)/Rg1 ,
+V(Iib_VP_val_neg) )}
    G60 VM 0 VALUE={VALIF( V(Vsense)>0 , 0 , V(Iib_VM_val) )}
```

```
    G_IOUT_SOURCED VCCP 0 VALUE={VALIF(I(VreadIo)>0, I(VreadIo),0)}
    GM1 0 VRG3 VALUE={VALIF( V(VP,VM)>=0 , V(Vsense_wake)/Rg1 , 0 )}
    G_ICC_VCC VCCP VCCN POLY(1) VCCP 0 2.4565217391304354E-4
+1.0869565217391281E-5
    G_IOUT_SINKED VCCN 0 VALUE={VALIF(I(VreadIo)>0, 0, I(VreadIo))}
.ENDS
*** End of subcircuit definition.

*******************************************************************************
*
* MODELS/SUBCKTS and PARAMS used by TSC1031 subckt:
*

.SUBCKT OPAMP_SR VM VP VS VCCP VCCN
    M_NMOS2 VO_DIFF_MINUS VM VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    M_NMOS1 VO_DIFF_PLUS VP VEE_N VCCN_ENHANCED MOS_N L={L} W={W}
    IEE_N VEE_N VCCN_ENHANCED DC {IEE}
    VVLIM_LOW_VB NET0109 NET0110 DC {Vd_compensazione}
    VPROT_IN_P_VCCP NET0123 NET0134 DC {V_DPROT}
    V_ENHANCE_VCCN VCCN_ENHANCED VCCN DC {VCCN_enhance}
    VVLIM_HIGH_VB NET0187 NET0153 DC {Vd_compensazione}
    V_ENHANCE_VCCP VCCP_ENHANCED VCCP DC {VCCP_enhance}
    V_OUTVLIM_LOW NET0224 NET125 DC {Vd_compensazione}
    VPROT_IN_M_VCCN NET0116 NET0192 DC {V_DPROT}
    V_OUTVLIM_HIGH NET0201 NET0131 DC {Vd_compensazione}
    VPROT_IN_P_VCCN NET0115 NET096 DC {V_DPROT}
    VPROT_IN_M_VCCP NET0190 NET0135 DC {V_DPROT}
    DVLIM_HIGH_VB VB NET0187 DIODE_NOVd
    DPROT_IN_M_VCCP VM NET0135 DIODE_VLIM
    DVLIM_LOW_VB NET0110 VB DIODE_NOVd
    DPROT_IN_M_VCCN NET0116 VM DIODE_VLIM
    D_OUTVLIM_LOW NET125 VB_3 DIODE_NOVd
    DPROT_IN_P_VCCP VP NET0134 DIODE_VLIM
    DPROT_IN_P_VCCN NET0115 VP DIODE_VLIM
    D_OUTVLIM_HIGH VB_3 NET0201 DIODE_NOVd
    CCOMP VB VB_2 {Ccomp}
    EMEAS_VOUT_DIFF VOUT_DIFF 0 VO_DIFF_PLUS VO_DIFF_MINUS 1.0
    EVLIM_HIGH_VB NET0153 0 VCCP 0 1.0
    EVLIM_HIGH_VOUT NET0131 0 VCCP 0 1.0
    EVLIM_LOW_VB NET0109 0 VCCN 0 1.0
    E2_REF NET0238 0 VCCN 0 1.0
    E_VREF VREF 0 NET0250 0 1.0
    E1_REF NET0210 0 VCCP 0 1.0
    EVLIM_LOW_VOUT NET0224 0 VCCN 0 1.0
    RO2_2 VB_3 VB_2 {Ro2_2}
    RPROT_IN_P_VCCP NET0123 VCCP {RPROT_VCCP}
    RPROT_IN_M_VCCP VCCP NET0190 {RPROT_VCCP}
    RO1 VS VB_3 {Ro1}
    RD1 VCCP_ENHANCED VO_DIFF_PLUS {RD}
    RD2 VCCP_ENHANCED VO_DIFF_MINUS {RD}
    RO2_1 VREF VB_2 {Ro2_1}
```

```
    R1_REF NET0210 NET0250 1Meg
    R1 VB VREF {R1}
    RPROT_IN_M_VCCN VCCN NET0192 {RPROT_VCCN}
    R2_REF NET0250 NET0238 1Meg
    RPROT_IN_P_VCCN NET096 VCCN {RPROT_VCCN}
    G_I_VB VB_2 VREF VB VREF {GB}
    GM1 VREF VB VOUT_DIFF 0 {1/RD}
.ENDS
*** End of subcircuit definition.

.PARAM RSEL = 5.5e6
.PARAM Vicm_LOW  = 2.9
.PARAM Vicm_HIGH = 75
.PARAM Iib = 10e-6
.PARAM Rg1 = 5k
.PARAM K1       = 25
.PARAM Rg3      = {K1*Rg1}
.PARAM K2_Av50  = 2
.PARAm K2_Av100 = 4
.PARAM Ro_sink = 2
.PARAM Ro_source = 2
.PARAM Ro_off = 1.05
.PARAM alpha_switch_Ro = 1e4
.PARAM CBW = 0.533p
.PARAM RD=1k
.PARAM VCCP_enhance=150m
.PARAM VCCN_enhance=-1100m
.PARAM Ccomp=11p
.PARAM IEE=10u
.PARAM A0=97.93103448E3
.PARAM Ro=17587.2
.PARAM W=11u
.PARAM L=1u
.PARAM gm_mos=0.0002347956532101469
.PARAM GB=10m
.PARAM Ro1=1
.PARAM Ro2_2=1e-3
.PARAM Ro2_1={Ro - Ro2_2 - Ro1}
.PARAM R1={A0/(gm_mos*GB*Ro2_1)}
.PARAM V_DPROT=150m
.PARAM RPROT_VCCP=100
.PARAM RPROT_VCCN=15k
.PARAM Vd_compensazione=-788.4u

.MODEL MOS_N  NMOS LEVEL=1 MODTYPE=ELDO VTO=+0.65  KP=500E-6
.MODEL DIODE_NOVd D LEVEL=1 MODTYPE=ELDO IS=10E-15 N=0.001
.MODEL DIODE_VLIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
.MODEL DIODE_ILIM D LEVEL=1 MODTYPE=ELDO IS=0.8E-15
.MODEL DX D LEVEL=1 MODTYPE=ELDO IS=1E-14
*
*******************************************************************************
```

# 4 DC simulations: macromodel behaviour

The macromodel matches the real current sensing TSC1031 DC behaviour: the following sections explain how the macromodel fits each DC specification.

## 4.1 Supply voltage ranges

The macromodel works if the applied voltages on the supply pins Vccp (positive supply voltage) and Vccn (negative supply voltage) respect the spefitication, therefore as follow:

- if there is a *single supply configuration* (Vccn connected to Gnd=0) then Vccp=Vcc must be $\in [2.7V, 5.5V]$;
- if there is a *dual supply configuration* then the allowed suply range is Vccn $\in [-8.0V, 0V]$ and Vccp $\in [2.7V, 5.5V]$
  or
  Vccn $\in [-11.0V, 0V]$ and Vccp $\in [2.7V, 3.0V]$.

If the applied supply voltages aren't inside the above specification range then the macromodel gives null output.

## 4.2 Total supply current consumption

Fig. 3 shows the circuit used to simulate it.

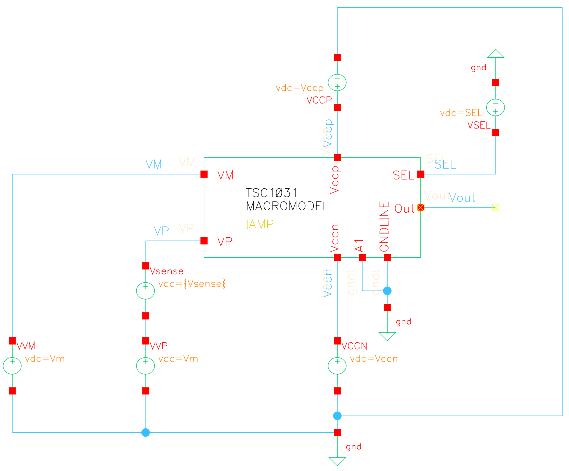


Figure 3: Total Consumption current (Icc): simulation schematic.

Fig. 4 shows the macromodel Icc (total consumption supply current) simulation considering the following datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc, Vccn=0 (single supply configuration), Vm=12V, **fixing Vsense=Vp-Vm=0V and varying Vcc in** $[2.7V, 5.5V]$.

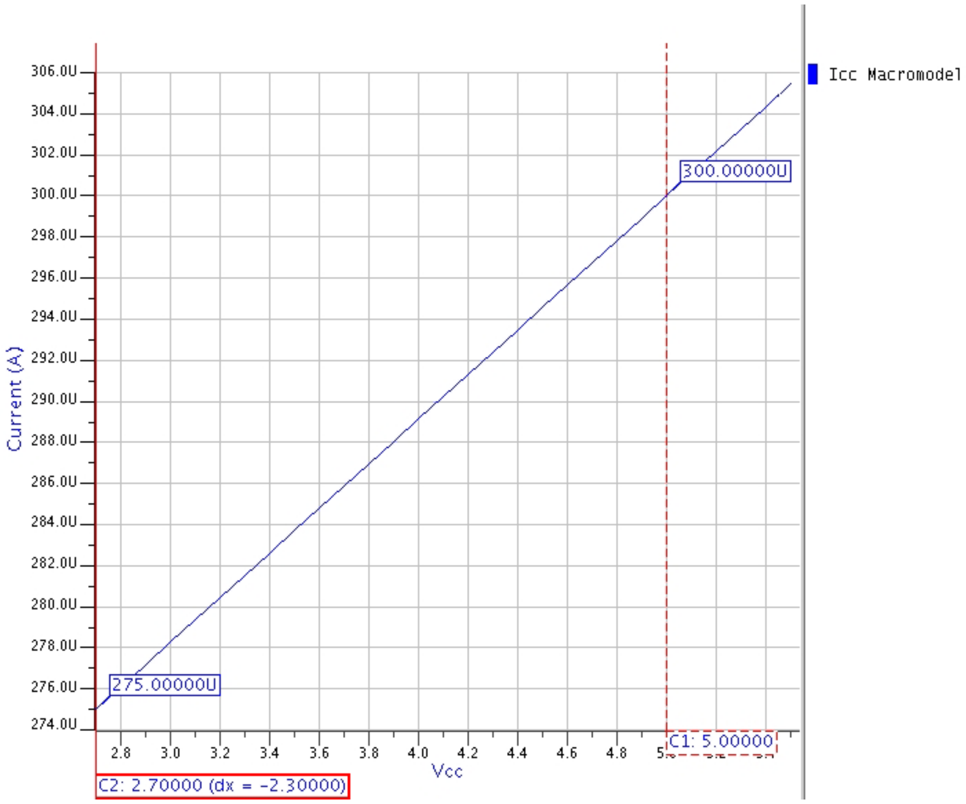


Figure 4: Total supply current (Icc) vs supply voltage (Vcc) (@ Vsense=0V): macromodel simulation result vs measure.

The following table 2 shows the Icc comparison among the macromodel and the datasheet typical value:

| Macromodel | Datasheet |
|---|---|
| 300 $\mu$A | 300 $\mu$A |

Table 2: Total Icc (Consumption current) @ Vsense=0V , Vcc=5V: macromodel simulations vs datasheet.

Fig. 5 shows the macromodel Icc (consumption supply current) simulation considering the following datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V and **varying Vsense=(Vp-Vm) in** $[-120mV, +120mV]$.

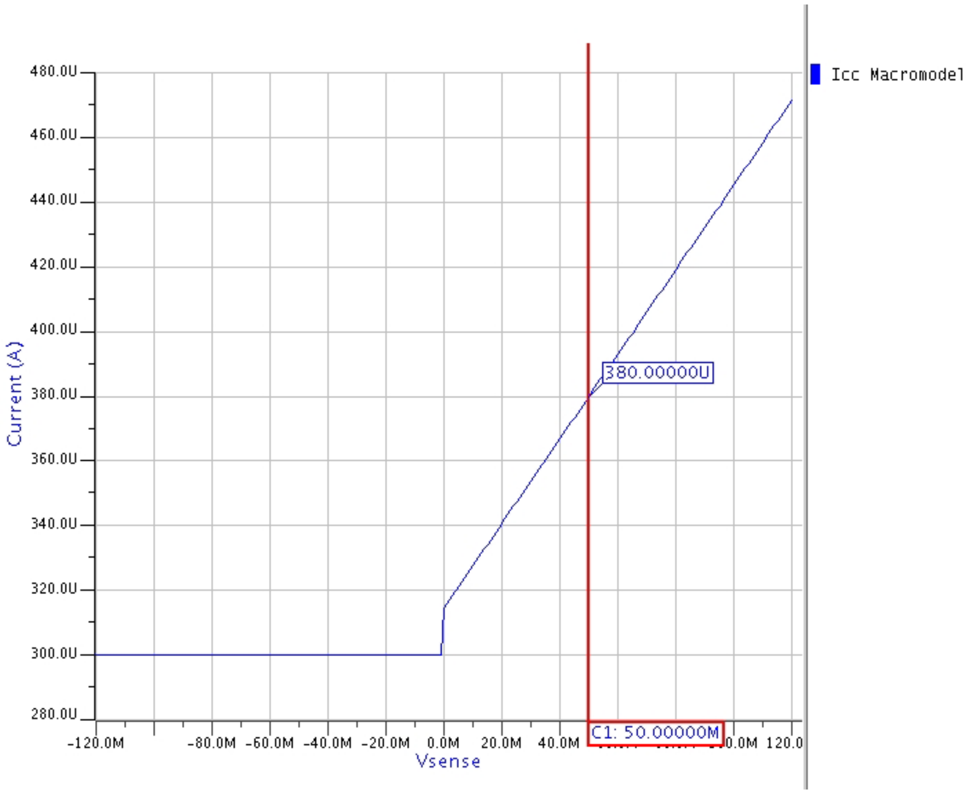


Figure 5: Total supply current (Icc) vs Vsense: macromodel simulation result.

The following table 3 shows the Icc comparison among the macromodel and the datasheet typical value at Vsense=50mV:

| Macromodel | Datasheet |
|---|---|
| 380 $\mu$A | 380 $\mu$A |

Table 3: Total Icc (Consumption current) @ Vsense=50mV , Vcc=5V: macromodel simulations vs datasheet.

## 4.3 Common mode input voltage (Vicm)

The TSC1031 macromodel matchs the real behaviour regarding the input common-mode explained in sec. 2, so the macromodel has independent input common-mode and power supply voltages and supports the datasheet voltage range shown in fig. 6; therefore the macromodel features an input common-mode voltage in the single-supply configuration (Vccn connected to Gnd=0) inside $[2.9V, 75V]$ and in dual-supply configuration it is offset by the voltage supplied on Vccn pin. If the input common mode voltage isn't inside the above specification ranges then the macromodel gives null output.

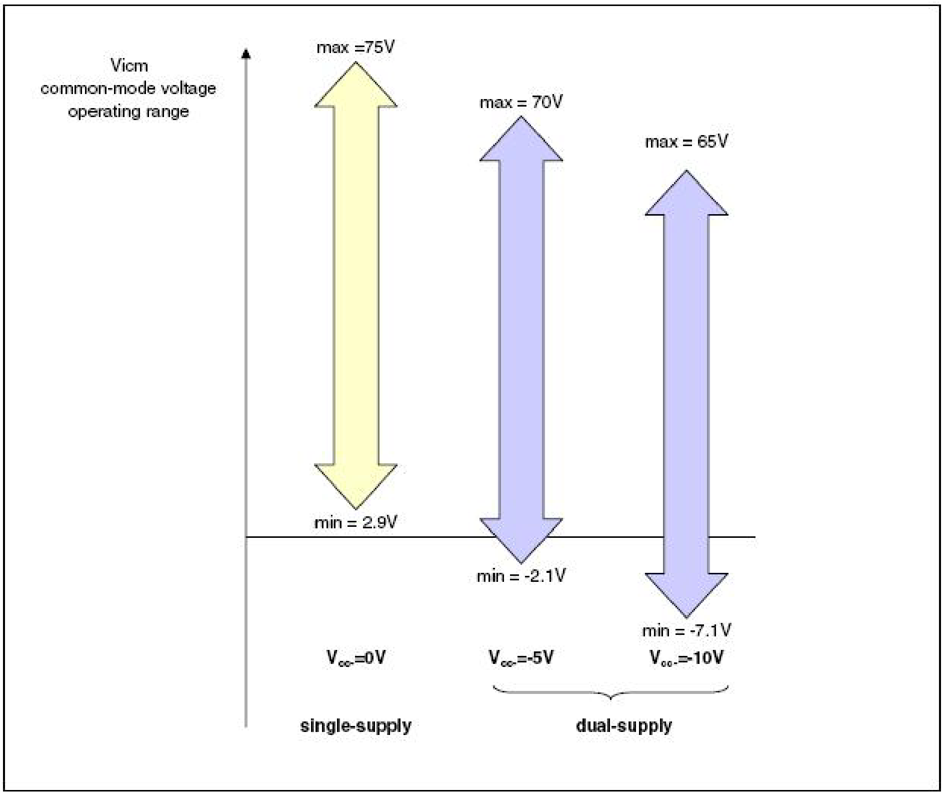


Figure 6: Common-mode versus supply voltage: macromodel behaviour.

## 4.4 Input bias current (Iib)

Fig. 7 shows the circuit used to simulate it.

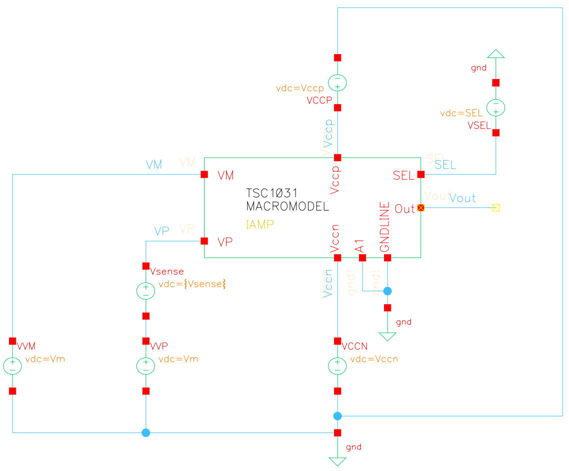


Figure 7: Input bias current (Iib): simulation schematic.

Fig. 8 shows the macromodel Vp pin input bias current simulation compared with the measured one, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V and **varying Vsense=(Vp-Vm) in** $[-1V, +0.3V]$.

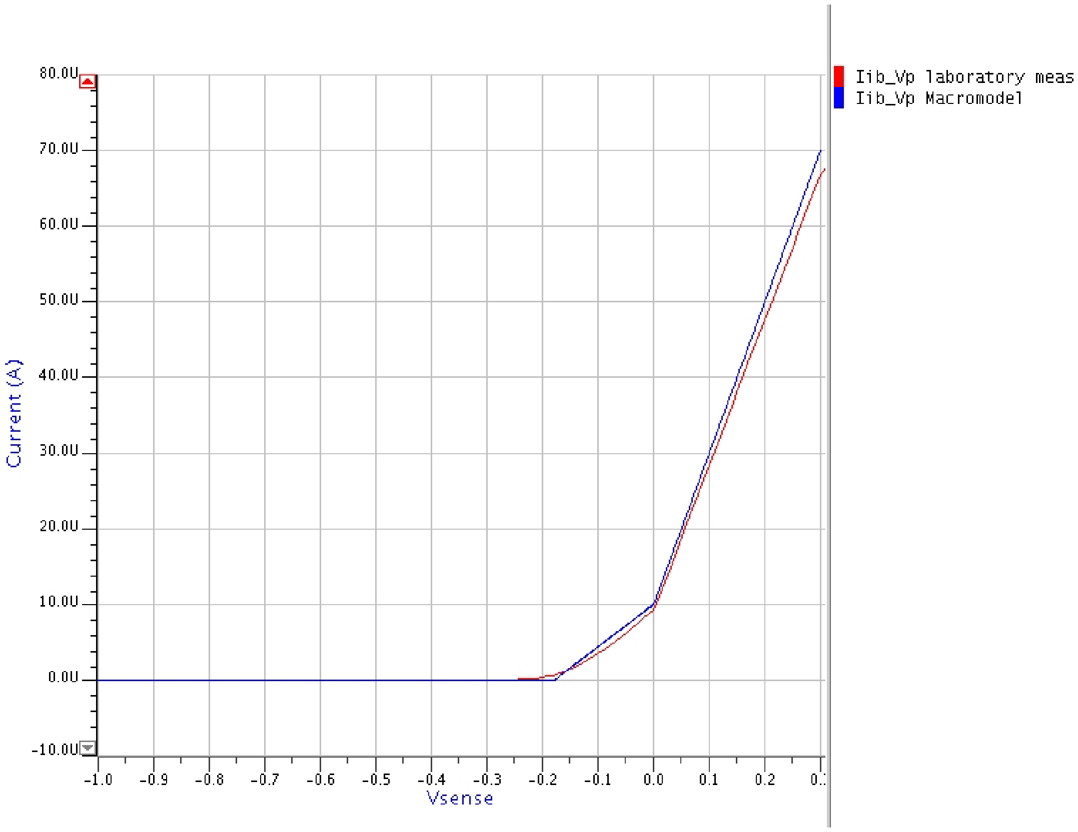


Figure 8: Vp pin input bias current vs Vsense: macromodel simulation result vs measure.

The following table 4 shows the Vp pin input bias current comparison of the macromodel, the laboratory measure and of the datasheet typical values @ Vsense=0V, Vcc=5V:

| Macromodel | Laboratory measure | Datasheet |
|---|---|---|
| 10 $\mu$A | 9.23 $\mu$A | 10 $\mu$A |

Table 4: Vp pin input bias current @ Vsense=0V , Vcc=5V: macromodel simulations vs datasheet vs laboratory measure.

The macromodel fits well the measured Vp pin input bias current, varying Vsense.

Fig. 9 shows the macromodel Vm pin input bias current simulation compared with the measured one, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V and **varying Vsense=(Vp-Vm) in** $[-1V, +0.3V]$.

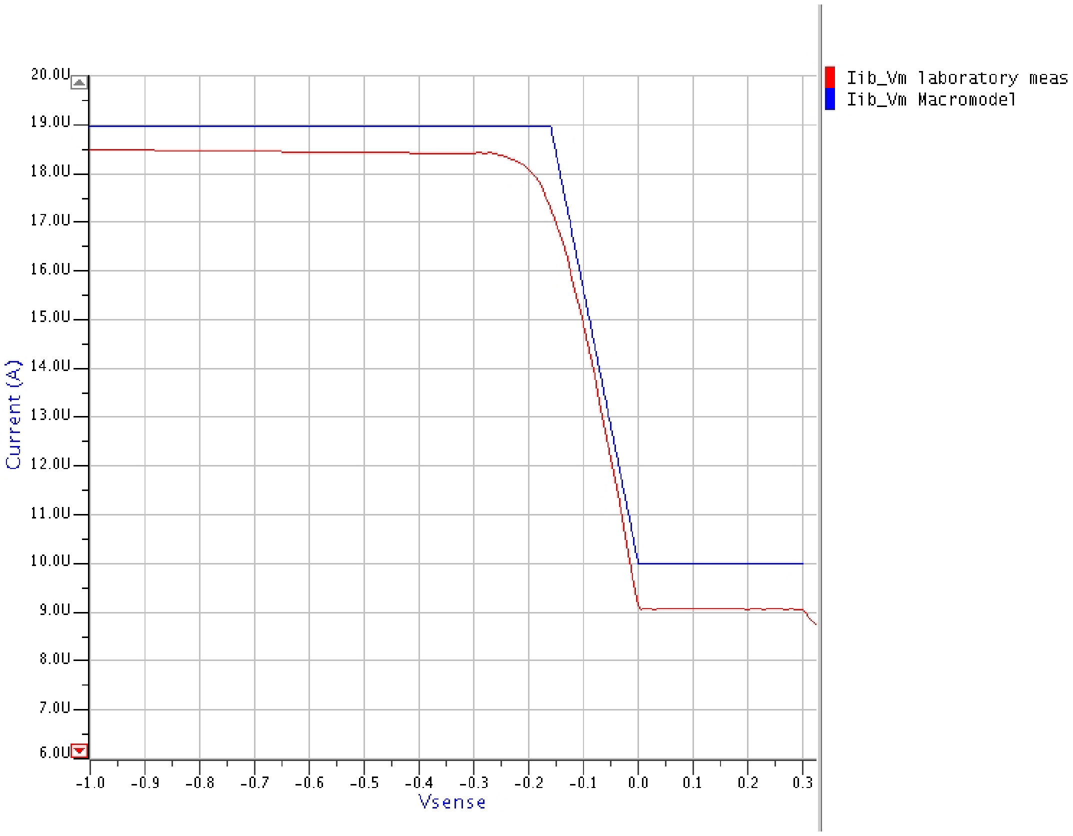


Figure 9: Vm pin input bias current vs Vsense: macromodel simulation result vs measure.

The following table 5 shows the Vm pin input bias current comparison of the macromodel, the laboratory measure and of the datasheet typical values @ Vsense=0V, Vcc=5V:

| Macromodel | Laboratory measure | Datasheet |
|---|---|---|
| 10 $\mu$A | 9.13 $\mu$A | 10 $\mu$A |

Table 5: Vm pin input bias current @ Vsense=0V , Vcc=5V: macromodel simulations vs datasheet vs laboratory measure.

The macromodel fits well the measured Vm pin input bias current, varying Vsense.

## 4.5 SEL pin logic states: voltage ranges

The macromodel maps the SEL pin voltage in its digital logic state according the following ranges:

| Voltage range | SEL pin logic state |
|---|---|
| $V(SEL) \in [+1.2V, Vccp]$ | High |
| $V(SEL) \in [-0.3V, +0.5V]$ | Low |

Table 6: SEL pin logic states map: macromodel behaviour.

## 4.6 Transfer function: output voltage vs Vsense

Fig. 10 shows the circuit used to simulate the transfer function, output voltage vs Vsense:

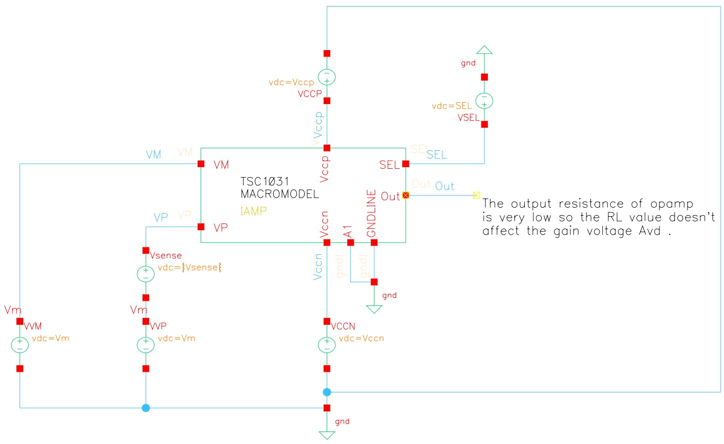


Figure 10: Transfer function, output voltage vs Vsense: simulation schematic.

The macromodel Avd (Large signal voltage gain) follows in table 7, simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc, Vccn=0 (single supply configuration), Vm=12V, Vcc=5V, no load on out.

| Macromodel | Datasheet (Typ.) | Conditions |
|---|---|---|
| 100 V/V | 100 V/V | SEL high |
| 50 V/V | 50 V/V | SEL low |

Table 7: Avd (Large signal voltage gain): macromodel simulations vs datasheet .

Fig. 11 shows the entire Vout vs Vsense curves simulation.

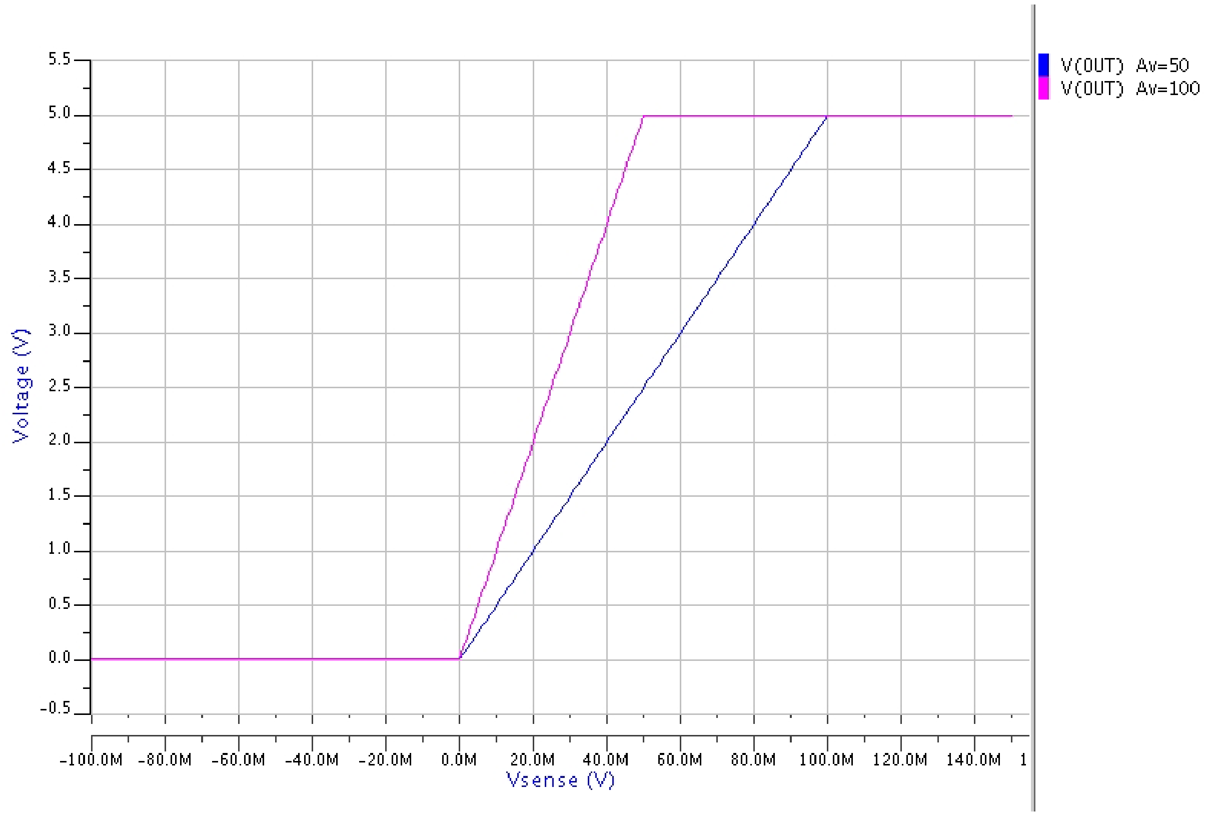


Figure 11: Output voltage (Vout) vs Vsense: macromodel simulation result.

Fig. 12 shows, for low Vsense values (<20mV), the Vout vs Vsense curves simulation.

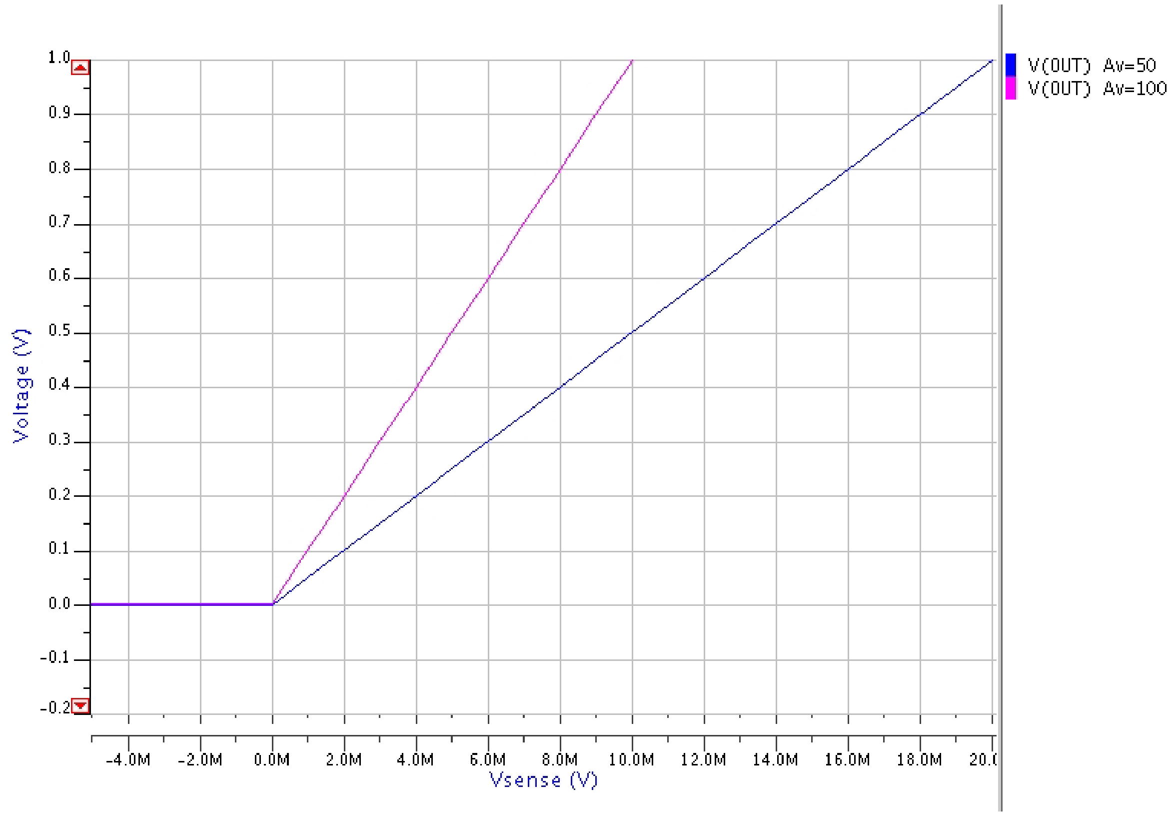


Figure 12: Output voltage (Vout) versus Vsense for low Vsense: macromodel simulation result.

## 4.7 Output stage load regulation ($R_{out} = \Delta V_{out}/\Delta I_{out}$)

Fig. 13 shows the circuit used to simulate it.

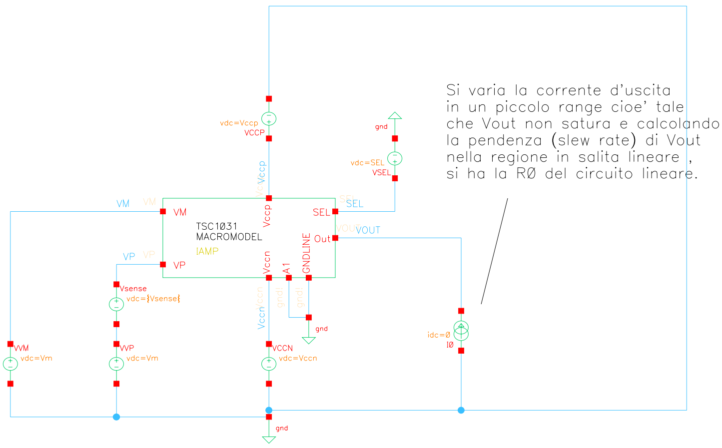


Figure 13: Output stage load regulation: simulation schematic.

Fig. 14 shows the macromodel output stage load regulation ( Vout-Vout0 vs Iout , Vout0 is Vout @ Iout=0) simulation, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Vsense=(Vp-Vm)=50mV and **varying Iout in** $[-10mA, +10mA]$.

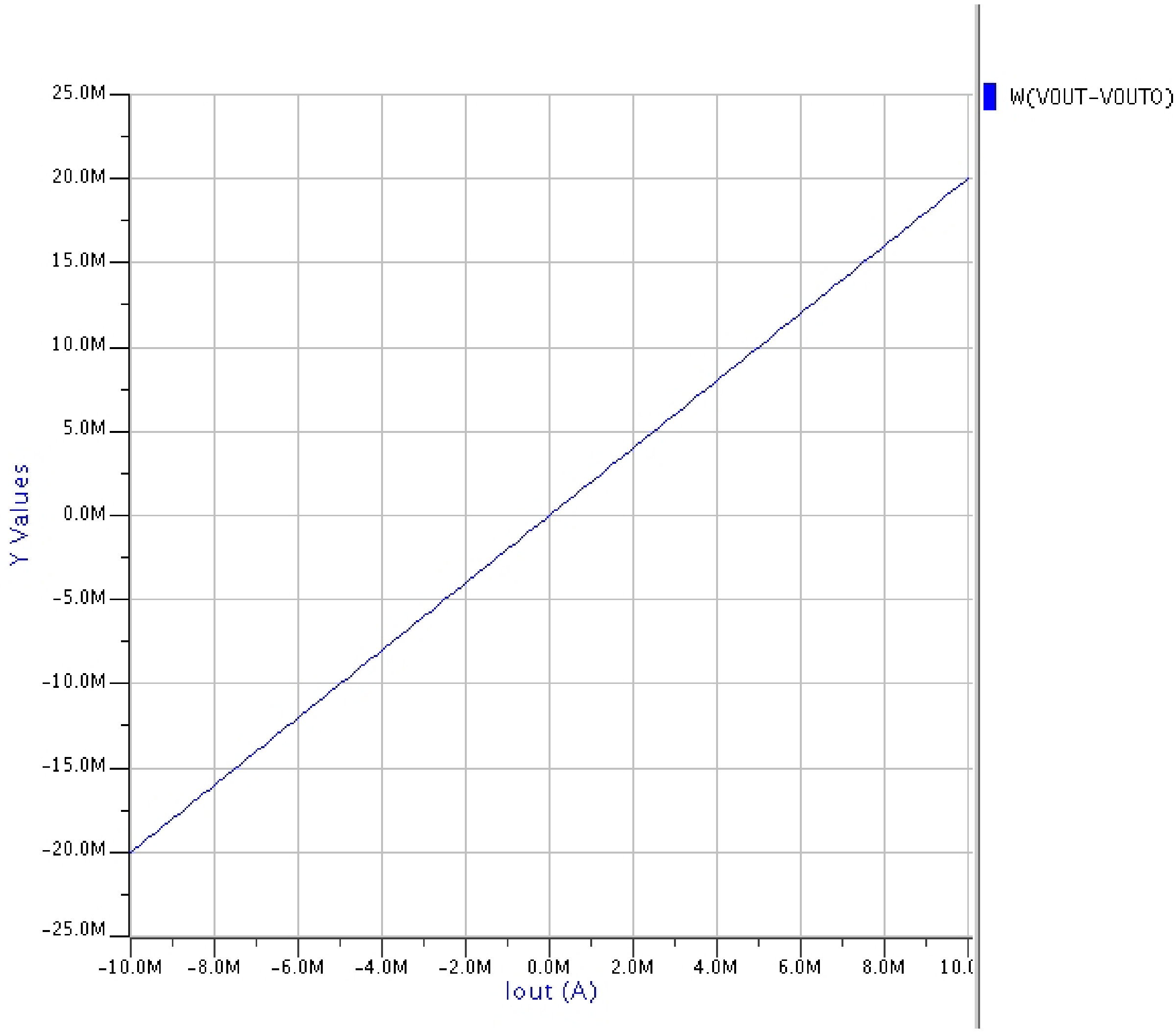


Figure 14: Output stage load regulation: macromodel simulation.

The macromodel fits well the datasheet $\Delta V_{out}/\Delta I_{out}$ specification: as shown in fig. 15, the macromodel has a $R_{out} = \Delta V_{out}/\Delta I_{out} \simeq 2\frac{mV}{mA}$ for output stage source/sink current.

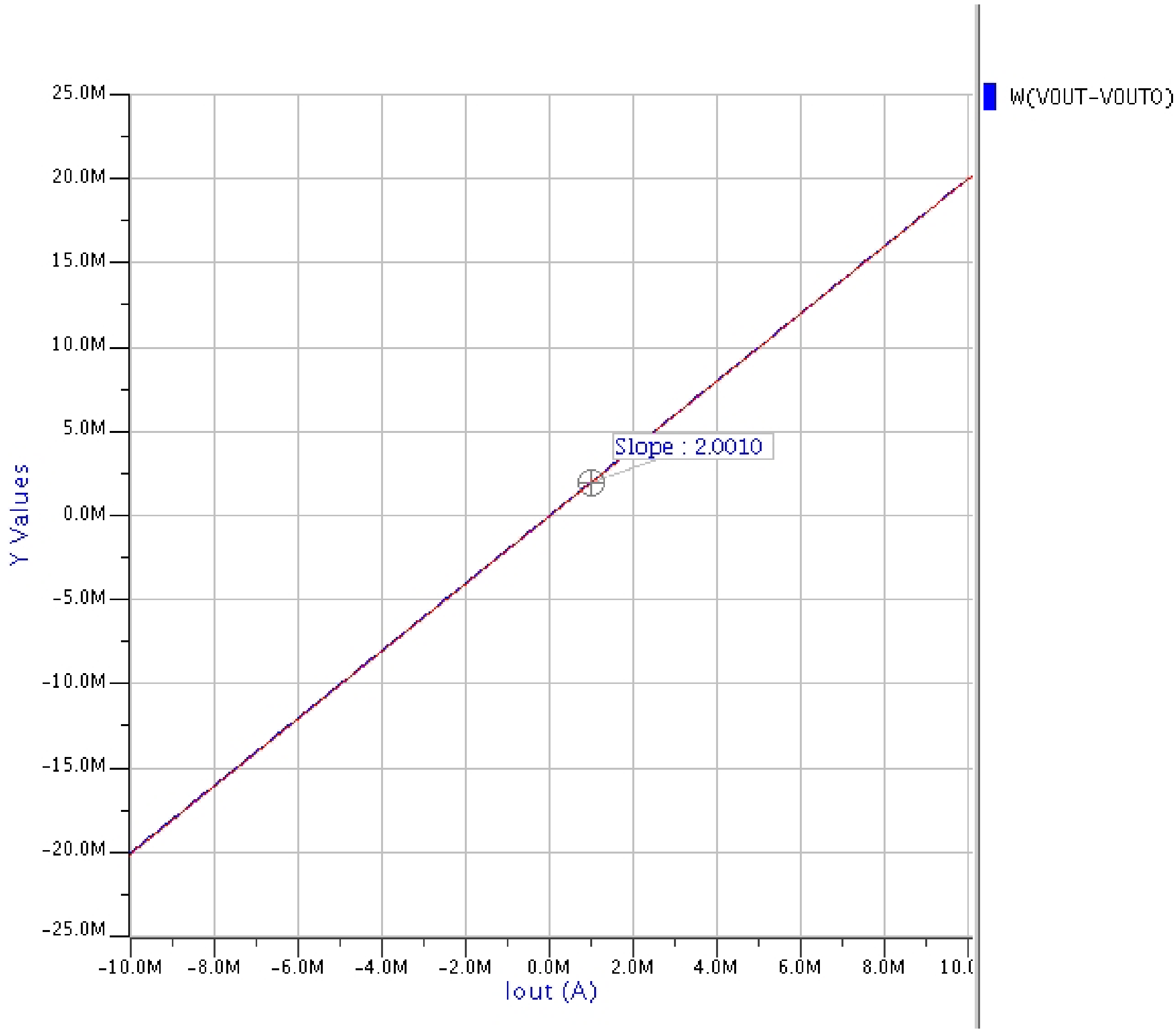


Figure 15: Output stage load regulation: slope $\Delta V_{out}/\Delta I_{out} = R_{out}$.

## 4.8 Isource short-circuit current

Fig. 16 shows the circuit used to simulate it.

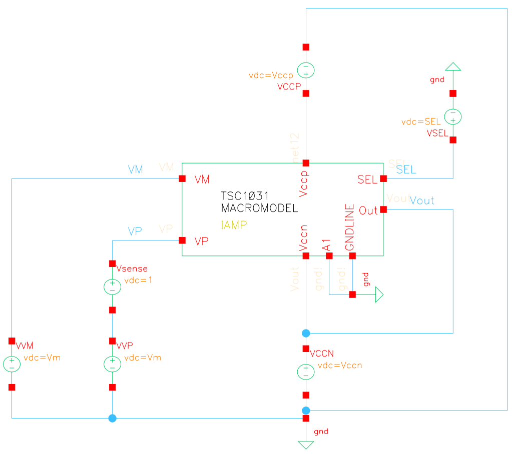


Figure 16: Isource short-circuit current: simulation schematic.

Follows the macromodel max source current simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Vsense=(Vp-Vm)=+1V and out connected to gnd:

| Macromodel | Datasheet (Typ.) |
|---|---|
| 26.08 mA | 26 mA |

Table 8: Isource (Max source current): macromodel simulations vs datasheet.

Fig. 17 shows I(Out), I(Vccp) and I(Vccn) varying Vcc in $[2.7V, 5.5V]$.

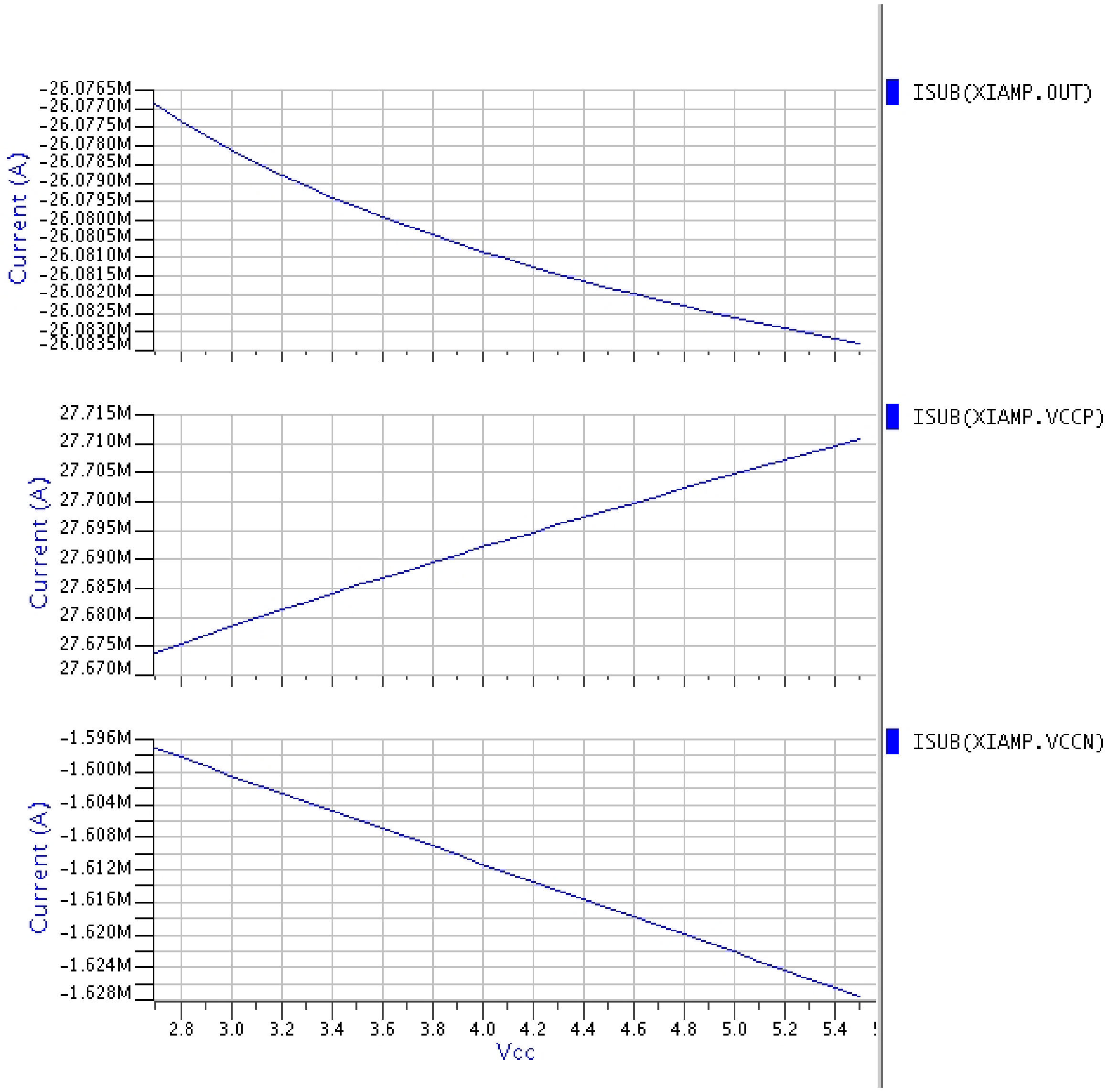


Figure 17: Isource short-circuit current: simulation results.

## 4.9 Isink short-circuit current

Fig. 18 shows the circuit used to simulate it.

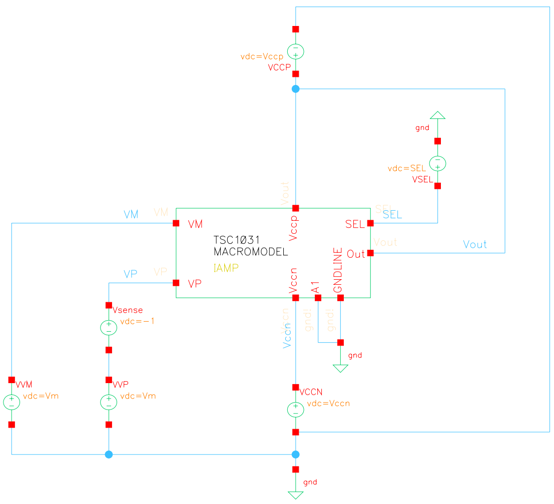


Figure 18: Isink short-circuit current: simulation schematic.

Follows the macromodel max sink current simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Vsense=(Vp-Vm)=-1V and out connected to Vcc:

| Macromodel | Datasheet (Typ.) |
|---|---|
| 26.08 mA | 26 mA |

Table 9: Isink (Max sink current): macromodel simulations vs datasheet.

Fig. 19 shows I(Out), I(Vccp) and I(Vccn) varying Vcc in $[2.7V, 5.5V]$.

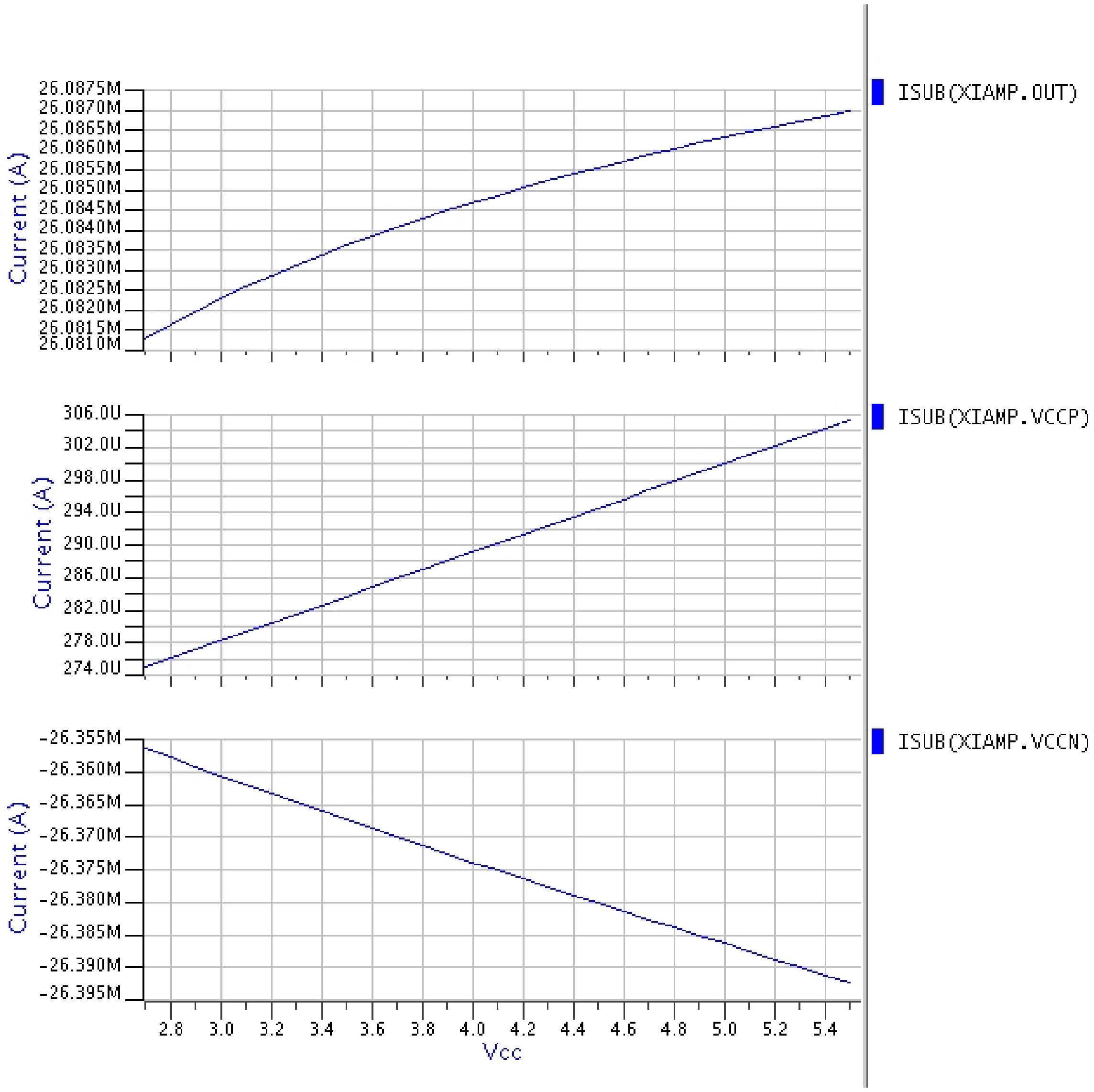


Figure 19: Isink short-circuit current: simulation results.

## 4.10 High level output voltage (Voh)

Fig. 20 shows the circuit used to simulate it.

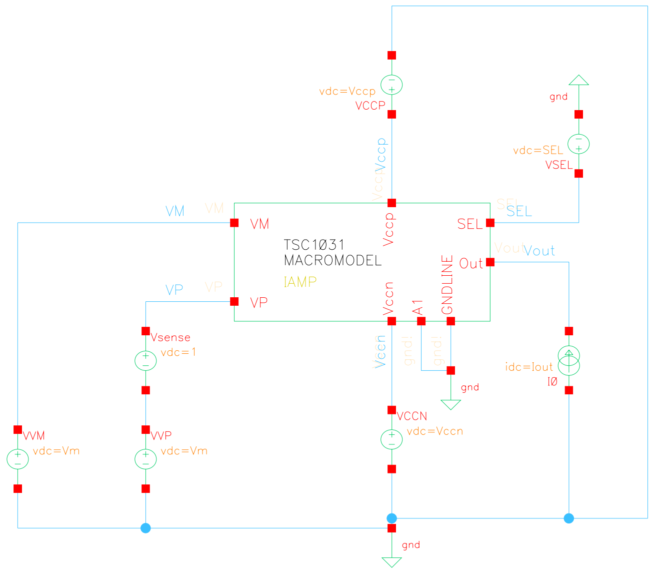


Figure 20: Voh (High level output voltage): simulation schematic.

Fig. 21 shows the macromodel output stage high-state saturation voltage (Voh) simulation, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Vsense=(Vp-Vm)=+1V and **varying Iout in** $[-10mA, +10mA]$ (negative Iout is a sourced Iout and positive Iout is a sinked Iout).

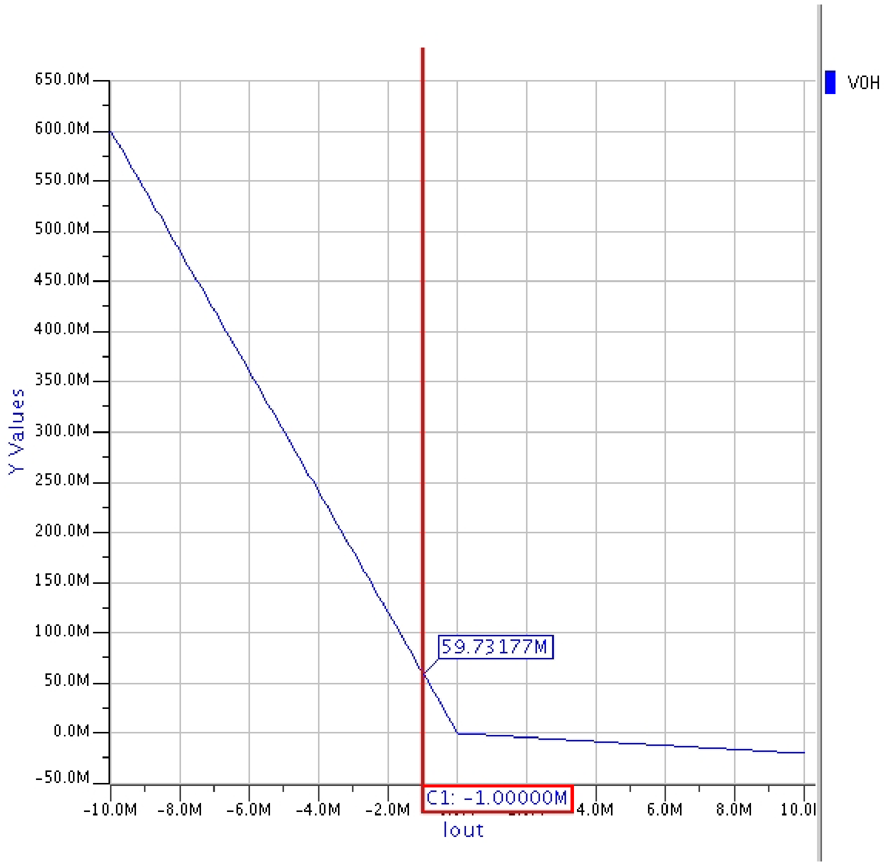


Figure 21: Voh vs Iout: macromodel simulation.

The following table 10 shows the output stage high-state saturation voltage (Voh) comparison among the macromodel and the datasheet typical value, at Iout_source=1mA:

| Macromodel | Datasheet |
|---|---|
| 59.7 mA | 60 mA |

Table 10: Output stage high-state saturation voltage (Voh), at Iout_source=1mA: macromodel simulation vs datasheet.

## 4.11 Low level output voltage (Vol)

Fig. 22 shows the circuit used to simulate it.

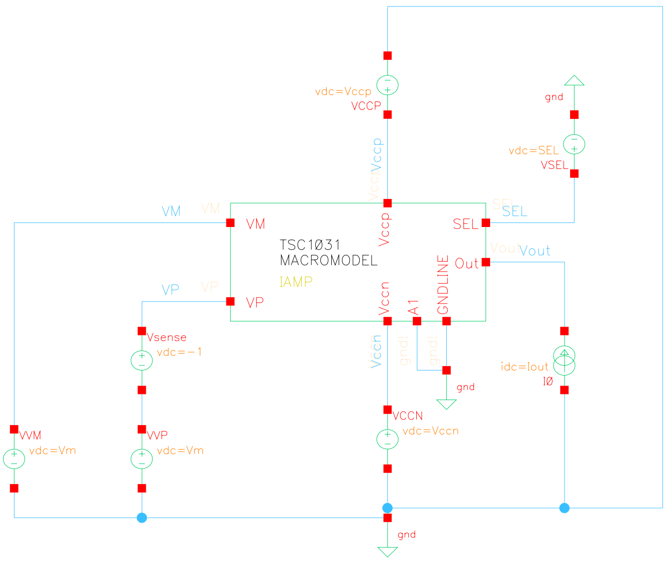


Figure 22: Vol (Low level output voltage): simulation schematic.

Fig. 23 shows the macromodel output stage low-state saturation voltage (Vol) simulation, considering the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Vsense=(Vp-Vm)=-1V and **varying Iout in** $[-10mA, +10mA]$ (negative Iout is a sourced Iout and positive Iout is a sinked Iout).

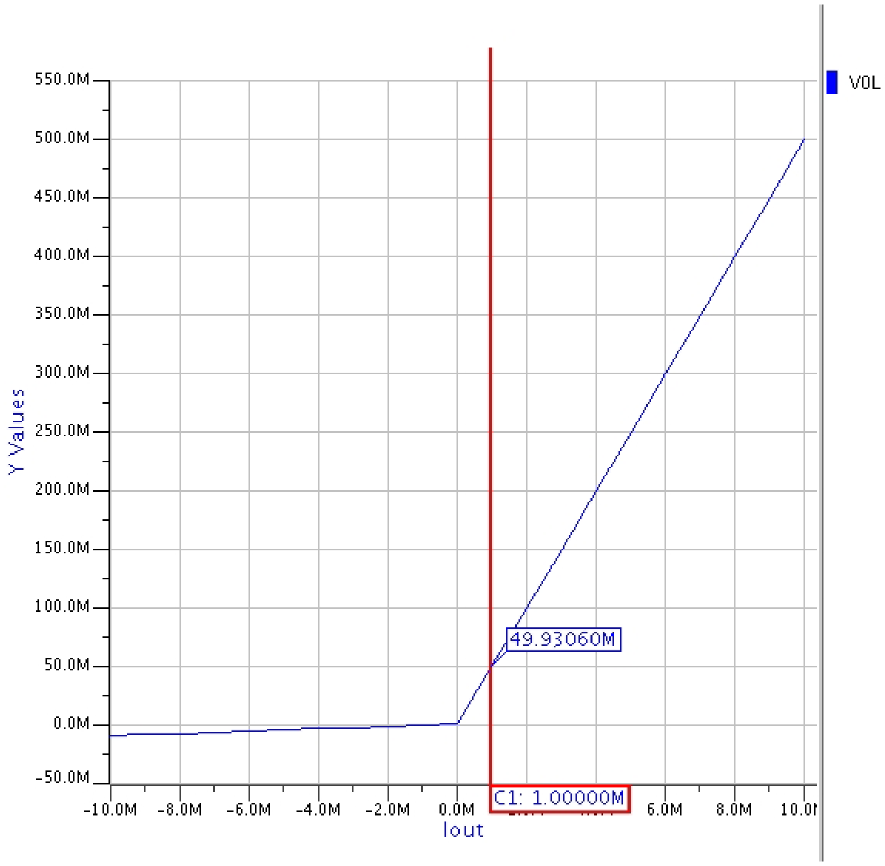


Figure 23: Vol vs Iout: macromodel simulation.

The following table 11 shows the output stage low-state saturation voltage (Vol) comparison among the macromodel and the datasheet typical value, at Iout_sink=1mA:

| Macromodel | Datasheet |
|---|---|
| 49.9 mA | 50 mA |

Table 11: Output stage low-state saturation voltage (Vol), at Iout_sink=1mA: macromodel simulation vs datasheet.

# 5 TRANSIENT simulations: macromodel behaviour

The macromodel matches the real current sensing TSC1031 transient behaviour: the following sections explain how the macromodel fits each transient specification.

## 5.1 Slew rate

Fig. 24 shows the circuit used to simulate it.

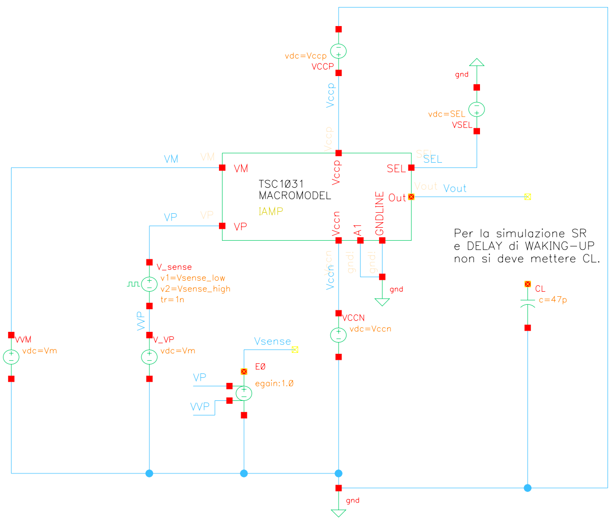


Figure 24: Slew rate: simulation schematic.

Table 12 shows the TSC1031 macromodel slew rate simulated in the same datasheet test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V and with an input step starting from Vsense_low=10mV to Vsense_high=100mV, both for Av=50 (SEl low) and Av=100 (SEL high).

Fig. 25 shows the entire TSC1031 macromodel step response.

The TSC1031 macromodel matchs well the datasheet slew rate specification .

| Macromodel | Datasheet (Typ.) |
|---|---|
| $0.9038V/\mu s$ | $0.9V/\mu s$ |

Table 12: Slew rate: macromodel simulation vs datasheet.

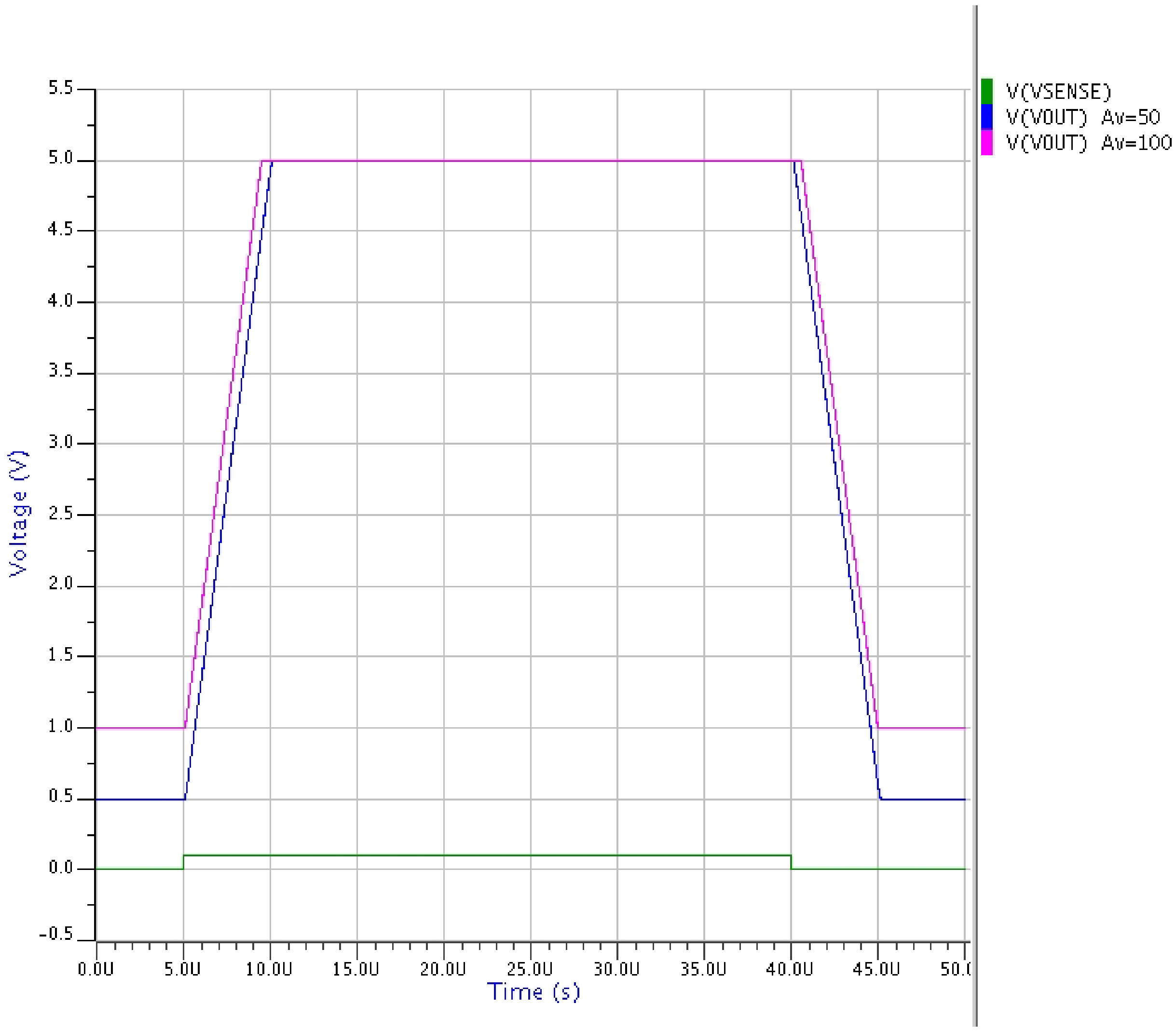


Figure 25: Slew rate: simulation results.

## 5.2 Waking-up effect

In the previous section 5.1 the TSC1031 output voltage isn't delayed respect to the input step stimulus, starting from Vsense_low=10mV to Vsense_high=100mV.

If this input step signal starts from a Vsense_low > 0 then the output voltage doesn't show any delay therefore the device is immediately ready to respond to the input step signal: instead if this input step signal starts from a Vsense_low <= 0 then the output voltage is delayed respect it; this effect is called waking-up.

The waking-up delay depend of the input overdrive voltage (Vsense_high value): the delay decreases increasing the input overdrive voltage.

The schematic shown in fig. 24 was simulated in the following test conditions: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Av=100 (SEL high) and with an input step starting from **Vsense_low= -1mV** to **Vsense_high** $\in$ **[2mV , 160mV]**. Fig.26 shows the entire TSC1031 macromodel output voltage response varying **Vsense_high** $\in$ **[2mV , 160mV]**.

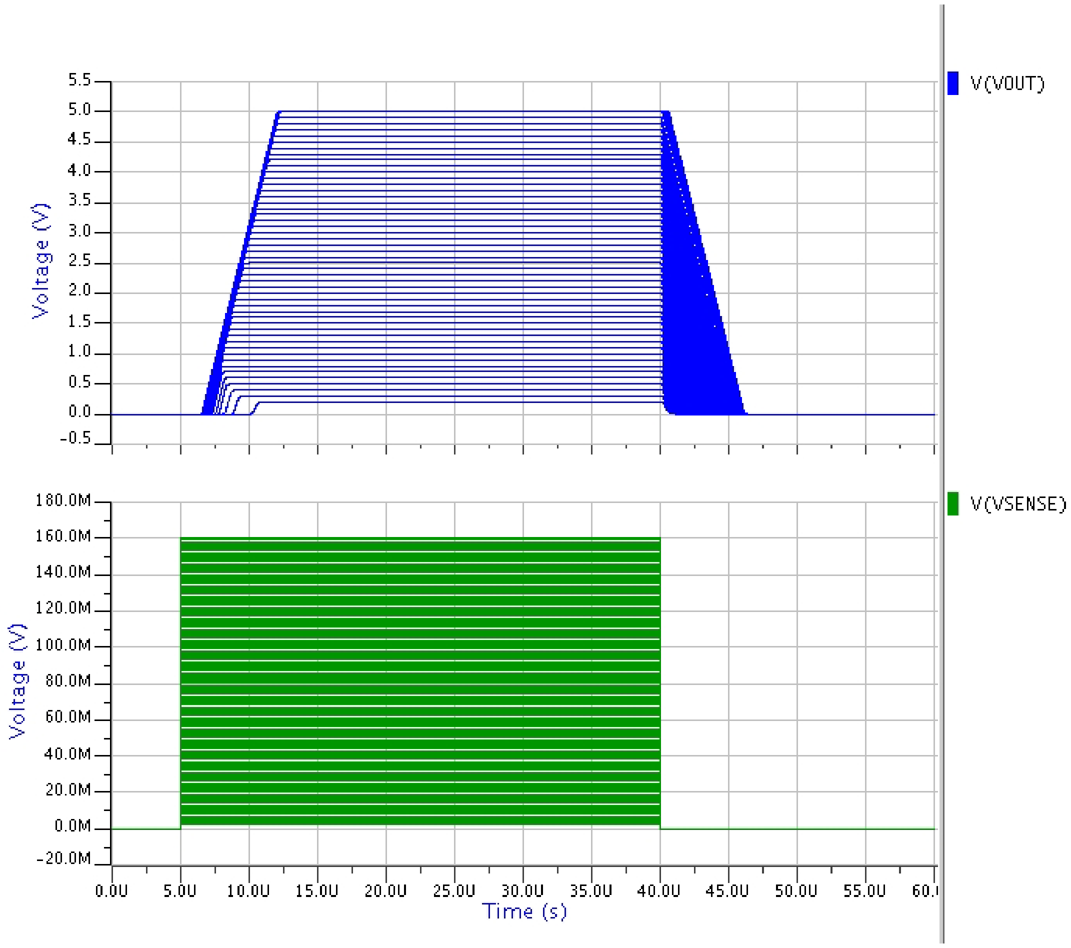


Figure 26: Waking-up, entire step response: simulation results.

Fig.27 shows the TSC1031 macromodel delay compared with the extracted one simulating the real TSC1031 designer netlist.

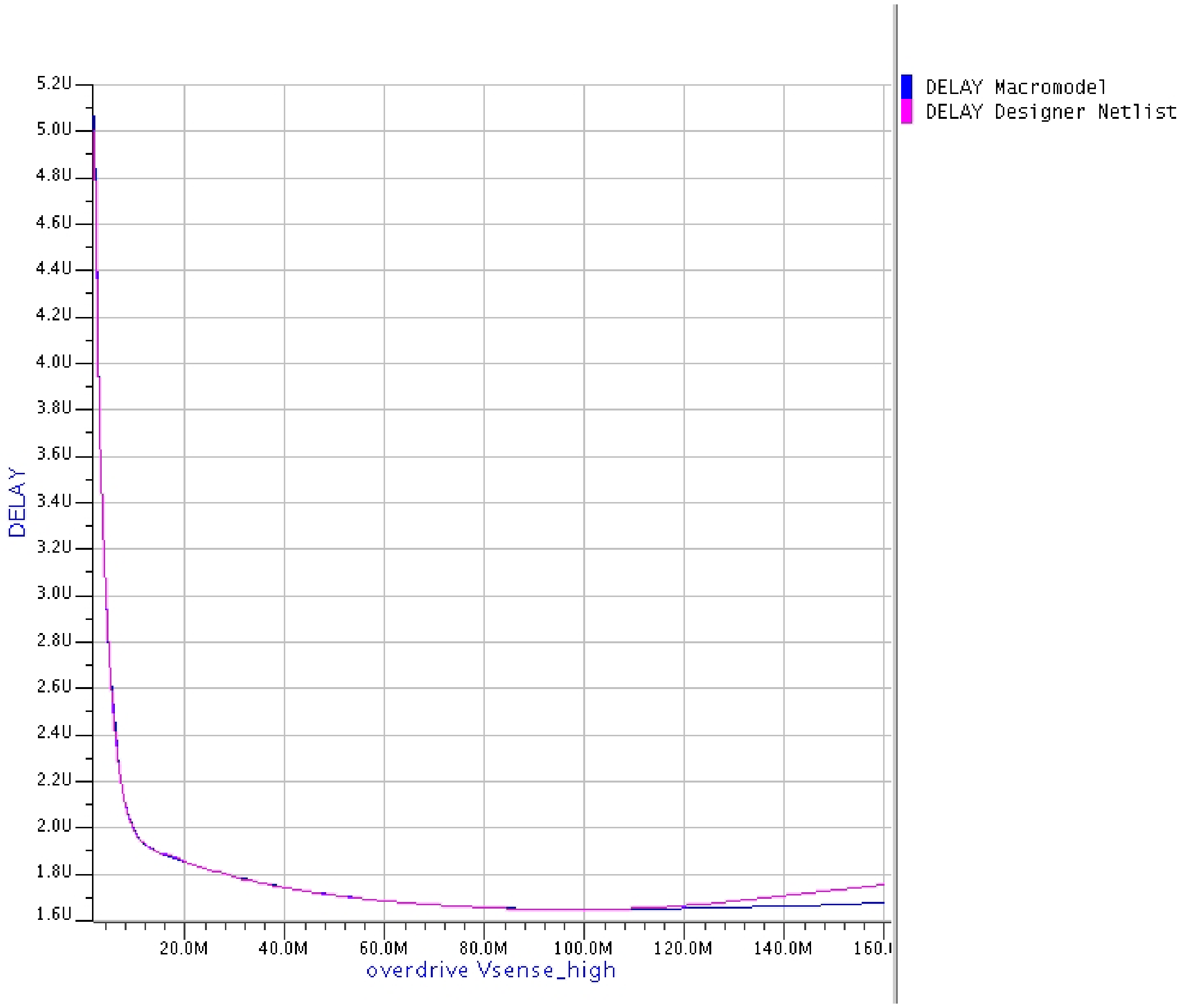


Figure 27: Waking-up, delay: TSC1031 macromodel simulation vs designer netlist simulation.

## 5.3 Gain selection transient

Fig. 28 shows the circuit used to simulate it.

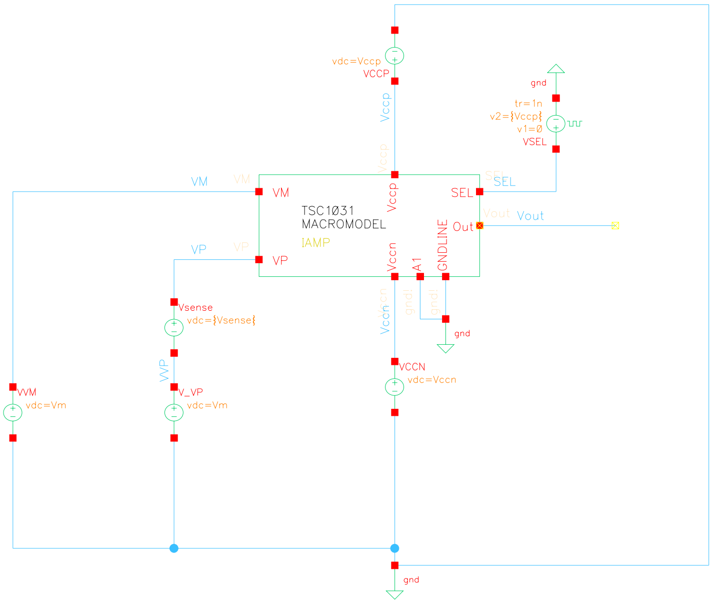


Figure 28: Gain change: simulation schematic.

The following test conditions were considered: $T_{amb} = 25^oC$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V, Vsense=50mV and with a pulse applied on the SEL pin switching from 0V (Av=50) to 5V (Av=100); Fig. 25 shows the pulse V(SEL), applied on the gain-select pin SEL, and the macromodel output voltage response V(OUT).

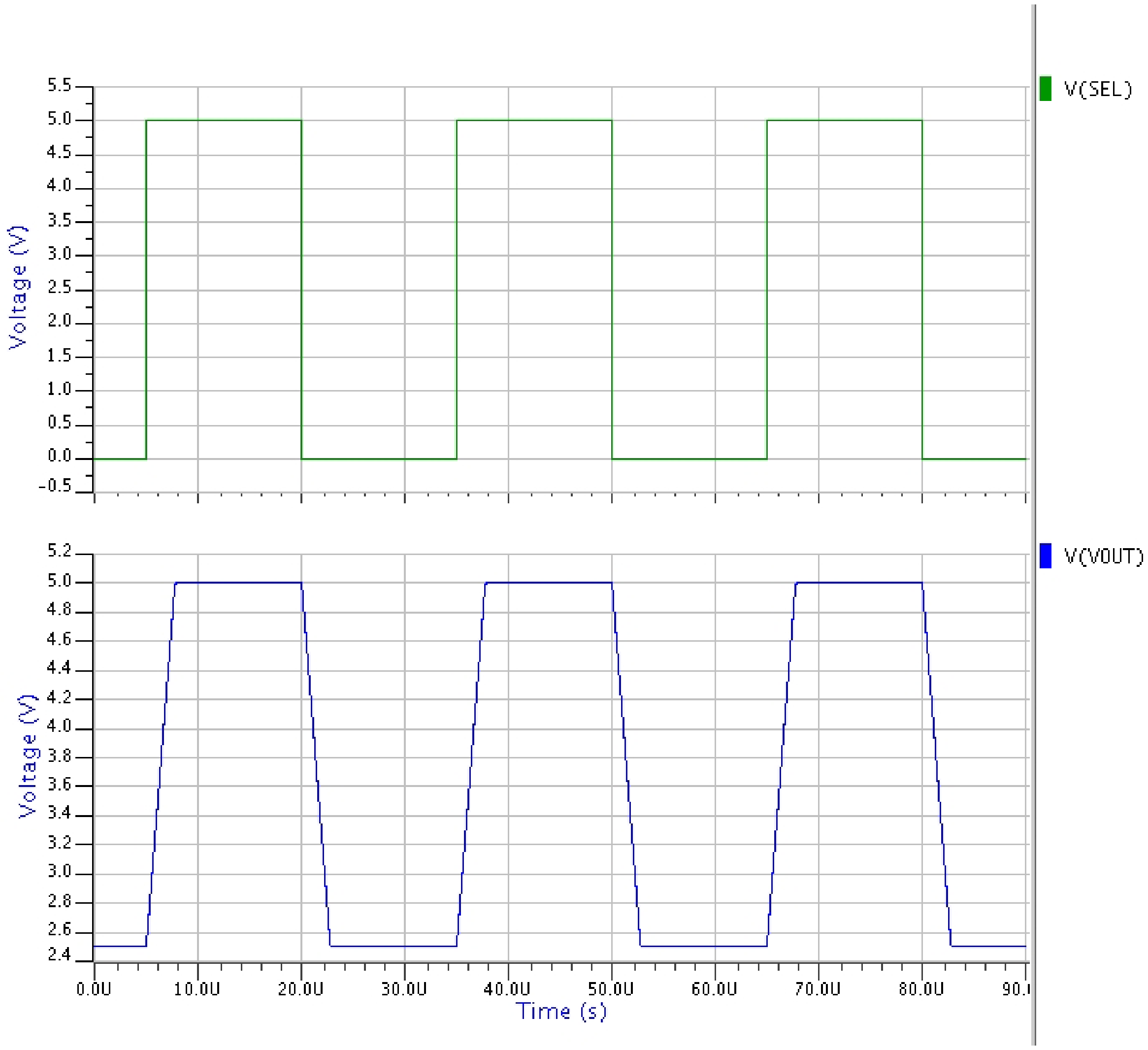


Figure 29: Gain selection transient: macromodel simulation.

# 6 AC simulations: macromodel behaviour

The macromodel matches the real current sensing TSC1031 AC behaviour: the following sections explain how the macromodel fits each AC specification.

## 6.1 AC open-loop response

Fig. 30 shows the circuit used to simulate the open-loop AC response:

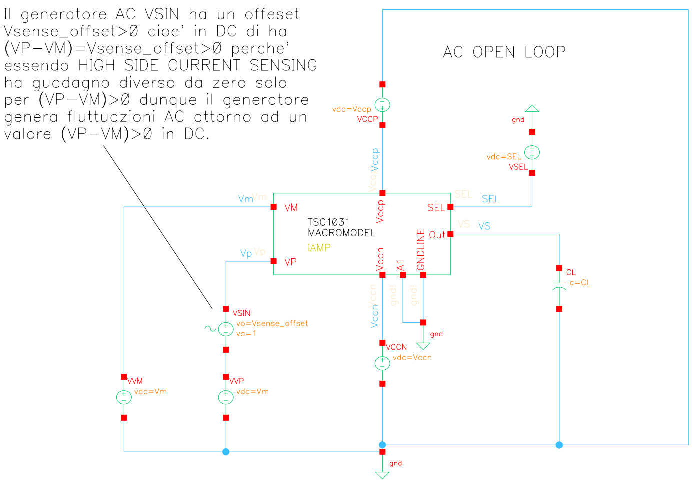


Figure 30: AC response in open-loop: simulation schematic.

Table 13 shows the TSC1031 macromodel 3dB bandwidth simulated in the same datasheet test conditions: $T_{amb} = 25^{o}C$, Vccp=Vcc=5V, Vccn=0 (single supply configuration), Vm=12V , Cload=47pF.

Fig. 31 shows the entire TSC1031 ac open loop response (mag and phase), for Av=100V/V and Vsense$_{dc}$=25mV, compared with the Designer netlist simulated one.

| Macromodel | Datasheet (Typ.) | Conditions |
|---|---|---|
| 800.3 | 800 | Av=50V/V , Vsense$_{dc}$=50mV |
| 800.3 | 800 | Av=100V/V , Vsense$_{dc}$=25mV |

Table 13: $BW_{3dB}$ (kHz): macromodel simulation vs datasheet.

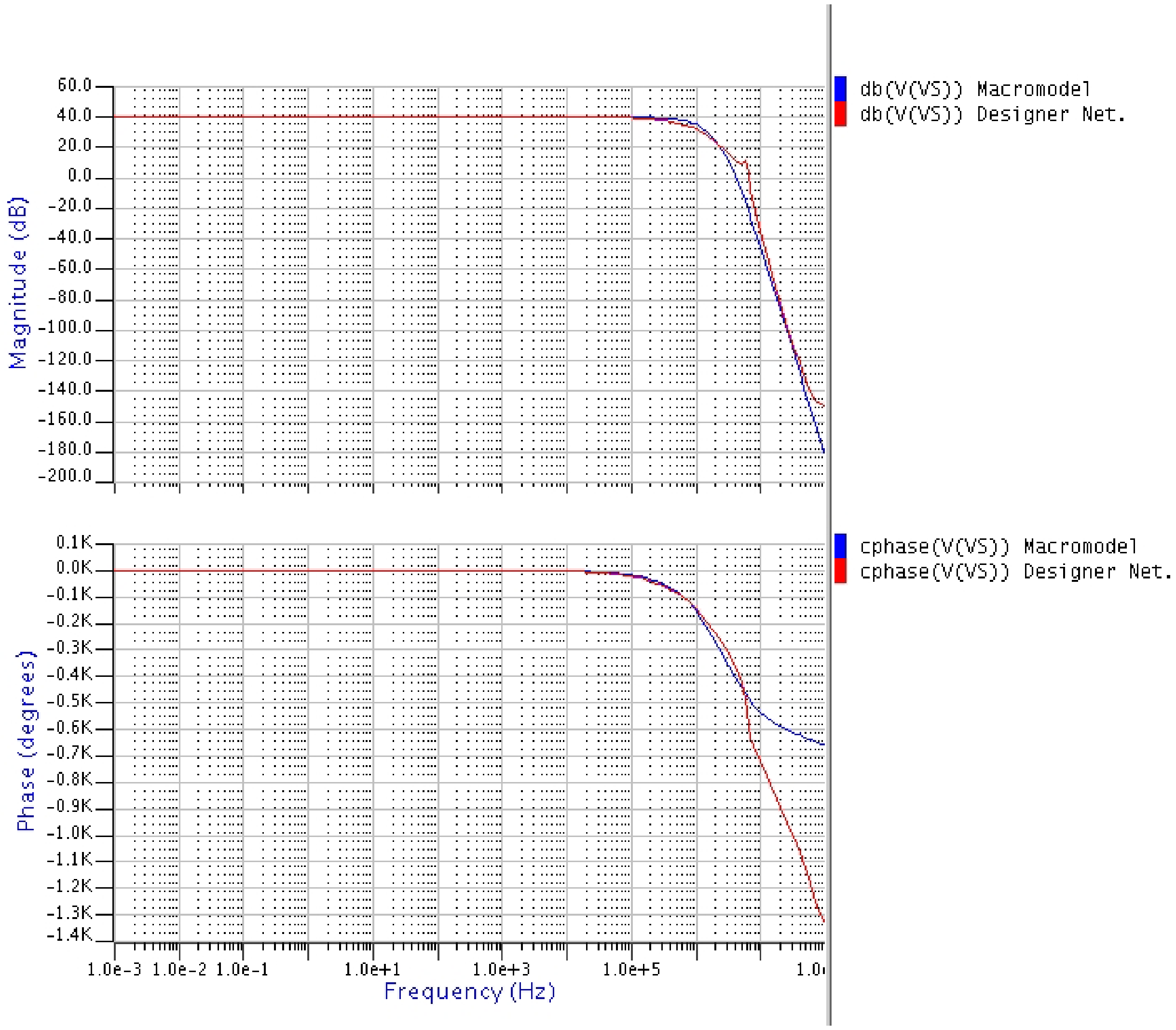


Figure 31: AC open loop response: TSC1031 macromodel simulation vs Designer Netlist simulation.

# 7 Conclusion

An analog macromodel, for Spice-like simulators, was implemented for TSC1031 high-voltage high side current sense amplifier, matching the datasheet DC, Transient and AC behaviour specifications: the macromodel guarantees the real design IP encryption and, containing a smaller number of non linear devices, allows faster simulations.

As shown in the previous sections, the implemented TSC1031 macromodel has a **good fitness** of the given DC, Transient and AC specifications datasheet and of the laboratory measures.

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