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FEATURED IN THIS EDITION

20 THERMAL MANAGEMENT OF CHIP-ON-BOARD LED SYSTEMS AND THEIR AGING RESPONSE TO CYCLIC POWER

26 SOLDER JOINT LIFETIME OF RAPIDLY CYCLED LED COMPONENTS

30 MECHANICAL CYCLING RELIABILITY TESTING OF TIMS DEVELOPED SPECIFICALLY FOR SEMICONDUCTOR TEST

6 *CALCULATION CORNER* APPLICATION OF TRANSIENT THERMAL METHODS TO MOISTURE DIFFUSION CALCULATIONS, PART I

12 *THERMAL FACTS & FAIRY TALES* FAIRY TALES ABOUT HEAT SINK PERFORMANCE CALCULATIONS

16 *STATISTICS CORNER* PROBABILITY

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CONTENTS

electronics COOLING
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2 EDITORIAL
Genevieve Martin

4 COOLING EVENTS
News of Upcoming 2020 Thermal Management Events

6 CALCULATION CORNER
Application of Transient Thermal Methods to Moisture Diffusion Calculations, Part I
Bruce Guenin

12 THERMAL FACTS & FAIRY TALES
Fairy Tales About Heat Sink Performance Calculations
Clemens J.M. Lasance

16 STATISTICS CORNER
Probability
Ross Wilcoxon

20 MECHANICAL CYCLING RELIABILITY TESTING OF TIMS DEVELOPED SPECIFICALLY FOR SEMICONDUCTOR TEST
David Saums, Tim Jensen, Carol Gowans, Ron Hunadi, Mohamad Abo Ras

26 THERMAL MANAGEMENT OF CHIP-ON-BOARD LED SYSTEMS AND THEIR AGING RESPONSE TO CYCLIC POWER
Lisa Mitterhuber, Julien Magnien, Elke Kraker

30 SOLDER JOINT LIFETIME OF RAPIDLY CYCLED LED COMPONENTS
Wendy Luiten

35 TECHNICAL EDITORS SPOTLIGHT

36 INDEX OF ADVERTISERS

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Lectrix
1000 Germantown Pike, F-2
Plymouth Meeting, PA 19462 USA
Phone: +1 484-688-0300; Fax:+1 484-688-0303
info@lectrixgroup.com
www.lectrixgroup.com

CHIEF EXECUTIVE OFFICER
Graham Kilshaw | Graham@lectrixgroup.com

VP OF MARKETING
Geoffrey Forman | Geoff@lectrixgroup.com

EDITORIAL DIRECTOR
Jennifer Arroyo | Jennifer@lectrixgroup.com

CREATIVE DIRECTOR
Chris Bower | Chris@lectrixgroup.com

BUSINESS DEVELOPMENT DIRECTOR
Janet Ward | Jan@lectrixgroup.com

BUSINESS DEVELOPMENT DIRECTOR
Mark Pantalone | Mark@lectrixgroup.com

PRODUCTION COORDINATOR
Jessica Stewart | Jessica@lectrixgroup.com

LEAD GRAPHIC DESIGNER
Kristen Tully | Kristen@lectrixgroup.com

CONTENT MARKETING MANAGER
Danielle Cantor | Danielle@lectrixgroup.com

ADMINISTRATIVE MANAGER
Eileen Ambler | Eileen@lectrixgroup.com

ACCOUNTING ASSISTANT
Susan Kavetski | Susan@lectrixgroup.com

EDITORIAL BOARD

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Signify
genevieve.martin@signify.com

Victor Chiriac, PhD, ASME Fellow
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Global Cooling Technology Group
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EDITORIAL

Genevieve Martin
Contributing Author

An open letter to our community and devoted readers: What is our future perspective on electronics cooling?

It is my privilege to write this editorial for two reasons: first, it's a celebration of our entering this new decade and secondly, it's my first editorial in this prestigious magazine. I am very honored to join the board of technical editors. *Electronics Cooling®* has grown in influence within the community over the years, and is recognized as the premium magazine in the field of electronics cooling and thermal management of electronics systems with articles authored by international experts. It is a great pleasure for me to become part of this family.

Let me introduce myself. I have been involved in the field of thermal management and cooling of electronics, primarily at the product system level, for more than two decades. I have been working in different application areas: consumer, professional and non-professional healthcare products, and lighting. Besides my work as thermal expert, my key work focus has always been on finding faster ways to design product range architectures, and also finding ways to work seamlessly with related fields like e.g. EMC, acoustic noise, optics, and electronics. For the last three years, I have coordinated the European project Delphi4LED, dealing with the very first model creation of an LED digital twin*. We have successfully managed to integrate, within a single model, a multi-domain (thermal-optical-electrical) digital representation that encompasses the die, package, and product use levels. In addition to my role as an expert in the field, at Signify (formerly Philips Lighting), I lead the thermal management and mechanics worldwide competence and also head a team of technology experts.

In this editorial, I would like to take the opportunity to raise the question of the role of the thermal expert in industry. During my career, I have seen the constant struggle over the role of the thermal management expert confirmed during discussions with other professionals. Thermal management has become a "commodity" in the industry context; oftentimes, thermal design is shifted to the mechanical designers or those with other expertise. Without good in-depth knowledge, the outcome can be disastrous; potential consequences of poor designs can include early failures of products, in terms of reliability or performance. This can result in the involvement of thermal management experts at the end of the design process, where opportunities for design changes are limited or resulting in high cost. Despite years of education of the community at large, this still happens nowadays in industry.

In brief, we all recognize that the thermal management essentially is managing waste, with all other domains considered as primary functions. However, we also know that our field remains important to fulfill performance, safety, reliability, and lifetime of products. There is hope. What new trends are making us stay relevant? With the advent of digital manufacturing, digital industry (production 4.E, Industry 4.0), I believe that our expertise is well equipped to embrace and integrate this new knowledge in early phases of product development. The growing digitalization of our competence over the past decades and our virtual prototyping capabilities give us some advantages compared to other domains. In addition, virtual prototyping without validation is non-viable. Therefore, we need to continue developing more efficient ways of characterization and measurements to feed our models.

From a collaboration perspective, we are well-positioned since our expertise has always required electronics cooling designers to work closely with those providing key functions, forcing us to understand the needs of those in other areas of expertise and translate their needs into the right inputs as well as communicate our results back to them in their "language".

Next, I'll speak to knowledge sharing to advance our community. Communicating new ideas and results at the leading edge of science is an important part of the scientific process and it is my goal to continue with the rest of the *Electronics Cooling®* team to bring forward new topics and enable greater visibility of high-quality research at the international level. International scientific sharing is the key to pursue high-level and world-class science research. In this regard, *Electronics Cooling®* benefits from all of your scientific contributions and the excellence that the international community has built since more than four decades. All our published articles are carefully reviewed to provide you with the best possible quality of content.

This is also our role and duty to educate and motivate the young researchers, scientists, and engineers to think differently in order to shape the future landscape of our competence field. I therefore invite you to contact us if you have suggestions regarding topics you want to share or read in upcoming issues.

I wish all of you a lot of reading pleasure for the coming year.

– Genevieve Martin

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COOLING EVENTS

News of Upcoming 2020 Thermal Management Events

EUROSIME

Vienna House Andel's, Cracow, Poland

International Conference on Thermal, Mechanical, and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems.

Desc. source: electronics-cooling.com

► www.eurosime.org

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Desc. source: electronics-cooling.com

► www.imaps.org/thermal/

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► www.thermal.live

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Desc. source: electronics-cooling.com
► www.ieee-itherm.net/itherm/conference/home

ADVANCEMENTS IN THERMAL MANAGEMENT

Hilton Denver City Center, Denver, CO, USA

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Desc. source: electronics-cooling.com
► www.thermalconference.com/conference

THERMINIC 2020

Fraunhofer Center, Berlin, Germany

26th International Workshop – Thermal Investigations of ICs and Systems.

Desc. source: electronics-cooling.com
► www.therminic2020.eu/

THERMAL MANAGEMENT SYSTEMS SYMPOSIUM

Sheraton Mesa Hotel, Mesa, AZ, USA

The Thermal Management Systems Symposium, organized by the SAE International will take place from October 6-8, 2020 in Mesa, United States Of America. The conference will cover areas like Mobile air conditioning systems, require new concepts to provide passenger compartment heating and cooling as well as heating and cooling of batteries and cooling of vehicle fuel systems.

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► www.10times.com/thermal-management-systems-mesa

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Online Event

THERMAL LIVE 2020 is a Free "online" learning and networking event for engineers to learn about the latest topics in thermal management. Produced by *Electronic Cooling®*, it showcases the newest techniques and products in the industry.

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Application of Transient Thermal Methods to Moisture Diffusion Calculations, Part I

Reprinted from the *Electronics Cooling*® 2012, Winter Issue

Bruce Guenin
Assoc. Technical Editor

INTRODUCTION

Many of the components currently used in electronics systems employ organic materials. Under certain circumstances, the diffusion of moisture into electronic components can lead to problems in the electrical performance and overall reliability of these components. Examples are the increase in the attenuation of high frequency signals in printed circuit boards and package substrates [1], reduction in optical fiber mechanical strength [2], and popcorn failure of organic packages during soldering operations[3].

On occasion, it is necessary to predict the rate of diffusion of moisture in organic materials in order to successfully manage these technical issues. The expertise for performing these calculations is often a rare commodity in engineering organizations. However, analogies between heat flow and moisture diffusion can be leveraged to allow the thermal engineer to perform accurate diffusion calculations by appropriately adapting more familiar thermal methods[4].

This article provides a procedure for quantifying moisture diffusion using a method, developed in a previous column, for the analysis of thermal transient problems involving the numerical solution of a multi-stage resistor-capacitor (RC) circuit [5,6].

MOISTURE DIFFUSION EXAMPLES

There are many situations in which the diffusion of moisture occurs in organic materials used in electronics hardware. Some are intentional such as: exposure to elevated temperature/humidity in conjunction with reliability or performance testing; and bake out procedures intended to promote the removal of moisture from components to avoid moisture-induced failures. Other exposures may occur in the field, while equipment is being stored in humid environments. Lastly, elevated temperatures resulting from equipment operation will reduce the moisture content of electronic components. In all of these cases it is important to be able to calculate the rate of moisture diffusion, both into and out of the components of interest and to determine the moisture concentration at any time during the exposure.

Part 1 of this article deals with a simple one-dimensional moisture diffusion situation at a constant temperature, that can be applied to many situations of interest. Part 2 will deal with a 2D moisture flow situation encountered in laminate semiconductor packages, both at a uniform temperature and under a thermal gradient resulting from the self-heating of the package.

CALCULATION METHOD

The basic equations governing heat flow and diffusion presented are indicated below. *Equation 1* is commonly referred to as Fourier's heat equation and *Equation 2* as Fick's first Law of diffusion.

$$\vec{q} = -k\nabla T \tag{1}$$

$$\vec{J} = -D\nabla Conc \tag{2}$$

In each case, the magnitude of a vector field (the flowing entity: thermal energy, q, or the mass flux of the diffusing substance, J, is determined by the product of the gradient of a scalar field (temperature, T, or concentration, Conc) and a rate-limiting parameter (thermal conductivity, k, or diffusion coefficient, D). [Author's note: a common symbol for concentration is C. In this article, the non-standard symbol, Conc, is used to represent concentration, since the symbol C has already been appropriated in this series of articles to mean capacitance.] When calculating either transient heat flow or mass flow using an RC circuit, the resistance is calculated using an appropriate equation containing the thermal conductivity or diffusivity and appropriate terms representing the geometry. The capacitance is equal to the heat capacity in the case of the thermal problem. For the diffusion problem, it is simply the volume of the component or region of interest. These analogies between heat flow and mass diffusion are summarized in *Table 1*, which also includes those governing electron flow.

<table>
<tr><th colspan="4">Table 1. Electrical - Thermal - Diffusion Analogy</th></tr>
<tr><td>Eqn Name</td><td>Ohm's Law</td><td>Fourier's Law</td><td>Fick's 1st Law</td></tr>
<tr><td>Entity Flowing</td><td>Elec Charge</td><td>Heat Energy</td><td>Mass of Moisture</td></tr>
<tr><td>Potential: to drive flow</td><td>Voltage</td><td>Temperature</td><td>Moisture Conc</td></tr>
<tr><td>Rate-limiting Mat Prop</td><td>Electrical Cond.</td><td>Thermal Cond.</td><td>Diffusion Coef.</td></tr>
<tr><td>C Lumped Element</td><td>Capacitance</td><td>Heat Capacity</td><td>Volume</td></tr>
<tr><td rowspan="2">R Lumped Element</td><td colspan="3">Function of geometry and</td></tr>
<tr><td>Electrical Cond.</td><td>Thermal Cond.</td><td>Diffusion Coef.</td></tr>
</table>

In a recent installment of this column, a numerical solution of a multi-stage RC circuit was described and applied to the thermal analysis of a high-power chip in thermal contact with a heat sink [5, 6]. This method can be applied directly to the diffusion problem, with appropriately calculated values of R and C.

The RC circuit assumed for the current calculations is presented in *Figure 1*. It is a four-stage RC circuit, representing moisture flow from an external surface, represented by node 0, and flowing in a series fashion through four successive regions. The fourth node is an internal one and is not directly connected to the environment. These regions can be parts of a single component or material, or they can be different materials.

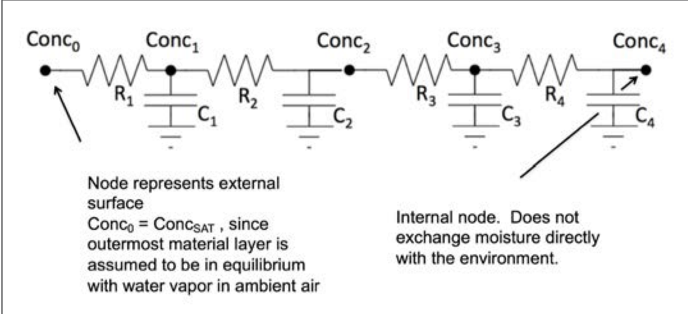


Figure 1: Four-stage transient RC circuit representing the diffusion process.

Figure 2 illustrates the operation of the numerical model, within a given time step, at a single stage in the circuit, in partitioning the incoming mass of moisture, M_{IN}, into a portion flowing into capacitor C_i and a portion flowing through R_i into the adjacent node i+1. A detailed description of the numerical method, along with recipe for implementing it in a spreadsheet are found in Reference [5].

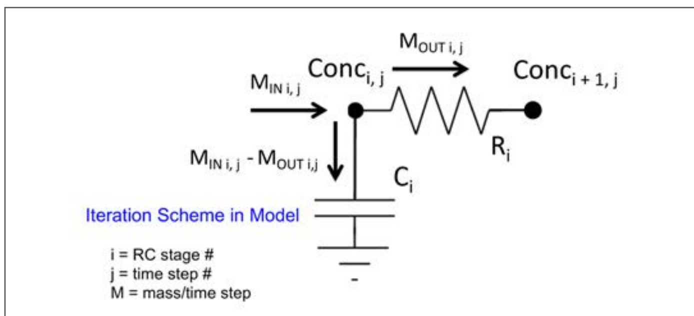


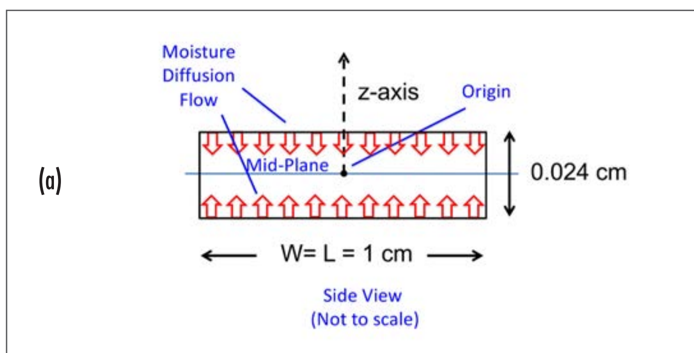
Figure 2: Single stage in RC network illustrating mass transfer in a single time step of the numerical model.

MODEL ASSUMPTIONS

Figure 3 depicts a common situation encountered in diffusion problems: a slab of homogeneous material in which moisture diffuses from the top and bottom surfaces toward the mid-plane. Diffusion from the edges is neglected, due to their much smaller surface area. The material is assumed to be BT (bismaleimide triazine), a dielectric material commonly used in laminate semiconductor packages.

Two different environmental exposures are assumed: 1) 85˚C/85% RH "soak" and 2) 105˚C "bakeout." In each case, the process is allowed to continue to completion; i.e.: the soak process achieves the saturation concentration of moisture throughout the sample and the bakeout process drives all moisture from the sample.

The sample thickness is somewhat arbitrary, but is representative of that for a single layer of a package laminate.



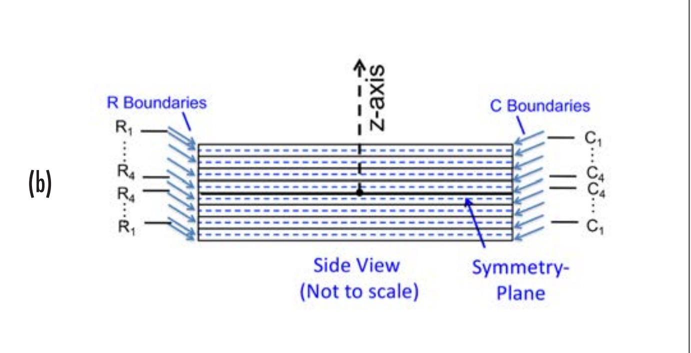


Figure 3: (a) Diagram of diffusion sample b) Diagram of boundaries for capacitor regions (solid lines) and resistor regions (dotted lines). Equations shown, for calculating R and C values, representing 1D diffusion.

DIFFUSION PROPERTIES

Two material properties are needed to perform diffusion calculations: the diffusion coefficient, D, and the saturated concentration of moisture ($Conc_{SAT}$). $Conc_{SAT}$ represents an upper limit for the moisture content of a particular organic material at given values of T and RH. These properties for the soak conditions were obtained from the literature [7]. To obtain a value for D at 105˚C for BT, it was necessary to calculate the activation energy, based on data from this reference taken at 50˚C and 85˚C, and extrapolate the data to 105˚C. The following equation relates the diffusion coefficient to the activation energy, U, where T is the absolute temperature and k equals Boltzmann's constant.

$$D = D_0 \bullet e^{\left(-U/kT\right)} \qquad (3)$$

Because of the functional form of this equation, log(D) is a linear function of 1/T, with the slope proportional to U.

An activation energy equal to 0.48 eV was derived from a best-fit

process. This method has been previously applied to the analysis of diffusion constants for epoxy molding compound [8]. *Figure 4* displays the resulting graph. Given the fact that diffusion coefficient data may not be available at the particular temperature(s) of interest, this method could be very valuable in deriving values of D at the required temperatures. [Note: the reader should be aware of the sensitivity of the resultant value of D to errors in calculating the activation energy when applying this equation, due to its non-linear nature A ±2% error in the activation energy will yield a ±30% error in D.]

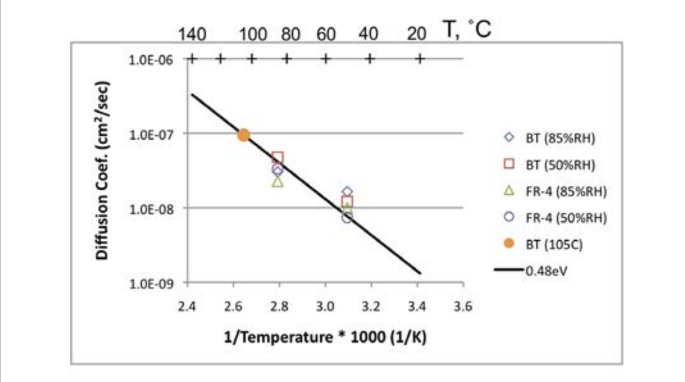


Figure 4: Plot of diffusion coefficient values versus 1/Temperature, on log-log scale. Line is fitted through data to predict diffusion coefficient at 105˚C.

Reference [7] is also valuable in this regard, since it provides values of $Conc_{SAT}$ for a number of organic materials commonly used in laminate and PCB fabrication over a range of values of T and RH. Reference [9] provides moisture-related data for a wide variety of polymeric materials.

Reference [7] also provides a value for percent of moisture, by weight, equal to 0.5%, for a BT sample after saturation at 85˚C/85% RH. This is transformed into $Conc_{SAT}$, the chosen parameter for this calculation, by multiplying it by the mass density of BT. The $Conc_{SAT}$ for the 105˚C condition was set at 0. The rationale for this choice was that the typical bakeout oven is open to the atmosphere. The partial pressure of water vapor at moderate levels of RH in the room containing the oven represents less than 1% RH at 105˚C. *Table 2* summarizes the material properties used in the subsequent calculations.

Table 2. Material Properties						
Material	Temperature	Relative Humidity	Density	H2O Conc. Sat.		Diffusion Coef
	(˚C)	(%)	gm/cm3	(Wt. %)	mg/cm3	cm2/sec
BT	20	N/A	1.77	N/A	N/A	N/A
	85	85	N/A	0.5%	8.85	3.03E-08
	105	0	N/A	0	0	9.44E-08

CALCULATION OF R AND C VALUES

When the transient thermal method in References [5] and [6] was applied to a chip + package + heat sink configuration, the physical model was composed of distinct components made of differing materials. Consequently the partitioning of the physical model into discrete R and C regions was rather straightforward. The present example differs from this earlier one since it consists of a single material.

The method used in the current problem is as follows.

- Since there is a symmetry plane at z = 0, it is only necessary to solve for one half of the model. Due to symmetry, this solution applies to both halves.
- Divide each half-model into four separate cuboidal C regions of equal volume. The thickness of of each cuboid is equal to 1/8 times the total sample thickness = 1/8 x 0.024 = 0.003 cm.
- The R regions are assumed to connect the centroid plane of each C region to that of its neighbor. Hence, the Δz value associated with each of these resistances would be 0.003 cm. The one exception is for the resistance between outermost C region (C1) and the exterior surface. In this case, the Δz value (for R1) would be 0.0015 cm.

The spatial boundaries of the different R and C regions are illustrated in *Figure 3b*. The figure also indicates the formulas for calculating the R and C values for a 1-D diffusion situation. *Table 3* provides the dimensions of each region and the calculated values of R and C based on the appropriate value of D and the specified geometry.

Table 3. Calculated Values of R and C							
Lumped Element	Δz	Area	Temperature	Relative Humidity	D	R	C
	(cm)	(cm2)	(˚C)	(%)	cm2/sec	sec/cm3	cm3
R1	0.0015	1	85	85	3.03E-08	4.95E+04	N/A
R2, R3, R4	0.003	1			3.03E-08	9.90E+04	
R1	0.0015	1	105	0	9.44E-08	1.59E+04	
R2, R3, R4	0.003	1			9.44E-08	3.18E+04	
C1, C2, C3, C4	0.003	1	N/A	N/A	N/A	N/A	0.003

DIFFUSION SIMULATION RESULTS

Figure 5 displays four graphs illustrating various aspects of the transient moisture behavior of the sample as it is transferred from a dry environment into the 85˚C/85% RH soak environment. *Figure 5a* plots the value of the moisture concentration in each of the four C regions. Region C1, representing the outermost region, responds most quickly. Conversely, region C4, associated with the innermost region, adjoining the symmetry plane, is the slowest to respond. *Figure 5b* plots each value of moisture concentration calculated as various values of elapsed time versus the z location of the centroid of each C region. Results for all regions of the sample, both above and below the symmetry plane are plotted to assist visualization of the 2D moisture concentration profile. It illustrates the time lag involved with the center region of the sample ultimately achieving moisture equilibrium with its environment.

Figure 5c plots the total mass of absorbed moisture versus time. It is calculated using the following equation. The prefactor of two results from the half-symmetry of the model.

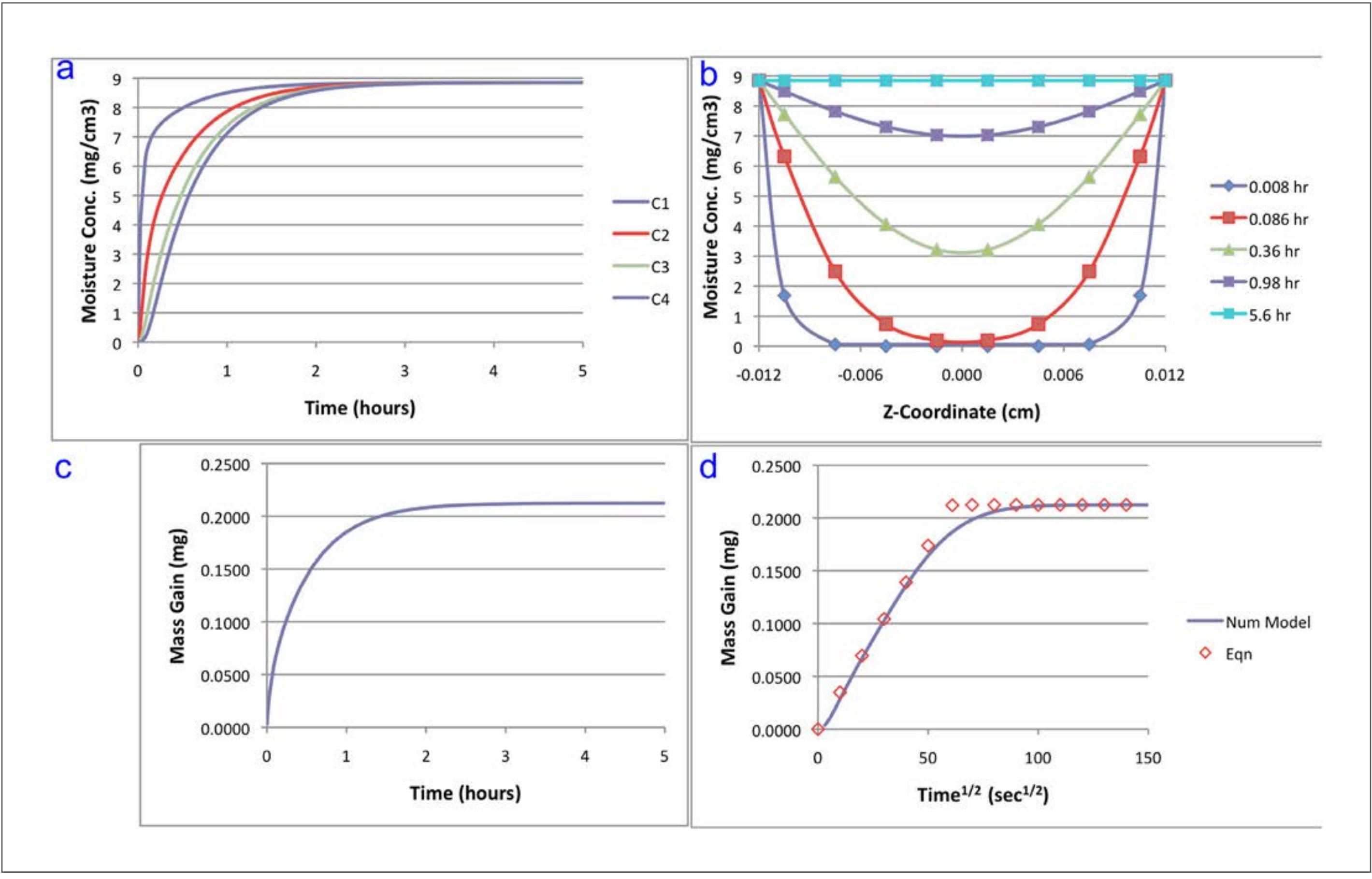


Figure 5: Solution results for BT sample, 85˚C/85% RH soak exposure. a) Concentration values at each capacitor. b) 2-D diffusion profile versus time. c) Mass gain curve, linear time scale. d) Mass gain curve versus time 1/2.

$$M_{H_2O} = 2 \bullet \sum_{i=1}^{4} Conc_i \bullet C_i \quad (4)$$

The shape of the M_{H2O} vs time curve is that expected in a soak situation. Its time constant (time to reach 63% of the saturated value) is 0.42 hours.

Finally, *Figure 5d* plots the total mass of absorbed moisture versus time$^{1/2}$. This is a useful way of plotting diffusion data since the slope of the M_{H2O} vs time$^{1/2}$ is a constant in the initial part of the diffusion transient. This behavior is quantified in *Equation 5*,

$$M_{H_2O} = k \bullet t^{1/2}, where\ k = \frac{4M_{SAT}}{l}\left(\frac{\pi}{D}\right)^{1/2} \quad (5)$$

where l is the thickness of the sample, which is assumed to be exposed to moisture from two opposing sides [6].

The symbols in *Figure 5d* for values < M_{SAT} are generated using the above equation. This serves as a validation of the numerical procedure. Also, it serves as an analytical method for approximating the M_{H2O} vs time curve it simple situations such as this, not requiring the precision of the numerical model.

The corresponding curves for the bake environment are shown in *Figure 6*. The sample is assumed to have been fully saturated with moisture from the 85˚C/85% RH at the moment it is placed into the bakeout oven at 125˚C. Qualitatively, the moisture versus time curves are the inverse of those in *Figure 5*. Quantitatively, however, the time constant for the bake process is approximately one-third of that in the soak process and is equal to 0.14 hour. This is due to the fact that at 125˚C, D is approximately three times its value at 85˚C. *Figure 6b* indicates, as before, that the moisture concentration at the center of the sample lags considerably behind the outer regions in equilibrating with the new, dry environment. The predicted curve in *Figure 6d* shows good agreement with the symbols, whose M_{H2O} values were calculated using *Equation 4* at the higher value of D, and where the slope was assigned a negative sign.

COMMENTS REGARDING THE GENERALITY OF THIS METHOD

The method presented here has been applied to a situation that could have been handled readily using purely analytical methods [2, 7, and 8]. The rationale for doing so was to use a simple example for demonstrating the method clearly and to be able to use the accompanying analytical solution to validate the numerical model.

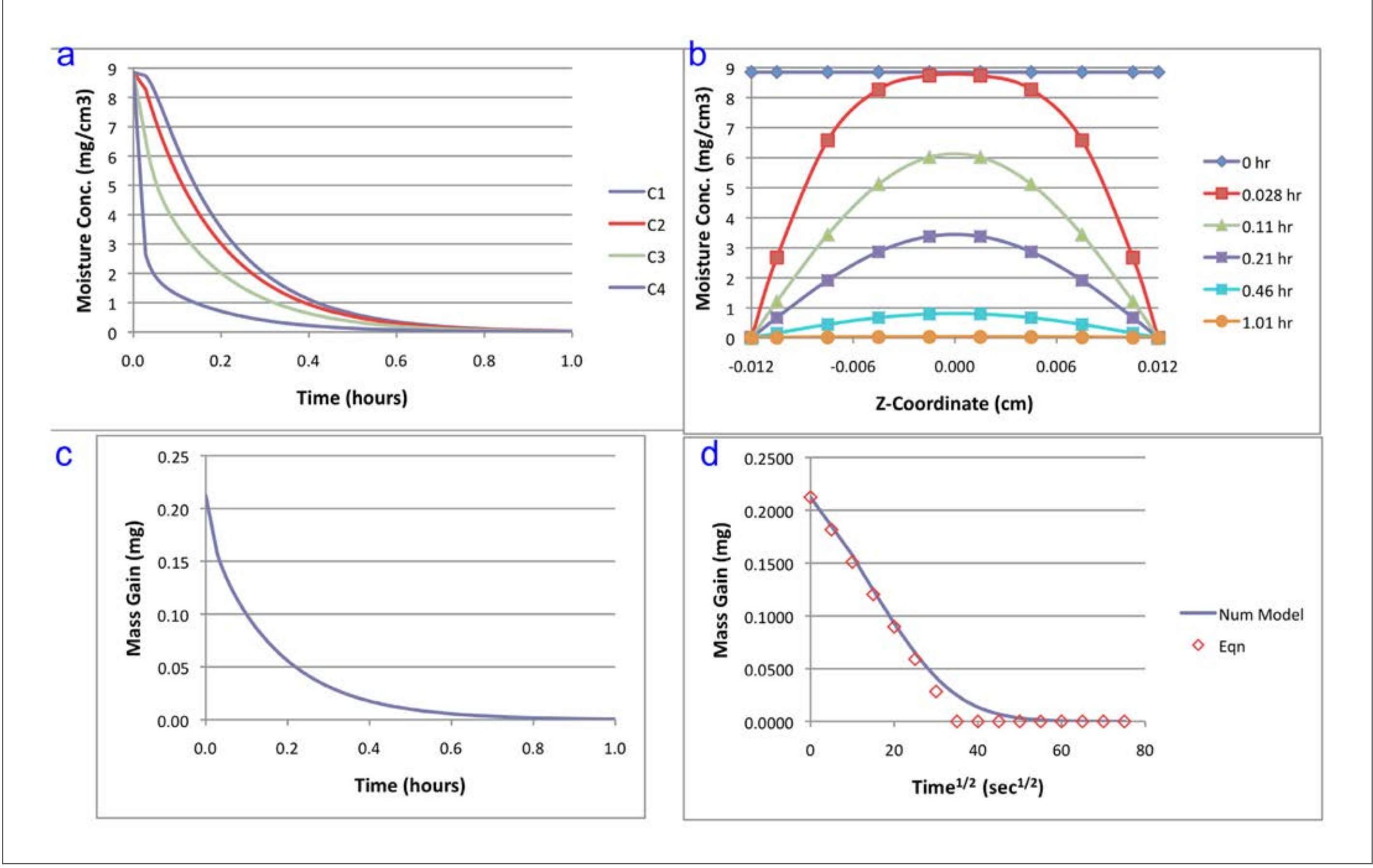


Figure 6: Solution results for BT sample, 105˚C/0% RH bake exposure. a) Concentration values at each capacitor. b) 2-D diffusion profile versus time. c) Mass gain curve, linear time scale. d) Mass gain curve versus time1/2.

The RC circuit demonstrated herein can be adapted to a greater range of geometries, since elements representing different geometrical "primitives" can be combined [10]. Furthermore, it is possible to modify the numerical solution to accommodate parallel flux paths, to provide even more adaptability to a variety of applications [11]. Alternatively, it is possible to use SPICE-type electrical circuit simulation software to perform these calculations [12]. In contrast, closed-form analytical methods are generally limited to simple geometries, typically cuboids, cylinders, and spheres.

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Fairy Tales About Heat Sink Performance Calculations

Reprinted from the *Electronics Cooling*® 2016, September Issue

Clemens J.M. Lasance,
Guest Editor, Philips Research Emeritus, Consultant@SomelikeitCool

INTRODUCTION

When Peter Rodgers invited me to again write a Thermal Facts and Fairy Tales (TF&F) column, I immediately thought of a recent webinar on basic heat sink calculations that I attended, in order to get an idea of the current status-quo in these matters. Well, in my humble view there was room for improvement. Apart from certain minor issues, I was triggered by three topics that I felt were not treated in a correct way when dealing with practical situations, namely;

- The fact that a heat sink does not only function as an area enlarger
- A much-too-simple explanation of the apparent (effective) emissivity of heat sinks
- The (mis)use of heat sink convective heat transfer correlations

With these three topics in mind, this TF&F column aims to outline my two cents on these issues.

A HEAT SINK HAS TWO FUNCTIONS

This topic has been treated *in extenso* in references [1, 2], with a summary provided here. One should realize that a heat sink performs two very different functions:

- Enlarge the surface area for heat transfer
- Spread the heat (providing a significant temperature gradient exists over the dissipating surface)

Suppose we wish to calculate the effect of a heat sink attached to an arbitrary generic electronic component without modelling all component–heat sink details. The first function is easy to address: simply multiply the real-life convective heat transfer coefficient by the area enlargement factor to obtain an effective heat transfer coefficient. It is the second function that can cause a problem when we need to consider the temperature gradient over the component surface that the heat sink is to be attached to. For this analysis, let's start by dividing the component surface into two areas: the central and periphery. When the heat sink is attached, the heat spreading reduces the maximum temperature of the central area and increases the minimum temperature in the peripheral region. This means that the effective heat transfer coefficient of the central area (required to lower its temperature is through addition of the heat sink base only) is significantly increased. Reference [1] highlights this aspect when a considerable increase in the average central heat transfer coefficient results, compared to the overall average value, i.e. 100 W/m^{2}K versus 8 W/m^{2}K, for a natural convection application. In this context, if we want to generate a heat sink compact model to increase the efficiency of computational auid dynamic (CFD) models, it is therefore mandatory to always explicitly model the heat sink base, with a compact description added for the remaining fin structure. Here is a first order estimation of this effect: suppose that for certain components that exhibit a significant surface temperature gradient, the central area is one quarter of the total area, and its effective heat transfer coefficient is 12 times higher than on the peripheral area, then the influence of the base is about as strong as a threefold total area extension.

THE QUESTION ABOUT THE APPARENT EMISSIVITY OF HEAT SINKS

The analytical calculation of the apparent (or effective) emissivity (or emittance) of a heat sink can represent a significant effort as it depends strongly on the heat sink geometry. The apparent heat sink emissivity can be determined with high accuracy by employing radiation network theory, as discussed in pages 291-303 of reference [3]. However such calculations are no longer necessary in the age of computer-aided engineering software having embedded radiation calculation options. Let us define the heat sink geometry as shown in *Figure 1(a)*.

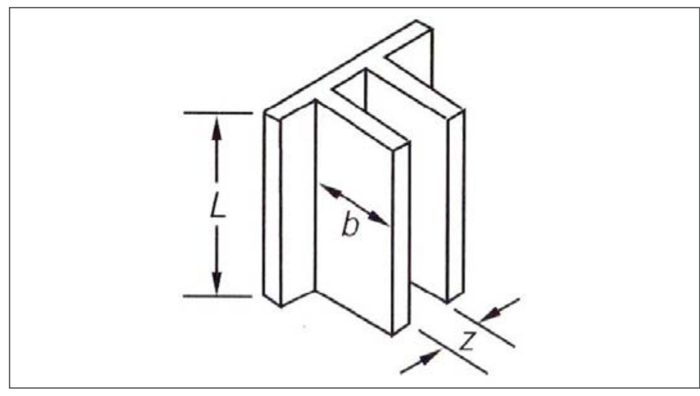

Figure 1(a): Heat Sink Geometry

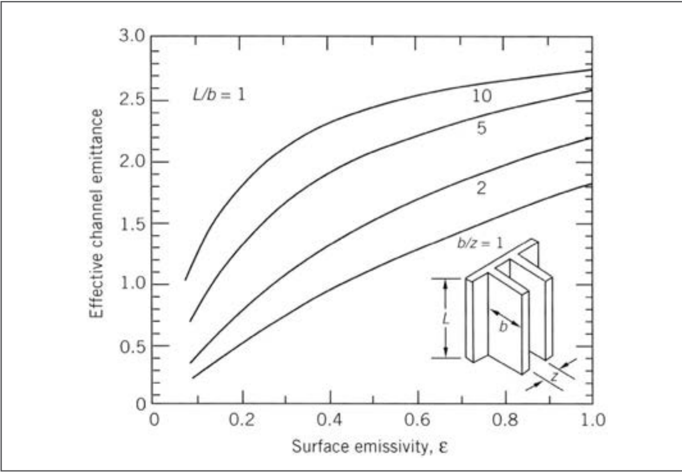

Figure 1(b): Channel radiative emittance for L/b = 1.

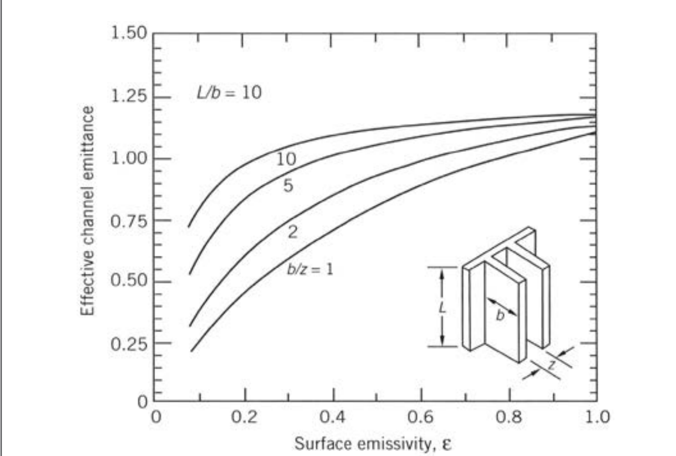

Figure 1(c): Channel radiative emittance for L/b = 10.

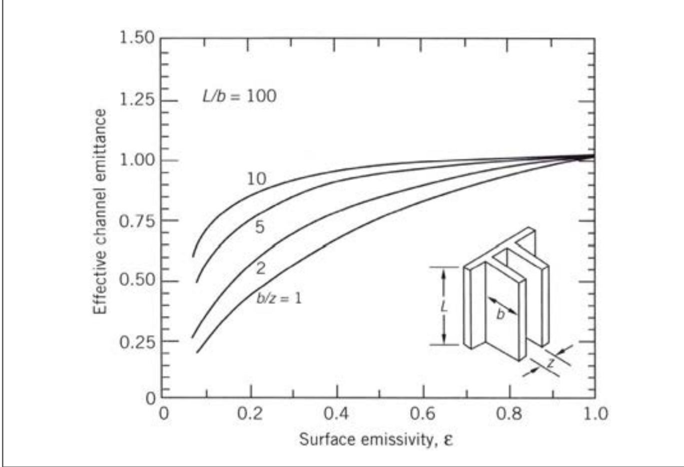

Figure 1(d): Channel radiative emittance for L/b = 100.

Figure 1. Effective (apparent) channel emittance (emissivity) for various heat sink geometries (taken from [3]).

The subsequent graphs shown in *Figures 1b* to *1d* provide a realistic impression of what to expect. Herein the apparent emissivity is related to the base surface area without fins. For short and wide fins (e.g. L/b=1, b/z=1), it is obvious that a considerable part of the additional area is exposed to the environment, and hence its emissivity does matter. Furthermore, because of the extended surface area, the apparent emissivity can be greater than one because the base area is the reference. The opposite is true for long and closely-spaced fins (e.g. L/b=100, b/z=10); in this case its emissivity does not play any role, and the extended area from a radiation point of view is negligible. The point is that the radiation entering the fin channel cannot escape without multiple reflections between the fin channel surfaces. In addition, heat sinks with such a layout are only used for forced convection, hence the radiation contribution to the total heat transfer is minimal anyway. The conclusion must be: don't bother with emissivity calculation for forced convection applications, but do for natural convection, especially for those applications where often widely spaced fins in a non-traditional shape are used, such as in the field of light emitting diode (LED) applications.

In summary, don't trust simple rules of thumb for natural convection applications. Caveat: check upfront if your application is really naturally convection driven. In most cases you will conclude that we encounter buoyancy-induced forced convection [4]. When a heat sink has already been selected, a simple test is recommended: measure the operating temperature drop before and after painting the heat sink.

THE (MIS)USE OF HEAT SINK CORRELATIONS

The problems with convective heat transfer correlations for practical purposes are extensively discussed in references [5-7]. Let me quote (a bit adapted) from my TF&F column of June 2015 [7].

The background in a nutshell is that the handbooks showing impressive heat transfer correlations are inherently based upon a set of conditions/constraints that are not satisfied in real life. When you believe in the following axioms, then the "Holy Books of Heat Transfer" are consistent and comprise a wealth of information, very useful for a basic understanding of the physics.

Here are the underlying axioms:

- Uniform boundary conditions, either constant temperature or flux
- Uniform approach aow with a degree of turbulence as close as possible to zero (that's why research type wind tunnels are huge).
- (Very) simple geometries: smooth, fat and thin plates, parallel plate channels, pipes
- Single source, especially for natural convection
- Constant properties
- Fan dynamics based on air flow chamber testing
- Extended surfaces based on Murray-Gardner assumptions (see e.g. [8])
- "Complex shapes" means there exists an analytical solution
- Heat spreading limited to one-layer, one-sided heat transfer
- Radiation diffuse and grey

This means that if and only if the physical situation conforms to the assumptions does the experimenter have the right to assume that the predicted results will be obtained. That means much more than simply matching Nusselt (Nu) with Rayleigh (Ra) or Reynolds (Re) numbers.

Specifically, most analytical (and numerical) studies assume uniform flow velocity with a specified turbulence (often zero), uniform temperature and the origins of the velocity boundary layer and the thermal boundary layer on the surface.

For many fields of heat transfer, such as turbulence, boiling, heat exchangers, channel flow, etc., these axioms form a sound base. **Not so for electronics cooling at the system level.**

Especially when referring to heat sinks, the author published a TF&F column titled "How useful are heat sink correlations" in [9]. Bottom line is that to use correlations to obtain a reasonable estimation of heat sink performance is a fairy tale.

What's wrong is that most equations are based on the following assumptions, in addition to the ones previously listed:

- Parallel plate heat sinks
- Fully ducted flow
- Fully developed flow
- Strong impact of 3D flow (especially in natural convection) not considered
- Equal number of fins and channels
- Negligible entrance and exit effects
- Laminar and uniform approach flow
- No temperature gradient in heat sink base
- Heat spreading effect of base not taken into account
- Uniform fin temperature (both between fins and within a fin)

Now, have a look at some state-of-the-art heat sink geometries for LED applications in *Figure 2*, in addition to the ones pictured in the December 2013 TF&F column [9].

Is there anyone out there who can tell me with a straight face that a Nusselt number correlation based on parallel-plate heat sinks will predict a realistic performance of these products? I don't think so.

Obviously, if you use handbook equations to base your heat sink design upon, or to predict the performance of a selected heat sink type, chances are high that you may miss all of the heat sinks shown in *Figure 2*. Sure, extrusion-based parallel-plate heat sinks are the cheapest around, but they score badly when it comes to optimization of shape, weight, volume, and performance, especially regarding optimal fin thickness. And the final argument in favor of using CFD codes instead of correlations: 3D printing is a booming business, and for sure parallel plates are not the ones that will be high on the list for optimization.

Figure 2: Non-parallel plate heat sink geometries for LED applications.

CONCLUSION

The starting point for this column was my experience with a heat sink webinar. I was not happy with the approach that it was presented, and the reasons why have been outlined in this column.

To all who want to transfer basic heat sink knowledge: tell facts, not fairytales. The fact is that reality is complex. Basic heat transfer about conduction, convection and radiation: OK, but tell the attendees also that in order to realize a competitive edge in eventual sales, much more knowledge is needed than some limited and outdated design rules. Compare it with electronic design: nobody believes that one is capable of designing a functional printed circuit board (PCB) after attending a webinar of half an hour. After this column one should understand why it is not simple to assess heat sink performance, which should be the bottom line.

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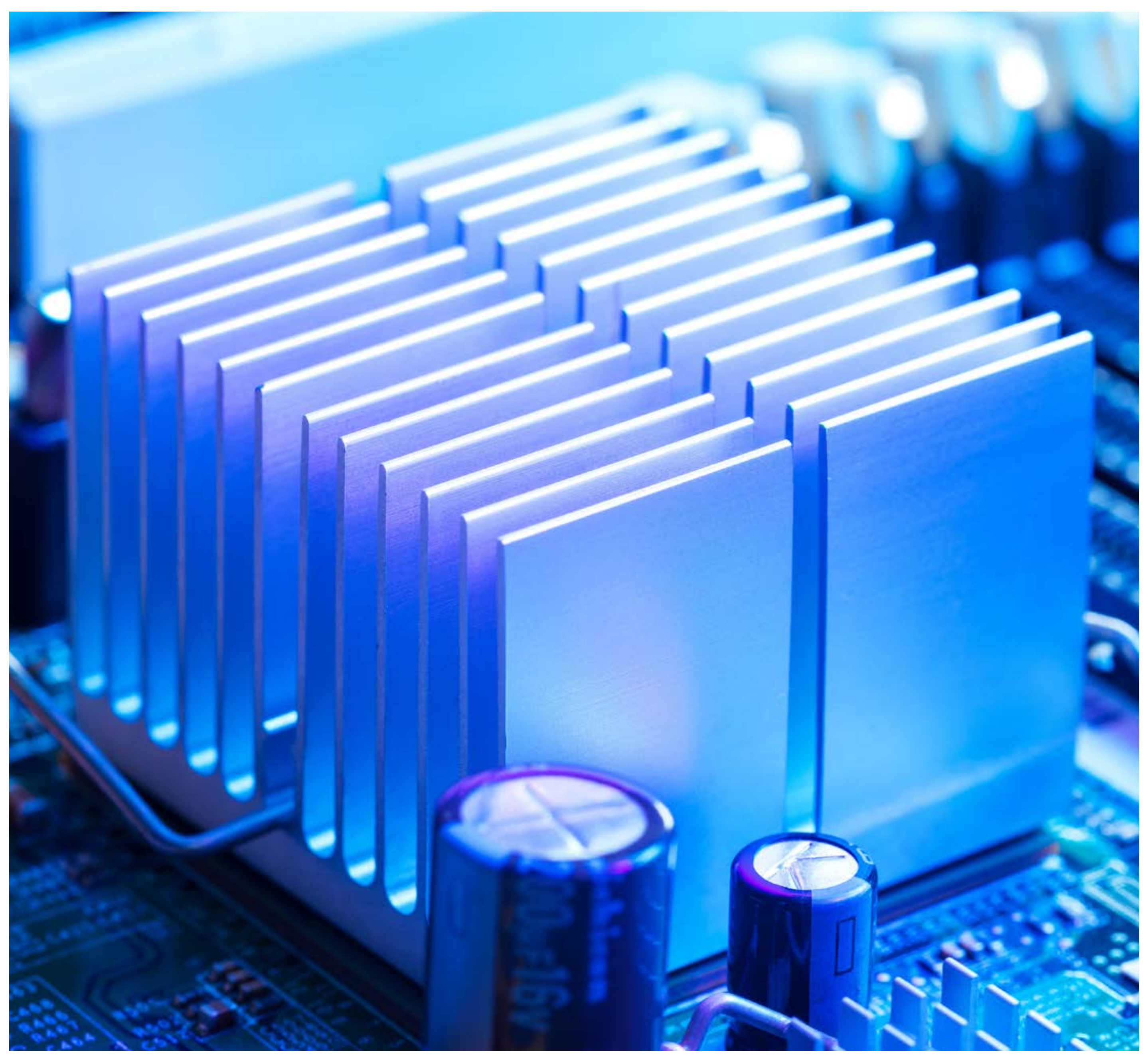

Probability

Ross Wilcoxon
Assoc. Technical Editor

INTRODUCTION

I've decided to introduce a new column to Electronics Cooling Magazine—and it's not just because I have run out of good ideas for "Thermal Facts and Fairy Tales" columns. For 2020, I will publish a series of columns in which I try to provide the readers with some insight into the field of statistics and a few tools for effective use of statistical methods. After a couple of decades in industry, I have observed that a number of experienced engineers can be intimidated by the topic of statistics—these columns will attempt to reduce the level of intimidation. While I have been interested in statistics for a few decades now, I don't claim to be an expert. I will do my best to get things as right as I can, as well as to make things useful and practical.

Statistical analysis is needed because data will always have some degree of uncertainty; a value that we determine from a single measurement, or even set of measurements, is not necessarily going to tell us exactly what value we will determine with additional measurements. Statistical analysis uses the mathematics of probability to create tools that we can use to deal with that uncertainty. This column discusses some aspects of probability concepts to set the basis for how the mathematics of probability can be applied to address uncertainty in statistical analysis.

Any discussion of statistical analysis must include a discussion on probability. Since the entire field of probability and statistical analysis began with gamblers attempting to improve their chances of winning, it seems appropriate that this discussion on probability begins with a game of chance: namely, throwing dice.

To begin, I assume that we have an infinite amount of time and patience that allows us to make a lot of throws, the dice that are not loaded (on any given throw they are equally likely to fall with any of its sides up), and we are not playing *Dungeons & Dragons*, so our dice only have six sides. In other words, I will use an Excel spreadsheet to simulate throwing dice. I trust that the random function is, in fact, fairly random, and that I can calculate the result of throwing a die with the equation "=ROUNDDOWN(RAND()*6,0)+1".

Figure 1 shows what fraction of 30,000 throws of 1-6 dice, as calculated using a simple Excel spreadsheet, had a total value of one to 36. For a single die, we would expect that the values one through six would each occur approximately 1/6th of the time—which is about what reasonably close to what was found in the calculations. As the number of dice included in the throws increases from one to six, the distributions change from a flat line to a triangle to an increasingly 'bell shaped curve'.

Figure 2 shows the same data, but plots the cumulative distributions that show what portion of the throws had a total value that was equal to or less than a value between one and 36. One of the

Figure 1: Probability distributions for 30,000 simulated dice throws.

Figure 2: Cumulative distributions for 30,000 dice throws.

fundamental tenets of probability theory is that the probability of the sum of all possible outcomes is equal to one, which is both logical and illustrated in the figure. In these cumulative distributions, the plots transition from a straight line to a 'tilted S shaped curve' as the number of dice increases from one to six.

Readers with some (any?) background in statistics likely can see where this is going—the 'bell' and 'tilted S' shaped curves start to look like the normal distribution that is widely used in statistical analysis. The discussion on that topic will be in the next column in this series.

A question that may be asked is "What would happen if we had to use actual dice and we didn't have the time needed to throw them 30,000 times?" Again, we can simulate that, with results shown for the probability and cumulative distributions for sets of only 30 throws of one through six dice in *Figure 3* and *Figure 4*. *Figure 3* is best described as an incoherent mess: for the 'one die' data, two values fell exactly on their expected theoretical value of 16.7%, while two other values were ~60% higher or lower than that. Data for more than one die do not appear to be much better behaved.

While the cumulative data for 30 throws, *Figure 4*, shows considerably more jitter than their counterparts for 30,000 throws (*Figure 2*), the cumulative distributions appear to be much less random than the raw distribution data (*Figure 3*). A comparison of *Figure 3* and the curves that show the same data in *Figure 4* illustrates why some data, such as from reliability testing, is often plotted in terms of a cumulative distribution rather than probability.

If a situation is governed by known physics, it can be relatively straightforward to estimate probabilities of a single event. In the case of rolling a single, non-loaded, six-sided die, it should seem obvious that there is a 1/6th chance of any of the six possible outcomes occurring. However, probability calculations can start to become less intuitive when we begin to consider combinations of multiple events. For example, consider the classic question that is considered to have been the beginning of mathematical analysis of probability—the likelihood of rolling a specific value within a specific number of attempts [1]. De Mere, a gambler in the 1600s, tended to win more often than not when he bet that he would roll a six within four attempts. His reasoning for why he would win was that the chances of rolling a six in one roll was 1/6th, so in four rolls his chances should be $4 * 1/6 = 2/3$. Since that value is larger than 50% and he was playing even odds (the loser pays the same amount regardless of who it is), he had concluded that it was, on average a winning bet. But when he extended the game to two dice and gave himself 24 attempts to roll a double six, which by his reasoning should have had the same probability ($24 * 1/6 * 1/6 = 2/3$), he began to lose money. He asked the mathematician Blaise Pascal to help him understand why his luck had changed.

When calculating probabilities of multiple events, two things that should be kept in mind are that the calculated probability of any outcome must never exceed 100%, and that it is often useful to think in terms of an event not happening. In de Mere's case, one simply has to consider the first point to recognize that his equation was incorrect. If the chances of rolling a six in four attempts is 2/3, then that equation states that the probability of rolling a six in eight attempts will be 133% (4/3). Clearly, this is not possible. To correctly determine the probability of rolling a six in four attempts, one can consider the probability of not rolling a six in one attempt and multiply that times itself four times. The probability of not rolling a six is (5/6 = 83.3%), so the probability of not rolling a six in four attempts is $(5/6)^4 = 48.2\%$. Since the probability of not rolling a six in those four attempts plus the probability of rolling a six in the same attempts must equal 100%, the probability of rolling a six in four attempts is 100%-48.2% = 51.8%. This probability is greater than 50%, so with even odds it makes sense that de Mere was coming out ahead. On the other hand, when using the same approach the probability of rolling double sixes in 24 attempts can be calculated as $1 - (35/36)^{24} = 49.1\%$, which is less than 50% and therefore not a good bet at even odds.

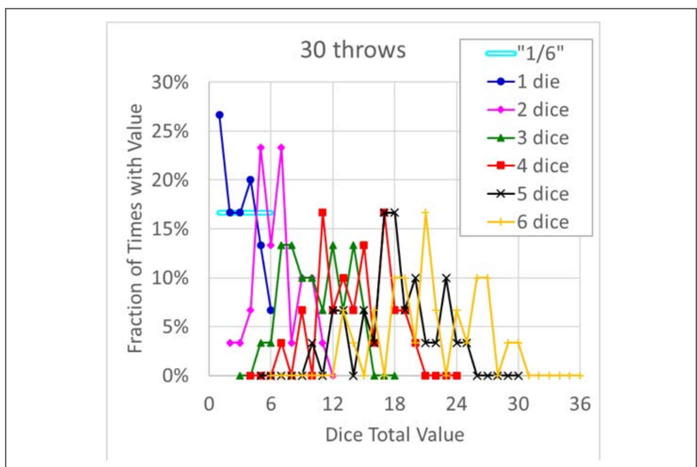

Figure 3: Probability distributions for 30 Simulated dice throws.

Figure 4: Cumulative distributions for 30 Dice throws.

SUMMARY

Probability theory is fascinating and, even the most cursory overview of it, encompasses far more than can be addressed in this short article. This is particularly true if one considers the topic of conditional probability [2], in which the probability of an event depends on another probabilistic event. The example described in this article illustrates that, in a reasonably well-behaved population of data, the effects of measurement variability tend to wash out and lead us to familiar-looking distributions. But it may require a lot of samples from that population to get there. If we only look at a small portion of the population, the distribution won't necessarily appear as a nice bell shape.

Future articles in this series will discuss some of the statistical approaches used to extract useful information and understand the distribution characteristics of data sets that are smaller than 30,000 that led to the smooth curves shown in *Figures 1* and *2*. Topics will include different parameters used to characterize a data set, what confidence we have regarding the uncertainty of those parameters, different models for distributions and how to use them, how to determine if one set of data is different from another, how many samples do we need for a given test, etc.

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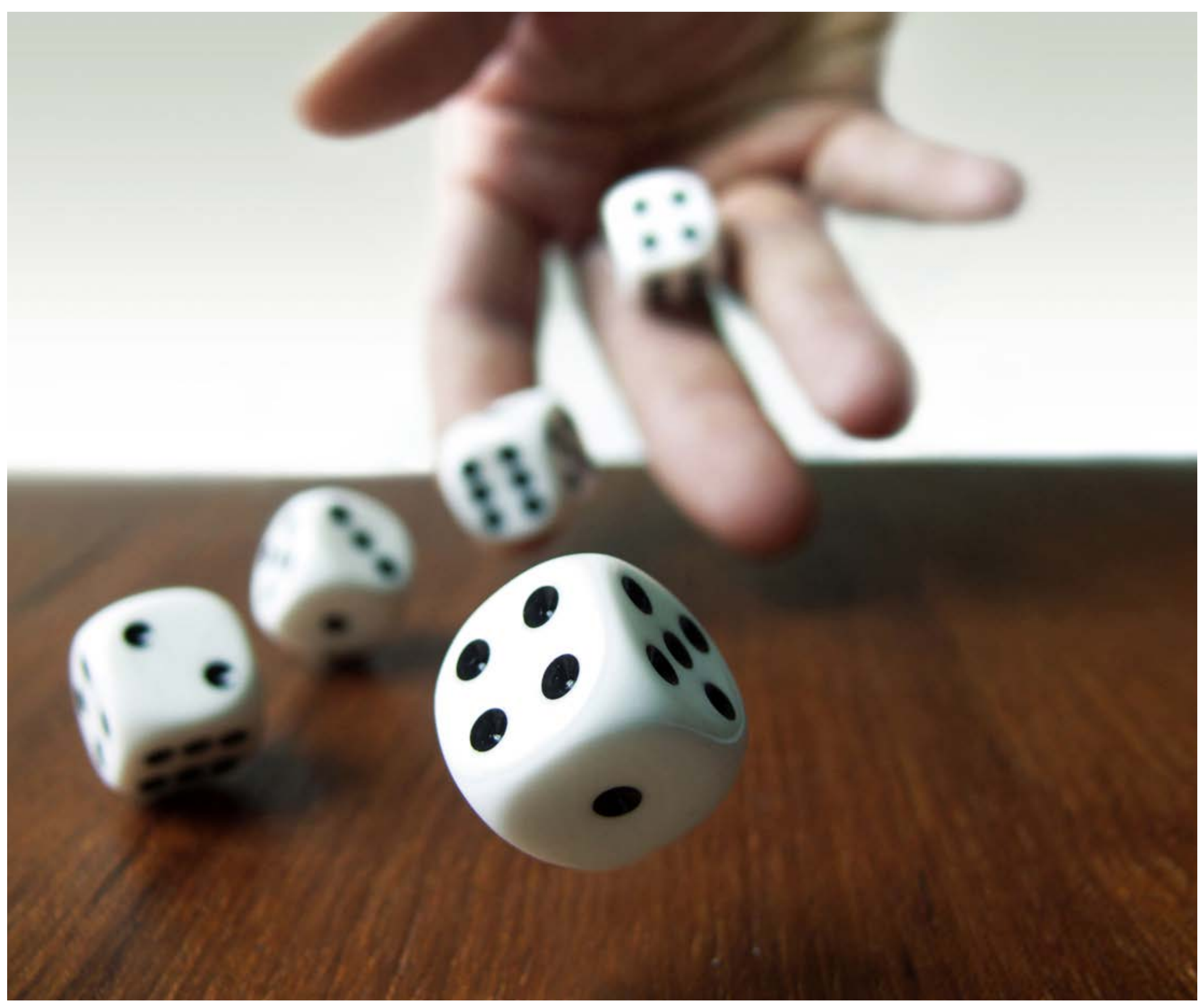

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David Saums*[1], Tim Jensen[2], Carol Gowans[2], Ron Hunadi[2], Mohamad Abo Ras[3]

[1]*DS&A LLC, Collaborative Innovation Works,* 11 Chestnut Street, Amesbury MA, 01913 USA
[2]*Indium Corporation,* 34 Robinson Road, Clinton NY, 13323 USA
[3]*Berliner Nanotest und Design GmbH,* Volmerstrasse 9B, D-12489 Berlin, Germany

* *Corresponding Author:* dsaums@dsa-thermal.com

David Saums
Dave Saums holds B.S. and MBA degrees from Clarkson University, with post-graduate work at Union College, all in New York. He has 41 years of work experience in electronics thermal management, working for several manufacturers of thermal materials, composites, and thermal management components and systems. He resigned as Vice President of Marketing for a specialty composites manufacturer to found DS&A LLC, a consulting firm focused on technical marketing, business strategy, and new product and business development. A presentation in 2008, in France, was the first implementation of a pumped two-phase dielectric liquid cooling system to IGBT modules and a complete electrical drive system. He has chaired a thermal management workshop in California as a volunteer for 19 years.

Tim Jensen
Tim Jensen is the Senior Product Manager for Indium Corporation's engineered solder materials, the company's most diverse product group, which includes solder preforms, wire, ribbon, and thermal interface materials. He is responsible for ensuring the product line is poised for long-term success by developing technologies that best meet the current and future needs of customers. Tim is a member of the SMTA's Board of Directors, has a bachelor's degree in chemical engineering from Clarkson University and an MBA from Syracuse University, and has authored numerous technical papers on soldering and thermal technology.

Carol Gowans
Carol Gowans has more than 30 years of experience in sales and product management. As the product manager for Indium Corporation's low-temperature products, her current focus is indium and bismuth products, which encompasses a variety of markets including medical, aerospace, cryogenic, and electronics manufacturing. Carol graduated from Utica College with a bachelor's degree in public relations and has authored papers on solder fortification® and improving solder joint reliability with the use of solder preforms.

Ron Hunadi
Ron Hunadi has more than 30 years of experience in sales, marketing, and business development in materials for electronics and microelectronics assembly. At Indium Corporation, he is a member of the Global Accounts Team and is responsible for developing new thermal interface business opportunities with large multi-national semiconductor companies. Ron has a bachelor's degree in chemistry from Penn State University, a master's degree and Ph.D. in organic chemistry from the University of California Riverside, and has authored more than 30 articles, papers, and patents.

Mohamad Abo Ras
Mohamad Abo Ras received his diploma and Master's degree in Applied Physics and Medical Engineering. During and after his studies, he joined Fraunhofer IZM in Berlin, in the thermal management group and in 2008, Berliner Nanotest und Design GmbH. Main focuses of his research work are development and application of test equipment for material characterization, as well as non-destructive methods for failure analysis. Since 2017, Abo Ras is chief executive officer of Berliner Nanotest und Design GmbH, in Berlin.

KEYWORDS

Thermal Resistance | Thermal Interface | Semiconductor Test | Durability | Cycling | Device Under Test

NOMENCLATURE

DUT Device Under Test
OSAT Out-Sourced Assembly and Test
Rth Thermal Resistance
S/TB Semiconductor Test and Burn-In
TIM Thermal Interface Material

ABSTRACT

Many thousands of thermal interface materials (TIMs) exist due to the very wide disparity in requirements across an extremely diverse range of market applications throughout the electronics industry. For certain market segments, such as geothermal and downhole petroleum exploration and semiconductor test and burn-in, application requirements may be so significantly challenging as to require development of materials for very specific and unusual requirements, beyond normal computing equipment and power electronic systems requirements. A test program in four phases has been designed to test such newly-developed materials against those very narrowly-defined and unusual requirements. The value of discussing such materials intended for a relatively narrow market segment is that this type of testing and development work can be useful in evaluating how to develop unusual test programs for other material applications. Three newly-developed TIMs designed specifically to address semiconductor test and burn-in (S/TB) requirements were tested and successfully passed each test phase.

SEMICONDUCTOR TEST REQUIREMENTS

The semiconductor test industry consists of manufacturers of very specialized test systems, companies that develop relatively complex test heads and sockets configured for specialized IC and power semiconductor packages, and the OSATs and semiconductor manufacturers that must perform testing of every device or according to a sampling regimen. This array of different customers for the TIMs utilized all have differing requirements that must be addressed. A short survey of a limited number of these manufacturers was conducted to develop a test regimen for clamping force, contact duration (dwell), temperature, and what is termed a "strike angle" for a non-parallel contact. Test procedures also include operation over a range of temperatures (typically 115-125°C) for defined periods, and, in certain burn-in tests, temperatures to 155°C. Mechanical test characteristics combined together (zero residue on the DUT, non-parallel contacting surfaces and potential for a strike angle as described, elevated temperatures, thousands of contacts with a single TIM) and this set of requirements is a major challenge for durability for any type of TIM selected.

Semiconductor test parameters include a variety of electrical performance tests for device performance and binning by frequency and other characteristics. Elevated temperatures during burn-in testing are intended to stress and cull early failures. The development of a single TIM type that can withstand many hundreds and thousands of contact cycles is critically important to test throughput and cost of semiconductor test. Some highly specialized devices may be very low unit volume, with only hundreds tested per day, while high-volume manufacturers of microprocessors and ASICs may require testing at rates up to tens of thousands per day. Stopping test programs in order to remove the TIM, clean the test head, and apply a replacement TIM can therefore be exceptionally costly in labor time and in yield.

Many different test head designs exist, to meet differing system requirements. Test is divided into two principal design categories: the use of a monolithic test head (i.e., a unitary flat contact surface facing the DUT), and the use of multiple electrical contact pin probes in an array (where no TIM is used). This discussion deals with the majority design category, the monolithic test head. These test head designs incorporate heating and cooling capabilities within the test head, with complex systems utilizing a liquid cold plate, one or more thermoelectric modules, and heaters, to apply the desired temperature cycles. The TIM must be applied to the flat test head surface facing the DUT.

MATERIALS DEVELOPMENT FOR SEMICONDUCTOR TEST

The critical requirement for semiconductor test, regardless of material type, is that any TIM used in contact with a device under test (DUT) must be of a type that does not leave any residue, oil, or contaminant on the surface of the device package (or die surface, if a bare die package). This requirement cannot be waived and eliminates all materials that are polymeric, in pad form, and capable of marking or leaving any detritus (especially electrically conductive), and all compounds such as greases and gels. While semiconductor test and burn-in (S/TB) may be a relatively low-unit-volume market segment, making this market a lesser choice for focusing new materials development, finding a material that will survive one to ten thousand contacts with a single TIM placement is highly desirable for test throughput and cost.

Table 1. Thermal/Mechanical Cycling Test Parameters

Organization	Test Pressure Reported	Test Temperature Range Reported (°C)	Dwell (Seconds)
Company A	11.7 bar (170 PSI)	25**/100	60
	11.7 bar (170 PSI)	100	60
Company B	6.7 bar (100 PSI)	-	60
Company C	-	120	-
Company D	-	100	-
Company E	-	80	60
Company F	4.1/6.7 bar (60/100 PSI)*	105**/125	-
	6.7 bar (100 PSI)*	105**/125	-

Notes: * Pressure applied dependent upon die or package contact area. ** Initial value.

Development of three new materials for S/TB has therefore focused on metallic and graphitic sheet materials. Graphitic mate-

rials are difficult to adapt to sharp corners and edges of test heads and also have a potential for shedding electrically-conductive flakes and fibers. Metal TIMs also, depending on metal and alloy selected, may be relatively brittle and have potential for shredding when the test head repeatedly contacts at an angle, on a 90-degree edge or on the sharp edge of a bare die. Taken together, these requirements as outlined in *Table 1* are a significant challenge for new materials development.

RELIABILITY TEST PROGRAM DEVELOPMENT

Use of a commercial TIM test stand was considered as the primary tool for a reliability test program. The ability to combine repeated, controlled cycling of a test material (for contact at a specific temperature, dwell, and release), with automated data collection per an industry-standard thermal resistance test procedure, was seen as a constructive approach, given the previously demonstrated reliability testing completed by the test stand manufacturer for other types of thermal materials. The test stand, designed and manufactured by a commercial manufacturer [1] to follow ASTM D 5470-17, incorporates servo motors with precise control of test head movement; a goniometer for planarity measurement; and internal software and motor controls. In addition, test heads are designed to be removable and in the standard system could be adapted to create a non-flat condition, with one test head capable of contacting the second at a pre-determined angle. [2, 3] This latter capability would mimic the so-called strike angle, found in high through-put semiconductor test systems where multiple types of devices (with lid; different lid sizes, different package types; bare die, and similar) flow through the test system. More complex system test heads include a gimbal, to allow the test head surface to adapt to these differences, as shown in *Figure 1*. [4]

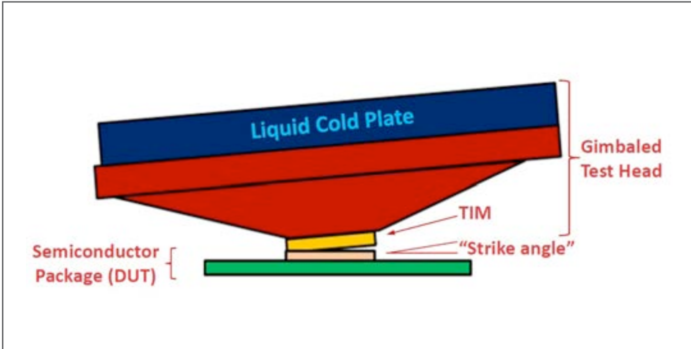

Figure 1: Illustration of a semiconductor test stand gimbal-mounted test head, allowing contact of the test head with attached TIM at different orientations to different devices under test with different package configurations and contact surface dimensions. (Adapted from Sanchez, [1]).

For this test program, four test phases were developed to place increasingly challenging durability requirements on each new development material; simultaneously, TIM thickness change was measured during each phase, as was thermal resistance. The four phases are summarized in *Table 2*; the first is the baseline set of data against which subsequent data sets were to be compared. Phases I and IV are similar to the conditions required for standard ASTM D 5470-17 thermal resistance testing, with parallel test heads and a uniform power and clamping force applied. [5, 6] Phases II and III address the elevated temperature and so-called "strike angle" introduced to mimic behavior in S/TB processes; the specific characteristics of these two phases were developed from the data obtained in a short industry survey of practice. Phases II and II therefore are not representative of a normal thermal resistance test per industry standard ASTM D 5470-17. (A dwell as short as sixty seconds would normally be considered to be insufficient for system stabilization and accurate data generation.) Specifications for the test heads are shown in *Table 3*.

Table 2. Thermal/Mechanical Cycling Test Program Design

Program Phase	Purpose	Test Head Configuration*	Operating Temperature (°C)	Data Output
I	Baseline Values	Parallel	70-95	R_{th}**, Thickness Change,*** 1,000 Contact Cycles
II	Strike Angle	Upper Body: Strike Angle	70-95	R_{th}**, Cycle Count
III	Strike Angle/ Elevated Temperature	Upper Body: Strike Angle at Elevated Temperature	125	R_{th}**, Cycle Count
IV	Baseline Values	Parallel	95	R_{th}**, Thickness Change,*** 5,000 Contact Cycles

Notes: * Test head configuration and test system design per ASTM D 5470-17 test methodology. [2]
** Thermal resistance and (***) thickness values used to indicate a stabilized test routine.

Table 3. Thermal/Mechanical Cycling Test Head Design

Property	Value
Material	Aluminum Alloy (AlMgSi1)
Contact Area	17.5mmx17.5mm (306mm²)
Contact Surface Roughness	Rz≤1µm
Sample Temperature	95°C
Upper Reference Body (Heater Bar)	125°C
Lower Reference Body (Liquid Cold Plate)	75°C
Temperature Measurement	In situ
Thickness Measurement Under Force Applied	In situ

MATERIALS TESTED

Three recently-developed TIM types were tested. Each of these has been developed to meet specific requirements for semiconductor test and burn-in applications. These are described in brief terms in Table 4; each is a metal alloy. The first is a dead-soft aluminum alloy coated with a non-silicone thermal compound applied to one side only, identified as HSMF-OS. The second and third are indium metal, a relatively compliant metal that can also be moderately tacky. Given the requirement for ST/B applications

that the TIM separate cleanly with no residue be left on the DUT, one indium TIM is manufactured with a very thin aluminum alloy cladding; this thin cladding is slightly stiffer and provides the clean separation and more durable surface required. This TIM was originally developed for rework requirements for high-dollar-value semiconductor processor modules for enterprise servers. The first aluminum-clad indium TIM is a flat foil. The second aluminum-clad indium TIM is manufactured with the same construction as the first, with a distinctive patterning applied to increase compliancy. [6]

Figure 2 illustrates one of these specialized TIMs, die-cut to a so-called "Red Cross" shape, as applied to the upper test stand test head. RTDs are evident in the figure, requiring through-holes in the arms of the TIM pre-form, where the RTDs are inserted into the test head after placement of the TIM.

Table 4. Thermal Interface Materials Tested	
Graph Key	Description
CLAD	Indium (99.99%) flat foil, clad one side (13μm/0.0005") aluminum
CLAD HSK	Indium (99.99%) foil, clad one side (13μm/0.0005") aluminum, HSK pattern applied*
HSMF-OS	Aluminum foil (51μm/0.002"), coated one side with dry thermal compound**

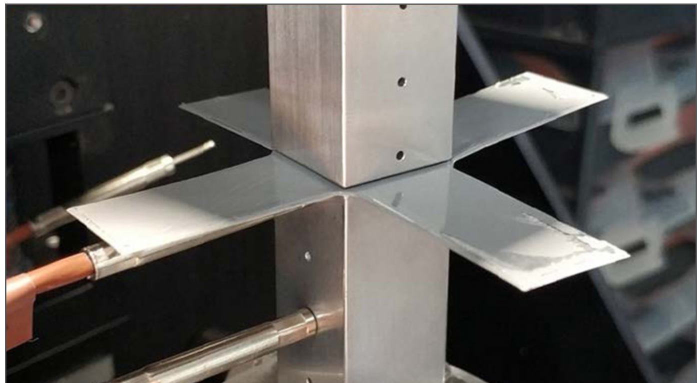

Figure 2: Test material as applied to test head, Phase I. This is the HSMF-OS TIM die-cut to a so-called "Red Cross" shape and prior to completed assembly. The four arms will be folded against the sides of the upper test head and a simple mechanical fixture attached to clamp the TIM to the upper test head, to mimic placement in a semiconductor test system.

TEST RESULTS AND EVALUATION

The usefulness of the selected commercial test stand [7] was shown in the consistent data, generated without any modification of the system controls and hardware. Automated data output for material thickness change during test was determined to be a useful indicator of any perturbations, whether in electrical power or in material durability. A perturbation was observed in one test due to an input electrical problem, which was corrected. The relatively smooth curve representing measured thickness change proved to be a useful determinant of stable test conditions, with no TIM degradation such as tearing or perforation (with the introduced strike angle). Nominal thermal resistance data was also used as a check for stability during the test regimen, for control purposes. The test system provided output values that included test head temperature measurement, material thickness, changes in thickness (for the selected TIM under test), bulk and interfacial thermal resistance values, and derived thermal resistance (Rth). Designed to incorporate removable test heads, the test program could therefore be designed with specification of contact surface roughness; the use of a fine adjustment feature allowed specification of a precise angle per the "strike angle" for Phases II and III. Such built-in features avoided the need for specially-designed equipment that would have added a cost and time penalty for the program.

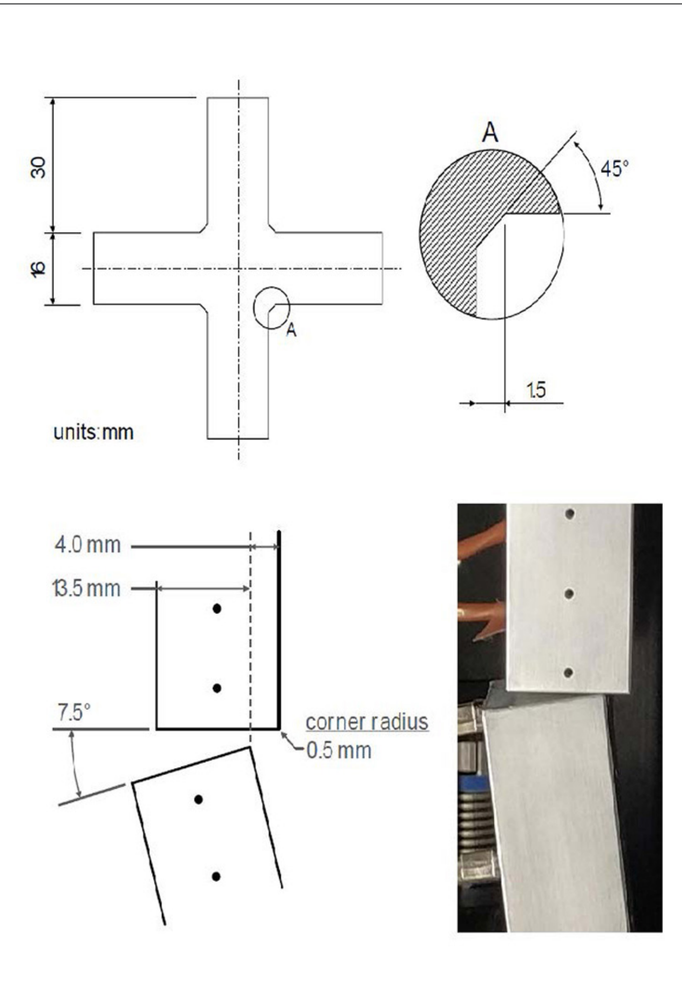

Figure 3: An example of the dimensioning of a so-called "Red Cross" die-cut TIM designed for use in semiconductor test systems The lower figure and photograph illustrate the test program design incorporating a 7.5° strike angle; the lower head moves in this implementation, to act as the contacting head.

Materials subjected to each test phase were examined visually for evidence of cracking, tearing, or other perturbation.

All materials tested exceeded the goal of one thousand contact and release cycles.

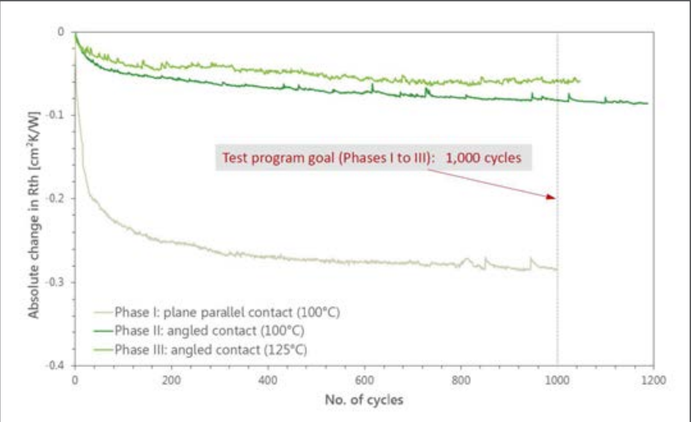

Figure 4: Thermal resistance values, Phases I - III, showing test results for 1,000 cycles completed per phase for a single material type. A change in attachment fixture resulted in lower initial values for Phases II and III, compared to Phase I.

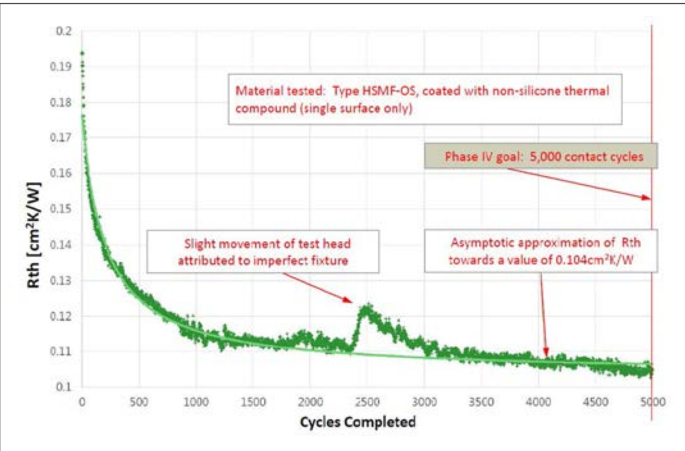

Figure 5: Thermal resistance values, Phase IV, showing test results for the stretch goal of 5,000 cycles completed for a single material type. A slight perturbation was analyzed; the reliability cycling test was completed successfully for this material.

Thermal resistance values for the first three phases of the test program are shown in *Figure 4*, for one of the development materials. During the cycling regimen, a plot was generated showing thickness change for each material, for each phase; each such graph showed a stable condition. No marking and no residue was found on the test head surfaces, upon completion of each test phase for each material.

Given successful completion of the first three test phases, an additional phase to test to achieve 5,000 contact cycles was conducted. The HSMF-OS material was selected and tested and this stretch goal for the test program was achieved. Again, no evidence of cracking or shredding of the TIM being tested, as well as no evidence of marking or residue left behind. [8]

CONCLUSIONS

This test program was based on a survey of challenging industry requirements for semiconductor test and burn-in applications. Based on the survey, a test program was developed in order to test and evaluate a set of specialized TIMs developed to meet these requirements. The test program consisted of four phases and all three development materials met the goals of these four test phases. The results have been analyzed, with no visible evidence of tearing, shearing, or marking of the devices under test. The indication is that this test program was completed successfully for all three TIM types examined, using a commercially-available test stand designed to follow an industry-standard thermal resistance test methodology. The result of this testing will be used to demonstrate how these specially-designed TIMs can be utilized for these intended applications.

ACKNOWLEDGMENTS

All testing was conducted in an independent test laboratory, Berliner Nanotest und Design GmbH, in Berlin, utilizing a test stand developed by Berliner Nanotest. Industry inputs by Jaime Sanchez, Intel Corporation, and other participants in the industry requirements survey, were very important for practical test program design.

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Thermal Management of Chip-on-Board LED Systems and Their Aging Response to Cyclic Power

Lisa Mitterhuber, Julien Magnien, Elke Kraker
Materials Center Leoben

INTRODUCTION

Twenty years ago, a lamp had exactly one purpose—to illuminate the room. A typical incandescent lamp lasted a year and failure was caused by a filament or/and a glass breakage [1]. Nowadays typical lighting is based on LED technology, which is considered as durable. Due to the fact that many materials are interacting in such a lighting system, the variety of failure modes is increasing too. Therefore, design and material issues are critical to the reliability of such an electronic system. Its testing is crucial to guaranteeing a long-lasting LED system.

Particular attention must be paid to thermal management [2], as thermal stress is one of the main triggers of failure modes in electronic systems. To predict the lifetime of the LED system and to ensure its reliability, knowledge about critical failures is needed. In this paper, an LED module based on four flip-chip LEDs is investigated in terms of design for reliability and aging phenomena during a supply switching test (SST), by using thermal impedance analysis.

TEST DEVICE AND METHODOLOGY

The investigated LED module consists of four blue flip-chip LEDs, electrically connected in series by SnAgCu (SAC305) solder joints on the copper electrodes of a printed circuit board (PCB). Here, the LED module has no underfill. The PCB was mounted on a liquid cooled heat-sink via thermal interface material (TIM). A schematic of the flip-chip (fc) LED-module can be seen in *Figure 1a*.

Lisa Mitterhuber | Lisa.Mitterhuber@mcl.at
Lisa Mitterhuber is working as a senior scientist in the department of materials for microelectronics at the Materials Center Leoben in Austria. She studied Technical Physics at the University of Technology in Graz from 2010 to 2016. In 2019 she got her Ph.D. degree in materials science at the Montanuniverstät Leoben. During her thesis she was developing a scale-bridging methodology of the thermal transport in microelectronic devices, considering both wafer as well as package level.

Julien Magnien | Julien.Magnien@mcl.at
Julien Magnien graduated from the Karl Franzens University of Graz in 2010 with a master's degree in physics and received the PhD degree from the University of Vienna in 2015, focused on the reliability of solder interconnection technologies. Since 2015, he is working at the Materials Center Leoben in the field of reliability and lifetime modeling for microelectronic packages. The main activities compromise the development of reliability monitoring models based on temperature sensitive electrical parameters, and parameter driven lifetime prediction.

Elke Kraker | Elke.Kraker@mcl.at
Elke Kraker studied physics at the University of Graz where she obtained her master's degree in 2004. Afterwards, she started her PhD studies at the University of Graz focusing on opto-chemical sensors combined with organic electronics and received her PhD in 2008. In 2012 she joined the business unit “Materials for Microelectronics” of the Materials Center Leoben Forschung GmbH and works there as leader of the “Reliability and Analytics for 3D Integration & Packaging” group. The main focus lies on the development of tests and methods for material characterization in the field microelectronics, development and evaluation of reliability tests.

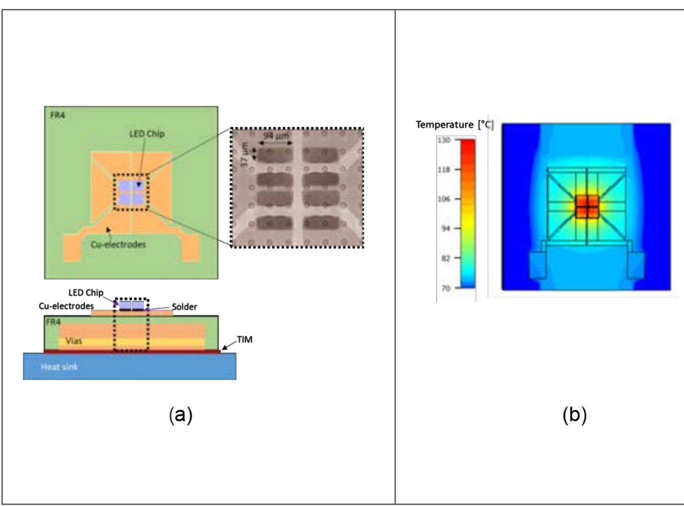

Figure 1: (a) Top view and side view of the tested device. The four LED chips are connected via soldering with the electrode on the PCB. (b) Simulation of the hot steady state operation of the LED-module.

Table 1. Material parameters of the thermal simulation after the validation process

Material	Thermal Conductivity [W/mK]	Specific Heat [J/kgK]	Density [kg/m³]	Thickness [µm]
GaN	170.0	431	6100	15
Saphire	26.8	856	3980	250
Solder	56.0	530	7500	50
Cu-electrodes	330.0	305	8930	50
Cu-core	385	435	8930	500
FR4	1.1	807	2340	Top layer: 70 Overall: 3500
Vias	In-plane: 3.0 Through-plane: 10	892	2520	70
TIM	3.0	700	2500	20

The supply switching test (SST) was applied for reliability testing. This SST leads to active heating due to the power losses occurring at the LED junction. The LED module was mounted on a heat-sink (T_s=8°C). Then a power load of 7 W was used for heating up the system to T_j=125°C with a dwell time of 30s. Afterwards, the system was switched off, also with a dwell time of 30s. This cycle was repeated to investigate the aging phenomena of the LED module and to gain knowledge of the anticipated service life of the package [3]. The active current based heating of the LED module was done using a commercial programmable power supply [4]. At the beginning and during the SST, the LED modules were monitored thermally to control their thermal performance and to analyze their reliability. The evaluation of the thermal performance of the LED module was carried out by thermal impedance analysis. The experimental investigations were done by using a commercial thermal test apparatus and accompanying analysis software [5] according to the JESD 51-14 standard [6][7].

A simulation was carried out for the thermal heat path using commercial finite volume software [8]. Both in the experiment and in the simulation, structure functions were generated. The structure function represents the heat path in the LED module from the junction to the heat sink as a thermal equivalent network of thermal resistances and thermal capacitances in a one-dimensional way. The comparison of these structure functions enables verification of the thermal model. The validated structure function provides an understanding of the heat path within an LED module [9]. By adjusting one specific parameter in the simulation, changes in the structure function can be used to identify the source of variations in the heat path of the LED system [10][11]. E.g., a "virtual" dual interface experiment can be performed by varying the thermal conductivity of the TIM.

THE INITIAL STATE OF THE LED AND ITS AGING PHENOMENA

Before starting the reliability testing, the initial state of the LED system was determined by the thermal impedance analysis. The structure functions were generated from both measurement and finite volume simulation. The structure function was divided into four different sections (dR_{th}1-4). The dR_{th} sections were chosen to be the distance between two significant peaks in the structure function (see *Figure 2*) [12]. Each section can be interpreted as a different region along the heat path of the LED system. The corresponding validated thermal simulation enabled each of these sections to be associated with real physical regions in the LED system. *Figure 2* shows the four dR_{th} sections of the structure function and their corresponding region in the LED system, represented as isotherms. The temperatures of the isotherms are the maximum temperature of each dR_{th} section. The dR_{th}4, which was assigned to the attachment of the LED module to the heat sink, the TIM, had the largest thermal resistance in the system followed by the PCB (dR_{th}2).

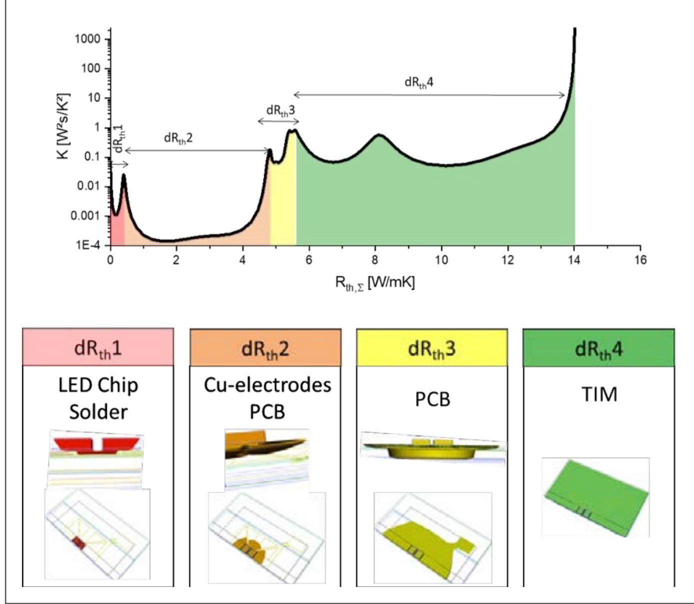

Figure 2: The structure function of the LED-system under investigation, divided into four dRth sections. Each section corresponds to different regions in the heat path in the LED module from the LED chip down to the heat sink.

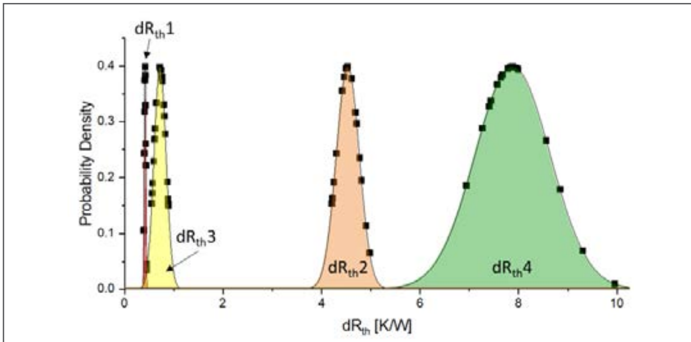

Figure 3: The probability density function of the initial dRth1-4 sections of all tested LED systems.

To analyze if an LED system undergoes a significant change in its thermal performance during the SST, all the LED systems were subject to an initial control. Here, 15 LED systems underwent the SST and their initial thermal resistance of each LED system was analyzed. The initial status of $dR_{th}1$-4 of all 15 LED system is shown as probability density functions in *Figure 3*. This analysis showed a Gaussian-shaped distribution of $dR_{th}1$-4. $dR_{th}4$, the attachment of the LED module to the heat-sink had the broadest range, followed by the $dR_{th}2$, $dR_{th}3$, and $dR_{th}1$.

The thermal impedance analysis allows us to check the LED system's performance in each SST cycle. During the SST the thermal total thermal resistance became higher with the number of cycles. This indicates that there were structural changes within the LED system. To reveal the root cause of the structural changes, the dRth sections were analyzed during the SST and material parameters of validated simulation were varied systematically. Degradation of the materials in the LED system can be assigned to changes in the heat path. This procedure is described in more detail in [11]. There, it was shown that even though the $dR_{th}4$ had the largest distribution initially, it stayed nearly constant during the SST. This indicated no degradation of the mounting over the whole SST runtime. $dR_{th}1$ and $dR_{th}2$ increased significantly with the number of cycles, pointing out that the connection between LED chips and the PCB is mainly affected by the SST. Concluding the dR_{th} analysis of the SST, the aging of this interconnection was found to contribute to the increase of the thermal resistance and hence the junction temperature in the fc LED module. [11]

PREDICTING THE LIFETIME OF THE LED MODULE

The information that the aging of interconnection is one of the major reliability concerns in the LED system can be used to create a reliability model. A reliability model allows for forecasting the number of cycles until failure and hence the remaining lifetime by using a parameter-driven monitoring model. The reliability model was generated empirically by using the change of the thermal resistance over the number of cycles. The parameter-driven monitoring model can be expressed as,

$$R_{th} = R_{th,0} + \frac{1}{P_H}\left(e^{B\,\Delta T_{pc}^{C}\,N} - 1\right) \qquad (1)$$

where R_{th} is thermal resistance at a specific number of SST cycles, $R_{th,0}$ is the initial thermal resistance of the device, P_H is the heating power, coefficient ΔT_{pc} is the initial set temperature swing of the SST, N is the number of SST cycles, and C and B is the empiricially determined power law. A more detailed description can be found in [13].

Equation 1 shows that two parameters are significant for the reliability model: the initial thermal resistance of the LED-module and the used power load in the SST. The higher the applied power and the thermal resistance of the LED-system, the higher the temperature swing during testing.

The magnitude of the temperature swing determines how fast the material degrades. The reliability model also revealed that there is a minor interaction between the two parameters, the initial total thermal resistance, and the power load. [14]

The left-hand axis of *Figure 4* shows the statistical distribution of the total thermal resistance of the LED system with its associated sigma level. The number of cycles until failure increases up to 37 times comparing the LED system with the highest (15.6 K/W) and the lowest (12.5 K/W) thermal resistance. As previously mentioned, this initial thermal resistance is mainly influenced by the attachment of the LED module to the heat-sink (see *Figure 3*).

The reliability model for different power loads is shown in *Figure 4* on the right-hand axis. The thermal resistance values with the power load of 7 W are determined experimentally; the other values with a higher power load were calculated from the model. For an LED system with an average thermal resistance of 14 K/W, it was shown that a reduction of power from 10 W to 7 W (a relative increase of 43%) causes an eight times higher number of cycles until failure. This is caused by the lower temperature swing, which results in lower mechanical stress in the interconnections and accordingly implies slower fatigue. [13]

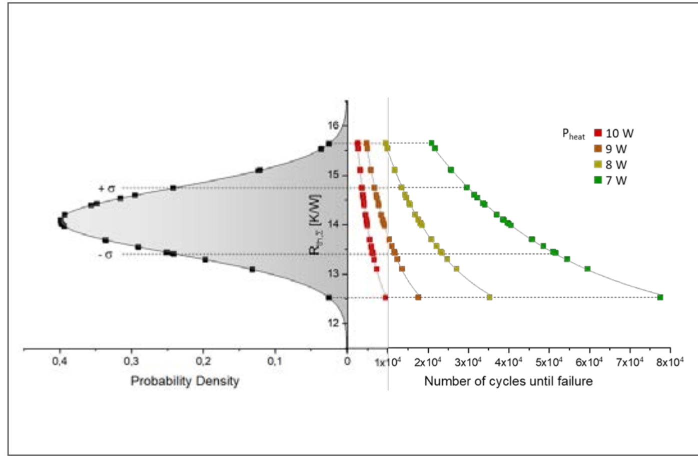

Figure 4: Right-hand axis: Probability density of the total thermal resistance of the tested LED systems with its corresponding sigma level. Left-hand axis: Expected lifetime reduction of the studied LED system depending on the initial total thermal resistance (y-axis) and depending on the applied power (different marker colors).

CONCLUSION

The thermal impedance analysis was used to investigate the major reliability concern of an fc LED module. In depth analysis of the impedance measurement, in terms of the corresponding structure functions and their dRth section, combined with thermal simulations confirmed solder fatigue as the main aging phenomena. Based on this, a reliability model for an SST was developed to describe the aging of an fc LED module. The lifetime of the package strongly depends on the temperature swing experienced during the SST, which is determined by the initial thermal resistance and the applied power load during testing.

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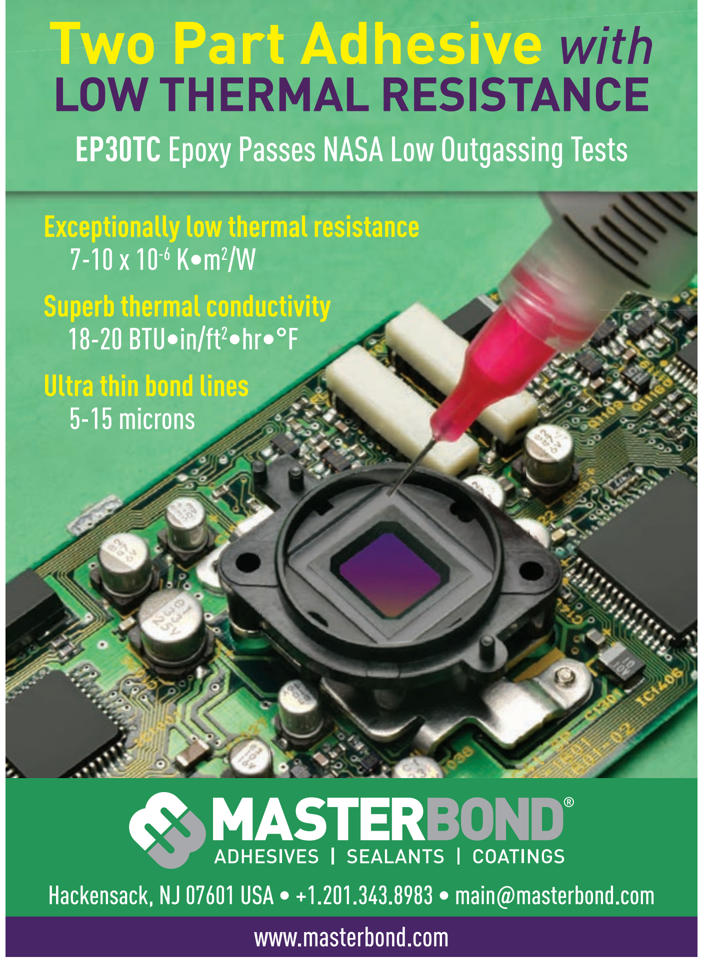

Solder Joint Lifetime of Rapidly Cycled LED Components

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Wendy Luiten
Electronics Cooling Specialist and Master Black Belt at WLC and Lecturer at the High Tech Institute Eindhoven
4wendyluiten@gmail.com

INTRODUCTION

Active LEDs in a consumer TV product are boosted and dimmed with the video picture content. Boosting and dimming of LEDs is a powerful means to improve visual experience, either through application of active LEDs in an ambient light feature, or through dimming and boosting of the display LEDs in a direct lit video display. Active driving of LEDs is also a significant consideration in the thermal management of a video display product [1, 2]. However, active driving of LEDs increases the number of temperature cycles by several orders of magnitude, and thermal cycling is well known to lead to so-called low cycle fatigue solder joint failure. How then will active driving of LEDs affect the lifetime of LED solder joints in a TV product?

SOLDER FATIGUE AT LONG TIME SCALE

The root cause of low cycle fatigue solder joint failure is that thermal mismatch between a component and PCB is taken up in deformation of the solder joint. Assume that a SMD (Surface Mount Device) LED is subjected to an instantaneous temperature rise ΔT at t=0 s. This results in a thermal shear strain ε_T in the solder joint, proportional to the temperature change, $\varepsilon_T \sim \Delta T$. At t=0s, the entire thermal strain is taken elastically. By Hooke's law, the shear stress σ is proportional to the elastic strain ε_e with proportionality constant G, the solder's shear modulus $G=\frac{E^e}{2(1+v)}$. Thus, at the instantaneous temperature rise $\sigma_0=G\cdot\varepsilon_e=G\cdot\varepsilon_T$. At longer times the solder starts to creep, that is, to flow very slowly, and part of the thermal strain is taken in creep strain ε_c. This lowers the elastic strain and the stress relaxes.

$$\sigma = G \cdot \varepsilon_e = G \cdot (\varepsilon_T - \varepsilon_c) \quad (1)$$

When the creep strain equals the thermal strain, $\varepsilon_c=\varepsilon_T$, the elastic strain is zero and the joint is stress-free. If the temperature is then lowered by $-\Delta T$, the change of temperature, with respect to the stress-free situation, will again cause a thermal mismatch, which will again cause stress in the solder joint, $-\sigma_0$, which will again relax away to the stress-free situation through solder creep. In this manner, temperature cycles result in cyclic loading, creep and stress relaxation in the solder joint. The diagram of stress versus creep, strain is shown in *Figure 1*.

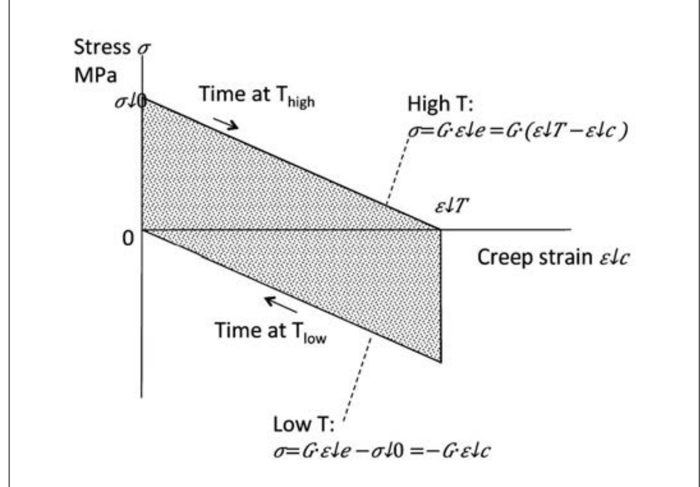

Figure 1: Stress-creep strain loop from cyclic thermal load.

In each cycle, an amount of damage is incurred that is proportional to the area inside the stress- creep strain loop. Solder joint failure occurs once the total accumulated creep damage exceeds a certain value C, which is usually determined through an accelerated test. *Figure 1* shows that the area inside the loop for a full creep cycle up to the stress free situation equals $\sigma_0 \cdot \varepsilon_T$. It follows that the area of the loop is proportional to ΔT^2:

$$\text{Area} = \sigma_0 \cdot \varepsilon_T = G \cdot \varepsilon_T^2 \sim \Delta_T^2 \quad (2)$$

A similar relationship is also found in the low-cycle fatigue law of Coffin-Manson [4], in the work of Engelmaier [5, 6] and of Norris-Landzberg [10] in the form of fatigue exponent, which roughly corresponds to a value 2. The quadratic dependency is also the basis for the common design rule relating the number of cycles to failure in operation N_f to the number of cycles to failure N_{test} in an accelerated test with temperature sweep ΔT_{test} :

$$N_f = \frac{N_{test}\,(\Delta T_{test})^2}{\Delta T^2} \quad (3)$$

The fatigue cycle shown in *Figure* 1 will only appear if the heating and cooling is instantaneous, and if dwell times are sufficiently long to allow for relaxation up to the stress free situation. It is well-known that the durations of ramp time and dwell time have a significant impact in accelerated temperature cycle tests [7]. Both the Engelmaier and the Norris-Landzberg model incorporate the effect of field vs. test timing in a time factor in their models. However, it is not obvious that these models are appropriate for short video time cycles. Typical temperature cycle tests have at most one order of magnitude difference from test to field condition. Since temperature effects dominate the acceleration factors, it then becomes difficult to separate out time effects with accuracy. Furthermore lifetime, test timing parameters, and test temperatures are interrelated in a complex manner [10]; therefore, separation of time and temperature effects does not lend itself to extrapolating with confidence. As an example, the Engelmaier relations were critically reviewed in [8] and shown not to be reliable for several cases. Hence using existing simple models incorporating the cycle time effects is not straightforward for short video cycles and more accurate numerical investigation using FEM is often not possible in view of limited project resources.

Table 1. SAC Material Properties

Parameter	Value	Unit
Schubert Model		
A	277984	s^{-1}
B	0.02447	MPa^{-1}
C	6.41	
D	6500	K^{-1}
Elastic Constrants		
E	mm x	MPa, T in Kelvin
v	0.36	

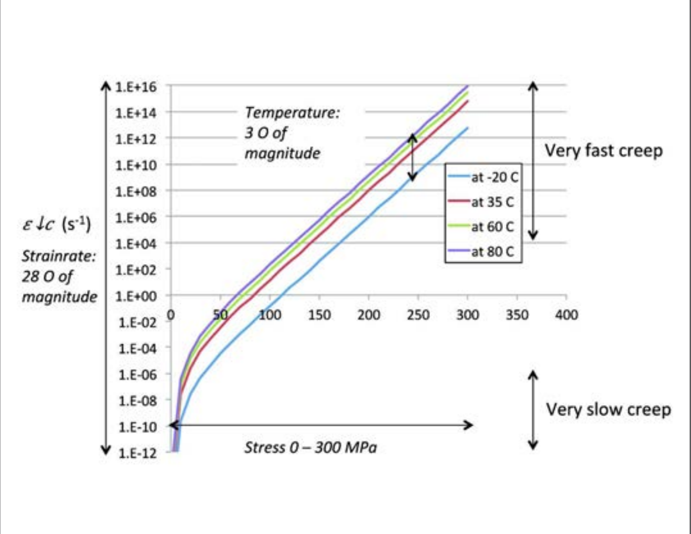

Figure 2: Creep strain rate ε↓c (s^{-1}) as a function of stress σ (MPa).

SOLDER FATIGUE AT SHORT TIME SCALE

The purpose of the current work is to find out the influence of short cycle times on solder failure in a less resource-intensive manner, allowing for a better lifetime estimate in a safe engineering envelope. Direct integration of the creep strain rate is used to determine how much creep will actually occur in the cycle time. The flow rate or creep strain rate of solder is extremely dependant on stress and temperature. According to Syed's formulation of the Schubert model for lead-free solder [9], the creep strain rate is the product of a stress dependent part $g(\sigma)$ and a temperature dependent part $f(T)$.

$$g(\sigma) = A\{\sinh(B\sigma)\}^C \tag{4}$$

$$f(T) = \exp\left(\frac{D}{T}\right) \tag{5}$$

$$\dot{\varepsilon}_c = g(\sigma)f(T) = A\{sinh(B\sigma)\}^C \, exp\left(\frac{D}{T}\right) \tag{6}$$

Table 1 shows the values for the material parameters A through D, as well as the elastic modulus E and Poisson ratio ν.

Figure 2 shows the calculated creep strain rates for a -20°C to 85°C temperature range and 0-300 Pa stress range.

It shows that the shear strain rate varies 28 orders of magnitude over the stress range. At high stress levels, the extremely high creep strain rate will immediately relax the stress to a lower level, so this part of the stress relaxation does not cost significant time. At low stresses, the very low creep rate will result in negligible creep in the time range of 1–104 s. *Figure 2* also shows that the creep strain rate varies three orders of magnitude in the temperature range -20°C to +80°C. In contrast, from *Table 1*, the variation in the elastic modulus over the same temperature range is only 14%. Therefore, in all subsequent calculations the shear modulus will be taken at the mean temperature of the high and the low temperature.

Total creep in the cycle time is closely coupled to the amount of stress relaxation. The stress relaxation curves at a certain temperature are obtained in the following way: The shear stress is proportional to the shear strain. Taking the time derivative of *Equation 1* and substituting *Equation 6*:

$$\dot{\sigma} = -G\dot{\varepsilon}_c = -G \cdot g(\sigma)f(T) \tag{7}$$

For sufficiently small increments Δσ, this can be used to find the time that it takes to realize the stress increment.

$$\Delta t = \frac{\Delta\sigma}{\dot{\sigma}} \tag{8}$$

$\varepsilon \downarrow c\,(\sigma)$ from Schubert model

$$\sigma = G \cdot \varepsilon \downarrow e = G \cdot (\varepsilon \downarrow T - \varepsilon \downarrow c)$$

$$\downarrow$$

$$\sigma = -G\varepsilon \downarrow c$$

$$dt = \Delta\sigma / \sigma$$

$$t = \Sigma dt$$

$$\downarrow$$

$$\sigma(t)$$

T (C)	-20			85		
T (K)	253			358		
G (Tavg)	15949			15949		
strainrate T part	6.95403E-12			1.30246E-08		
shearstress	stress rate	dt	t-cumulative	stress rate	dt	t-cumulative
MPa	MPa/s	s	s	MPa/s		
152	8.17E+06	2.69E-06	2.69E-06	1.53E+10	1.44E-09	1.44E-09
130	2.57E+05	3.89E-05	4.16E-05	4.82E+08	2.08E-08	2.22E-08
120	5.32E+04	1.88E-04	2.30E-04	9.96E+07	1.00E-07	1.23E-07
110	1.10E+04	9.13E-04	1.14E-03	2.05E+07	4.87E-07	6.10E-07
100	2.24E+03	4.46E-03	5.60E-03	4.20E+06	2.38E-06	2.99E-06
90	4.53E+02	2.21E-02	2.77E-02	8.48E+05	1.18E-05	1.48E-05
80	8.97E+01	1.11E-01	1.39E-01	1.68E+05	5.95E-05	7.43E-05
70	1.72E+01	5.81E-01	7.20E-01	3.22E+04	3.10E-04	3.85E-04
60	3.12E+00	3.20E+00	3.92E+00	5.85E+03	1.71E-03	2.09E-03
50	5.17E-01	1.93E+01	2.33E+01	9.68E+02	1.03E-02	1.24E-02
40	7.25E-02	1.38E+02	1.61E+02	1.36E+02	7.36E-02	8.61E-02
30	7.48E-03	1.34E+03	1.50E+03	1.40E+01	7.13E-01	7.99E-01
20	4.07E-04	1.23E+04	1.38E+04	7.63E-01	6.55E+00	7.35E+00
15	5.77E-05	8.67E+04	1.00E+05	1.08E-01	4.63E+01	5.36E+01
10	3.96E-06	5.05E+05	6.05E+05	7.42E-03	2.70E+02	3.23E+02
8	9.26E-07	2.16E+06	2.77E+06	1.73E-03	1.15E+03	1.48E+03
6	1.44E-07	1.39E+07	1.67E+07	2.69E-04	7.42E+03	8.90E+03
4	1.06E-08	1.89E+08	2.06E+08	1.98E-05	1.01E+05	1.10E+05
2	1.23E-10	1.62E+10	1.64E+10	2.31E-07	8.66E+06	8.77E+06

Figure 3: Spreadsheet implementation.

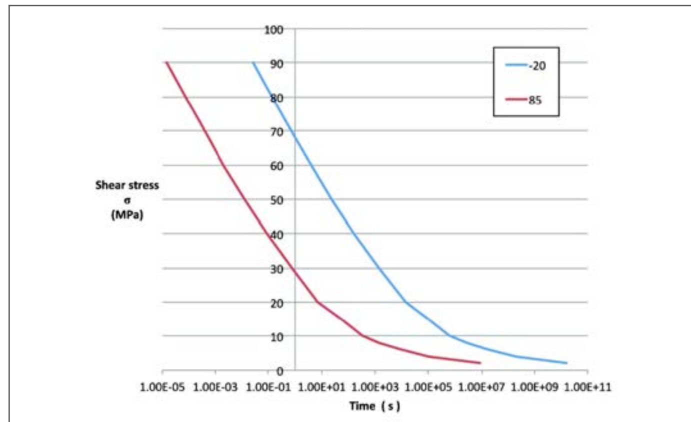

Figure 4: Stress relaxation curves at -20°C and +85°C.

Summing the time increments associated with the stress increments results in an approximation of the stress relaxation over time. The whole scheme is easily implemented in a spreadsheet, as shown in *Figure 3*. The corresponding stress relaxation curves at -20°C and +85°C are shown in *Figure 4*.

Similar curves can be made for different initial stress levels and different temperatures, and these are used to determine how much stress relaxation will take place in a certain creep time. Subsequently the stress-creep strain cycle can be constructed.

VIDEO LED APPLICATION

We consider an idealized temperature cycle with instantaneous temperature change and an equal time at the high and at the low temperature. Four cases are of interest: a) the accelerated test, b) the on/off cycle, c) a long 100 s video cycle, and d) a short 5 s video cycle.

Figure 5 shows the calculated stress/creep strain cycles and Table 2 the load case details and resulting creep strain. In all cases, even in the accelerated test, creep times turn out to be too short for full creep to occur. *Figure 5* and *Table 2* show that using a large temperature step in the accelerated test case works out like intended: the area of the test cycle is much larger compared to the use cycles. Thus failure will be accelerated and the failure energy value can be obtained in shorter time. Creep in the on/ off cycle case is slightly less complete compared to the accelerated case. Therefore using the accelerated test to predict the number of cycles to failure as per the normal design rule in *Equation 3* works out well with a sensible engineering margin of (79/71 - 1) = 11%. This is not the case for the video cycles. Not taking the short time effect into account leads to roughly a factor 2 underestimation in lifetime for the long video cycle. In case of the short video cycle, the temperature excursions are all taken elastically, no creep damage is incurred and use of *Equation 3* is not appropriate at all. This shows that for short cycle times the time effect must be taken into account for correct lifetime prediction of the solder joints.

Table 2. Load Cases

		T_{low}	T_{high}	creep time	ΔT	ε_T	σ_0	% full creep
Case		C	C	s	C		Mpa	
a	Accelerated test	-20	85	3000	105	0.95%	152	79%
b	on/off	35	80	3600	45	0.41%	63	71%
c	long boost	60	90	100	30	0.27%	41	37%
d	short boost	60	80	5	20	0.18%	27	0%

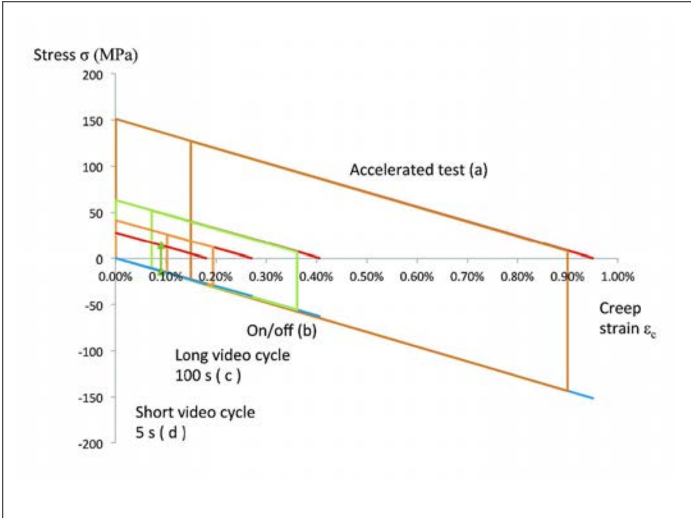

Figure 5: Stress-creep strain loops.

SUMMARY AND CONCLUSION

The effect of short creep time on low cycle fatigue failure of SMD LEDs was investigated. It was shown that for an idealized case with instantaneous temperature change, full creep i.e. stress relaxation to the stress free level and with temperature independent elastic moduli, the creep damage per cycle is proportional to ΔT2. Direct integration was used to construct stress relaxation curves incorporating the highly non-linear behavior of the lead free solder as per the Syed/Schubert model; these were used to construct a simplified stress-strain fatigue cycle, incorporating the effect of creep time. Application to active LEDs in a TV product demonstrated the validity of accelerated testing and the ΔT^2 design rule to product on/off cycles. In contrast, this was not the case for the typical video cycle times.

The short cycle times only allow for partial creep, doing less damage per cycle, and so the use of the uncorrected design rule leads to under prediction of solder joint lifetime. At very short cycle times, the cyclic thermal mismatch is taken fully in elastic excursions with no creep at all, and low cycle fatigue is not the appropriate failure mode. Although the complexity of the solder joint fatigue cycle was very much simplified in the work, the approach was shown to be of merit in clarifying main effects in low cycle solder fatigue, and in enabling correct first order engineering estimations using only a commercial spreadsheet.

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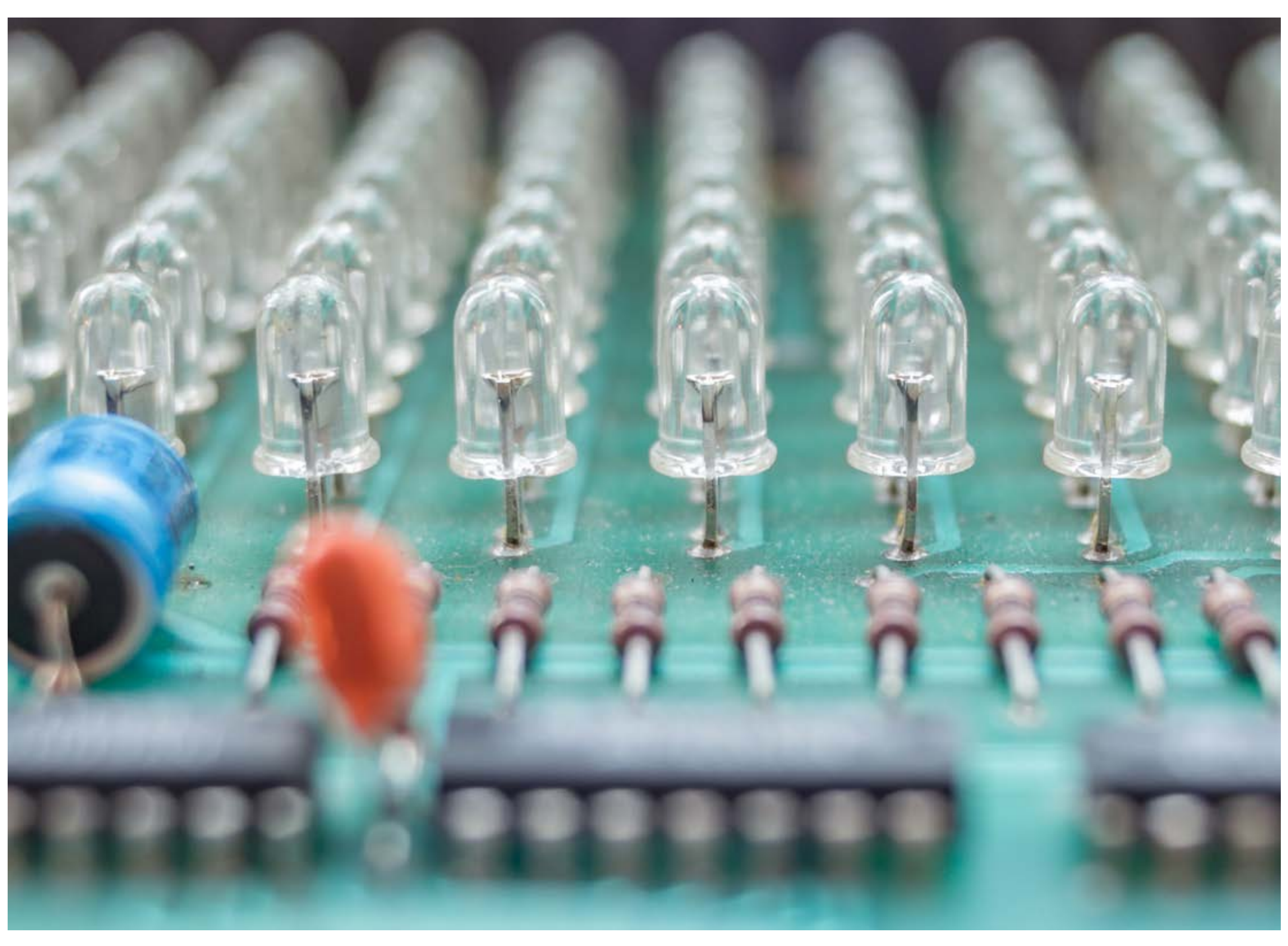

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Genevieve Martin (F) is R&D manager for thermal & mechanics competence at Signify (former Philips Lighting), The Netherlands. She is working in the field of cooling of electronics and thermal management for over twenty years in different application fields. From 2016 to 2019, she coordinates the European project Delphi4LED (3 years project) dealing with multi-domain compact model of LEDs. She served as General chair of Semitherm conference and is an active reviewer and technical committee in key conferences Semi-Therm®, Therminic, Eurosime.

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