

N- and P-Channel 2.5-V (G-S) MOSFET

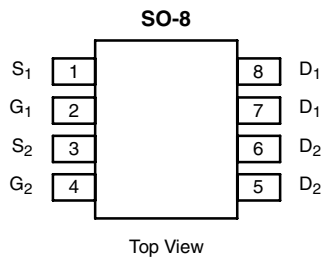
PRODUCT SUMMARY			
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.025 at V _{GS} = 4.5 V	7.1
		0.035 at V _{GS} = 2.5 V	6.0
P-Channel	- 20	0.033 at V _{GS} = - 4.5 V	- 6.2
		0.050 at V _{GS} = - 2.5 V	- 5.0

FEATURES

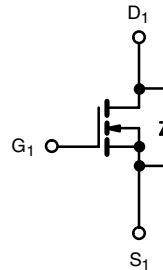
- TrenchFet[®] Power MOSFET: 2.5 Rated



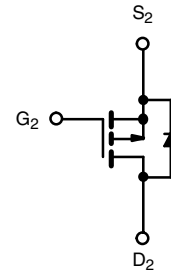
Available
RoHS*
COMPLIANT



Ordering Information: Si4562DY-T1
Si4562DY-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	- 20	V
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	7.1	- 6.2	A
	T _A = 70 °C	5.7	- 4.9	
Pulsed Drain Current	I _{DM}	40	- 40	
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	- 1.7	
Maximum Power Dissipation ^a	T _A = 25 °C	2.0		W
	T _A = 70 °C	1.3		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes:

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted

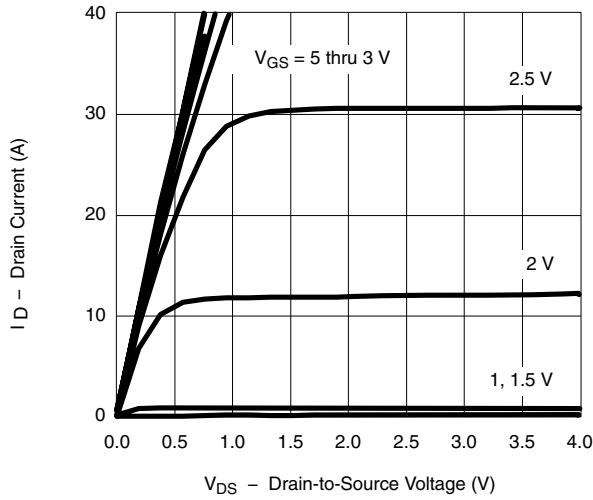
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.6	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.6	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch P-Ch			± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	20			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-20			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 7.1\text{ A}$	N-Ch		0.019	0.025	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -6.2\text{ A}$	P-Ch		0.027	0.033	
		$V_{GS} = 2.5\text{ V}, I_D = 6.0\text{ A}$	N-Ch		0.025	0.035	
		$V_{GS} = -2.5\text{ V}, I_D = -5.0\text{ A}$	P-Ch		0.040	0.050	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 7.1\text{ A}$	N-Ch		27		S
		$V_{DS} = -10\text{ V}, I_D = -6.2\text{ A}$	P-Ch		20		
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\text{ A}, V_{GS} = 0\text{ V}$	N-Ch			1.2	V
		$I_S = -1.7\text{ A}, V_{GS} = 0\text{ V}$	P-Ch			-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.1\text{ A}$	N-Ch		25	50	nC
Gate-Source Charge	Q_{gs}		P-Ch		22	35	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -6.2\text{ A}$	N-Ch		6.5		nC
			P-Ch		7		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		40	60	ns
			P-Ch		27	50	
Rise Time	t_r	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		40	60	ns
			P-Ch		32	50	
Turn-Off Delay Time	$t_{d(off)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		90	150	ns
			P-Ch		95	150	
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		40	60	ns
			P-Ch		45	70	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	N-Ch		40	80	ns
		$I_F = -1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	P-Ch		40	80	

Notes:

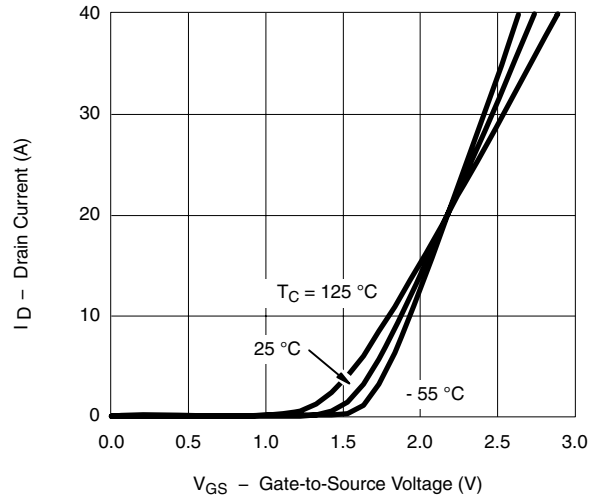
- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

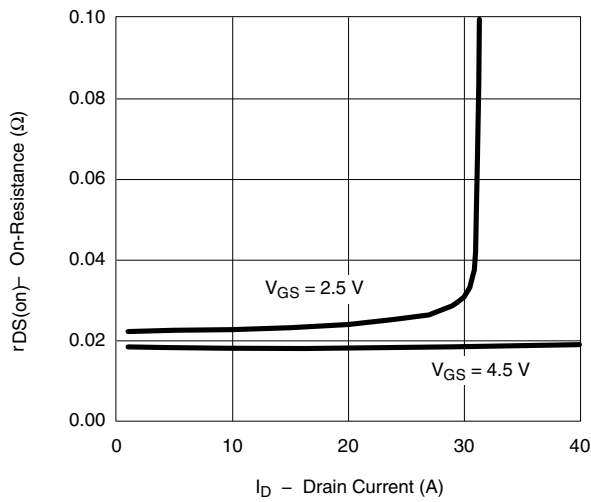
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



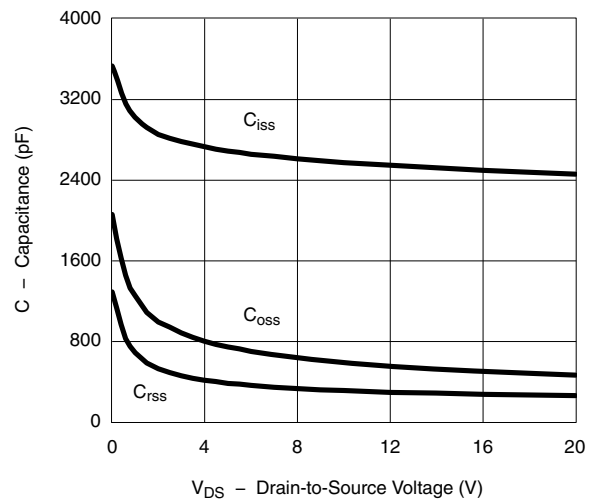
Output Characteristics



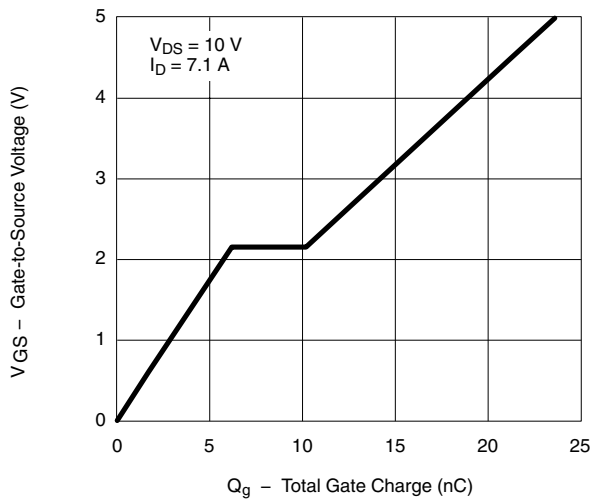
Transfer Characteristics



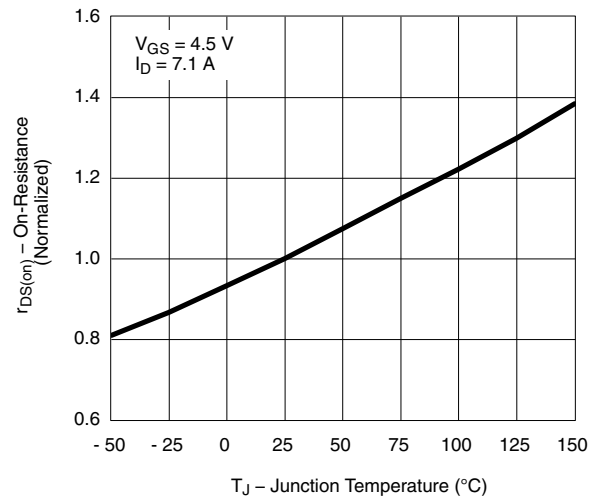
On-Resistance vs. Drain Current



Capacitance

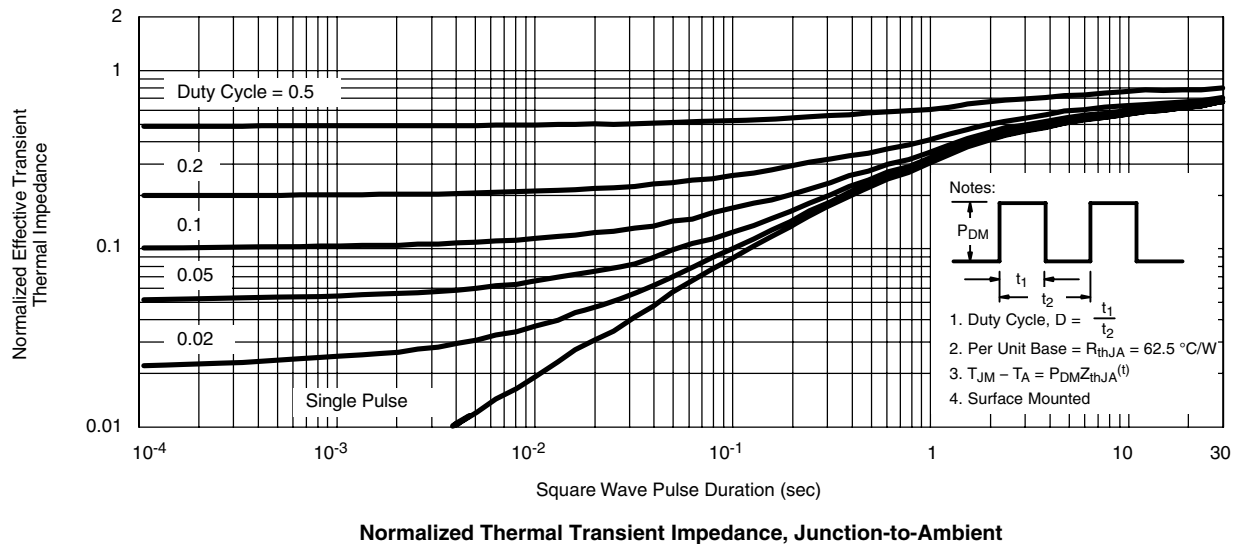
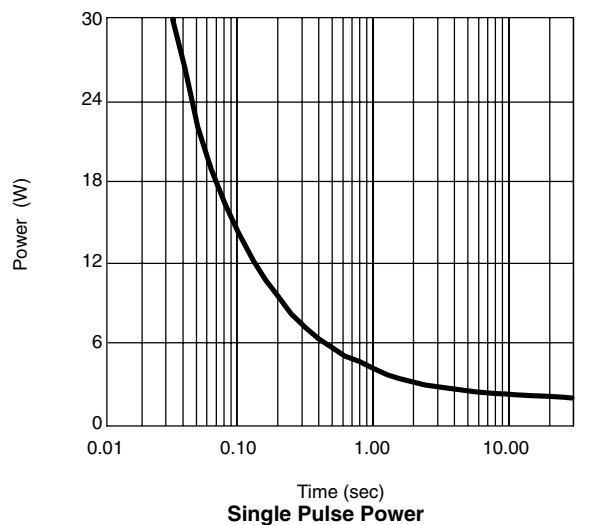
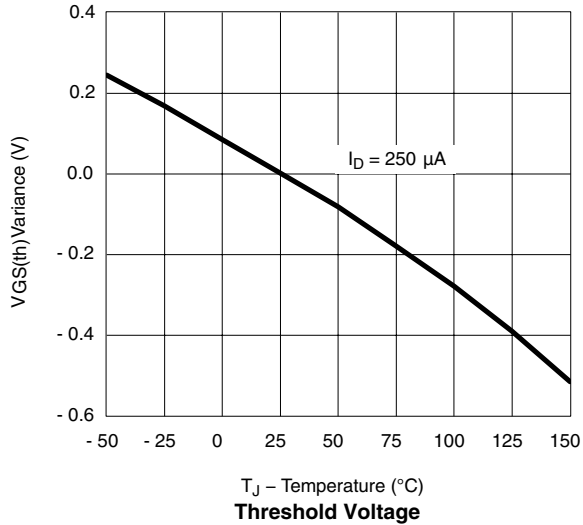
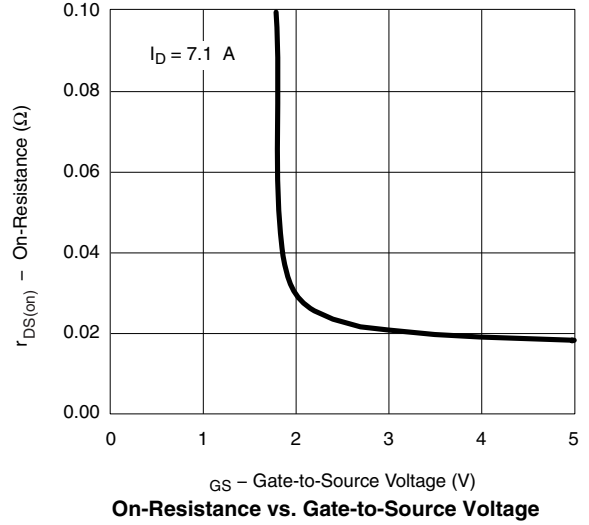
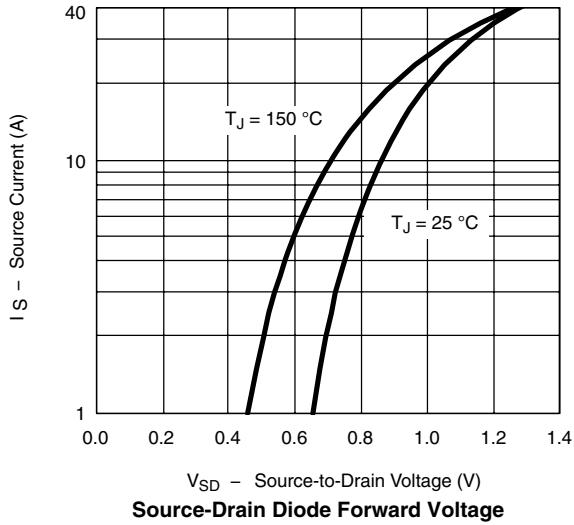


Gate Charge

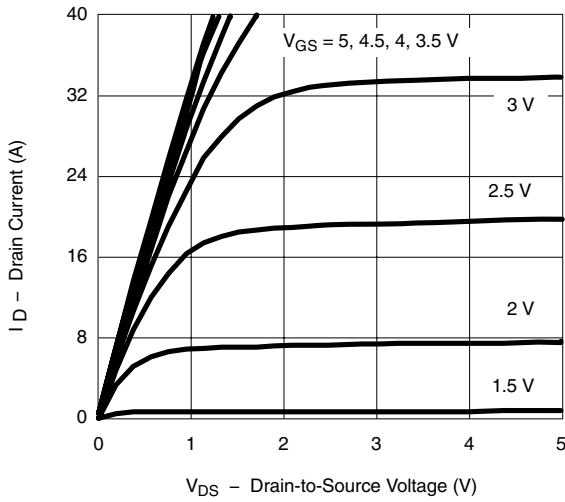


On-Resistance vs. Junction Temperature

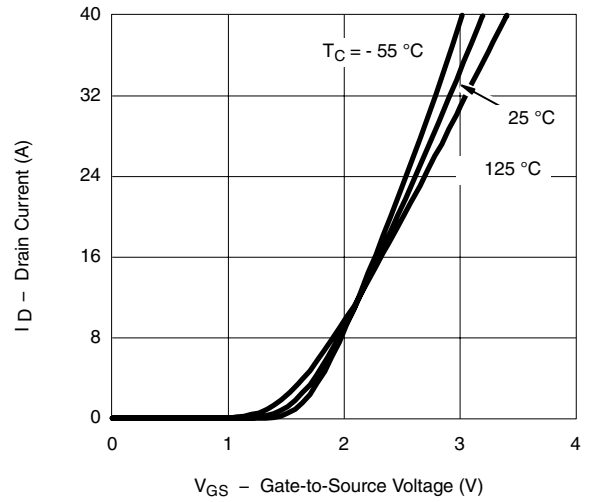
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



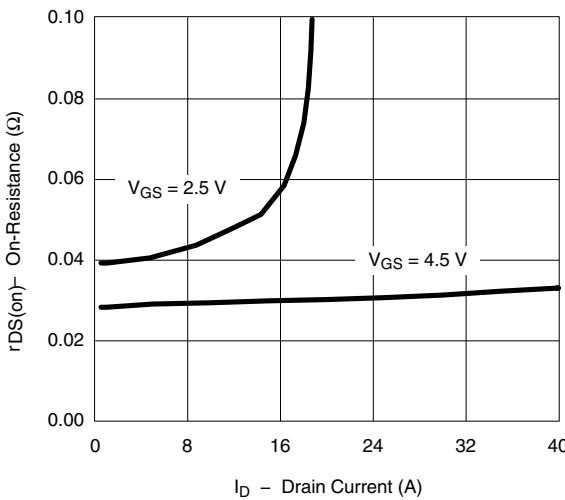
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



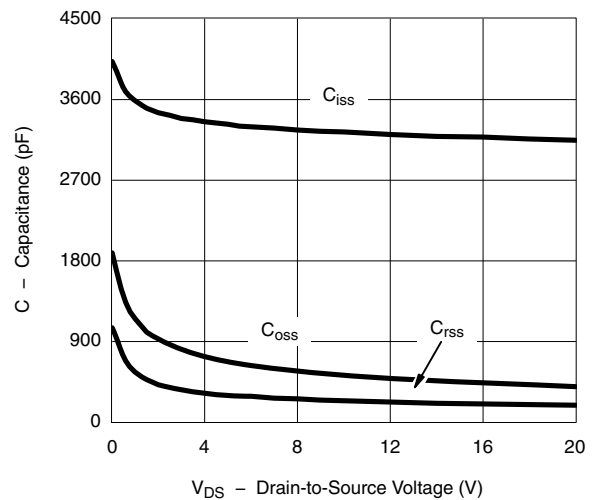
Output Characteristics



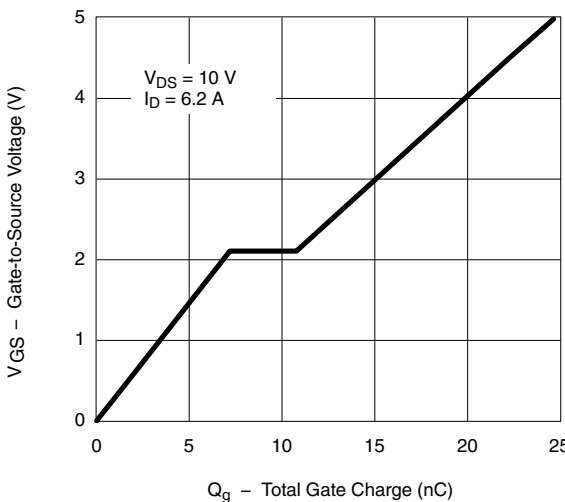
Transfer Characteristics



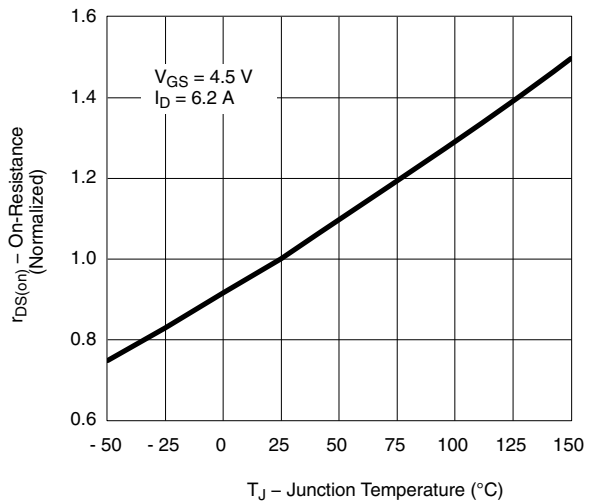
On-Resistance vs. Drain Current



Capacitance

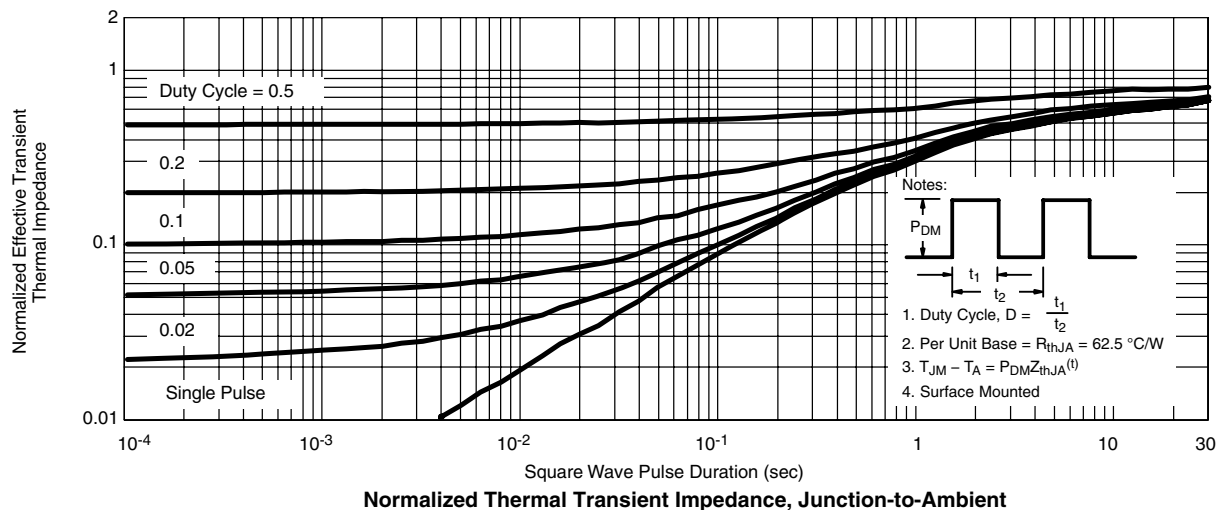
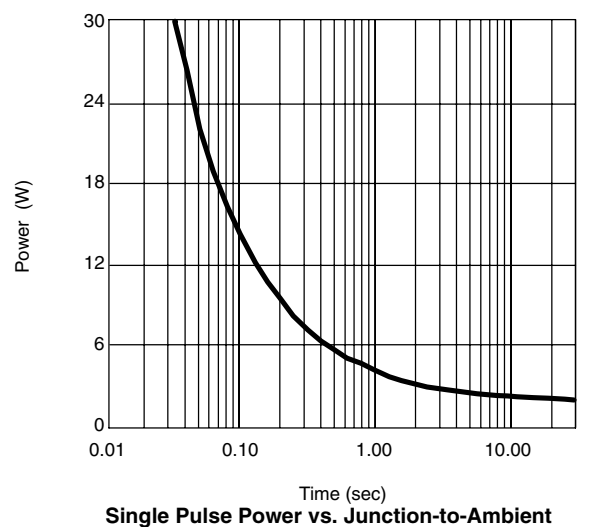
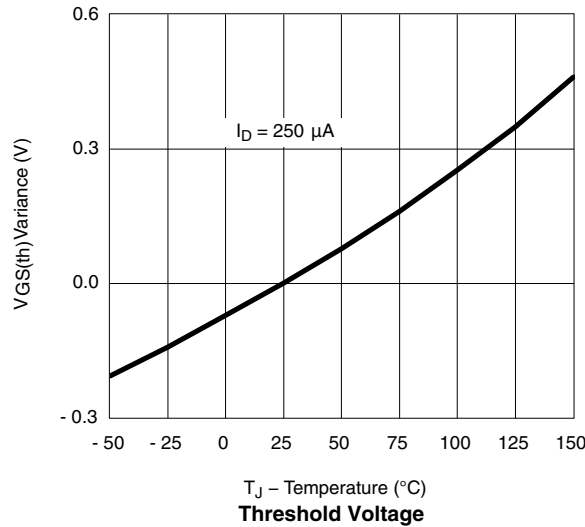
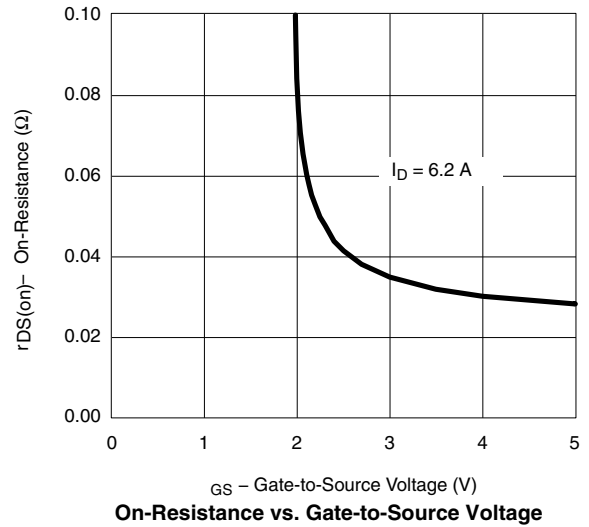
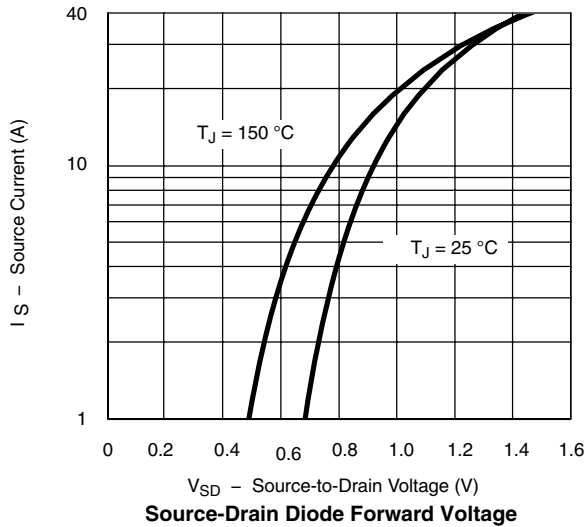


Gate Charge



On-Resistance vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70717>.



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