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ICL50/51, ICK70/71 Schematics Document

Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M

(With ATI MXM/B)

2007-4-20

REV:1A

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Issued Date	2007/04/04	Deciphered Date	2008/04/04	Title: Cover Page
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				Date: Monday, April 23, 2007; Sheet 1 of 48

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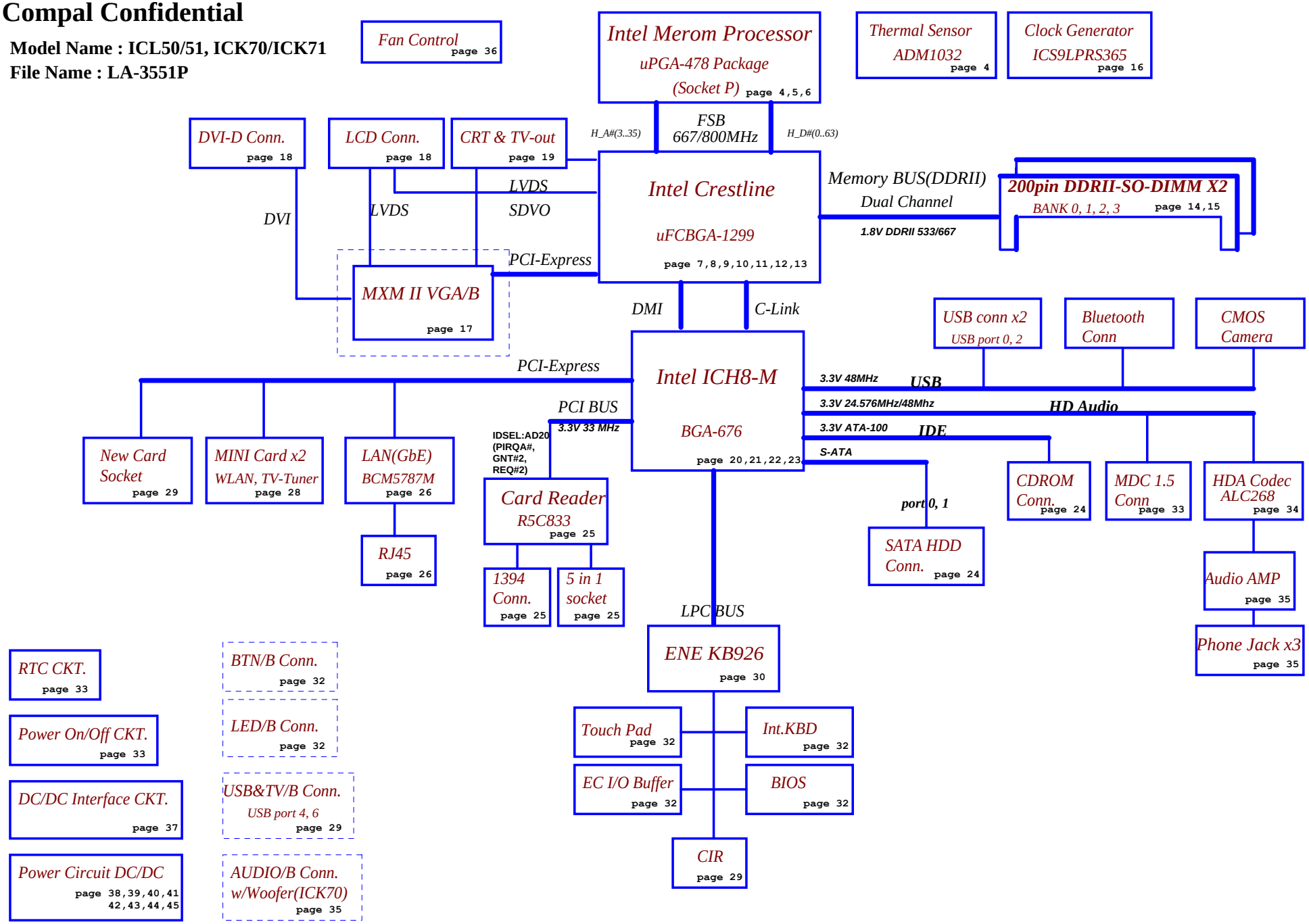
Model Name : ICL50/51, ICK70/ICK71
File Name : LA-3551P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE
			PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@

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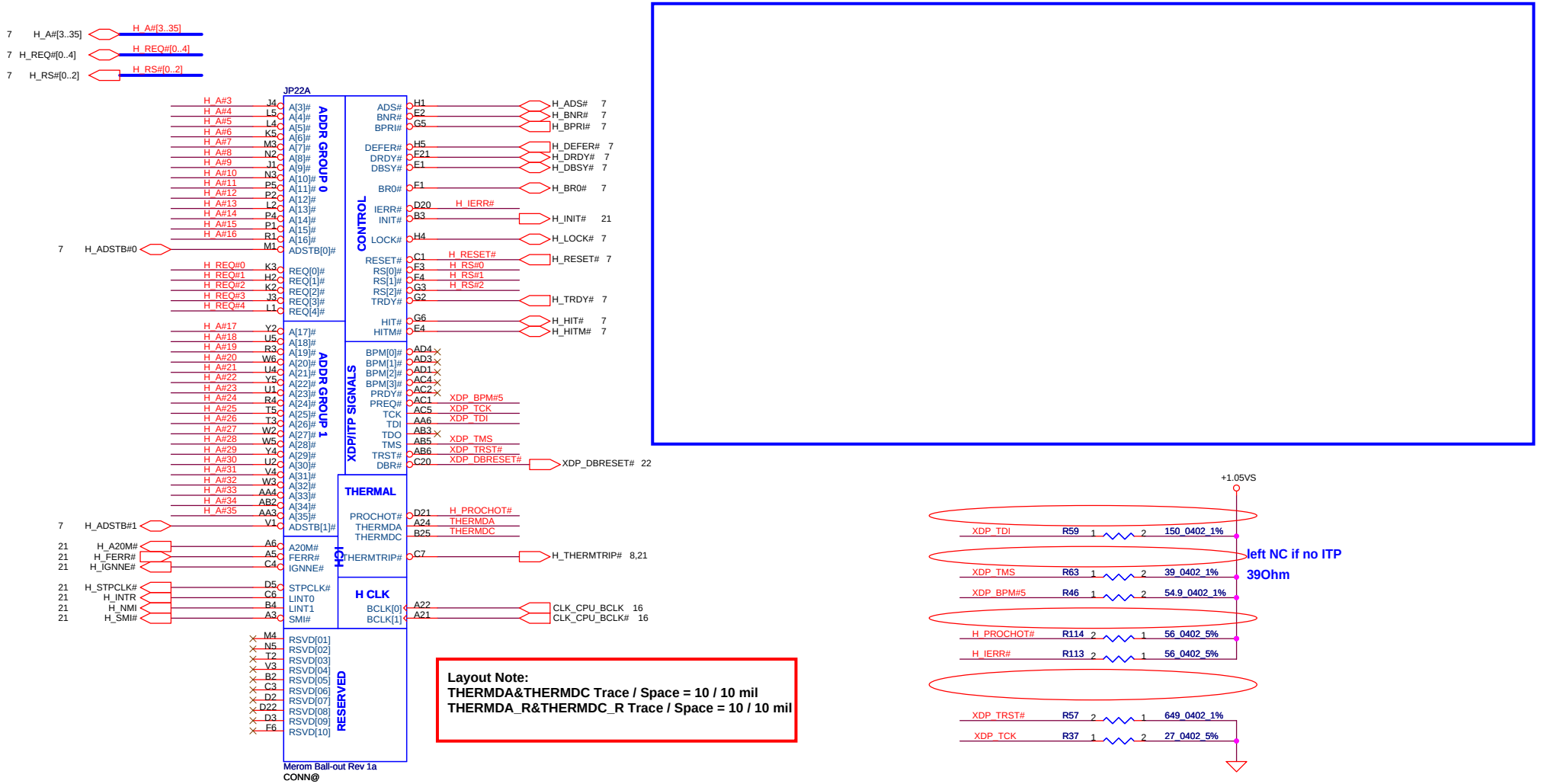
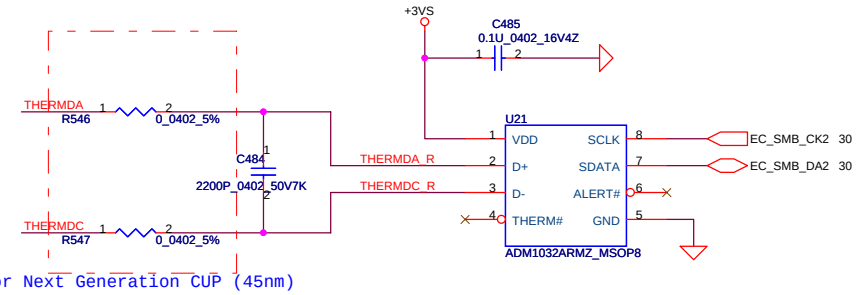


Layout Note:
THERMDA&THERMDC Trace / Space = 10 / 10 mil
THERMDA_R&THERMDC_R Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	1	0	200
0	1	1	166



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Compal Electronics, Inc.

Title: Merom (1/3)

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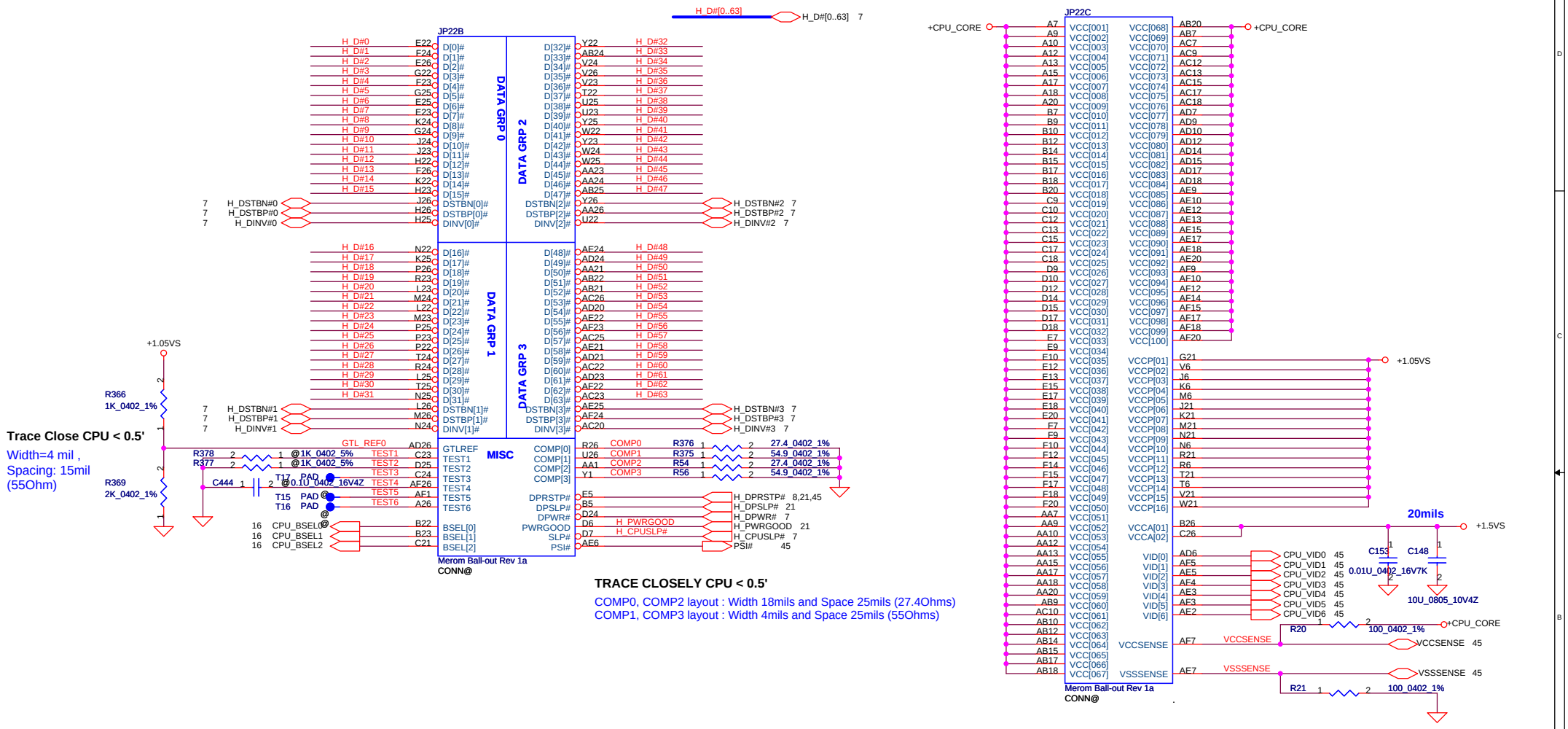

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Compal Electronics, Inc.

Title: Merom (2/3)

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	0.6

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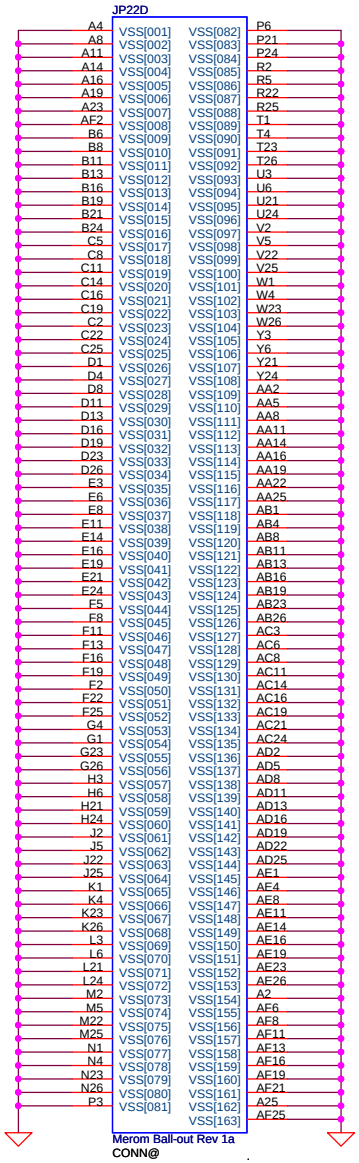
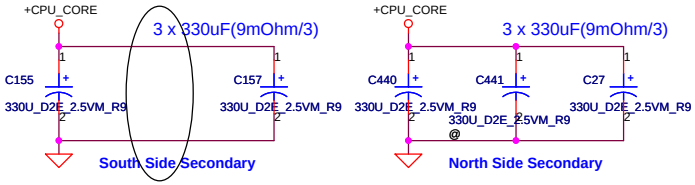
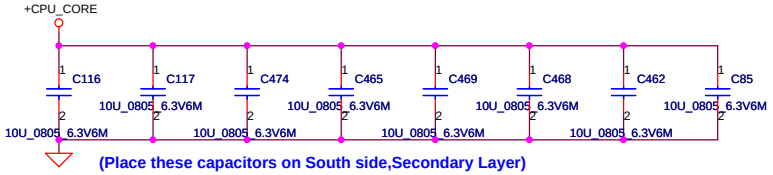
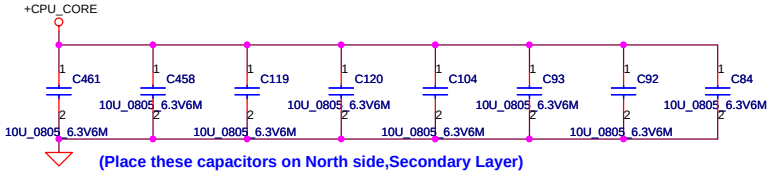
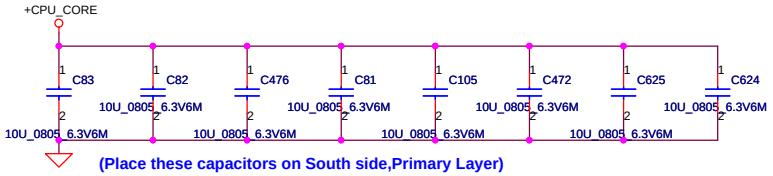
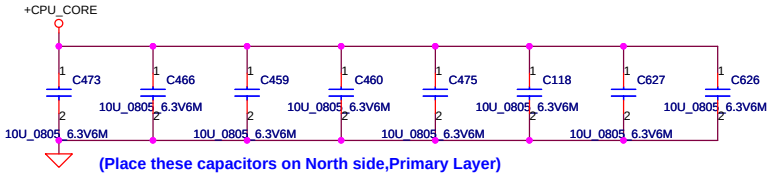




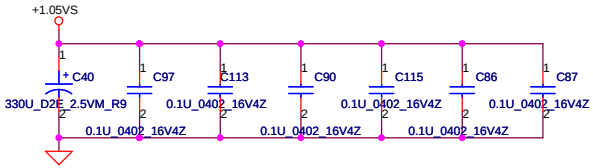








+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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Title: Merom (3/3)

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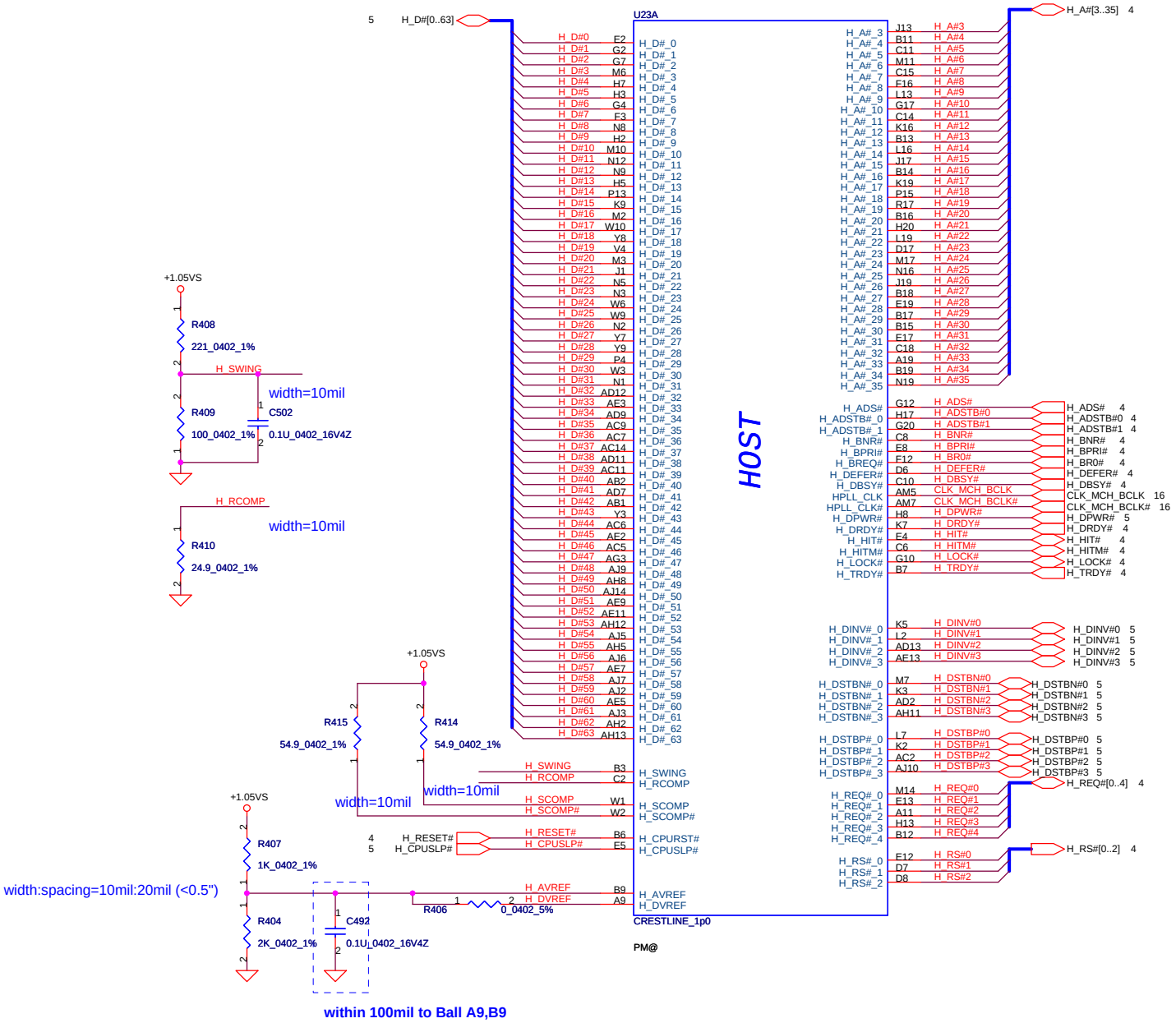

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Compal Electronics, Inc.

Title: Crestline GMCH(1/7)-GTL

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 0.6

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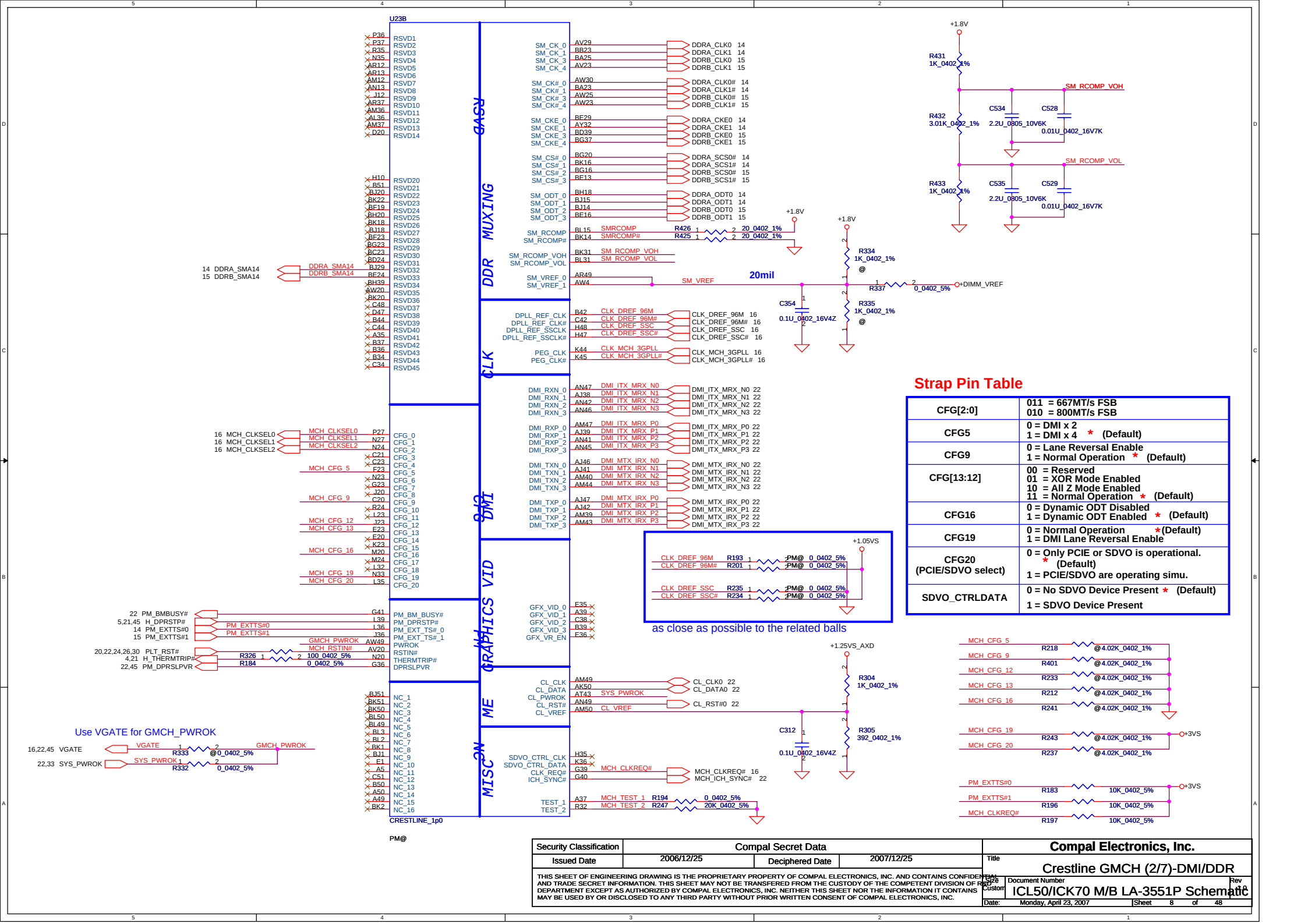

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Title: Crestline GMCH (2/7)-DMI/DDR

Size: Custom | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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14 DDRA_SDQ[0..63] DDRA_SDQ[0..63]

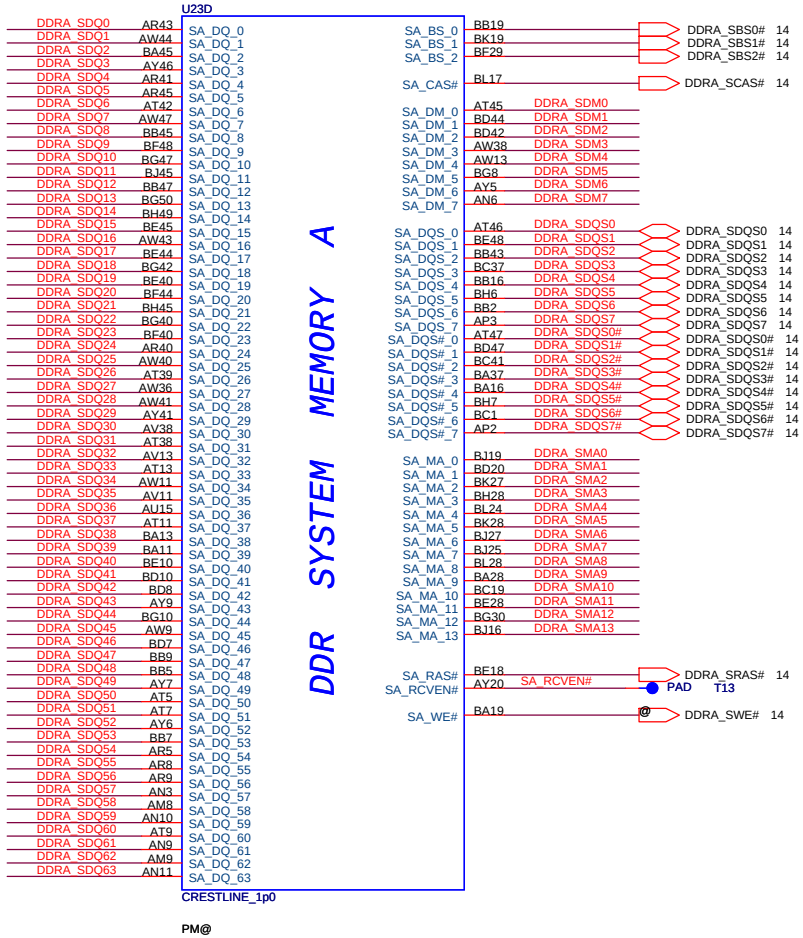
14 DDRA_SDM[0..7] DDRA_SDM[0..7]

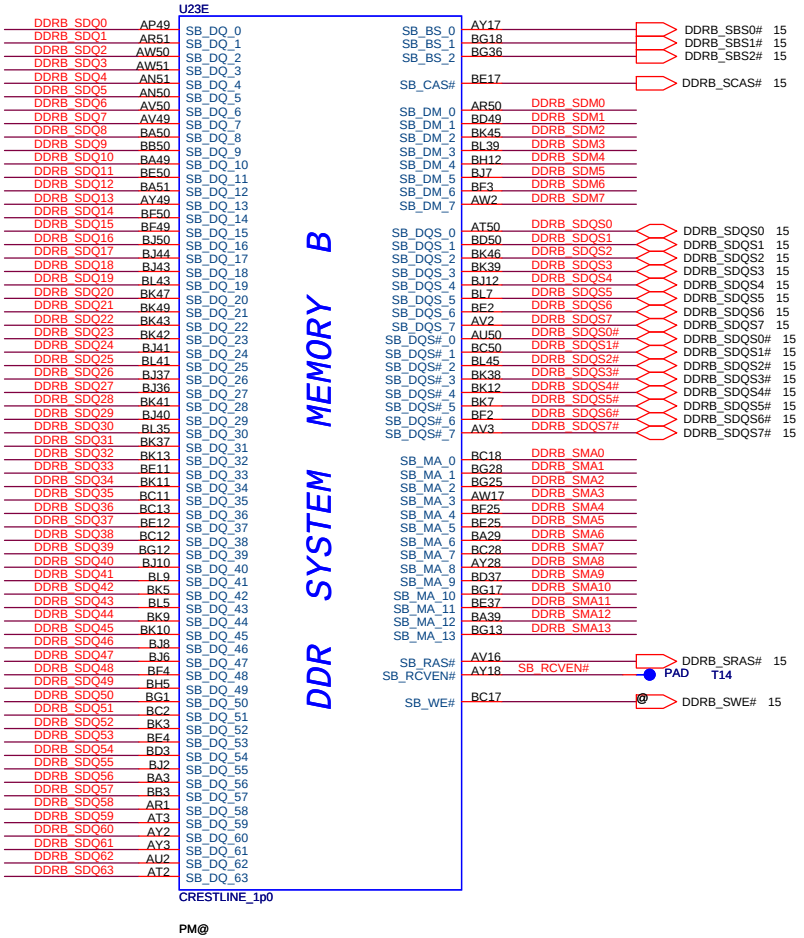
14 DDRA_SMA[0..13] DDRA_SMA[0..13]

15 DDRB_SDQ[0..63] DDRB_SDQ[0..63]

15 DDRB_SDM[0..7] DDRB_SDM[0..7]

15 DDRB_SMA[0..13] DDRB_SMA[0..13]





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Title: Crestline GMCH (3/7)-DDRII

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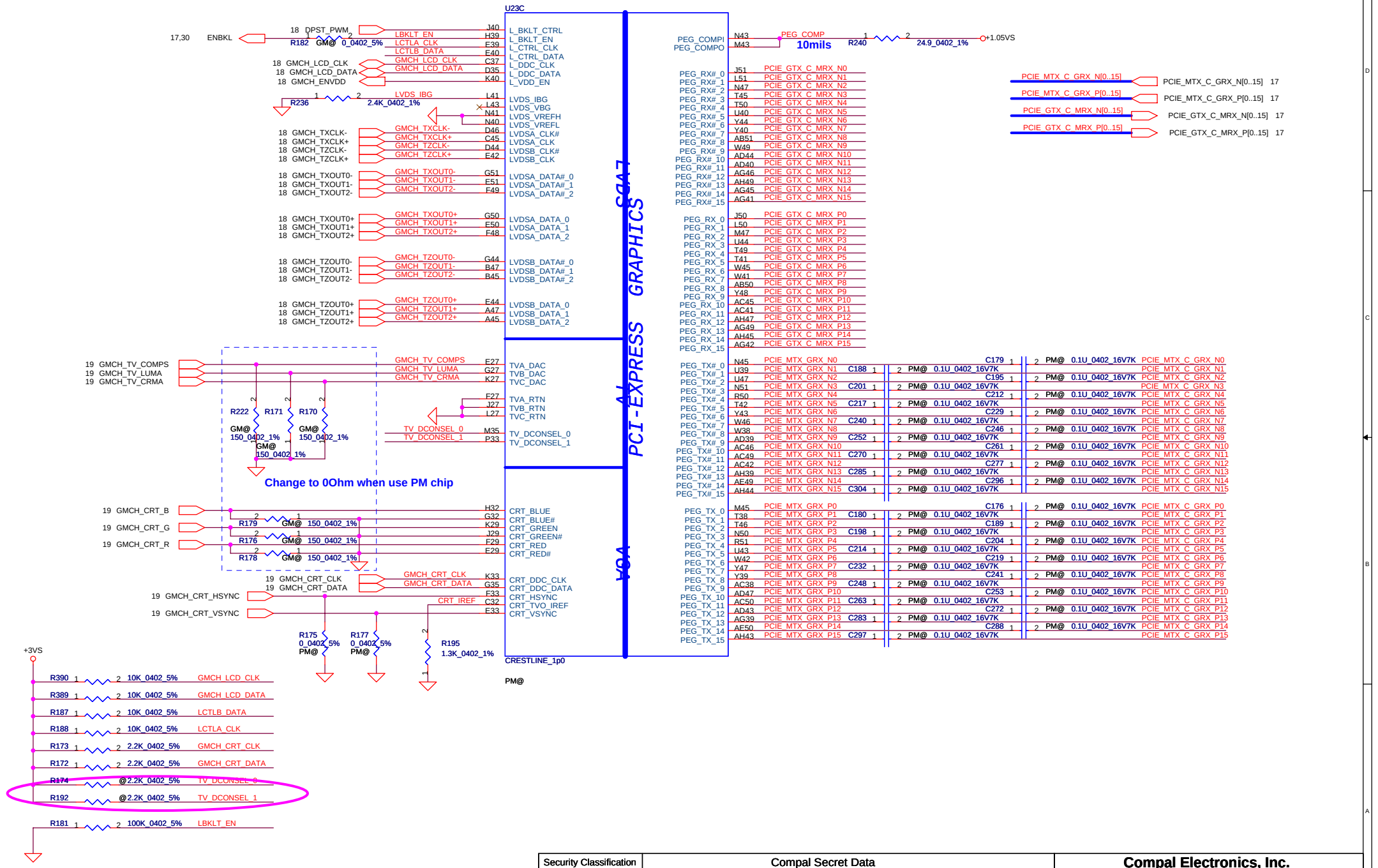

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Crestline GMCH (4/7)-VGA/LVDS/TV

Size	Document Number	Rev
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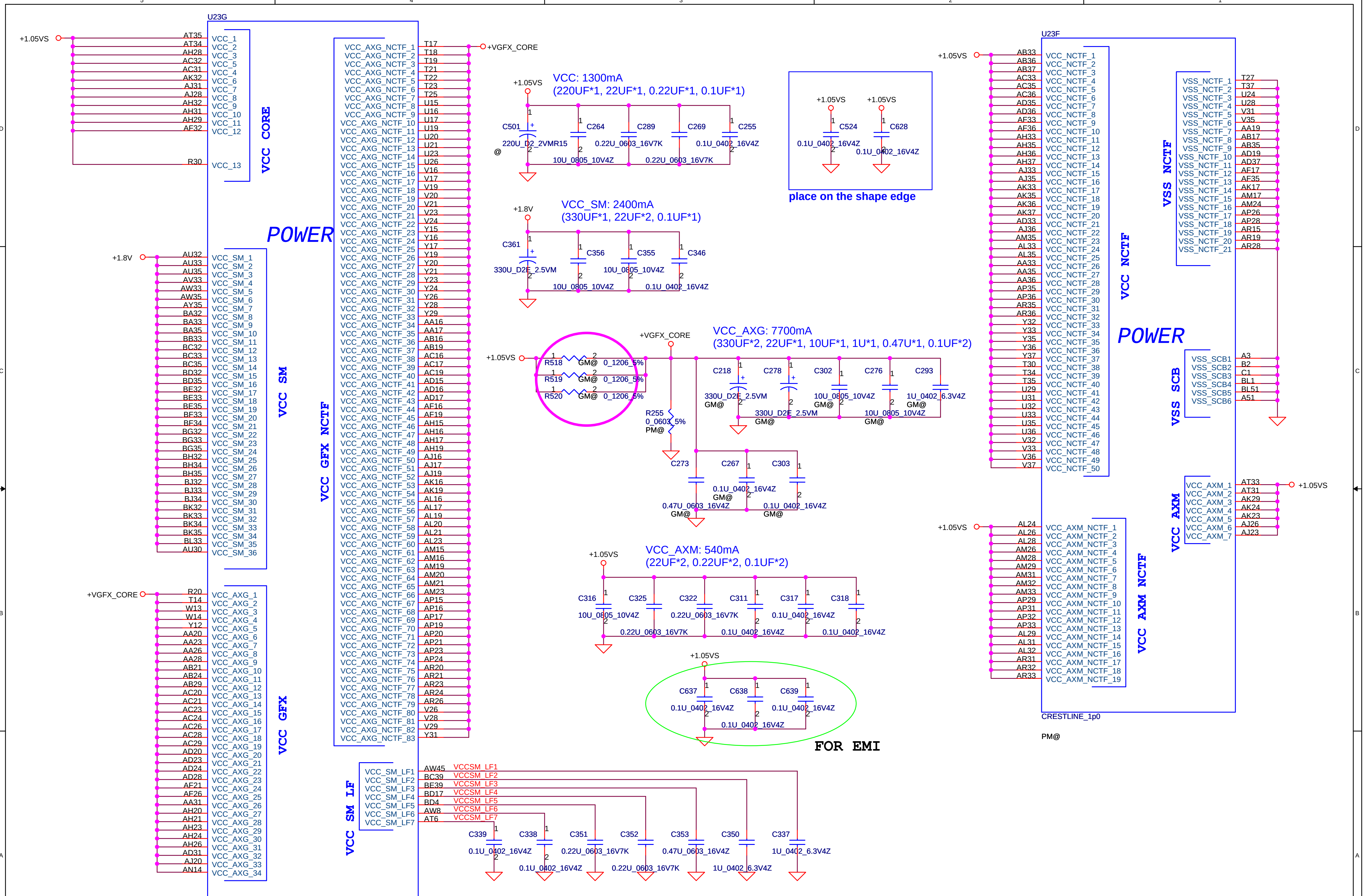

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Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title: Crestline GMCH (5/7)-VCC

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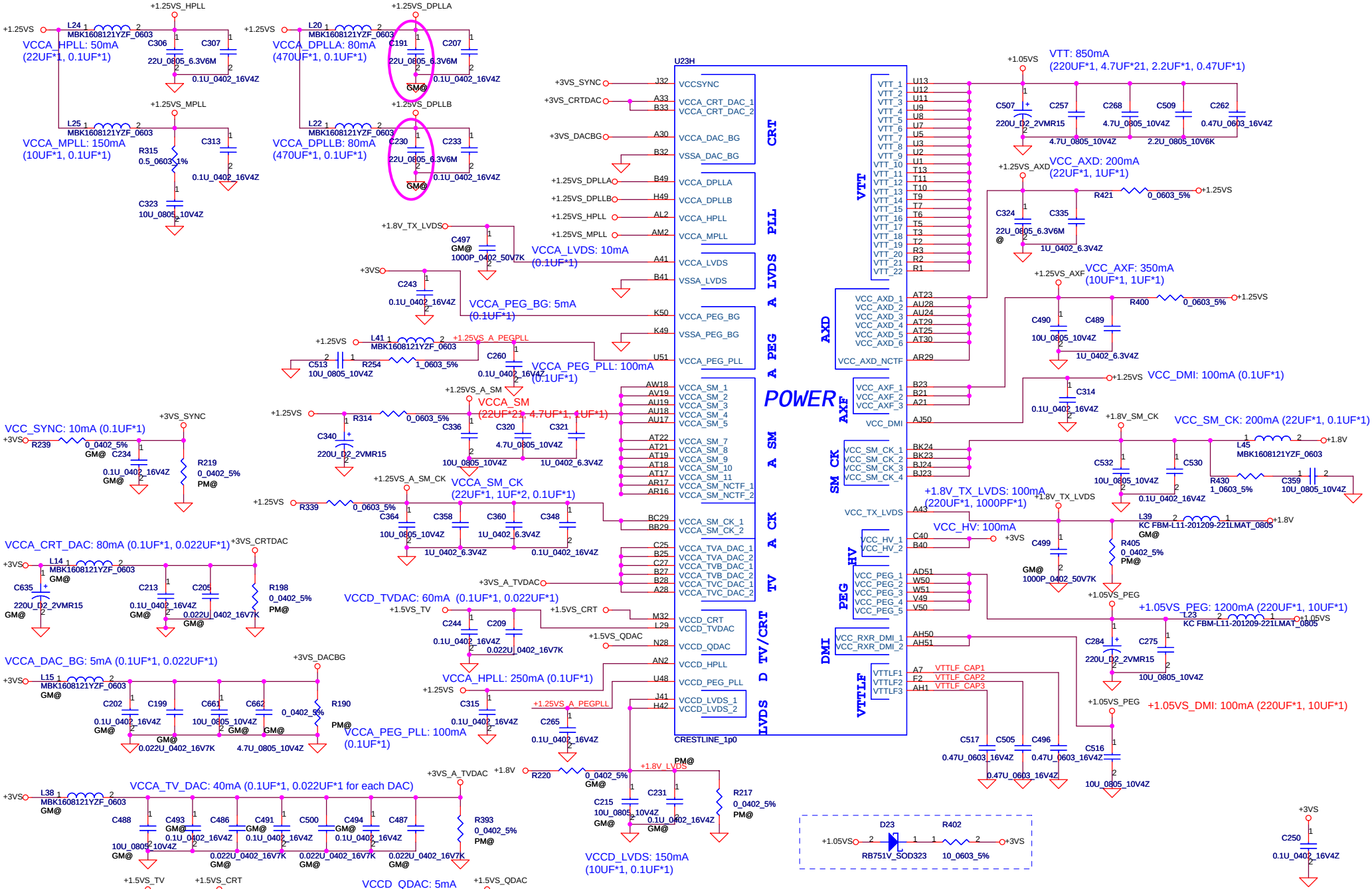

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Title: Crestline GMCH (6/7)-VCC

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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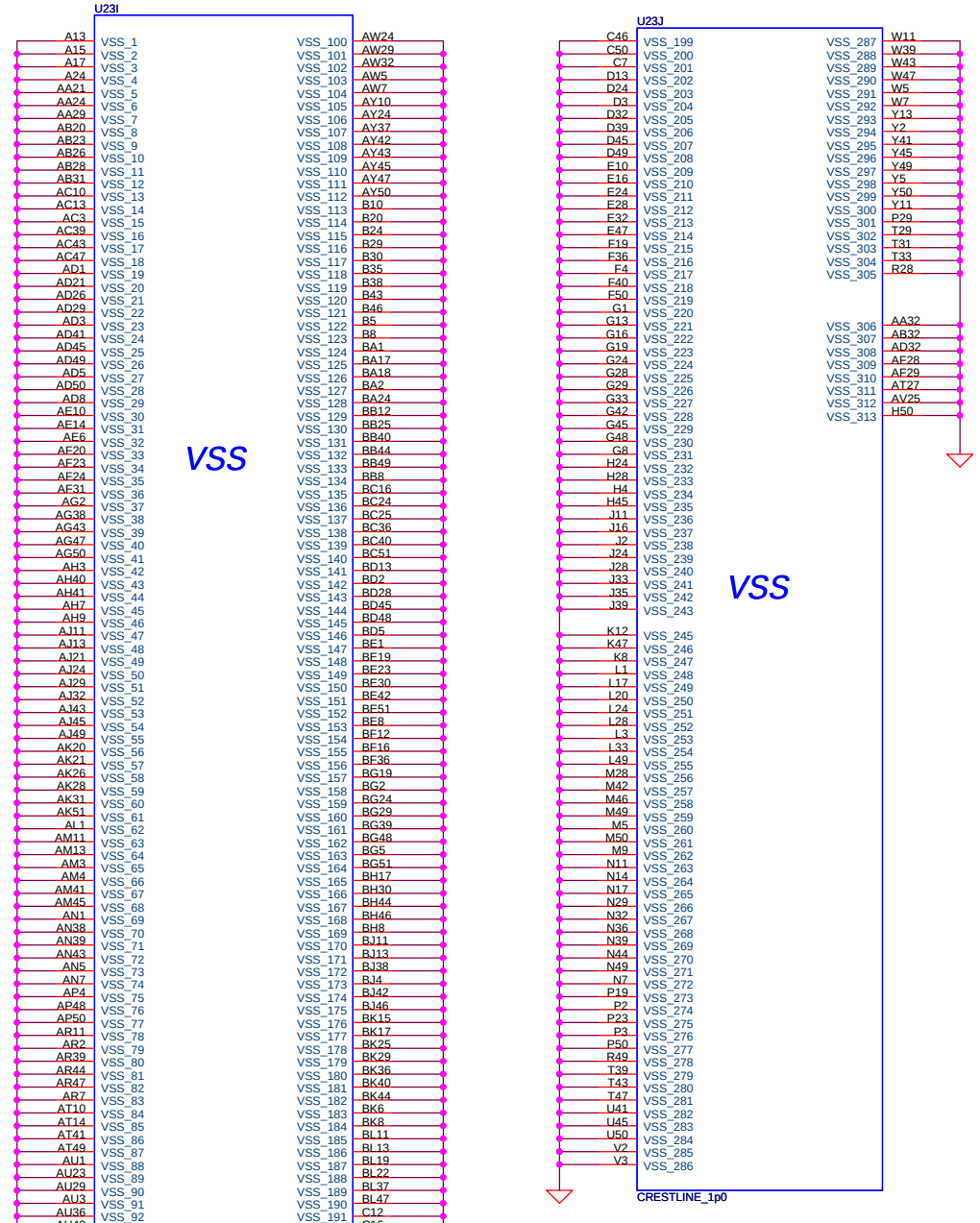

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Title: Crestline GMCH (7/7)-GND

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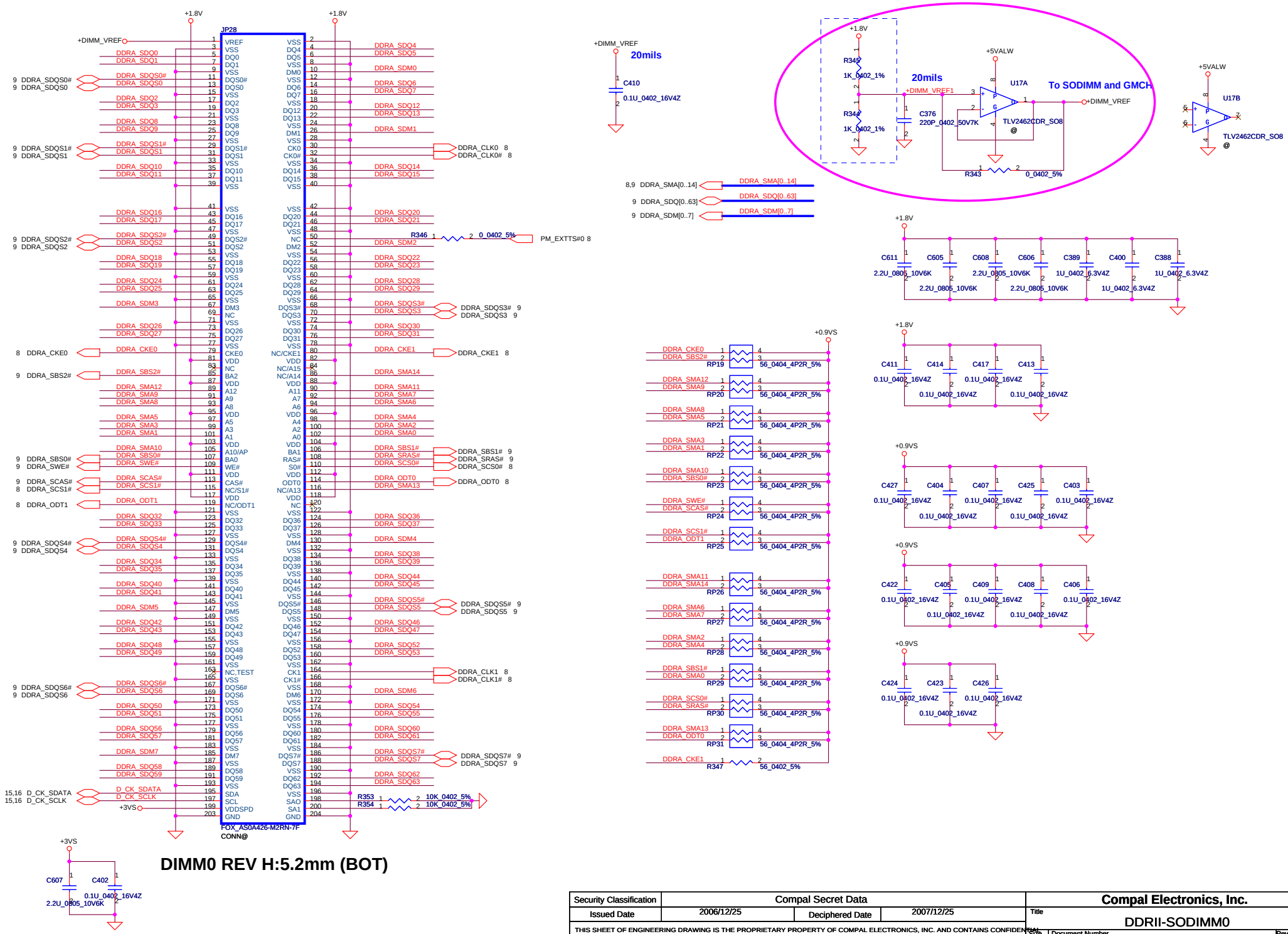

DIMM0 REV H:5.2mm (BOT)

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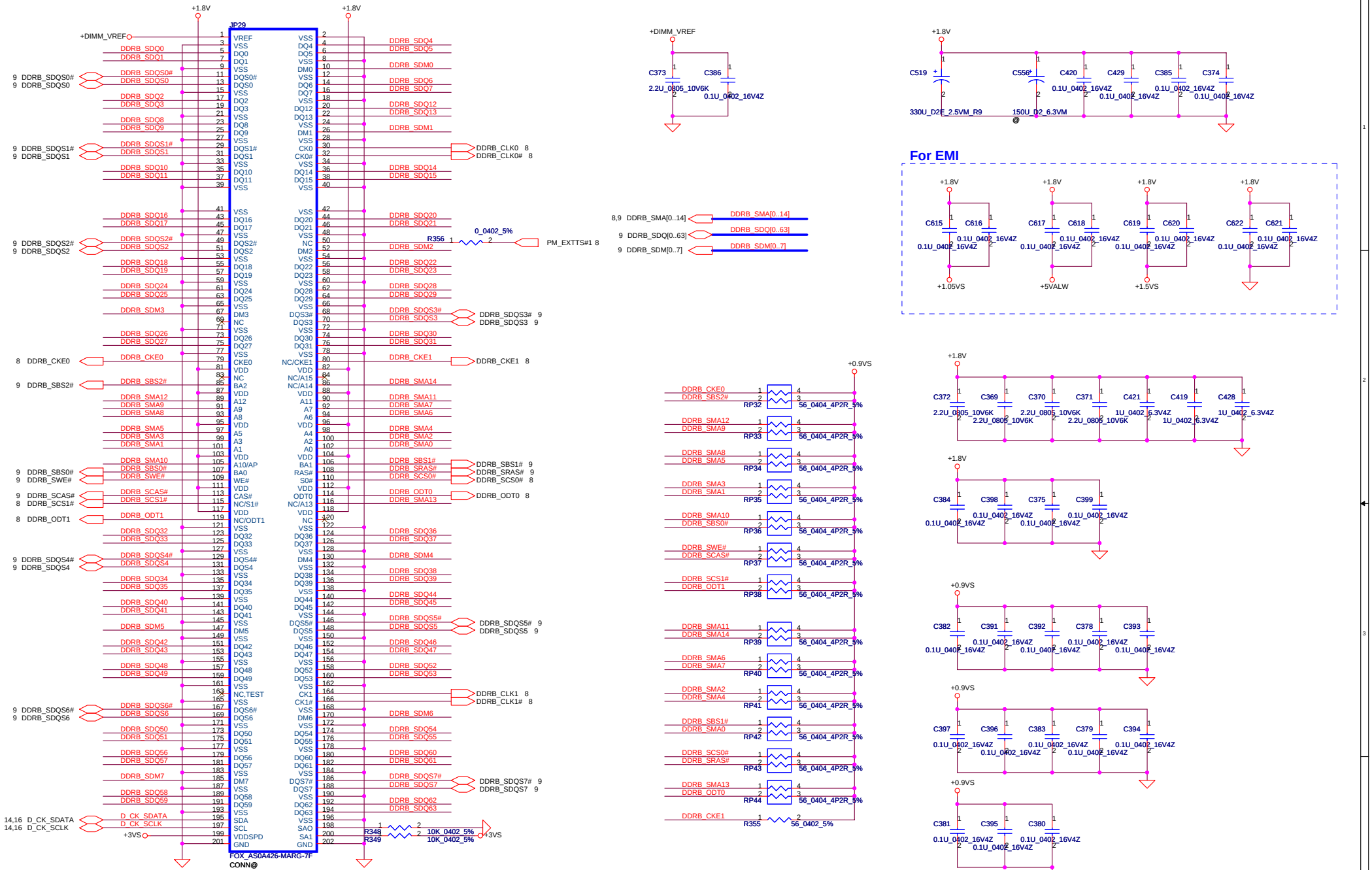

DIMM1 REV H:9.2mm (BOT)

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Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR365

CLK_REQ#	Control	Free-Run
CR#_A(WLAN)	PCIEX2	PCIEX0
CR#_B(MCH)	PCIEX4	PCIEX1
CR#_G(NEW CARD)	PCIEX9	
CR#_H(MINI CARDII)	PCIEX10	

SRC6(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+3VS R104 10K_0402_5% CLK_PCI2

CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)

R106 @10K_0402_5%

mount to Enable ITP_CLK

R107 10K_0402_5% CLK_PCI5

CLK_PCI5=0, Pin46,47is SRC_CLK
CLK_PCI5=1, Pin46,47is ITP_CLK

R91 10K_0402_5% CLK_PCI4

CLK_PCI4=0, Pin17,18 is SRC_CLK
Pin13,14 is DOT96_CLK

R22 @10K_0402_5% CK_PWRGD

22,26,28,29 ICH_SMBDATA — R47 4.7K_0402_5% — +3VS — D_CK_SDATA — Q8 2N7002_SOT23

22,26,28,29 ICH_SMBCLK — R27 4.7K_0402_5% — +3VS — D_CK_SCLK — Q7 2N7002_SOT23

+1.05VS

CLKSEL0: R92 @56_0402_5%; R81 2.2K_0402_5%; R110 1K_0402_5% → MCH_CLKSEL0 8; R100 @1K_0402_5%; R99 0_0402_5% → CPU_BSEL0 5

CLKSEL1: R372 @1K_0402_5%; R370 1K_0402_5% → MCH_CLKSEL1 8; R373 @0_0402_5%; R371 0_0402_5% → CPU_BSEL1 5

CLKSEL2: R363 @1K_0402_5%; R36 10K_0402_5%; R362 1K_0402_5% → MCH_CLKSEL2 8; R35 @0_0402_5%; R364 0_0402_5% → CPU_BSEL2 5

+3VS R25 10K_0402_5% @ CK505_PWRGD → Q5 2N7002_SOT23 @ → CLK_ENABLE# 45

+1.25VS — L10 KC FBM-L11-201209-221LMAT_0805 — C109 10U_0805_10V4Z

+CLK_VDDSRC: C125 10U_0805_10V4Z; C47 0.1U_0402_16V4Z; C49 0.1U_0402_16V4Z; C46 0.1U_0402_16V4Z; C102 0.1U_0402_16V4Z; C103 0.1U_0402_16V4Z; C100 0.1U_0402_16V4Z

+3VS — L9 KC FBM-L11-201209-221LMAT_0805 — C79 10U_0805_10V4Z

+CLK_VDD: C51 10U_0805_10V4Z; C44 0.1U_0402_16V4Z; C45 0.1U_0402_16V4Z; C48 0.1U_0402_16V4Z; C99 0.1U_0402_16V4Z; C98 0.1U_0402_16V4Z; C101 0.1U_0402_16V4Z

mount to Enable ITP_CLK

U1 ICS9LPRS365AGLFT_TSSOP64

+CLK_VDD: VDDPCI, VDD48, VDDPLL3, VDDREF, VDDSRC, VDDCPU

+CLK_VDDSRC: VDD96_IO, VDDPLL3_IO, VDDSRC_IO, VDDSRC_IO, VDDCPU_IO

+3VS R72 10K_0402_5%

28 MINI1_CLKREQ# — R76 475_0402_1% — PCI0/CR#_A

8 MCH_CLKREQ# — R90 475_0402_1% — PCI1/CR#_B

25 CLK_PCI_1394 — CLK_PCI_1394 — R105 33_0402_5% — CLK_PCI2 — PCI2/TME

30 CLK_PCI_LPC — CLK_PCI_LPC — R79 33_0402_5% — CLK_PCI3 — PCI3

CLK_PCI4 — PCI4/27_Select

20 CLK_PCI_ICH — CLK_PCI_ICH — R75 33_0402_5% — CLK_PCI5 — PCI_F5/ITP_EN

C32 33P_0402_50V8J — CLK_XTALIN — X1

Y1 14.31818MHz_20P_FSX8L14.318181M20FDB

C33 33P_0402_50V8J — CLK_XTALOUT — X2

22 CLK_ICH_48M — CLK_ICH_48M — R80 33_0402_5% — CLKSEL0 — USB_48MHZ/FSLA

CLKSEL1 — FSLB/TEST_MODE

22 CLK_ICH_14M — CLK_ICH_14M — R43 33_0402_5% — CLKSEL2 — REF0/FSLC/TEST_SEL

+CLK_VDDSRC — VDDSRC_IO

GNDSRC, GNDPCI, GND48, GND, GND, GNDCPU, GNDSRC, GNDSRC, GNDREF

NC

SCLK — D_CK_SCLK — D_CK_SCLK 14,15
SDATA — D_CK_SDATA — D_CK_SDATA 14,15

PCI_STOP# — PM_STP_PCI# — PM_STP_PCI# 22
CPU_STOP# — PM_STP_CPU# — PM_STP_CPU# 22

CPU0 — CLK_CPU0 — R44 0_0402_5% — CLK_CPU_BCLK — CLK_CPU_BCLK 4
CPU0# — CLK_CPU0# — R45 0_0402_5% — CLK_CPU_BCLK# — CLK_CPU_BCLK# 4

CPU1_F — CLK_CPU1 — R31 0_0402_5% — CLK_MCH_BCLK — CLK_MCH_BCLK 7
CPU1#_F — CLK_CPU1# — R32 0_0402_5% — CLK_MCH_BCLK# — CLK_MCH_BCLK# 7

SRC8/CPU2_ITP — CLK_SRC8 — R39 0_0402_5% — CLK_PCIE_LAN — CLK_PCIE_LAN 26
SRC8#/CPU2_ITP# — CLK_SRC8# — R40 0_0402_5% — CLK_PCIE_LAN# — CLK_PCIE_LAN# 26

SRC10 — CLK_SRC10 — R53 0_0402_5% — CLK_PCIE_MINI2 — CLK_PCIE_MINI2 28
SRC10# — CLK_SRC10# — R52 0_0402_5% — CLK_PCIE_MINI2# — CLK_PCIE_MINI2# 28

SRC11/CR#_H — R55 475_0402_1%
SRC11#/CR#_G — R97 475_0402_1% — MINI2_CLKREQ# 28; EXP_CLKREQ# 29
R60 10K_0402_5% +3VS; R103 10K_0402_5% +3VS

SRC9 — CLK_SRC9 — R73 0_0402_5% — CLK_PCIE_CARD — CLK_PCIE_CARD 29
SRC9# — CLK_SRC9# — R74 0_0402_5% — CLK_PCIE_CARD# — CLK_PCIE_CARD# 29

SRC7/CR#_F — CLK_SRC7 — R33 0_0402_5% — CLK_PCIE_SATA — CLK_PCIE_SATA 21
SRC7#/CR#_E — CLK_SRC7# — R34 0_0402_5% — CLK_PCIE_SATA# — CLK_PCIE_SATA# 21

SRC6 — CLK_SRC6 — R41 PM@ 0_0402_5% — CLK_PCIE_VGA — CLK_PCIE_VGA 17
SRC6# — CLK_SRC6# — R42 PM@ 0_0402_5% — CLK_PCIE_VGA# — CLK_PCIE_VGA# 17

UMA: disable this pair by BIOS

SRC4 — CLK_SRC4 — R86 0_0402_5% — CLK_MCH_3GPLL — CLK_MCH_3GPLL 8
SRC4# — CLK_SRC4# — R87 0_0402_5% — CLK_MCH_3GPLL# — CLK_MCH_3GPLL# 8

SRC3/CR#_C — CLK_SRC3 — R95 0_0402_5% — CLK_PCIE_ICH — CLK_PCIE_ICH 22
SRC3#/CR#_D — CLK_SRC3# — R96 0_0402_5% — CLK_PCIE_ICH# — CLK_PCIE_ICH# 22

SRC2/SATA — CLK_SRC2 — R84 0_0402_5% — CLK_PCIE_MINI1 — CLK_PCIE_MINI1 28
SRC2#/SATA# — CLK_SRC2# — R85 0_0402_5% — CLK_PCIE_MINI1# — CLK_PCIE_MINI1# 28

SRC1/SE1/27MHz_NonSS — CLK_SRC1 — R93 GM@ 0_0402_5% — CLK_DREF_SSC — CLK_DREF_SSC 8
SRC1#/SE2/27MHz_SS — CLK_SRC1# — R94 GM@ 0_0402_5% — CLK_DREF_SSC# — CLK_DREF_SSC# 8

SRC0/DOT96 — CLK_DOT — R82 GM@ 0_0402_5% — CLK_DREF_96M — CLK_DREF_96M 8
SRC0#/DOT96# — CLK_DOT# — R83 GM@ 0_0402_5% — CLK_DREF_96M# — CLK_DREF_96M# 8

CK_PWRGD/PD# — CK505_PWRGD — R29 0_0402_5% — CK_PWRGD 22
R30 @ 0_0402_5% — VGATE 8,22,45

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 0.6

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10 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
10 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

JP19A

+MXM_B+ 1,3,5,7,9,11,13,15 PWR_SRC
17,19,21,23 GND
2,4,6,8,10,12,14 1V8RUN → +1.8VS
140mil(3.5A)
16 RUNPWROK → VGA_ON 33
18 5VRUN → +5VS
20,22,24 GND

PCIE_GTX_C_MRX_N15	25	PEX_RX15#	PRSNT2# 26
PCIE_GTX_C_MRX_P15	27	PEX_RX15	PEX_TX15# 28 PCIE_MTX_C_GRX_N15
	29	GND	PEX_TX15 30 PCIE_MTX_C_GRX_P15
PCIE_GTX_C_MRX_N14	31	PEX_RX14#	GND 32
PCIE_GTX_C_MRX_P14	33	PEX_RX14	PEX_TX14# 34 PCIE_MTX_C_GRX_N14
	35	GND	PEX_TX14 36 PCIE_MTX_C_GRX_P14
PCIE_GTX_C_MRX_N13	37	PEX_RX13#	GND 38
PCIE_GTX_C_MRX_P13	39	PEX_RX13	PEX_TX13# 40 PCIE_MTX_C_GRX_N13
	41	GND	PEX_TX13 42 PCIE_MTX_C_GRX_P13
PCIE_GTX_C_MRX_N12	43	PEX_RX12#	GND 44
PCIE_GTX_C_MRX_P12	45	PEX_RX12	PEX_TX12# 46 PCIE_MTX_C_GRX_N12
	47	GND	PEX_TX12 48 PCIE_MTX_C_GRX_P12
PCIE_GTX_C_MRX_N11	49	PEX_RX11#	GND 50
PCIE_GTX_C_MRX_P11	51	PEX_RX11	PEX_TX11# 52 PCIE_MTX_C_GRX_N11
	53	GND	PEX_TX11 54 PCIE_MTX_C_GRX_P11
PCIE_GTX_C_MRX_N10	55	PEX_RX10#	GND 56
PCIE_GTX_C_MRX_P10	57	PEX_RX10	PEX_TX10# 58 PCIE_MTX_C_GRX_N10
	59	GND	PEX_TX10 60 PCIE_MTX_C_GRX_P10
PCIE_GTX_C_MRX_N9	61	PEX_RX9#	GND 62
PCIE_GTX_C_MRX_P9	63	PEX_RX9	PEX_TX9# 64 PCIE_MTX_C_GRX_N9
	65	GND	PEX_TX9 66 PCIE_MTX_C_GRX_P9
PCIE_GTX_C_MRX_N8	67	PEX_RX8#	GND 68
PCIE_GTX_C_MRX_P8	69	PEX_RX8	PEX_TX8# 70 PCIE_MTX_C_GRX_N8
	71	GND	PEX_TX8 72 PCIE_MTX_C_GRX_P8
PCIE_GTX_C_MRX_N7	73	PEX_RX7#	GND 74
PCIE_GTX_C_MRX_P7	75	PEX_RX7	PEX_TX7# 76 PCIE_MTX_C_GRX_N7
	77	GND	PEX_TX7 78 PCIE_MTX_C_GRX_P7
PCIE_GTX_C_MRX_N6	79	PEX_RX6#	GND 80
PCIE_GTX_C_MRX_P6	81	PEX_RX6	PEX_TX6# 82 PCIE_MTX_C_GRX_N6
	83	GND	PEX_TX6 84 PCIE_MTX_C_GRX_P6
PCIE_GTX_C_MRX_N5	85	PEX_RX5#	GND 86
PCIE_GTX_C_MRX_P5	87	PEX_RX5	PEX_TX5# 88 PCIE_MTX_C_GRX_N5
	89	GND	PEX_TX5 90 PCIE_MTX_C_GRX_P5
PCIE_GTX_C_MRX_N4	91	PEX_RX4#	GND 92
PCIE_GTX_C_MRX_P4	93	PEX_RX4	PEX_TX4# 94 PCIE_MTX_C_GRX_N4
	95	GND	PEX_TX4 96 PCIE_MTX_C_GRX_P4
PCIE_GTX_C_MRX_N3	97	PEX_RX3#	GND 98
PCIE_GTX_C_MRX_P3	99	PEX_RX3	PEX_TX3# 100 PCIE_MTX_C_GRX_N3
	101	GND	PEX_TX3 102 PCIE_MTX_C_GRX_P3
PCIE_GTX_C_MRX_N2	103	PEX_RX2#	GND 104
PCIE_GTX_C_MRX_P2	105	PEX_RX2	PEX_TX2# 106 PCIE_MTX_C_GRX_N2
	107	GND	PEX_TX2 108 PCIE_MTX_C_GRX_P2

ACES_88990-2D08
CONN@

JP19B

	109	PEX_RX1#	GND 110
PCIE_GTX_C_MRX_N1	111	PEX_RX1	PEX_TX1# 112 PCIE_MTX_C_GRX_N1
PCIE_GTX_C_MRX_P1	113	GND	PEX_TX1 114 PCIE_MTX_C_GRX_P1
	115	PEX_RX0#	GND 116
PCIE_GTX_C_MRX_N0	117	PEX_RX0	PEX_TX0# 118 PCIE_MTX_C_GRX_N0
PCIE_GTX_C_MRX_P0	119	GND	PEX_TX0 120 PCIE_MTX_C_GRX_P0
16 CLK_PCIE_VGA# CLK_PCIE_VGA#	121	PEX_REFCLK#	PRSNT1# 122
16 CLK_PCIE_VGA CLK_PCIE_VGA	123	PEX_REFCLK	TV_C/HDTV_Pr 124 VGA_TV_CRMA → VGA_TV_CRMA 19
	125	CLK_REQ#	GND 126
20 PLTRST_VGA#	127	PEX_RST#	TV_Y/HDTV_Y 128 VGA_TV_LUMA → VGA_TV_LUMA 19
	129	RSVD	GND 130
	131	RSVD	TV_CVBS/HDTV_Pb 132 VGA_TV_COMPS → VGA_TV_COMPS 19
D_EC_SMB_DA1	133	SMB_DAT	GND 134
D_EC_SMB_CK1	135	SMB_CLK	VGA_RED 136 VGA_CRT_R → VGA_CRT_R 19
	137	THERM#	GND 138
19 VGA_CRT_HSYNC VGA_CRT_HSYNC	139	VGA_HSYNC	VGA_GRN 140 VGA_CRT_G → VGA_CRT_G 19
19 VGA_CRT_VSYNC VGA_CRT_VSYNC	141	VGA_VSYNC	GND 142
19 VGA_DDC_CLK VGA_DDC_CLK	143	DDCA_CLK	VGA_BLU 144 VGA_CRT_B → VGA_CRT_B 19
19 VGA_DDC_DATA VGA_DDC_DATA	145	DDCA_DAT	GND 146
	147	IGP_UCLK#	LVDS_UCLK# 148 VGA_TZCLK- → VGA_TZCLK- 18
	149	IGP_UCLK	LVDS_UCLK 150 VGA_TZCLK+ → VGA_TZCLK+ 18
	151	GND	GND 152
	153	RSVD	LVDS_UTX3# 154
	155	RSVD	LVDS_UTX3 156
	157	RSVD	GND 158
	159	IGP_UTX2#	LVDS_UTX2# 160 VGA_TZOUT2- → VGA_TZOUT2- 18
	161	IGP_UTX2	LVDS_UTX2 162 VGA_TZOUT2+ → VGA_TZOUT2+ 18
	163	GND	GND 164
	165	IGP_UTX1#	LVDS_UTX1# 166 VGA_TZOUT1- → VGA_TZOUT1- 18
	167	IGP_UTX1	LVDS_UTX1 168 VGA_TZOUT1+ → VGA_TZOUT1+ 18
	169	GND	GND 170
	171	IGP_UTX0#	LVDS_UTX0# 172 VGA_TZOUT0- → VGA_TZOUT0- 18
	173	IGP_UTX0	LVDS_UTX0 174 VGA_TZOUT0+ → VGA_TZOUT0+ 18
	175	GND	GND 176
	177	IGP_LCLK#/DVI_B_CLK#	LVDS_LCLK# 178 VGA_TXCLK- → VGA_TXCLK- 18
	179	IGP_LCLK/DVI_B_CLK	LVDS_LCLK 180 VGA_TXCLK+ → VGA_TXCLK+ 18
	181	DVI_B_HPD/GND	GND 182
	183	RSVD	LVDS_LTX3# 184
	185	RSVD	LVDS_LTX3 186
	187	GND	GND 188
	189	IGP_LTX2#/DVI_B_TX2#	LVDS_LTX2# 190 VGA_TXOUT2- → VGA_TXOUT2- 18
	191	IGP_LTX2/DVI_B_TX2	LVDS_LTX2 192 VGA_TXOUT2+ → VGA_TXOUT2+ 18
	193	GND	GND 194
	195	IGP_LTX1#/DVI_B_TX1#	LVDS_LTX1# 196 VGA_TXOUT1- → VGA_TXOUT1- 18
	197	IGP_LTX1/DVI_B_TX1	LVDS_LTX1 198 VGA_TXOUT1+ → VGA_TXOUT1+ 18
	199	GND	GND 200
	201	IGP_LTX0#/DVI_B_TX0#	LVDS_LTX0# 202 VGA_TXOUT0- → VGA_TXOUT0- 18
	203	IGP_LTX0/DVI_B_TX0	LVDS_LTX0 204 VGA_TXOUT0+ → VGA_TXOUT0+ 18
	205	DVI_A_HPD	GND 206
18 DVI_DET DVI_DET	207	DVI_A_CLK#	DDCC_DAT 208 I2CC_SDA → I2CC_SDA 18
18 VGA_DVI_TXC- VGA_DVI_TXC-	209	DVI_A_CLK	DDCC_CLK 210 I2CC_SCL → I2CC_SCL 18
18 VGA_DVI_TXC+ VGA_DVI_TXC+	211	GND	LVDS_PPEN 212 ENVDD → ENVDD 18
	213	DVI_A_TX2#	LVDS_BL_BRGHT 214
18 VGA_DVI_TXD2- VGA_DVI_TXD2-	215	DVI_A_TX2	LVDS_BLEN 216 ENBKL → ENBKL 10,30
18 VGA_DVI_TXD2+ VGA_DVI_TXD2+	217	GND	DDCB_DAT 218 VGA_DVI_SDATA → VGA_DVI_SDATA 18
	219	DVI_A_TX1#	DDCB_CLK 220 VGA_DVI_SCLK → VGA_DVI_SCLK 18
18 VGA_DVI_TXD1- VGA_DVI_TXD1-	221	DVI_A_TX1	2V5RUN 222 +2.5VS
18 VGA_DVI_TXD1+ VGA_DVI_TXD1+	223	GND	GND 224
	225	DVI_A_TX0#	3V3RUN 226 +3VS
18 VGA_DVI_TXD0- VGA_DVI_TXD0-	227	DVI_A_TX0	3V3RUN 228
18 VGA_DVI_TXD0+ VGA_DVI_TXD0+	229	GND	3V3RUN 230
	231	GND	GND 232

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+MXM_B+
160mil(4A)
L44 2 1 KC FBM-L11-201209-221LMAT_0805 PM@
L43 2 1 KC FBM-L11-201209-221LMAT_0805 PM@
C526 PM@ 680P_0603_50V7K
C527 68P_0402_50V8J
C525 0.1U_0603_25V7K
B+ 160mil(4A)

+2.5VS
C471 0.1U_0402_16V4Z PM@

+5VS
C520 0.1U_0402_16V4Z PM@

+3VS
30,32,41 EC_SMB_DA1 → D_EC_SMB_DA1
Q46 PM@ 2N7002_SOT23
30,32,41 EC_SMB_CK1 → D_EC_SMB_CK1
Q47 PM@ 2N7002_SOT23

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: MXM Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 0.6

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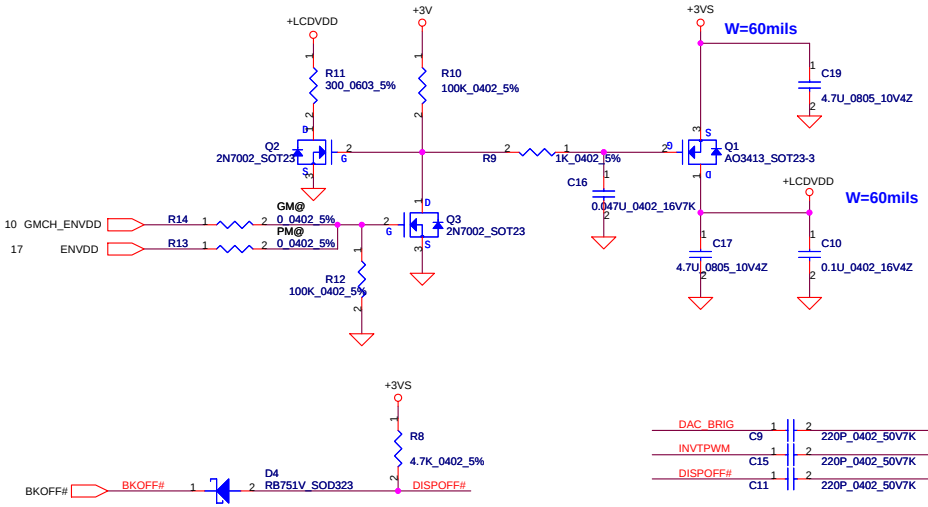
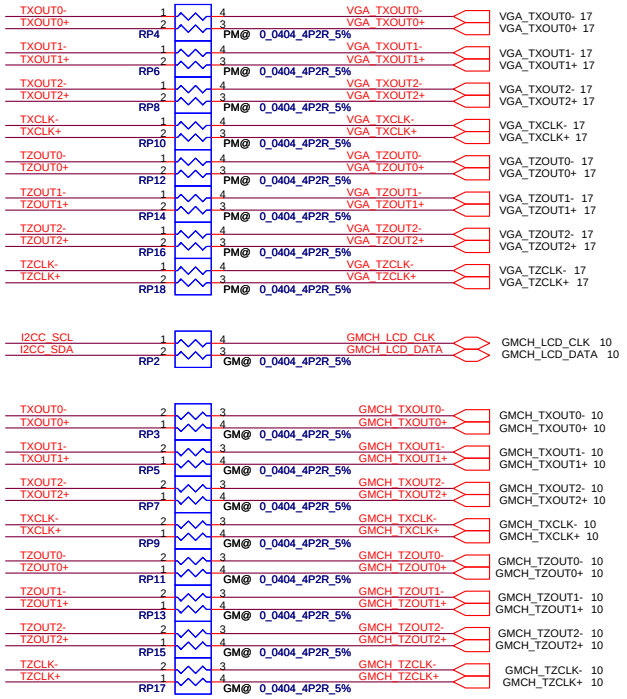
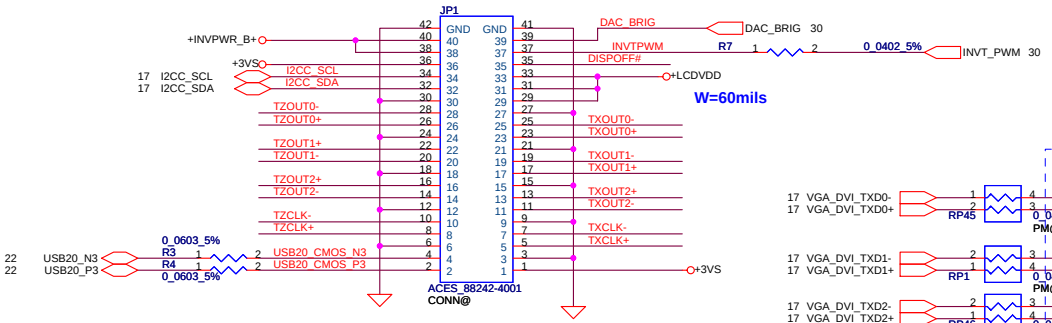
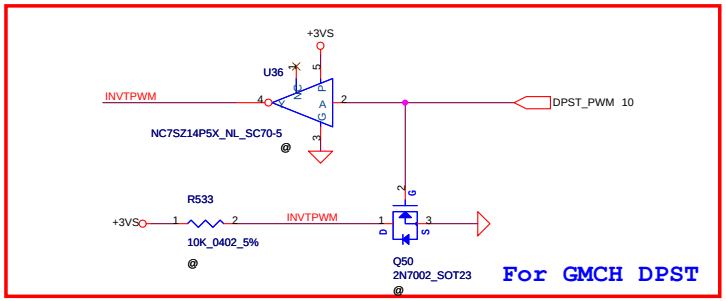
LCD POWER CIRCUIT

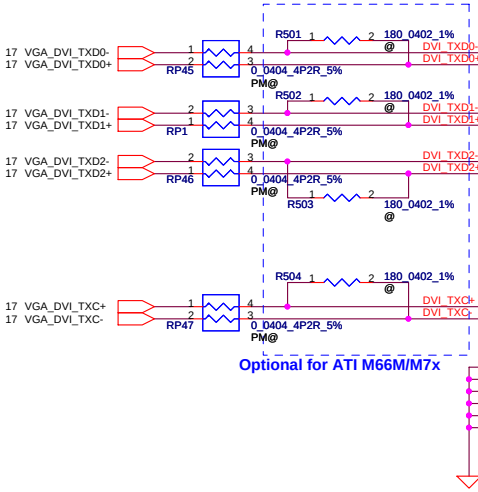




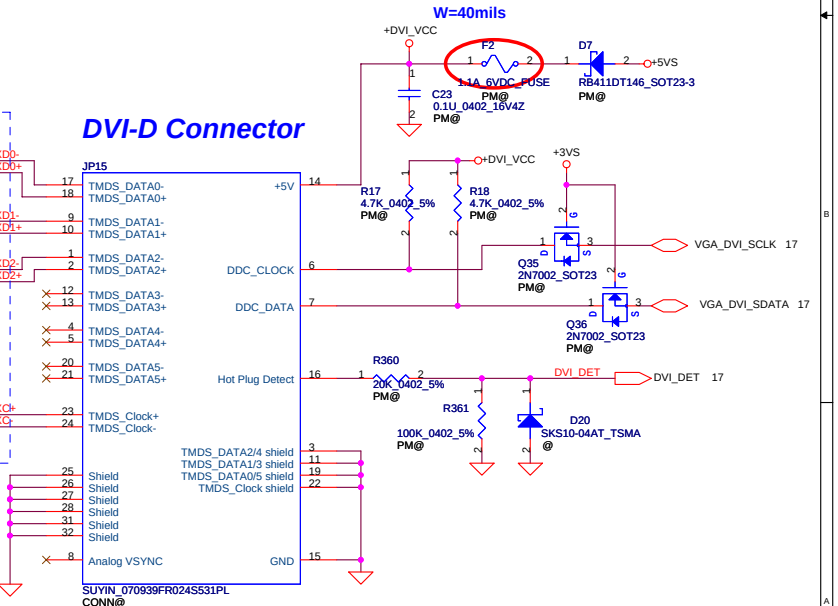
LCD/PANEL BD. Conn.

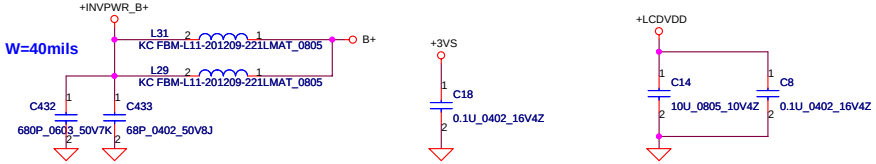






DVI-D Connector





Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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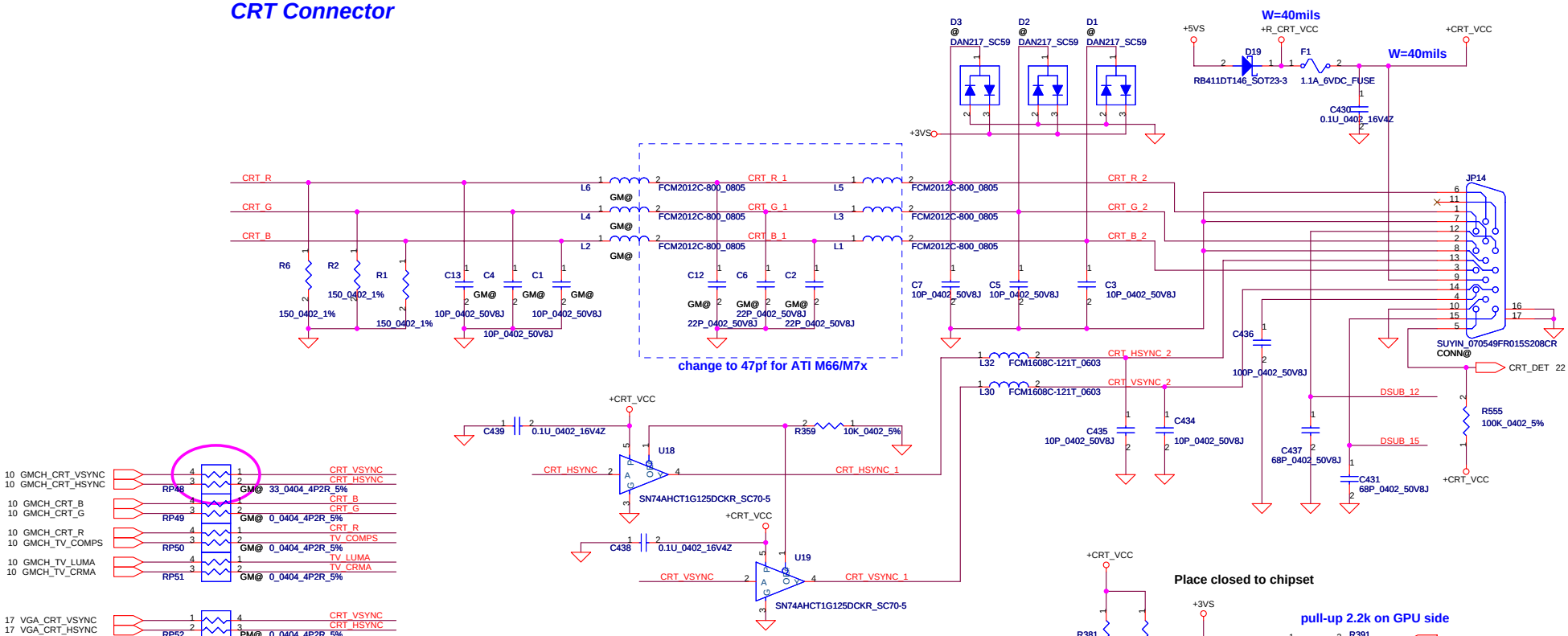
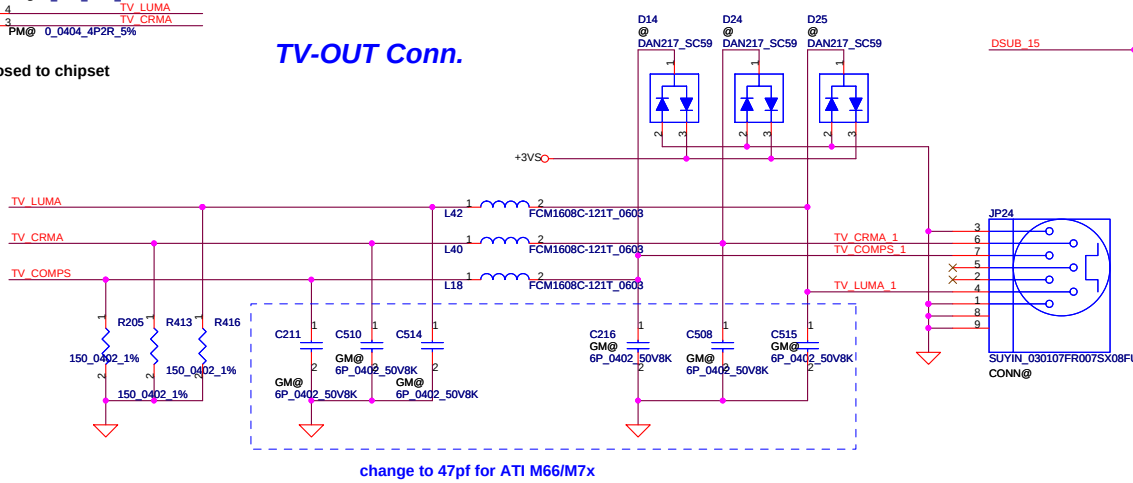
CRT Connector



TV-OUT Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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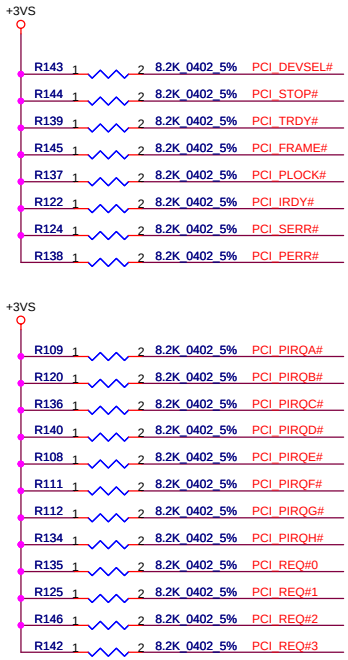
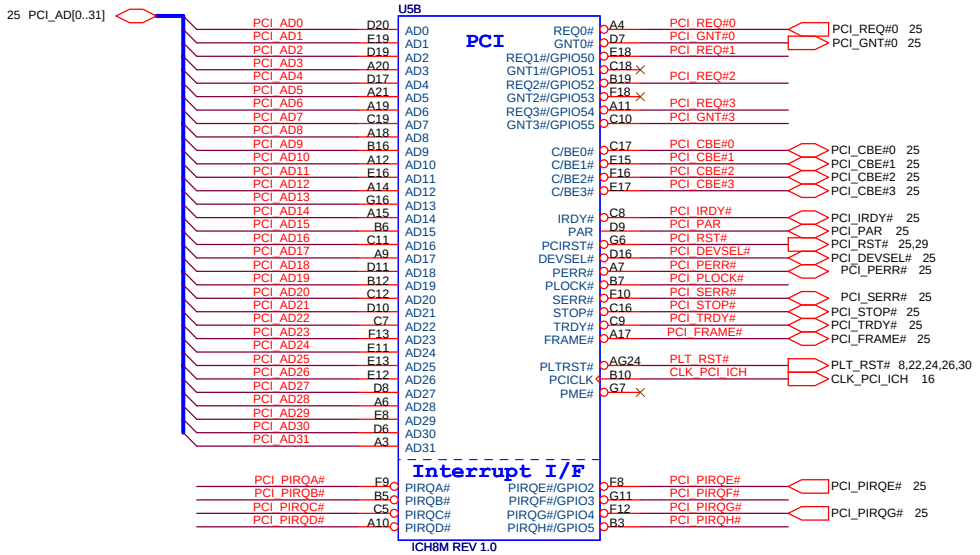
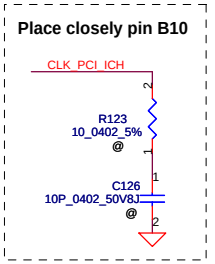
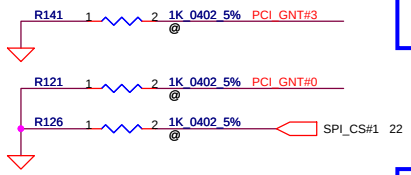


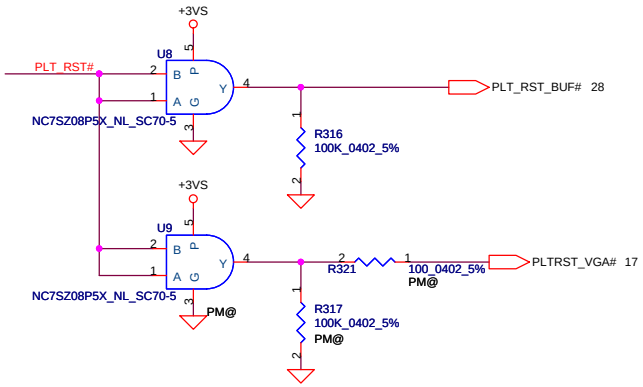






A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



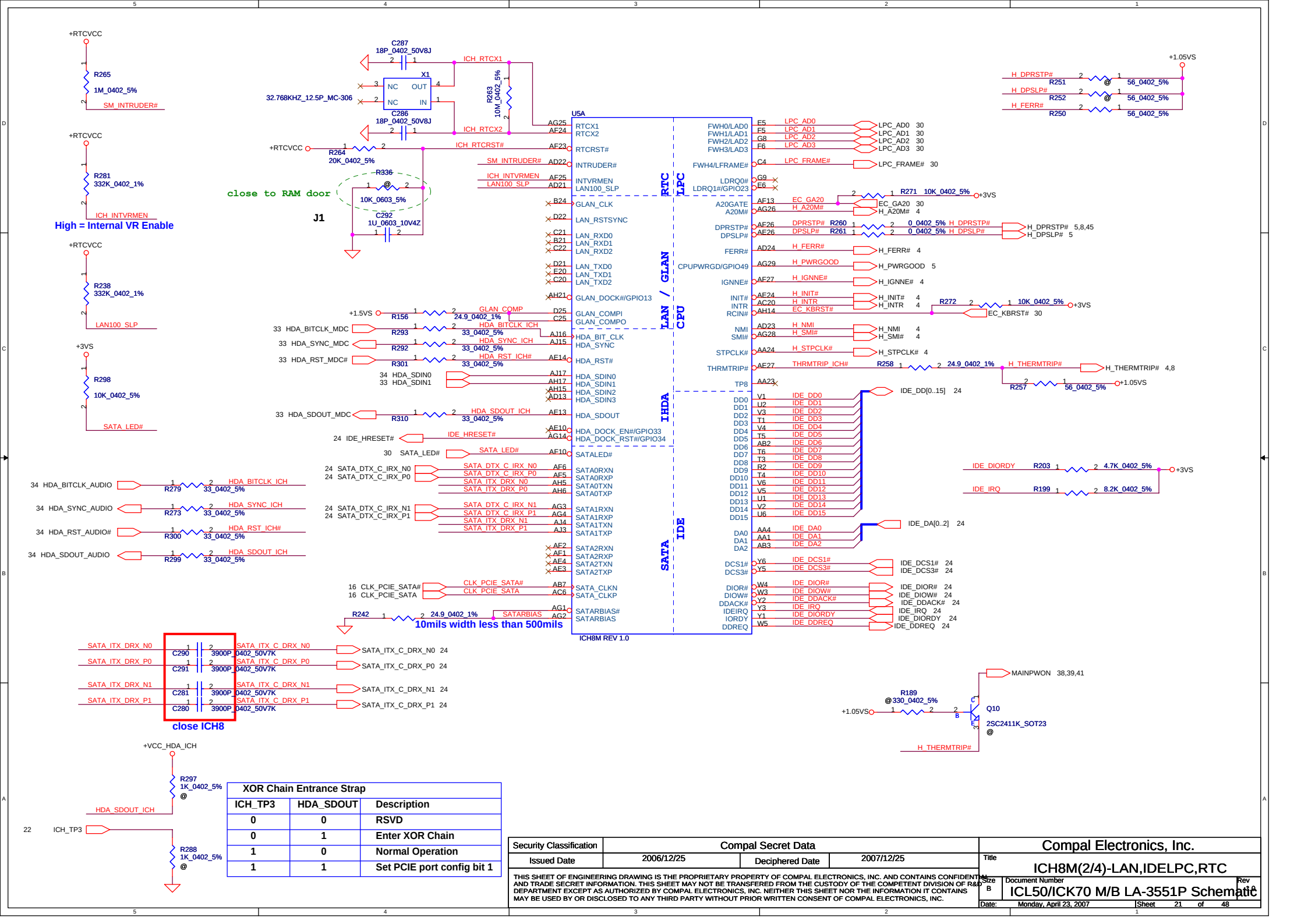
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH8M(1/4)-PCI

Size | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Monday, April 23, 2007 | Sheet 20 of 48



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH8M(2/4)-LAN,IDELPC,RTC

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

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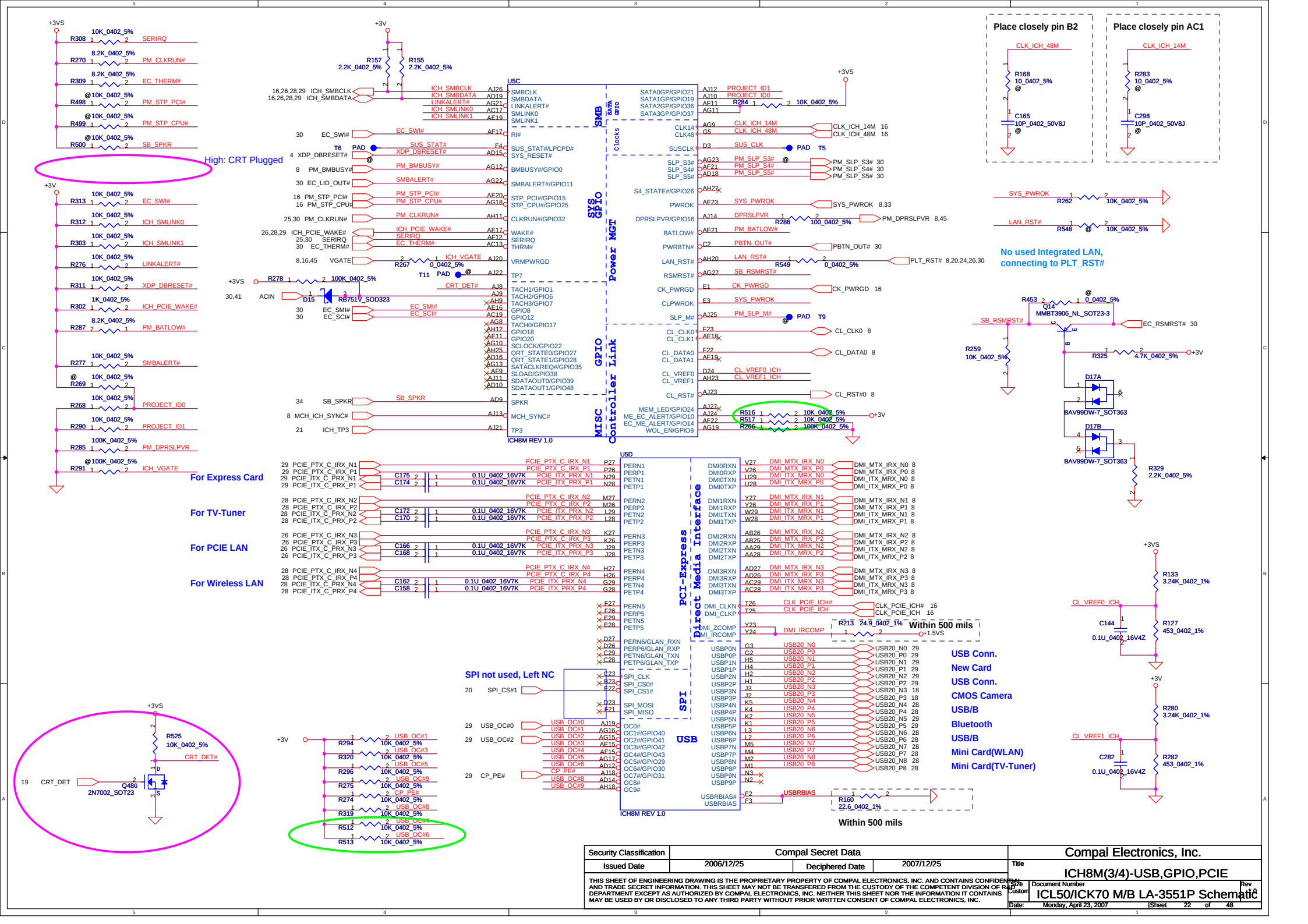


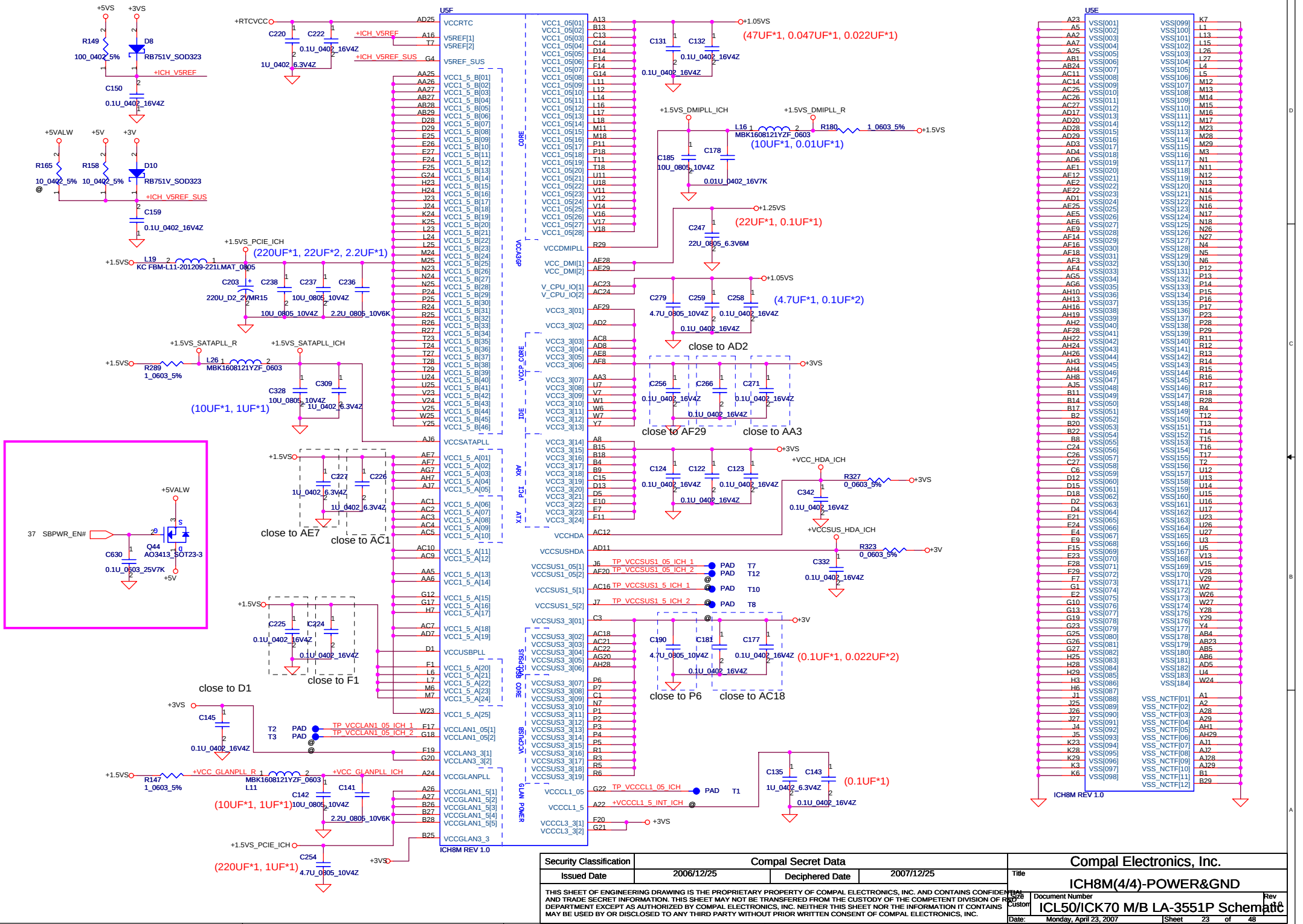
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH8M(3/4)-USB,GPIO,PCIE

Size: Custom | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Monday, April 23, 2007 | Sheet 22 of 48



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH8M(4/4)-POWER&GND

Size: Custom | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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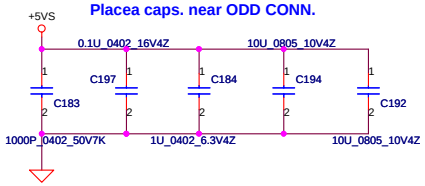
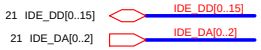
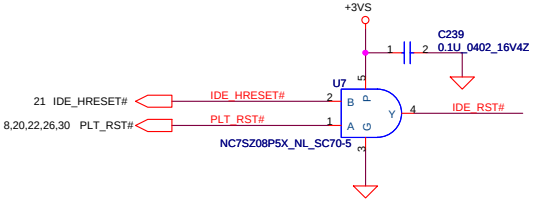
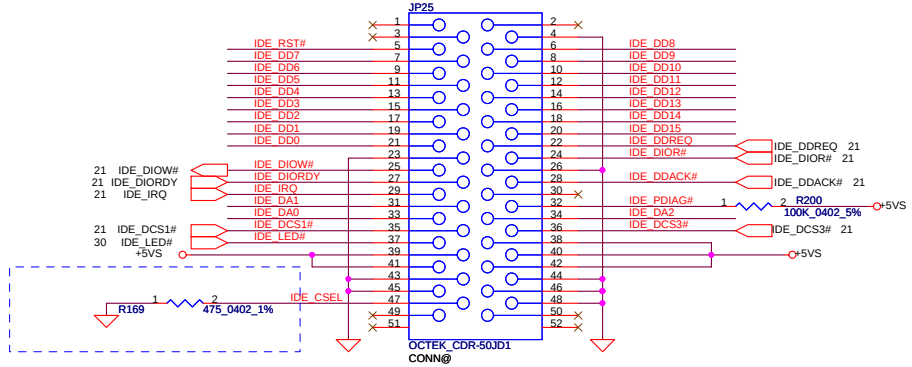
Placea caps. near ODD CONN.

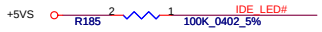


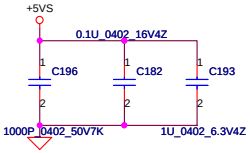


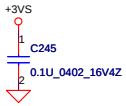




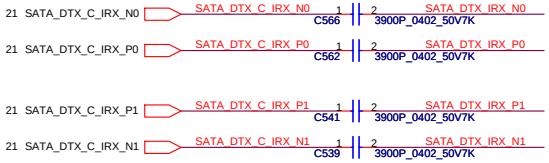
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

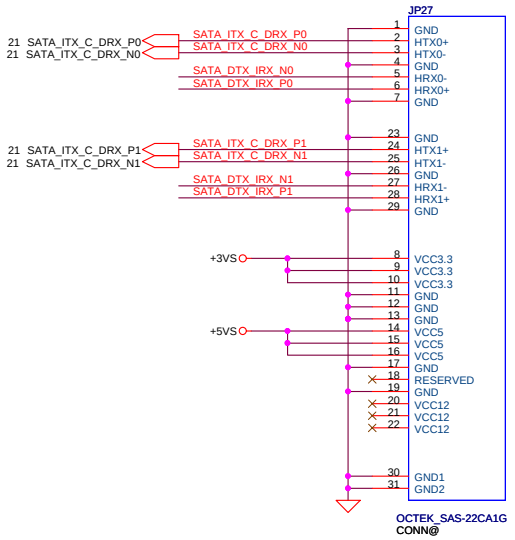






SATA HDD Conn.(SAS Connector)





First HDD for 15.4"

2nd HDD for 17"

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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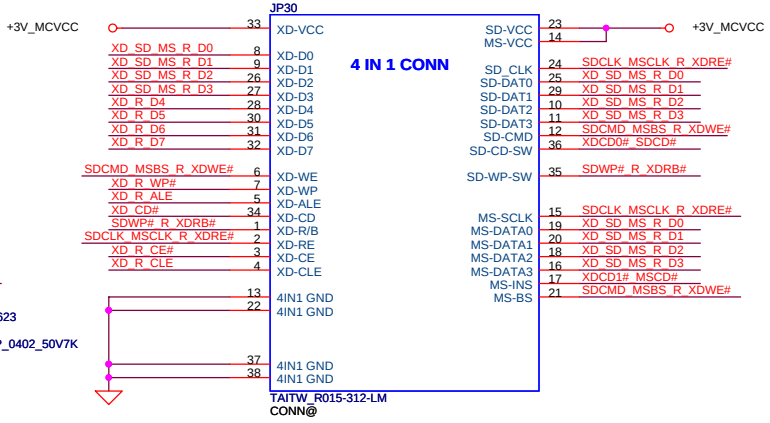
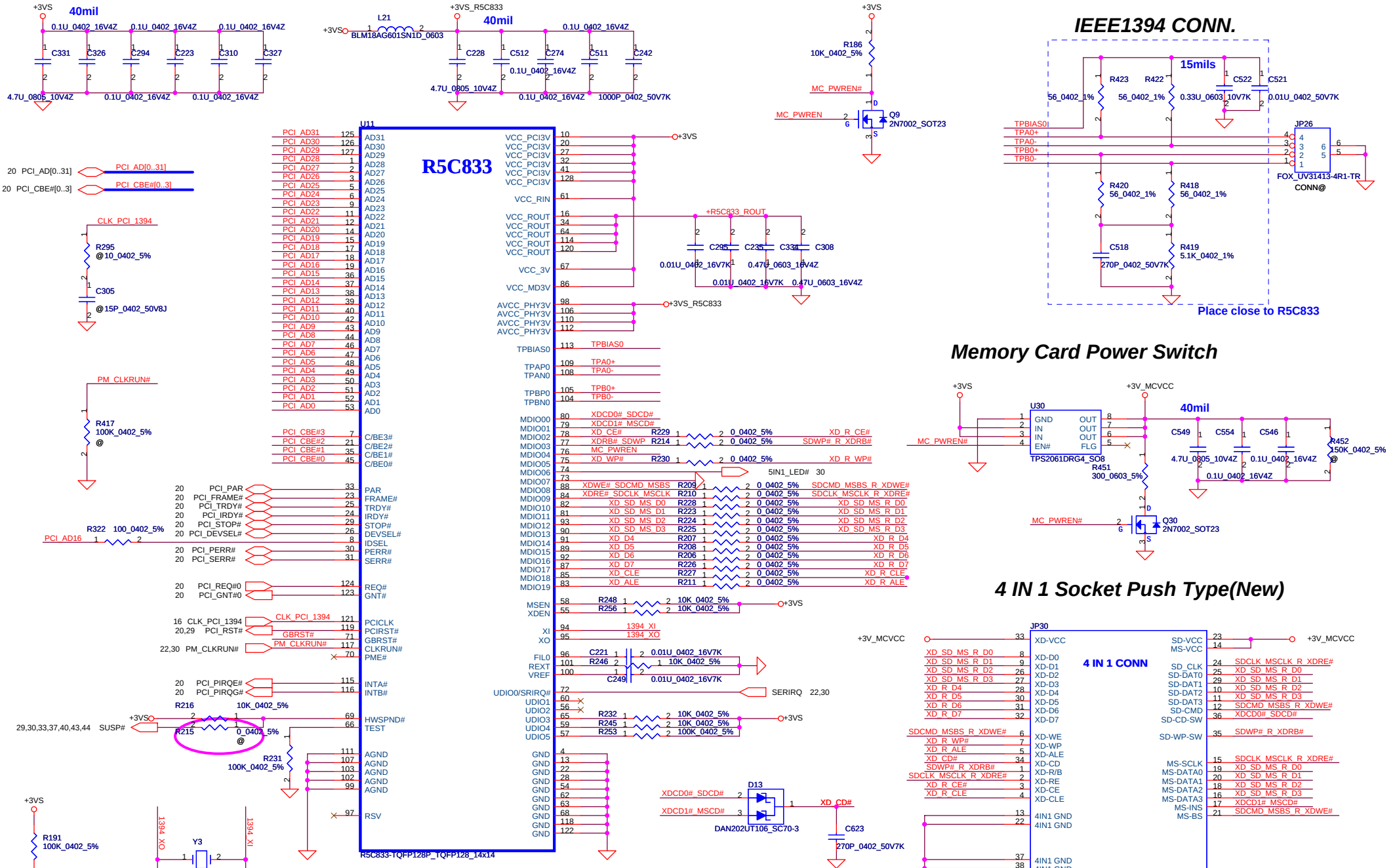
IEEE1394 CONN.

Memory Card Power Switch

4 IN 1 Socket Push Type(New)





Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

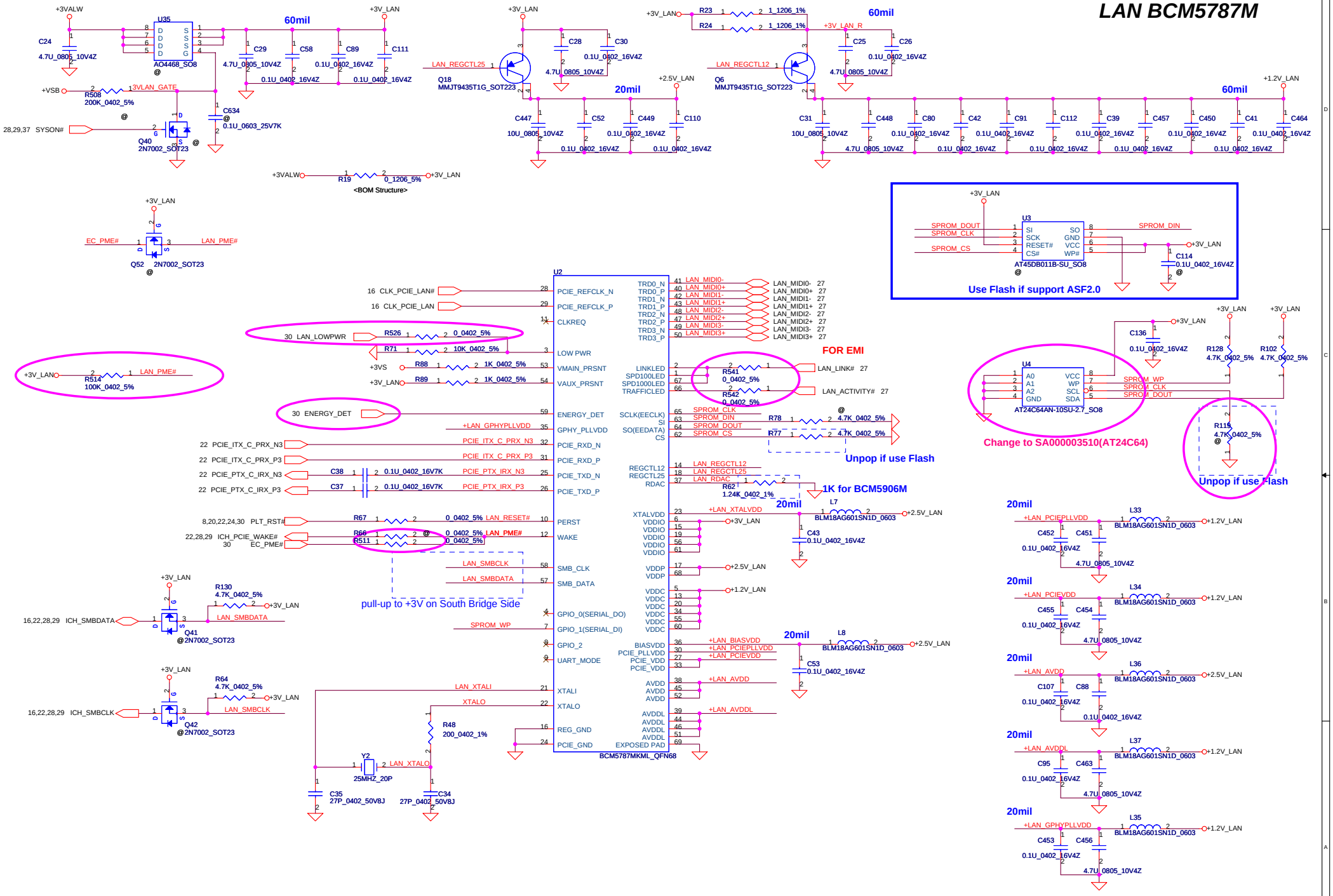
Compal Electronics, Inc.

Title: R5C833 5IN1 & IEEE1394

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 0.6

Date: Monday, April 23, 2007 | Sheet 25 of 48

LAN BCM5787M



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

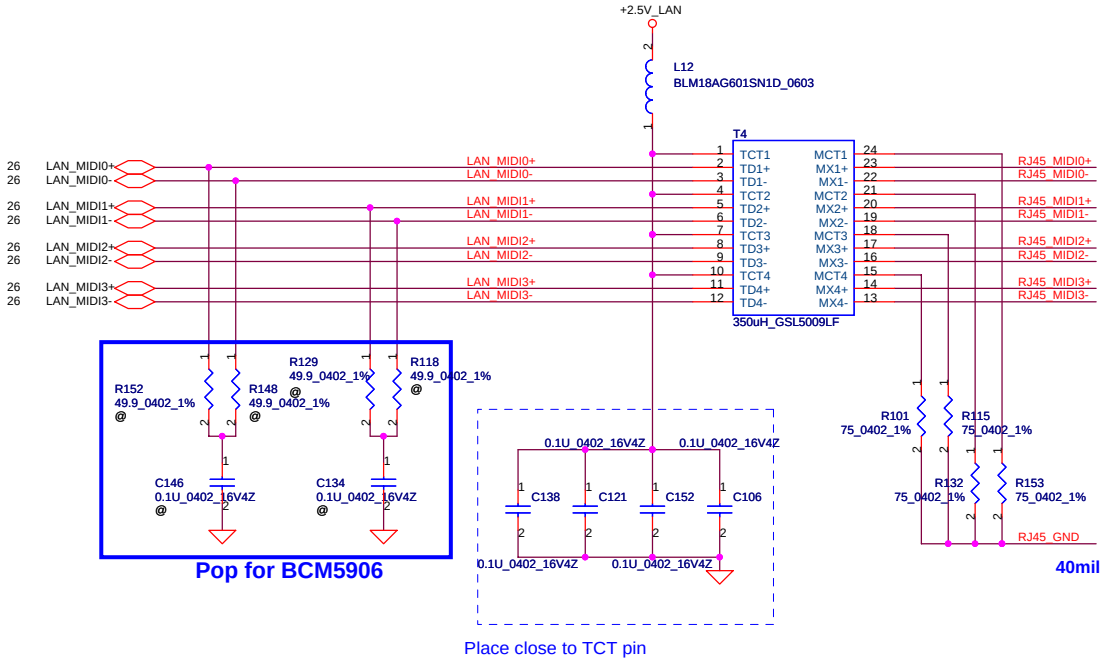
Compal Electronics, Inc.

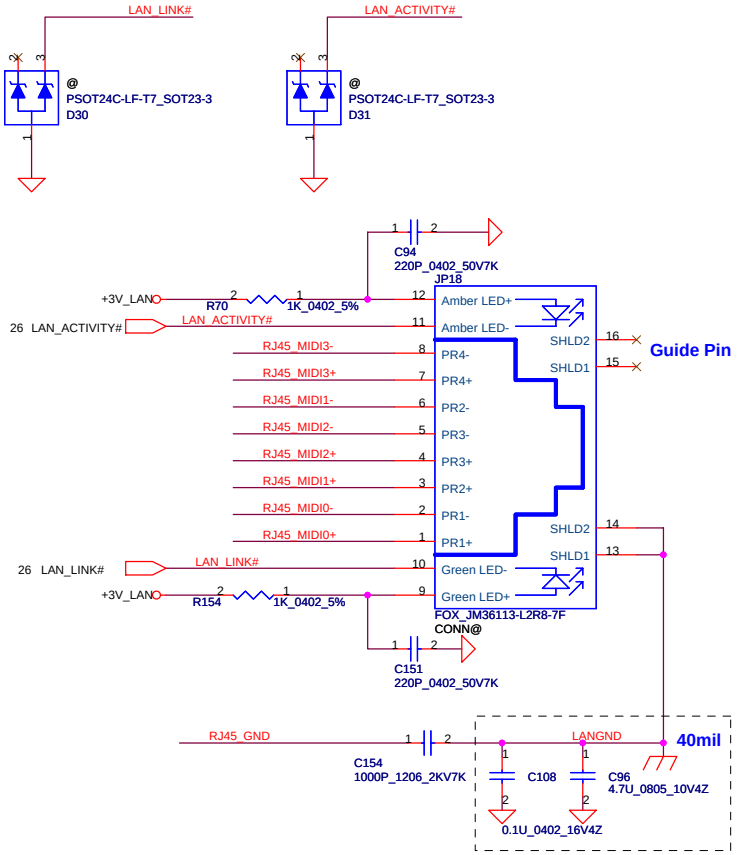
Title: LAN BCM5787M

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Monday, April 23, 2007 | Sheet 26 of 48

LAN BCM5787M





Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45/RJ11

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	0.6

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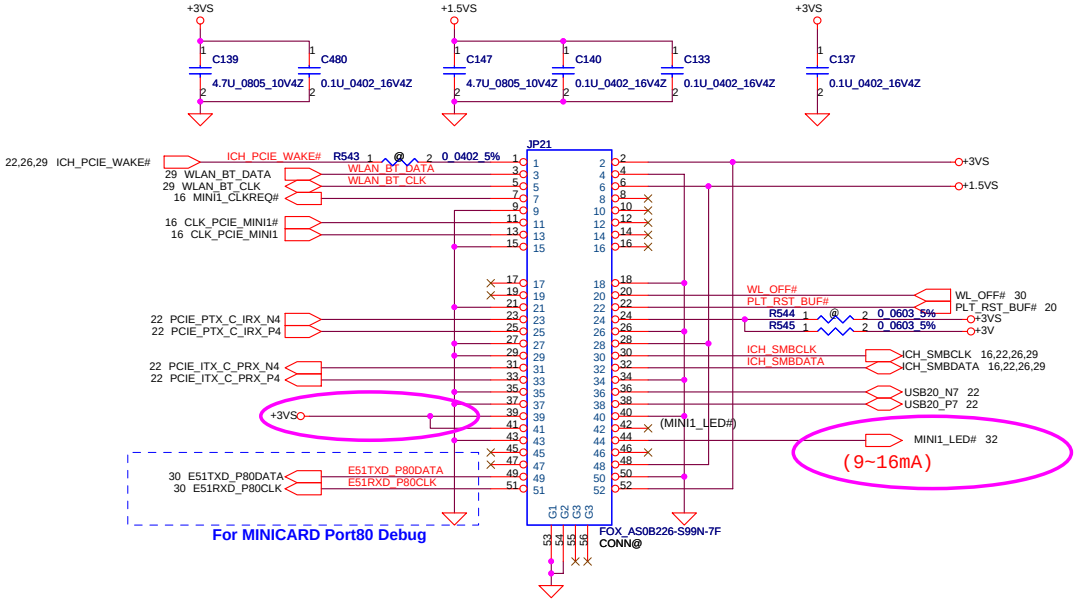
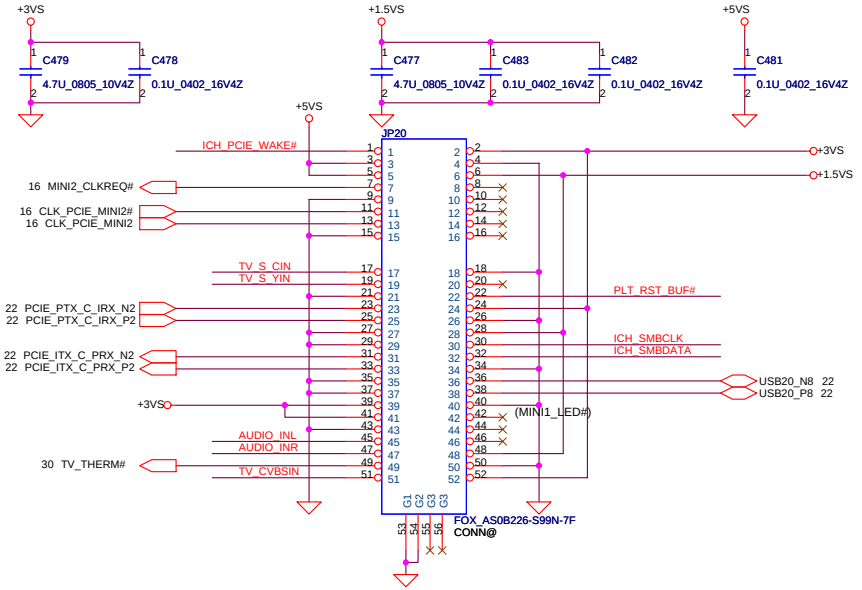
For Wireless LAN

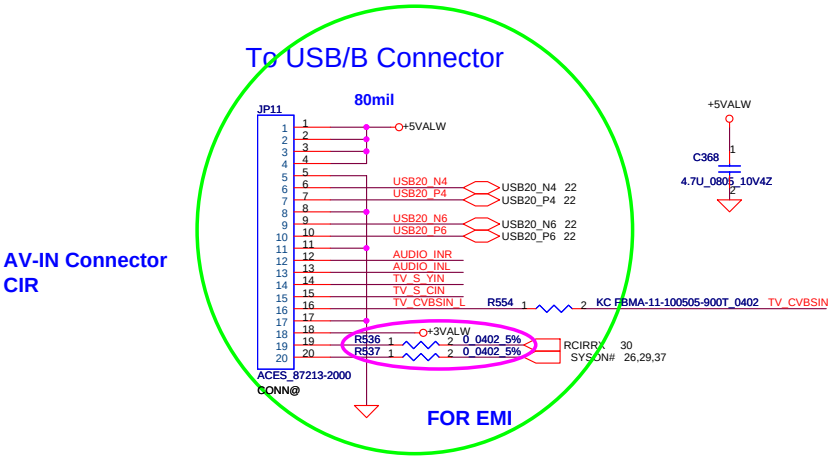


For TV-Tuner/HW MPEG



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

To USB/B Connector



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/12/25	Deciphered Date 2007/12/25	Title: MINI CARD (WLAN & TV-Tuner)
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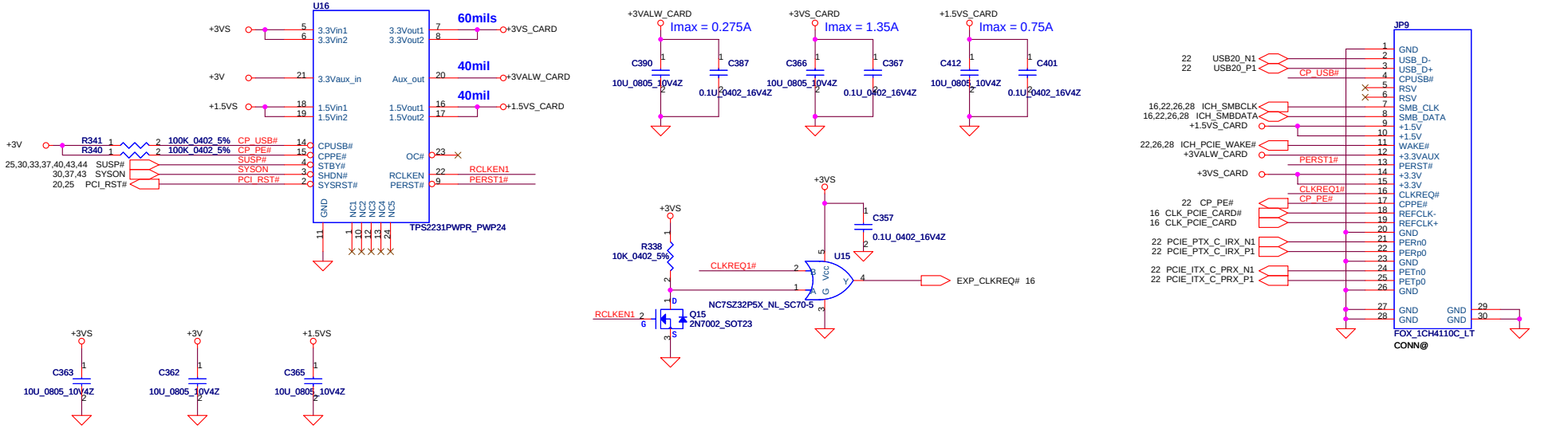
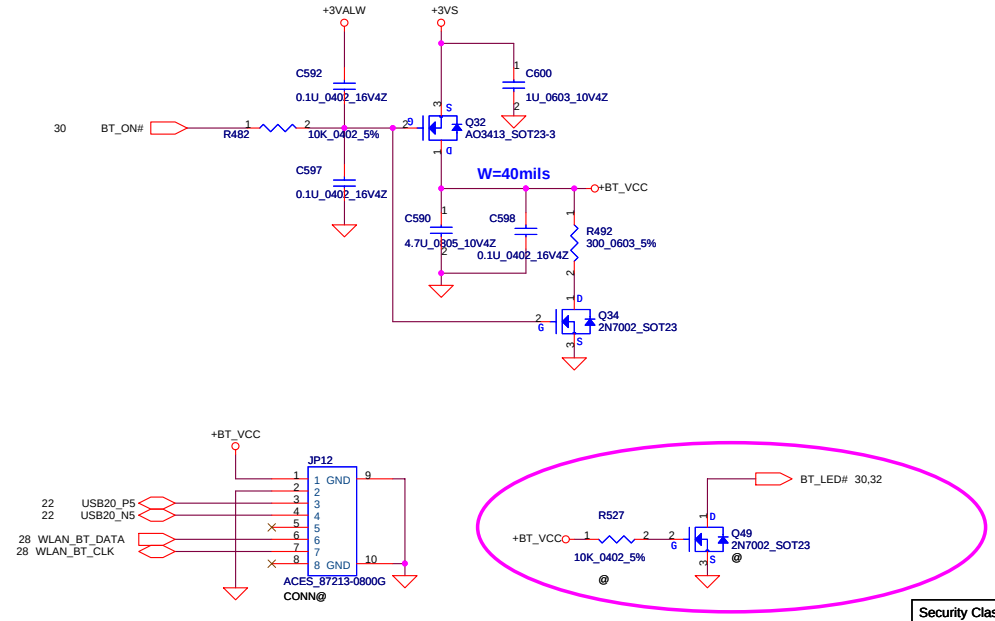
			Date: Monday, April 23, 2007; Sheet 28 of 48

New Card Power Switch

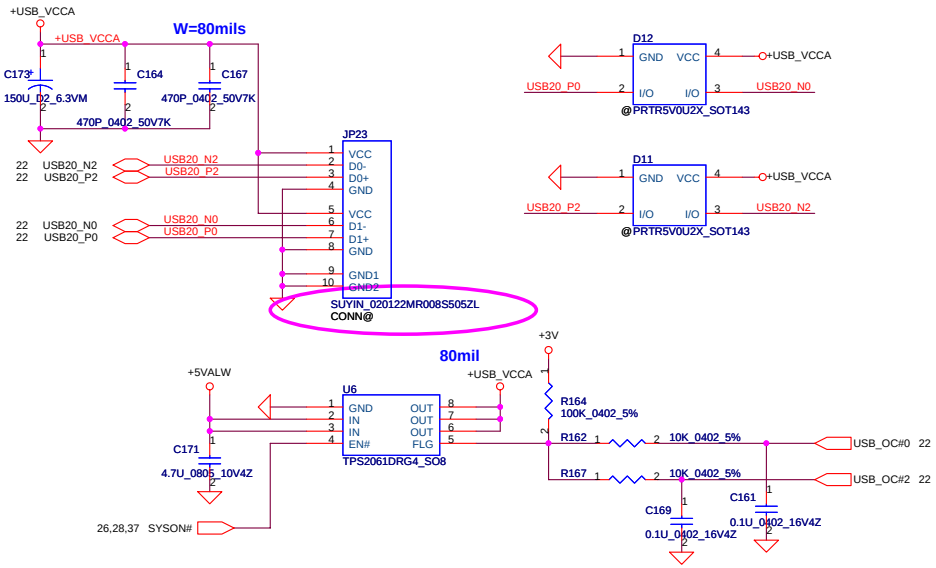


New Card Socket (Left/TOP)

Bluetooth Conn.



USB CONN. (Stack-up Type)



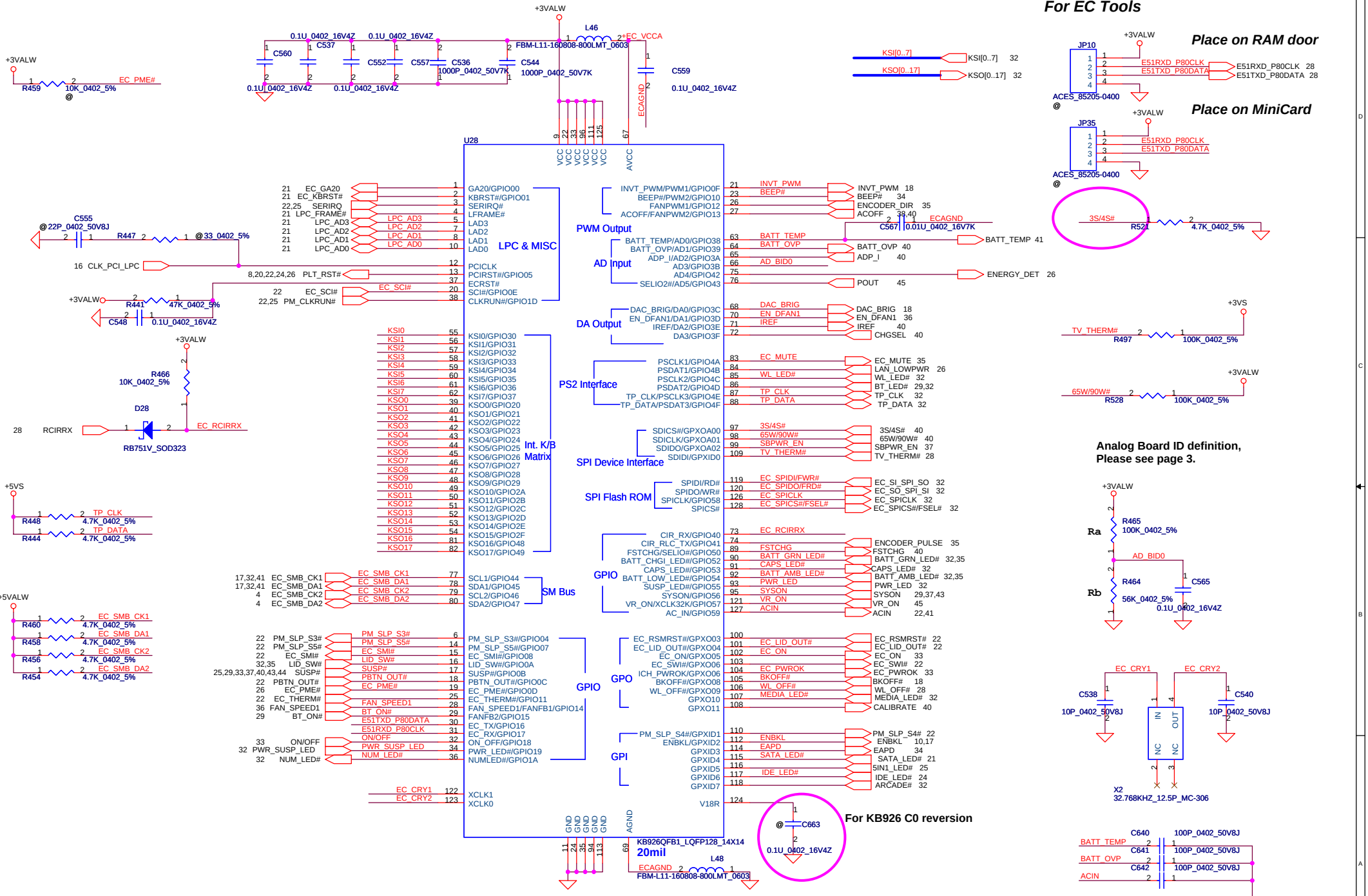
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: NEW CARD & USB Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Monday, April 23, 2007 | Sheet 29 of 48



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Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: EC ENE KB925(Reserved)

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

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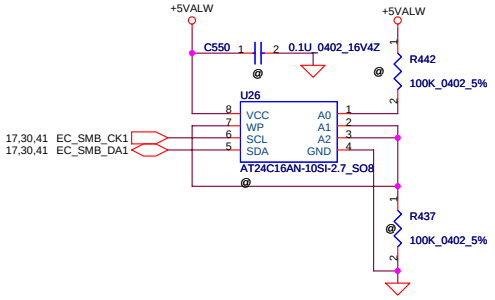
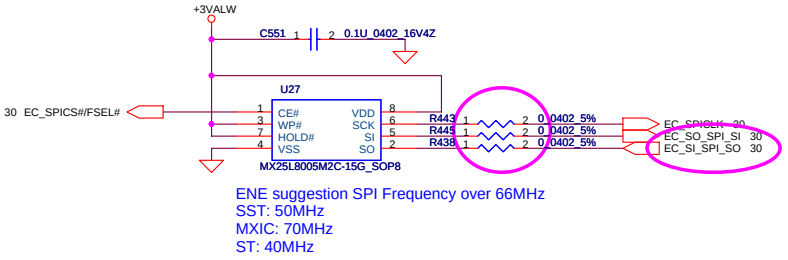
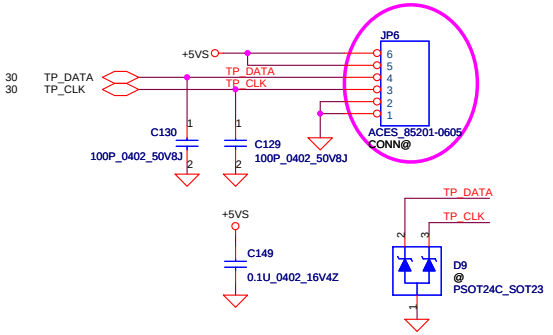


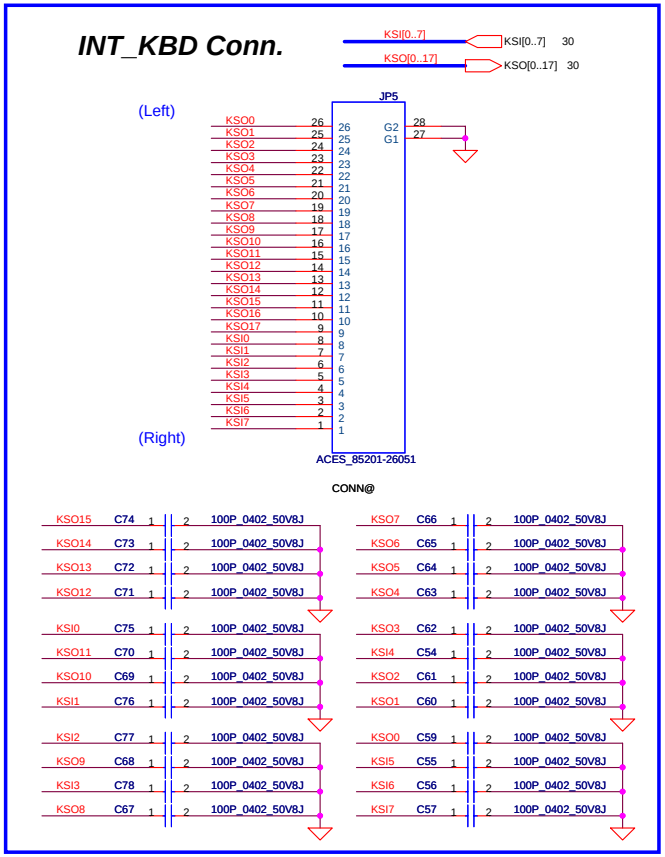


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

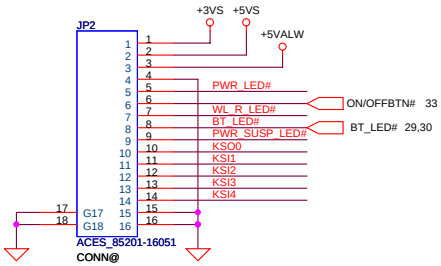
To TP/B Conn.

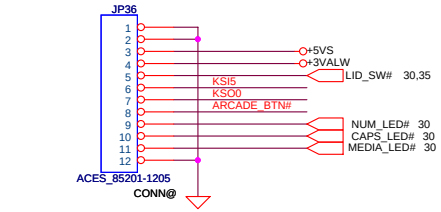


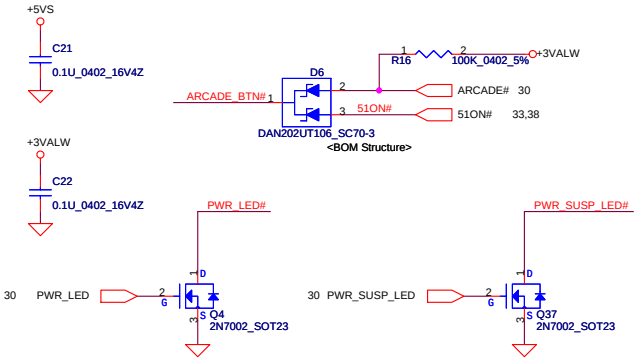
INT_KBD Conn.

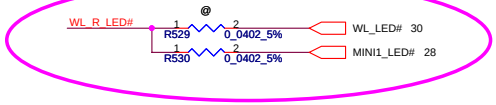


To BTN/B Conn.

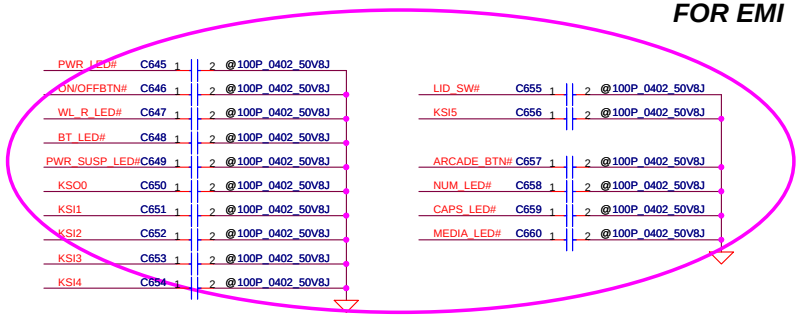








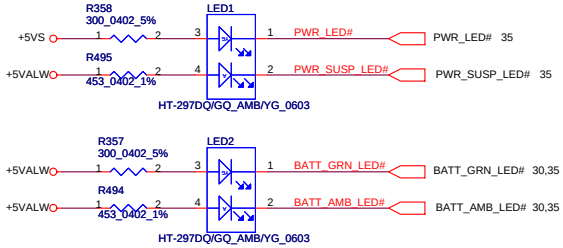
FOR EMI



	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

Compal Footprint

4 2
3 1



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

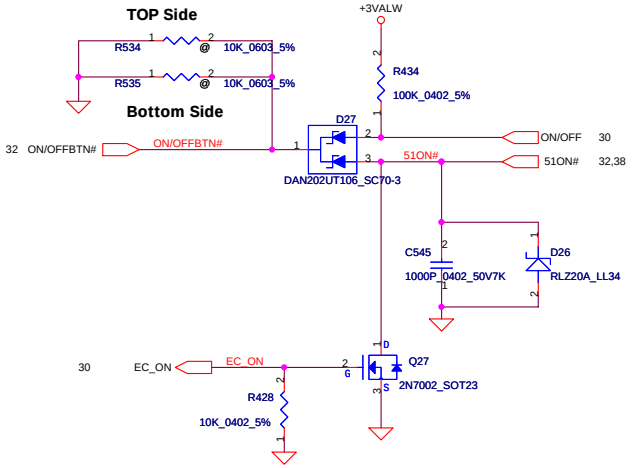
Title: BIOS, I/O Port & K/B Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

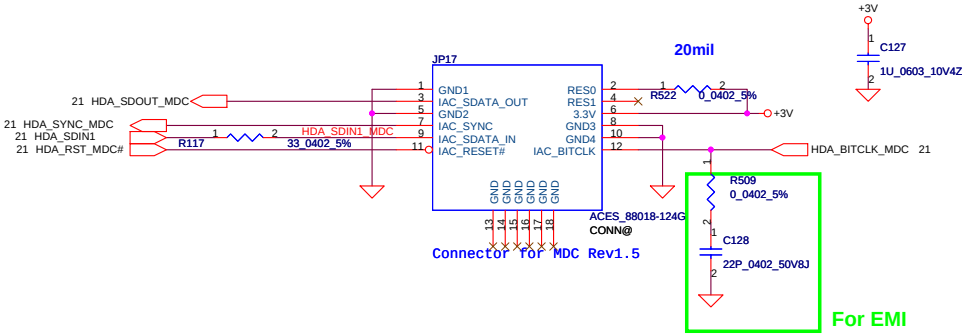
Date: Monday, April 23, 2007 | Sheet 32 of 48

Power Button

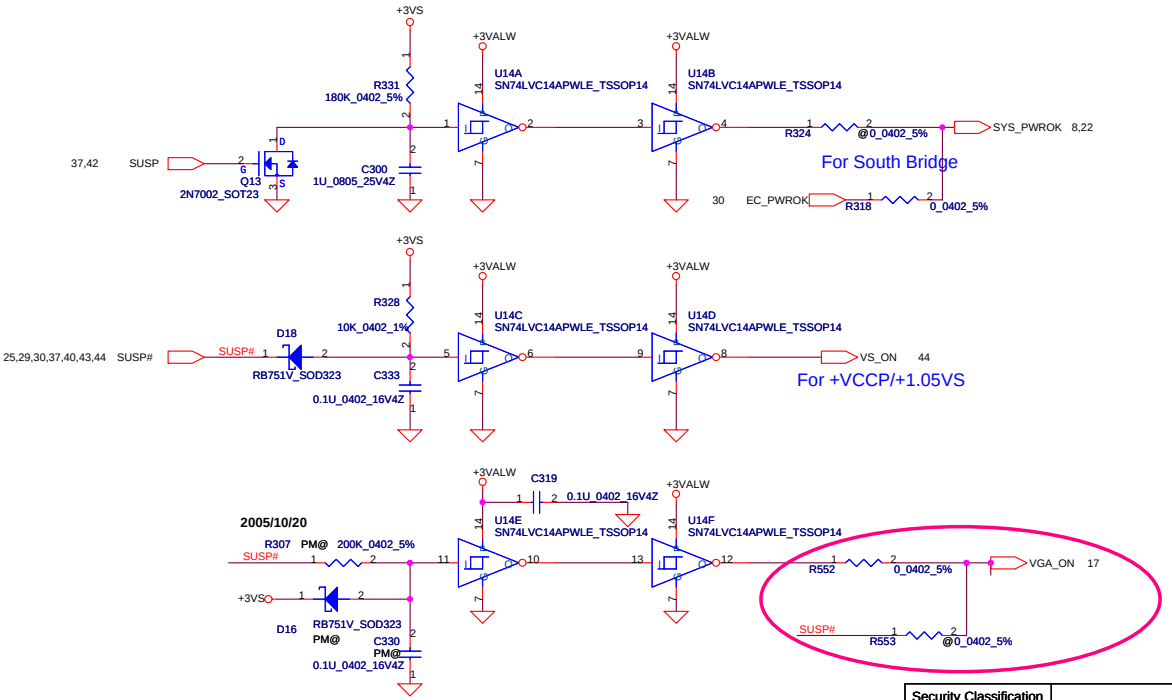
ON/OFF switch



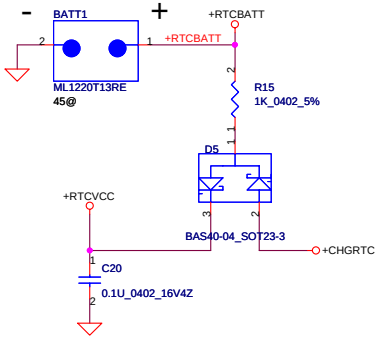
HDA MDC Conn.



Power ON Circuit



RTC Battery



Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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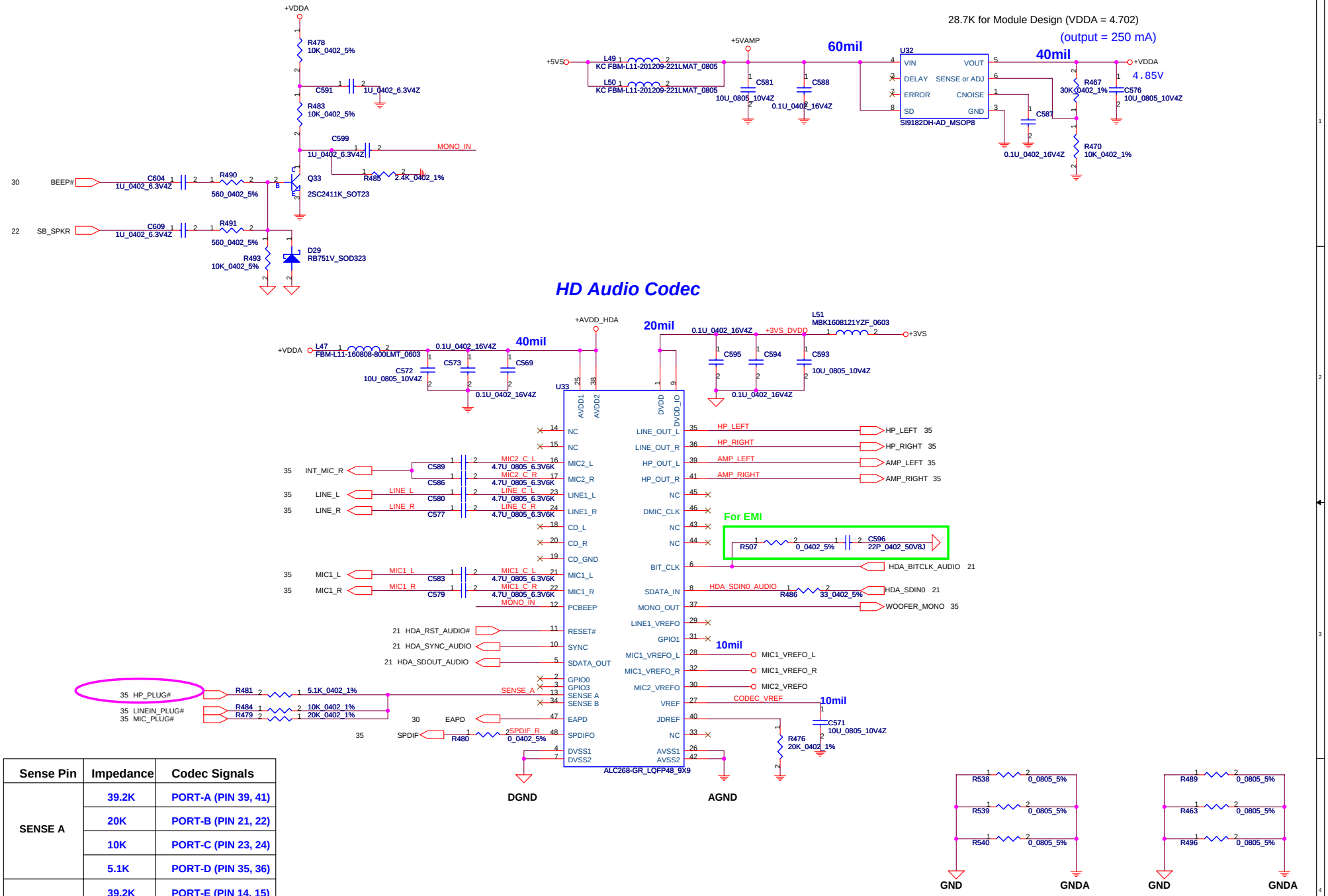
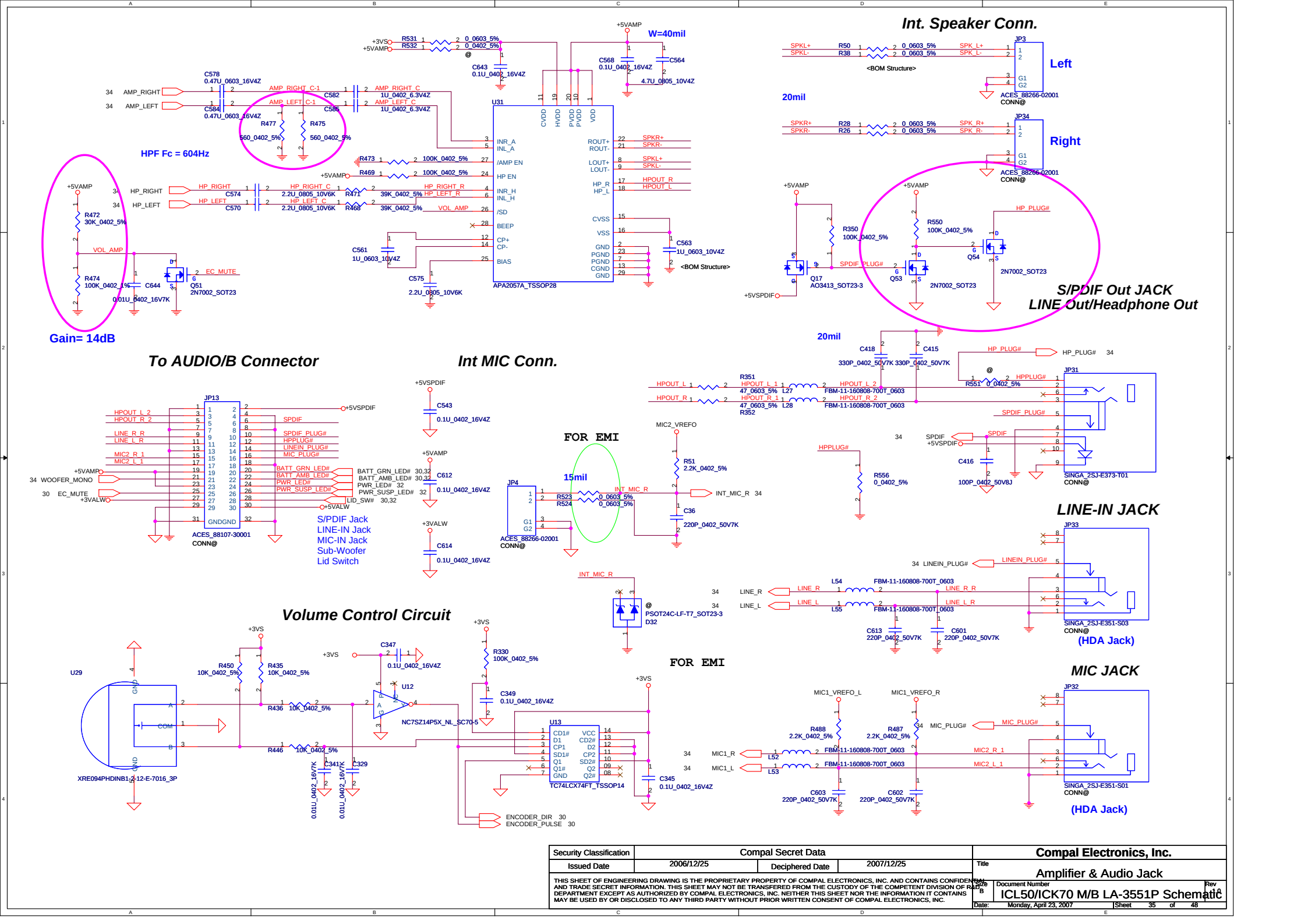


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/12/25	Deciphered Date 2007/12/25	Title: HD Audio Codec ALC268

Size B	Document Number ICL50/ICK70 M/B LA-3551P Schematic		Rev 1.0
Date: Monday, April 23, 2007	Sheet 34 of 48		



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

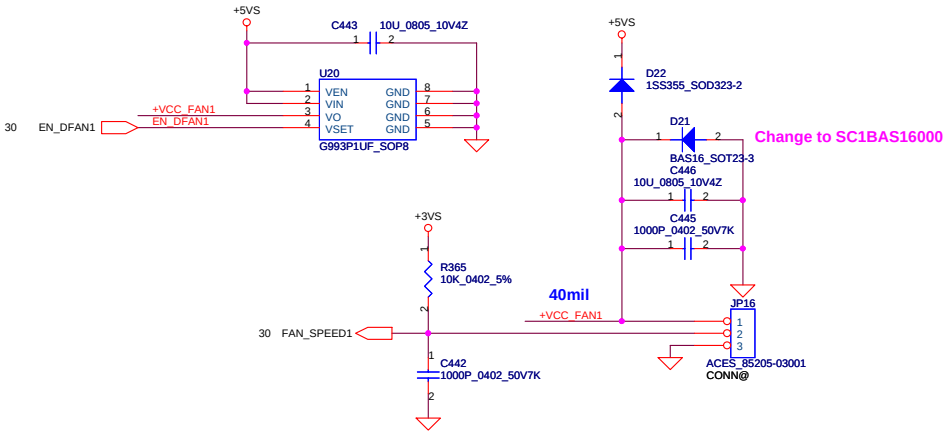
Compal Electronics, Inc.

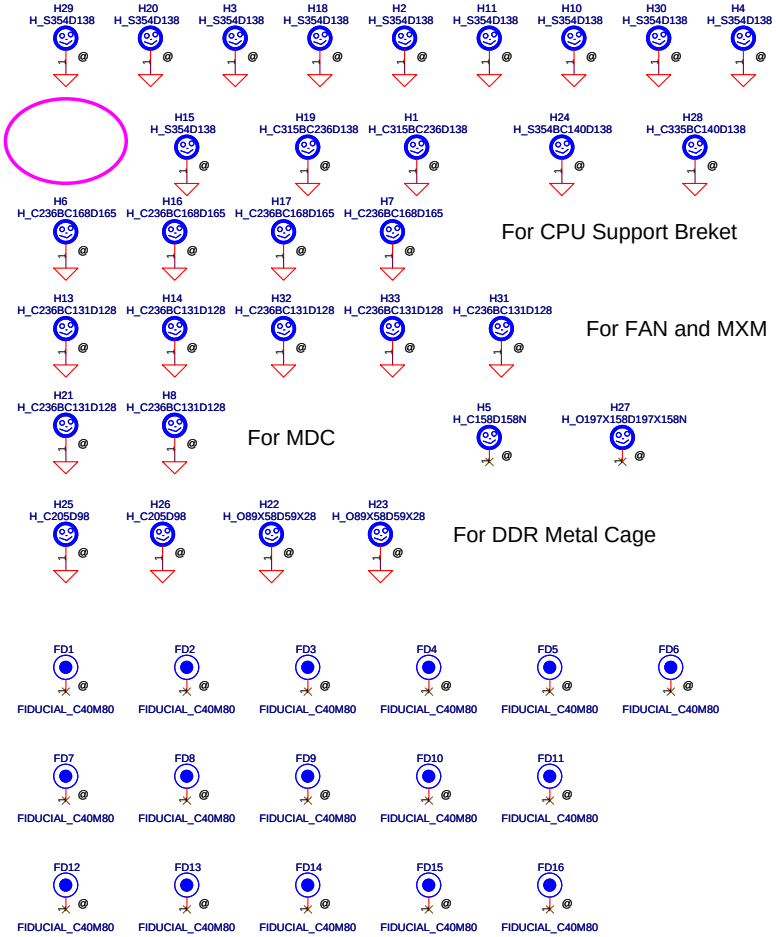
Title: Amplifier & Audio Jack

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Monday, April 23, 2007 | Sheet 35 of 48

FAN1 Conn

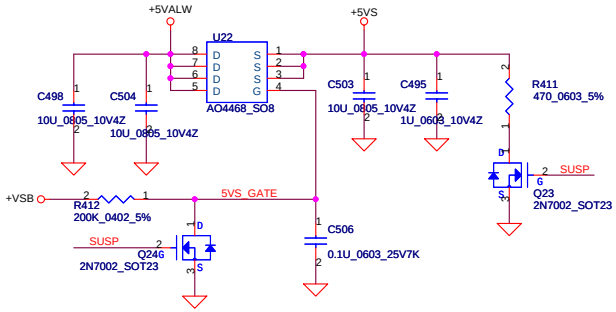




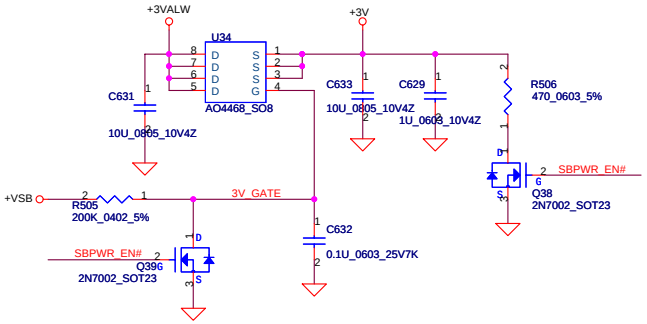
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/12/25	Deciphered Date	2007/12/25

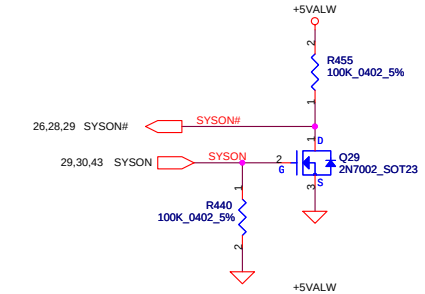
Title	FAN & Screw Hole		
Size B	Document Number ICL50/ICK70 M/B LA-3551P Schematic		Rev 1.0
Date: Monday, April 23, 2007	Sheet 36 of 48		

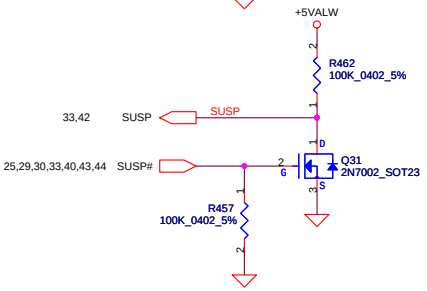
+5VALW TO +5VS



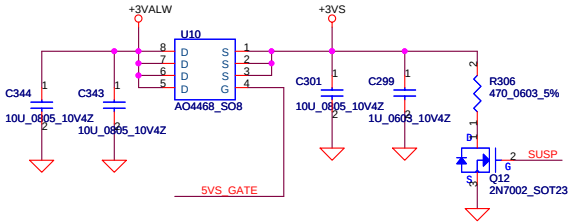
+3VALW TO +3V_SB(ICH8M AUX Power)



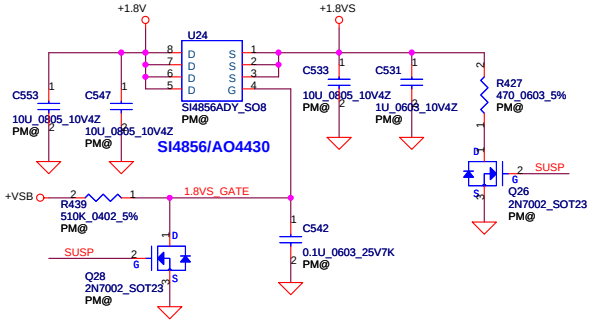


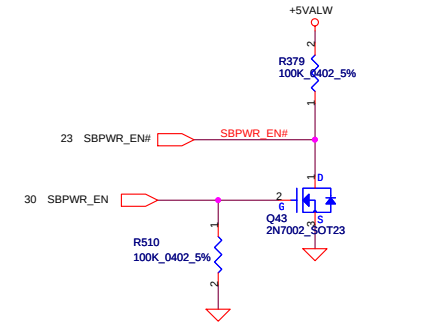


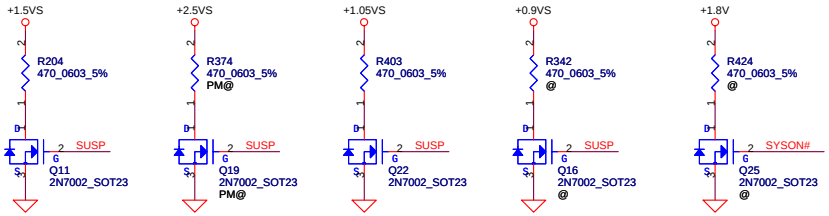
+3VALW TO +3VS



+1.8V to +1.8VS







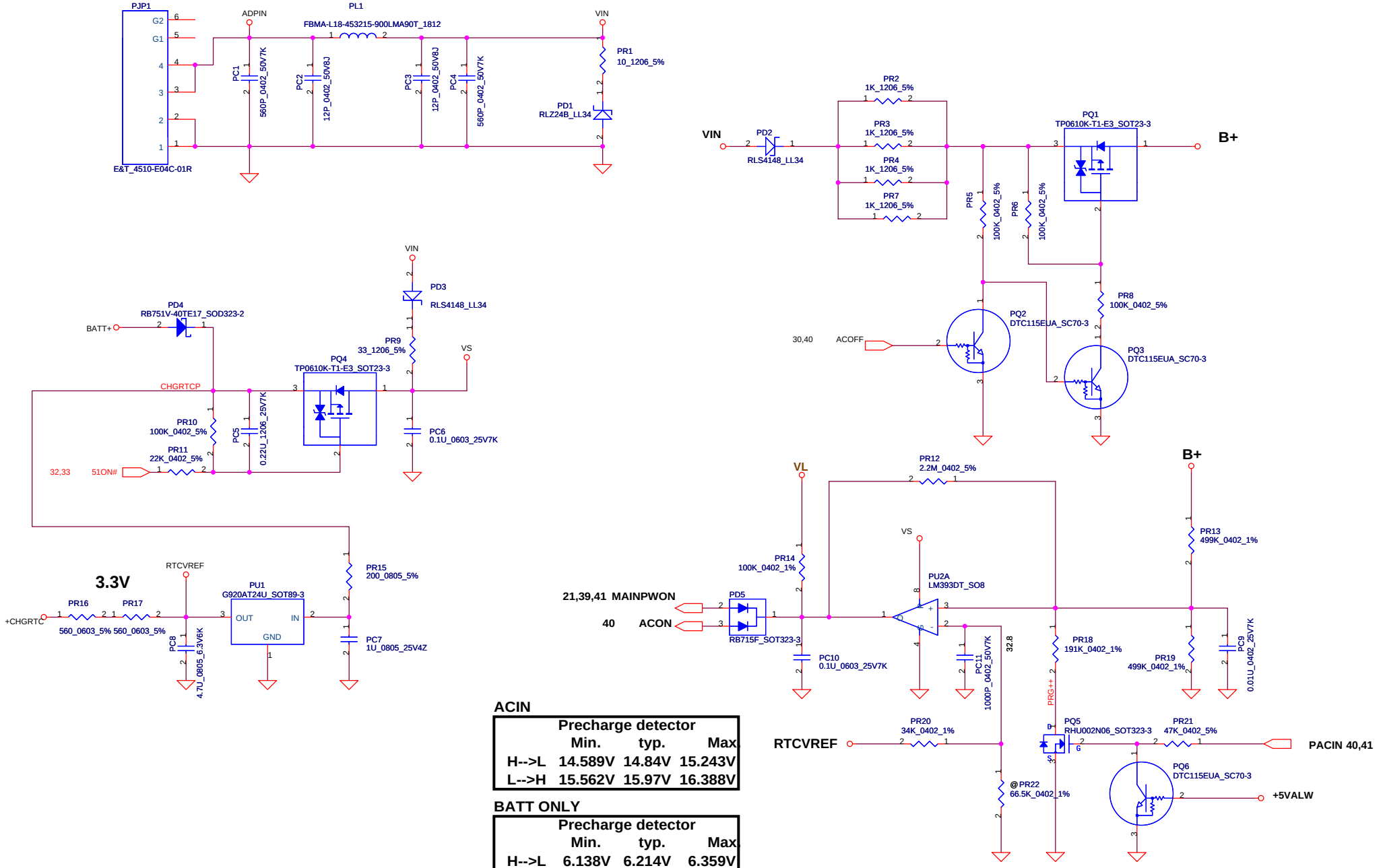
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

Date: Monday, April 23, 2007 | Sheet 37 of 48



ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

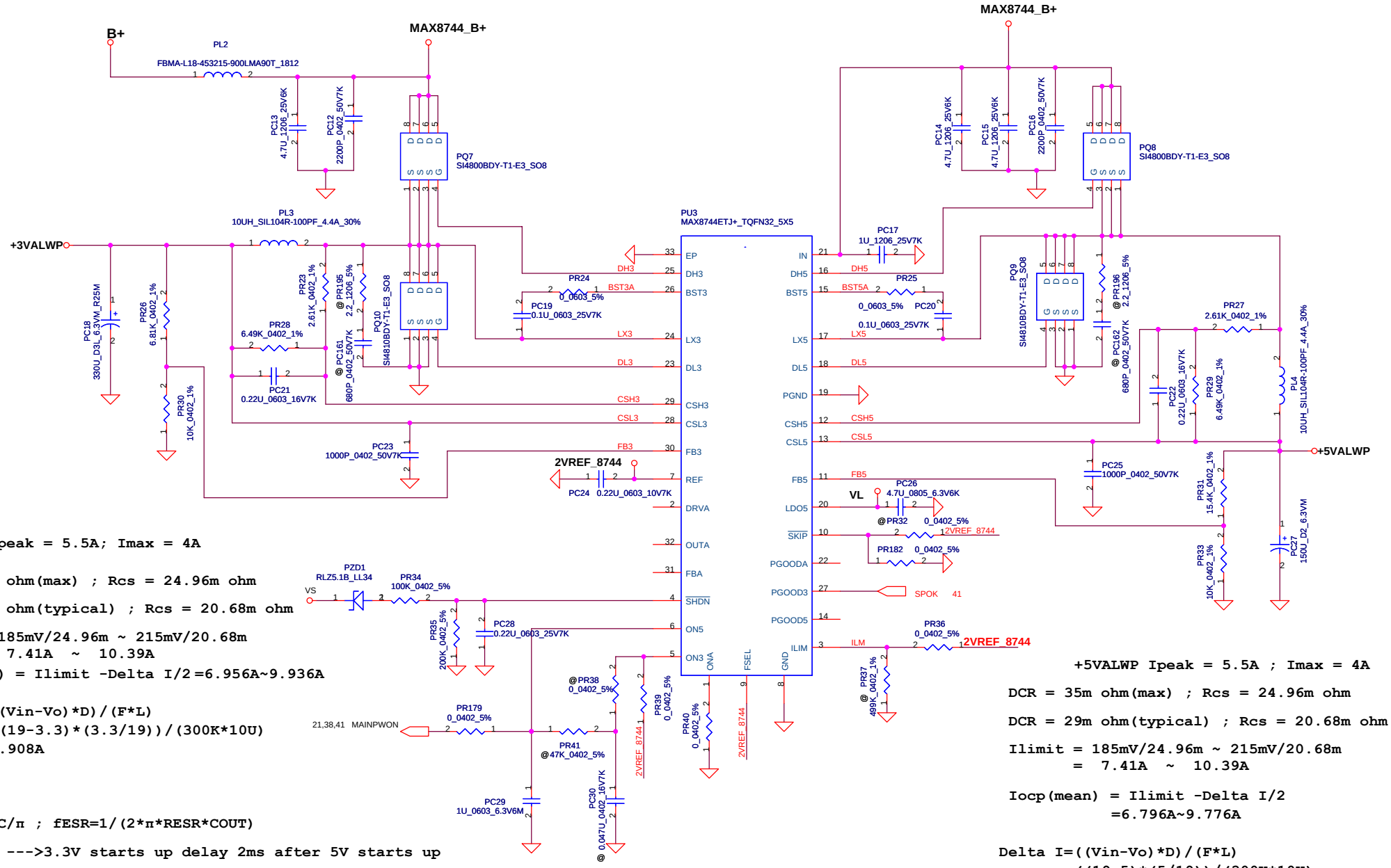
Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/08/22

Compal Electronics, Inc.

Title: DCIN/DECTOR

Size	Document Number	Rev
B	ICL50/ICK70	1.0

Date: Thursday, April 19, 2007 | Sheet 38 of 48



+3VALWP Ipeak = 5.5A; Imax = 4A

DCR = 35m ohm(max) ; Rcs = 24.96m ohm

DCR = 29m ohm(typical) ; Rcs = 20.68m ohm

Ilimit = 185mV/24.96m ~ 215mV/20.68m
= 7.41A ~ 10.39A

Iocp(mean) = Ilimit -Delta I/2 =6.956A~9.936A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-3.3)*(3.3/19))/(300K*10U)
=0.908A

Notes :

fESR<=fOSC/π ; fESR=1/(2*π*RESR*COUT)

ON3 = REF --->3.3V starts up delay 2ms after 5V starts up

+5VALWP Ipeak = 5.5A ; Imax = 4A

DCR = 35m ohm(max) ; Rcs = 24.96m ohm

DCR = 29m ohm(typical) ; Rcs = 20.68m ohm

Ilimit = 185mV/24.96m ~ 215mV/20.68m
= 7.41A ~ 10.39A

Iocp(mean) = Ilimit -Delta I/2
=6.796A~9.776A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-5)*(5/19))/(300K*10U)
1.228A

Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/08/22

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size	Document Number	Rev
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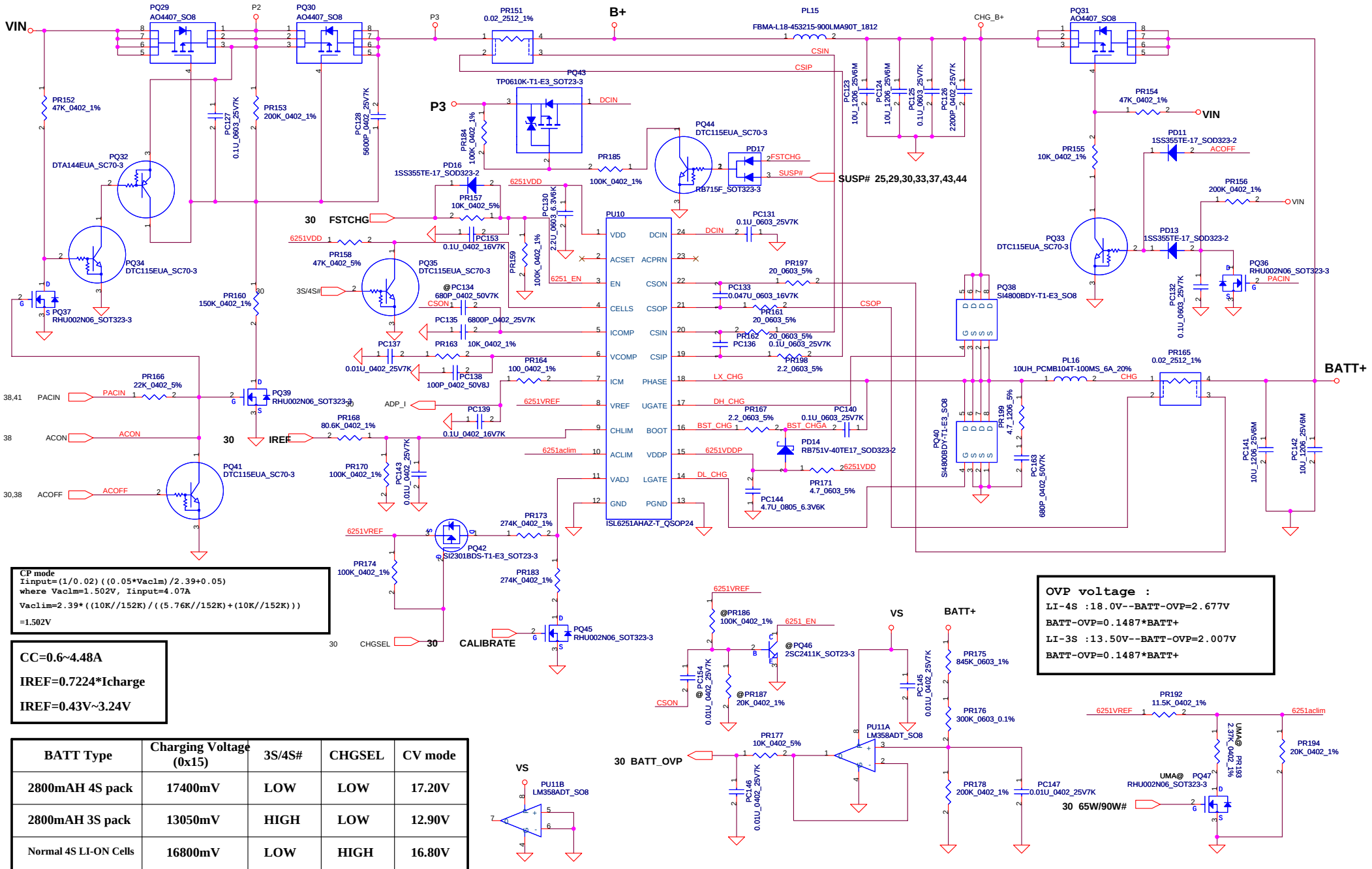
Iada=0~4.74A(90W)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode

Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

Vaclim=2.39*((10K//152K)/((5.76K//152K)+(10K//152K)))

=1.502V

OVP voltage :

LI-4S :18.0V--BATT-OVP=2.677V

BATT-OVP=0.1487*BATT+

LI-3S :13.50V--BATT-OVP=2.007V

BATT-OVP=0.1487*BATT+

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/0822

Compal Electronics, Inc.

Title: CHARGER

Size: C | Document Number: ICL50/ICK70 | Rev: 1.0

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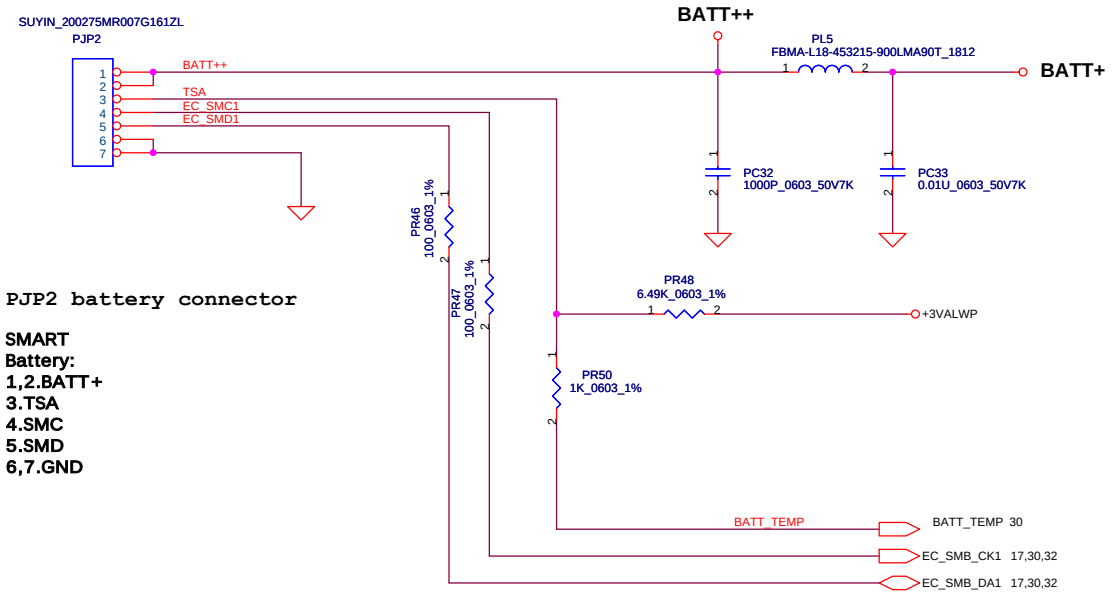
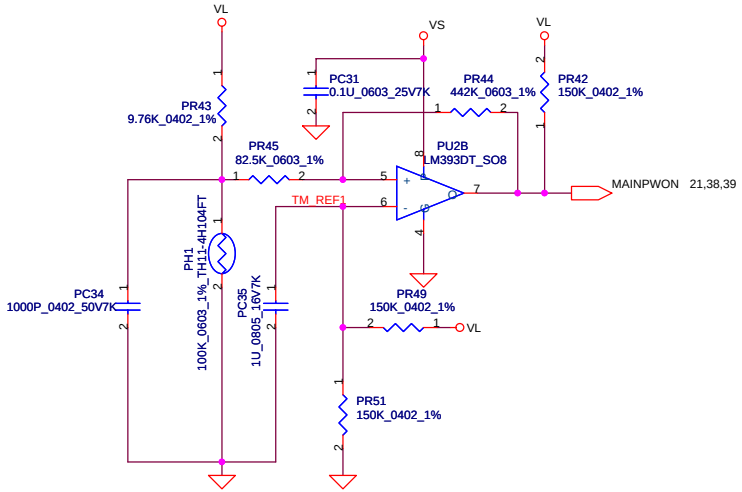
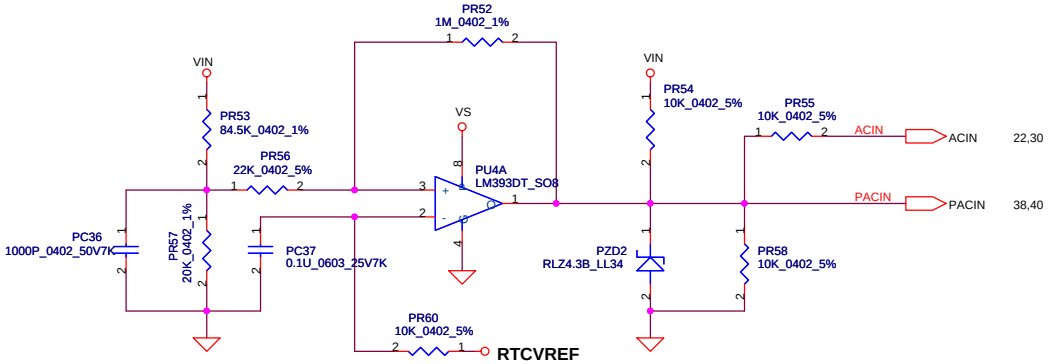
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C

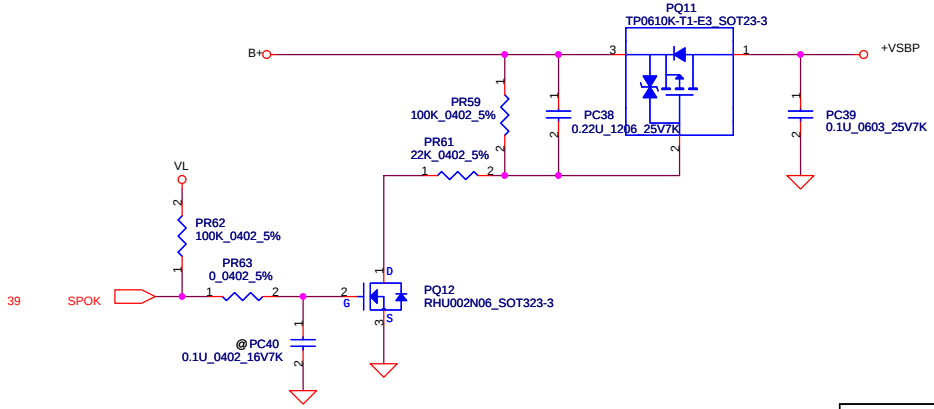


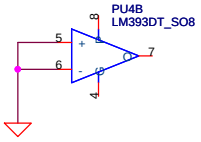
PJP2 battery connector

SMART
Battery:
1,2.BATT+
3.TSA
4.SMC
5.SMD
6,7.GND









Vin Detector	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/08/22

Compal Electronics, Inc.

Title: BATTERY CONN. / OTP

Size	Document Number	Rev
B	ICL50/ICK70	1.0

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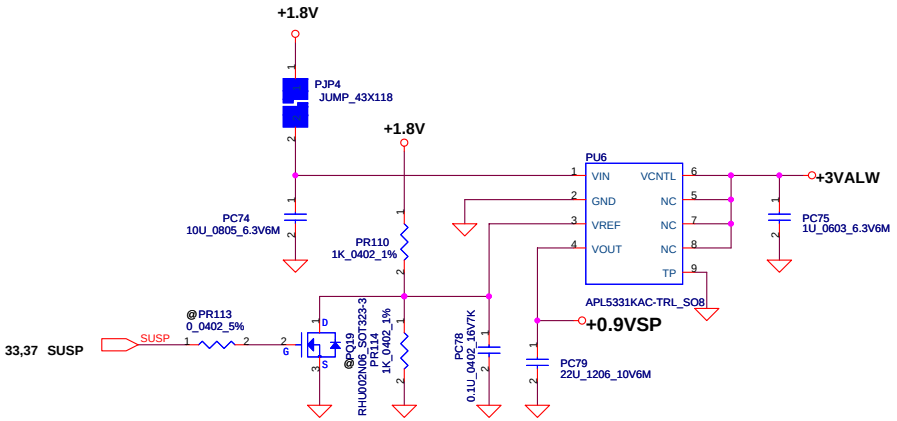
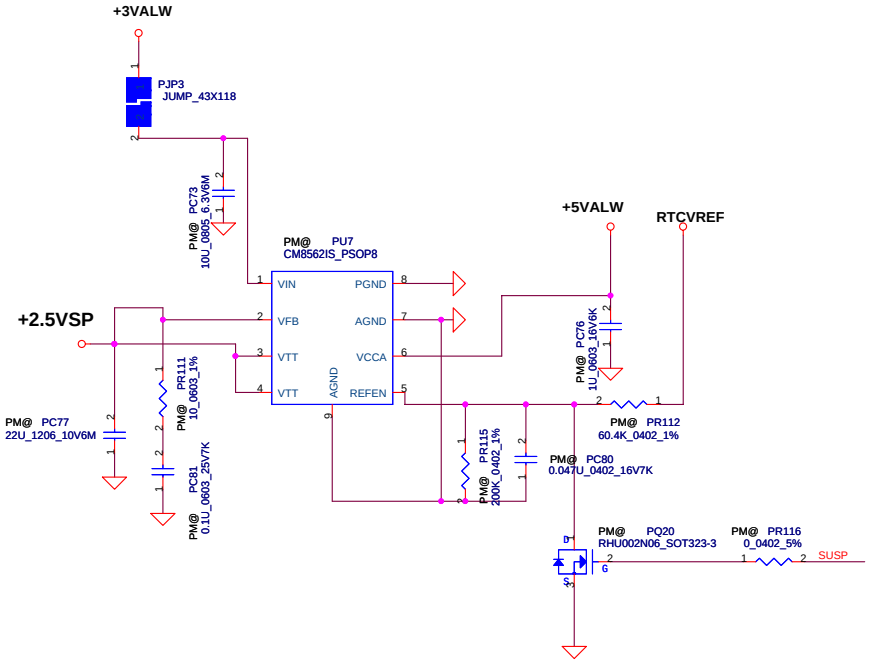
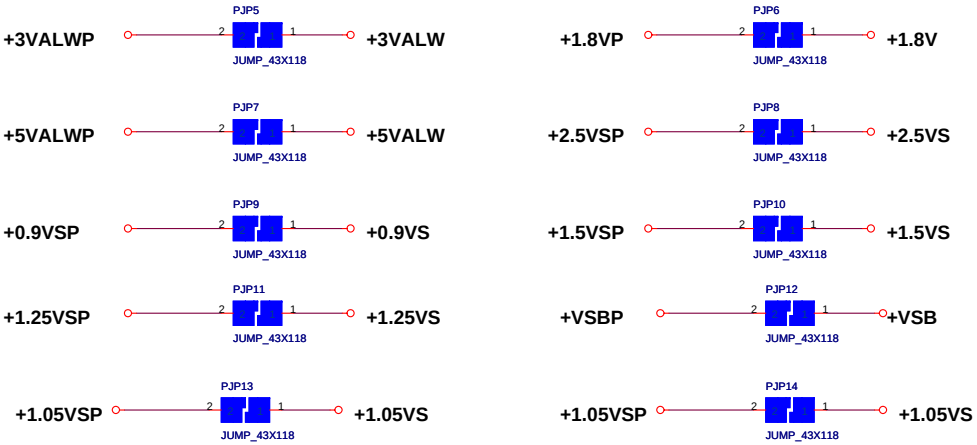






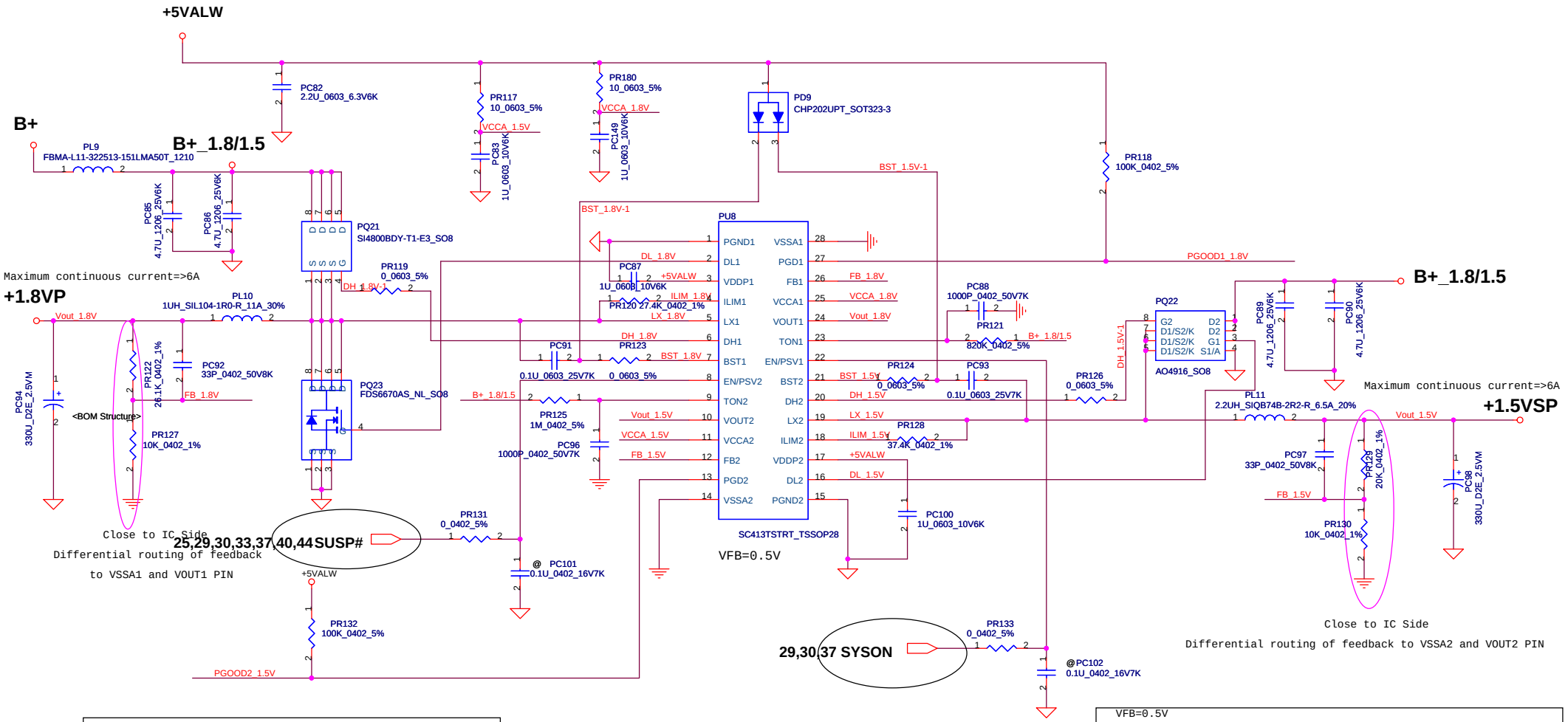
Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/08/22

Compal Electronics, Inc.

Title: +0.9VSP/+2.5VSP

Size	Document Number	Rev
Custom	ICL50/ICK70	1.0

Date: Thursday, April 19, 2007 Sheet 42 of 48



VFB=0.5V
Vo=VFB*(1+PR122/PR127)=1.805V
Ipeak=11.73A, Imax=8.211A
Ton=(3.3E-12*(PR121+37K)*(Vout/VBat))+50ns
=3.3*10e-12*(820K+37K)*(1.8/19)+50ns=0.3179us
FDS6670AS:Rds(on)=>Typ:9 mOhm
Max:11.5 mOhm
Iocp=Ivalley+"Iripple%/2
Iripple=(vin-vout)*(Ton/L)=5.467A, 1/2 Iripple=2.734A.
Ivalleymin=10E-6*(PR120/Rds(ON)max*1.5)
=9*10e-6*(27.4K/0.0115*1.5)=14.295A>11.73*1.2=14.076A
Ivalleymax=10E-6*(PR120/Rds(ON)typ*1.2)
=11*10e-6*(27.4K/0.009*1.2)=27.907A.
OCP==>17.029A~30.641A

VFB=0.5V
Vo=VFB*(1+PR129/PR130)=1.5V
Ipeak=4.39A+2.91A=7.3A, Imax=7.3*0.7=5.11A
Ton=(3.3E-12*(PR125+37K)*(Vout/VBat))+50ns
=0.3201us
AO4916 Rds(on)=>Typ:21 mOhm
Max:27 mOhm
Ivalleymin=9*E-6*(37.4K/0.027*1.4)=8.904A>7.3*1.2=8.76A
Ivalleymax=11*E-6*(37.4K/0.021*1.1)=17.809A
Iripple=(vin-vout)*(Ton/L)=2.546A, 1/2Iriiple=1.273A
Iocp=Ivalley+"Iripple%/2
OCP==>10.177A~19.082A

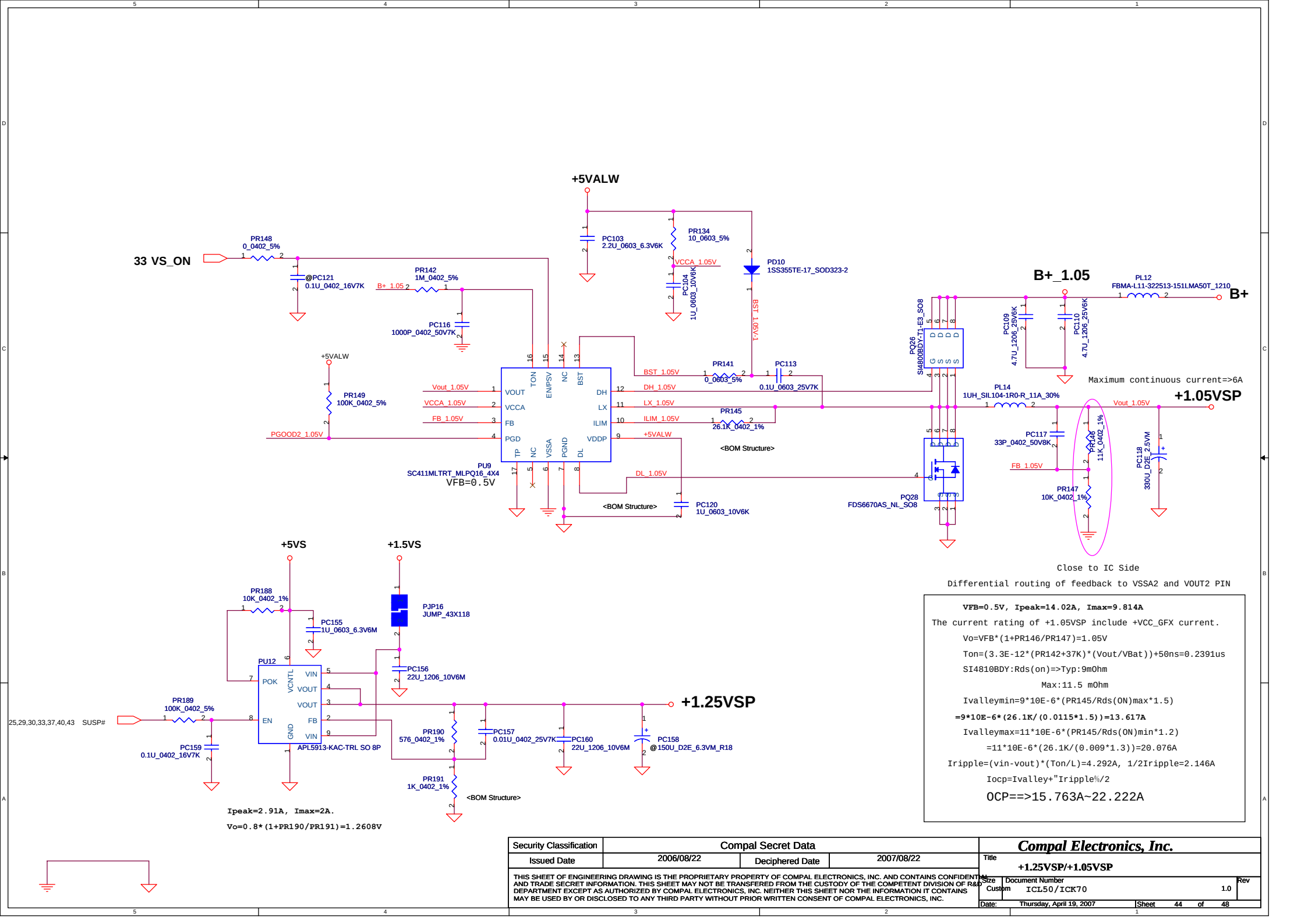
Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/08/22

Compal Electronics, Inc.

Title: +1.5VSP/+1.8VP

Size	Document Number	Rev
Custom	ICL50/ICK70	1.0

Date: Thursday, April 19, 2007 Sheet 43 of 48



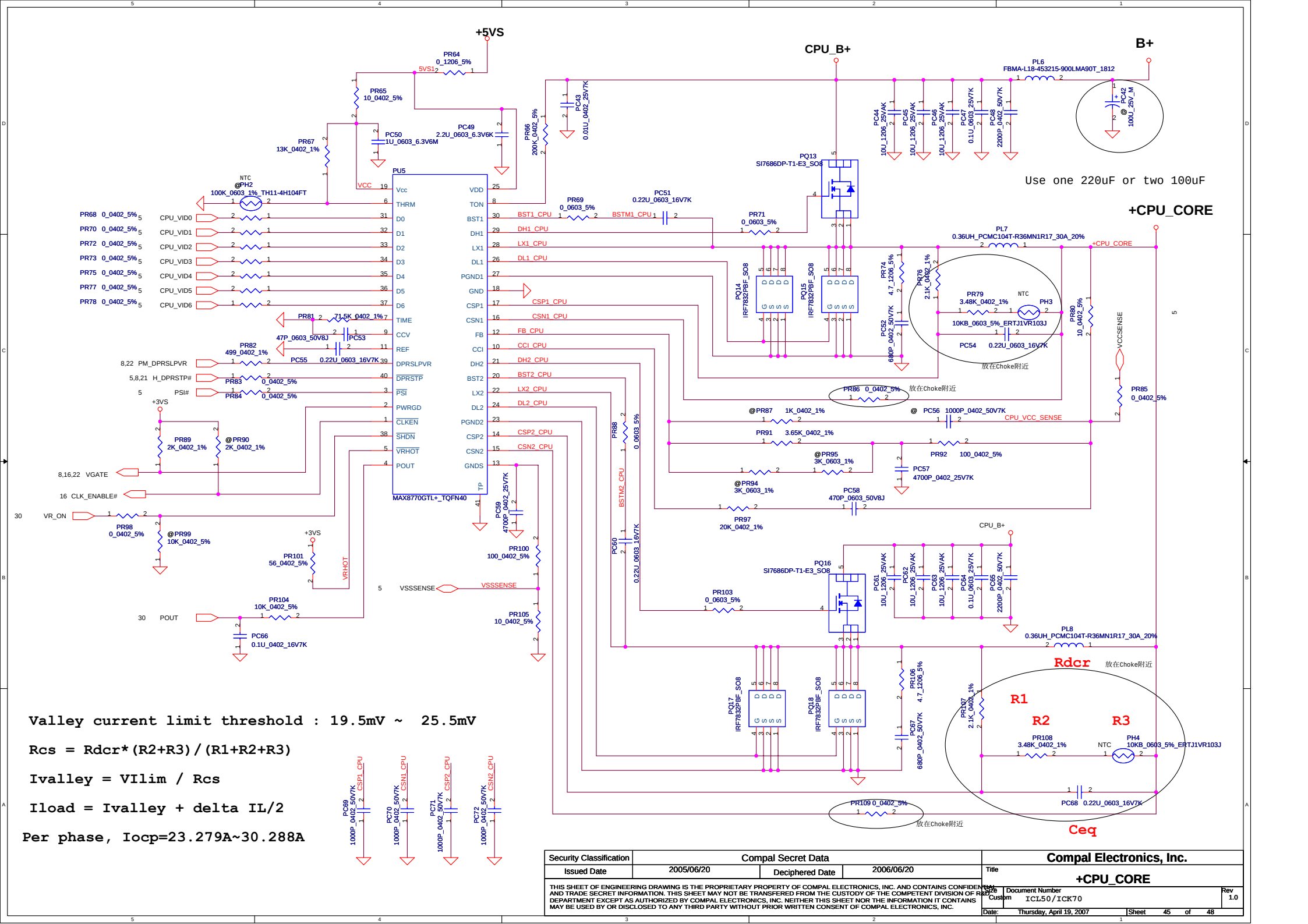
Security Classification	Compal Secret Data		
Issued Date	2006/08/22	Deciphered Date	2007/08/22

Compal Electronics, Inc.

Title: +1.25VSP/+1.05VSP

Size	Document Number	Rev
Custom	ICL50/ICK70	1.0

Date: Thursday, April 19, 2007 Sheet 44 of 48



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.			
Title	+CPU_CORE		
Size: Custom	Document Number: ICL50/ICK70		Rev: 1.0
Date: Thursday, April 19, 2007	Sheet 45 of 48		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU_CORE high side MOS desine change	In order to prevent EOL of SI7840, change to SI7686.	0.1	45	Change PQ13 and PQ16 form SB578400080(S TR SI7840DP-T1-E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N SO8).	10/30/06	EVT
2	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ43 SB906100210(S TR TP0610K)	12/21/06	DVT
3	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ44 SB301150000(S TR DTC115EUA)	12/21/06	DVT
4	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD16 SC1SS355010(S DIO 1SS355) Delete PD12 SC1SS355010(S DIO 1SS355)	12/21/06	DVT
5	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD17 SCSB715F000(S DIO RB715F)	12/21/06	DVT
6	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR184,PR185 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
7	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC153 SE076104K80(S CER CAP 0.1U 0402 16V K X7R)	12/21/06	DVT
8	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ45 SB502060000(S TR RHU002N06)	12/21/06	DVT
9	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ46 SB324110010(S TR 2SC411K)	12/21/06	DVT
10	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR183 SD034274380(S RES 1/16W 274K 0402 1%)	12/21/06	DVT
11	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR186 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
12	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR187 SD034200280(S RES 1/16W 20K 0402 1%)	12/21/06	DVT
13	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC154 and PC146 SE075103K80(S CER CAP 0.01U K 25V X7R 0402)	12/21/06	DVT
14	Noise issue in S3 mode and idle mode.	In order to prevent noise issue in S3 mode and idle mode.	0.2	40	Add PC42 SF22004M210(S CAP 220U_25V_M)	12/21/06	DVT
15	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Change PR157 from SD028000080(s res 1/16w 0 0402 5%) TO SD0281000280(S RES 1/16W 10K 0402 5%)	12/21/06	DVT
16	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR34 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100380(S RES 1/16W 100K 0402 5%)	12/21/06	DVT
17	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR35 SD028100380(S RES 1/16W 100K 0402 5%) to SD028200380(S RES 1/16W 200K 0402 5%)	12/21/06	DVT
18	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PC28 from SE042104K80(S CER CAP 0.1U 25V K X7R 0603) to SE000005ZM8(S CER CAP 0.22U 25V K X7R 0603)	12/21/06	DVT
19	CPU MOSFET switching has interference.	Improve CPU switching interference.	0.2	45	Change PC69,PC70,PC71,PC72 from SE082221J80 to SE068102J80 (S CER CAP 1000P 25V J NPO 0402)	12/21/06	DVT
20	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PU7 SA085620080 from X63470BOL01.	12/21/06	DVT
21	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PQ20 SB502060000 from X63470BOL01.	12/21/06	DVT
22	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR111 SD014100A80 from X63470BOL01.	12/21/06	DVT
23	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR112 SD034604280 from X63470BOL01.	12/21/06	DVT

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR115 SD034200380 from X63470BOL01.	10/30/06	EVT
2	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR116 SD028000080 from X63470BOL01.	12/21/06	DVT
3	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC73 SE142475K80 from X63470BOL01.	12/21/06	DVT
4	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC76 SE135105K80 from X63470BOL01.	12/21/06	DVT
5	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC77 SE116226M80 from X63470BOL01.	12/21/06	DVT
6	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC80 SE076473K80 from X63470BOL01.	12/21/06	DVT
7	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC81 SE042104K80 from X63470BOL01.	12/21/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ25 SB548000310(S TR SI4800BDY).	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ27 SB548100020(S TR 4810BDY)	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PD10 from SC1P202U010 to SC1SS355010.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR135 SD034100380.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR140,SD013000080, PR150 SD028000080.	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR181 SD013100A80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR139 SD034150280.	12/27/06	DVT
15	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR144 SD034100280	12/27/06	DVT
16	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR137 SD034105280.	12/27/06	DVT
17	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR138 SD028100480.	12/27/06	DVT
18	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delelte PC105,PC106 SE142475K80.	12/27/06	DVT
19	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC107,PC151 SE080105K80.	12/27/06	DVT
20	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC108 SE074102K80.	12/27/06	DVT
21	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC111 SE042104K80.	12/27/06	DVT
22	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC112 SE068330K80	12/27/06	DVT
24	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PL13 SH000008Y80.	12/27/06	DVT

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC114 SGA20221D30	12/27/06	DVT
2	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PU9 from SA00001FD80 to SA00001FB80	12/27/06	DVT
3	For SMT BOM convenient.	For SMT BOM convenient.	0.3	40	Change PD14 from SC1H751H010 to SC1B751V010.	12/27/06	DVT
4	Increase _1.5VSP OCP point	Increase _1.5VSP OCP point for +1.25VSP new solution.'	0.3	43	Change PR128 from SD034154280 to SD034374380.	12/27/06	DVT
5	Decrease +1.05VSP OCP point.	Decrease +1.05VSP OCP point.	0.3	44	Change PR145 from SD034324280 to SD034261280		DVT
6	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PU12 SA000015410.	12/27/06	DVT
7	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR188 SD034100280.	12/27/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR189 SD034100380.	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR191 SD034100180.	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR190 SD034576080.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC155 SE107105M80.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC156, PC160 SE116226M80	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC157 SE075103K80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC159 SE076104K80.	12/27/06	DVT
15	Increase +1.5VSP output capacitor.	Increase +1.5VSP output capacitor.	0.3	43	Change PC98 from SGA20221D30 to SGA19331D00	12/27/06	DVT
16	Cost issue.	Cost issue.	0.3	44	Change PC118 from SGA20471D00 to SGA19331D00.	12/30/06	DVT
17	BOM issue.	BOM issue.	0.3	45	Change PH3, PH4 from SL210021F20 to SL200000200	12/30/06	DVT
18	Assembly issue.	Due to assemly hard, delete PC42.	0.3	45	Delete PC42 SM22004M210.	12/30/06	DVT
19	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE142475K80 to SE093106M80	01/04/06	DVT
20	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE153106K80 to SE093106M80	01/04/06	DVT
21	Add pull high resister for VAGTE.	Add pull high resister for VAGTE.	0.4	45	Add PR89 SD034200180(S RES 1/16W 2K 0402 1%)	01/04/06	DVT
22	Delete PQ46	PQ46 has potemtial risk to cause system battery OVP.	0.4	40	Delete PQ46 SB324110010(S TR 2SC411K)	01/04/06	DVT
23	Material shipping issue.	Material shipping issue.	0.4	45	Change PC69, PC70, PC71, PC72 from SE068102J80 to SE074102K80	01/04/06	DVT

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Cost down	Cost down	0.5	40	Change PQ38 from SB548100020 to SB548000310.	03/09/07	PVT
2	Cost down	Cost down	0.5	40	Change PQ40 from SB548100020 to SB548000310.	03/09/07	PVT
3	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PR199 SD001470B80(S RES 1/4W 4.7 1206 +-5%)	04/01/07	Pre-MP
4	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PC163 SE074681K80(S CER CAP 680P 50V K X7R)	04/01/07	Pre-MP
5							
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