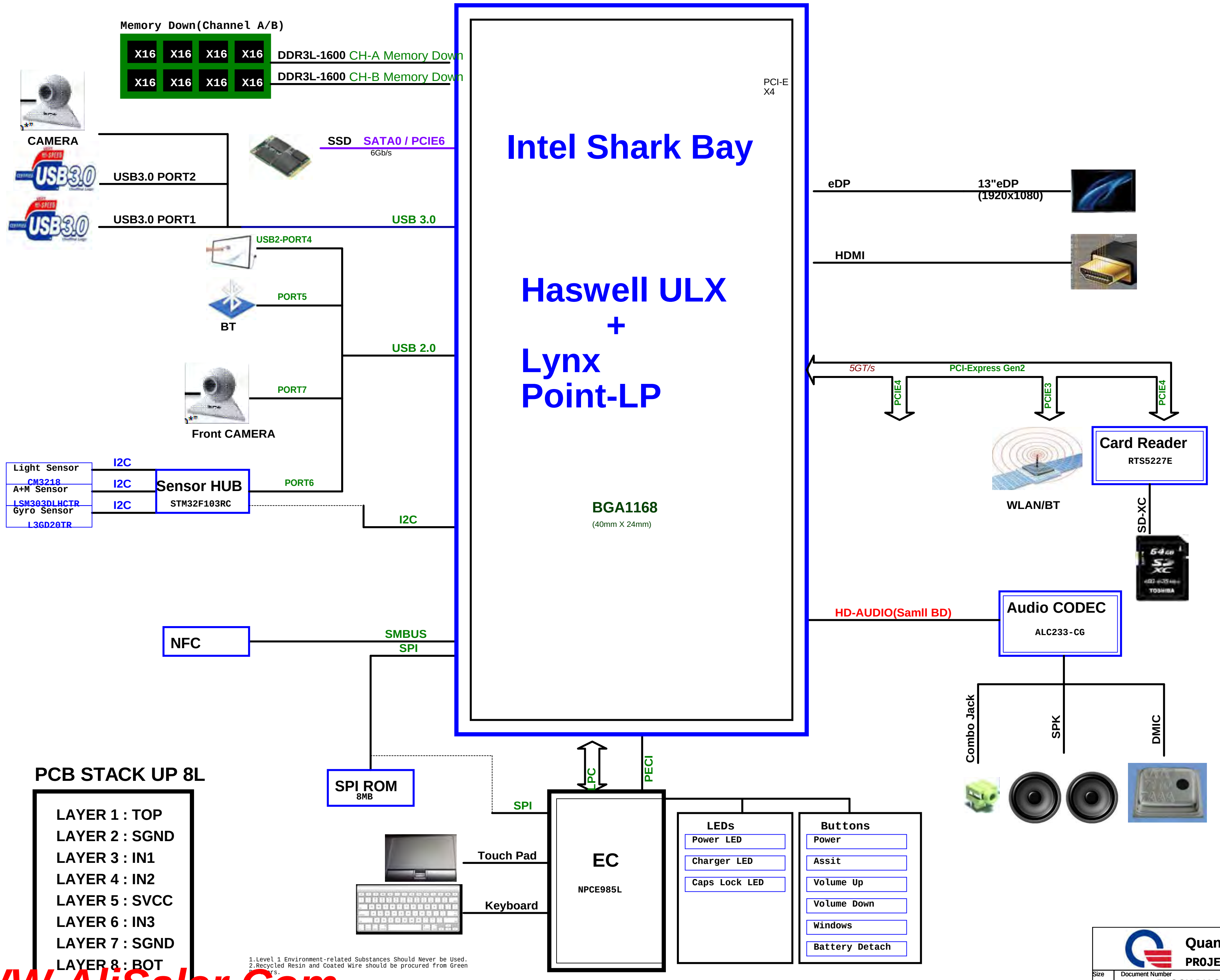
1

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

Mule BLOCK DIAGRAM



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green ...rs.

Quanta Computer Inc.		
PROJECT : FI1		
Size	Document Number: BLOCK DIAGRAM	Rev 1A
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Change List

DVT-2013-05-05
P15 Add serial resistor RP11~RP16 on K/B matrix
Reason :For ESD protection
Possible Risk: no

DVT-2013-05-05
P4 Change netname of GPIO 78 from EC_A20GATE to GPIO78
P16 Remove EC_A20GATE
Reason : EC_A20GATE is not necessary

DVT-2013-05-05
P9 PCH GPIO29 use for WLAN_PW_EN
Reason :Change the power well of WLAN_PW_EN from sus to DSW. .

DVT-2013-05-05
P20 Add R24460 without mount for TPS2543 .
Reason :Reserve for TPS2543 .

DVT-2013-05-05
P22 remove R671,R673 for cost down .

DVT-2013-05-05
P22 change R2442 from unmout to mount
P22 change R656 from mout to unmount
Reason :Change PLTRST#_WLAN instead of PLTRST for RTD3

DVT-2013-05-05
P22 Add a AND gate U30 for WLAN power enable
P16 add GPIO84 for EC_WLAN_PWR_EN

DVT-2013-05-05
P22 Change WLAN_WAKE# PU power well from +3V_S5 to +3V_S5_DSW .
Reason :The signal is belong to" DSW " power well

DVT-2013-05-06
P15 unmount KB 220P (C184~C207)

DVT-2013-05-08
P9 Add TP150 for ME

DVT-2013-05-10
P23 Add U54 for SATA & PCIE Detect
P23 Add +3.3V PU R24461 10Kohm

DVT-2013-05-10
P12 Add C302 0.47uf capacitor for inrush current.(VCCDSW3_3)

DVT-2013-05-10
P17 Add mode_lid-2# signal
P16 Add KR28 PU and change EC GPIO32 from IMVP_PWRGD to MODE_LID-2#

DVT-2013-05-10
P25 remove CN2 and add SW3 ,SW4

DVT-2013-05-10
P18 MR2,MR3 mount

DVT-2013-05-11
P19 R200,R202 change from 2.2k to 4.7k for VEVS 7-1 DDC 130ohm test item

DVT-2013-05-13
P16 Change EC GPIO55 from DRAM_VOLTAGE_SET to SIO_WAKE_GPIO27#
P11 GPIO27 add SIO_WAKE_GPIO27# From EC

DVT-2013-05-13
P8 Change Y1 package for Broadwell requirement

DVT-2013-05-13
P8 Change Y1 package for Broadwell requirement

DVT-2013-05-13
P16 Add KC16 150 pF for EC_PECI

DVT-2013-05-14
P11 Add R24462 100K pull down for CR_PW_EN and unmount R297

DVT-2013-05-14
P36 Change U29 to AL000527000 and power source from +5V_WAKE to +3V_WAKE
P36 Add R24470 ,R24469 to PD,R2449 mount, remove R2450
P36 Add R24471 to PD
P36 Remove R2384 and mount R2451
P36 Add R24472 for SH_ALS_INT# PU

DVT-2013-05-14
P21 mount L2007,L2008,L2009

DVT-2013-05-14
P18 Change MR12,MR13,MR14,MR15,MR16,MR17 from 43ohm to 20 ohm

DVT-2013-05-15
P15 remove H19

DVT-2013-05-16
P17 Change U51 as AL000527000
P17 Change R2413 as 40.2K ohm and mount;Change R24455 as 100Kohm
P17 remove R258,R259,R2436,R2435

DVT-2013-05-16
P11 Change R2433,R304,R310,R308,R297,R306 from mount to un-mount .

DVT-2013-05-16
P4 Change the netname of GPIO77 from EC_EXT_SMI# to GPIO77
P8 Change the netname of GPIO35 from GPIO35 to EC_EXT_SMI#

DVT-2013-05-16
P16 Add KD5 for EC_PWROK

DVT-2013-05-16
P17 Change U52 from G5254T11U to G527ATP11U
P17 mount R258 40.2k ohm and change R24456 as 100k ohm
P17 Change U26 from G5254T11U to G527ATP11U
P17 mount R2436 40.2k ohm and change R24454 as 100k ohm

DVT-2013-05-19
P21 Change U53 from G5254T11U to G527ATP11U
P21 Change R2431 to 40.2Kohm and Add R24473 as 100K ohm

DVT-2013-05-19
P22 Change U27 to G547E1P81U
P22 Delete R2454

DVT-2013-05-19
P4 Change R271,R272,R273,R274,R275,R276,R277 to 100Kohm

DVT-2013-05-19
P7 Change R42 as 100Kohm

DVT-2013-05-19
P8 R278,R279,R280,R281 change to 100Kohm, and remove R2048

DVT-2013-05-19
P9 Change R73, R282 from 10k ohm to 100k ohm

DVT-2013-05-19
P10 Change R24474(no mount), R24475, R86 from 10k ohm to 100k ohm,and remove RP4

P11 Change R283, R285, R300, R315, R313, R317,
R311, R296, R290, R291, R301, R303, R305, R307, R309, R312,
R314, R316(no mount), R318, R319, R320, R2433(no mount), R298,
R299, R304(no mount), R295, R310(no mount), R308(no mount),
R284, R112, R24448, R115, R292, R287, R294, R116, R117, R118, R119,
R286, R289, R297(no mount), R128(unmount),R114, R122, R306(no mount),
R125, R126(unmount), R127, R129(no mount), R130,
R131(no mount), R132, R133(no mount), R134, R135(unmount),R293
from 10k ohm to 100k ohm
P16 Change KR2, KR4, KR19, KR26, KR27, KR28 from 10k ohm to 100k ohm
P22 Change R24445,R2446 from 10k ohm to 100k ohm
P4 Change R14,R15 from 10k ohm to 100k ohm

DVT-2013-05-21
P36 U29 PIN1 change +3V_SENSORHUB for optional non CS design
P36 R2451 change +3V_S5 for optional non CS design
P36 change U29 ,C2337,R24469,R2449,R24470 to un-mout

DVT-2013-05-21
P22 Add R24476 0 ohm
P22 Mount R656
P22 Un-mount R2446,R24442,Q34,Q35,R2447,U28,R2442,R2443,U30,C2336

DVT-2013-05-21
P8 Change R62 as 330ohm,change CON1 P/N

DVT-2013-05-22
P20 Add C2432,C2433 0.22uF CAP

DVT-2013-05-22
P23 :TP function mount D8,D9,D10,D11,D12 for ESD

DVT-2013-05-22
P25 :Change SW1 as DHP00XJ1J01

DVT-2013-05-23
P23:change Q8 as BAM34040001

DVT-2013-05-28
P36:Mount R2359,R2361,R2364,R2365,R2367,R2369

DVT-2013-05-23
P24: Add R24477 for EMI

DVT-2013-05-23
P21: Change U45 as AL000918000,U46,U47 as AL000916007
P21: Change R2149,R2147;R786,R790;R2152,R2148

DVT-2013-05-25
P11: Mount R310

DVT-2013-05-25
P17: Change CON6 FP(P/N: DFHS40FS104)

DVT-2013-05-25
P23: Change SW2,SW3,SW4 FP, and reserve D45,D46,D47,D48,C2435,C2436,C2437

DVT-2013-05-25
P4:Add R24480 and Reserve R24478,R24479

DVT-2013-05-25
P8:R24451 change to 15Kohm

DVT-2013-05-25
P18:unmount MC21,MC24,MU2,MC23,MR20,MU3,MR22,MR23,ML4
P18:mount ML2,MR24

DVT-2013-05-27
P19: R186,R187,R189,R190,R192,R193,R195,R196 change to 470 ohm

DVT-2013-05-27
P19: R186,R187,R189,R190,R192,R193,R195,R196 change to 470 ohm

DVT-2013-05-27
P22: Remove R236,Q17,U28,R2442,R2443,U30,R24442,R2446,Q35,R2447,C2336,Q34,R24445,Q36

DVT-2013-05-27
P11:R315 unmount

DVT-2013-05-28
P22:Con14 Change to DFFC04FR066

DVT-2013-05-29
P33:add R24481 33ohm and reserve C2438

DVT-2013-05-29
P17:L10 mount

DVT-2013-05-30
P23:Delete R2407,R2408

DVT-2013-05-30
P7:mount C49 680P

DVT-2013-05-30
P7:mount C49 680P

DVT-2013-05-30
P21:unmount U53,R24473,C2415,R2431,R219 and add R24484 and R24482

DVT-2013-05-31
P19:unmount R185,R188,R191,R194

DVT-2013-05-31
P17:Add U56,R24485

DVT-2013-06-01
P23: remove R342

DVT-2013-06-01
P22: ADD C303,R24486

DVT-2013-06-03
P24: Change F10,F12 footprint

DVT-2013-06-03
P20: Add R24488,R24489,R24490,R24491,R24492,R24493,R24494,R24495

DVT-2013-06-04
P16: Add KR29

DVT-2013-06-04
P19: Add TU3,TC2,TR3,TR4,TQ2

DVT-2013-06-04
P25: Add R24496, R24497

DVT-2013-06-07
P8: Unmount R59,R60,R61,R64,R65,R66

DVT-2013-06-12
P16: Unmount KC16

DVT-2013-06-13
P19: mount R185,R188,R191,R194

DVT-2013-06-19
P25: Change Q25,Q26 PN BA001240Z11

DVT-2013-05-16 (Power Portion)

P27 POWER 3VPCU&RVCC5(TPS51427)
Removed PG1,PG2,+5V_WAKE-1 and +3V_WAKE-1
Reason : DVT is not necessary.

P28 POWER 1.35VSUS/VTT_MEM
Change PCB footprint of PU4 from 21P to 26P
Reason : 21P is incorrect componet.
Removed PC75
Reason : PC75 will lead to delay DDR_PG signal.
Possible : DDR_PG signal will be unstable.
Removed PG3 and +1.35V_SUS-1
Reason : DVT is not necessary.

P29 POWER +1.05V/+1.5V/Thermal
Change PC81 from CH6104K9A00 to CH6104M9901.
Reason : To decrease the temperature of PQ34 and PQ35.
Removed PG4 and +1.05V_M-1
Reason : DVT is not necessary.

P30 POWER(BAT IN / ADAIN /UL)
Change “One-Shot 10ms POCHOT# For ADP/BAT” circuit to “One-Shot 10ms POCHOT# For ADP”.
Reason : Order to fine-tune for new 45W adapter.
Change System OVP for VEDS from “+5V_WAKE-1 ,+3V_WAKE-1, +1.35V_SUS-1 and +1.05V_M-1”
to “+5V_WAKE ,+3V_WAKE, +1.35V_SUS and +1.05V”
Reason : +5V_WAKE-1 ,+3V_WAKE-1, +1.35V_SUS-1 and +1.05V_M-1 are removed

P31 POWER CHARGER (ISL88732)
Change PR215 from 95.3K to 140K.
Change PR217 from 34.8K to 31.6K.
Change charge current from 2.81A to 2.688A
Reason : Modify Max Charge Current Limit from 4.5A to 3.2A.

DVT-2013-05-23 (Power Portion)
To change PSW P/N from DHP0TJ42600 to DHP00XJ1J01.
Reason : To change the swich component.
To change PU9 P/N from AL088732000 to AL088732001.
Reason : IC version update.
To add PR196 and to change PC141 P/N from CH21006KB16 to CH5102K9B06.
Reason : To reserve a RC delay time filter in ISENSE_IN route.

DVT-2013-05-29 (Power Portion)
To change PR23 value from 24Kohm to 24.9K.
Reason : To modify the Vhcore Loadline.

To use PC10 1200pF and to close PC9 1000pF.
Reason : To modify the Vhcore load transient.

To use PC21~PC23.
Reason : To modify the Vhcore load transient overshoot.

To correct PU107A into PU104A.
Reason :PU104A and PU104B is a group IC.

DVT-2013-06-05 (Power Portion)
Change PR23 from 24.9K to 23.7K
Change PC170 from 470PF to 220PF
Reason : modify Vhcore’s Dynamic Iout accury.

DVT-2013-06-06 (Power Portion)
Update FI1 Power portion DVT 0606 schematics
To add PR145 430K and PR141 in parallel.
Change PR141 from 470K NTC to 680K NTC
Change PR146 from 6.98K to 0 ohm.
Reason : The minimum temp of PQ36 trigger point will be increased from 86C to 98C

DVT-2013-06-07 (Power Portion)
FI1 power portion 0607 update(for DVT building BOM)
Change PR141,PR146 and PR145 from DVT value to EVT value.
Reason : PR141 680K lack parts.

MP-2013-08-09
P21: Change C932 as 1u
P21: add D49,R24517 , C2446

MP-2013-08-10
P10: Add R24518,R24519,R24520,R24521,R24522
P23: Change C330,C317,C319 and reserve C2447

MP-2013-08-11
P19: remove R185,R188,R191,R194 as 330 ohm,
add C2448,C2449,C2450,C2451

MP-2013-08-16
P21: R804, R2145 change to 0 ohm
P17: Change F2

PVT-2013-07-18 (Power Portion)

P26,P27,P29
Change to Short pad PR7,PR15,PR25,PR27,PR838,PR54,
PR45,PR53,PR55,PR37,PR231,PR96,PR116,PR193
Reason : PVT stage do not need to reserve 0 ohm.

P27 POWER 3VPCU&RVCC5(TPS51427)
Change PC44,PC46 from CH7221M8601 to CH7221MT603
Reason : NEO assign Cap P/N.
Add +1.35V_SUS discharge circuit (PR64,PR65,PR67,PR69,PQ16,PQ17)
Reason : +1.35V_SUS discharge

P29 POWER +1.05V/+1.5V/Thermal
Add PC 151 parallel with the PR220

P30 POWER(BAT IN / ADAIN /UL)
Change PG5 PCB foot print from short pad jumper to RC 0603

P31 POWER CHARGER (ISL88732)
Add PC54 parallel with the P161
Reason : Avoid BAT over voltage.

PVT-2013-07-18
P8: reserve Q46 , R24498 for no power issue
P16:EC GPIO85 add EC_RTC_RST for workaround solution
P12:R138,R139 change to short pad.
P13:DR1,DR2 change to short pad.
P14:DR50,DR53 change to short pad.
P16 KL1,KR25,KR18 change to short pad.
P17 add U58,R24499,R24501,R24500,C2444, remove F6
P22 R619 change to short pad.

PVT-2013-07-19
P17 change F2 footprint

PVT-2013-07-19
P22 Add R24507,R24508 and unmount R24486

PVT-2013-07-19 (Power Portion)
modified 1.35V_SUS discharge ciruit
Reason: change PQ17 from dual package to single package.

PVT-2013-07-21
P10 change R95,R96,R97,R98 to shortpad
P17 change R329 to shortpad
P36 change R2374 to shortpad
P21 delete L2008,L2009

PVT-2013-07-22 (Power Portion)
P31 POWER CHARGER
Added EC176 0.1U/25V/Y5V_4
Reason: EMI suggestion
P30 POWER(BATIN/ADAIN/UL)
Added EC11 0.1U/50V/X7R_6
Reason: EMI suggestion

PVT-2013-07-22
P4 change R24480 to shortpad
P17 change R2437 to shortpad
P17 unmount R24455,R24454 ,C294,C295
P21 change R219 to shortpad
P11 mount R308,R306
P25 Change R226 as 120 ohm,R264 as 300 ohm;
R263 as 680ohm,F18 unmount
P25 Add R24509,R24510 and Q47

PVT-2013-07-23
P17 reserve D24

PVT-2013-07-27
P17 Change the R185,R188,R191,R194 as 330 ohm

PVT-2013-07-29
P17 unmount R24455,R24454 ,C294,C295,R2438,R2448,
mount R24512,R24511

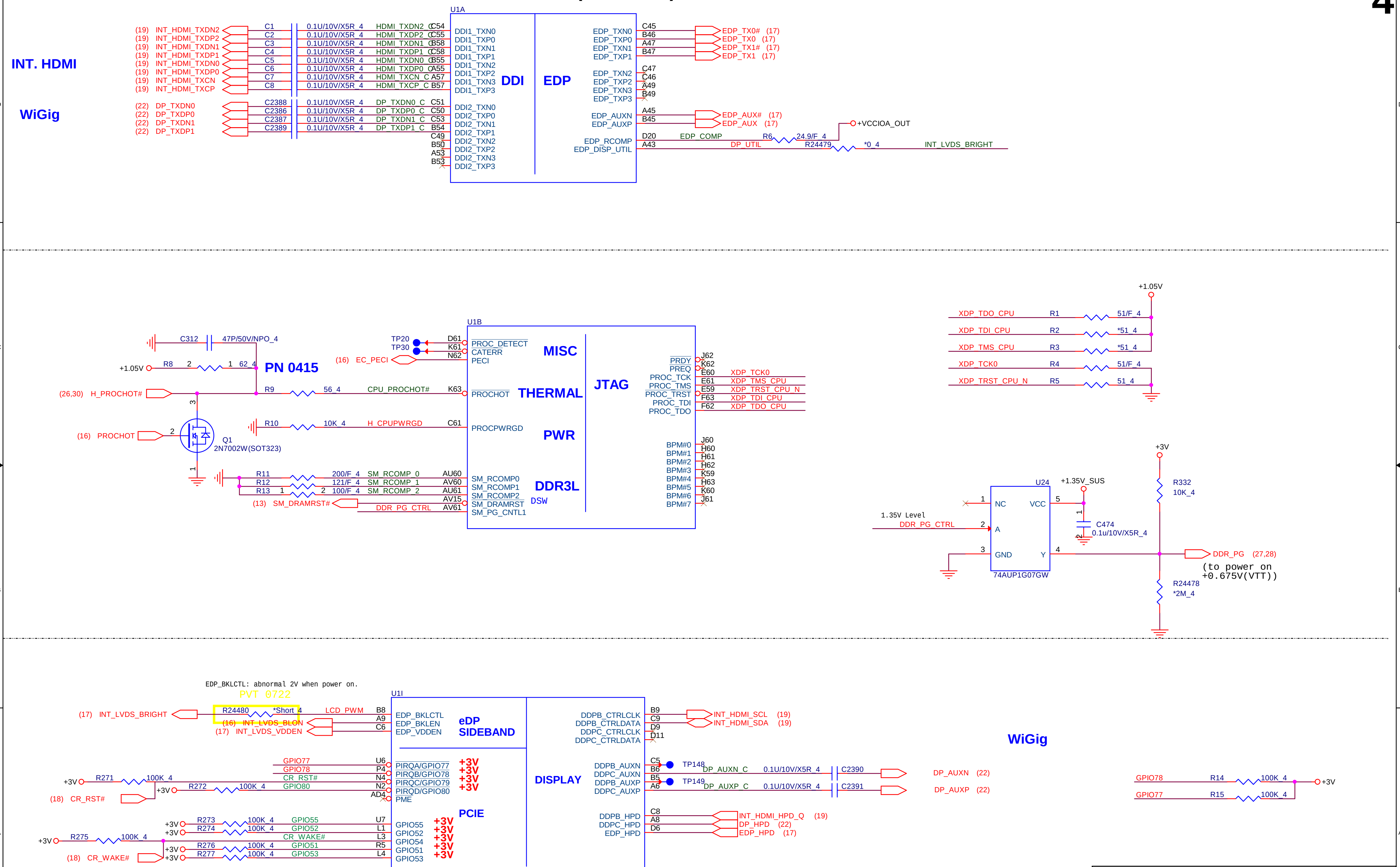
PVT-2013-07-30
P36 Change U20 AR0W08D0000(FW26)

PVT-2013-07-31
P17 R24512 change to 0 ohm

PVT-2013-08-01
P17 change C2331,C2332,C2333 to 2.2u

PVT-2013-08-01
P19 change R208 to 57.6k,R212 to 23.7k
P19 change R206 to 100k,R211 to 42.2k

Haswell ULT (DISPLAY)



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PROJECT : FI1

Size	Document Number	Rev
	HSW MCP(Display/eDP)	1A
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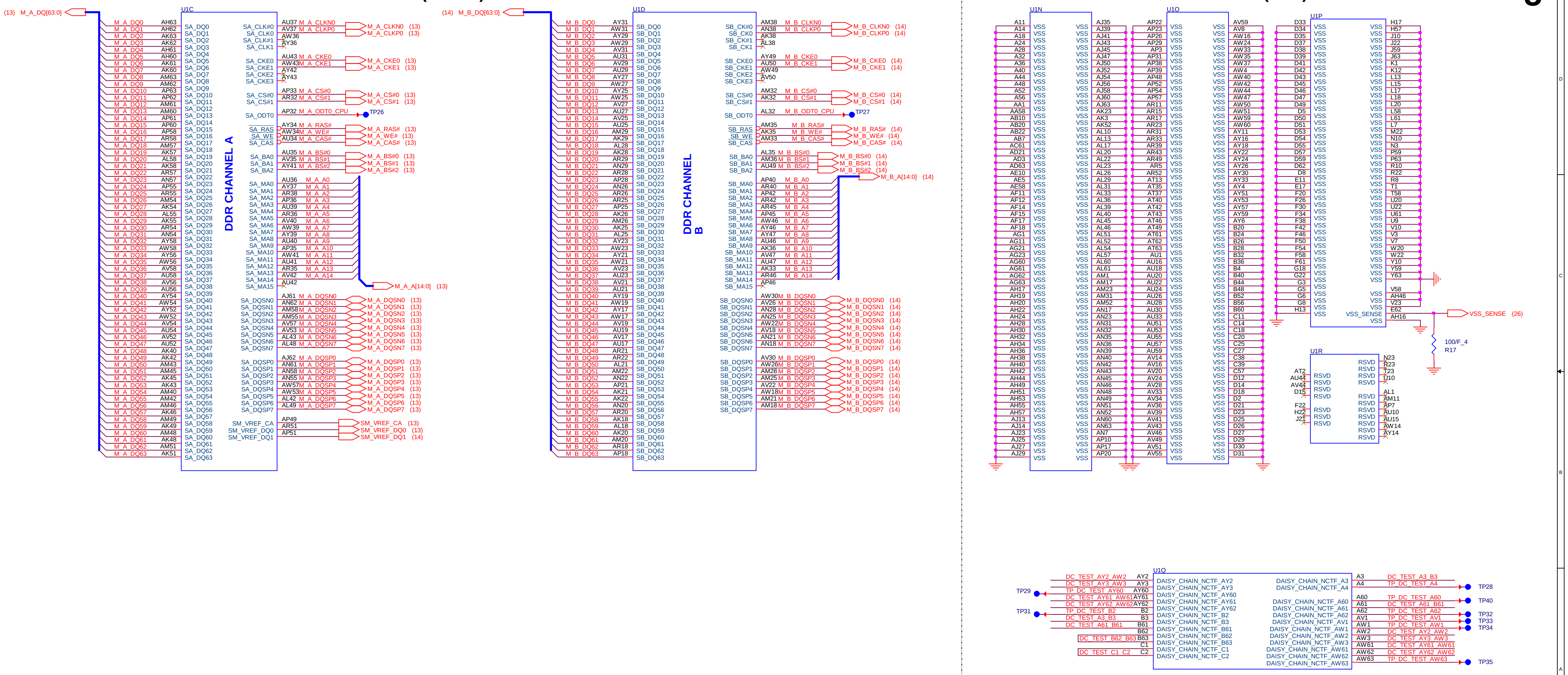
Haswell ULT (DDR3L)

HSW ULT(GND)



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PROJECT :FI1

Size	Document Number	Rev
	HSW MCP(Memory)	1A

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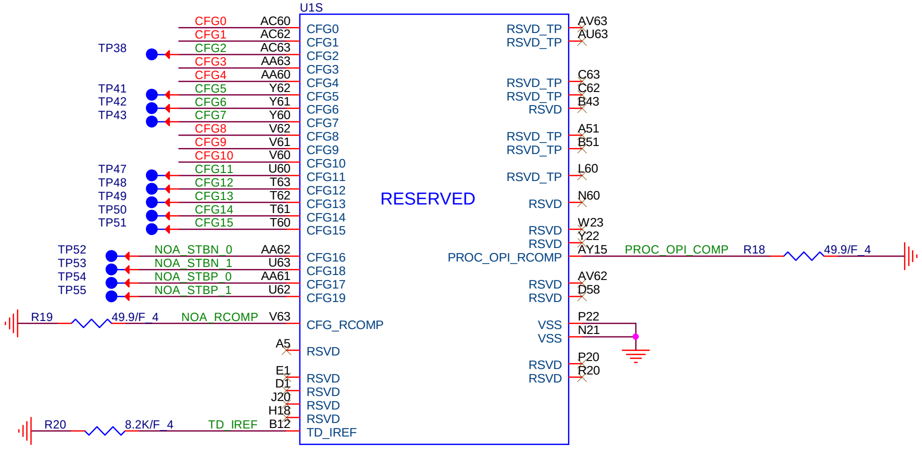

Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R21 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R22 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R23 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG4 R24 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG8 R25 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R26 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R27 *1K_4

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PROJECT : FI1

Size	Document Number	Rev
	HSW MCP(CFG)	1A
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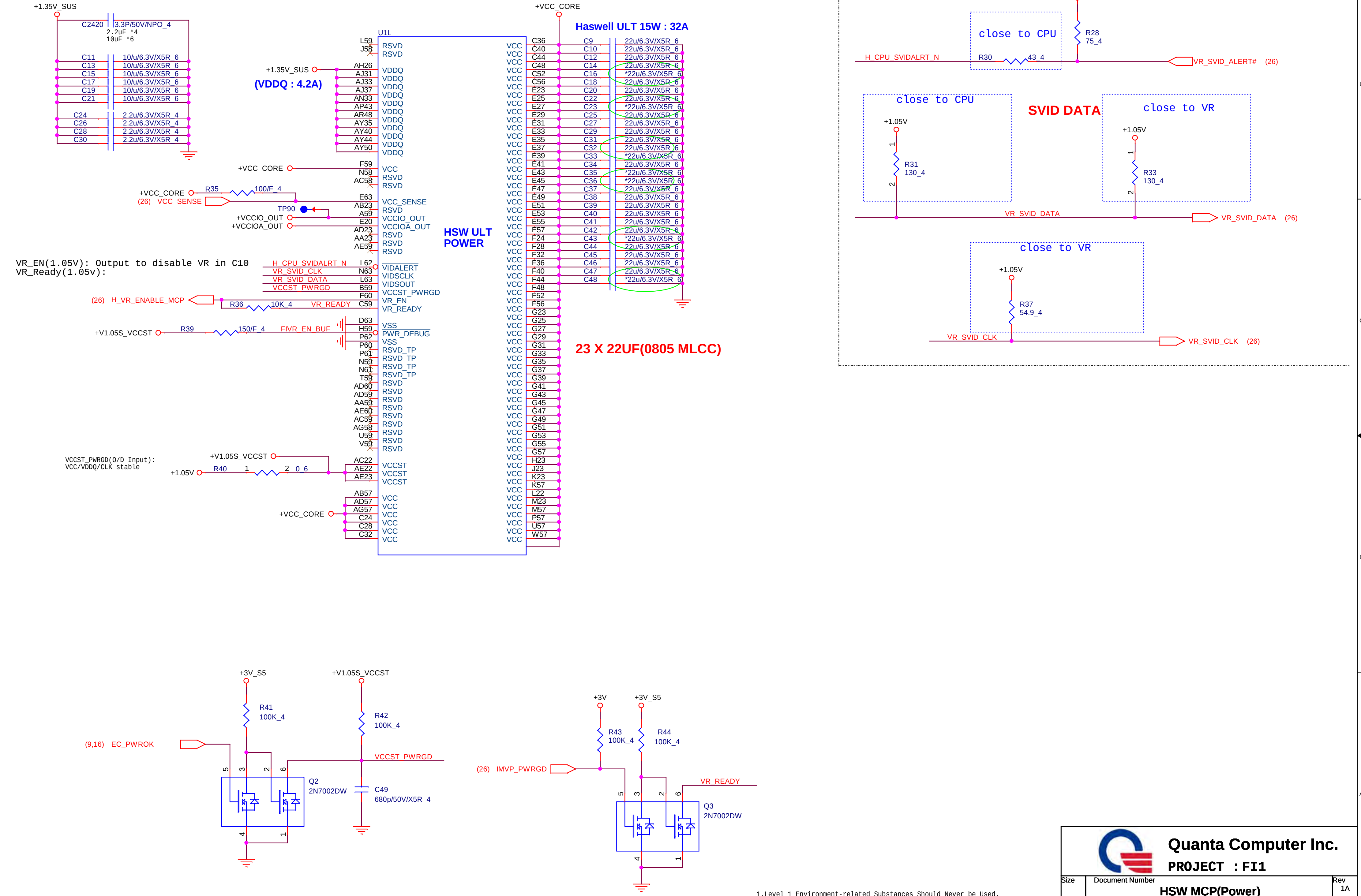
Haswell ULT MCP(POWER)



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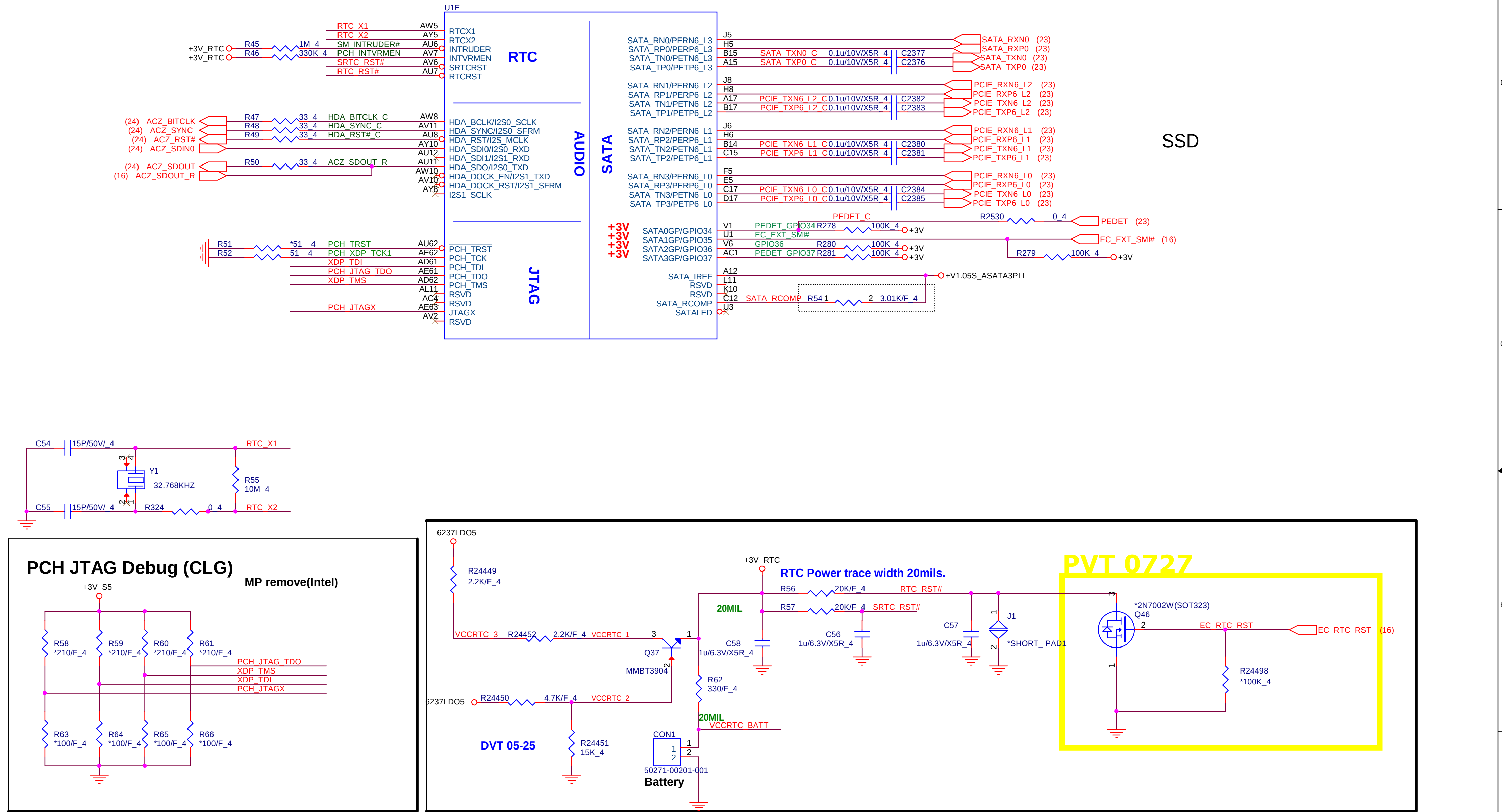
Haswell ULT (RTC, HDA, JTAG, SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R67 *1K_4 SPKR (11,24)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

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Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(RTC/HDA/SATA)	1A
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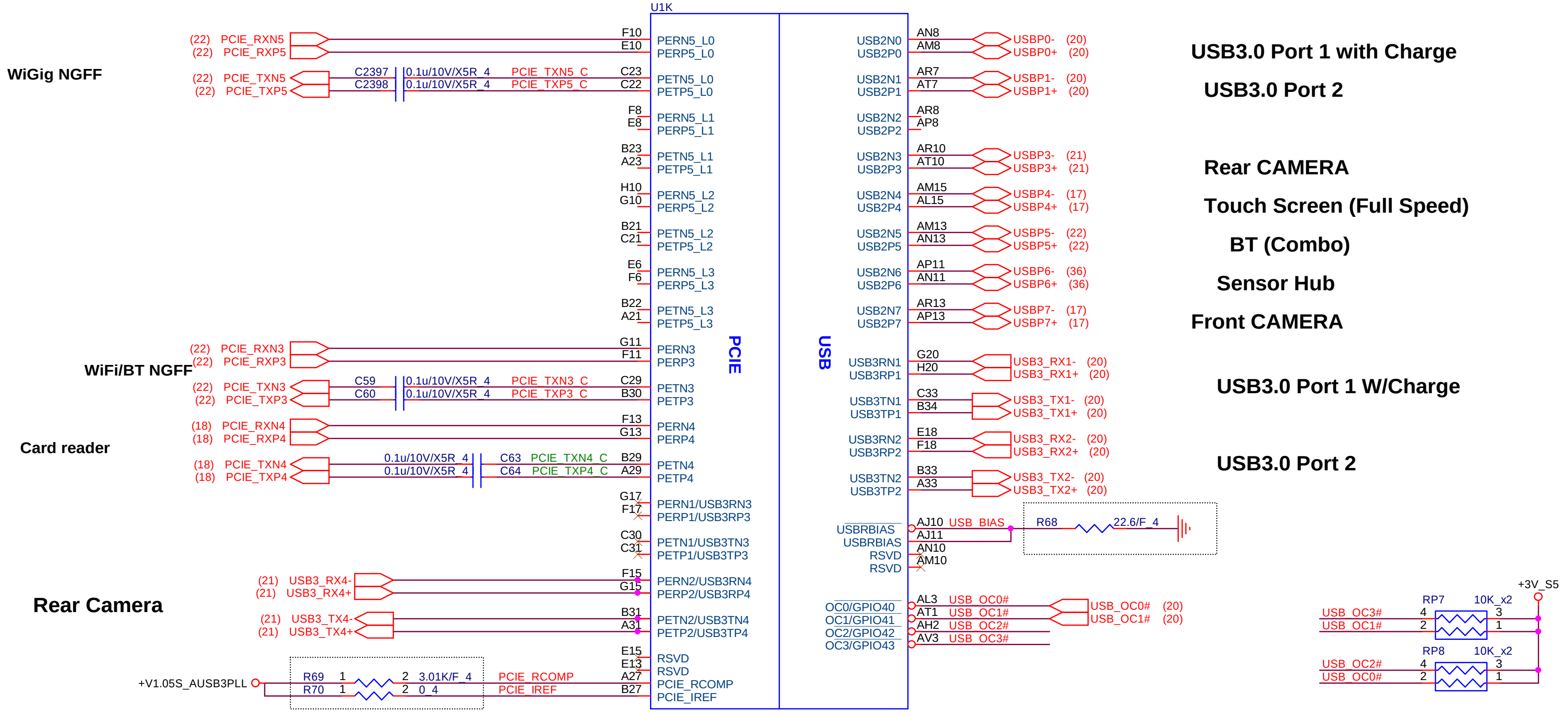
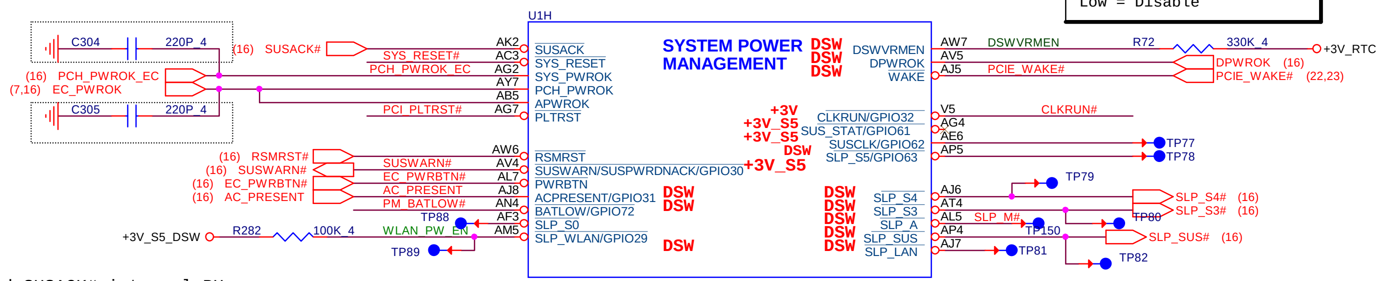
Haswell ULT (PCIE,USB)



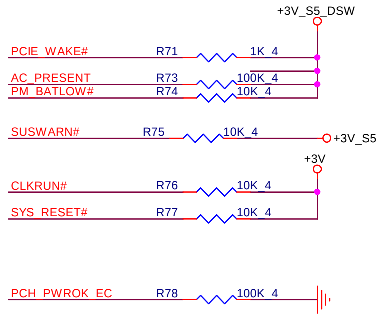
Haswell ULT (SYSTEM POWER MANAGEMENT)

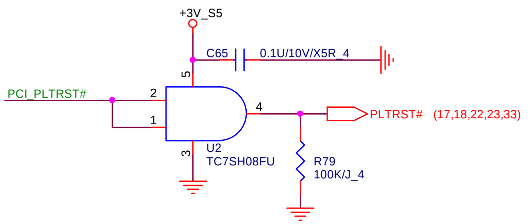
On Die DSW VR Enable
High = Enable (Default)
Low = Disable



PWRBTN# and SUSACK# internal PU

PCH Pull-high/low(CLG)





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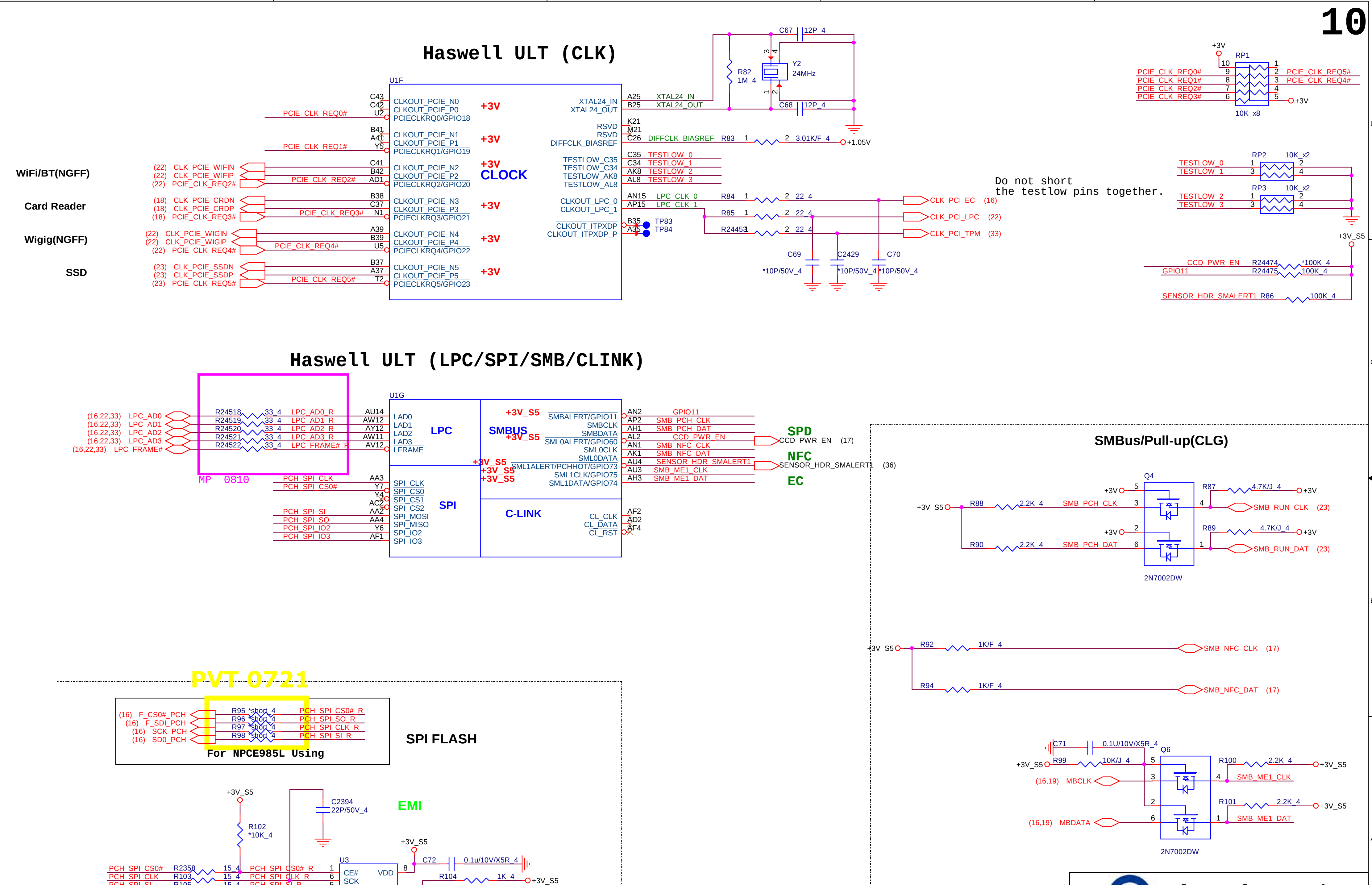

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Quanta Computer Inc.

PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(CLK/LPC/SPI/SMB)	1A
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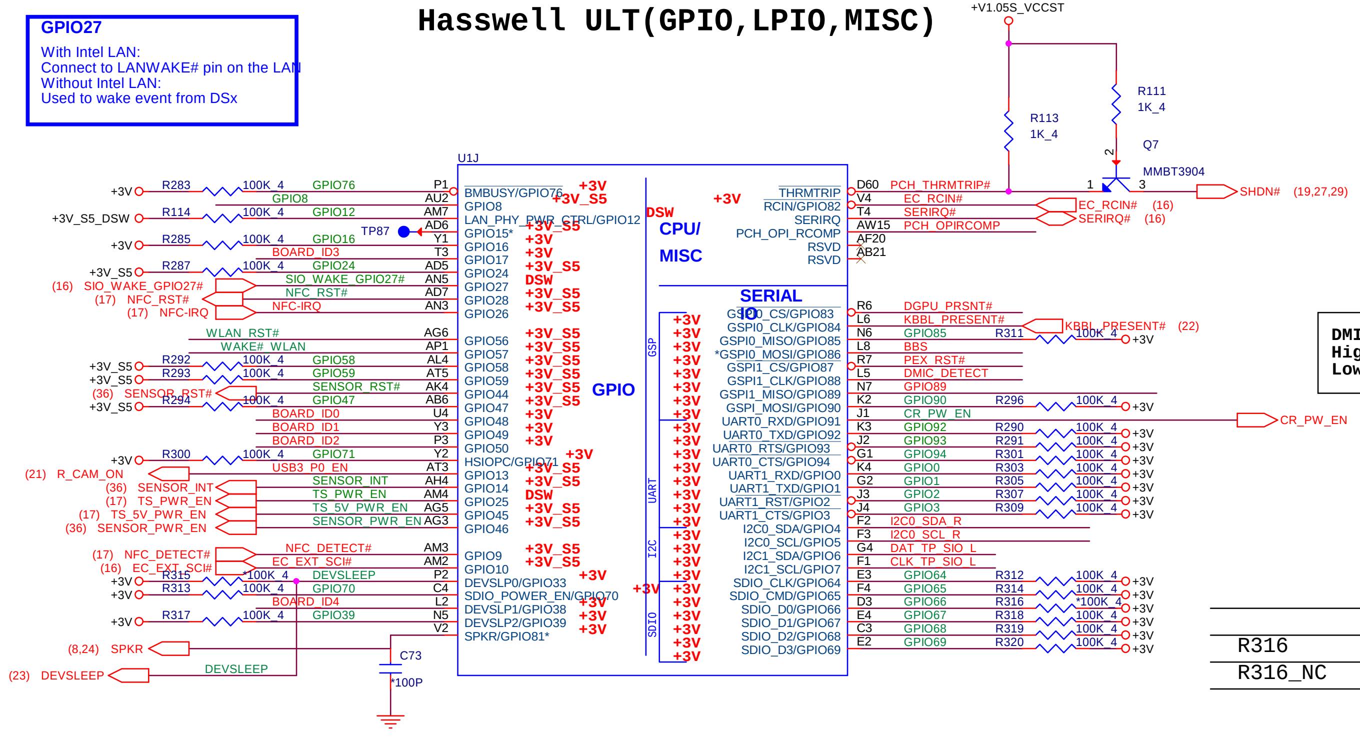
Hasswell ULT(GPIO,LPIO,MISC)

GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

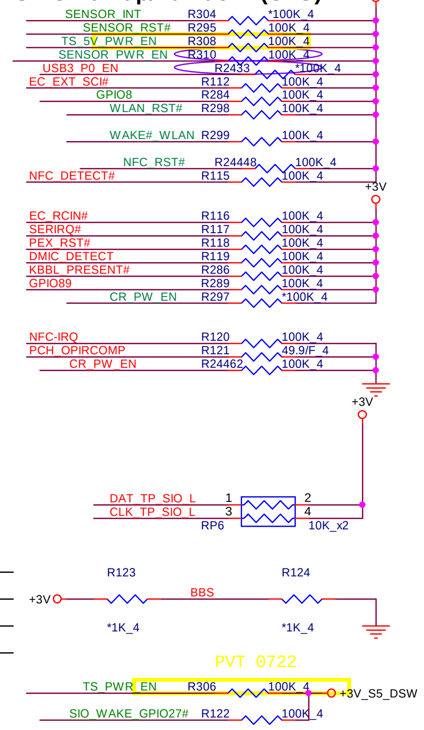


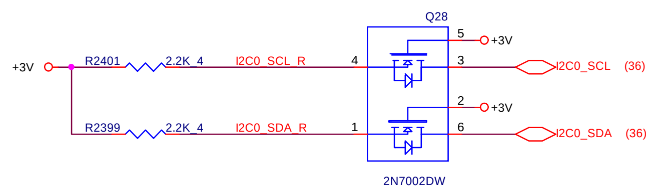
DMIC_DETECT:
High : Single DMIC
Low : Dual DMIC

GPIO66	
R316	ENABLE
R316_NC	DISABLE(Default)

GPIO Pull-up/Pull-down(CLG)

PVT 0722





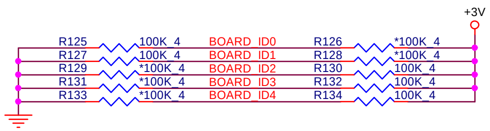
Vendor	Vendor Part Number	BOARD_ID2	BOARD_ID3	BOARD_ID4
Elpida(4G)	EDJ4216EFBG-GN-F	0	0	0
Samsung(4G)	K4B4G1646B-HYK0	0	0	1
Hynix(4G)	H5TC4G63AFR-PBA	0	1	0
Elpida(8G)	EDJ8416E6MB-GN-F	0	1	1
Samsung(8G)	K4B8G1646B-MYK0	1	0	0
Hynix(8G)	H5TC8G63AMR-PBA	1	0	1
		1	1	0
		1	1	1

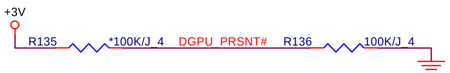
	R127(Low) R128(High) Board ID1	R125(Low) R126(High) Board ID0
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1

GPIO86	
PU	LPC
PD	SPI (Default IPD)

No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN





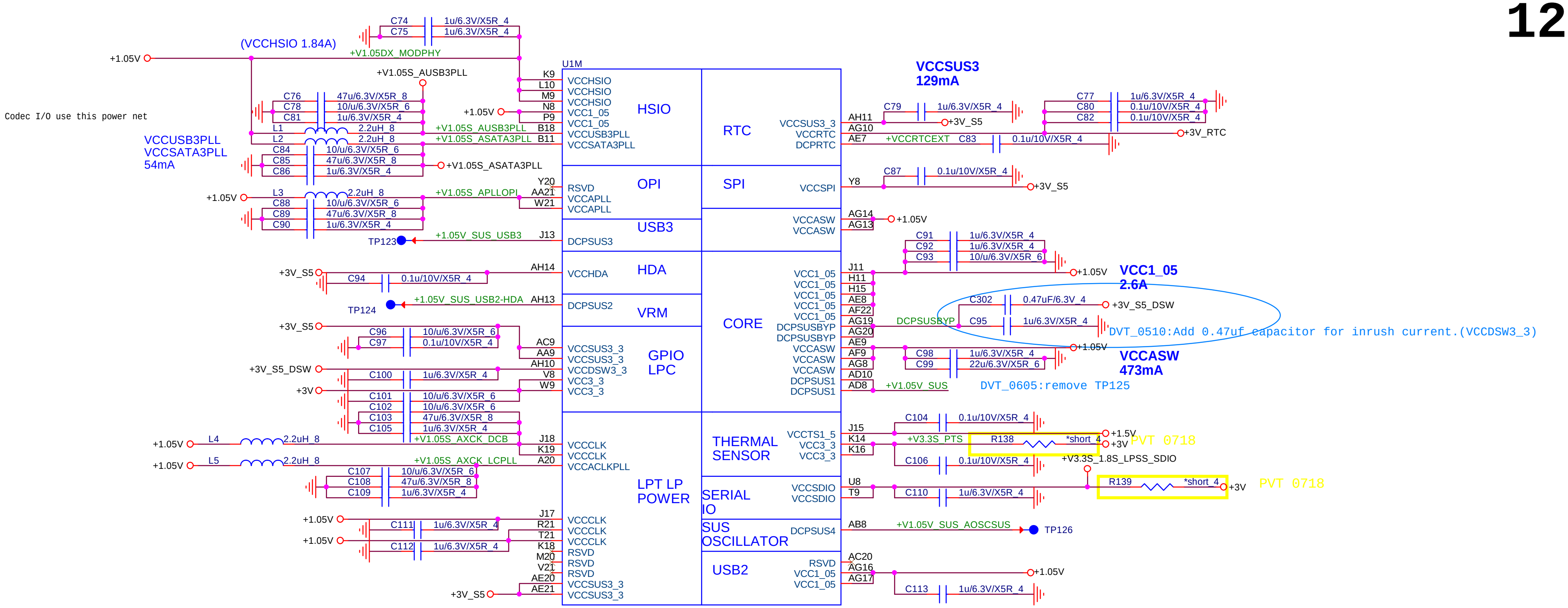
PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

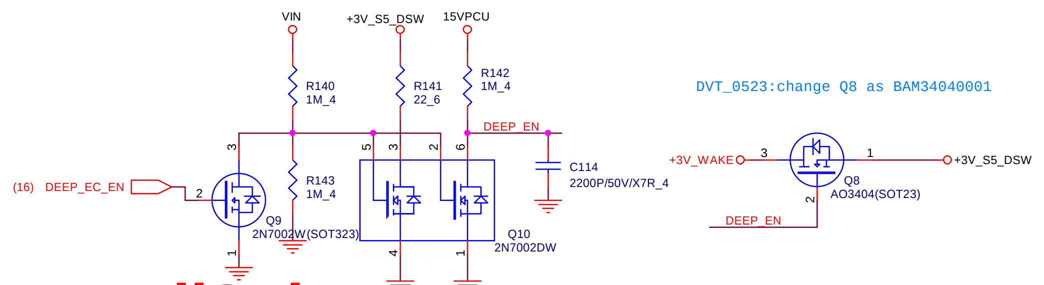
Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(GPIO/MISC)	1A

Date: Monday, August 19, 2013 Sheet 11 of 40



DEEP STANDBY



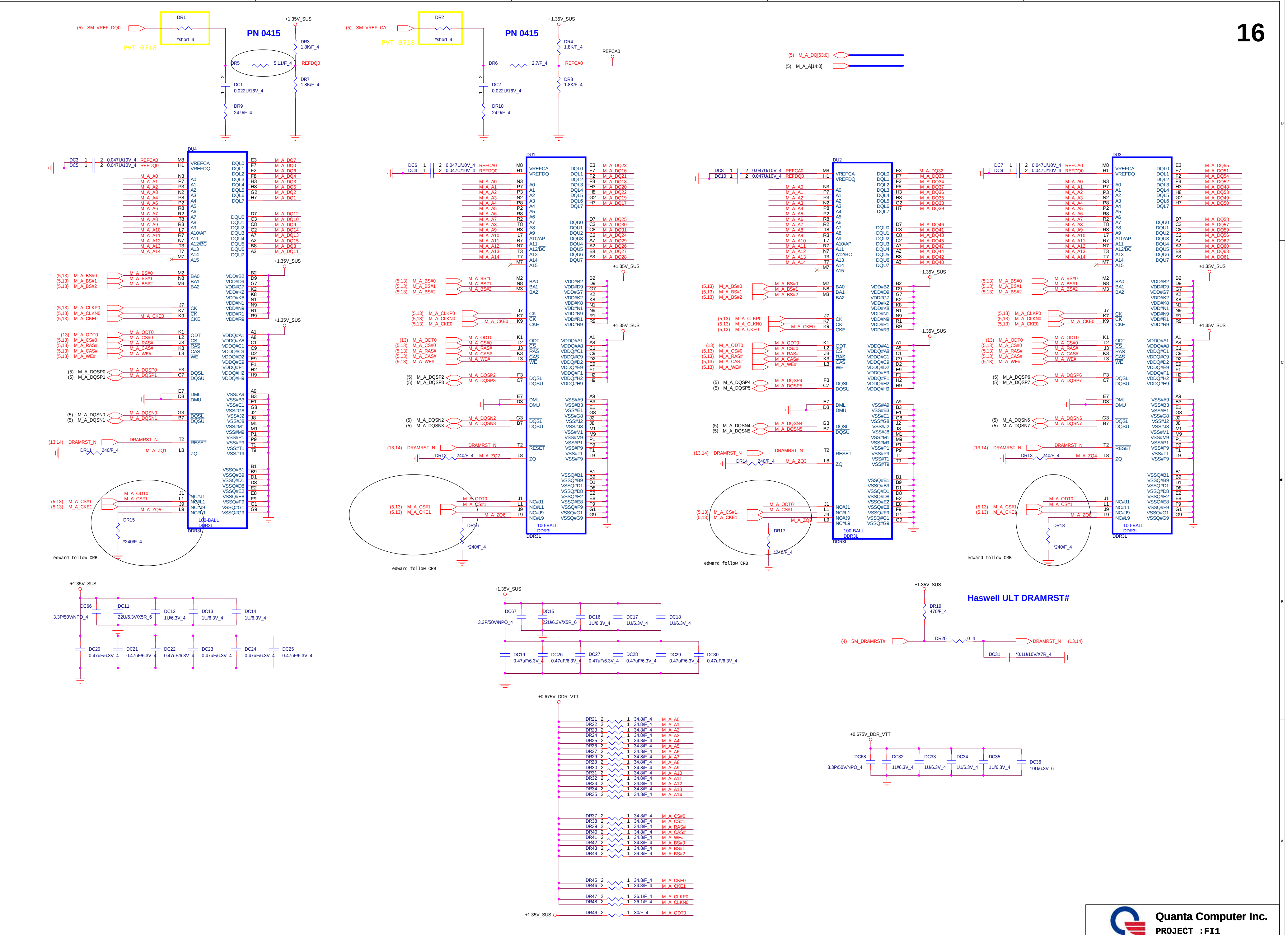
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(Power)	1A

Date: Monday, August 19, 2013 | Sheet 12 of 40

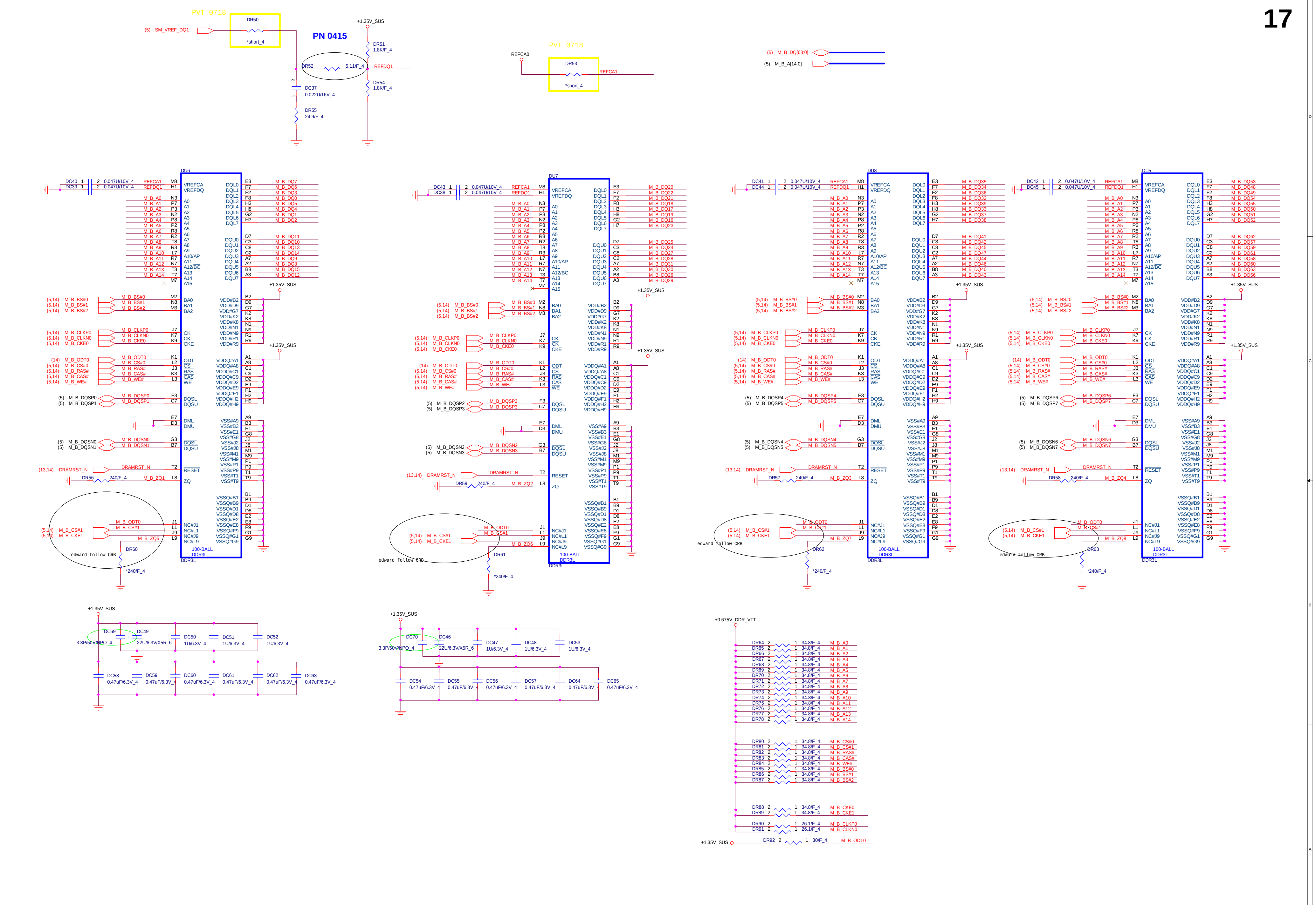


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

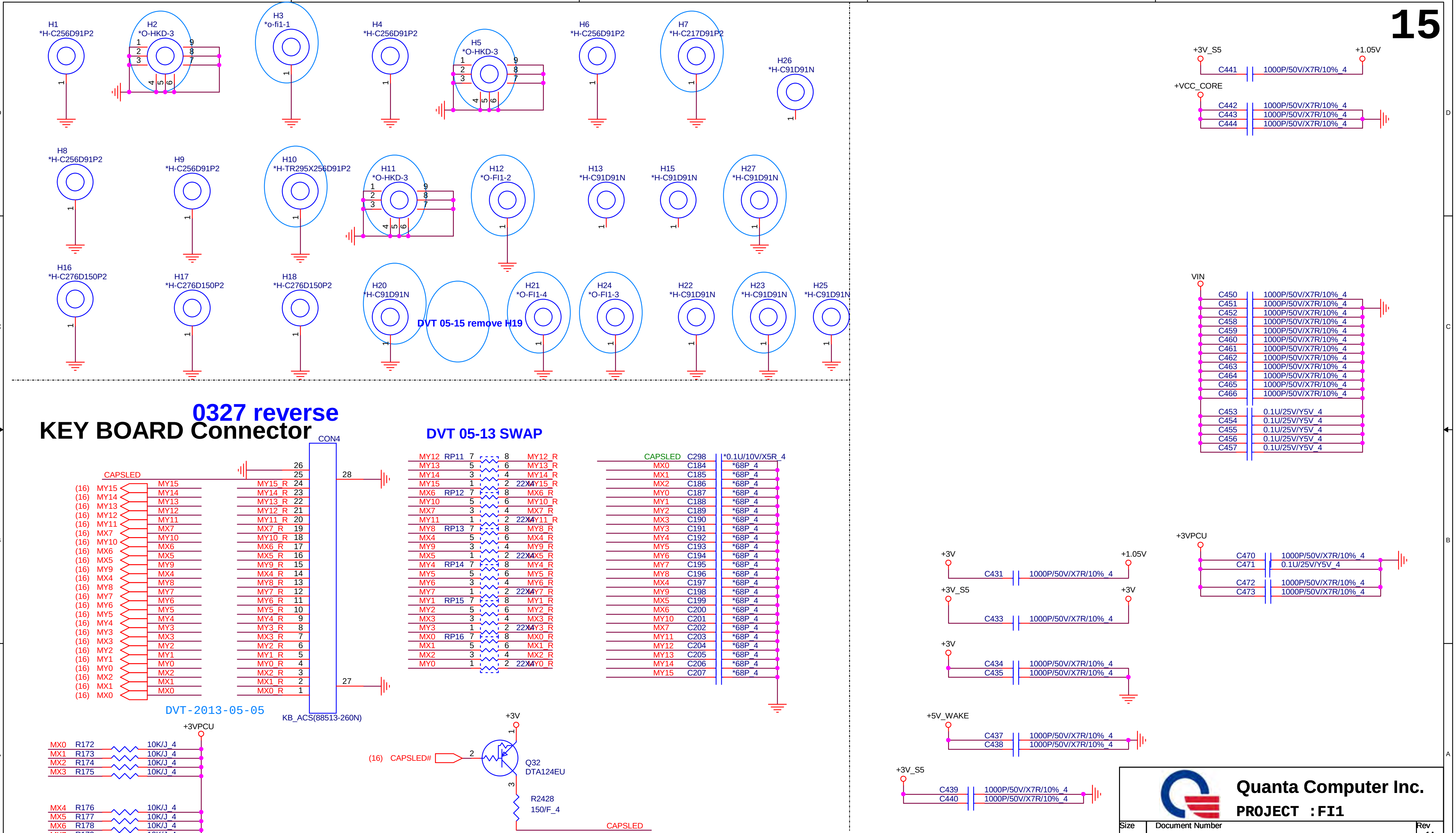
Size	Document Number	Rev
	DDR3L MEMORY_x16(CH-A)	1A

Date: Monday, August 19, 2013 Sheet 13 of 40



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT :FI1		
Size	Document Number: DDR3L MEMORY_x16(CH-B)	Rev: 1A
Date: Monday, August 19, 2013	Sheet 14 of 40	



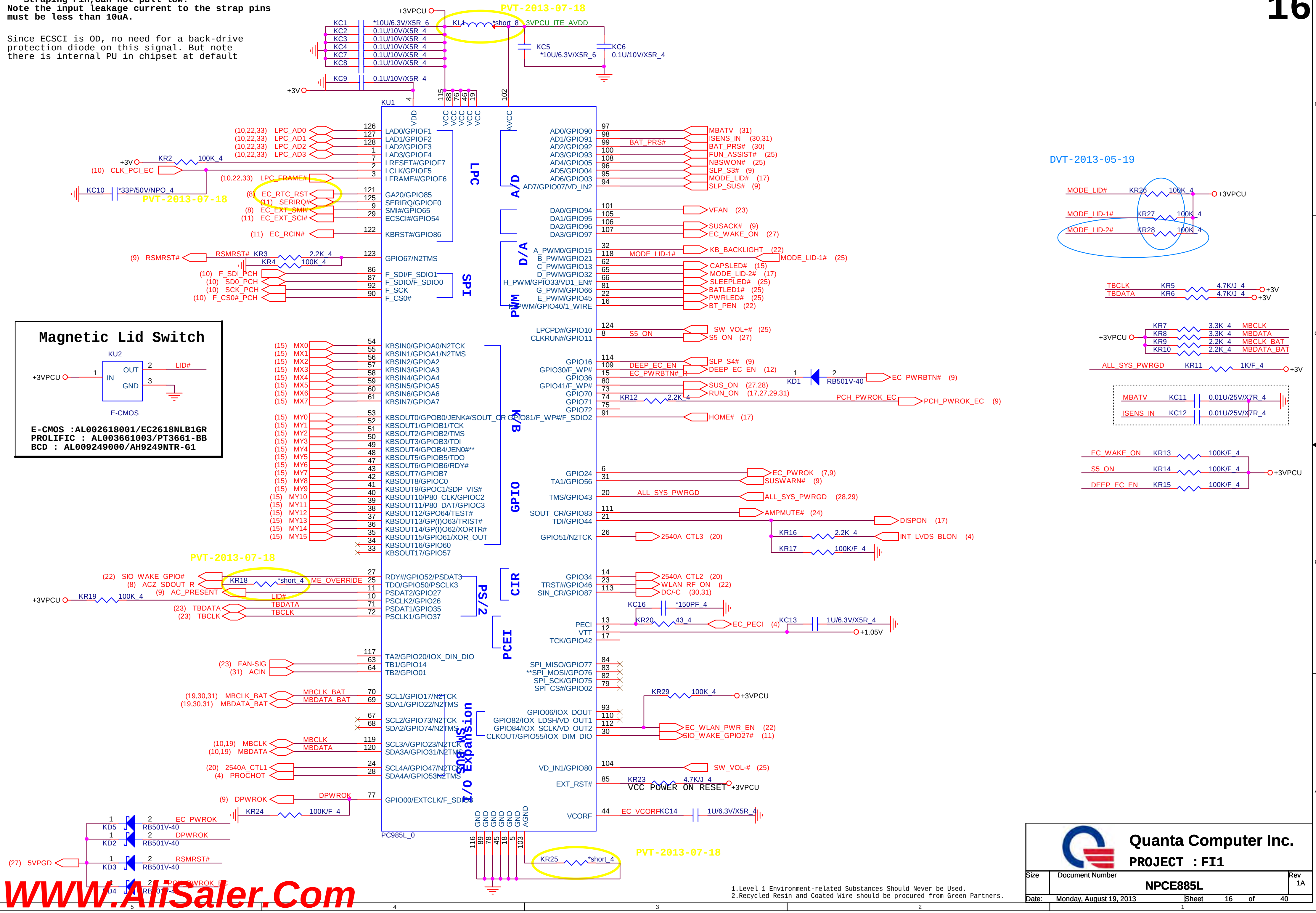
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT :FI1		
Size	Document Number: HOLE/EMI/KB	Rev: 1A
Date: Monday, August 19, 2013	Sheet 15 of 40	

New ADD

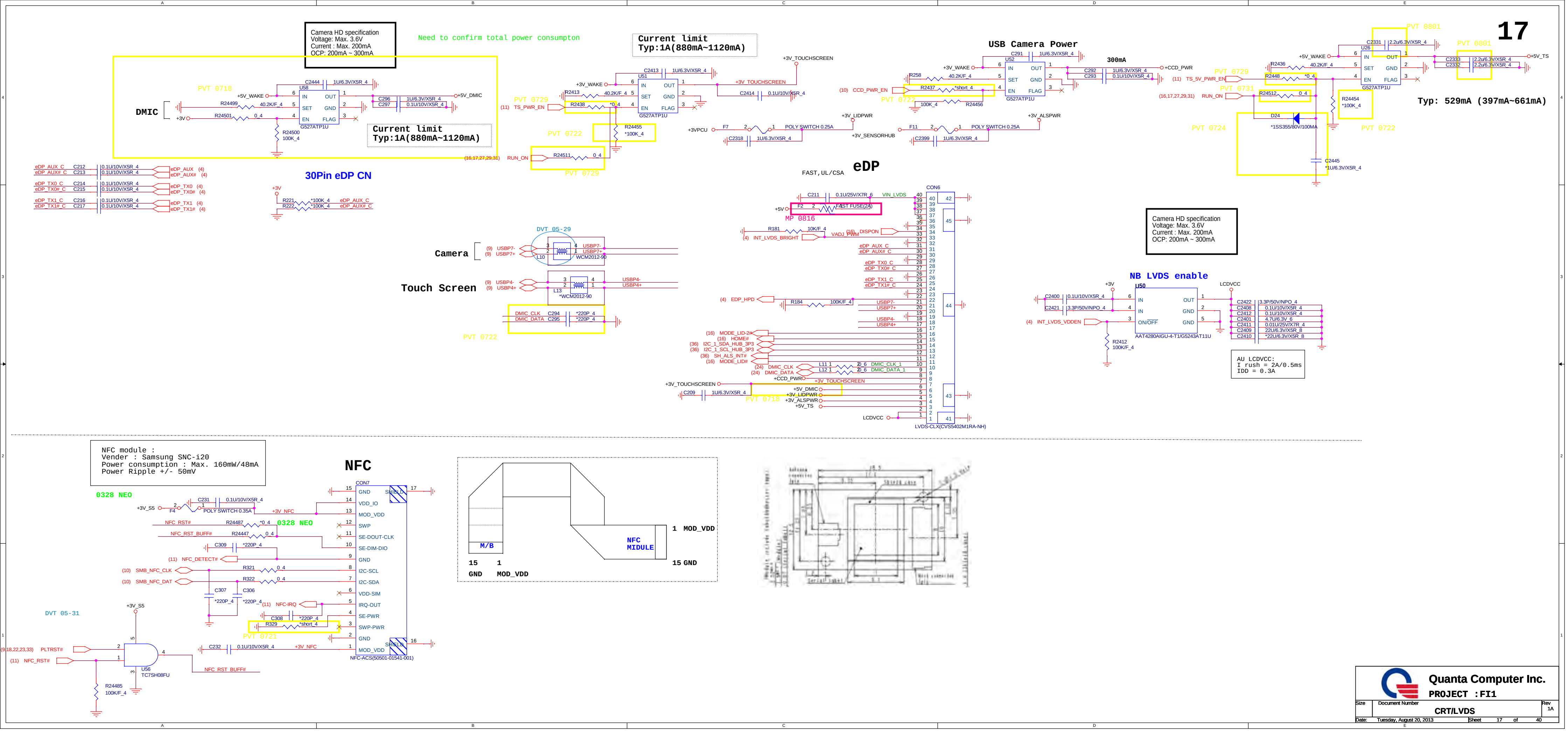
** Straping Pin,Can not pull low.
Note the input leakage current to the strap pins
must be less than 10uA.

Since ECSCI is OD, no need for a back-drive
protection diode on this signal. But note
there is internal PU in chipset at default

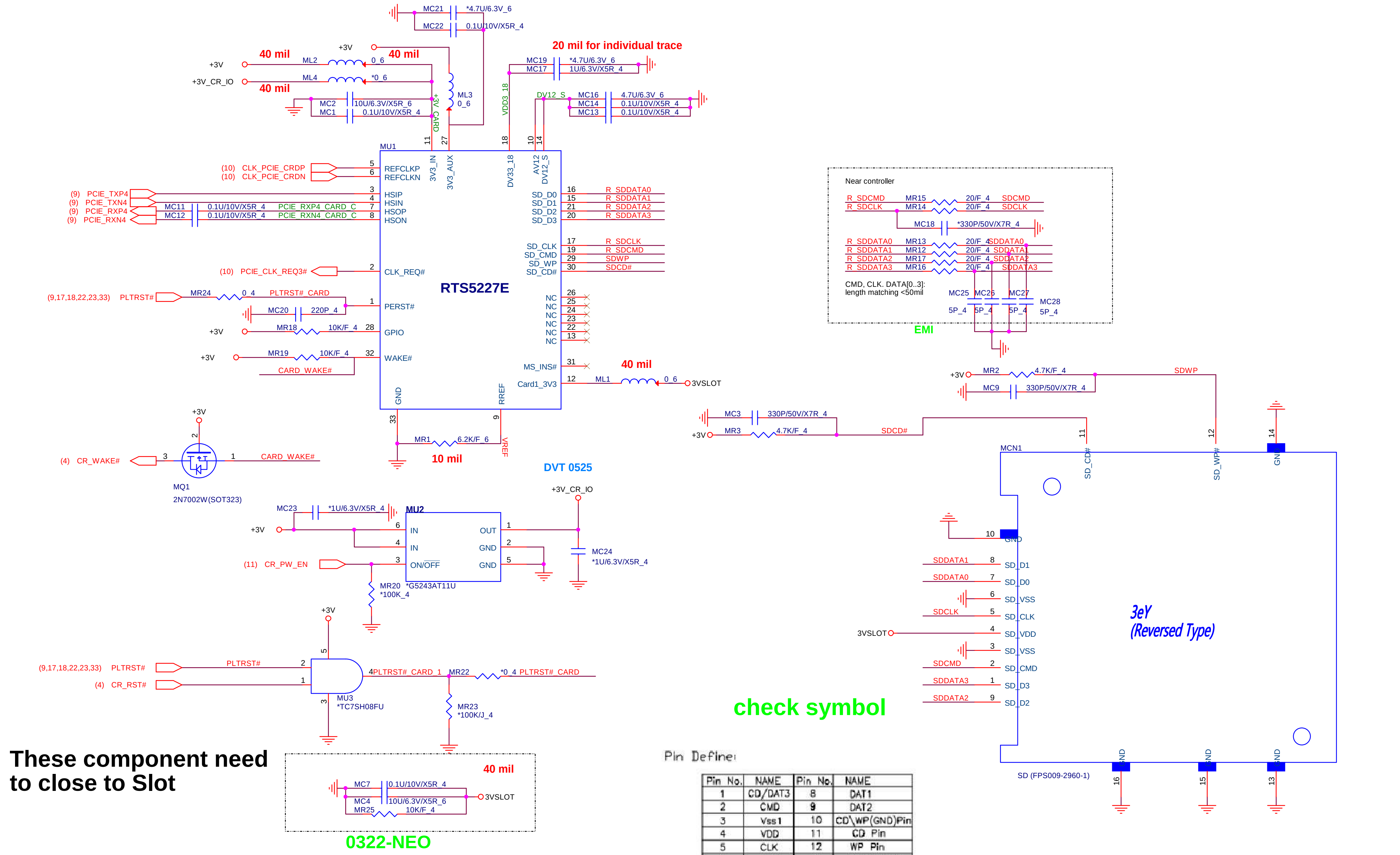


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI1		
Size	Document Number: NPCE885L	Rev: 1A
Date: Monday, August 19, 2013	Sheet 16 of 40	



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



Pin Define:

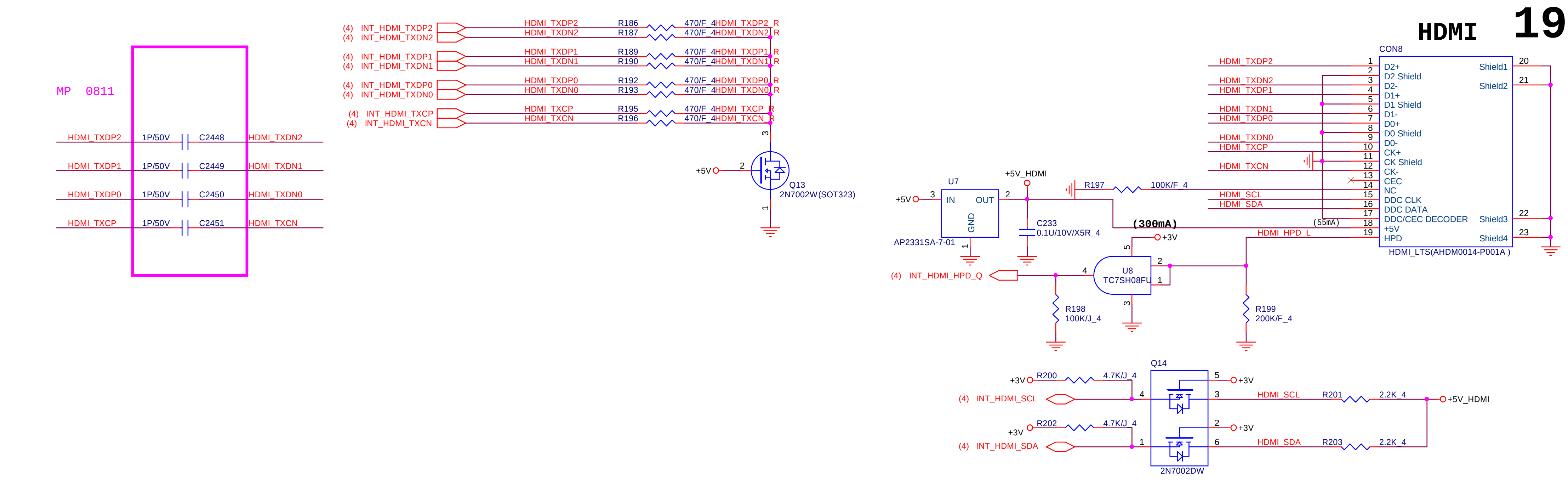
Pin No.	NAME	Pin No.	NAME
1	CD/DAT3	8	DAT1
2	CMD	9	DAT2
3	Vss1	10	CD\WP(GND)Pin
4	VDD	11	CD Pin
5	CLK	12	WP Pin
6	Vss2	13	GND(Shell)
7	DAT0	14	GND(Shell)
		15	GND(Shell)
		16	GND(Shell)

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

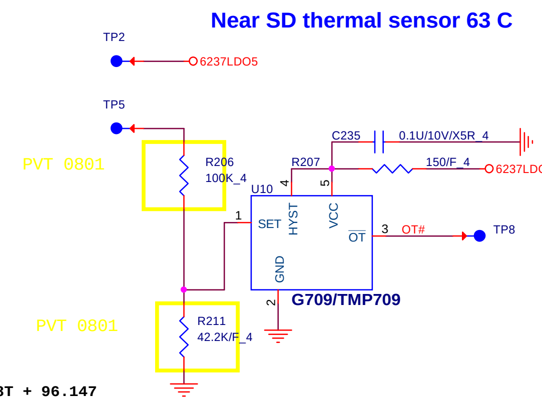
Quanta Computer Inc.

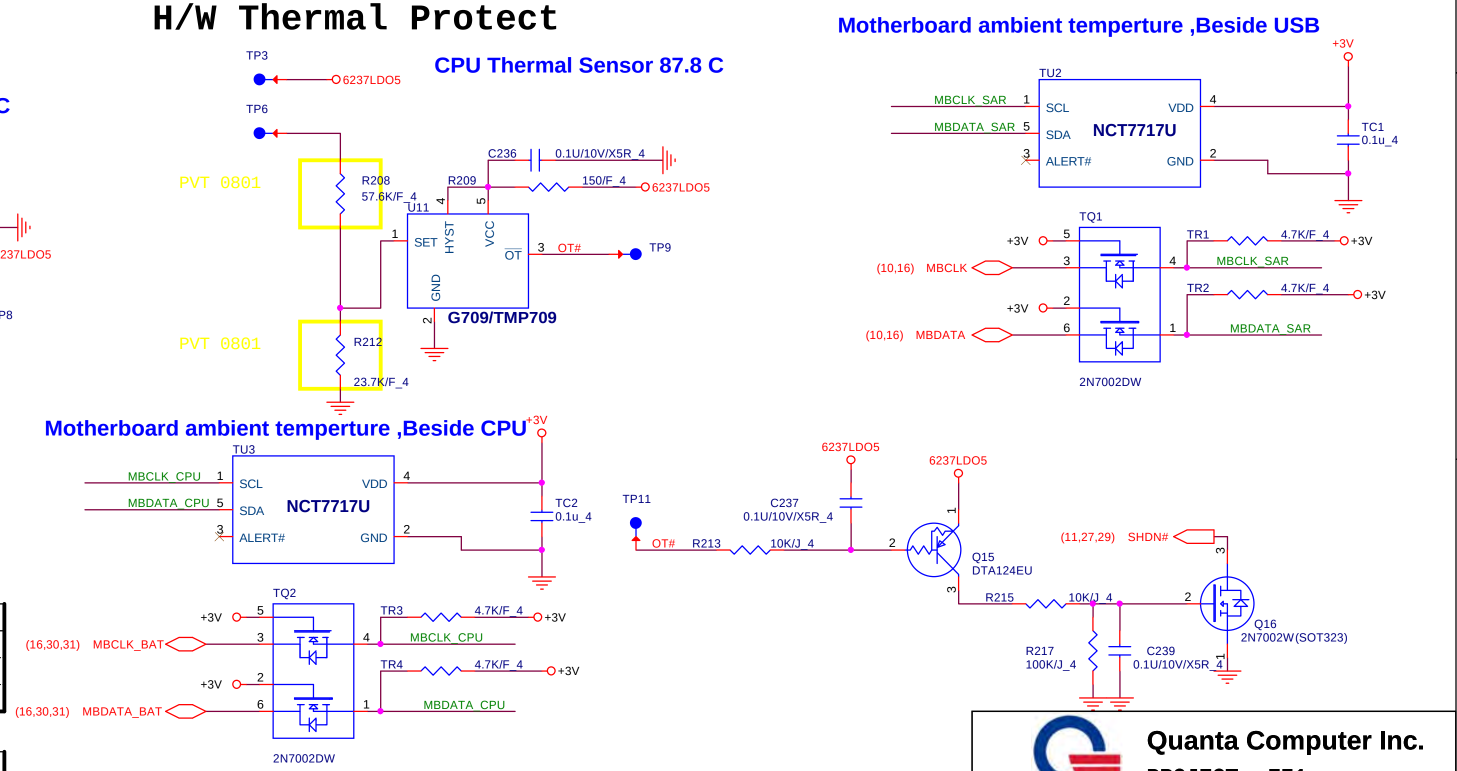
PROJECT : FI1

Size	Document Number	Rev
	CARD	1A
Date: Monday, August 19, 2013	Sheet 18 of 40	



H/W Thermal Protect





RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

95	18.5K
100	15K
107	10.3K
110	8.2K

DIS SKU

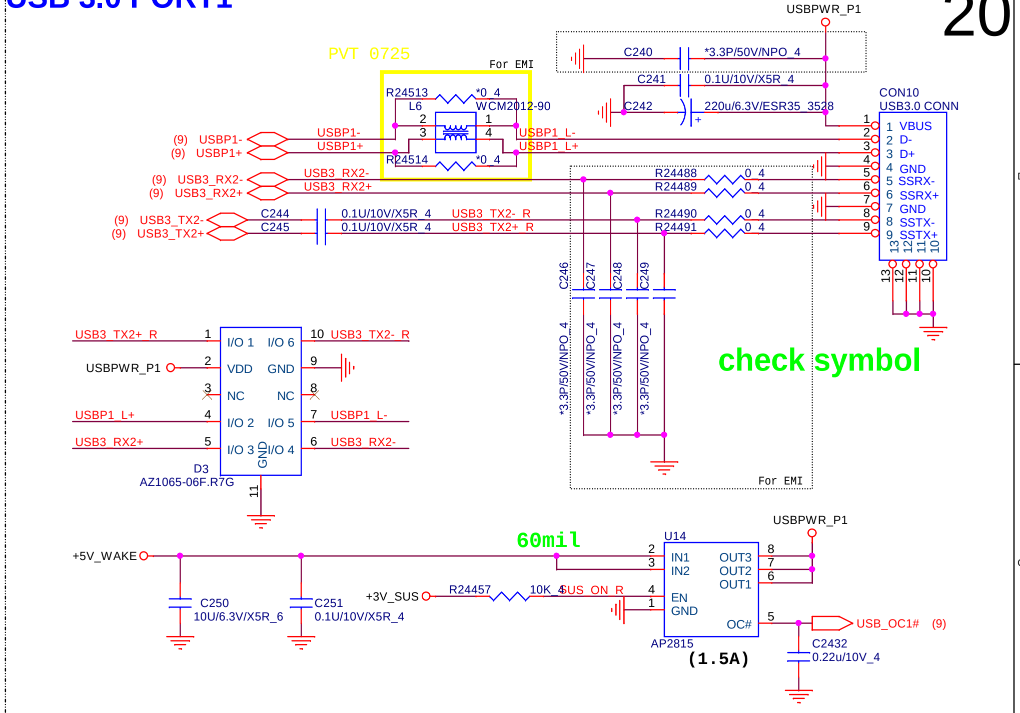
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	70	R208=36.87K	36.5K	71	70
Near GFX sensor temp	65	R146=40.72K	40.2K	66.3	65.1
Near AUDIO sensor temp	60	R345=44.62K	44.2K	61.2	60

UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	81	R208=28.63K	28K	82.3	81.4
Near AUDIO sensor temp	58	R345=46.2K	46.4K	58.4	57.1

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

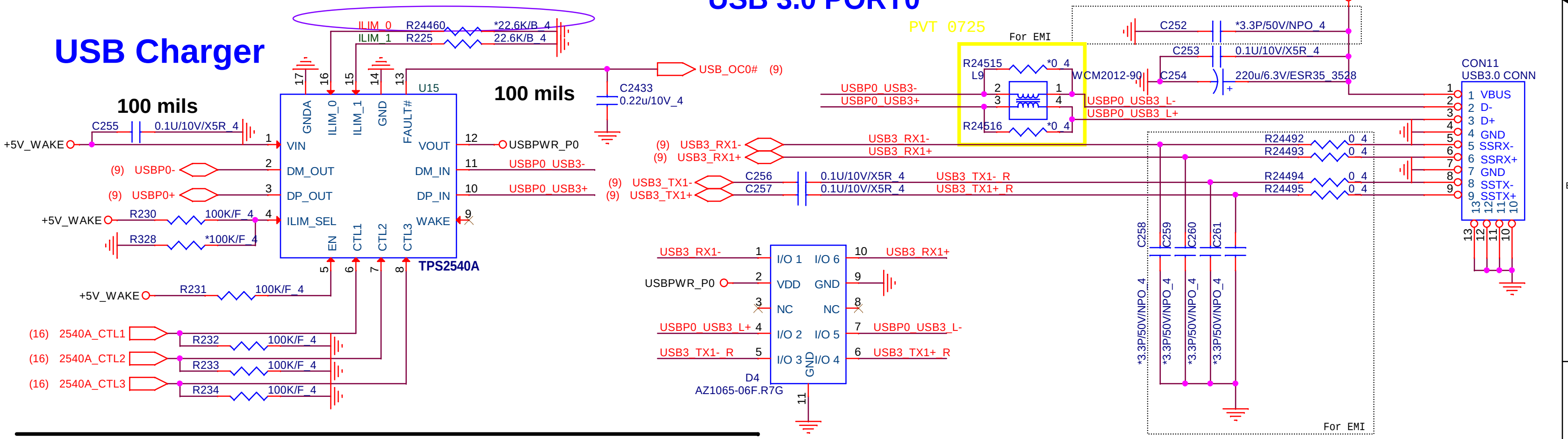
USB 3.0 PORT1



DVT-2013-05-05 : Symbol reserve for TPS2543

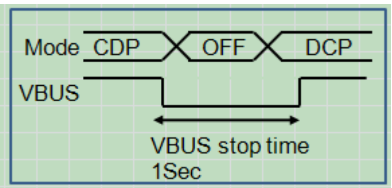
USB Charger

USB 3.0 PORT0



	TPS2540A		TPS2543	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

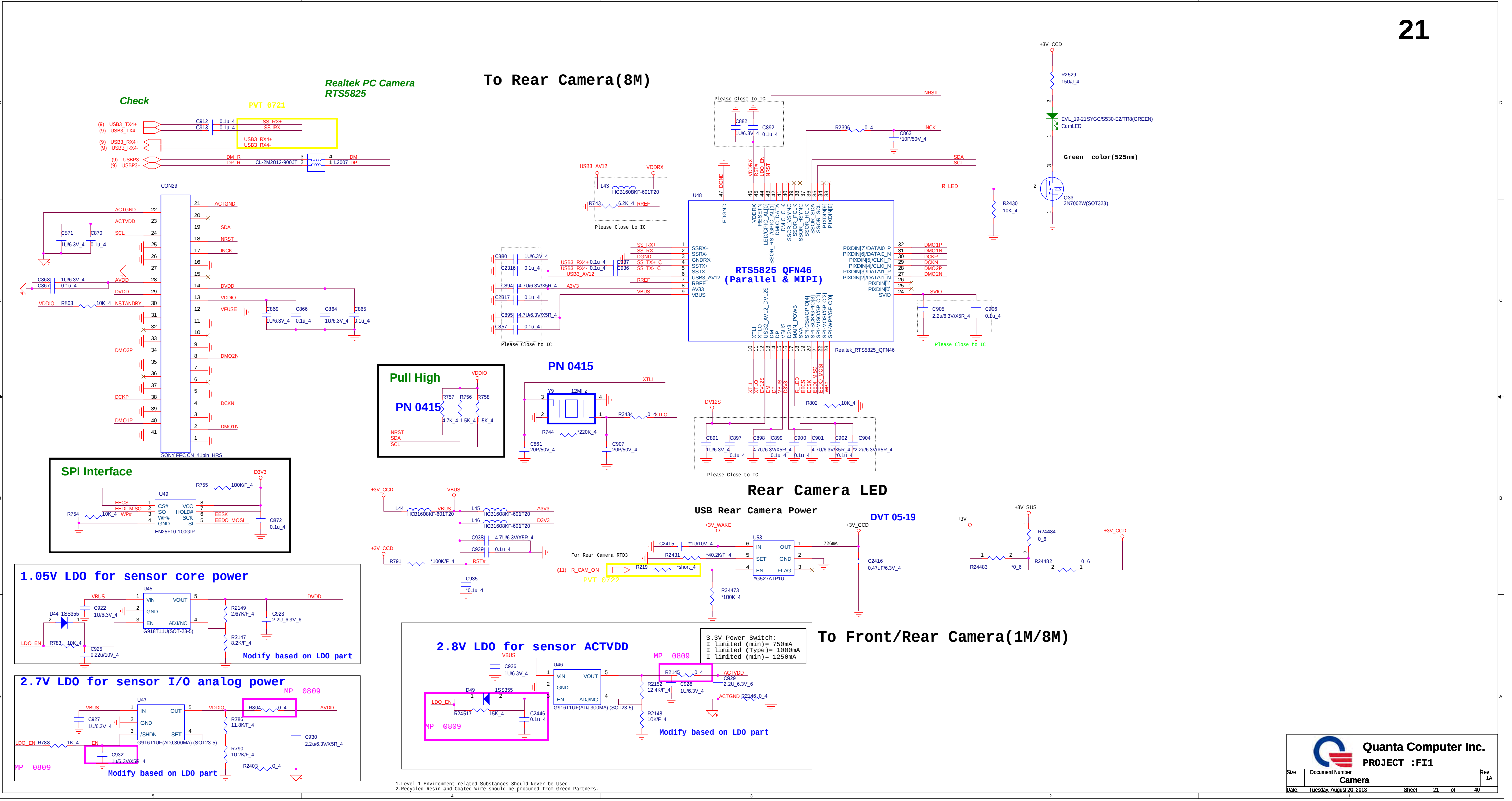


CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	SDP (S0, 0.5A)

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

ILIM_SEL	(I LIMIT(A)= 48000/R)
HI	I_LIM_1
LO	I_LIM_0
	48000/22.6K=2.123A

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



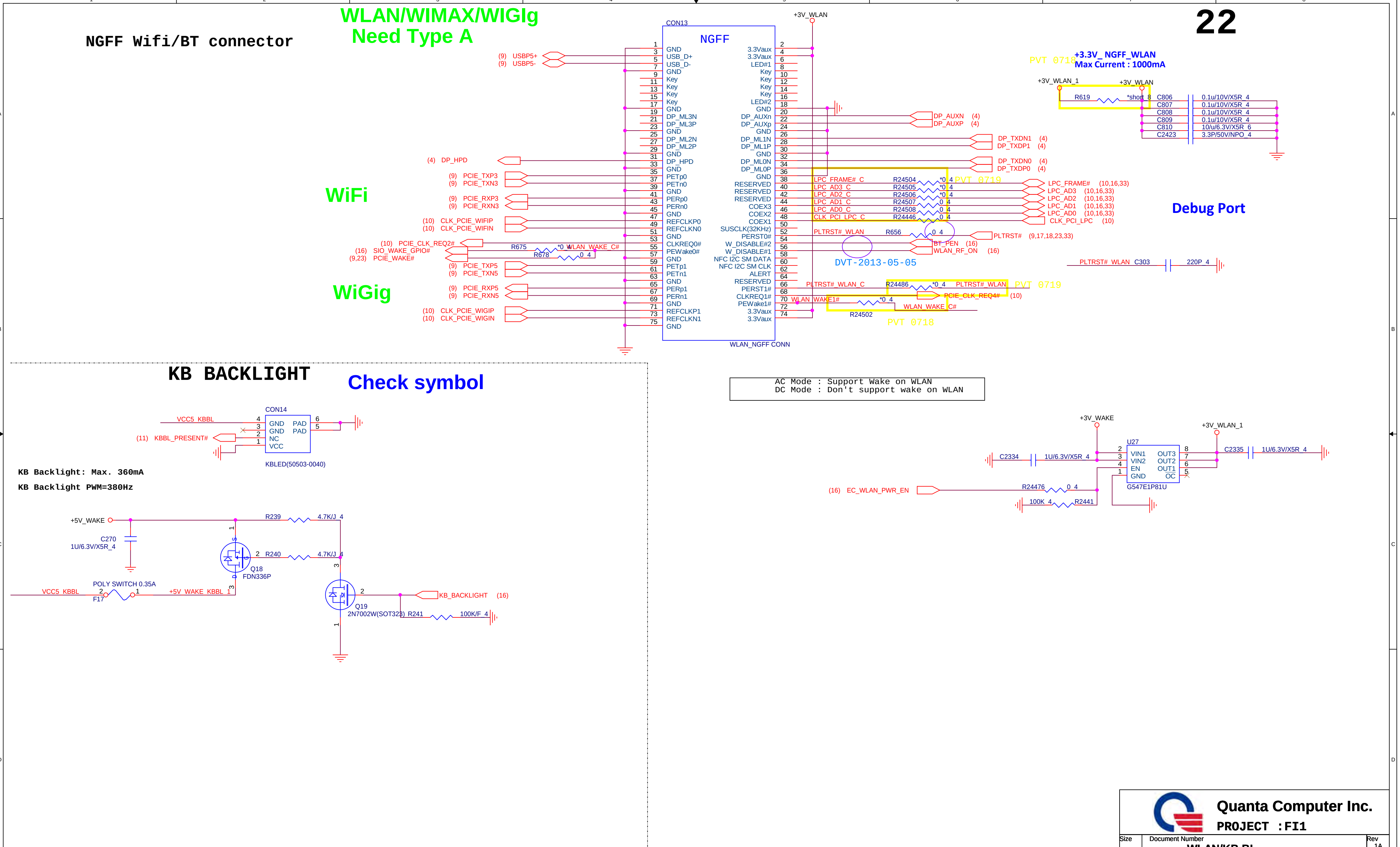
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT :FI1

Size	Document Number	Rev
	Camera	1A

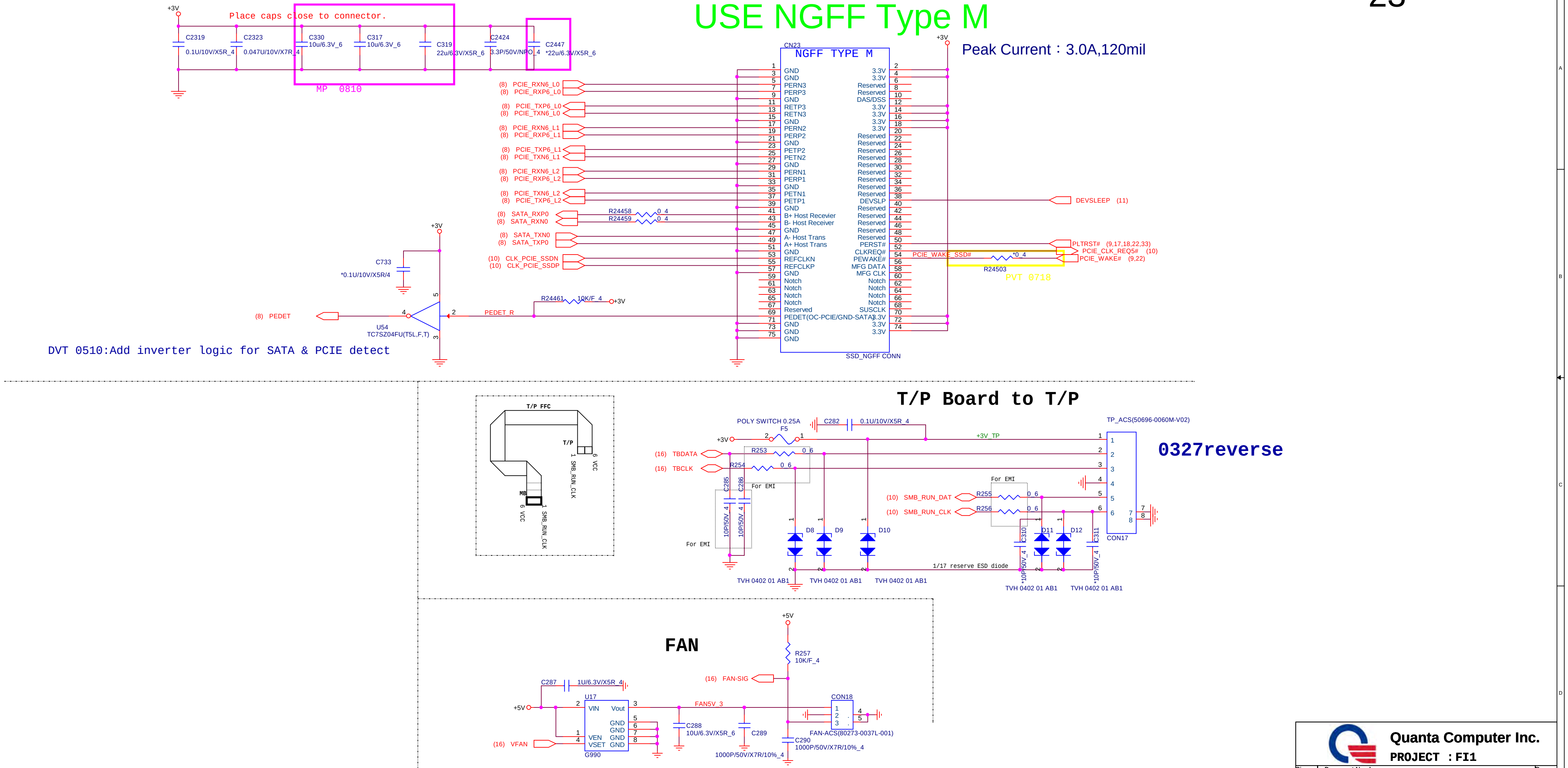
Date: Tuesday, August 20, 2013 Sheet 21 of 40



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI1		
Size	Document Number: WLAN/KB BL	Rev 1A
Date: Monday, August 19, 2013	Sheet 22 of 40	

USE NGFF Type M



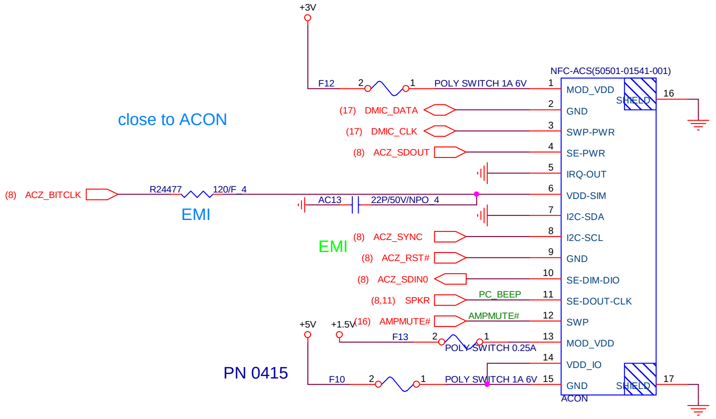
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT : FI1

Size	Document Number	Rev
	HDD/ODD/TP/FAN	1A

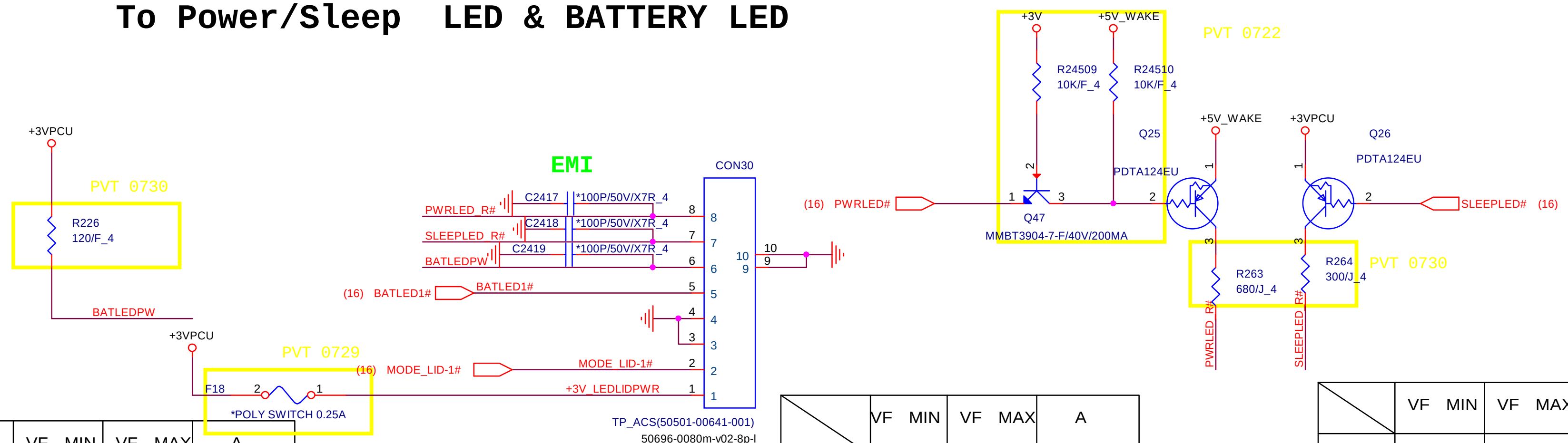
Date: Monday, August 19, 2013 Sheet 23 of 40



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.	PROJECT : FI1	
Size	Document Number: Audio Codec ALC233-CG	Rev 1A
Date: Monday, August 19, 2013	Sheet 24 of 40	

To Power/Sleep LED & BATTERY LED



	VF MIN	VF MAX	A
Umber LED	1.75V	2.35V	7.27mA / 4.09 mA

(3.3 - 1.75)V /120 Ω = 12.9 mA
(3.3 - 2.35)V / 120Ω =7.92 mA

	VF MIN	VF MAX	A
Pure green LED	2.7V	3.7V	4.89mA / 2.76 mA

(5- 2.7)V / 680 Ω =3.38 mA
(5 - 3.7)V / 680Ω = 1.91 mA

	VF MIN	VF MAX	A
Umber LED	1.7V	2.4V	7.27mA / 4.09 mA

(3.3 - 1.7)V /300 Ω = 5.3 mA
(3.3 - 2.4)V / 300Ω =3mA

Power & Assist SW

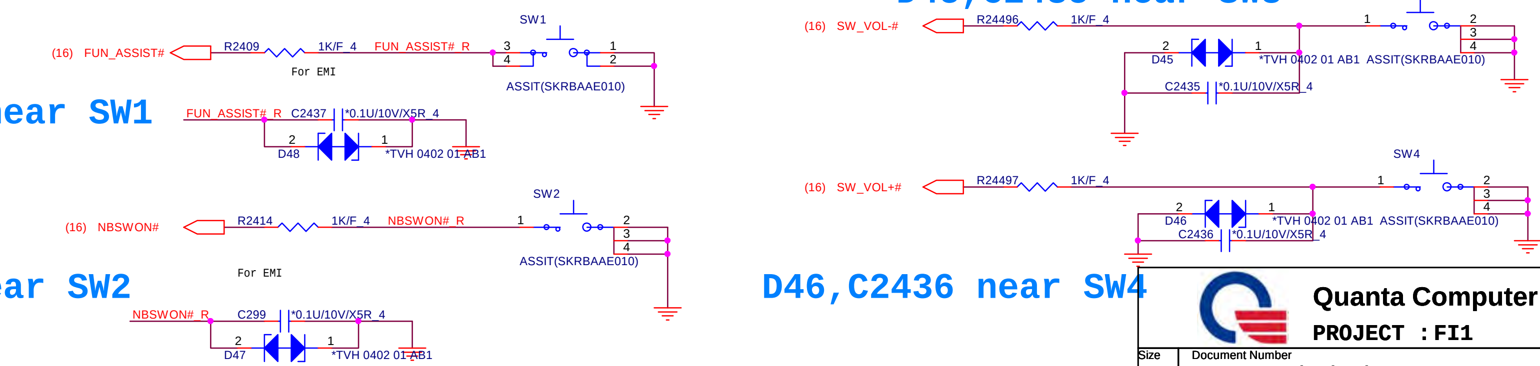
Follow FI3

D45,C2435 near SW3

D48,C2437 near SW1

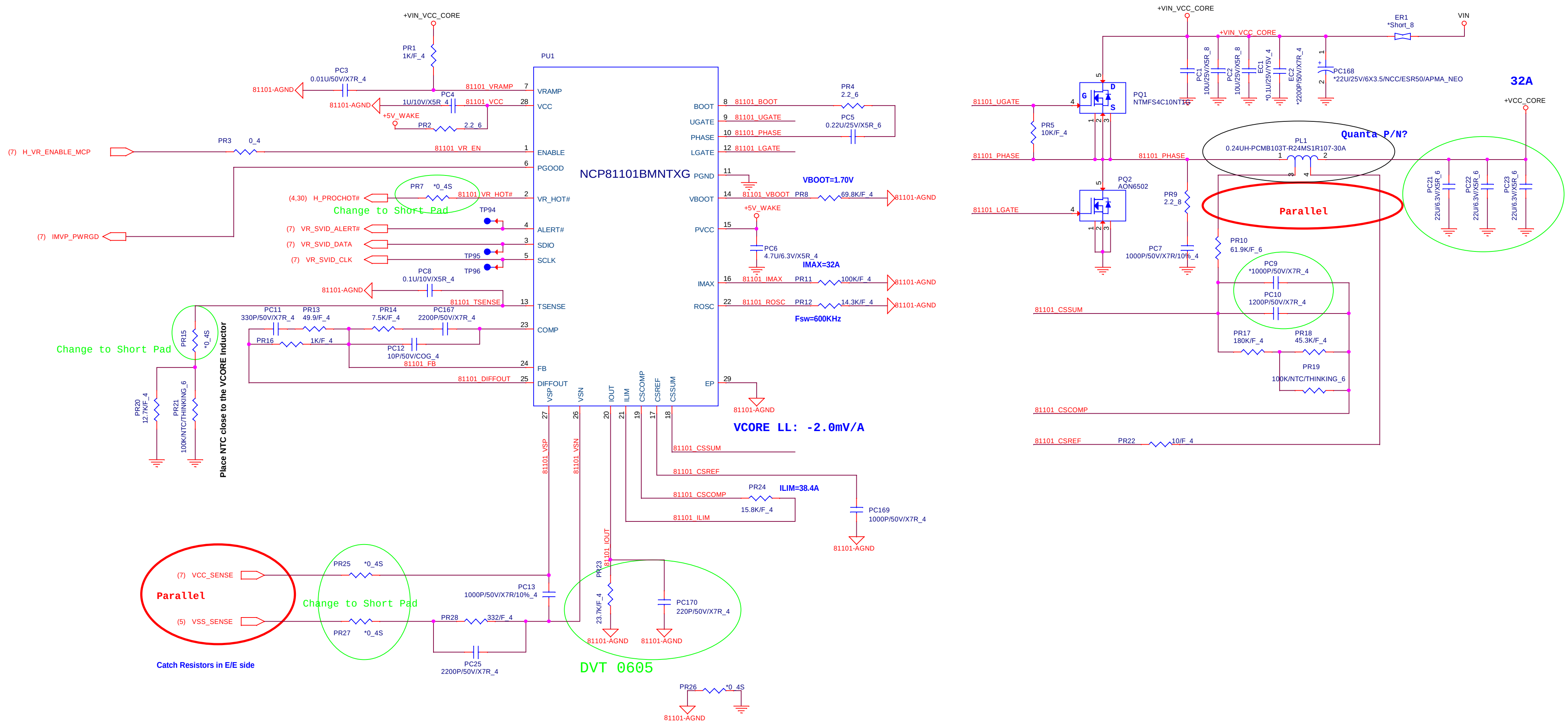
D47,C299 near SW2

D46,C2436 near SW4



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI1		
Size	Document Number: LED/RF/KB/PS	Rev 1A
Date: Monday, August 19, 2013	Sheet 25 of 40	



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT : FI1

Size	Document Number	Rev
	+VCC_CORE (NCP81101)	PVT

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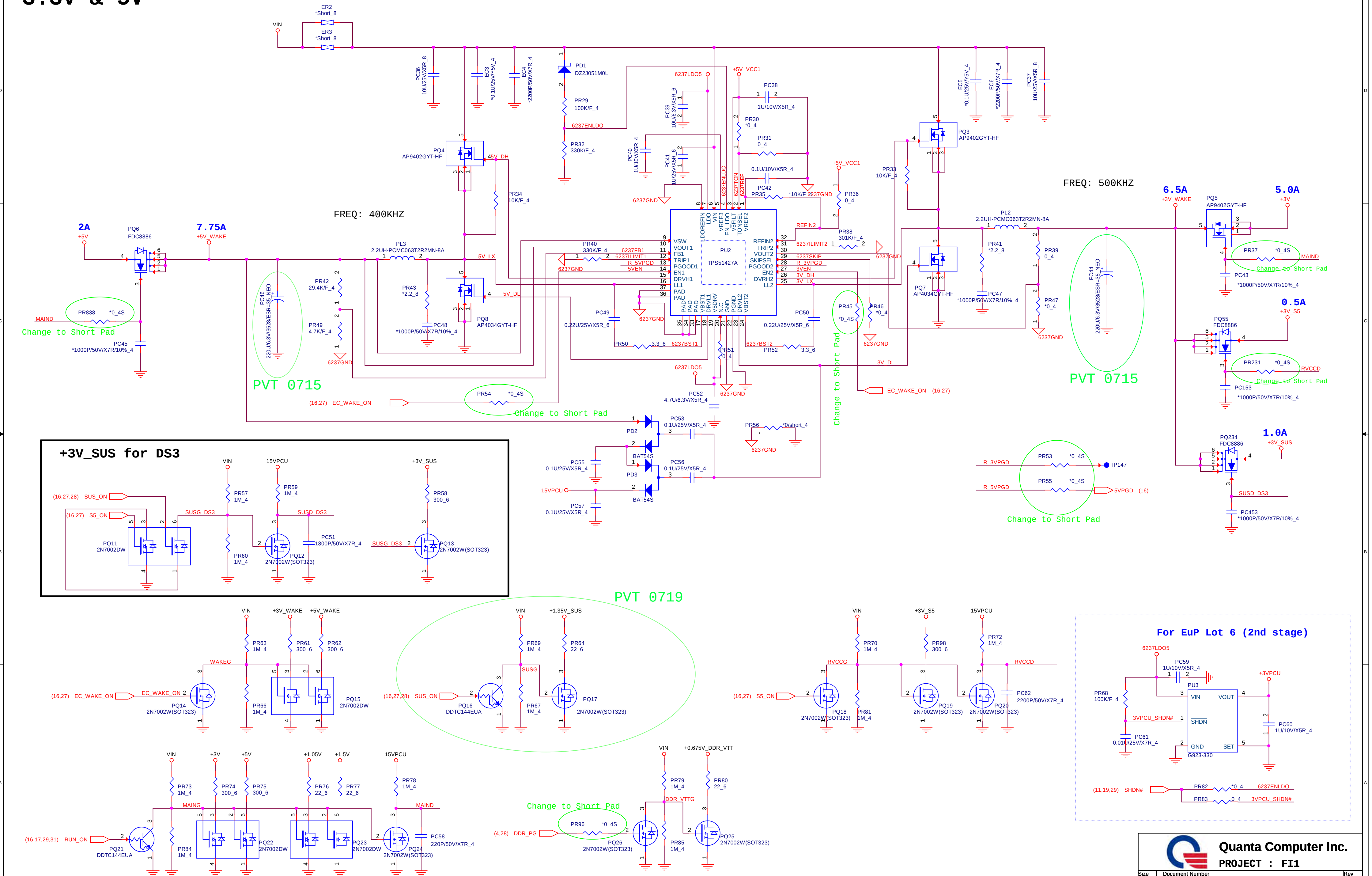
3.3V & 5V



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.	PROJECT : FI1
Size / Document Number	3VPCU&5VPCU(TPS51427A)
Rev	PVT
Date:	Monday, August 19, 2013
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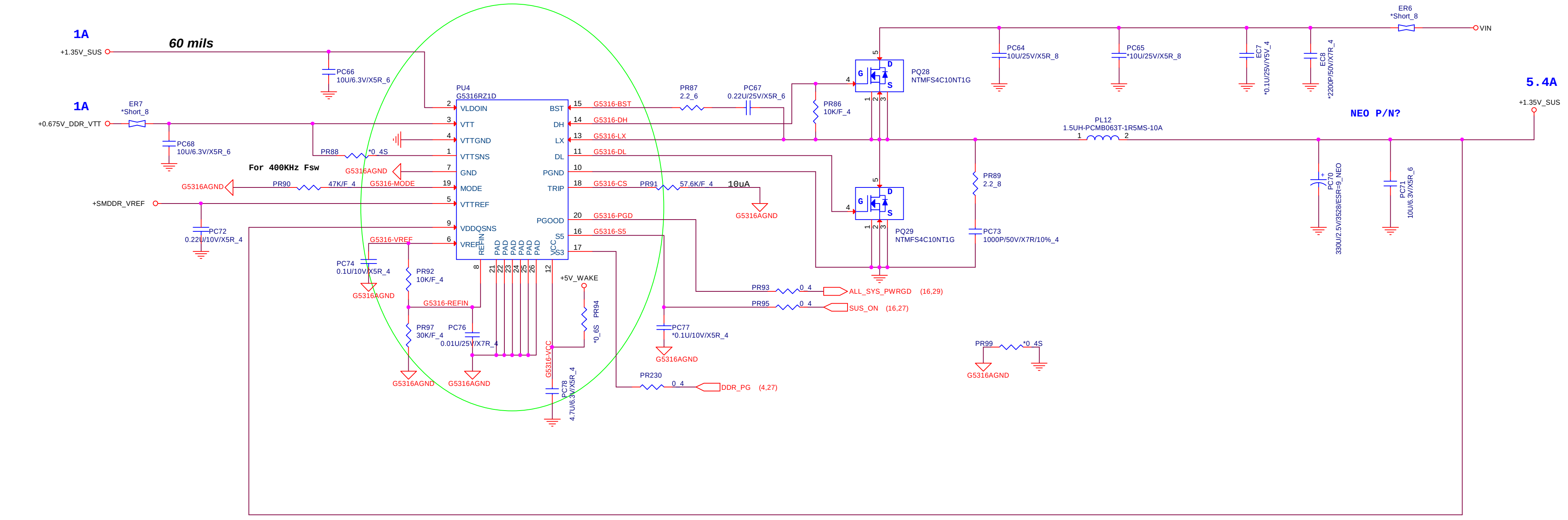
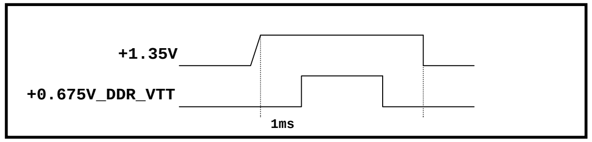
1.35VSUS & VTT_MEM



MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



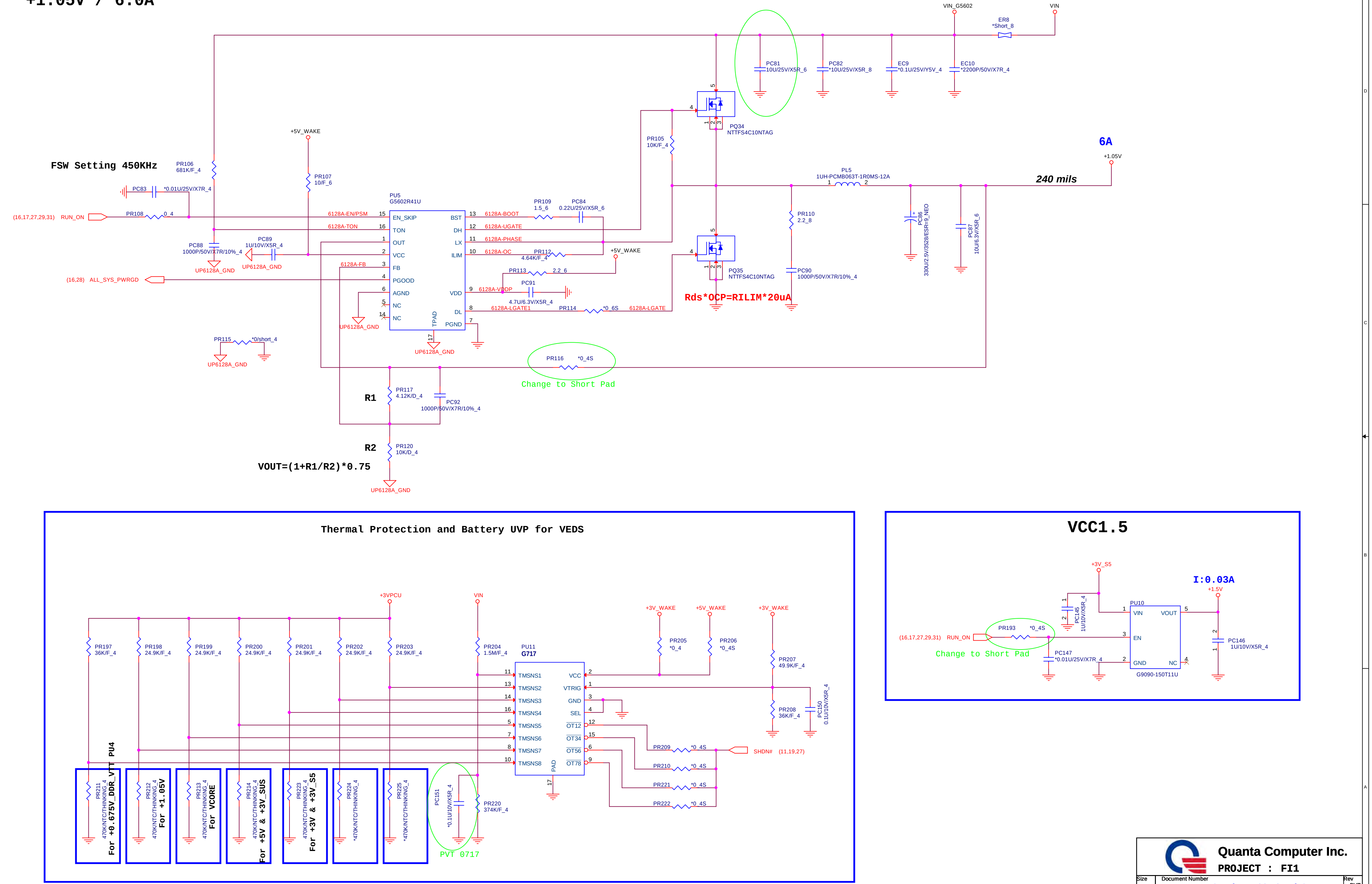
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size | Document Number: 1.5VSUS/VTT_MEM | Rev: PVT

Date: Monday, August 19, 2013 | Sheet 28 of 40

+1.05V / 6.0A



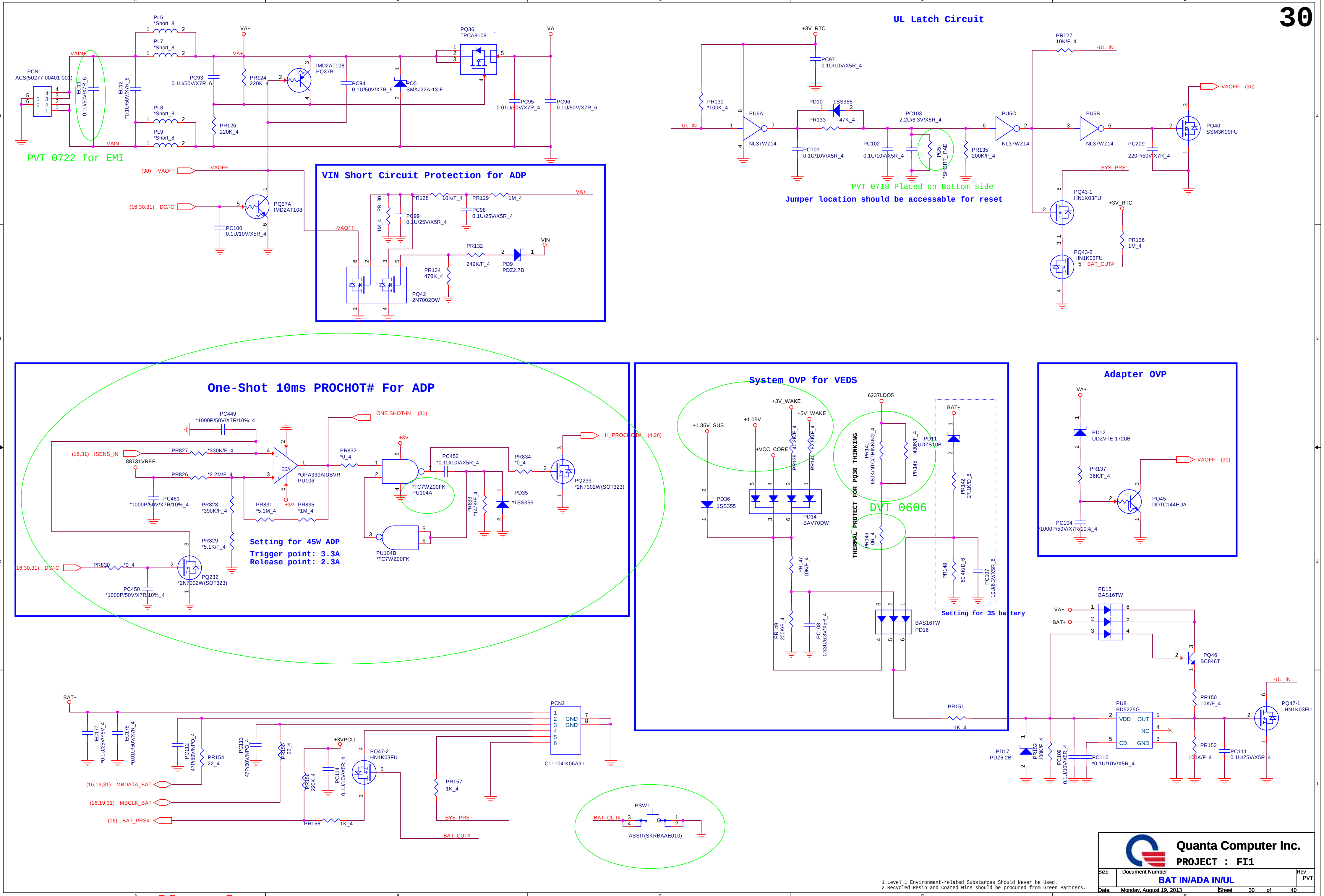
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT : FI1

Size	Document Number	Rev
	+1.05V (UP1522RQDD)-6A	PVT

Date: Monday, August 19, 2013 Sheet 29 of 40


UL Latch Circuit
PVT 0722 for EMI
VIN Short Circuit Protection for ADP
PVT 0718 Placed on Bottom side
Jumper location should be accessable for reset
One-Shot 10ms PROCHOT# For ADP
System OVP for VEDS
Adapter OVP
THERMAL PROTECT FOR PQ36 THINKING
DVT 0606
Setting for 3S battery
Setting for 45W ADP
Trigger point: 3.3A
Release point: 2.3A
PCN1
ACS(50277-00401-001)
PQ36
TPCA8109
PQ37B
IMD2AT108
PQ37A
IMD2AT108
PD5
SMAJ22A-13-F
PQ42
2N7002DW
PD9
PDZ2.7B
PU6A
NL37WZ14
PU6C
NL37WZ14
PU6B
NL37WZ14
PQ40
SSM3K09FU
PQ43-1
HN1K03FU
PQ43-2
HN1K03FU
PU106
*OPA330AIDBVR
PU104A
*TC7WZ00FK
PU104B
*TC7WZ00FK
PQ233
*2N7002W(SOT323)
PQ232
*2N7002W(SOT323)
PD14
BAV70DW
PD16
BAS16TW
PD11
UDZS10B
PD12
UDZVTE-1720B
PQ45
DDTC144EUA
PD15
BAS16TW
PQ46
BC846T
PU8
BD5225G
PQ47-1
HN1K03FU
PQ47-2
HN1K03FU
PD17
PDZ6.2B
PCN2
C11104-K06A9-L
PSW1
ASSIT(SKRBAAE010)
VA+
VA
VAIN+
VAIN-
-VAOFF
DC/-C
VIN
+3V_RTC
-UL_IN
-SYS_PRS
BAT_CUT#
ISENS_IN
88731VREF
ONE SHOT-IN
H_PROCHOT#
+3V
+1.35V_SUS
+1.05V
+3V_WAKE
+5V_WAKE
+VCC_CORE
6237LDO5
BAT+
+3VPCU
MBDATA_BAT
MBCLK_BAT
BAT_PRS#
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.
Quanta Computer Inc.
PROJECT : FI1
Size
Document Number
Rev
PVT
BAT IN/ADA IN/UL
Date: Monday, August 19, 2013
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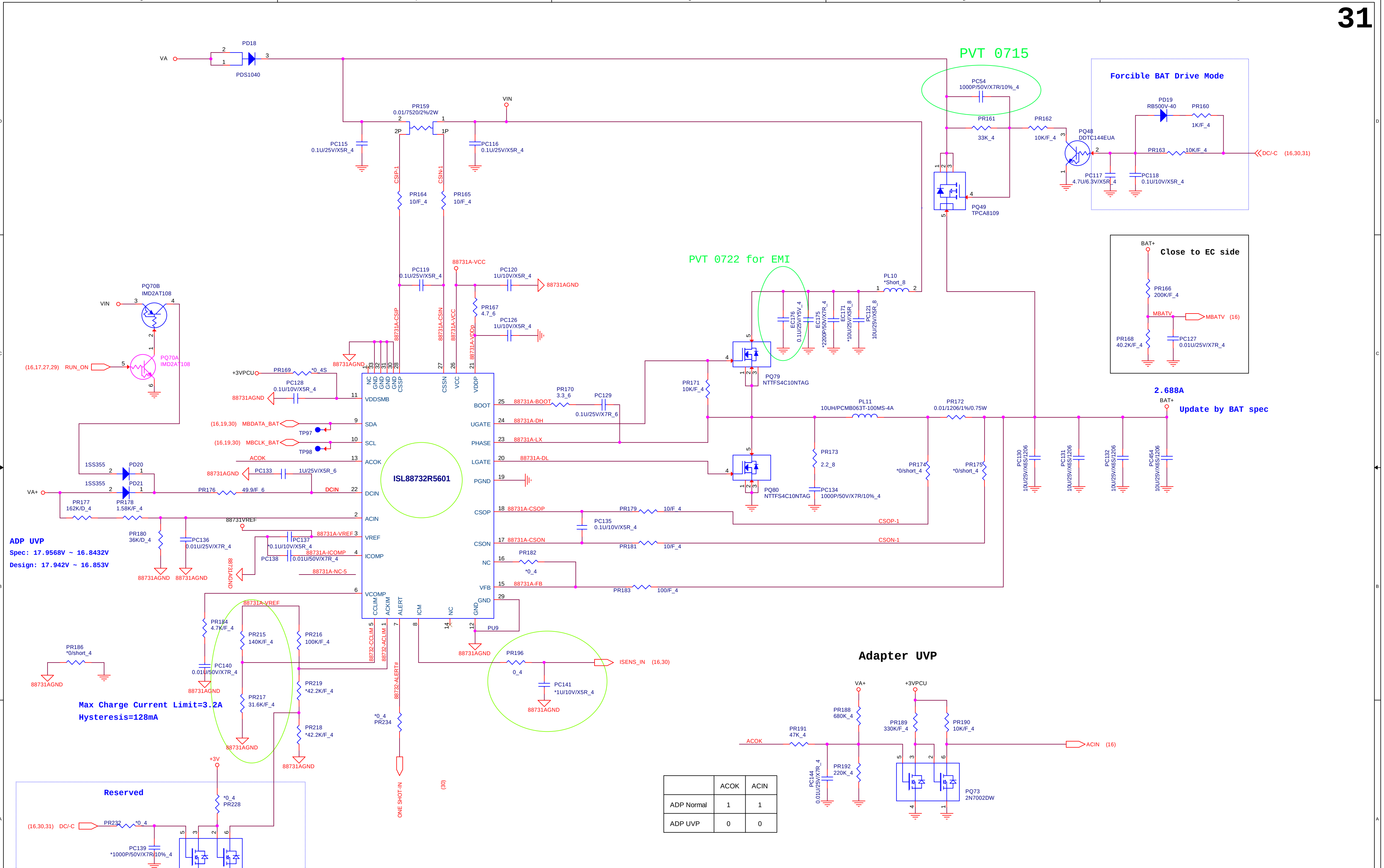


	ACOK	ACIN
ADP Normal	1	1
ADP UVP	0	0

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	CHARGER(ISL88731C)	PVT

Date: Tuesday, August 20, 2013 Sheet 31 of 40

5 4 3 2 1

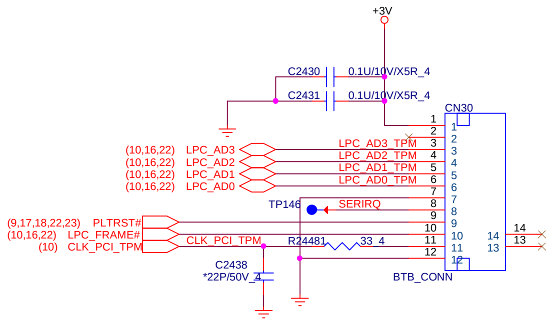
D C B A

Quanta Computer Inc.

PROJECT : FI1

Size	Document Number	Rev
	Debug con	1A
Date: Monday, August 19, 2013	Sheet 32 of 40	

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT : FI1

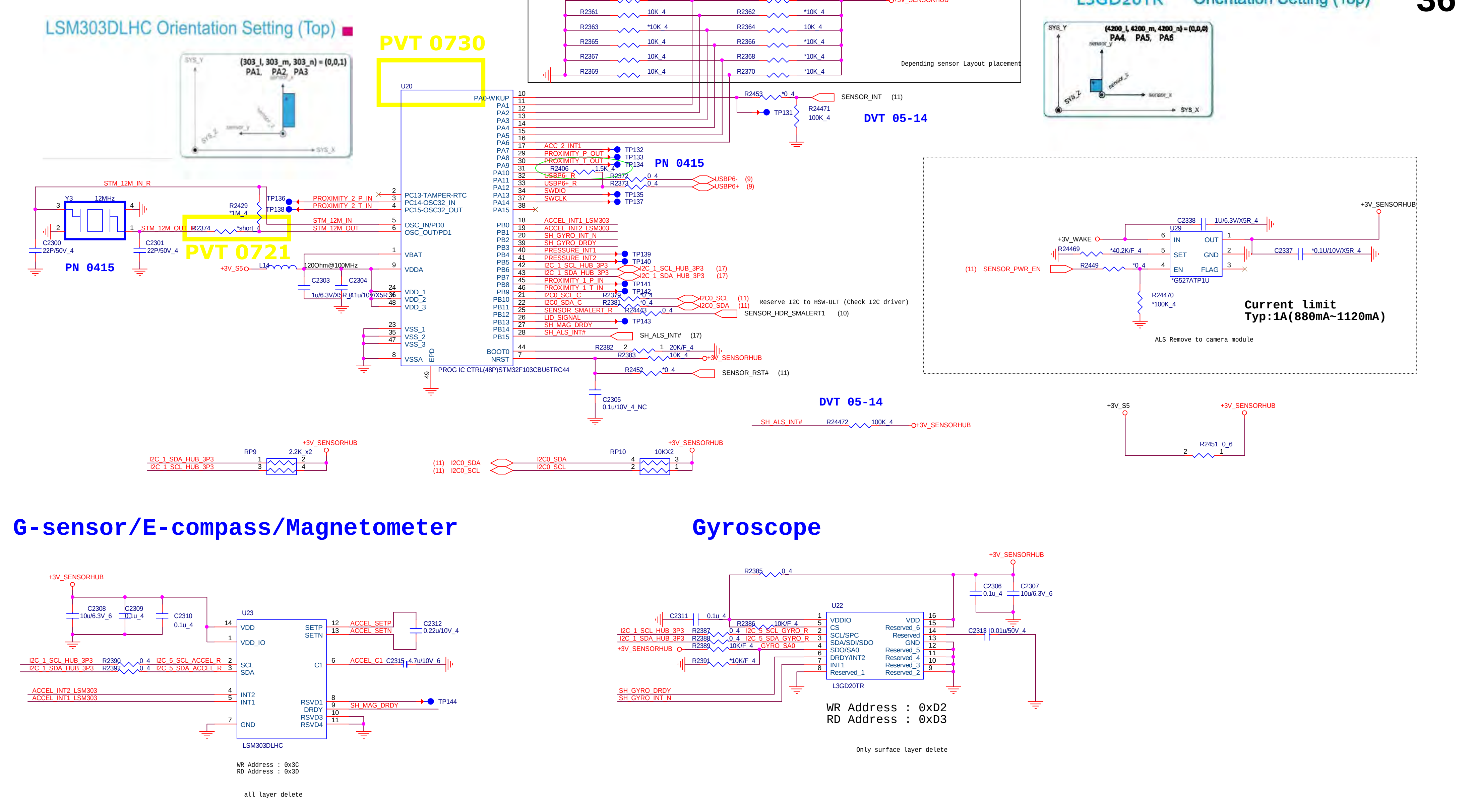
Size	Document Number	Rev
	Nvidia 2/4	1A

Date: Monday, August 19, 2013 Sheet 33 of 40

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Sensor HUB



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI1		
Size	Document Number: Sensors Hub & Sensors	Rev 1A
Date: Monday, August 19, 2013	Sheet 36 of 40	

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	Blank	1A
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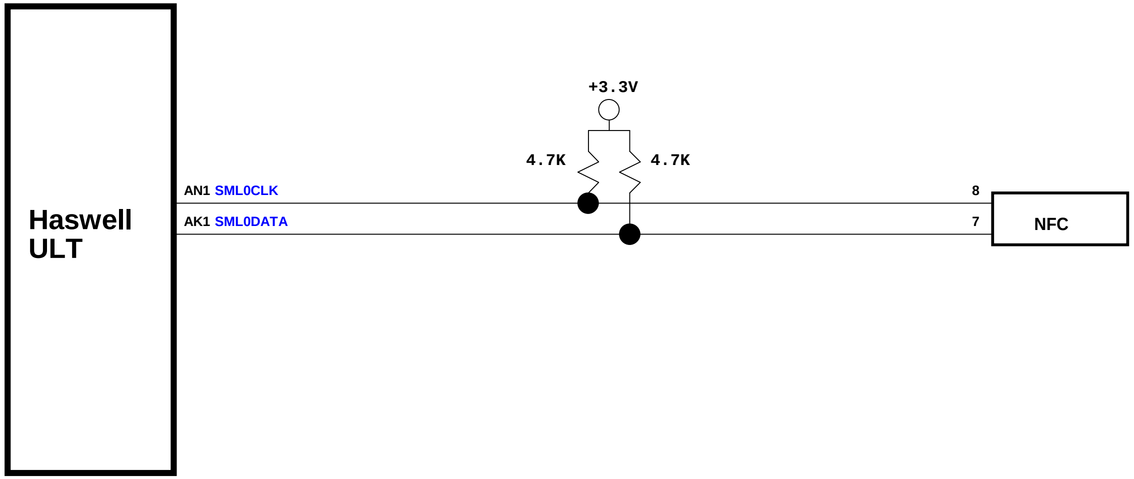

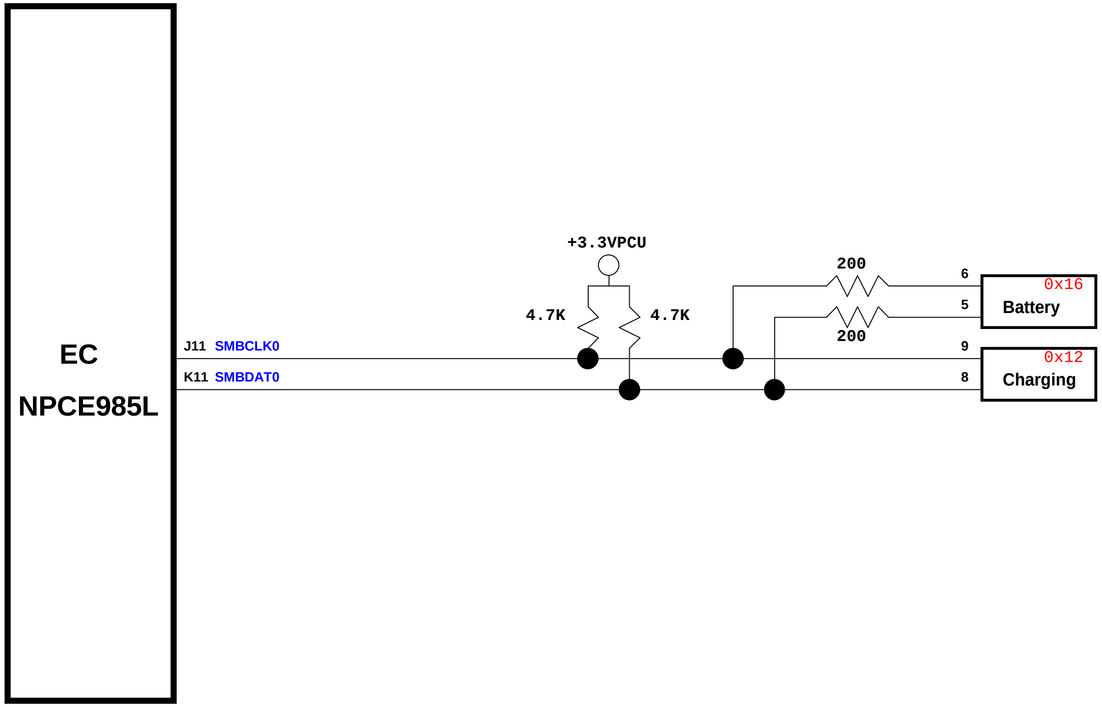

Function	IC	SMBus Address
Charge IC	ISL88731CHRTZ	0X12
Battery	Battery	0X16
NFC		

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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	Camera	1A

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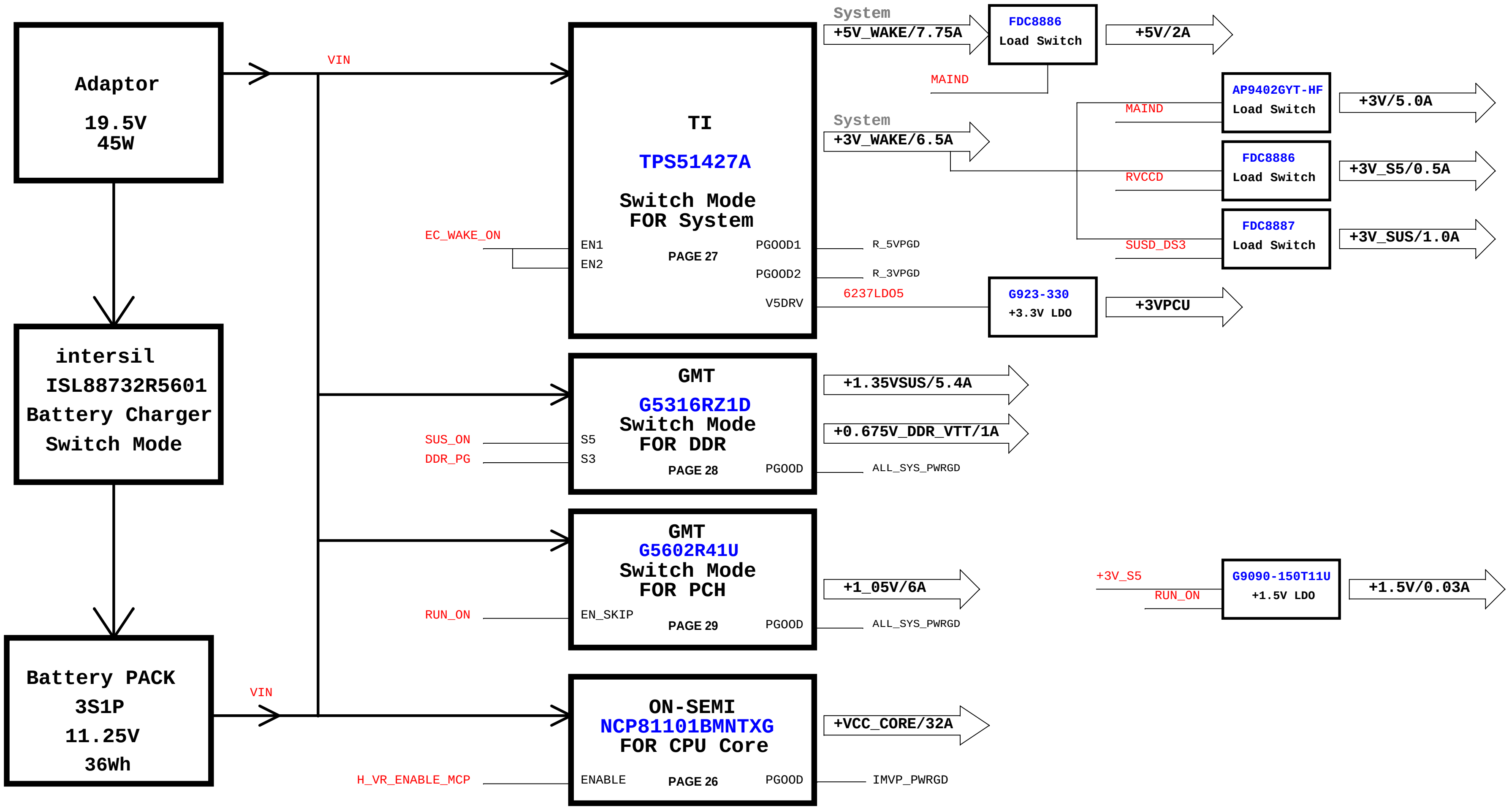
Power	Voltage	S0	S3	DS3	S4 (/W RTC Wake up)	S4 (/WO RTC Wake up)	S4 (/WO CHANGE)	S4 (/W CHANGE)	S5 (/WO CHANGE)	S5 (/W CHANGE)	Ctl Signal
+3VPCU	3.3V	V	V	V	V	V	V	V	V	V	Adapter/BAT in
+3.3V_DSW	3.3V	V	V	V	V	V	V	V	V	V	DEEP_EC_EN
+3V_WAKE	3.3V	V	V	V	V			V		V	**EC_WAKE_ON**
+5V_WAKE	5V	V	V	V	V			V		V	**EC_WAKE_ON**
+5V_S5	5V	V	V		V						**S5_ON**
+3V_S5	3.3V	V	V		V						**S5_ON**
+1.35V_SUS	1.35V	V	V	V							**SUS_ON**
+3V	3.3V	V									**RUN_ON**
+5V	5V	V									**RUN_ON**
+0.675V_DDR_VTT	0.675V	V									**RUN_ON**
+1.05V	**1.05V**	V									**RUN_ON**
+1.5V	**1.5V**	V									**RUN_ON**
+VCC_CORE	**By VID**	V									**RUN_ON**



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Size	Document Number	Rev
	Power TREE	1A

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