MOSFET SPICE model grade

Overview

This section presents the grades of MOSFET SPICE models we provide, and compares the calculated results of these models with the characteristic curves of the data sheet. Referring to this application note, please select the most suitable model grade for the simulation environment and purpose.

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1. Introduction

In recent years, simulation has become important to reduce the development lead time and circuit design. Simulations include electric circuit simulations, thermal simulations and mechanical stress simulations. In electric circuit simulations, we are promoting the publication of SPICE models of PSpice® and LTspice® on the Web (https://toshiba.semicon-storage.com/jp/design-support/simulation.html).

Although the actual circuit evaluation may not always be able to grasp the voltage, current and various characteristics inside the circuit, the ideal operation can be verified by the electric circuit simulation with SPICE model without taking into account the effect of the measuring equipment etc. So, the accuracy of SPICE is important.

We are preparing two types of models for MOSFET, SPICE model (G0) which can verify the function of the circuit in a short time and SPICE model (G2) which has enhanced the accuracy of transient properties. This application note defines the G0 and G2 models, and compares the behavior of actual devices and simulation models using the low voltage MOSFET (U-MOS series) and medium high voltage MOSFET (DTMOS series).

2. Definition of model name and model grade

2.1. Model name

SPICE models are provided with the grade name. The file name configuration is shown below. Each model grade is listed behind the product name.

TPH1R204PL	_ G2	_ 01 _	PSpice _	rev1 _	enc	. lib
Product name	Grade name	Additional number	Simulator name	Control No.	Encryption	extension

2.2. Encryption

Some of the SPICE models we provide are encrypted according to the Simulator, and the one with “enc” in the model name is the encryption model. It is possible to check the Simulator in the model name and the presence or absence of encryption.

Table2-1 The model grade with or without encryption by simulation

SPICE Model grades	PSpice	LTspice
G0	Unencrypted	Encrypted
G2	Encrypted	Encrypted

2.3. Definition of model grades G0 and G2

Table 2-2 shows the reproducibility of the characteristic curve by the grade. The percentage in the table indicate the RMS error (Root Mean Square) that is currently used as the criteria for modeling. The higher the grade, the higher the fitting accuracy to the characteristic curve, which allows more accurate simulations. On the other hand, we recommend that you select the suitable model grade for your simulation environment and purpose because there is a trade-off relationship between fitting accuracy and convergence and time of calculations.

Table 2-2 Model Grade and Characteristic Curve Reproducibility

SPICE Model grades	I_D-V_{DS}	C_{rss}-V_{DS}	C_{oss}-V_{DS}	C_{iss}-V_{DS}
G0 (RMS error criterion)	○ (10% or less)	× (Not applicable)	× (Not applicable)	× (Not applicable)
G2 (RMS error criterion)	○ (5% or less)	○ (2% or less)	○ (2% or less)	○ (2% or less)

① G0

It is a standard device model based on BSIM3 and is a model with short calculation speed and suitable for function checking.

② G2

Compared with the G0 model, this model enhances the reproducibility of the high current region characteristics of I_D-V_{DS} curve and the voltage dependent characteristics of the parasitic capacitance, enabling highly accurate switching simulations that are closer to actual measurements.

3. Fitting accuracy (RMS error)

The fitting accuracy of SPICE model can be quantified by RMS error. For MOSFETs, this RMS error is used when determining the accuracy of the created SPICE model, and the difference from the actual measurement is quantified and we use them as the criteria. Figure 3-1 shows the RMS-error formula~~s~~ used in creating the MOSFET SPICE models we provide.

Chapters 4 and 5 show examples of low voltage MOSFET (U-MOS series) and medium high voltage MOSFET (DTMOS series).

$$\sqrt{\frac{\sum_{j=1}^{N}(sim_j - meas_j)^2}{\sum_{j=1}^{N}(meas_j)^2/N}/N}$$

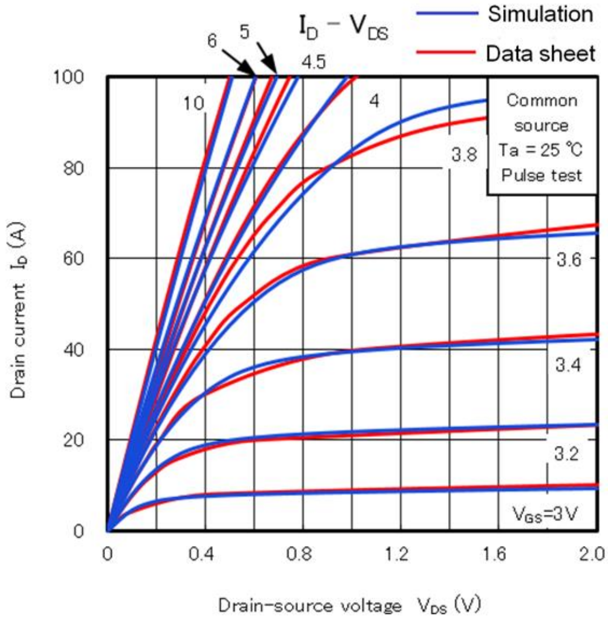
sim_j : Simulation value
$meas_j$: Measured value

Figure 3-1 RMS error expression used when creating a Web published device model

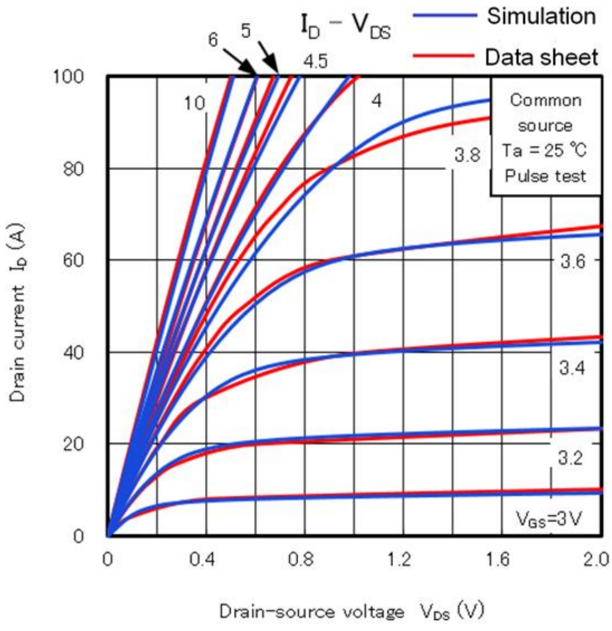
Fitting accuracy comparison of G0 and G2 model in U-MOS series

4.1 I_D-V_{DS} curve (TPH5R60APL)

U-MOS Series is a MOSFET Series with a trench gate structure with 12V～300V withstand voltage. Fig. 4-1 shows a fitting curve sample for I_D-V_{DS}. The slope of I_D from low V_{GS} to high V_{GS} can be simulated, and good fitting accuracy is achieved with 2.43% RMS failure for both the G0 and G2 models.



G0 model (RMS error: 2.43%)

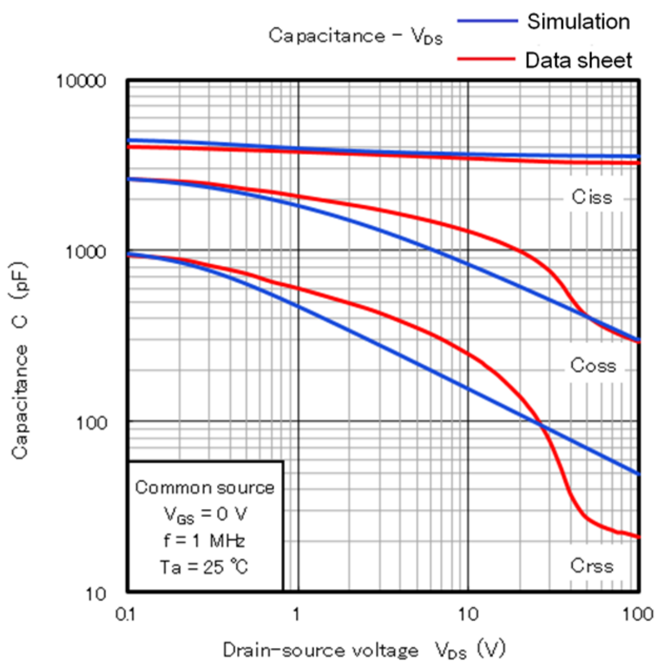


G2 model (RMS error: 2.43%)

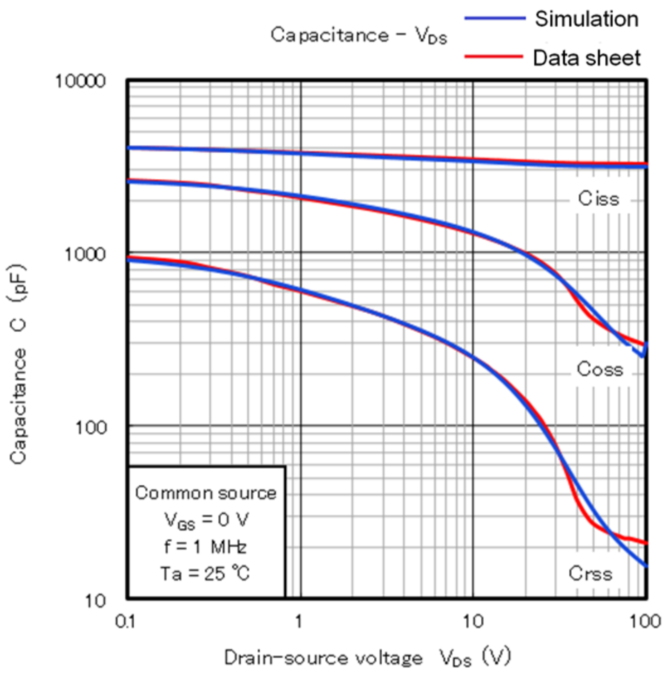
Figure 4-1 I_D-V_{DS} Characteristics curve simulated by G0 and G2 models and data sheet

4.2 Parasitic capacitance curve (TPH5R60APL)

Fig. 4.2 shows C_{iss}, C_{oss}, C_{rss} capacitance curves. Since the G0 model is based on BSIM3, it cannot represent the nonlinearity of the capacitance characteristics, and the simulation curves of C_{rss} and C_{oss} deviate significantly from the characteristic curves of the datasheet. On the other hand, the G2 model is sufficiently capable of representing the characteristic curve of the data sheet.



G0 model
RMS error
C_{iss}:0.33%、C_{rss}:1.92%、C_{oss}:1.35%



G2 model
RMS error
C_{iss}:0.06%、C_{rss}:0.27%、C_{oss}:0.16%

Figure 4-2 Parasitic capacitance characteristics simulated by G0 and G2 models and data sheet

4.3 Switching Analysis (TPH1R306PL)

Next, the switching analysis is described. This analysis was performed using our fabricated resistive load board. A simple circuit model for this test board is shown in Figure 4-3. Figure 4-4 shows the comparison simulation results of this circuit model and measured voltage, current waveforms.

As shown in Section 4.2, the G0 model cannot suppress steeply changing current and voltage due to inadequate nonlinearity representation of capacitance characteristics and inability to express the original capacitance values. As a result, ringing occurs at the drain-source voltage (V_{DS}). On the other hand, in the G2 model, almost the same change as the actual capacitance is realized during the rising process of the drain voltage, so the process in which V_{DS} transitions to the steady state is sufficiently expressed in the same way as the measured waveform.

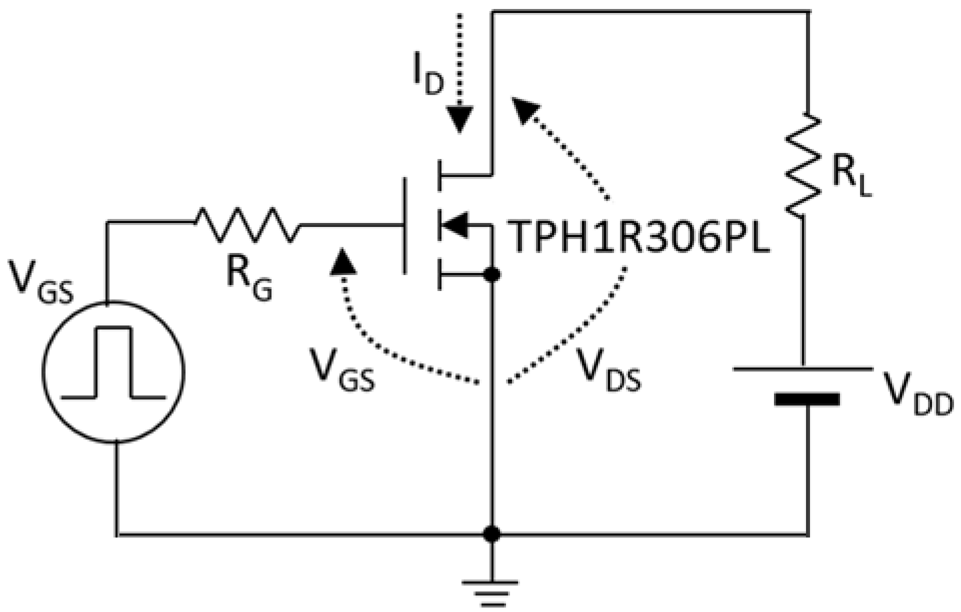


Figure 4-3 Resistive load switching circuit

Measurement conditions: Resistive load circuit,
V_{DD}=30V, V_{GS}=0/10V, I_D=60A, R_L=0.5 ohms, Ta = room temperature (measured)/27 °C (simulated)

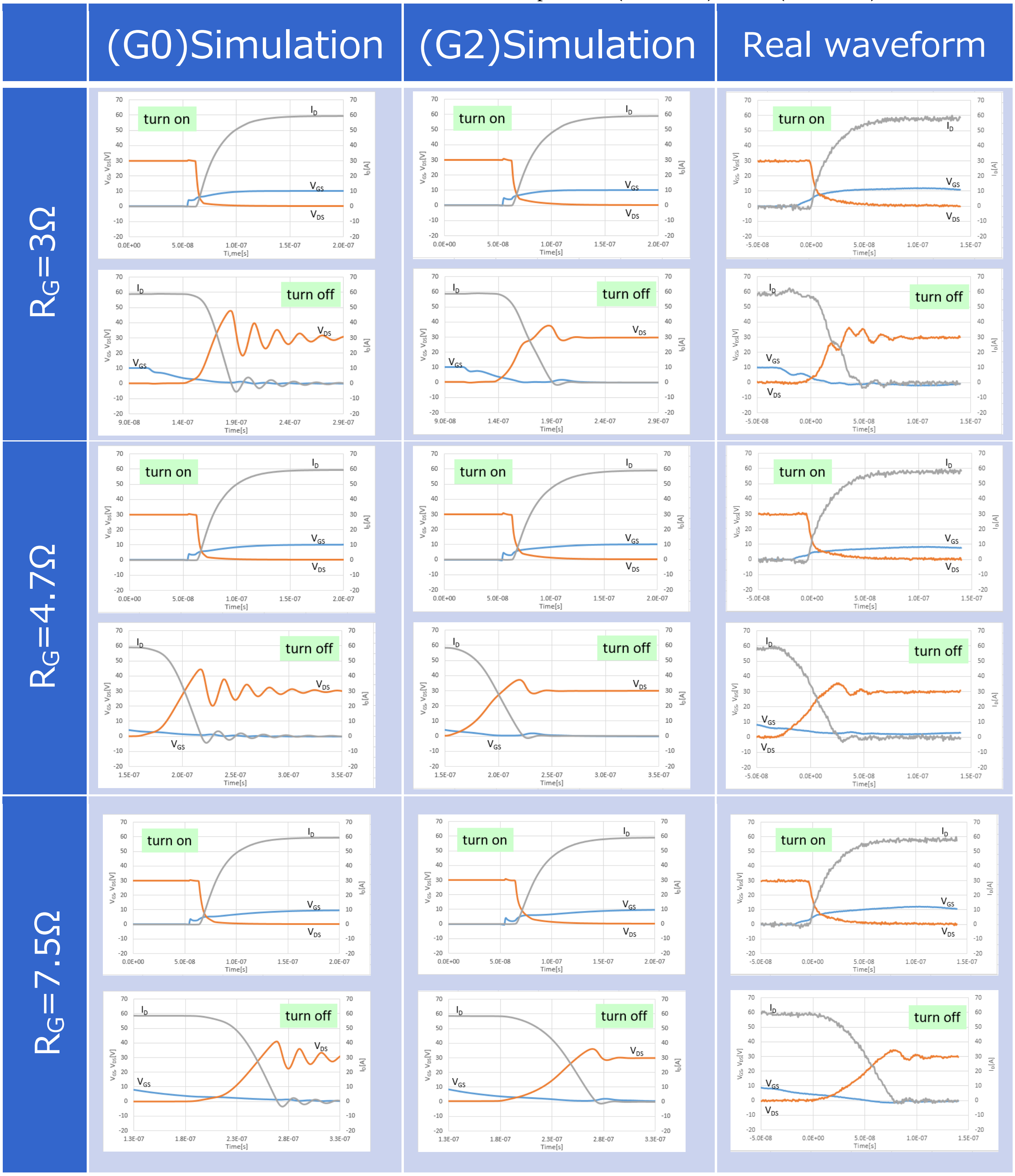
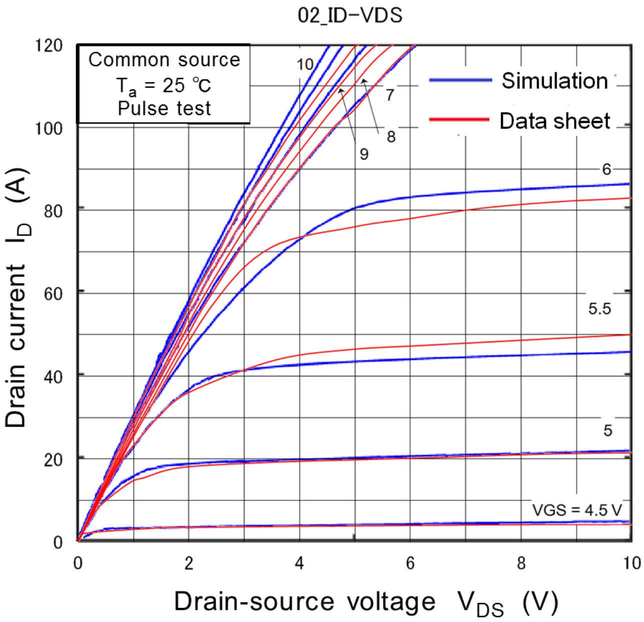


Figure 4-4 Simulation and actual measurement comparison of resistive load circuit switching waveforms

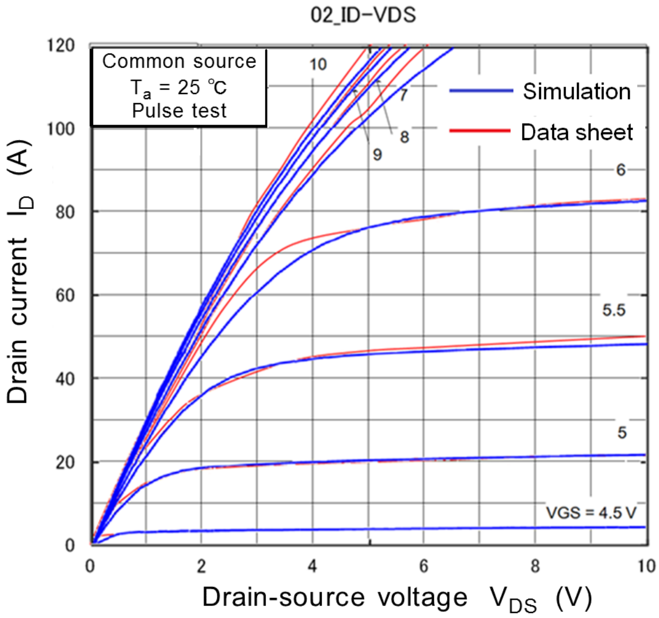
5. Fitting accuracy comparison of G0 and G2 model in DTMOS series

5.1 I_D-V_{DS} curve (TK040N65Z)

The DTMOS series is a MOSFET series with a super junction (SJ) structure of 600V to 800V. Fig. 5-1 shows I_D-V_{DS} fitting curve of DTMOSVI series TK040N65Z. DTMOS series G2 model provides better reproducibility of saturation properties in the high current region of I_D-V_{DS}. As a result, the RMS error of the G0 model is 4.72%, while that of the G2 model is 2.18%, which shows good fitting accuracy.



G0 model (RMS error: 4.72%)

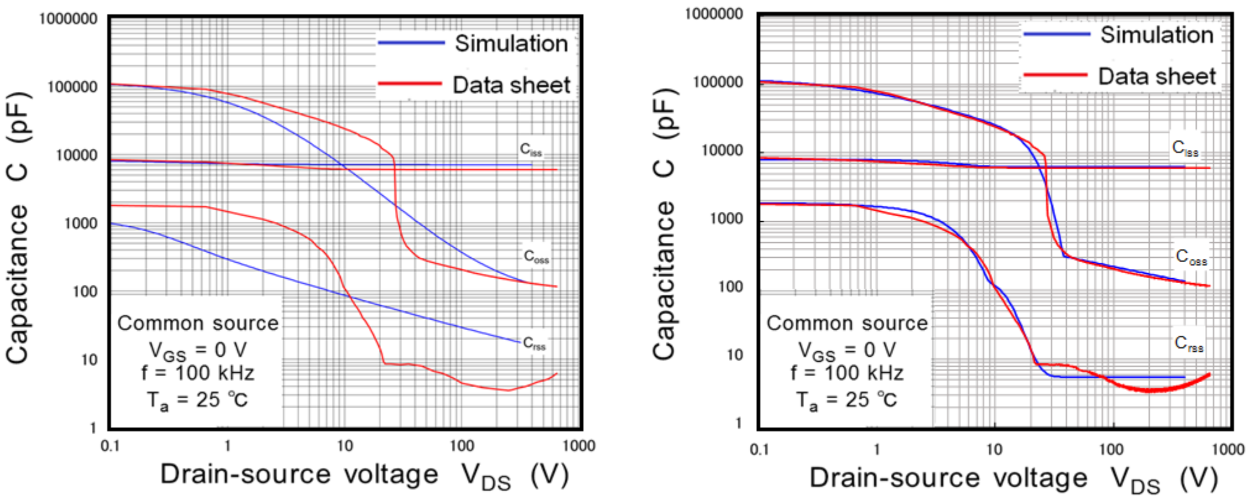


G2 model (RMS error: 2.18%)

Figure 5-1 I_D-V_{DS} Characteristics curve simulated by G0 and G2 models and data sheet

5.2 Parasitic capacitance curve (TK040N65Z)

Fig. 5-2 shows C_{iss}, C_{oss}, C_{rss} capacitance curve. Since DTMOS series has a super-junction (SJ) structure, the C_{rss}, C_{oss} curves for V_{DS} decreases sharply from a certain voltage value. Since the G0 model is based on BSIM3, it is not possible to express the non-linearity of this steeply decreasing capacitance characteristic, and the simulation curves of C_{rss} and C_{oss} deviate significantly from the characteristic curve of the data sheet. On the other hand, the G2 model can express the parasitic capacitance curve with an RMS error of 2% or less.



G0 model
RMS error
C_{iss}:0.53%、C_{rss}:6.25%、C_{oss}3.96%

G2 model
RMS error
C_{iss}0.22%、C_{rss}0.914%、C_{oss}0.97%

Figure 5-2 Parasitic capacitance characteristics simulated by G0 and G2 models and data sheet

5.3 Switching Analysis (TK040N65Z)

Next, the switching analysis is described. This time, we performed an analysis using our fabricated inductive load switching board. A simple circuit model for this test board is shown in Figure 5-3. Figure 5-4 shows the simulation results of this circuit model and comparison of measured voltage and current waveforms.

As shown in Section 5.2, the G0 model has insufficient nonlinear representation of the capacitance characteristics and cannot express the actual capacitance value, so that the gate voltage oscillation observed in actual measurements cannot be seen.

Also, the turn-off loss (E_{off}) is not consistent with the actual measurement and larger than that. On the other hand, the G2 model is able to express that the gate-oscillation voltage decreases with increasing R_G, and that difference of E_{off} is also within 10% from the actual measurement. Therefore, the G2 model is a device model capable of verifying the dynamic characteristics.

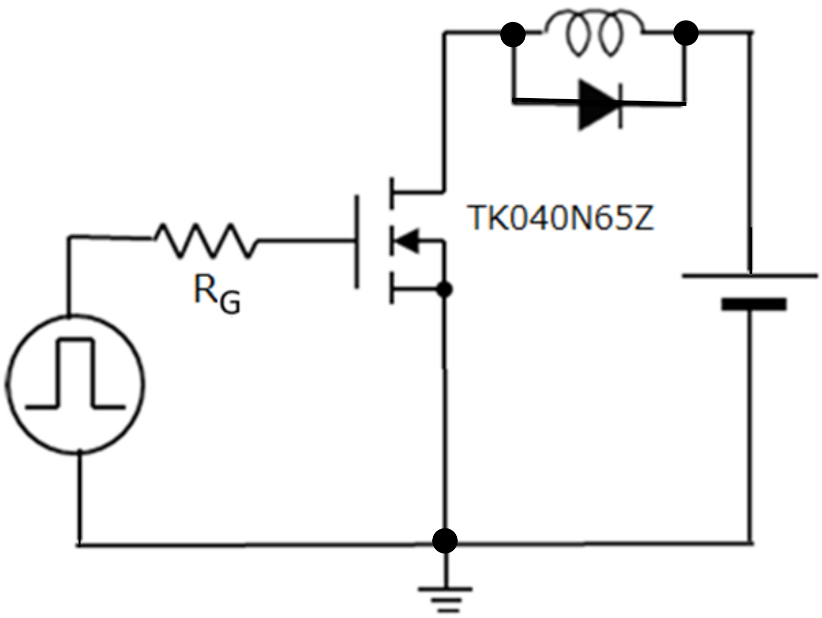


Figure 5-3 Inductive Load Switching Circuit

Measurement conditions: inductance load circuit,
V_{DD}=400V, V_{GS}=0/10V, I_D=10A, Ta = room temperature (measured)/27°C (simulated)

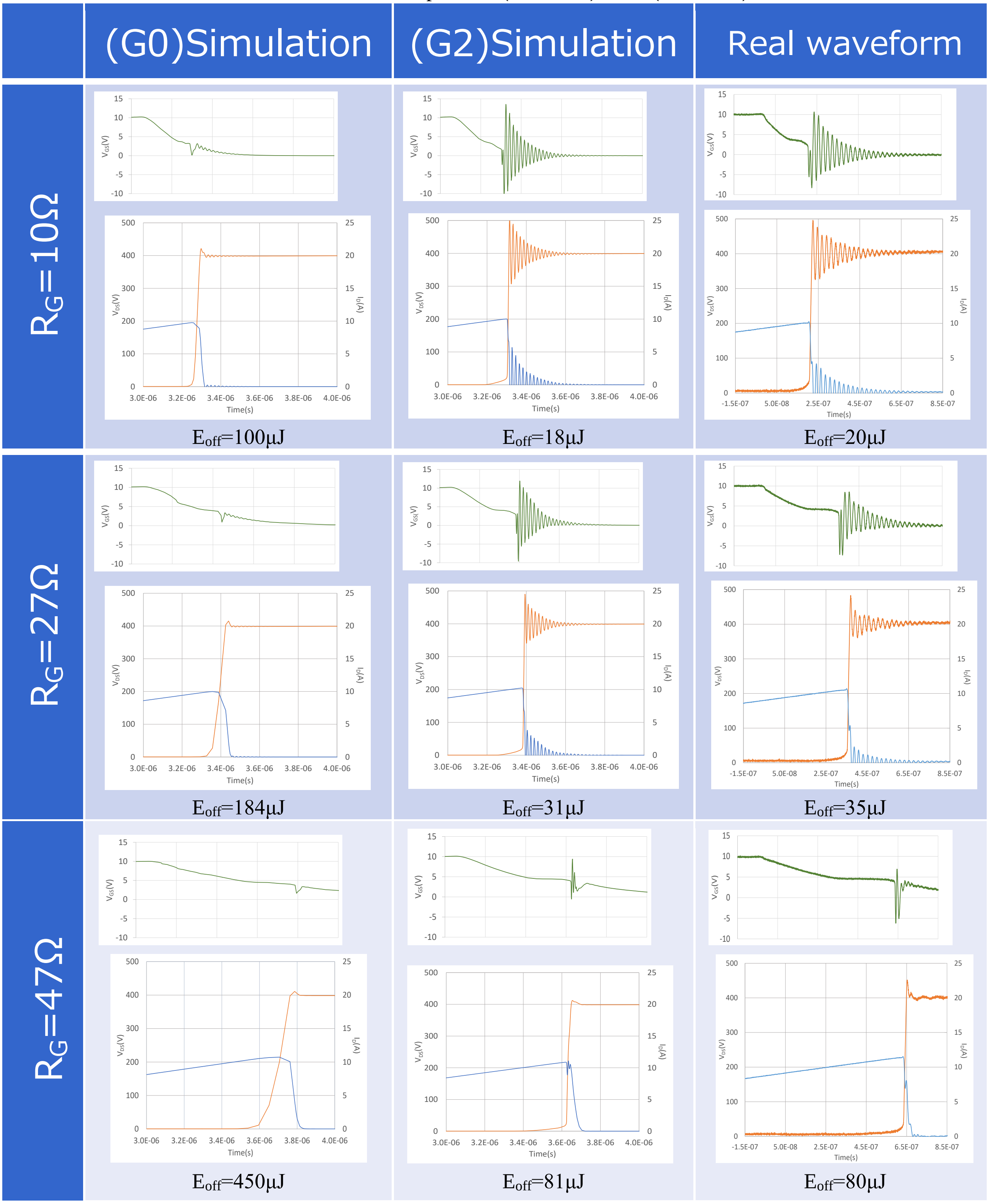


Figure 5-4 Simulation and actual measurement comparison of inductive load circuit switching waveforms

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