TI IBIS File Creation, Validation, and Distribution Processes

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ABSTRACT

The Input/Output Buffer Information Specification (IBIS), also known as ANSI/EIA-656, has become widely accepted among electronic design automation (EDA) vendors, semiconductor vendors, and system designers as the format for digital electrical interface data. Because IBIS models do not reveal proprietary, internal processes, or architectural information, semiconductor vendors' support for IBIS continues to grow. IBIS models are one of the most important tools used to support TI customers. TI's goal is to create IBIS models that are compatible with the latest IBIS specifications for every new logic part. This application report describes TI's IBIS creation, validation, and distribution process, so that customers can be better informed about our IBIS models. This application report also discusses the accuracy of IBIS models provided by TI.

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1 Introduction

1.1 What is IBIS?

The input/output buffer information specification (IBIS) is a behavioral-modeling specification. It is a standard for describing the analog behavior of the buffers of a digital device using plain ASCII-text formatted data. The data in an IBIS file is used to perform signal integrity (SI) simulations of printed circuit boards. The information needed to perform this simulation is buffer voltage-current (V-I) characteristics and switching (output voltage versus time) characteristics.

1.2 History of IBIS

IBIS was created in the early 1990s to promote tool-independent I/O models for system-level signal-integrity work. PCI bus signal-integrity simulations were ramping up at Intel™, but no one had a PCI buffer designed. In general, SPICE models were not commonly available. To overcome this problem, Intel™ developed a behavioral buffer model in HSPICE that simulates any buffer characteristics. The behavioral model was so successful that Intel™ decided to supply it to customers. But, all customers did not use HSPICE, so a tool-independent model format was needed. Several electronic design automation (EDA) tool vendors showed interest in a common modeling format, and the IBIS open forum was formed. The first IBIS specification, 1.0, was released in April 1993.

1.3 Input Model

SPICE models are the most widely used models. SPICE models are based on transistor-level modeling. For complicated electronic circuits, the total time required to complete a simulation in SPICE is long. SPICE models also should be encrypted, or there should be a nondisclosure agreement (NDA) in place to protect proprietary information. On the other hand, IBIS is a behavioral model and does not reveal any proprietary information. Because IBIS is a behavioral model, the total time for simulation is much less than for SPICE.

2 Brief Description of Some Common Types of IBIS Models

An IBIS file of a device contains the electrical characteristics of all the unique pins of that device. Electrical characteristics of a specific pin are called an IBIS model of that pin. An IBIS file also contains the package resistance, inductance, and capacitance (R, L, and C) data for each pin.

The following are the most common types of pins in a digital-logic device:

- Input
- 2-state output
- 3-state output
- Input/output (I/O)
- Open drain

Similarly, the model in an IBIS file can be input, 3-state, I/O, etc.

2.1 Input Model

The input pin structure of a digital device can be thought of as a combination of the following circuits and elements.

- A circuit that is activated if the input voltage is over V_{CC} or logic high (power clamp)
- A circuit that is activated if the input voltage is below ground or logic low (ground clamp)
- A circuit that is activated if the input is within V_{CC} and ground (active circuit)
- Resistance, inductance, and capacitance of the package (R, L, and C)
- Die capacitance of the input pin

The data for these circuits and elements are described under several keywords in the IBIS file. IBIS keywords are shown in square brackets.

The behavior of the first circuit is listed under the [POWER Clamp] keyword, and the behaviors of the latter two circuits are listed under the [GND Clamp] keyword. R, L, and C are listed under the [Pin] keyword. Most often, a CMOS digital device has the input structure shown in Figure 1. In this input structure, V_{DD} is the power-clamp reference because the upper clamp diode is connected to the dc voltage source V_{DD}†, and $-V_{SS}$† is the ground-clamp reference because the lower clamp diode is connected to the dc voltage source $-V_{SS}$. The details of power-clamp and the ground-clamp references are discussed later in this application report. Even though the package R, L, and C data are included for the input pin, the ground-clamp and power-clamp data for the IBIS model are extracted without package data; i.e., package R, L, and C do not have any effect on this data.

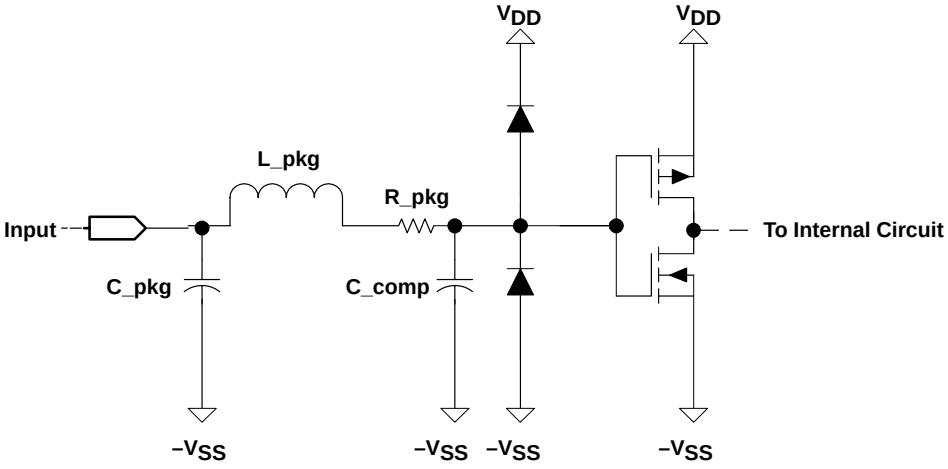


Figure 1. Input Model Structure

The upper clamp diode is forward biased when the input is approximately 0.7 V over V_{DD}. The lower clamp diode is forward biased when the input is approximately 0.7 V less than $-V_{SS}$.

† V_{DD} is equivalent to V_{CC} or power supply and $-V_{SS}$ is equivalent to GND in TI digital logic devices.

The input-type model has the following data. Subparameters are enclosed in parentheses.

- Maximum lower threshold voltage (Vinl): V_{IL} in the data sheet.
- Minimum upper threshold voltage (Vinh): V_{IH} in the data sheet.
- Power-clamp reference [Power Clamp Reference]: In most digital circuits, the power-clamp reference voltage is V_{CC} because the power-clamp diode is connected to V_{CC}. However, in some cases it may be different than the V_{CC} or power supply. For example, with 5-V safe 3.3-V buffers, the power-clamp reference is 5 V.
- Ground-clamp reference [GND Clamp Reference]: In most digital circuits, the ground-clamp reference voltage is 0. However, in some cases it may be different than the ground. For example, in RS-232 devices it is –12 V.
- Recommended power supply [Voltage Range].
- Recommended temperature [Temperature Range]: The junction temperature of transistors.
- C_comp data (C_comp): This is the total die capacitance as seen at the die pad. C_comp does not include package capacitance. It includes parasitic capacitance of transistors and circuit elements, metal capacitance-connecting transistors with the die pad, and die-pad capacitance.
- Power-clamp data [POWER Clamp]: Voltage-current characteristics of the power-clamp circuit. This data is referenced to the power-clamp reference voltage, i.e., in the IBIS file the power clamp voltage is V_{table} = [Power Clamp Reference] – V_{in}, where V_{in} is the voltage referenced to ground. For example, if power-clamp reference is V_{CC}, then the voltage data in IBIS file is $V_{table} = V_{CC} - V_{in}$. This is the voltage across the diode, not the input voltage.
- Ground-clamp data [GND Clamp]: Voltage-current characteristics of the ground-clamp circuit. This data is referenced to ground-clamp reference voltage, i.e., in an IBIS file the ground-clamp voltage is $V_{table} = V_{in}$ – [GND Clamp Reference], where V_{in} is the voltage referenced to ground. For example, if the ground-clamp reference is ground, the voltage data in the IBIS file is $V_{table} = V_{in}$.

If the power-clamp reference voltage is not mentioned, then, by default, it is equal to the recommended power-supply voltage. Similarly, if the ground-clamp reference voltage is not mentioned, then, by default, it is equal to ground or 0.

The range of data is based on the worst-case scenario of a transmission line. For example, a device with a power-clamp reference of V_{DD} and a ground-clamp reference of $–V_{SS}$ has a maximum voltage of $(2 \times V_{DD} + V_{SS})$ and minimum voltage of $–(2 \times V_{SS} + V_{DD})$.

The power-clamp diode is on from V_{DD} to maximum voltage; i.e., $2 \times V_{DD} + V_{SS}$. As in the IBIS file, power-clamp data is V_{DD} relative, so the range would be $–(V_{DD} + V_{SS})$ to 0 (V_{table} = [(power-clamp reference voltage) – V_{in}]). Ground-clamp diode data range from $–(2 \times V_{SS} + V_{DD})$ to V_{DD}. In the IBIS file, the data ranges from $–(V_{SS} + V_{DD})$ to $(V_{DD} + V_{SS})$ ($V_{table} = V_{in}$ – ground-clamp reference voltage).

So, for a 5-V V_{CC} device, the range of ground-clamp data in the IBIS file is from –5 V to 5 V, and for power-clamp data, the range is –5 V to 0 V. There may be a question of why the range of ground-clamp data is from –5 V to 5 V, since the diode is forward biased only from –5 V to 0, and from 0 to 5 V, the diode is reverse biased. The reason is that, even though it is designated as ground clamp, the data also contains the V-I data at the normal operating conditions. For example, if IBIS users need to know what the input current at threshold is or what the bus-hold current is, they can get it from the ground-clamp data.

2.2 2-State Output

A device with a 2-state output does not have an enable pin to disable the output. The 2-state output pin can be thought of as a combination of the following elements and circuits.

- A pullup circuit that is activated when the output is high
- A pulldown circuit that is activated when the output is low
- Die capacitance of the output pin
- R, L, and C of package

The 2-state buffers contain the following information:

- Data-sheet parameter for ac measurement: These subparameters are used to describe the test condition during propagation-delay measurement. The subparameters are Rref, Cref, Vref, and Vmeas. The definitions of these terms are given later in this application report.
- Pullup reference voltage [Pullup Reference]: This is the reference for the pullup circuit. For example, in most digital circuits, the pullup reference voltage is V_{CC} because the pullup circuit is connected to the V_{CC} or power-supply rail. The default reference is the power supply listed under (Voltage range) in the IBIS model.
- Pulldown reference [Pulldown Reference]: This is the reference for the pulldown circuit. For example, in most digital circuits, the pulldown reference is ground because the pulldown circuit is connected to the ground. The default reference is ground.
- Recommended power supply [Voltage range]
- Recommended temperature [Temperature Range]: This is the junction temperature of transistors.
- C_comp data (C_comp)
- Pullup data [Pullup]: These are the V-I characteristics of the pullup circuit. This data is referenced to the pullup reference voltage; i.e., in the IBIS file, V_{table} = [Pullup Reference] – V_{in}, where V_{in} is the voltage referenced to ground. For example, if the pullup reference is V_{CC}, the voltage data in the IBIS file is $V_{table} = V_{CC} – V_{in}$. This is the voltage across the pullup circuit, not the voltage at the output.
- Pulldown data [Pulldown]: These are the V-I characteristics of the pulldown circuit. This data is referenced to the pulldown reference voltage; i.e., in the IBIS file, $V_{table} = V_{in}$ – pulldown reference voltage, where V_{in} is the voltage referenced to ground. For example, if the pulldown reference is ground, the voltage data in the IBIS file is $V_{table} = V_{in}$.
- Ramp data [Ramp]
  - Output rise slew rate; i.e., dV/dt for the rising waveform (dV/dt_r). This data is derived from a resistive load connected to the pullup reference.
  - Output fall slew rate; i.e., dV/dt for the falling waveform (dV/dt_f). This data is derived from a resistive load connected to the pulldown reference.
  - Test load (R_load). Resistive load used to generate the dV/dt data. The default value is 50 Ω.

The definition of dV and dt in an IBIS model is:

$dV = 0.8 \times (V_{max} - V_{min}) - 0.2 \times (V_{max} - V_{min})$

dt = time between $0.8 \times [V_{max} - V_{min}]$ and $0.2 \times [V_{max} - V_{min}]$ during a transition.

V_{max} and V_{min} are the maximum and minimum voltages during a transition.

The ramp rate must be specified as an explicit fraction and must not be reduced.

Rising and falling waveform data for an output model reveals how much time it takes to change from one state to another when driving a resistive load. Minimums of four V-T curves are needed to adequately describe a push-pull buffer.

- Rising waveform [Rising Waveform] data with resistive load connected to pulldown reference. These data also are known as pullup on data. The turn-on time for pullup circuits can be determined from these data.
- Falling waveform [Falling Waveform] data with resistive load connected to pullup reference. These data also are known as pulldown on data. The turn-on time for pulldown circuits can be determined from these data.
- Rising waveform [Rising Waveform] data with resistive load connected to pullup reference. These data also are known as pulldown off data. The turn-off time for pulldown circuits can be determined from these data.
- Falling waveform [Falling Waveform] data with resistive load connected to pulldown reference. These data also are known as pullup off data. The turn-off time for pullup circuits can be determined from these data.

The EDA simulator tool uses the V-t data and V-I data in the IBIS model for signal-integrity simulation. There is a concern about the simulation result being accurate if the V-t data is taken at a resistive load that is different than that being used by the customer in their simulation.

Figure 2 shows a test setup for simulation to compare the accuracy of an IBIS model created with V-t data taken at a 50-Ω load, versus a 500-Ω load. Figure 3 shows the plot of voltage waveforms comparison at the transmission-line end. The simulation was done using the SN74LVC04A IBIS model, TSSOP package, 3.3-V V_{CC}, nominal temperature, and 10-MHz frequency. HSPICE was used as the simulator tool and the V-t options were ramp_rwf = 2 and ramp_fwf = 2. In Appendix A, a test file to use an IBIS model in HSPICE is described, and the details of these options are discussed. From the plot, it is clear that the difference in simulation due to R_fixture is negligible.

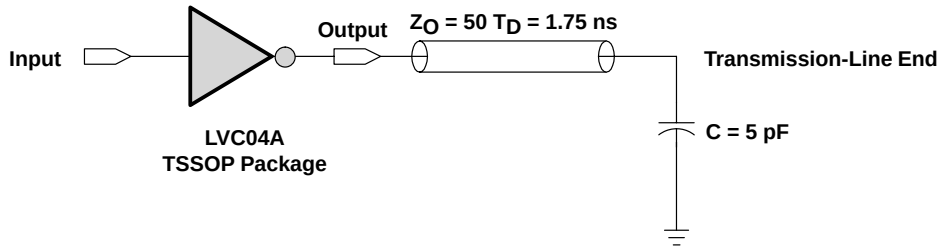


Figure 2. Test Simulation Setup to Compare the Difference in Voltage Waveforms Due to R_fixture

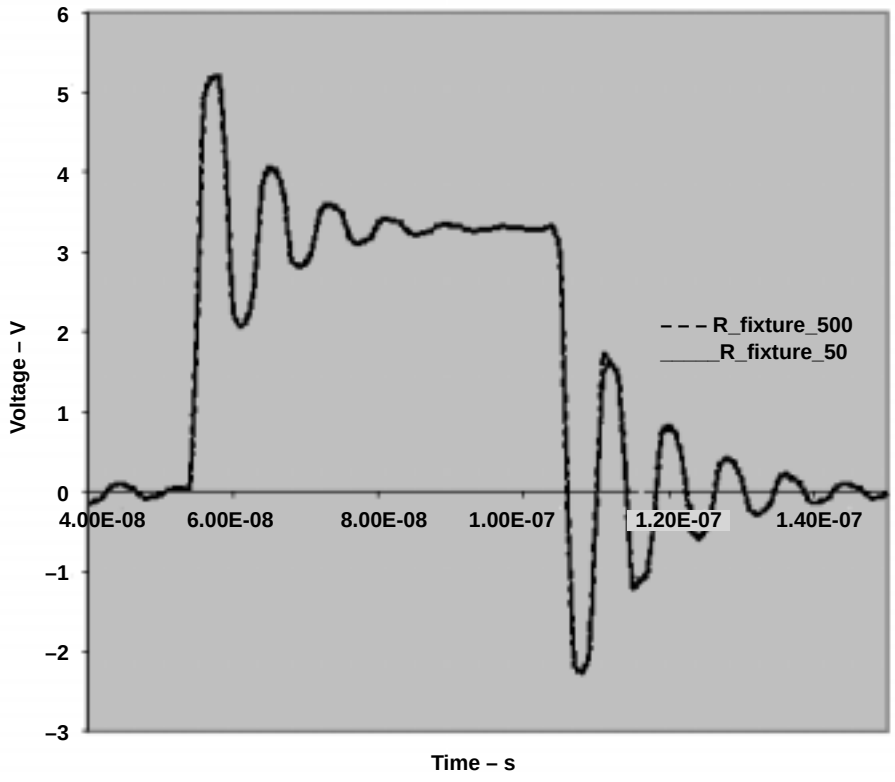


Figure 3. Comparison of Voltage Waveforms for IBIS Model Created With 50-Ω and 500-Ω Loads

IBIS does not limit the total number of sets of V-t data. The V-t data can be more than four sets (two rising and two falling). Also, the voltage need not be the pullup and pulldown reference voltage. The resistive load is termed R_fixture in the IBIS model and the voltage source it is connected to is termed V_fixture. There are two more subparameters: (L_fixture) and (C_fixture). R_fixture, L_fixture, V_fixture, and C_fixture are shown in Figure 4.

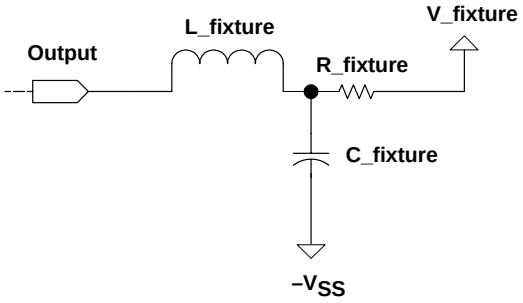


Figure 4. V_fixture, R_fixture, C_fixture, and L_fixture in AC Test

A simplified 2-state output is shown in Figure 5. Even though the package is shown as part of the output, the IBIS data does not include the effect of the package.

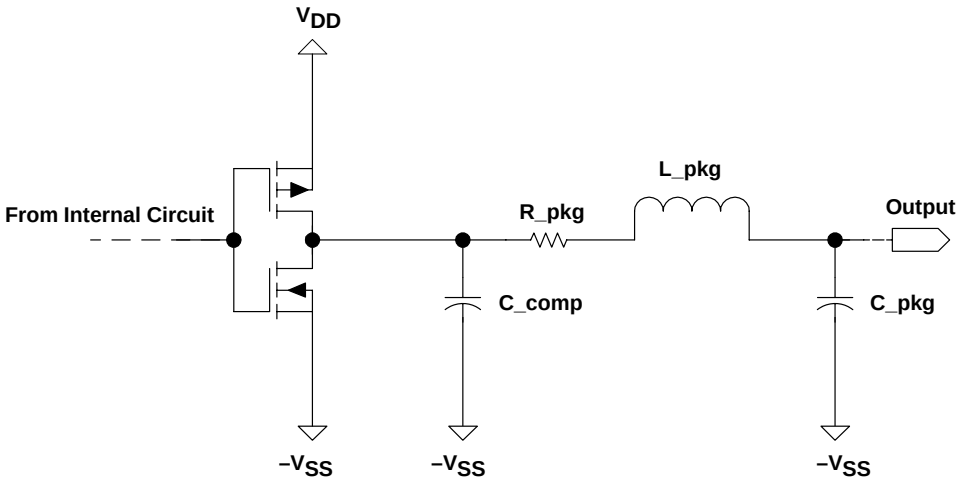


Figure 5. Two-State Output Model Structure

When the output is logic high, the p-channel FET is on and the n-channel FET is off. Pullup characteristics are the V-I characteristics of the p-channel FET. In a real device, there may be additional pullup paths; i.e., additional transistors that are on may be connected from output to V_{DD} and, as a result, pullup data is the total drive strength of the device at a logic-high state. Similarly, pulldown data is the total drive strength of the device at a logic-low state.

A 2-state buffer may have clamp diodes connected at the output. There is no way to make both transistors be off at the same time and get the V-I data for clamp diodes. The pullup and pulldown data contains the V-I data of clamp diodes, if there is any.

Cref and Rref correspond to the test loads that the semiconductor vendor uses when specifying the propagation delay. Vref corresponds to the test voltage during the propagation delay measurement. Values of Vref, Cref, and Rref can be found in the data-sheet parameter-measurement information. The assumed connections for Vref, Rref, and Cref are shown in Figure 6.

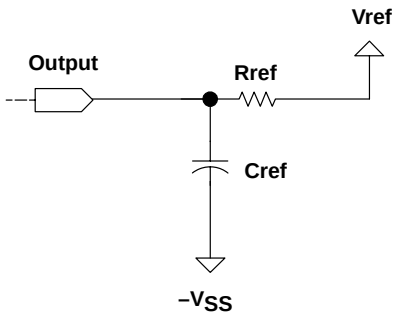
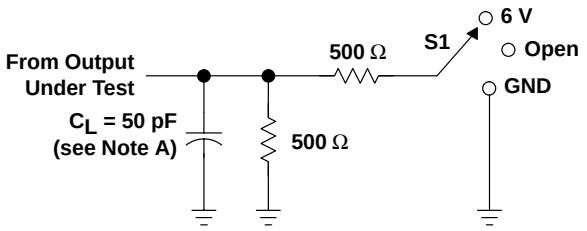


Figure 6. Rref, Cref, and Vref During Propagation-Delay Test

Figure 7 shows the propagation-delay measurement setup presented in a data sheet. When t_{pd} is measured, 50 pF and 500 Ω are connected to ground. Compare the values in Figure 7 (Vref = 0 V, Rref = 500 Ω, and Cref = 50 pF) with corresponding components in Figure 6.

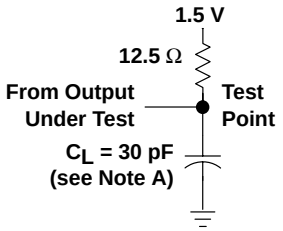


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

Note A. C_L includes probe and jig capacitance.

Figure 7. Data-Sheet Parameter-Measurement Information

Another example is shown in Figure 8 where Vref = 1.5 V, Rref = 12.5 Ω, and Cref = 30 pF.



LOAD CIRCUIT FOR B OUTPUTS

Note A. C_L includes probe and jig capacitance.

Figure 8. Parameter-Measurement Information for GTLP Devices

Vmeas is the voltage at which propagation delay is measured. Vmeas can be found in the parameter-measurement information of a data sheet. In Figure 9, Vmeas is 50% of V_{CC}, as the propagation delay is measured when output voltage is $0.5 \times V_{CC}$.

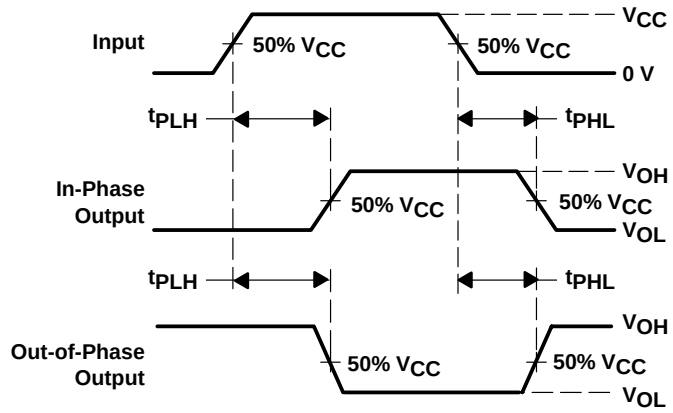


Figure 9. Vmeas in Propagation-Delay Measurement

2.3 3-State Model

The 3-state model is similar to the 2-state output model except that it has the high-impedance state, in addition to high and low states. V-I data at the high-impedance state is needed. In addition to pullup and pulldown data, the 3-state model has ground-clamp and power-clamp data at the high impedance, or Z, state. For 3-state models, the current at high impedance is subtracted from the high-state or low-state current so that the pullup and pulldown data in the IBIS file contains V-I characteristics of only the pullup or pulldown circuit, and high-impedance V-I characteristics are described under the [POWER Clamp] and [GND Clamp] keywords. In Figure 10, a simplified output structure of a 3-state model is shown.

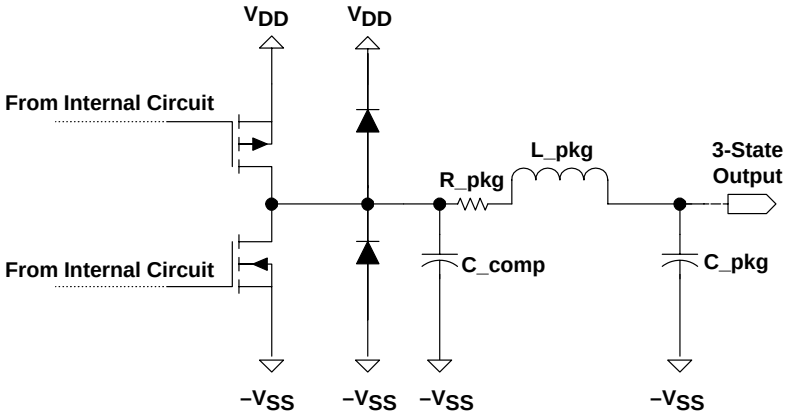


Figure 10. 3-State-Output Model Structure

Unlike the 2-state output model, it is possible to simulate the off condition of both the pullup and pulldown transistors to get V-I data for the clamp diodes. In the IBIS model of a 3-state buffer, pullup and pulldown data does not include the V-I data of the clamp diodes. The EDA simulation software adds the clamp currents to the pullup and pulldown currents.

2.4 Input/Output Model

The input/output model is similar to the 3-state model, but like the input model, Vinl and Vinh keywords are needed to specify the upper and lower thresholds because the pin can act as an input. An input/output buffer is shown in Figure 11.

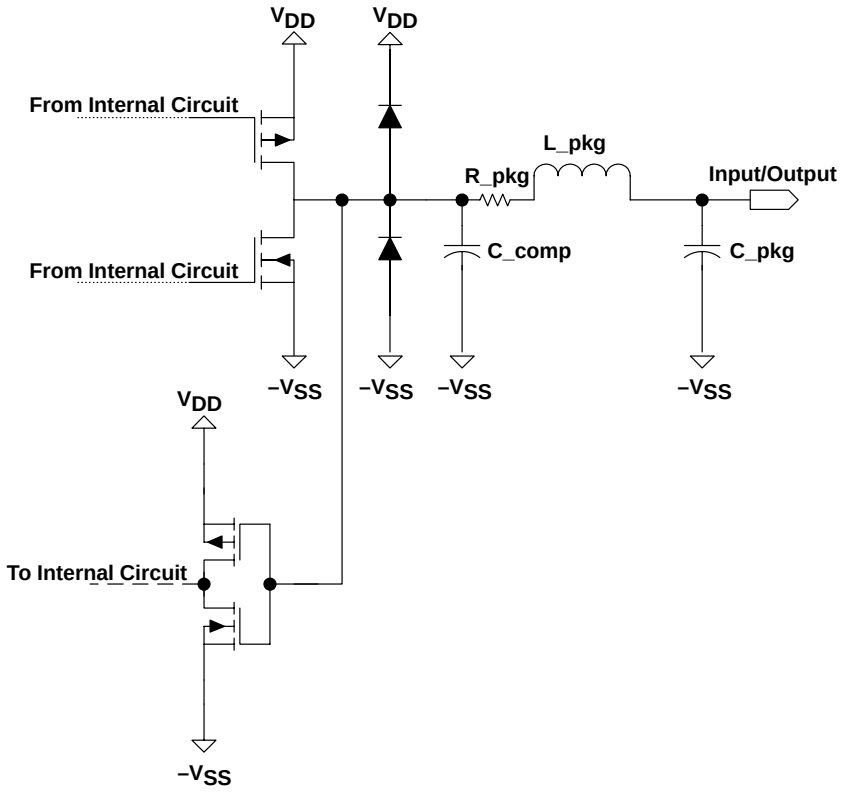


Figure 11. Input/Output Buffer Model Structure

2.5 Open-Drain Model

The open-drain model is similar to the 3-state model, but differs from the 3-state model in the following ways:

- Only pulldown data is needed because there is no pullup circuit.
- Only one set of rising waveform data is taken, with the resistive load connected to V_{CC} or the manufacturer-suggested terminal voltage. Slew rate (dV/dt_r) also is taken from this setup.
- Only one set of falling waveform data is taken, with the resistive load connected to V_{CC} or manufacturer-suggested terminal voltage. Slew rate (dV/dt_f) also is taken from this setup.
- A pullup reference keyword is needed if the manufacturer-suggested terminal voltage is not the same as V_{CC}. The pullup reference, in this case, is the manufacturer-suggested terminal voltage. If not specified, the pullup reference, by default, is V_{CC}.

3 IBIS Creation

The source for IBIS data can be generated from laboratory measurement or SPICE simulation. Simulation is the preferred method because the data is much more accurate. In the simulation, the effect of package parasitics can be excluded from the data and the minimum and maximum data values can be generated. Two types of SPICE net-list are used for creating the IBIS models from simulations: net-list without the parasitic capacitors and resistors, and net-list with parasitic capacitors and resistors. The second type of net-list is generated from the actual layout information and can be used to generate very accurate IBIS data.

3.1 SPICE Simulation Setup for IBIS Data

In SPICE simulation, the net-list of the device is used without any package connected to it. The setup to extract pullup, pulldown, ground clamp, power clamp, and rising and falling waveforms is described in the following paragraphs. The setup to extract ground-clamp and power-clamp data for input pins or control pins is similar to output pins. For output pins, the high-impedance state is created during the extraction of ground-clamp and power-clamp data.

3.1.1 Pullup

The SPICE setup to extract pullup data is shown in Figure 12. Follow this procedure to get the data:

1. Activate output by applying the appropriate signal to the enable pin.
2. Apply an appropriate input voltage to get a high at the output pin.
3. Connect a dc voltage source (V_{PIN}) between the output pin and the pullup reference V_{DD}.
4. Sweep V_{PIN} from $-(2 \times V_{SS} + V_{DD})$ to $(2 \times V_{DD} + V_{SS})$ and print the current value, I (V_{PIN}). (Assume that V_{DD} is the pullup reference and $-V_{SS}$ is the pulldown reference.)

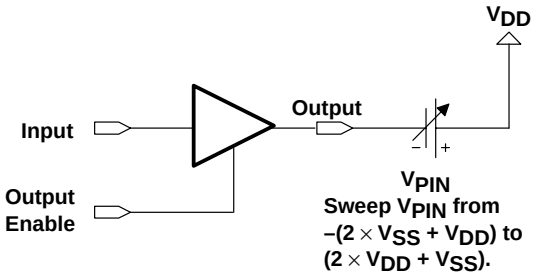


Figure 12. SPICE Setup to Extract Pullup Data

3.1.2 Pulldown

The SPICE setup to extract pulldown data is shown in Figure 13. Follow this procedure to get the data:

1. Activate output by applying the appropriate signal to the enable pin.
2. Apply an appropriate input voltage to get a low at the output pin.
3. Connect dc voltage sources, V_{PIN} and $V_{CURRENT}$ with ground-clamp reference $-V_{SS}$, as shown in Figure 13.

4. Sweep V_{PIN} from $-(2 \times V_{SS} + V_{DD})$ to $(2 \times V_{DD} + V_{SS})$ and print the current value through dc voltage source $V_{CURRENT}$, I ($V_{CURRENT}$). (Assume that V_{DD} is the pullup reference and $-V_{SS}$ is the pulldown reference.)

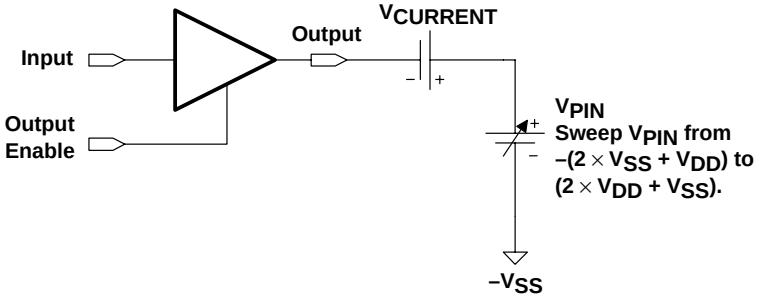


Figure 13. SPICE Setup to Extract Pulldown Data

3.1.3 Ground Clamp

The ground-clamp setup is similar to the pulldown setup, but the output is disabled or deactivated by using the output-enable pin.

The SPICE setup to extract ground-clamp data is the same as the pulldown data (see Figure 13). Follow this procedure to get the data:

1. Disable the output pin by using the output-enable pin, i.e., apply a high if active low or a low if active high.
2. Connect dc voltage sources, V_{PIN} and $V_{CURRENT}$ with ground-clamp reference $-V_{SS}$, as shown in Figure 13.
3. Sweep V_{PIN} from $-(2 \times V_{SS} + V_{DD})$ to $(2 \times V_{DD} + V_{SS})$ and print the current value through dc voltage source $V_{CURRENT}$, I ($V_{CURRENT}$). (Assume that V_{DD} is the pullup reference and $-V_{SS}$ is the pulldown reference.)

3.1.4 Power Clamp

The power-clamp setup is similar to the pullup setup, but the output is disabled or deactivated by using the output-enable pin. The power-clamp test setup is the same for input, 3-state, Input/output, and open-drain models.

The SPICE setup to extract power-clamp data is the same as the pullup data (see Figure 12). Follow this procedure to get the data:

1. Disable the output pin by using the output-enable pin, i.e., apply a high if active low or a low if active high.
2. Connect a dc voltage source (V_{PIN}) between the output pin and the power-clamp reference as shown in Figure 12.
3. Sweep V_{PIN} from $-(2 \times V_{SS} + V_{DD})$ to $(2 \times V_{DD} + V_{SS})$ and print the current value, I (V_{PIN}). (Assume that V_{DD} is the pullup reference and $-V_{SS}$ is the pulldown reference.)

3.1.5 Ramp, Rising, and Falling Waveform Data

3.1.5.1 Rising Waveform for R_fixture Connected to Pullup Reference

The following is the SPICE setup to extract the rising waveform data when the R_fixture is connected to the pullup reference, V_{DD} (see Figure 14). Follow this procedure to get the data:

1. Activate the output by using the enable pin.
2. Apply the appropriate input voltage pulse to get a low-to-high transition at the output pin.
3. Measure the rising slew rate, i.e., dV/dt_r.
4. Take enough data points in the transient simulation so that the voltage waveform becomes stable.

3.1.5.2 Falling Waveform for R_fixture Connected to Pullup Reference

The following is the SPICE setup to extract the falling waveform data, when the R_fixture is connected to the pullup reference, V_{DD}. This setup is similar to the one that extracts the rising waveform data (see Figure 14). The input stimulus is different than that of the rising waveform. Follow this procedure to get the data:

1. Activate the output by using the enable pin.
2. Apply an appropriate input voltage pulse to get a high-to-low transition at the output pin.
3. Take enough data points in the transient simulation so that the voltage waveform becomes stable.

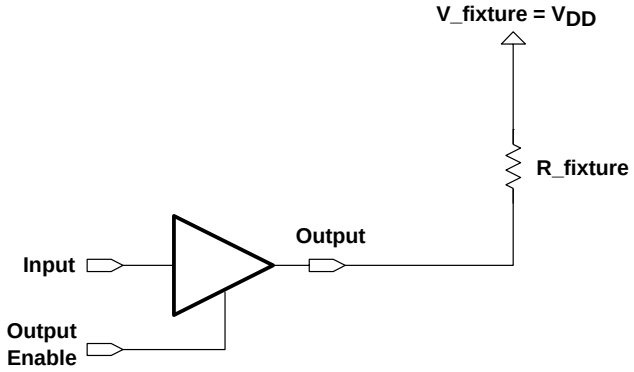


Figure 14. SPICE Setup for V-T data (R_fixture Connected to Pullup Reference)

3.1.5.3 Rising Waveform for R_fixture Connected to Pulldown Reference

The following is the SPICE setup to extract the rising waveform data, when the R_fixture is connected to the pulldown reference, $-V_{SS}$ (see Figure 15). Follow this prcedure to get the data.

1. Activate the output by using the enable pin.
2. Apply an appropriate input voltage pulse to get a low-to-high transition at the output pin.
3. Take enough data points in the transient simulation so that the voltage waveform becomes stable.

3.1.5.4 Falling Waveform for R_fixture Connected to Pulldown Reference

The following is the SPICE setup to extract falling waveform data when the R_fixture is connected to the pulldown reference, $-V_{SS}$. This setup is similar to the one that extracts the rising waveform data (see Figure 15). The input stimulus is different than that of the rising waveform. Follow this procedure to get the data:

1. Activate the output by using the enable pin.

2. Measure the falling slew rate, i.e., dV/dt_f.
3. Apply an appropriate input voltage pulse to get a high-to-low transition at the output pin.
4. Take enough data points in the transient simulation so that the voltage waveform becomes stable.

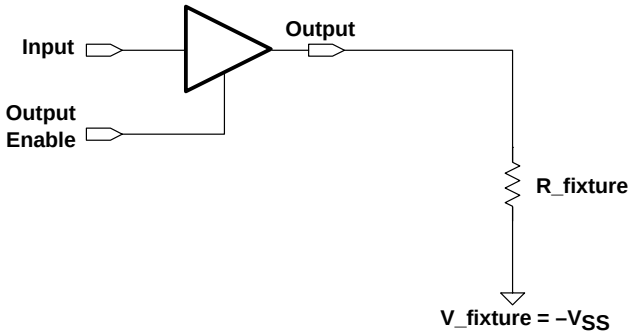


Figure 15. SPICE Setup for V-T Data (R_fixture Connected to Pulldown Reference)

3.1.6 C_comp

The SPICE setup to determine C_comp is similar for the input, 3-state, input/output and open-drain models. In the 3-state, input/output, and open-drain models, the output is disabled while determining C_comp. So, basically C_comp is a 3-state capacitance. For the 2-state output model, because there is no way to disable the output, C_comp is determined by taking the average of the capacitance determined in the high and low states. The SPICE setup to measure C_comp is shown in Figure 16.

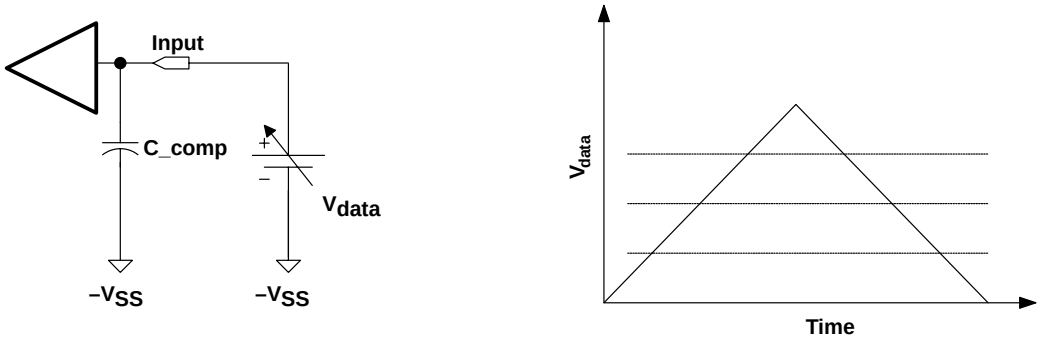


Figure 16. SPICE Setup to Measure C_comp

A slow triangular voltage pulse is applied at the input or output pin and the current is recorded at various points on the voltage pulse (see the V_{data}-versus-time curve in Figure 16). C_comp then is determined from the following formula, and an average is taken.

$$C = \frac{I}{dV/dt}$$

3.2 IBIS File Data Extraction and Formatting

From the SPICE simulation result, the necessary IBIS models for all the pins of a specific device are extracted to create an IBIS file. The number of data points allowed for any set of dc or ac data is 100. Over 1000 data points are generated in dc or ac SPICE simulation. TI uses the “100-best-points algorithm” to choose 100 simulation data from the dc or ac simulation results. This algorithm uses linear interpolation between points and selects the 100 best points that accurately describe the dc or ac behavior, so that when the EDA tool uses these data for simulation, it can get simulation results close to SPICE.

The appropriate mathematical operation is done before putting this data in the IBIS file. For example, for a 3-state model, the power-clamp current is subtracted from the pullup data and the ground-clamp data is subtracted from the pulldown data. Data for all models are extracted from SPICE simulations.

The IBIS file contains the lumped R, L, and C values for the package. These data are combined with the extracted data from simulations, formatted according to the latest IBIS specifications, and put together in one file.

4 IBIS File Validation

After creating an IBIS file for a device, the file undergoes a validation procedure to ensure that the customer gets the most accurate IBIS model. TI follows a strict validation procedure. The following is a concise summary of validation checks.

- In all packages, a model for every electrically different pin, and models for all possible V_{CC} ranges are included.
- Passes data-sheet parameters V_{OH}, V_{OL}, I_i, $I_{i(hold)}$, etc.
- No errors are generated when the file is checked, using the latest IBISCHK.
- All warnings are documented in the notes section, with an explanation.
- V-I curves must be monotonic. If they are nonmonotonic, the reason for nonmonotonocity should be explained in the notes section of the IBIS file. For example, due to the feedback circuit, the input of bus-hold devices exhibits nonmonotonocity in the ground-clamp curve.
- All of the dc curves pass through the origin (0 mA at 0 V).
- The entire V-T curve has full swings, and rise and fall time is compatible with the data sheet.
- If the device has balanced propagation delay ($t_{PLH} = t_{PHL}$), the time to reach the threshold voltage in the rising and the falling waveforms should be equal.
- Electrostatic discharge (ESD) diode characteristics in the ground-clamp and the power-clamp data agree with the device characteristics.
- It contains all the necessary parameters, keywords, etc., as described in IBIS Specification 3.2.
- The IBIS file contains the nominal, weak, and strong data over the entire recommended V_{CC}, temperature, and process range.

5 Visual Check of IBIS Waveform

A visual check of IBIS waveforms can give a quick idea about the accuracy of that model. In the following paragraphs, examples of a dc (pullup, pulldown, ground clamp, and power clamp) and an ac waveform (rising and falling) in an IBIS file are shown. The waveforms were captured using the Visual IBIS Editor, which is a free tool provided by INNOVEDA™ . Each set of waveforms shows characteristics at typical, minimum, and maximum condition. Typical data is taken at nominal V_{CC}, nominal temperature, and nominal process. Minimum data is taken at minimum V_{CC}, weak process, and at a temperature that will generate the worst performance data. Maximum data is taken at maximum V_{CC}, strong process, and at a temperature that will generate the best performance data.

5.1 Pullup Waveforms

An example of pullup waveforms is shown in Figure 17. The V_{OH}-I_{OH} data from the device data sheet can be compared with the pullup curve. For example, if the data sheet says that I_{OH} = – 8 mA for V_{OH} (minimum) is 2 V at V_{CC} = 3 V, the equivalent voltage to look at the pullup waveform is V = 3 – 2 =1 V. If, on the pullup waveform, at V =1 V, the absolute magnitude of minimum pullup current (taken at V_{CC} = 3 V) is greater than or equal to 8 mA, the data are correct.

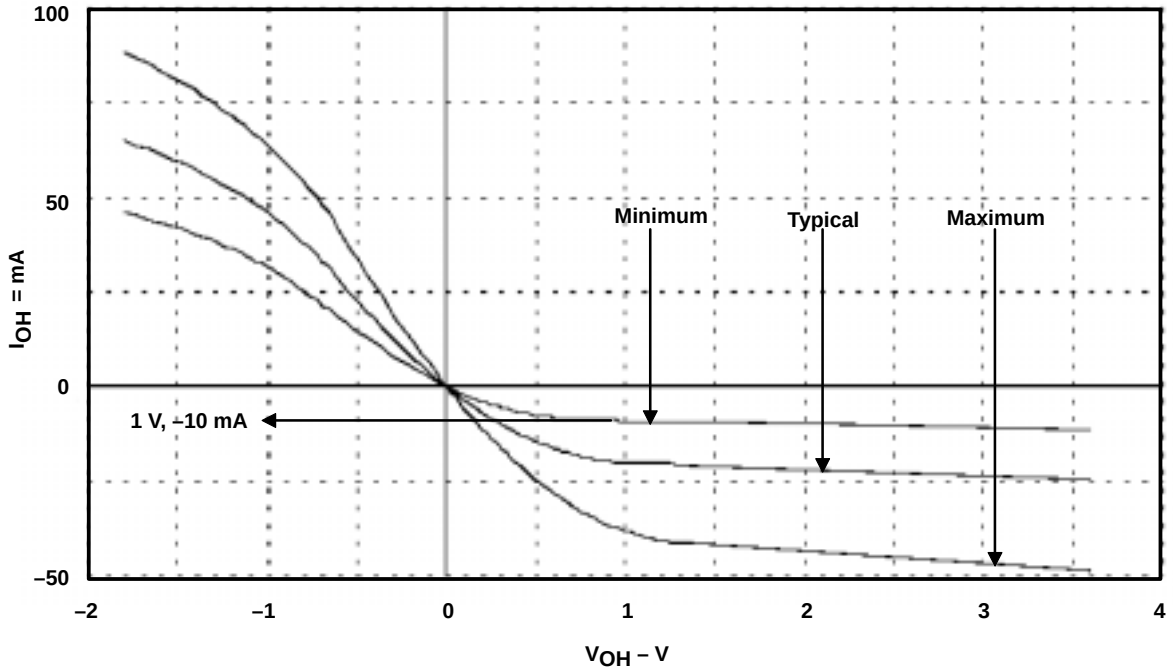


Figure 17. Pullup Waveforms

5.2 Pulldown Waveforms

An example of pulldown waveforms is shown in Figure 18. The V_{OL}-I_{OL} data from the device data sheet can be compared with the pulldown curve. For example, if the data sheet says that I_{OL} = 10 mA for V_{OL} (maximum) is 0.55 V at V_{CC} = 3 V, the equivalent voltage to look at the pulldown waveform is V = 0.55 V. If, on the pulldown waveform, at V = 0.55 V, the absolute magnitude of minimum pulldown current (taken at V_{CC} = 3.0 V) is greater than or equal to 10 mA, the data are correct. Typical and maximum pulldown current also should be greater than 10 mA.

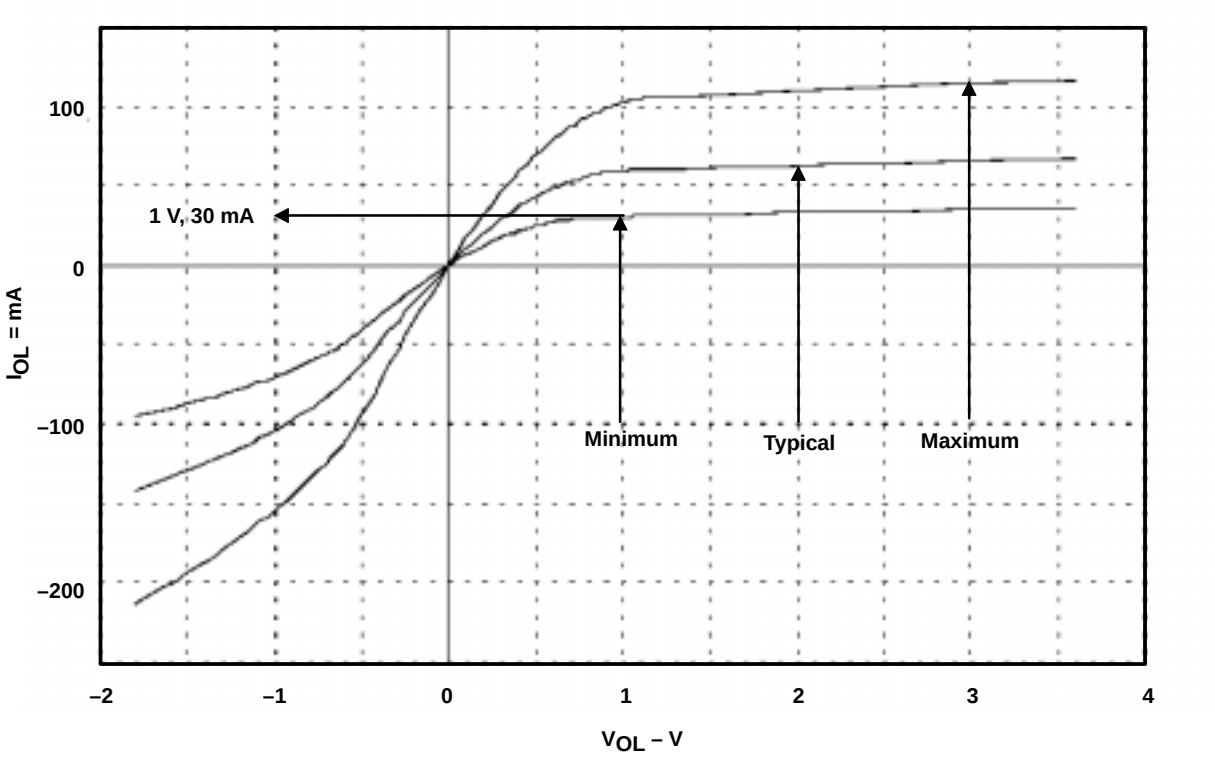


Figure 18. Pulldown Waveforms

Pullup and pulldown waveforms may have different shapes than those shown in Figures 17 and 18. Due to the presence of some special circuits, pullup waveforms may be different. For example, overvoltage-tolerant circuits can cause the current in the negative voltage region to decrease as the voltage becomes more negative. Damping resistors can cause the current in the positive-voltage region to become less negative as the voltage increases. Due to the presence of dynamic output control circuits, there may be a large increase in the slope of the curve in the positive-voltage region. Similarly, the pulldown waveforms can show different shapes, due to presence of special circuits.

5.3 Rising Waveforms

An example of a rising waveform is shown in Figure 19. Rising waveforms should have rail-to-rail swing, and the rise time should be less than or equal to the data-sheet value, if R_fixture in the IBIS file is the same or greater than the data-sheet resistive load.

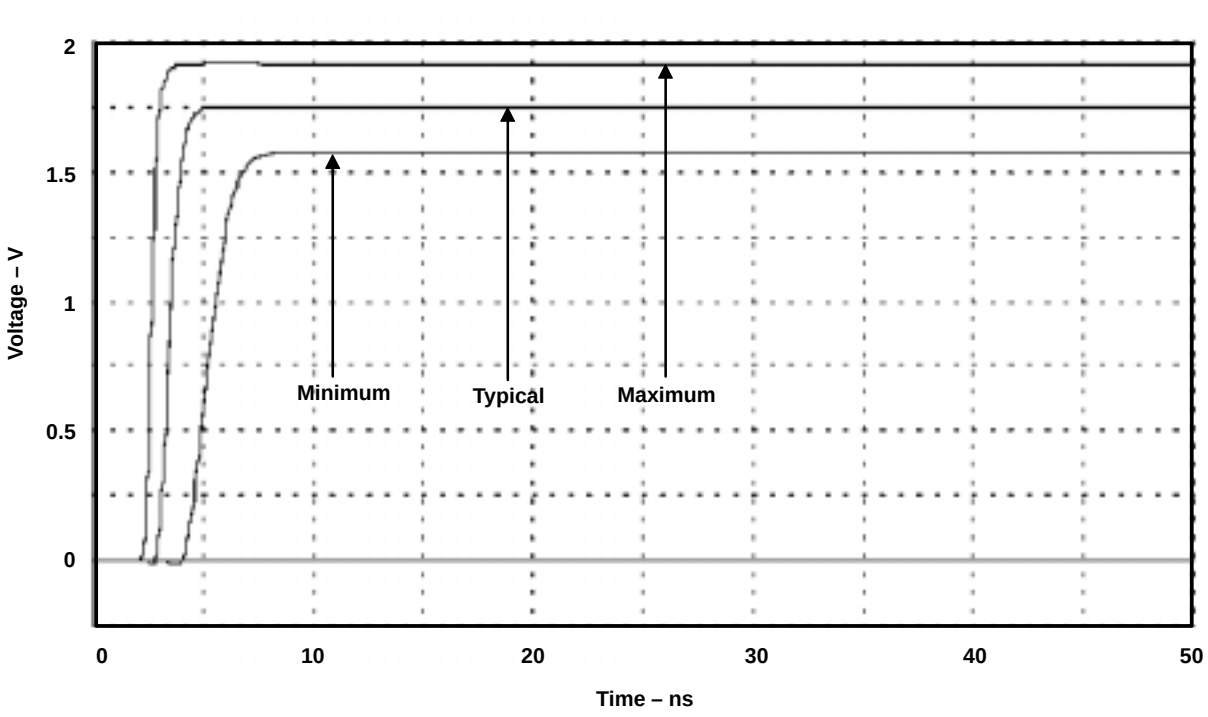


Figure 19. Rising Waveforms

5.4 Falling Waveforms

An example of a falling waveform is shown in Figure 20. Falling waveforms should have the rail-to-rail swing, and the fall time should be less than or equal to the data-sheet value, if R_fixture in the IBIS file is the same or greater than the data-sheet resistive load.

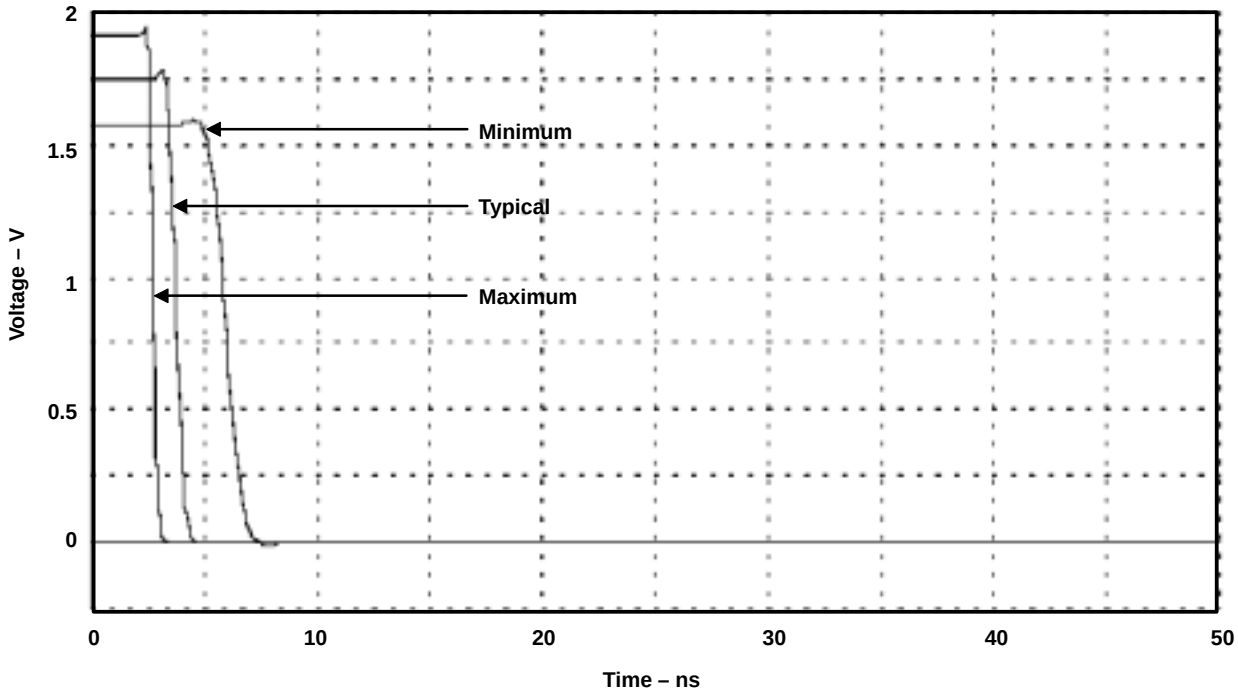


Figure 20. Falling Waveforms

5.5 Ground-Clamp Waveforms

An example of the ground-clamp waveforms is shown in Figure 21. Some devices may have a diode connected between the input and ground or between the output and ground. Ground-clamp waveforms describe the V-I characteristics of those diodes. Sometimes there are V_{ik}-I_{ik} data in a data sheet. In that case, the absolute magnitude of ground-clamp current at $V = V_{ik}$ should be equal to or greater than I_{ik}. For example, if V_{ik}= –1.2 V and I_{ik} = –18 mA, on the waveform at $V = V_{ik}$, the absolute magnitude of the current should be greater than or equal to 18 mA.

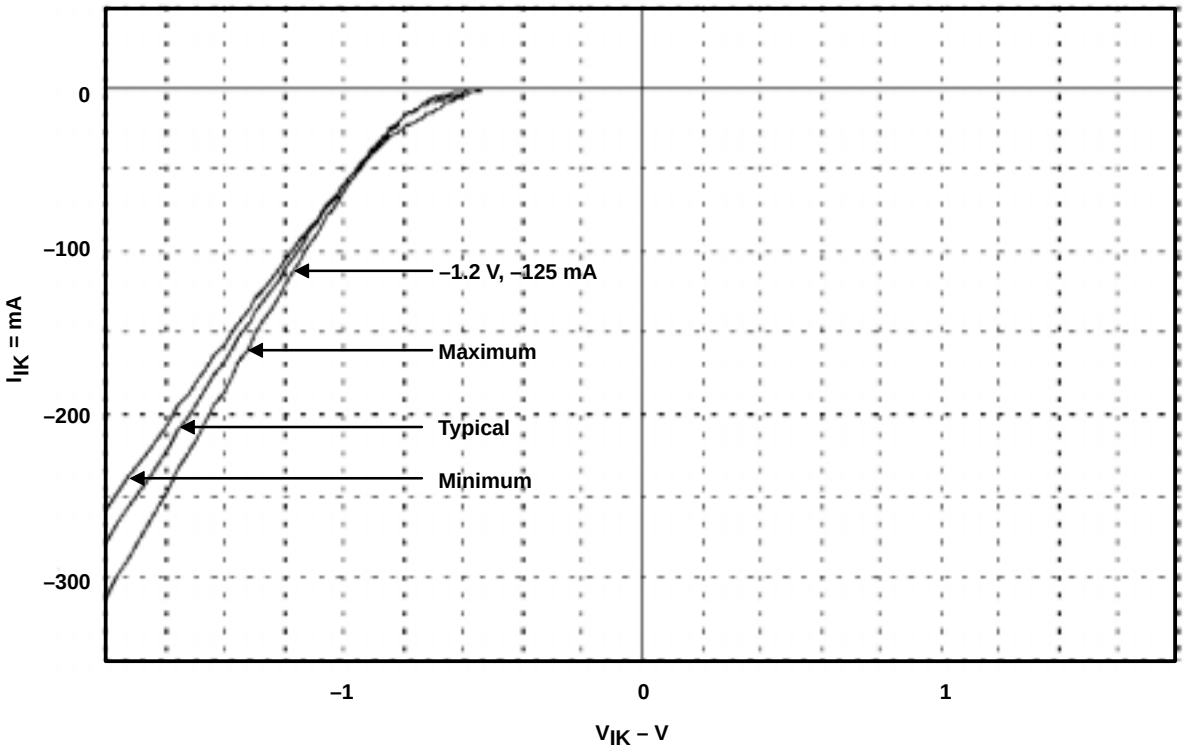


Figure 21. Ground-Clamp Waveforms

5.6 Bus-Hold Behavior in Ground-Clamp Data

If the device has bus hold at the input, the input ground-clamp waveforms should be an S shape in the voltage range between 0 and V_{CC} (see Figure 22). The voltage/current relationship should match the data-sheet V_i and $I_{i(hold)}$ data. If the data sheet is specified at V_i = 0.8 V, minimum $I_{i(hold)}$ 75 μA, the current at V = 0.8 V on the ground-clamp waveform should be at least 75 μA.

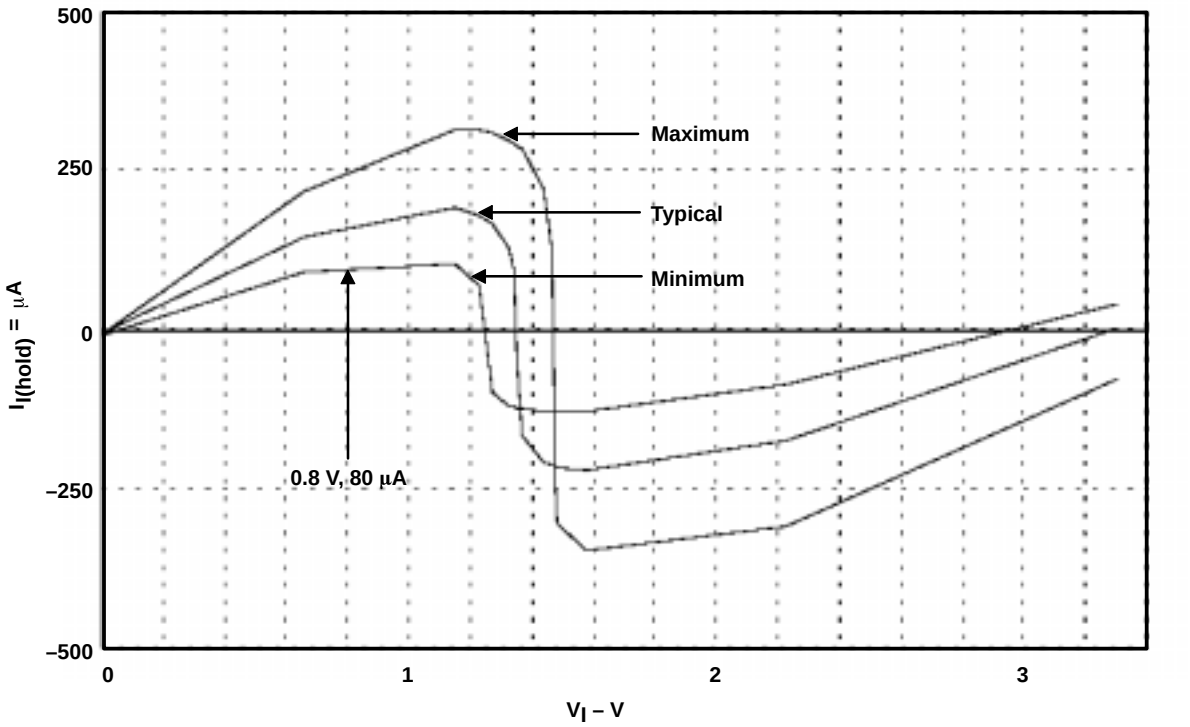


Figure 22. Bus-Hold Behavior in Ground-Clamp Data

5.7 Power-Clamp Waveforms

An example of power-clamp waveforms is shown in Figure 23. Some devices may have a diode connected between the input and V_{CC} or between the output and V_{CC}. If the device has a diode, the power-clamp waveform should exhibit the V-I characteristics of the diode.

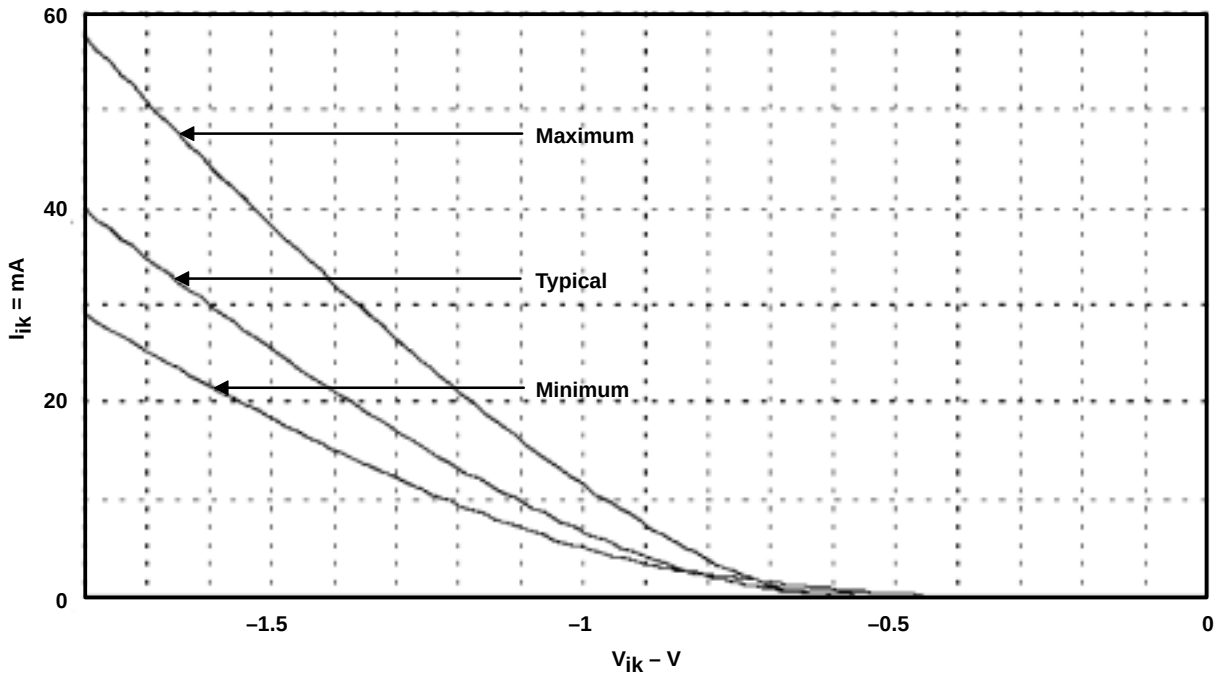


Figure 23. Power-Clamp Waveforms

6 IBIS File Warnings and Errors

The IBIS file is checked using a parser to ensure that the syntax is correct. This parser is called IBISCHK and can be downloaded from the official IBIS homepage. In the following paragraphs, some common warnings and errors are discussed, along with the reasons for those warnings and errors. Validation ensures that there is no error and all warnings are documented in the notes section of IBIS file. In case of any warning or error, customers can consult the notes section in IBIS file and contact TI customer service.

- Some warnings may be generated due to device characteristics. The following are some examples.
  - WARNING (line n0) - GND Clamp Minimum data is non-monotonic.

    Non-monotonic data in ground-clamp may be due to special circuits. For example, due to the bus-hold circuit, a ground-clamp waveform can exhibit non-monotonicity. There should be a note in the notes section of the IBIS file explaining the cause of non-monotonicity.
  - WARNING (line n1) - Pullup Minimum data is non-monotonic.

    Non-monotonic data in pullup may be due to a damping resistor, an over-voltage protection circuit, or dynamic output control circuit. There should be a note in the notes section of the IBIS file explaining the cause of non-monotonicity.

  - WARNING (line n2) - Pulldown Minimum data is non-monotonic.

    Non-monotonic data in pulldown may be due to the dynamic output control circuit or any feedback circuit at the output. There should be a note in the notes section of the IBIS file explaining the cause of non-monotonicity.

- The following are some examples of warnings and errors that may be generated due to inaccurate IBIS data or incorrect syntax.
  - WARNING (line n1) – Typ value is not in between Min and Max.

    Package typical data may be wrong.
  - ERROR – Component ’ALVCH16373_DGG’: Model ’ALVCH16373_OUT’ for Pin ’2’ not defined.

    The model for pin 2 in the pin section of the IBIS file is not defined in the IBIS file.
  - ERROR – Model ’ALVCH16373_IN_33’ in Model Selector ’ALVCH16373_IN’ is not defined in the file.

    The model described in the model section under the “Model Selector” keyword is not defined in the IBIS file.
  - WARNING – Model ’ALVCH16373_LEIN_25’: Model_type ’Input’ must have V_{inl} set.
  - WARNING – Model ’ALVCH16373_LEIN_25’: Model_type ’Input’ must have V_{inh} set.

    The threshold parameter value (V_{il} and V_{ih} in the datasheet) is missing from the input model.
  - WARNING – Model ’ALVCH16373_OUT_33’: TYP VI curves cannot drive through Vmeas = 1.5 V given load Rref = 5 ohms to Vref = 0 V.

    This warning is generated when the pullup and pulldown current is not enough to drive the load Rref up to Vmeas. Rref may be too small or Vmeas may be too high. If these are correct, but the warning remains, then the pullup and pulldown data may be incorrect. V–T data, if not allowed to settle down to a stable value, can generate this warning.
  - WARNING – Model ‘ALVCH16373_OUT_33’: Pulldown has Decreasing Current.

    The pulldown characteristics may be wrong. Pulldown should be increasing from negative voltage up to positive voltage. Simulation setup may be wrong.
  - ERROR (line n2) – Exceeds 80 characters.

    In an IBIS file, the total number of characters in a line should not exceed 80. Most often, this error is due to difference in end-of-line characters in a different platform. For example, an IBIS file created in the windows platform may have this error if it is downloaded in the UNIX platform, as UNIX adds an end-of-line character at the end of each line in the IBIS file. The file can be converted to use in UNIX by ‘dos2unix’ command.

- ERROR – Model ‘ALVCH16373_OUT_33’: The [Falling Waveform] with [R_fixture]=500 Ohms and [V_fixture_min]=3V has MIN column DC endpoints of 0.55V and 3.00v, but an equivalent load applied to the model’s I–V tables yields different voltages (0.05V and 3.00V), a difference of 963.74% and 0.01%, respectively.

  The error is due to dc and ac data mismatch. The end point of the voltage-time data is not the same as the dc data. For example, if the end point in the falling waveform is 0.55, then with R_fixture = 500 the current through R_fixture is determined. This current should represent the same voltage of 0.55 in the pulldown table. Most of the time this warning is generated when the simulation data are not taken for a sufficient time, i.e., until the voltage waveform settled to a stable value. Sometimes, the warning may be generated because the rising and falling waveform does not contain the full rail-to-rail switching.

  If the percentage difference in voltage is less than a certain value, the error can come up as a warning. If the difference is negligible it does not significantly affect the accuracy. An IBIS model created from an actual laboratory measurement can cause this warning.

- ERROR (line n3) – File name opened ’scem259.ibs’ not the same as File_name ’sn74auc16245.ibs’

  The name of the IBIS file should be the same name as described under “File Name” keyword in the IBIS file.

  TI provides two different formats of the IBIS file, one with the .ibs extension and the other with the zip extension. The .ibs file has to be renamed similar to the file name described under (File Name) keyword in the IBIS file. The .zip file is the compressed version of the .ibs file. It can be uncompressed and the IBIS file can be used directly without renaming the file.

7 IBIS File Distribution

If the IBIS model passes validation, it is sent to an external TI website. IBIS models can be obtained by accessing http://www.ti.com.

8 Resources

The IBIS open forum is a working group of the EIA association and, as such is responsible for the official IBIS specification. The official website for provides information on IBIS, articles, free tools, and models.

9 References

1. *Introduction to IBIS Models* – Arpad Muranyi, Signal Integrity Engineering, Intel Corporation.
2. *I/O Buffer Information Specification,* Version 3.2, IBIS Committee.
3. *I/O Buffer Modeling Cookbook*, IBIS Open Forum.
4. *Star-HSPICE Manua*l, Release 1999.2, Avanti Corporation.
5. *Innoveda Visual IBIS Editor,* Version 3, www.innoveda.com

Appendix A Using IBIS Model in HSPICE Simulation

```
*An IBIS test file.

*********|*********|*********|*********|*********|*********|********|*********|

.OPTIONS search='./'
.OPTIONS POST=2                 $ Enables HSPLOT interface
.OPTIONS ACCT OPTS              $ Prints stats & option values used
.OPTIONS SPICE=1                $ Forces Berkeley compatibility
.OPTIONS GMIN=1E-10             $ Lowest allowable conductance values
.OPTIONS GMINDC=1E-10           $ A conductance in parallel w/ PN junctions
.OPTIONS ITL1=400               $ Maximum DC iteration limit
.OPTIONS ITL4=40                $ Maximum transient iterations/timestep
.OPTIONS ITL5=0                 $ No limit to total transient iterations
.TEMP    25                     $ Nominal temperature
.OPTIONS LIST NODE PROBE

********************TYPICAL CONDITION**********************

*********DRIVER************************

b_io                            *Buffer call ---must start with "b"*
+nd_pu                          *Power supply to pullup*
+nd_pd                          *GND supply to pulldown*
+nd_out                         *Output node*
+nd_in                          *Input node ---A voltage source must be connected
+nd_en_driver                   *Enable input**
+v_out_of_in                    *This is used by the hspice-- no voltage source should
                                *be connected to this node. This is used when the I/O
                                *model works as an input model. This voltage source
                                *can be monitored to see when
                                *the input signal crosses the
                                *Vinl and Vinh level. This voltage source produces a 1
                                *or 0 based on the input signal.
+nd_pc                          *power supply to power clamp*
+nd_gc                          *GND supply to ground clamp*
+file='sn74lvc245a.ibs'         *name of the ibis file. The name of the ibis file
                                *should match the file name under the 'File Name'
                                *keyword in the IBIS file
+model='LVC245A_IO_33           *Model name*
+typ=typ                        *typical,min or max condition**
+power=on                       *power on-hspice will take the power from Ibis file,
                                *If off then connect voltage source to
                                *pullup,pulldown,gnd_clamp,power_clamp
+buffer=3                       *buffer type 3 for I/O **
*+xv_pu=nd_state_pu             *These two nodes are used to monitor exactly how the
*+xv_pd=nd_state_pd             *transition is taking place. The state of these two
                                *node changes from 0 to 1 or vice versa during the
                                *transition.
+interpol=1                     *1=linear, 2=quadratic bi-spline. TI uses linear
                                *interpolation when creating IBIS file
+ramp_fwf=2                    *Defines which falling waveform data to use
                                *If 0 then uses the dv/dt_f data, default 0
                                *If 1 then uses the first falling waveform data
                                *If 2 then uses both sets of falling waveform data
+ramp_rwf=2                    *Defines which rising waveform data to use
                                *If  0  then uses the dv/dt_r data, default 0
                                *If 1 then uses the first rising waveform data and
                                *If 2 then both sets of rising waveform data and

*+rwf_tune=                    *Tuning parameter. Used when ramp_rwf=0 or 1. This
                                *parameter is a value between 0 and 1 and used in
                                *conjunction with dv/dt_r in the IBIS model to
                                *determine the time when the pulldown circuit
                                *switches *from ON to OFF. Use ramp_rwf=2 and this
```

```
                                *parameter is unused.

*+fwf_tune=                     *Tuning parameter. Used when ramp_fwf=0 or 1. This
                                *parameter is a value between 0 and 1 and used in
                                *conjunction with dv/dt_f in the IBIS model to
                                *determine the time when the pullup circuit
                                *switches from ON to OFF. Use ramp_fwf=2 and this
                                *is unused

*+nowarn                        *suppresses warning messages



****PKG CONNECTION***
CPKG nd_out 0       2.19870E-13*HSPICE simulator does not connect the pkg data with
LPKG driver_out cen 4.31600E-09*the IBIS model. Connect the package R, L and C data.
RPKG cen nd_out     6.00971E-02

*****************************************



****LOAD ****TRANSMISSION  LINE*****

TLOAD driver_out 0 lineend 0  ZO=50  TD=5.81ns  L=1.3769


****TERMINATION*****

Rpu     lineend tt 50
Vterm    tt 0   dc 3.3

.tran  0.1ns 245ns

*********TRANSIENT ANALYSIS**********

Vin     nd_in 0 PULSE  0  1  6.07n 0n 0n 123n 240n

Ven1    nd_en_driver    0 dc 0v                         **ACTIVE LOW***

.print tran V(driver_out) V(nd_in)

*************************************

.END
```

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