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A complete low voltage analog lock-in amplifier to recover sensor signals buried in noise for embedded applications

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Abstract

This paper presents a low-voltage 3V single supply analog lock-in amplifier (LIA) for processing small AC sensor signals buried in noise, including those presenting a relative phase with respect to the reference signal. Reference and bias sensor signals are provided by a quadrature oscillator. Experimental results confirm the capability of the proposed lock-in amplifier to effectively recover information from signal to noise ratios below 0.025, with an error below 9%.

Keywords: Lock-in amplifier; phase-shift detector; condictioning electronics; sensor signal conditioning

1. Introduction

In some conditions, sensor output signals can be some orders of magnitude smaller than the present electrical noise level. In those cases, linear filtering is not a suitable choice to extract signal information, making necessary the use of other techniques. An interesting possibility is the employment of lock-in amplifiers [1]–[3], which use the phase-sensitive detection technique (PSD) to single out the data signal at a specific reference frequency. In PSD-based systems, noise signals at frequencies other than the reference signal are rejected, and thus do not significantly affect the desired signal information.

PSD techniques are basically based on the synchronous rectification of the data signal (Fig. 1), according to a control signal that selects the amplification sign. When data and control signals have the same frequency and phase values, the data signal is full-wave rectified at the output. By using a low-pass filter to obtain the average value of the processed signal, noise is cancelled and the signal information is recovered. This technique requires a perfect match in the frequency and phase values of data and control signals. Thus, if the data signal is provided by a device that can shift the phase value, such as capacitive sensors, this solution is not the best option. In this case, phase dependency can be eliminated by adding a second lock-in amplifier branch which operation is controlled by a

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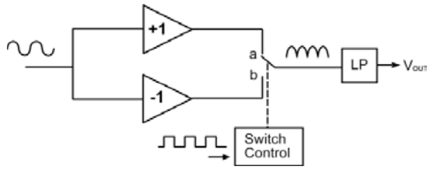


Fig. 1: Digitally switched analog mixer, and the low-pass filter that provides the data signal average value

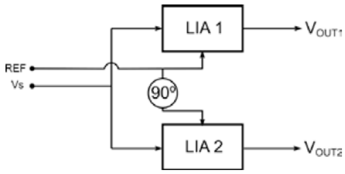


Fig. 2: Dual-phase lock-in block diagram

second control signal shifted 90 degrees [4], as shown in the block diagram of Fig. 2. If θ is the phase shift between the control signal V_{ref} in LIA1 and data signal V_s, the average voltage values V_{out1} and V_{out2} are given by:

$$V_{OUT1} = \frac{2A\cos(\theta)}{\pi}; \quad V_{OUT2} = \frac{2A\cos(\theta+90)}{\pi} = \frac{2A\sin(\theta)}{\pi} \tag{1}$$

Where A is the amplitude of the sensor signal V_S. In this way, the recovered output amplitude is given by:

$$A = \frac{\pi}{2}\sqrt{V_{OUT1}^{\,2} + V_{OUT2}^{\,2}} \tag{2}$$

Currently, analogue lock-in amplifiers are designed using dual power supplies [5]-[6], thus limiting their application in portable systems, as battery-operated wireless sensing networks [7]. In these systems, whose energy is usually provided by two 1.5 V batteries, it is necessary to design the processing elements working in single supply operation. This work presents the design and test of a PSD-based conditioning circuit for sensor signal processing in battery-operated small form-factor applications. This system is suitable to process sensor signals, properly recovering the information for signal to noise levels below 0.05 (noise levels up to 20 times higher than the data amplitude).

2. PSD-based System

Fig. 3a shows the proposed system block scheme. Due to the use of the proposed system in battery-operated applications, it is necessary to center the data signals in the middle of the supply range. In this case, the system has been designed to operate at 3 V, thus centering the data signals adding a 1.5 V offset (Fig. 4a).

The developed lock-in conditioning system consists of a quadrature oscillator and two parallel PSD, that eliminate the system phase dependence [3], thus enabling its use for both resistive and capacitive sensors. The variable frequency quadrature oscillator (Fig. 3b) consists of two integrators and an inverter amplifier. The oscillator provides two 140 Hz sinusoidal waves with 90 degrees of phase shift and 1.5V DC level. The signals provided by the oscillator are used as exciting sensor signal and inputs for two comparators that provide the square waves that control the mixers operation. The need of a DC offset level in the data signal due to the single supply operation requires modifying the mixer operation. Fig. 4b shows the mixer architecture and its operation, given by:

$$V_o = \begin{cases} (V_{in} - 0) & if \quad V_{in} > 1.5V \\ (3 - V_{in}) & if \quad V_{in} < 1.5V \end{cases} \tag{3}$$

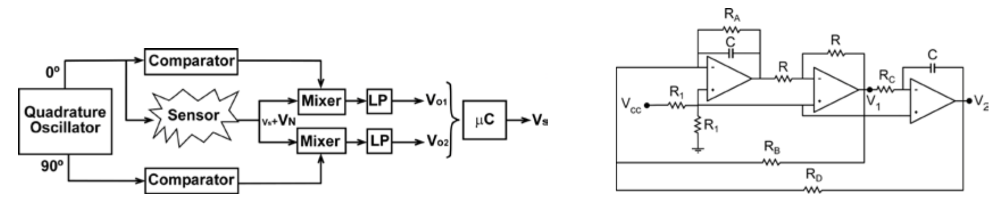
where V_o is the output of the block and V_{in} is the signal to be processed. The resulting output voltage is shown in Fig. 4c. In the lock-in amplifier branches (Fig. 3a) the resulting signals are low-pass filtered by RC circuits, with a cutoff frequency of 1 Hz, giving the average values according to (1), plus the 1.5 V additional DC offset level. The resulting DC signals V_{01} and V_{02} can be processed by a microcontroller, obtaining the noise-free amplitude A of the signal provided by the sensor according to:

$$A = \frac{\pi}{2}\sqrt{\left(V_{01} - 1.5V\right)^2 + \left(V_{02} - 1.5V\right)^2} \qquad (4)$$

The experimental characterization of the structure has been performed using commercial ICs. Fig. 5 shows a photograph of the tested prototype. To simulate the behavior of the sensor in a controllable low SNR environment we used an USB6212 DAQ board from NI [8]. In this work, the SNR is defined as:

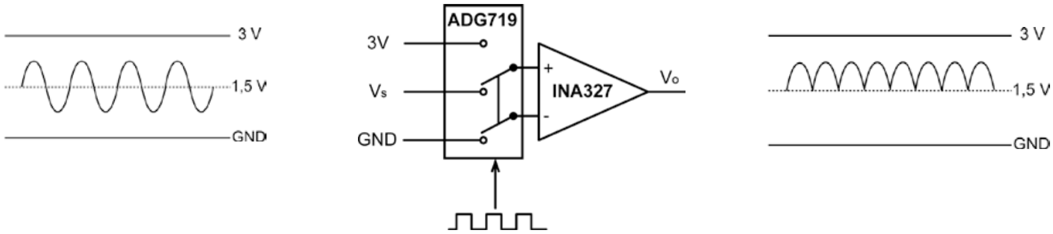
$$SNR = \frac{A_{SIGNAL}}{A_{NOISE}} \qquad (5)$$

The designed LIA system ability to recover information from signals buried in noise has been evaluated. Fig. 6 shows the error achieved in the recovery of the noise-free amplitude of the sensor for different noise levels. In Fig 6a data signal is masked with a white noise; as we can see, measurement errors are below 9% for SNR up to 0.025 (noise levels 40 times higher than the signal amplitude). Fig 6b shows the errors in signal amplitude recovery for a sinusoidal signal contamination at two different frequencies (50 Hz and 100 Hz). The system behavior is appropriate for a 50 Hz noise frequency, while degrading its performance for the 100 Hz noise signal, mainly due to the closeness of the noise and reference frequencies.



(a) (b)

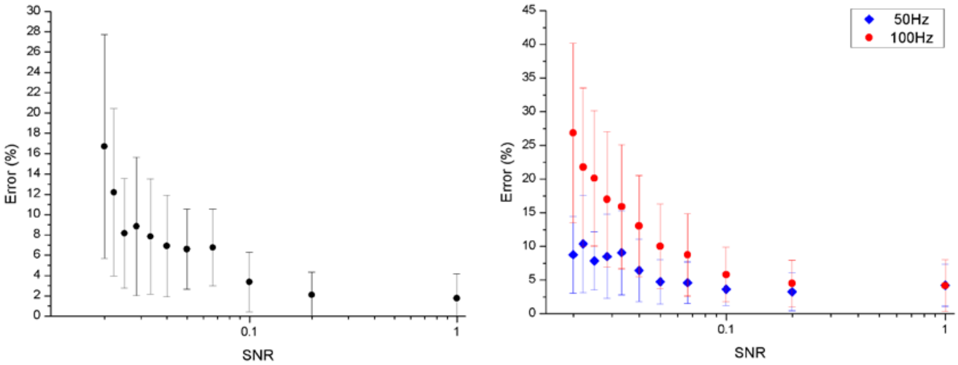
Fig. 3: (a) Block scheme of the proposed lock-in system; (b) Quadrature oscillator. V_1 and V_2 are the 90º phase shifted control signals



(a) (b) (c)

Fig. 4: (a) Input signal to the mixer; (b) Signal mixer; (c) Rectified output signal

Fig. 5:Compact lock-in amplifier prototype made with SMD components



(a) (b)

Fig. 6: Errors in the estimation of the signal amplitude for different SNR. (a) White noise contamination; (b) Sinusoidal contamination at a fixed frequency

3. Conclusions

This paper presents a complete single supply lock-in amplifier targeting a processing system for embedded applications in low SNR environments. It has the ability to process data signals provided by sensors that shift the signal phase value, such as capacitive sensors.

Experimental measurements have confirmed the capability of the proposed lock-in system to recover signals with low SNR level (> 0.025) whit errors below 9%.

Using commercial components, the analog amplifier has been designed according to power requirements in portable applications. The power consumption of the system (19 mW) is mainly due to the instrumentation amplifiers in the signal mixers: The amplifier must present a true input rail-to-rail characteristic, which currently penalizes the power consumption. Currently we are working in the design of a monolithic version, powered by a low single supply voltage in a standard low-cost 1.8V-0.18 μm CMOS technology.

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