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A CMOS vector lock-in amplifier for sensor applications

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ABSTRACT

The design of an integrated lock-in amplifier is discussed, specifically conceived for the detection of low-level signals at a harmonic of the drive frequency in magnetically excited resonant structures. The circuit includes in-phase and quadrature analogue signal processing channels, whose outputs feed an integrated $\Sigma\Delta$ analogue to digital converter. The circuit can be operated in different configurations, depending on the application requirements: in particular, by combining the digitized outputs of the two channels, vector operation can be obtained. The entire analogue chain, including the $\Sigma\Delta$ modulator, was designed using fully differential elaboration. The circuit was developed in a 0.35 μm, dual poly-Si, four metal layers analogue CMOS technology with high resistivity poly-Si option. Circuit performance is discussed on the basis of transistor-level simulations and measurement results.

1. Introduction

Resonant sensors consist of a mechanical resonator, typically implemented using MEMS technologies, and of the associated excitation and readout electronics. The measurand (a force, a temperature, a concentration, etc.) modifies the mechanical properties of the resonator, and thus its resonance frequency. Determination of the resonance frequency requires a drive mechanism for exciting the mechanical oscillation, a suitable technique to detect the amplitude of the oscillation and a control system continuously sweeping the drive frequency until the maximum amplitude of oscillation is found. Since the level of the detected signal is low, synchronous detection, using the drive signal as a reference, becomes attractive. Implementations of integrated lock-in amplifiers suitable for sensor applications are reported in [1,2]. Conventional single-channel lock-in amplifiers, however, require adjusting the phase delay of the reference channel when the geometrical arrangement of the resonator is modified, in order to ensure maximum sensitivity. A lock-in capable of vector operation, directly providing the magnitude of the detected signal, would not require any phase adjustment.

Recently, the advantages of synchronous detection at the second or third harmonic of the excitation frequency were demonstrated for the detection of resonance in cantilevers stimulated by electrostatic forces [3].

Signal detection at harmonics of the excitation frequency turns out to be attractive also in the case of oscillations excited by magnetic forces. In fact, mechanical resonance can be excited in a conductive, non-magnetic beam using a contact-less setup, where an external coil generates a magnetic field at frequency f_e that induces eddy currents in the beam. The interaction between the magnetic field and the currents causes Lorentz forces at frequency $2f_e$. By adjusting f_e, the structure can be brought into mechanical resonance.

Different approaches were reported for contact-less, magnetic readout of the resonance. A sensing coil in proximity of the vibrating beam [4], Fig. 1(a), collects a linked flux at frequency f_e, generated by the eddy currents, modulated by the mechanical displacement at $2f_e$. This gives rise to an e.m.f. at $3f_e$ in the sensing coil, whose amplitude peaks at the mechanical resonance frequency f_m, i.e. when $f_m = 2f_e$. In the following, we shall refer to this sensing scheme as *base-band probing*, since the sensing coil signal is in the base band. In another setup, hereafter called *HF probing*, a sinusoidal probing current of much higher frequency f_p is superimposed to the excitation current at f_e [5], see Fig. 1(b). The probing current excites eddy currents also at f_p, but does not induce appreciable vibrations, due to its high frequency. Thus, a properly placed sensing coil collects a linked flux contribution, generated by the eddy currents at frequency f_p, that is modulated by the mechanical displacement at $2f_e$, and gives rise to an e.m.f. contribution at $f_p \pm 2f_e$.

For both readout schemes, synchronous detection can be conveniently applied to extract the resonance information. In the case of base-band probing, a vector lock-in amplifier with reference input at frequency $3f_e$ can be used to determine the

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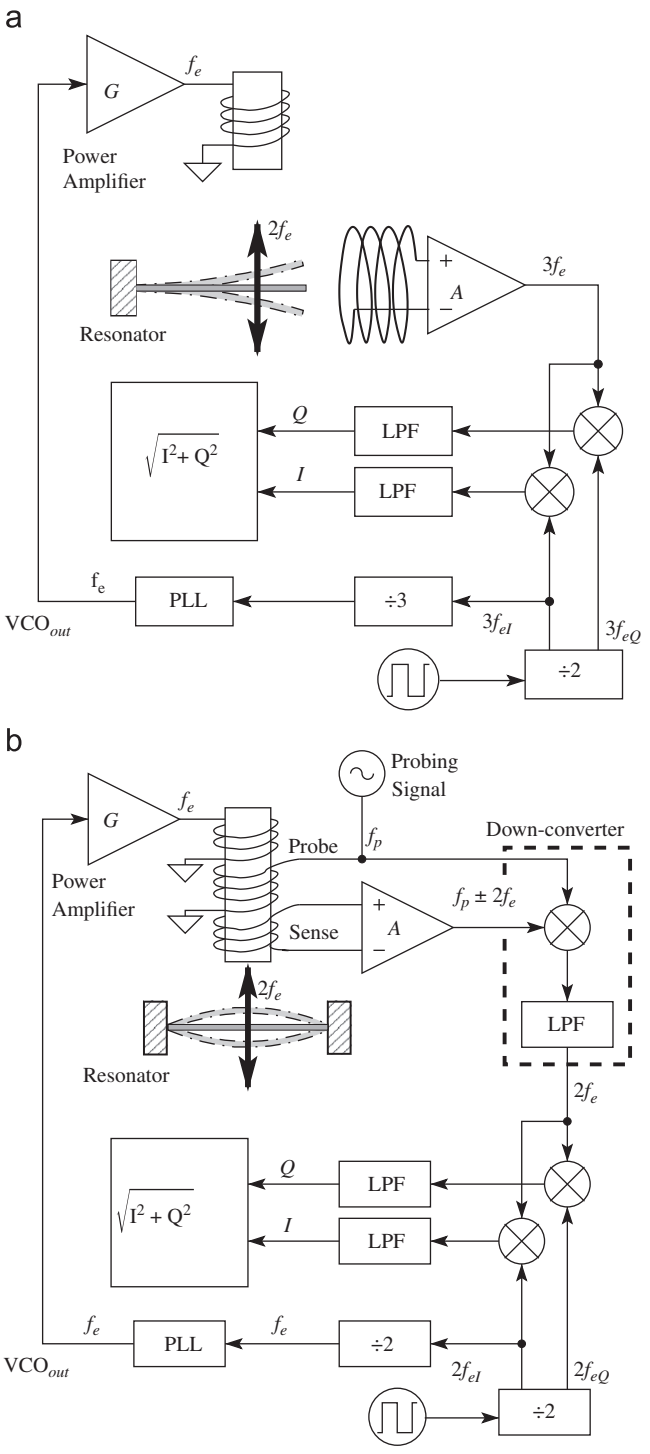

Fig. 1. Experimental setup for contactless readout of magnetically stimulated mechanical resonators: (a) base-band probing, (b) HF probing. The developed integrated interface is suitable for both schemes.

amplitude of the signal component at $3f_e$. In the case of HF probing, the signal from the readout coil is first mixed with the probing signal. The amplitude of the down-converted and filtered signal at $2f_e$ represents the amplitude of the vibration; and can be analysed with a lock-in amplifier with reference frequency $2f_e$. In both cases, the excitation frequency has to be swept until $2f_e = f_m$; mechanical resonance is revealed by the peaking of the signal detected by the lock-in amplifier, which occurs at $1.5f_m$ for base-band probing, and at f_m for HF probing.

This work discusses the design of an integrated lock-in amplifier operating at a harmonic of the excitation frequency, specifically conceived for magnetic probing. The amplifier, with an external digital processor, may be operated in vector mode, eliminating the need for delay adjustments as the reference frequency is modified.

2. System architecture

The mechanical resonance of the target system is expected to occur in the 20–40 kHz range. In the case of base-band probing, experiments on a resonator prototype suggest that the expected amplitude of the open-circuit voltage at $3f_e$ may be of the order of several microvolts at resonance, superimposed to an interference arising from the excitation at f_e that is larger by two orders of magnitude.

Similar problems may be expected for HF probing, where the sensing coil can collect unwanted contributions at the excitation frequency f_e and at the probing frequency f_p, which fortunately can be chosen sensibly higher than f_e.

Since the phase relationship between the excitation at f_e and the system response at $2f_e$ or $3f_e$ depends on the mechanical arrangement and is unknown a priori, a vector implementation of the lock-in amplifier is preferred, in order to recover amplitude information independently of any phase shift.

A block diagram of the system is shown in Fig. 2. Starting from a master clock at frequency f_{ck}, two quadrature square waves ref_I and ref_Q at $f_{ck}/2$ are obtained, used as reference inputs for the in-phase and quadrature channels of the lock-in. By further division by 3 (base-band probing), by 2 (HF probing) or simply by direct connection (conventional lock-in operation), a reference at the frequency f_e required for the excitation of the coil is derived. This reference is used to synchronize, by means of an external PLL, a high spectral purity voltage-controlled oscillator (VCO) which drives the excitation coil via a power amplifier. Thus, by sweeping f_{ck} in the range [60, 120 kHz] for base-band probing, or in the range [40, 80 kHz] for HF probing, $2f_e$ scans the range where mechanical resonance is expected.

The input to the lock-in amplifier is represented by the open-circuit voltage provided by the readout coil in the case of base-band probing, by the output of the down-converter in the case of HF probing. The lock-in front-end consists of three cascaded stages: a low-noise amplifier (LNA), with a gain around 40 dB in order to ensure that the equivalent input noise voltage of the entire system is determined by the preamplifier itself, followed by a high-pass active filter (HPF) with second order roll-off, to suppress offset and low-frequency noise and reject possible 50 Hz line disturbances, and by a programmable gain stage (PGA_{AC}).

Offset is a major concern in the design of the front-end op-amps. The propagation of the LNA output offset being eliminated by the HPF, it is important to ensure that the offset at the outputs of both the LNA and the PGA_{AC} are limited, in order to ensure highly linear operation. It was preferred to avoid making use of dynamic offset cancellation techniques, considering the risk of injecting noise in a section of the processing chain where the signal level is still very low and the signal frequency may vary in a wide range, considering that the IC may also be used as a down-converter in the HF probing approach.

In fact, harmonic distortion of the front-end should be carefully considered. In the case of base-band probing, for instance, the maximum useful signal is expected to remain 40 dB below the interference at f_e. In order to ensure that the peak originated by the mechanical resonance can be easily detected, the third-harmonic distortion introduced by the entire front-end should remain at least 80 dB below the fundamental tone.

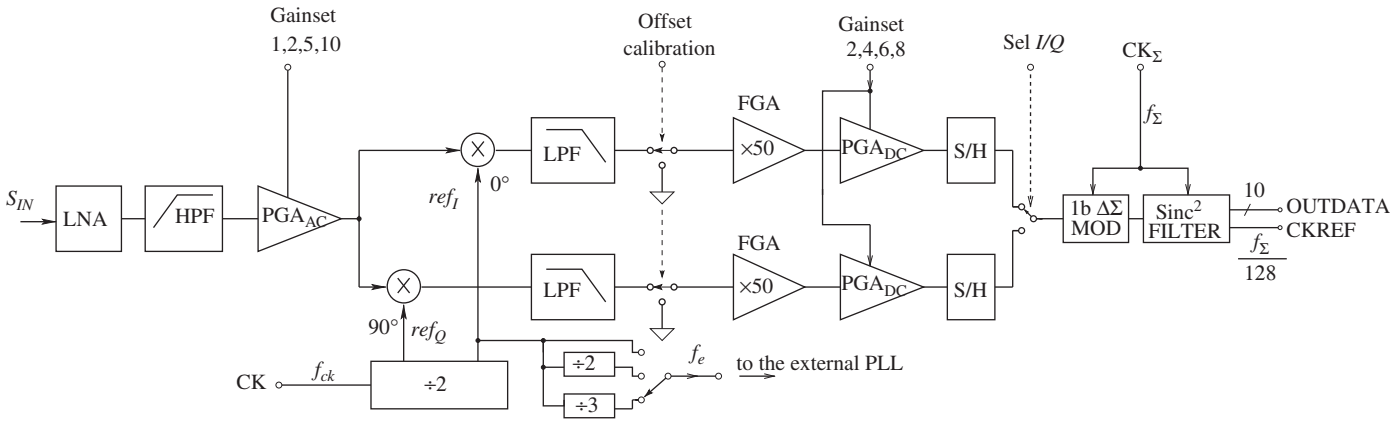

Fig. 2. Lock-in simplified block diagram: vector elaboration is highlighted. A single ADC is multiplexed between the in-phase and quadrature channels.

Otherwise the front-end may distort the interference at f_e and produce a component at $3f_e$, where the useful signal is expected.

Concerning preamplifier noise, it can be traded with the equivalent noise bandwidth (ENBW) of the low-pass filter which follows the mixer. A noise specification of 20 nV/$\sqrt{\text{Hz}}$ at 20 kHz, combined with a 5 Hz ENBW of the low-pass filter, would result in an effective noise voltage below 70 nV, sufficient for the detection of the 1 μV peak while allowing to track slow variations of the resonance frequency, and seems therefore adequate. The front-end feeds the signal to the I and Q mixers, implemented as passive, MOSFET bridge mixers. At their outputs, low-pass filters with very low cut-off frequency must be connected, in order to recover the DC levels representing the in-phase and quadrature components of the signal. In every case strong amplification is required, since the useful signal level is still very low.

Two options are offered: if the signal-to-noise ratio is relatively low, it may be necessary to achieve bandwidths of the order of a fraction of hertz, more conveniently achieved by digital filtering and decimation. Since, however, the signal level at the mixer output is still too low for proper operation of an analogue to digital converter (ADC), the mixer output is first low-pass filtered, for the purpose of anti-aliasing, then amplified to the desired level with a programmable gain stage, then fed to an ADC which can be alternatively connected to the I or Q channel. The ADC is a first order $\Sigma\Delta$ modulator operating at $f_\Sigma = 1$ MHz, followed by a sinc^2 stage performing decimation by 128. The output data stream, represented by 10b words at 7.8 kHz, is passed to an external processor for final low pass filtering and further decimation. The processor also computes the vector sum of the I and Q outputs, representing the signal amplitude, and takes care of offset calibrations for the two channels. This mode of operation will be referred to as *mixed-signal operation*; it is planned to completely integrate the functions demanded to the external processor in the final version of the chip.

If, on the contrary, the signal-to-noise ratio at the output of the mixer is reasonably high, low-pass filtering may be fully demanded to the analogue low-pass filters, since cut-off frequencies of the order of tens of hertz can be easily achieved. As before, the filters are followed by the PGAs, which may be connected to the ADC, and the external processor is not required to perform filtering and decimation. This mode of operation will be referred to as *fully analogue*.

In addition, it is desired that the chain formed by the front-end, one mixer and the corresponding analogue low-pass filter may also be used stand-alone, as an IC down-converter for the sensing coil signal in the HF probing scheme of Fig. 1(b).

3. Implementation aspects

Since definitive specifications for the lock-in amplifier were not available during the design phase, flexibility was an important goal of the project. As mentioned in the previous section, the lock-in can be operated in a fully analogue way if the final low-pass filter bandwidth is not exceedingly narrow, or in the mixed-signal mode, if digital filtering turns out to be convenient because of the narrower bandwidths required.

The design was developed in a 0.35 μm, dual poly-Si, four metal layers analogue CMOS technology with high resistivity poly-Si option [12]. The circuit is powered by a single 3.3 V supply. The entire analogue circuitry is implemented differentially, with control circuitry forcing a common mode voltage of 1.6 V referenced to ground. The input voltage in the base-band system, Fig. 1(a), is provided by the readout coil, which intrinsically provides AC coupling, and can be directly connected to the lock-in amplifier inputs. In the system of Fig. 1(b), HF probing, the readout coils feed the down-conversion chain, implemented using the same front-end blocks of the IC. The differential output of the down-conversion chain can be simply AC connected to the lock-in amplifier input; such flexibility allows the use of the same integrated interface for both resonator setups.

3.1. Low noise amplifier (LNA)

The LNA is a classical three op-amp instrumentation amplifier featuring an overall differential gain around 40 dB, Fig. 3. The first two op-amps, OPa, provide a nominal voltage gain of 30; the third is a differential-input, differential-output amplifier, OPb, with a gain of 5 and continuous-time common-mode feedback. Low-valued resistors are mandatory in order to achieve low-noise operation: in fact the nominal values ($R_1 = 20\,\Omega, R_2 = 290\,\Omega$) were chosen. Parasitic interconnect resistances play therefore a significant role, and post-layout parasitics extraction and simulation is required. The estimated overall DC gain of the extracted LNA ranges between 100 and 126, depending on the chosen extraction tool. This uncertainty is tolerable, because in the specific application the measurand is not the amplitude of the signal, but the excitation frequency which results in maximum signal amplitude. The LNA -3 dB bandwidth is about 800 kHz, and the amplitude response is flat to within -0.03 dB in the band [20, 60 kHz] of interest for both the lock-in amplifiers of Fig. 1.

The op-amps are based on an n-channel differential pair, folded-cascode architecture with active loads and output buffers, and achieve a gain-bandwidth product of 100 MHz. Thanks to the

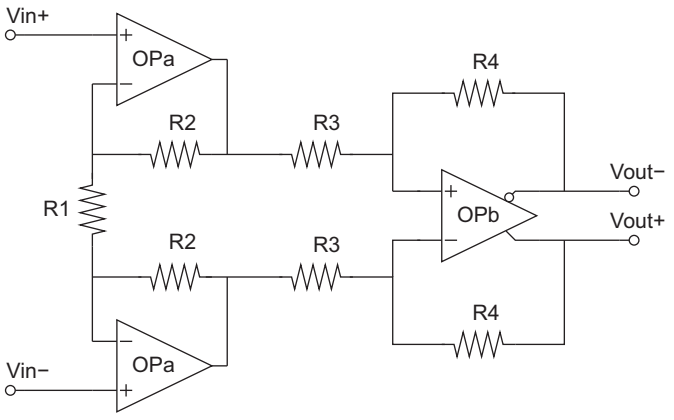

Fig. 3. Three op-amps low noise instrumentation amplifier.

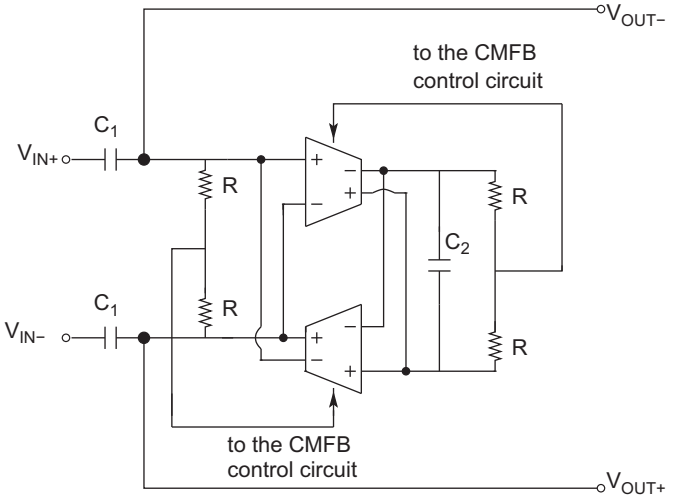

Fig. 4. Active Gm-C high-pass filter employing external capacitor for programmability. Common-mode sensing resistors are selected in order to obtain a suitable merit factor.

large area devices in the differential pairs and to the low-valued feedback resistors, the total input-referred op-amp noise in the band [30, 60 kHz] is below 15 nV/$\sqrt{\text{Hz}}$ in typical conditions, with a corner frequency around 8 kHz: an alternative implementation using the available p-channel devices for the differential pair did not provide significant improvements. Three-sigma output-referred offset voltage, estimated from Monte Carlo simulation, is below 300 mV, ensuring that the amplifier operates in a high linearity region, despite the limited voltage headroom. Third harmonic distortion is below -66 dB for an input amplitude of 1 mV, one order of magnitude larger than the maximum expected interference, while the total harmonic distortion is better than 0.8% for an input signal amplitude of 3 mV. The stage drains 9.9 mA, mostly due to the output buffers driving the low-valued load resistors.

3.2. High-pass filter (HPF)

The LNA is followed by a high-pass filter, which removes the LNA offset and thus prevents the saturation, at maximum gain, of the following programmable-gain stage. The filter, Fig. 4, is a second-order, fully differential G_m-C active filter using two external capacitors C_1 and featuring continuous-time common-mode feedback. The value of external capacitors C_1 and C_2 is 10 nF.

The merit factor Q is fixed by the resistors R (30 kΩ) used, in the common-mode feedback (CMFB) circuitry, for sensing the common-mode voltage. It is worth to remark that this implementation does not require additional resistors for the filter.

The filter features unity gain in the pass-band and a -3 dB cut-off frequency of 3.7 kHz, chosen not far from the noise corner frequency of the preamplifier in order to suppress low-frequency noise contributions, and ensuring almost 75 dB attenuation for possible 50 Hz line disturbances. The filter drains 900 μA.

3.3. Programmable-gain AC amplifier (PGA_{AC})

The programmable gain stage is a differential-input, differential-output amplifier offering gains of 1, 2, 5, 10: by choosing the gain, the lock-in dynamic reserve may be adapted to the operating conditions. The desired gain value is obtained by selecting the op-amp feedback resistors, according to the logic state of two input pins. The bandwidth of the entire front-end amplifier is about 1 MHz, allowing the use of the IC as a down-converter in the HF probing scheme of Fig. 1(b). At maximum gain, the three-sigma offset at the output of this stage is below 100 mV, compatible with proper operation of the mixers which follow.

3.4. Mixers

Mixers were implemented as passive n-MOS bridges [6], featuring a conversion gain of 0.62 very close to the ideal $2/\pi$. A passive bridge, biased with zero DC current ensures very low noise at low frequency and ideal performances for the operations of the lock-in amplifiers.

To this aim the driving waveforms were carefully designed to avoid the simultaneous closure of the two bridge paths. This ensures [7] an effective rejection of the $1/f$ noise of the four MOS switches. The total noise referred to the mixer input, estimated by a cycle-stationary analysis tool, is below 7 nV/$\sqrt{\text{Hz}}$ at 1 mHz in the typical case, and is absolutely negligible considering the front-end gain.

3.5. Low-pass filter and programmable gain DC amplifiers

In order to keep the offset as low as possible, the low-pass filter is implemented as a second order passive RC filter whose bandwidth can be easily adjusted between a few hertz and hundreds of kilohertz by changing two external capacitors. In fully analogue operation (bandwidths of several hertz) the filter can be used as the final low-pass filter of the lock-in amplifier. If a large bandwidth (tens of kilohertz) is chosen, it behaves as the base-band filter in the down-converter including front-end, mixer and $2f_e$ low-pass filter in the HF probing scheme of Fig. 1(b). If an intermediate bandwidth is chosen, it acts as anti-aliasing filter for the $\Delta\Sigma$ ADC. With reference to the case of base-band probing (Fig. 1(a)), if configured for a 3 dB cut-off frequency of 500 Hz, it ensures, in the worst case, more than 60 dB attenuation of the disturbance originated by the tone at f_e, which is found at $2f_e$ after mixing.

The DC amplifier consists of two cascaded, differential-input, differential-output stages with continuous-time, common-mode feedback. The first stage (Fig. 5) offers a fixed gain of 50 (fixed gain amplifier, FGA) and makes use of the dynamic input offset cancellation scheme reported in [8], implemented using poly–poly capacitors and operated at a fixed 10 kHz frequency.

The second stage is a programmable gain amplifier (PGA_{DC}) providing four selectable gain levels (2, 4, 6, 8) without offset cancellation. The three-sigma, output referred offset voltage in maximum gain configuration, not considering mixer non-idealities, is below 90 mV, and mostly arises from amplification of the output offset of the first stage.

Finally, a sample-and-hold (S/H) eliminates the commutations associated with the operation of the offset cancellation circuitry.

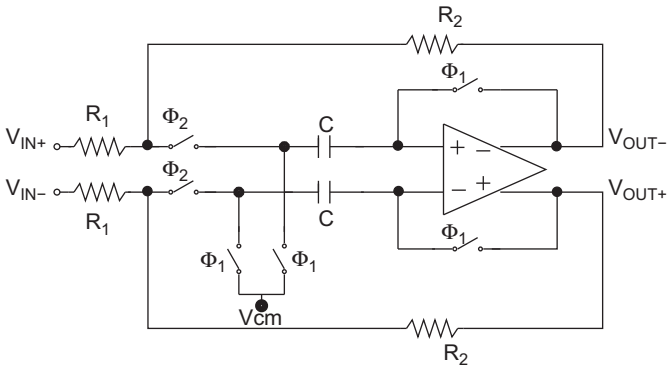

Fig. 5. Fixed gain amplifier (FGA) featuring dynamic input offset cancellation; the gain is set by R2/R1 = 50.

It consists, for each signal line, of a switch, a hold capacitor and a custom operational amplifier configured as unity-gain buffer.

Fig. 6 documents the need for offset cancellation along the DC amplification chain. Hundreds of Monte Carlo "mismatch and process" simulations were carried out, with all the four mixer transistors switched off and the low-pass filter inputs short-circuited. The resulting DC voltage distributions are reported at the fixed-gain amplifier output, Fig. 6(a), and at the output of the PGA_{DC}, Fig. 6(b), configured for maximum gain. Offset distributions without offset cancellation (upper part of the figure) and with offset cancellation in the fixed-gain stage (lower part) are reported. It appears that without offset cancellation, it is impossible to keep the output within the input range of the A/D converter. In the present implementation, offset cancellation is performed only in the FGA. An offset calibration mode of operation is provided, whereby all the four transistors of the mixer are kept open and the inputs of the FGA are shorted. Then, the offset measured at the IC digital output, including the contributions from the fixed gain stage, the PGA_{DC} and the ADC, can be measured and subtracted from subsequent ADC readings by the digital processor, at the cost of a moderate reduction of the ADC input dynamic range (according to the simulations, about 18% max considering 3σ offset).

Overall, the current drawn by the DC processing chains is about 22 mA.

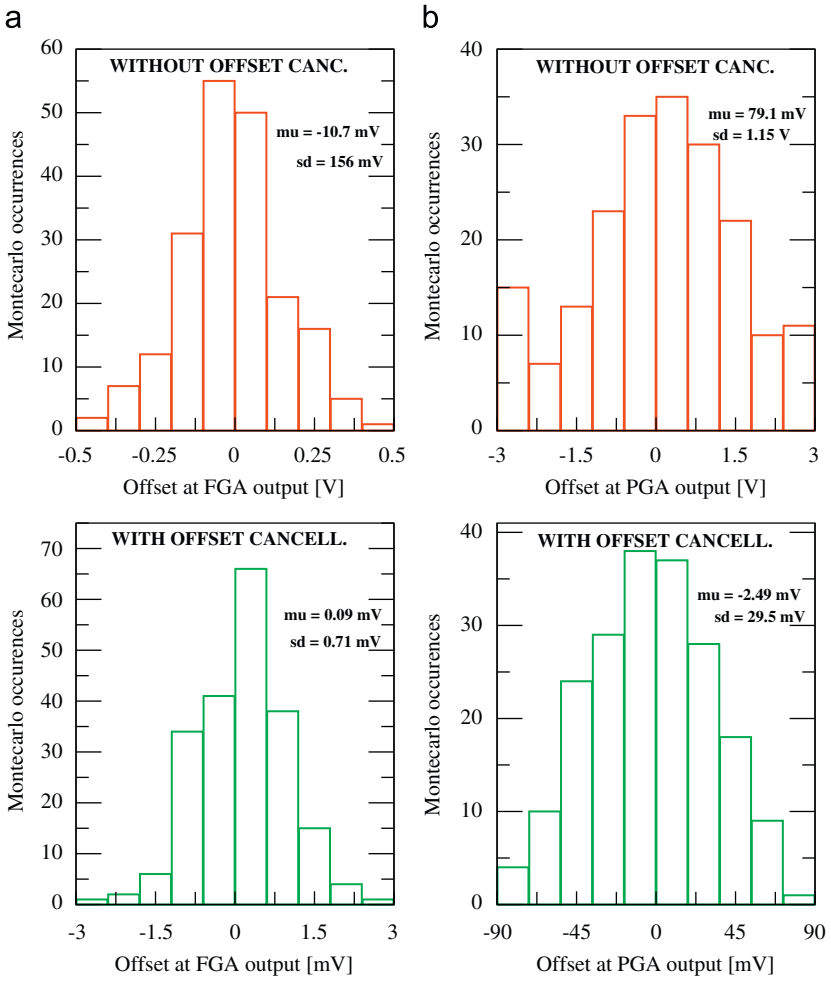

Fig. 6. Monte Carlo simulations of the distribution of offset voltage in the DC processing chain after the mixer. Offset distribution at: (a) the 50× FGA output, (b) the PGA_{DC} output. The upper part of the figure was obtained without offset cancellation, the lower part with offset cancellation enabled.

3.6. The analogue-to-digital converter

The ADC is based on fully differential, first order $\Delta\Sigma$ modulator operating at $f = 1$ MHz, with a nominal input range of ± 0.5 V differential [10]. The modulator has been developed exploiting switched-capacitor techniques; it includes a low-power operational amplifier featuring a switched-capacitor common-mode feedback operating at the same frequency, a latching-comparator and a clock generation circuitry similar to the ones described in [9,10]. The modulator employs 1 and 2 pF capacitors and the sampling switches are transmission gates; the comparator is a fully differential low-power dynamic latch with dual positive feedback loops.

The oversampling ratio of the converter is 128 corresponding to a signal bandwidth of 3.9 kHz. The modulator is followed by a sinc^2 stage implemented as second order accumulate-and-dump digital circuit [11], performing decimation by 128. In the present implementation, the output data stream is represented by 10b words at 7.8 kHz. Simulations demonstrate an effective number of bits equal to 9.4 at the 7.8 kHz output rate, over an input range of ± 500 mV differential, just slightly lower than the maximum ENOB achievable, 9.9b.

4. Simulated performance

The performance of the lock-in amplifier was evaluated by means of transistor level simulations of the full elaboration chain. The effect of lock-in amplification is shown in Fig. 7, where the spectra at the LPF output are reported for both I/Q channels. A 1 μV 30 kHz useful signal has been superimposed to a 10 kHz interference 40 dB higher (base-band probing, $f_e = 10$ kHz), the phases of the useful signal and the input clock being set almost equal.

At the LPF output, the useful signal is down-converted to DC whereas the interference is up-converted to 20 kHz; the mixed interference is now 60 dB lower than the useful DC signal and affects both channels. It is worth noticing that such interference is further rejected by the low-pass profile of the ADC.

The 11 kHz signal in Fig. 7 is an incoherent disturbance originated by the switching of the offset cancellation circuitry in the FGA.

Also the final ADC was simulated at transistor level by stimulating its input with a sinusoidal tone at 3.83 kHz; the spectrum of the digitized output is reported in Fig. 8, where the input tone and the folded harmonics may be noted. The simulated signal-to-distortion ratio is 61 dB whereas the ADC output noise power integrated over the bandwidth [30, 4000 Hz] is 4.1 μV^2.

The target performances of the developed lock-in amplifier are summarized in Table 1.

As it may be noticed, power consumption is relatively high, since the same basic design was used for all the op-amps in this exploratory design, considering that the application does not call

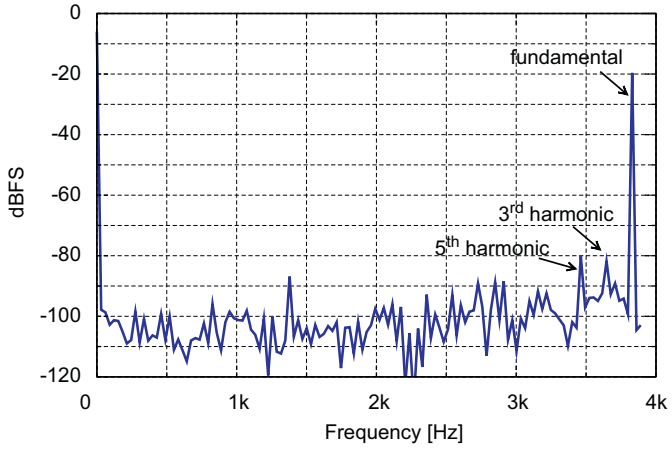

Fig. 8. Simulated spectrum of the $\Sigma\Delta$ ADC output; the input signal is set to 3.9 kHz.

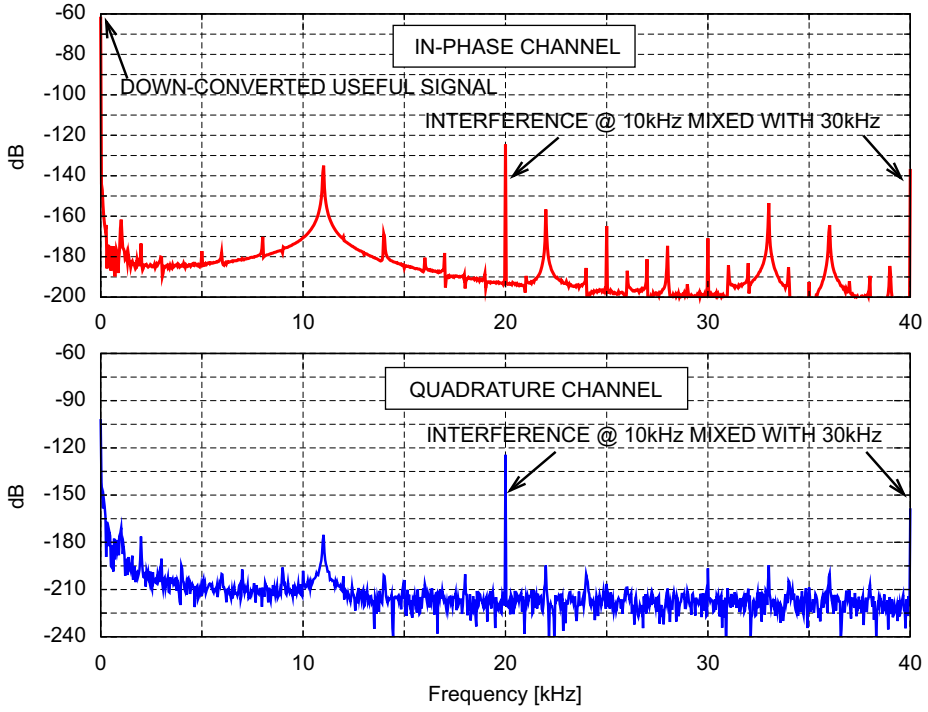

Fig. 7. Signal spectra at LPF output for both channels: simulations were performed with useful signal at 30 kHz and interference at 10 kHz.

Table 1
Amplifier performance.

	Design value	Measured value
General		
Die area (I/O pads excluded)	2.5 mm^2	
Supply voltage	(3.3 ± 0.3) V	
Power dissipation at 3.3 V, $f_\Sigma = 1$ MHz	110 mW	
Front-end		
LNA		
Nominal gain	40–42 dB	40 dB
-3 dB cut-off freq.	800 kHz	
Input referred noise voltage	15 nV/$\sqrt{\text{Hz}}$	17 nV/$\sqrt{\text{Hz}}$
Noise corner frequency	8 kHz	
HPF	Active second order	
In-band gain	0 dB	0.1 dB
-3 dB lower cut-off freq.	Cap-progr., nominal 3.7 kHz	
PGA_{AC} gains	(0, 6, 14, 20) dB	(-0.1, 5.8, 13.8, 19.7) dB
I and Q channels		
Mixer loss	4.2 dB	
LPF	Second order	
In-band loss	1.6 dB	
-3 dB cut-off freq.	Cap-prog., nominal 500 Hz	
FGA+PGA_{DC} gains	(40, 46, 49.5, 52) dB	
Total maximum differential gain	106–108 dB	
ADC	$\Sigma\Delta$ 1st order, 1-b modul.	
Clock frequency	1 MHz	
ENOB	9.4 at 7.8 kHz output rate	
Signal-to-distortion ratio	61 dB	
Output noise power	4.1 μV^2 over [30–4000] Hz	

for low power. Slightly less than one third of the total power is required by the LNA, and is related to the necessity of driving low resistance loads in order to achieve low noise operation; this part of the power budget cannot be easily reduced unless by a substantial revision of the LNA architecture. On the contrary, it is expected that substantial power saving may be achieved by using power optimized op-amps in the DC processing chain.

5. Experimental results

The chip layout was developed taking care to ensure maximum symmetry between the two lock-in channels. The design flow was completed and the chip was manufactured by a silicon foundry service.

Fig. 9 shows a micrograph of the chip. The die area is 2.5 mm^2, I/O pads excluded.

First, the in-band gains of the various sections of the amplification chain were measured. The overall LNA gain measured at 30 kHz turned out to be about 40 dB, compatible with the post-layout simulation of the extracted circuit, while an in-band gain about 0.1 dB was measured for the HPF. Also the measured gains of the other sections of the AC chain closely agree with the expected values.

The input referred LNA noise was then measured by connecting a SR785 FFT spectrum analyzer to the test point available at the LNA output. Taking into account the actual measured gain of the LNA, the input referred noise is 17 nV/$\sqrt{\text{Hz}}$, close to the simulated value of 15 nV/$\sqrt{\text{Hz}}$.

Fig. 10 demonstrates the operation of the circuit in the conventional mode, where the input to the lock-in (a 4.5 μV sinewave at 30 kHz) is at the same frequency as the local oscillator driving the I and Q mixers. The DC voltages measured at the S/H outputs of the I and Q channels are reported as a function of the phase between the input signal and the local oscillator reference. The low-pass filter is arranged for a 3 dB cut-off of 190 Hz.

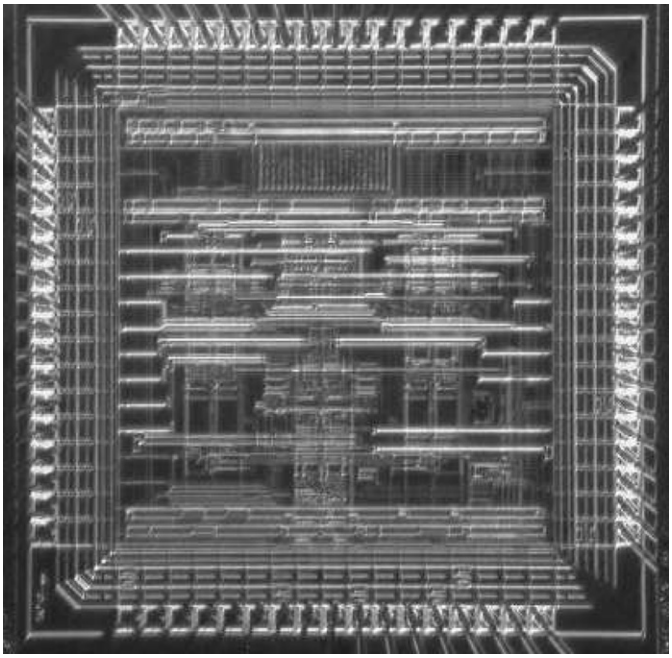

Fig. 9. Chip microphotograph.

Experimental points correspond to the average of 100, 1 s integration time, digital voltmeter measurements. The dash- and dash-dot lines show a least squares sinusoidal fit which allows to extract the amplitude and the relative phase of the two sinewaves. The measured amplitude unbalance between the two channels is 0.07 dB and the quadrature error is 0.3°. A sensible DC offset is observed between the channels, non-fully explained by the offsets of the two DC processing chains, which can be measured in the offset calibration mode, and more relevant at

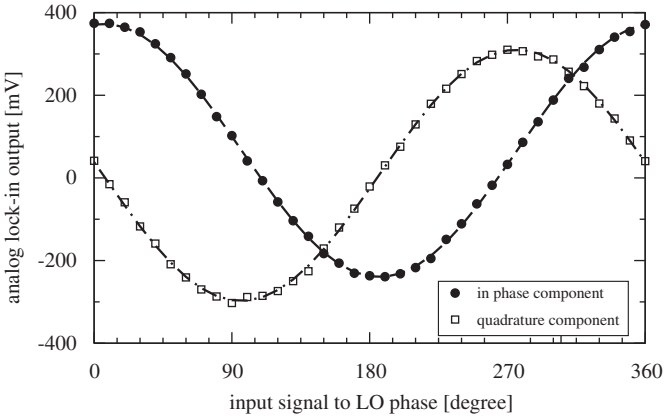

Fig. 10. Measured DC voltages at the S/H outputs of the two channels as a function of the phase between the input signal and the local oscillator reference which drives the mixers.

high values of the PGA_{AC} gain: this suggests that it may take origin from non-perfect DC rejection of the two mixers. At present, therefore, offset should be removed in the digital domain, by performing measurements of the type illustrated in Fig. 10, evaluating the DC term superimposed to the sine functions and subtracting this term from the output readings taken in normal operation, by means of the external digital processor. Since this obviously entails a larger than expected reduction of the maximum amplitude of the tractable signal, adoption of offset compensation techniques also in the PGA_{DC} and improvement of the mixer's DC rejection should be considered in a redesign.

Since the system was developed for an application where a strong interference at one third of the signal frequency is expected, the measurement was repeated on a different sample at lower signal level (900 nV_{rms} at 30 kHz), with and without a strong interferer (90 μV_{rms} at 10 kHz). A different distribution of gains along the chain was used. The signal was obtained by suitably attenuating the internal oscillator output of a Stanford Research SR830 DSP Lock-In Amplifier whose reference was driven by a square wave obtained by dividing by 2 the 60 kHz source used to drive the CK input of the circuit (see Fig. 2) and by suitably delaying it in order to obtain the desired phase shift; the 10 kHz interferer, provided by the oscillator output of a SR810 Lock-In Amplifier, was not synchronized to the signal.

Fig. 11 demonstrates that the presence of an interferer has a limited effect on the measurement. The voltage was measured with an integration time of 2 s. The I channel output is shown; black dots correspond to no interference, white dots to the presence of the interferer. One-sigma error bars are shown for the last case: less than 100 nV are resolved in 2 s with the available test board. Considering also the Q channel, the new measurements with new gain settings demonstrate again a reasonable quadrature error (below 2°) and amplitude unbalance (0.04 dB).

Fig. 12 documents the lock-in linearity. It reports the S/H output of the in-phase channel vs. the input amplitude for a sinewave signal without quadrature components. For each point 50 digital voltmeter measurements with an integration time of 2 s were taken: the symbol corresponds to the average, i.e. to a total integration time of 100 s. The standard deviation from the interpolating straight line is around 200 μV, in a range of 170 mV. At such long integration time, 100 nV increments can be very well resolved.

Concerning the sigma–delta A/D converter, unfortunately decimator operation could not be verified, due to a faulty connection to an output pad. However, it was possible to assess

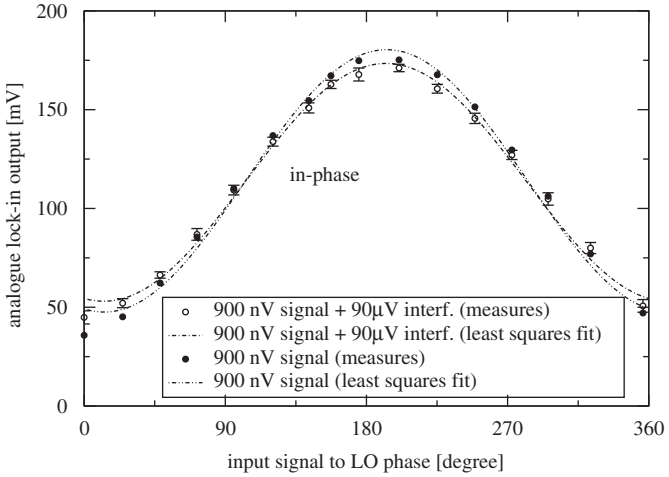

Fig. 11. Measured DC voltage at the S/H output of the in-phase channel as a function of the phase between the input signal and the local oscillator reference which drives the mixers. Black dots correspond to no interference, white dots to the presence of a 10 kHz interferer 100 times larger than the useful signal. One-sigma error bars are shown for the last case.

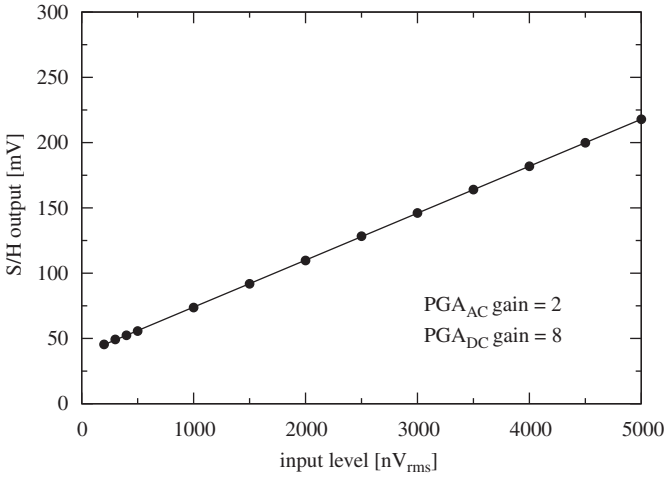

Fig. 12. S/H output voltage of the in-phase channel vs. rms amplitude of an input sinewave without quadrature component.

the ΣΔ modulator functionality by measuring the conversion characteristic, i.e. by measuring the average frequency of the pulses at the modulator output (number of counts observed in a gate time of 100 ms, averaged over 16 measurements) vs. the input DC voltage, directly applied to the modulator input through the available test pins (see Fig. 13). As expected, linearity is good (the correlation coefficient of the regression line is above 0.9999). The observed residual may be in part be ascribed to the DC voltage source, in part to fixed pattern noise.

6. Conclusions

An integrated CMOS vector lock-in amplifier was developed, specifically conceived for the detection of low-level signals in magnetically excited resonant sensors. The circuit includes in-phase and quadrature analogue signal processing channels and an integrated ΣΔ analogue-to-digital converter. The circuit can be operated in various configurations: in particular, by combining

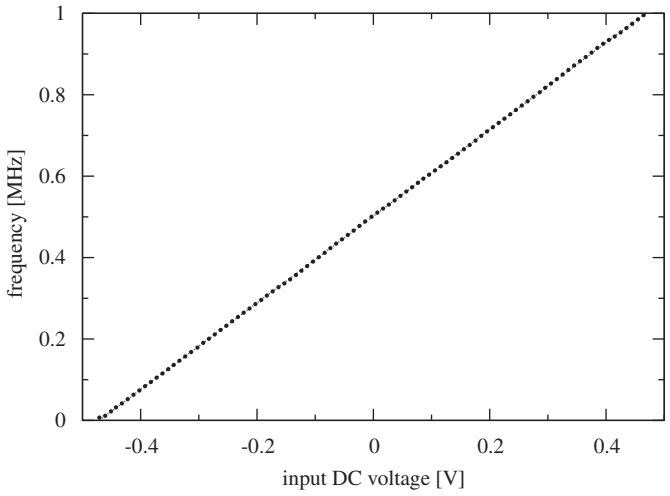

Fig. 13. Average frequency of the pulses at the $\Sigma\Delta$ modulator output vs. DC voltage directly applied to the modulator input.

the digitized outputs of the two channels, vector operation is possible.

Measurement results on the first silicon demonstrate an input-referred noise below $20\,nV/\sqrt{Hz}$, and maximum gain above 100 dB, in the [20, 60 kHz] band. Acceptable quadrature error and amplitude unbalance between the I and Q channels were demonstrated. Measurements on the first test board also demonstrate the capability of resolving 100 nV variations in the input signal in a measurement time of the order of 1 s, so that a 50 points frequency scan can be completed in less than 2 min.

Acknowledgements

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