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A new electric conductance conversion method suitable for very low power applications

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ABSTRACT

This article describes a new electrical conductance converter method suitable for low power applications and an implementation in standard CMOS technology. Despite being designed to meet specific measurements requirements, this converter is intended for applications where device power requirements are determinative such self powered sensors networks and implantable devices. The topology is described and an implementation is presented. Results show the possibility of being powered by a single 1.2 V accumulator cell with a consumption of 8 nJ per conversion.

1. Introduction

Many sensory systems rely on power consumption for device size, life cycle or availability. Thus, energy efficiency can rule the device design, may prevail over speed or precision and ultimately dictate the viability of some applications. Implantable devices and autonomous sensory networks are such examples.

Herd management by automatic prediction of optimum time to proceed with artificial insemination is another application. Electric bio-conductance and temperature are physiologic parameters that systematically depends on estrus cycle and can easily be assessed by a low power implantable device to improve IA effectiveness and economic performance [1,2]. In fact, studies show a substantial higher electric conductance during the estrus phase at reproductive tissues. Measurements at 16 and 100 kHz shows an increase from 29% to 45% relative to conductance baseline values [3]. Cycle hormonal changes manifests at both intracellular and extracellular levels [4,5], therefore no significant admittance phase variations are observed.

Bio-technology field have already motivated the development of electric bio-impedance sensor aiming low-power and single chip implementation [6]. Most of them apply a bipolar pulsed current source into a biological tissue, and uses synchronous demodulation to extract real and imaginary components of impedance [7]. Both components are separately filtered or sampled and converted components are separately filtered or sampled and converted to digital domain. This method is effective but do not minimize power consumption. Moreover, for many others applications including the referred IA application, the imaginary component can be neglected.

In precision agricultural farms, a sensor network can evaluate soil moisture and solar radiation for automatic water management. The presented examples rely on electrical conductance measurement and benefit with low power demand. Nevertheless, due to the vast resistive

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transducer types many others applications can benefit from a low power conductance measurement device.

A previous article described briefly the idea and implementation accomplished with simulations [8]. Here, a noise suppression characteristic provided through the converter architecture is presented and the description of prototype implementation is accomplished with several analog design parameters. Finally, the results of prototype performance testes are here presented.

2. Topology and conversion method

The electrical conductance measurement process is achieved by integrating a voltage developed on the Unit Under Test (UUT) when it is biased with a controlled current. The conversion output is number of the source pulses (N_P) required for the integration voltage overcame (V_{INT}) a constant threshold (V_{TH}) corresponding to the difference from the main circuit reference (V_{REF}) to a comparison voltage (V_{CMP}). Fig. 1 presents the converter topology and Fig. 2 presents the main signals involved on the conversion process [8].

The first chopper provides a simple way to implement a bipolar current source that guarantees the average current to be zero. The amplifier isolates the UUT from the second chopper and amplification if needed. A single carrier signal (C) should be applied to both choppers to ensure operation synchronism. This carrier assumes only two values each half current source period (T): $C_{T/2} = \{1, -1\}$.

The process of voltage integration allows the UUT to be biased with very low amplitude current. The second chopper is required to rectify the UUT voltage allowing it to be integrated.

The conversion operation can be performed using several current source signal types if their average is zero and if they can be synchronized with the choppers. Sinusoidal would be the preferable signal due to the less harmonic content. The proposed bipolar current signal S with two zero level sections aims the implementation simplification and void energy loss. In a discrete time implementation with a two-phase integrator, the zero level sections must occur during the integration phase when its input is ignored. To archive such a bipolar excitation current at UUT, the period of S is divided in for equal sections: $S_{T/4} = \{0, 1, 0, 1\}$.

The conversion output N_P depends on the current source amplitude I_S, the amplifier gain A_V, the voltage threshold and the conductance of UUT (G_{UUT}) itself according to the equation:

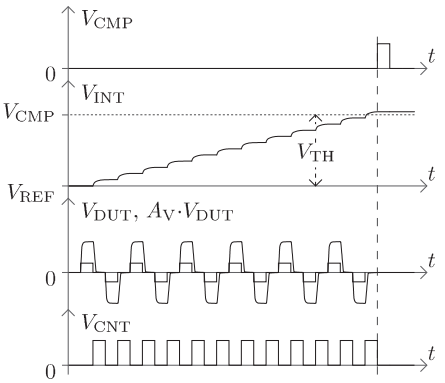

Fig. 2. Main signals involved on the conductance conversion process.

$$N_P = \frac{V_{TH}}{A_V \cdot I_S} \cdot G_{UUT}, \tag{1}$$

2.1. Main features

This simple topology has some features in favour of low power. First it can be implemented or included in a single and low-voltage CMOS chip. Secondly, the combination of chopper stabilization and voltage integration has a lock-in amplifier characteristic providing offset cancellation from the current source and amplifier, and noise suppression introduced in the UUT. Fig. 3 shows the noise spectrum at the integrator output (V_{nO}) resulted from an unitary white noise source added to the UUT after 1, 10 and 100 bipolar current source cycles (N_C). Each bipolar current source cycle requires two current source pulses ($N_C = N_P/2$).

In contrast to its preceding signals, the integrator output is expected to have a superior voltage range and a superior signal-to-noise ratio, due to voltage integration and noise suppression. This feature can be useful to achieve precision or can be exploited to reduce power consumption.

This topology does not require any sample-and-hold as the simple slope converter does. Its resolution is not constant, though. Relative resolution to the input depends on UUT itself according to the expression 2.

$$\frac{\Delta G_{UUT}}{G_{UUT}} = \frac{A_V \cdot I_S}{V_{TH}} \cdot \frac{1}{G_{UUT}} \tag{2}$$

This feature may reduce the UUT range. However the topology allows the development of a converter optimized to meet some specific application.

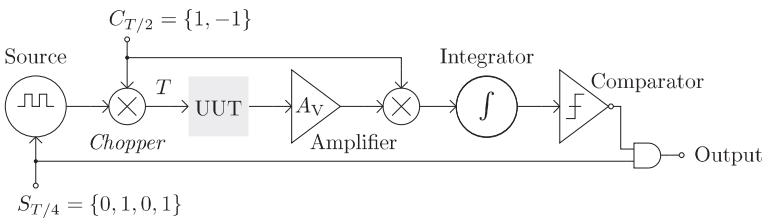

Fig. 1. Proposed electrical conductance converter topology.

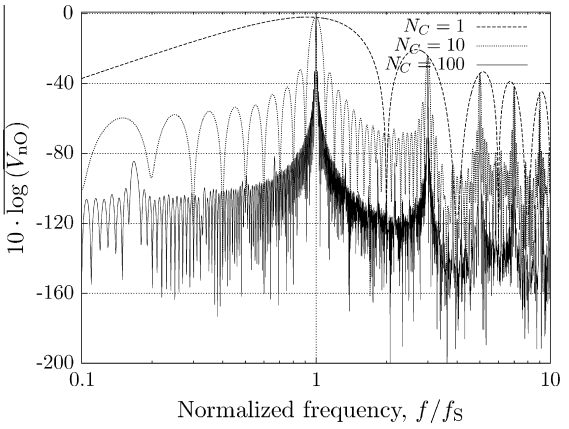

Fig. 3. Noise suppression characteristic in two decades after 1, 10 and 100 bipolar current source cycles (N_C).

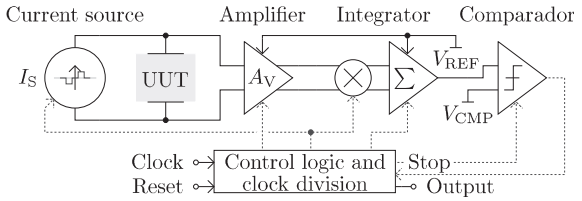

Fig. 4. Prototype block diagram.

2.2. Design choices

A characteristic inherent to this topology is design flexibility to meet application requirements of resolution, measurement frequency and power consumption. If the UUT admittance imaginary component matters, power depends on circuitry speed to process signal at a desired measurement frequency. Otherwise, power and speed are a compromise for a specified measurement range and resolution. With very little adjustment on biasing and input clock frequency division it is possible to perform impedance measurements at a wide frequency range with the same circuit.

Minimum voltage is dictated by amplifier cells and process technology. Weak or moderate channel inversion provides small transistor source-drain saturation voltage allowing analog cells to operate at low voltages.

UUT range can be extended by two different means: by controlling the current source amplitude, or performing several integration cycles. In the first case current source requires a controllable multiple current mirror. In the second case, another comparator is required.

3. CMOS implementation

The implementation has the purpose to evaluate the minimum power consumption of a conductance converter and the consequent measurement performance. The goal of power minimization led to the choice of a discrete time implementation. To reduce the current source amplitude and the amplifier output, a differential implementation is required, with the exceptions of integrator output and comparator input. Fig. 4 shows the block diagram of the implemented prototype.

The amplitude I_S was chosen to be 350 nA and the bias reference current 70 nA. This allows most transistors to operate on the efficient weak or moderate inversion regions. V_{REF} and V_{CMP} are external and were set respectively to 0.72 and 0.12 V.

3.1. Current source

The source includes the first chopper and is based on a H bridge fed by NMOS current mirror M_9–M_{10} (Fig. 5). This simple circuit guarantees no DC current output. Two complementary $S_{P\overline{N}}$ and $S_{\overline{P}N}$ signals control the output current direction and $\overline{E}$ blocks output current by stealing all the reference current from the mirror through M_{11}. M_5–M_9 form two inverters to reduce transition glitches on step current output transitions by reducing the gate voltages on bridge transistors. Output terminals are connected to the UUT and differential amplifier inputs.

In this figure and following ones, transistors channel sizes are indicated in the format width/length (μm/μm) and bias currents indicated in ampere. All transistors sizes can be deduced through circuit symmetry. M_9–M_{10} mirror operates in the transition of weak inversion (WI) with moderate inversion (MI) and all the others operate in WI.

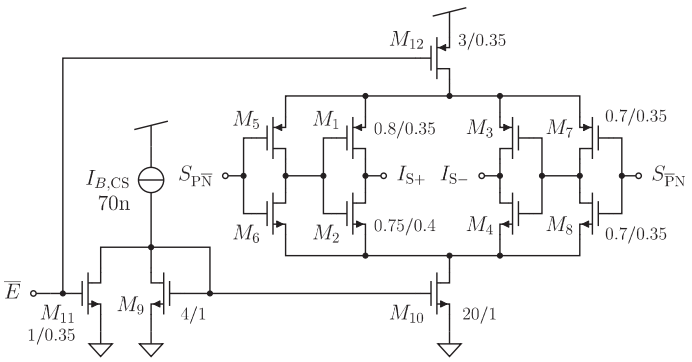

Fig. 5. Current source schematic. The circuit includes a controllable current mirror and H bridge.

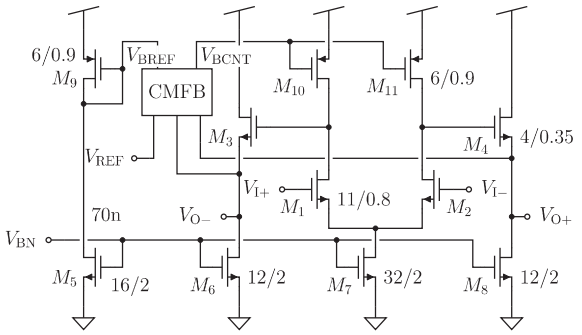

Fig. 6. Fully differential amplifier schematic.

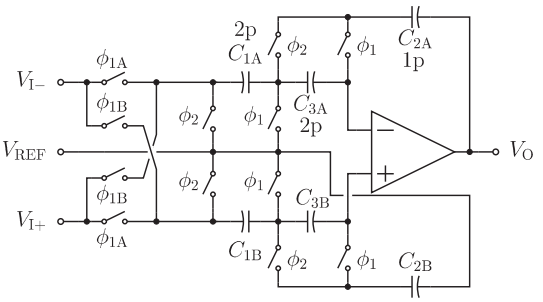

Fig. 8. Differential input integrator employing double sample technique and including a chopper by adding two switches at the input.

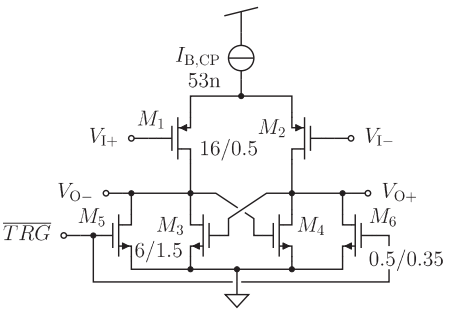

Fig. 9. Triggered comparator schematic.

3.2. Differential amplifier

The amplifier isolates the UUT from the second chopper and provides the desired voltage gain. As shown on Fig. 6, it consists of a transconductance gain stage followed by common drain stage. The transconductance gain is given by $gm_1/(gds_1||gds_{10})$. The drain stage provides the current output and has a voltage gain almost unitary, given by $1/n$, where n is the substrate factor. This circuit does not require stability compensation once it has no feedback.

In this circuit the differential pair input load M_{10}–M_{11} and M_9 operate in the WI–MI transition and all others operate in WI.

Once amplifier is fully differential, it requires a common mode control circuit (CMFB). This was implemented with a switch capacitor (SC) network represented on Fig. 7 which adds almost no power consumption [9,10]. C_2 and C_3 provide a AC path from each output to V_{BCNT}. Both paths provide negative feedback but only their common mode takes effect. C_1,C_4 and the switches provide the correct output DC shift by sampling $V_{REF} - V_{BREF}$ and applying this shift to C_2 and C_3.

3.3. Integrator

In the presented topology, any small input offset on integrator can produce large measurement error because it would be integrated during all conversion cycles. Fortunately the step signal characteristic at the input allows using a double sample technique removing the op-amp input offset. This technique also reduces the finite-gain errors [11]. These features allows to use a low performance op-amp witch is decisive for very low power applications. The voltage gain is given by C_1/C_1 ratio. C_3 capacitors stores the op-amp input offset during the storage phase and removes it during the integration phase.

This integrator presented in Fig. 8 is a differential input version of the single input double sample technique integrator [12]. A symmetric input was added, doubling capacitor and switch numbers, and requiring a modified connection to the reference. Miller op-amp was chosen due to good power dissipation to gain-bandwidth compromise and the possibility to work at 1.2 V. The current consumption in the implemented op-amp is 140 nA in the differential input stage and bias mirror and more 140 nA in the output stage. All its transistors operate in WI.

Since the integrator has two switches at the input, two more were added to include the second chopper at the integrator input. This inclusion was completed by dividing the sampling phase ϕ_1 into ϕ_{1A} and ϕ_{1B}.

3.4. Comparator

The triggered comparator shown in Fig. 9 was chosen due to the discrete-time implementation. It consists of a differential pair loaded by a negative resistance to provide positive feedback [13]. Two transistors switches were added forcing both outputs to be zero. When switches are released the outputs are set. All transistors operate in WI.

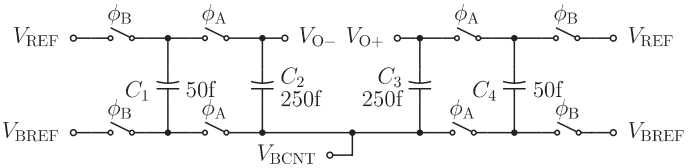

Fig. 7. Low power SC CMFB circuit.

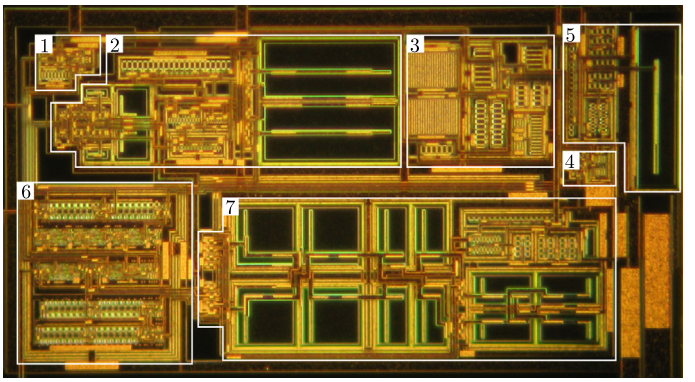

Fig. 10. Prototype layout with blocks identification: 1 – current source, 2 – differential amplifier, 3 – bias block, 4 – comparator, 5 – buffer, 6 – control block, and 7 – integrator. Dimensions are 220 μm · 390 μm on a 0.35 μm CMOS process.

3.5. Control and bias blocks

The control block generates the clock signals to all the converter blocks from the same clock input. All these signals are disabled when the comparator output Stop is activated ending the conversion process. To restart the process the Reset input must be activated.

The bias block is a constant transconductance mirror circuit that establishes bias to all analog blocks [14]. Bias current can be adjusted through an external resistor. In this implementation all transistors operate in WI.

Though they are quite simple, these blocks allow the prototype to be tested at several bias currents and for several measurement frequencies.

3.6. Prototype layout

A voltage follower was added to the prototype of Fig. 4 to allow the integrator output (V_{INT}) to be measured from the outside. Prototype circuit requires an area of 0.086 mm^2 to layout it on a 0.35 μm CMOS process without connection pads. Careful attention was taken to dispose digital control block as far as possible from the integrator capacitors and the bias block. Fig. 10 presents the layout with block identification.

4. Results and discussion

The prototype was tested in a dedicated circuit board with nine conductance references within the specified range at controlled temperature. Fig. 11 shows the integration voltage and current source output showing the correct behaviour of the prototype.

4.1. Linearity error

For each reference 250 samples were obtained at 1 kHz, 5 kHz and 25 kHz at 26 °C. Fig. 12 shows the transference function drawn with the average value of each sample. The linearity error is 6.8% at 5 kHz and about 12% for both 1 kHz and 25 kHz.

The output error most notable at the high end of UUT range suggests that linearity loss is mainly due to charge redistribution losses. The lower end range values shows convergence for the tested frequencies suggesting that er-

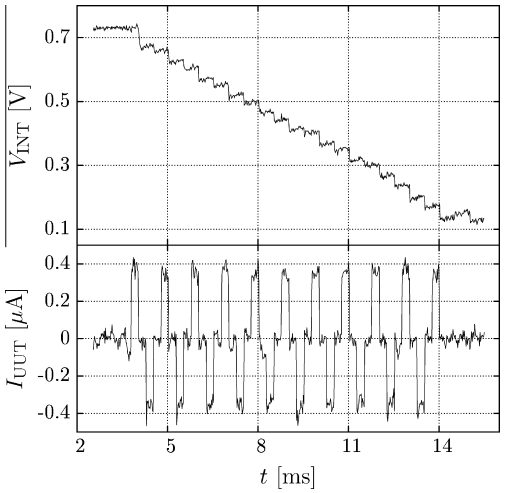

Fig. 11. Transitory of current source output (I_{UUT}) and integrator output (V_{INT}) signals.

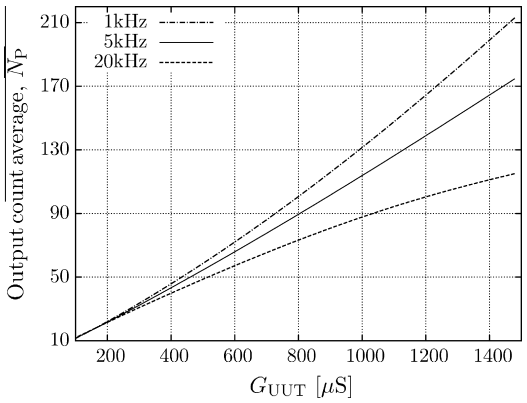

Fig. 12. Conversion output average (N_P) for UUT conductance range from 100 to 1500 μS at 1, 5 and 20 kHz.

Table 1
Standard derivation values (σ) of N_P for UUT from 100 to 1500 μS at 1, 5 and 20 kHz.

Frequency (Hz)	UUT conductance (μS)								
	100	149	196	256	372	499	767	1003	1479
1 k	0.497	0.497	0.556	0.799	1.289	2.064	4.172	7.321	10.979
5 k	0.458	0.447	0.398	0.740	1.350	1.893	3.686	6.088	9.503
20 k	0.0	0.519	0.557	0.644	1.289	1.559	1.673	3.093	4.377

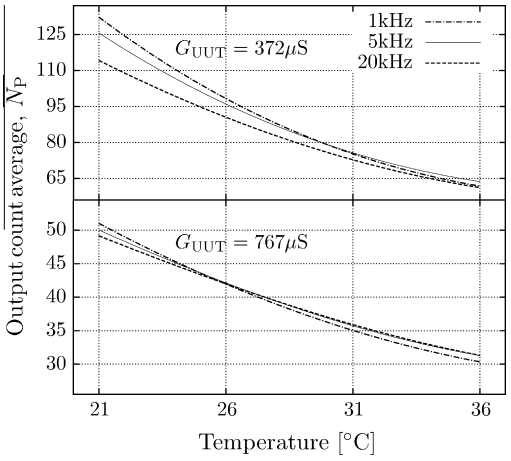

Fig. 13. Temperature dependency of conversion average ($\overline{N_P}$) from 21 °C to 36 °C.

rors due to the differential amplifier and integrator recovery times are negligible. The linearity error can be reduced using larger capacitors in the integrator.

4.2. Repeatability error

Table 1 shows the standard derivation values (σ) for each UUT respectively to Fig. 12. Table 1 data shows a systematic repeatability error increase along the measurement range. This is due to the corresponding signal-to-noise decrease at the amplifier input along the same range.

This repeatability feature can be justified for two main reasons. First, the discrete-time integrator bandwidth is limited to the maximum measurement frequency ($1/T$) so it can't provide the noise suppression shown in Fig. 3. Secondly, noise can also affect circuit performance because it affects bias currents and all analog circuitry. The use of larger transistors, higher bias currents and the use of a continuous time integrator with improved bandwidth would increase precision but can increase power consumption.

4.3. Temperature dependency

Temperature dependency was evaluated with G_{REF} = 372 μS and G_{REF} = 767 μS references from 21 °C to 36 °C. Fig. 13 shows a significant temperature dependency with the average values.

Within 15 °C range a variation of 90% and 65% was observed respectively for 767 μS and 372 μS. This dependence is mainly due to the differential amplifier. Another gain stage topology should be used to prevent this dependence. Nevertheless, the constant transconductance bias circuit should stabilize the transconductance in all analog circuitry.

4.4. Power consumption

The total power consumption for the tested voltage supply of 1.135 V at 26 °C is lower than 1.175 μW. V_{REF} and V_{CMP} references are note included. Because consumption is proportional to conversion time, frequency should be maximized to reduce consumption. For the tested conductance range and at 20 kHz, the maximum consumption is lower than 8nJ. This are modest requirements that can be completed with a single 1.2 V cell or a super capacitor fed by conventional power scavenging techniques.

5. Conclusion

A new conductance conversion method was presented and tested through a implemented prototype. Although simple, this conversion method applies chopper stabilization and lock-in amplification techniques to provide noise suppression aiming to improve energy efficiency.

A prototype was designed in a discrete-time circuitry and implemented using a standard bulk CMOS process. Despite of its modest measurement performance, it proved to be suitable for low-power applications. The consumption of only 8nJ per conversion shows that such converter can be easily incorporated in self-powered devices.

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