Analog Integr Circ Sig Process (2013) 75:369–382
DOI 10.1007/s10470-013-0042-x

General-purpose high-speed integrated lock-in amplifier with 30 dB dynamic reserve at 20 MHz

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Received: 13 November 2012 / Revised: 1 February 2013 / Accepted: 6 February 2013 / Published online: 6 March 2013

Abstract We present the design of a general-purpose high-speed integrated lock-in amplifier (LIA). The LIA measures the amplitude and phase of the input signal with frequencies from 15 to 20 MHz at SNR as low as −30 dB. The magnitude measurement circuitry relies on the band-pass filter and current integrator to extract the signal amplitude. The phase measurement circuitry relies on the phase-locked loop to extract the phase difference between the input signal and the reference signal. The designed LIA is fabricated in TSMC 0.18 μm technology. The LIA consumes 37 mW of power. The output signal dynamic range is 300 mV for 600 mV input signal variation, and therefore the output-to-input sensitivity is approximately 0.5 V/V.

Keywords Lock-in amplifier · Phase-lock loop · High-speed amplifier

1 Introduction

Lock-in-amplifiers (LIAs) are well-known instruments that are widely used in physical and chemical sensing and materials spectroscopy applications [1–7]. LIAs aim to solve a common problem encountered in the data acquisition of weak (small amplitude current or voltage) signals that are distorted by noisy background signals. LIAs are capable of detecting signals embedded within considerable noise, where the noise power can greatly exceed the signal level in many applications [3–5]. Commercially available instrumentation LIAs such as the model SR830 from Stanford Research Systems Inc. [8] are widely used for signal detection in many general laboratory settings, where the signal frequency is <100 kHz range. The advantages of the instrumentation LIAs include setup convenience, large input and output signal dynamic range, large frequency range and huge dynamic reserve. Dynamic reserve refers to the maximum noise-to-signal ratio at the input where the LIA is able to extract the magnitude and the phase of the input signal. The drawbacks include high equipment cost and huge power consumptions, where system integration with other devices is greatly limited. On-chip integrated LIAs have also been designed such as in [9–10] for a few targeted applications, where the silicon area and power consumption of the LIA chip are suitable for miniaturized integration purposes.

Lock-in-amplifiers designed for high-speed applications where the signal frequency is in the MHz range are much less common. Currently, high-speed instrumentation LIAs offered by Stanford Research Systems Inc. [11] and Zurich Instruments Inc. [12]. These instruments offer excellent performance but at the expense of high power consumption and having a large table-top size equipment. To the Authors best knowledge, on-chip integrated high-speed LIAs are not reported in literature to date. In this paper, a general-purpose high speed integrated LIA is reported where the frequency operating range is between 15 and 20 MHz. The proposed design does not require any off-chip components and achieves 30 dB dynamic reserve with power consumption of 37 mW.

Low-speed LIAs typically use the phase-sensitive detection (PSD) technique to extract the amplitude and the

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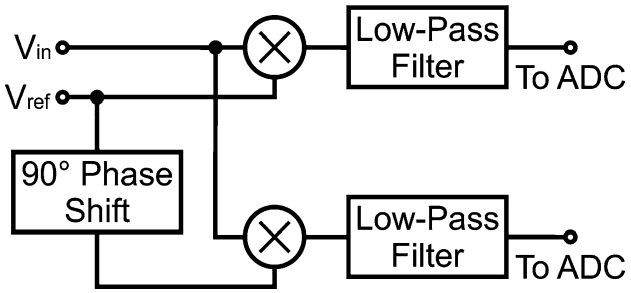

Fig. 1 The PSD technique used in low-speed LIA design

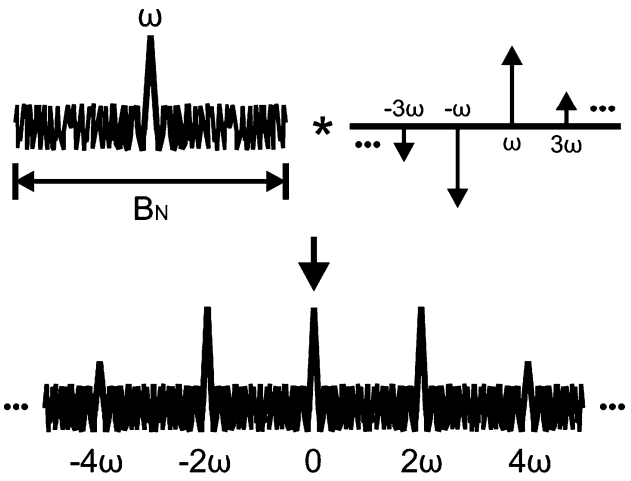

Fig. 2 Signal spectrum of the time multiplication before and after the mixer

phase of the input signal as illustrated in Fig. 1. The input signal is usually the sum of the signal to be detected and the noise with the spectrum spanning over a frequency range. After pre-amplification and filtering, the input signal is applied to two mixers. The reference signal with the same frequency as the input signal is also applied to the mixers. The reference signal is phase-shifted by 90° before it is applied to the second mixer. The corresponding signal spectrum is shown in Fig. 2. The input signal with frequency ω is embedded within noise with bandwidth B_N. The reference signal is usually generated by an on-chip oscillator, and the signal spectrum consists of tones at ±ω, ±3ω, and so forth. The convolution of the two signals leads to the tones at DC, ±2ω, ±4ω, and so forth. The tone at DC carries the information of the input magnitude and phase, and is the signal of interest. A low-pass filter following the mixer removes the undesired harmonics and the noise. The nth harmonic of the reference signal folds the high-frequency noise down to the baseband when $2n\omega < B_N$. Also, undesired tones at small frequency offset with respect to the input signal are usually hard to filter out. Therefore, a low-pass filter with narrow bandwidth and faster roll-off is highly desired. For a first-order low-pass filter with cut-off frequency f_{3dB}, the SNR improvement due to PSD is given by,

$$SNR_{After} = \frac{2B_N}{\pi f_{3dB}} SNR_{Before} \quad (1)$$

B_N is a modest approximation of the noise bandwidth as the total noise power is increased due to noise folding. While low pass filter with narrow bandwidth offers greater SNR improvement, the implementation usually requires extra large passive components, which is disadvantageous for on-chip integration.

Phase-lock loop (PLL) technique has been widely used in the communication receivers to recover signals embedded within noise. A PLL with small bandwidth averages the phase error between the input signal and the oscillator signal, where the input random phase variation is greatly suppressed by the feedback loop. A PLL is a well fit for on-chip integration, where highly integrated frequency synthesis and data recovery circuits based on PLL are widely used in wireless and wire-line applications. Also, PLL offers a huge frequency operating range from MHz to GHz, and is well suited for high-speed applications. One disadvantage of the PLL is that it can only keep track of the phase error of the input signal while the random amplitude variation of the input signal is ignored. Therefore, PLL is only used in the phase measurement in the proposed LIA, while the magnitude measurement is carried out with filters and time-average approach. The rest of this paper is organized as follow: Section II describes the structure of the designed LIA. Section III and IV describe the circuitry in the magnitude measurement and phase measurement components of the LIA, respectively. Section V presents the measurement results of the designed LIA. The paper is concluded in section VI.

2 System architecture

The architecture of the proposed LIA is shown in Fig. 3. The input sinusoidal signal to be measured is denoted as,

$$V_{SIG} = A_{SIG}(\cos \omega t + \theta_{SIG}). \quad (2)$$

The design is able to measure the amplitude of V_{SIG} with the amplitude measurement circuitry, and the relative phase difference between V_{SIG} and V_{REF} with the phase measurement circuitry. The measured amplitude and phase signals are denoted as V_{MAG} and V_{PH} as shown in Fig. 3. A band-limited white noise V_{NOISE} with the bandwidth B_N is superimposed on top of the input signal through an analog adder, where the signal-to-noise ratio is denoted as SNR_{in}. The analog adder is implemented based on OPAMP and resistors. A band-pass filter with bandwidth f_{BPF} follows the analog adder, and improves SNR_{in} to,

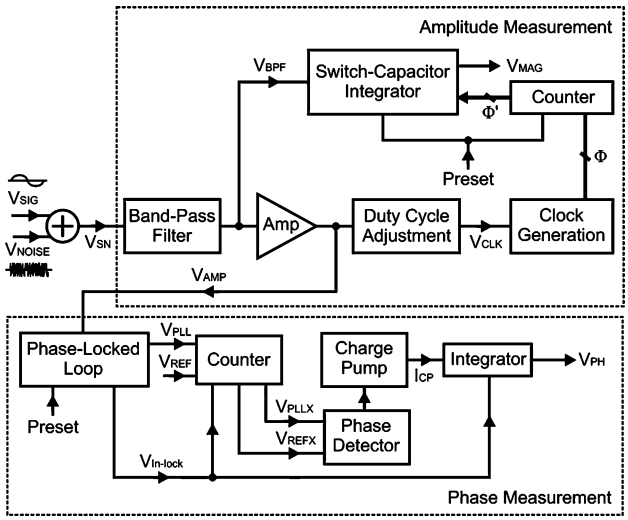

Fig. 3 The system architecture of the proposed integrated lock-in amplifier

$$SNR_{After-BPF} = \frac{2B_N}{\pi f_{BPF}} SNR_{in}, \tag{3}$$

where, f_{BPF} is much smaller than B_N. The simulated waveforms of V_{SIG} and V_{BPF} are shown in Fig. 4. For an arbitrary cycle j, the amplitude and phase of V_{SIG} are denoted as $A_{SIG,j}$ and $\theta_{SIG,j}$, where both $A_{SIG,j}$ and $\theta_{SIG,j}$ vary from cycle to cycle due to V_{NOISE}. A voltage amplifier increases the signal swing of V_{BPF} to rail-to-rail as shown in Fig. 4. A duty cycle adjustment circuit changes the duty cycle of V_{AMP} from 50 to 25 %. Since both V_{AMP} and V_{CLK} inherits the same $\theta_{SIG,j}$ from V_{BPF}, the falling edges of V_{CLK} approximately sample the peak amplitude of V_{BPF} as shown in Fig. 4. Multi-phase clock signals Φ are generated from V_{CLK}, and control a switch-capacitor integrator. The integrator calculates the average value (V_{MAG}) of A_{SIG} over N cycles, where,

$$V_{MAG} = \frac{1}{N}\sum_{j=1}^{N} A_{SIG,j}. \tag{4}$$

V_{AMP} is also used as the reference signal of a PLL with noise bandwidth B_{PLL}. The PLL attenuates the out-of band random phase variation of V_{AMP}, and further improves $SNR_{After\text{-}BPF}$ to,

$$SNR_{After-PLL} = \frac{\pi f_{BPF}}{2B_{PLL}} SNR_{After-BPF}. \tag{5}$$

The phase difference between V_{PLL} and V_{REF} are compared by a phase detector. The output of the phase detector controls a charge pump, which generates the I_{CP} signal where the time-averaged magnitude of I_{CP} is proportional to the phase difference between V_{PLL} and V_{REF}. I_{CP} over N multiple periods are added and averaged

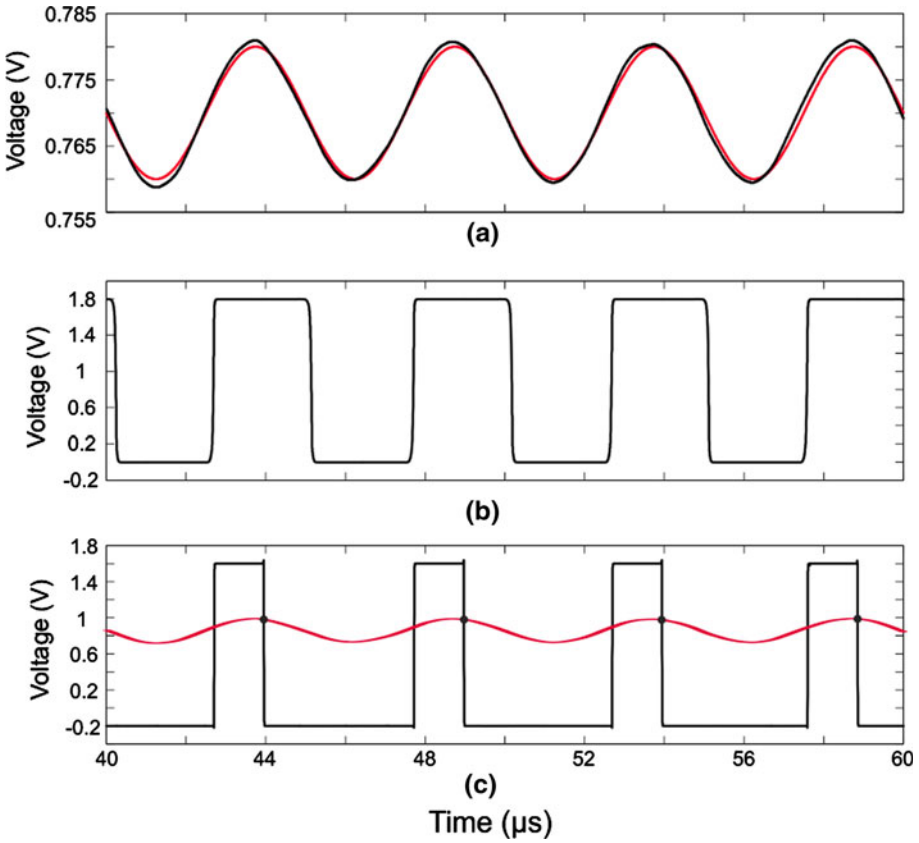

Fig. 4 Simulated transient voltage waveforms for amplitude measurement. **a** V_{SIG} (*red*) and V_{BPF} (*black*). **b** V_{AMP}. **c** V_{BPF} (*red*) and V_{CLK} (*black*)

by a current integrator, and the output signal V_{PH} is given by,

$$V_{PH} = \frac{K_{PH}}{N}\sum_{j=1}^{N}\left(\theta_{SIG,j} - \theta_{REF}\right), \quad (6)$$

where K_{PH} depends on the gain of the current integrator and will be derived later on. *N* for both the amplitude and phase measurements can be conveniently set by the digital counters.

3 Component descriptions of the amplitude measurement circuitry

This section describes the circuit components of the amplitude measurement section of the LIA in Fig. 1. It takes V_{SN} as the input, and generates a DC signal V_{MAG}, where the magnitude of V_{MAG} is proportional to the amplitude of V_{SIG}.

3.1 Band-pass filter

The circuit schematic of the gm-C band-pass filter is shown in Fig. 5 [13]. The center frequency and quality factor are given by,

$$\omega_C = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}}, \quad (7)$$

and

$$Q = \frac{\sqrt{g_{m2}g_{m3}}}{g_{m4}}\sqrt{\frac{C_1}{C_2}} \quad (8)$$

The feedback loop formed by trans-conductors two and three will oscillate for moderate g_m values, and trans-conductor one is able to stabilize the output voltage for large g_{m1} values at the cost of reduced filter quality factor. However, the effectiveness of trans-conductor one degrades as g_{m1} decreases. Therefore, trans-conductor four is added to make the filter quality factor independent of g_{m1}. The structures of the transconductors are differential to single-ended amplifiers. The center frequency is tunable by changing the biasing current of trans-conductor three, which effectively varies g_{m3}. By setting $g_{m2} = 4g_{m4}$ and $C_1 = 16C_2$, quality factor over 20 is achieved while the frequency tuning range is from 14 to 22 MHz.

The voltage amplifier following the band-pass filter increases the signal swing to rail-to-rail. Since V_{CLK} samples the peak value of V_{BPF}, it is critical that the amplifier bandwidth is high enough such that no phase shift exists between V_{BPF} and V_{AMP}. As a result, amplifier with common source configuration is employed due to its high bandwidth and large output dynamic range.

3.2 Duty-cycle adjustment and clock generation

The duty cycle of V_{CLK} is adjusted from 50 to 25 % through the circuitry shown in Fig. 6(a). An inverter-based voltage-controlled delay line (VCDL) as shown in Fig. 6(b) provides a quarter of a signal period time delay. An AND gate produces V_{CLK}, which is phase aligned with V_{AMP}. The time delay of the VCDL is adjustable through the current sources above and below the inverters.

V_{CLK} is converted into multi-phase clock signals Φ through the circuitry shown in Fig. 7. As shown in Fig. 8, the falling edge of V_{CLKB} triggers the falling edge of Φ_2, where the time delay T_1 is,

$$T_1 = T_{pd,Inv1} + T_{pd,NOR2\_2} + T_{pd,Inv4} + T_{pd,Inv5}. \quad (9)$$

Also, the falling edge of Φ_2 triggers the rising edge of Φ_3, and the time delay T_2 is given by,

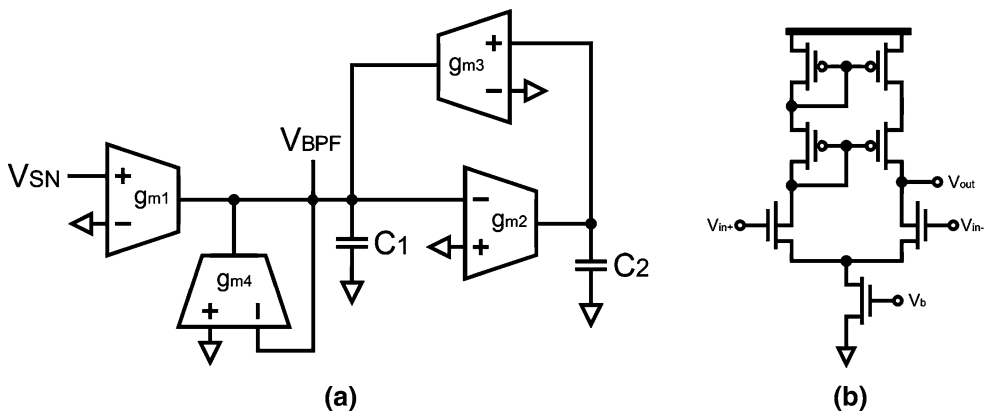

Fig. 5 **a** Schematic of the band-pass filter. **b** Schematic of the trans-conductance cell. Design parameters: $C_1 = 64$ pF, $C_2 = 4$ pF, $g_{m1} = g_{m2} = g_{m3} = 4g_{m4} = 1.59$ mA/V

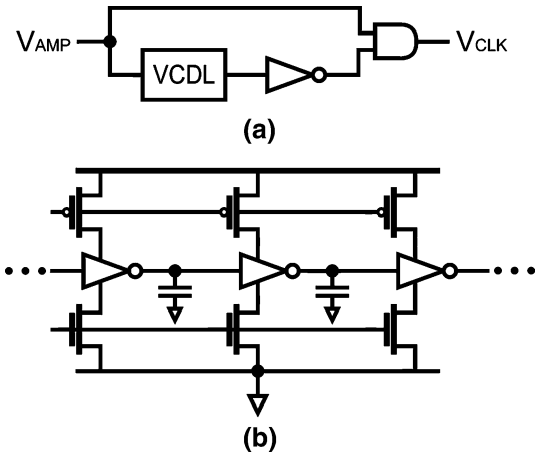

Fig. 6 **a** Duty cycle adjustment circuitry. **b** Inverter-based VCDL

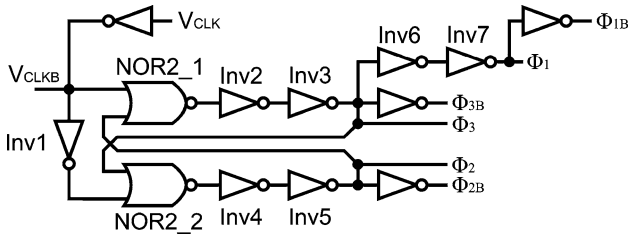

Fig. 7 Schematic of the clock generation circuitry

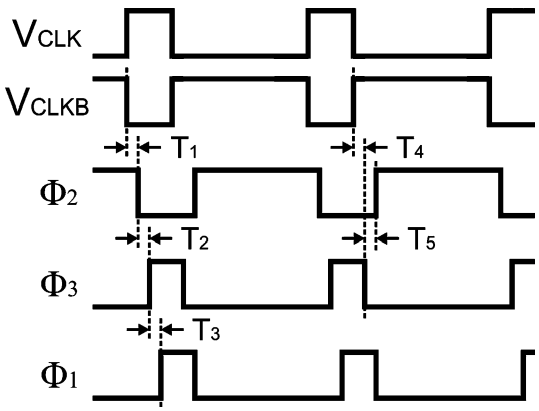

Fig. 8 Timing diagram of the multiple-phase clock

$$T_2 = T_{pd,NOR2\_1} + T_{pd,Inv2} + T_{pd,Inv3}. \quad (10)$$

Similarly, T_3 is given by,

$$T_3 = T_{pd,Inv6} + T_{pd,Inv7}. \quad (11)$$

T_4 equals to T_2, and T_5 is given by,

$$T_5 = T_{pd,NOR2\_2} + T_{pd,Inv4} + T_{pd,Inv5}. \quad (12)$$

The timing constraint requires that

$$T_1 + T_2 + T_3 < 0.25T_{CLK}. \quad (13)$$

At F_{CLK} equals to 20 MHz, Eq. (13) can be easily realized with CMOS sub-micron technology. Φ_1 is delayed with respect to Φ_3 to ensure that the charge injections due to the switches are input signal independent [14].

3.3 Programmable counter and switch-capacitor integrators

The integrating step in (4) is adjustable through the programmable count-down counter as shown in Fig. 9. The 4-bit counter consists of four S-R latch and D flip-flops (SR-DFFs). The count value is set through $P_{3\text{-}0}$, and the maximum count can reach 15. When Preset is set to logic-high, the initial count of the counter is set to $P_{3\text{-}0}$, and the end-of-count (EOC) signal is set to logic-low. The counter is triggered by setting Preset to logic-low. When the count reaches 0000, the EOC signal becomes logic-high, which forces all the inputs of the NOR-4 gate to logic-low. Therefore, EOC is kept logic-high thereafter until Preset becomes logic-high again.

After the instance where V_{CLK} causes the counter output to be 0000, the propagation delay through DFF_1, NOR4, and $MUX_{1,2}$ cannot be longer than the period of V_{CLK} as,

$$T_{pd,DFF1} + T_{pd,MUX1} + T_{pd,MUX2} + T_{pd,NOR4} < T_{CLK}. \quad (14)$$

Since T_{CLK} evaluates to 50 ns, (14) can be easily satisfied with CMOS sub-micron technology.

The schematic of the switch-capacitor integrator is shown in Fig. 10(a). When the EOC signal is logic-low, the clock signal $\Phi_{1,2,3}$ control the switches of the integrator. After EOC becomes logic-high, all the switches are turned off and V_{MAG} is held constant. A high-pass filter consisting of C_{HF} and R_{HF} is added to ensure that only the AC magnitude of V_{BPF} is integrated while the DC component is blocked. When Preset is set to logic-high, V_{MAG} is forced to be V_{AGND}. When Preset becomes logic-low, V_{MAG} becomes,

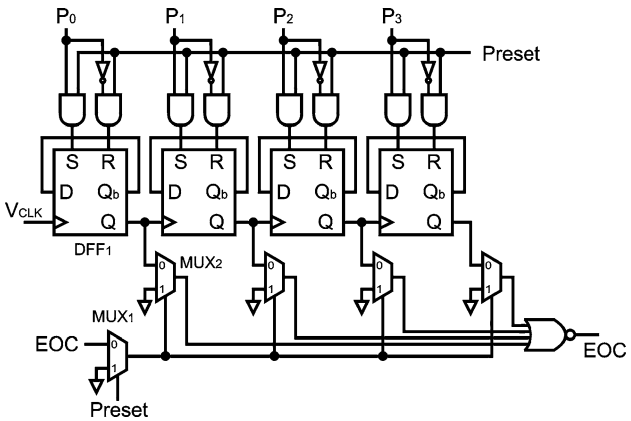

Fig. 9 Schematic of the 4-bit programmable counter in the magnitude measurement circuitry

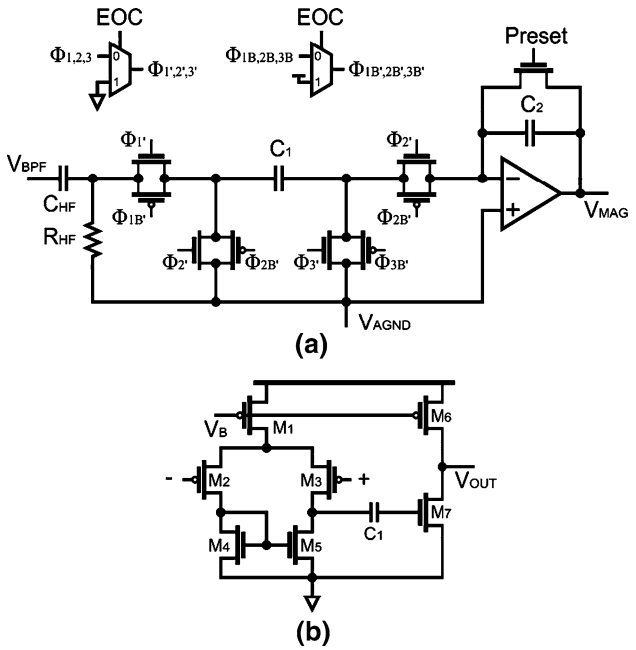

Fig. 10 **a** Schematic of the switch-capacitor integrator. PMOS and NMOS switches: W/L = 2/0.18 μm. $C_1 = C_2 = 2$ pF. **b** Schematic of the integrator OPAMP. Component parameters: $C_1 = 1$ pF, $W_{1,6} = 120$ μm, $W_{2-3} = 75$ μm, $W_{4-5} = 12$ μm, $W_7 = 24$ μm, $L_{1-7} = 0.18$ μm

$$V_{MAG} = V_{AGND} + \frac{C_1}{C_2}\sum_{j=1}^{N} A_{SIG,j} \tag{15}$$

after *N* cycles.

During the integrating phase of the operation, approximately $7\tau_{OPA}$ is required for the OPAMP output to settle within 0.1 % of the final value [15] where τ_{OPA} is the time constant of the OPAMP. Since the time duration allocated to the integrating phase is $0.75T_{CLK}$, if the final value is required to settle within $0.4T_{CLK}$, τ_{OPA} should be <2.857 ns. Since,

$$\tau_{OPA} = \frac{1}{\beta\omega_{UGB}}, \tag{16}$$

where

$$\beta = \frac{C_2}{C_1 + C_2}, \tag{17}$$

and ω_{UGB} is the unity-gain bandwidth of the OPAMP [15], ω_{UGB} should be larger than 111.4 MHz when C_1 equals to C_2. This is achieved through the OPAMP shown in Fig. 9(b). ω_{UGB} is designed to be 1.82 GHz, more than a decade above the required ω_{UGB}.

4 Component descriptions of the phase measurement circuitry

This section describes the implementation of the phase measurement circuit of the LIA as shown in Fig. 1. V_{AMP} is taken as the input of the PLL. The output signal V_{PH} is a DC voltage where the magnitude is proportional to the phase difference between V_{SIG} and V_{REF}.

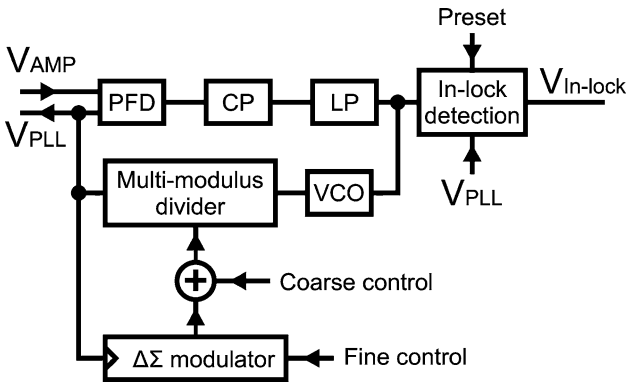

Fig. 11 Schematic of the fractional-N PLL

4.1 Phase-locked loop

The structure of the fractional-N phase-locked loop is shown in Fig. 11. The reference signal of the PLL is V_{AMP} where the random phase variation of V_{AMP} due to V_{NOISE} can be filtered out by the low-pass characteristic of the PLL. The transfer function of the PLL is given by,

$$\frac{\theta_{PLL}}{\theta_{REF}} = \frac{K_{PD}K_{VCO}F(s)}{sN + K_{PD}K_{VCO}F(s)}, \tag{18}$$

where K_{PD}, K_{VCO}, F(s) and N represent the gain of the phase detector, the gain of the VCO, the loop filter transfer function, and the feedback division value, respectively. At low frequency offset, the random phase noise passes to the output un-attenuated. As the frequency increases beyond the PLL loop bandwidth, the PLL can no longer track the reference phase variation thus the phase noise is effectively filtered at higher frequency offset.

4.1.1 The phase frequency detector and charge pump

The schematic of the PFD and the charge pump are shown in Fig. 12 and 13 respectively. The PFD is implemented based on CMOS logic, which is fully functional for the intended input frequency range. A well-known issue encountered with the PFD is the dead-zone problem, where the PFD and the charge pump cannot supply sufficient output current to the loop filter when the time difference between the reference signal and the feedback signal is smaller than the switch delay of the charge pump [16]. The reduced gain of the PFD directly leads to reduced loop bandwidth, which could make the PLL less stable. A common approach to resolve this issue is to add extra time delay in the PFD such that the propagation delay of the PFD is longer than the switch delay of the charge pump.

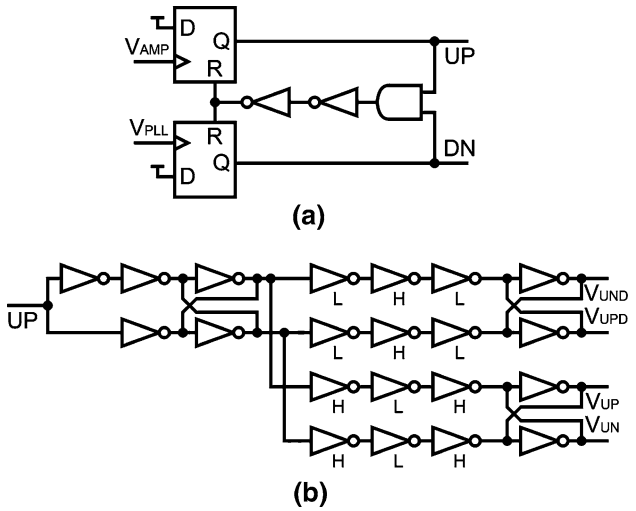

Fig. 12 Schematic of the phase-frequency detector

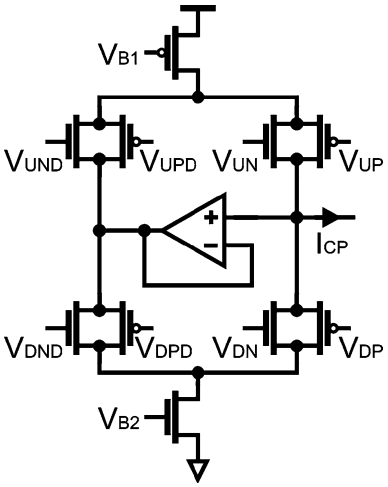

Fig. 13 Schematic of the differential charge pump

The apparent drawback of this approach is the addition of the extra phase error.

The UP and DN signal of the PFD are converted into eight control signals for the charge pump (identical circuitry for UP and DN signal) as shown in Fig. 12(b) [17]. The control signals of the charge pump switches should not turn both branches off at any time instance in order to avoid the glitch at the drains of the biasing transistors. Therefore, the falling edge of V_{UND} lags V_{UP}, and the rising edge of V_{UND} leads V_{UP} as shown in Fig. 14. To achieve the require timing waveforms, the threshold voltages of the inverters are adjusted as shown in Fig. 12(b), where Inverter-H has high switching threshold voltage by making the aspect ratio of the PMOS transistor much larger than that of the NMOS transistor, and vice versa. Also, cross-coupled inverters are used to ensure the phase alignment between V_{UP} and V_{UN}. The switch sizes are made minimum to reduce the charge

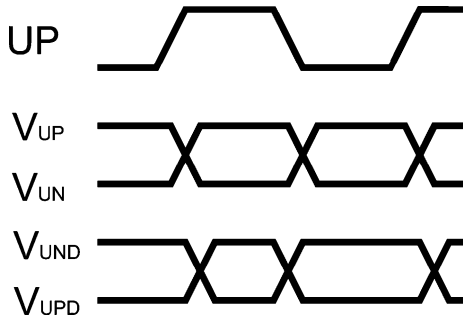

Fig. 14 Timing diagram of charge pump switch control

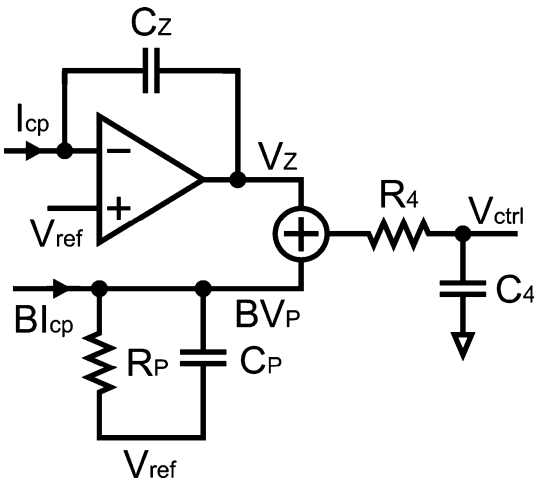

Fig. 15 Schematic of the dual-path loop filter

injection effect. A voltage follower in Fig. 13 is added to limit the charge sharing effect [16].

4.1.2 The loop filter

Since the PLL can only filter phase variation at frequency offset above the PLL loop bandwidth, lower PLL loop bandwidth is highly desired in the intended LIA applications. Large passive capacitor is usually required to achieve low PLL bandwidth, and is not suitable for on-chip integration. The dual-path loop filter proposed in [18] achieves the same loop bandwidth and dynamic range but with much smaller capacitance value as shown in Fig. 15. The loop filter requires two charge pumps with output currents I_{CP} and BI_{CP}. The first path of the loop filter consists of a current integrator, and the second path is a low-pass filter. The sum of the two paths is passed to another low-pass filter to attenuate the reference spur. The transfer function of the loop filter is given by,

$$F(s) = \frac{1}{sC_Z}\frac{1+s\tau_Z}{(1+s\tau_P)(1+s\tau_4)}, \tag{19}$$

where $\tau_Z = BR_PC_Z$, $\tau_P = R_PC_P$ and $\tau_4 = R_4C_4$. Therefore, for the same zero location τ_Z, the required capacitance C_Z

Table 1 Summary of the loop filter parameters

Component	Value
I_{CP}	26 μA
B	10
C_Z	163 pF
R_P	7.8 kΩ
C_P	68.4 pF
R_4	3.9 kΩ
C_4	137 pF

can be reduced by B times. The structure of the amplifier in the integrator path is a differential pair. The analog adder proposed in [19] is implemented in this design. The loop filter parameters are summarized in Table 1. Capacitors C_Z and C_4 are integrated on-chip.

From (19), the zero frequency is 12 kHz, and the frequency of the two poles is 300 kHz. The PLL loop bandwidth is given by,

$$K = \frac{I_{CP}K_{VCO}R_P}{2\pi N}\frac{C_P + BC_Z}{C_Z}, \tag{20}$$

which evaluates to 52.1 kHz when K_{VCO} equals to 78.4 MHz/V. Therefore, $K\tau_Z$ and $K\tau_P$ are approximately 4.3 and 0.174, respectively.

The PLL open-loop response is simulated as shown in Fig. 16. At low frequency, the magnitude response decreases at −40 dB/dec. The zero at τ_Z increases the slope to −20 dB/dec, and the two poles at τ_P and τ_4 decease the slope to −60 dB/dec. At the crossover frequency, the phase margin is approximately 57°.

4.1.3 LC voltage controlled oscillator

For low power applications, the top-biased complementary LC-VCO is implemented in this design as shown in Fig. 17 due to its better phase noise performance. L_1 is increased several times beyond the minimum length to reduce the flicker noise power of the biasing transistor. W_{2-3}/W_{4-5} is adjusted to ensure the half-cycle symmetry of the oscillating signal for better phase noise performance [20]. L_{2-5} is kept at the minimum length to reduce the impact of the M_{2-5} oxide capacitance on the frequency tuning range. L_6 is made large to extend the frequency tuning range at the expense of the degraded phase noise.

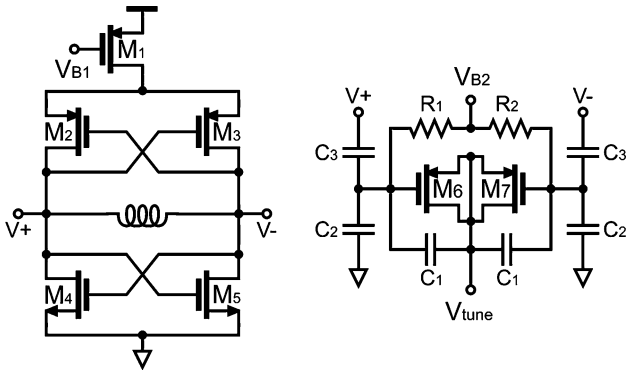

Fig. 17 Schematic of the top-biased complementary LC-VCO. Component parameters: $W_1 = 250$ μm, $W_{2-3} = 240$ μm, $W_{4-5} = 120$ μm, $W_{6-7} = 800$ μm, $L_1 = 1$ μm, $L_{2-5} = 0.18$ μm, $L_{6-7} = 3$ μm, $C_{1-2} = 5$ pF, $C_3 = 15$ pF

Passive capacitors C_{1-3} are added to reduce the biasing transistor flicker noise up-conversion effect at the cost of the reduced frequency tuning range. V_{B2} sets the biasing of the varactor, where the mid-point of the frequency tuning curve is biased at half point of the power supply.

The structure of the on-chip inductor is differential octagon implemented with single-layer top metal. The dimension of the inductor is optimized to achieve optimal quality factor over the intended operating frequency range. The performance of the LC-VCO is summarized in Table 2.

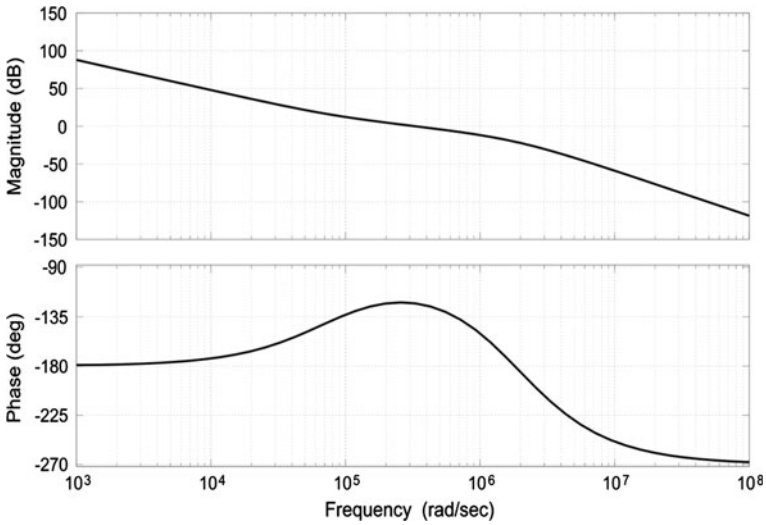

Fig. 16 Simulated bode plot of the PLL open-loop response

4.1.4 Multi-modulus programmable divider

For the required input frequency range 15–20 MHz and the VCO frequency tuning range, the feedback divider division ratio should reach at least 50. The multi-modulus divider proposed in [21] is implemented in this design, where the divider has five control bits and the maximum division ratio is 63. Since the maximum operating frequency is around 1 GHz, the entire divider is implemented with CMOS logic for lower power consumption. The divider output is taken from the same mod 2/3 block as the input signal for best phase noise performance.

Table 2 Simulated performance summary of the LC-VCO

Frequency tuning range	885–960 MHz
VCO gain	78.4 MHz/V
Power consumption	3 mA from 1.8 V
Phase noise @ 1 MHz	−126 dBc/Hz
Phase noise @ 3 MHz	−135 dBc/Hz
Inductor Q @ 960 MHz	5.8

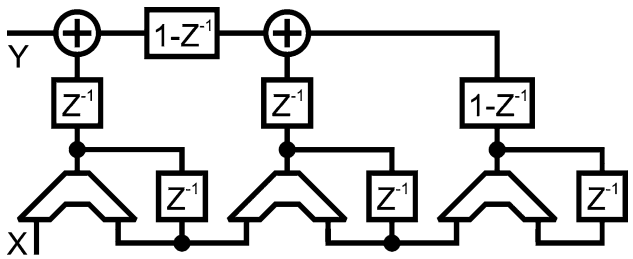

Fig. 18 Block diagram of the MASH ΔΣ modulator

4.1.5 ΔΣ Modulator

An all-digital 3rd-order 3-bit MASH ΔΣ modulator is designed as shown in Fig. 18. The three digital phase accumulators are implemented based on full adders and DFFs. The transfer function is given by

$$Y = Xz^{-3} + q_1\left(1 - z^{-1}\right)^3, \tag{21}$$

where, q_1 is the quantization noise of the first accumulator. Since the MASH ΔΣ modulator consists of three first order modulators, it is always stable while providing higher order noise filtering.

The narrow PLL loop bandwidth leads to relatively slow settling time. To improve the settling time, the VCO output frequency is held constant such that the input frequency hopping is offset by the variation of the feedback

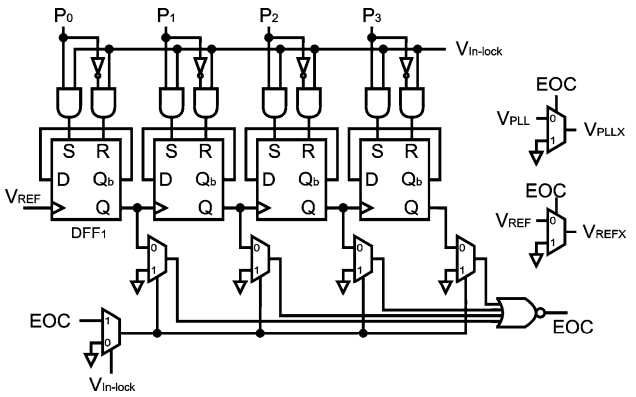

Fig. 21 Schematic of the 4-bit programmable counter in the phase measurement circuitry

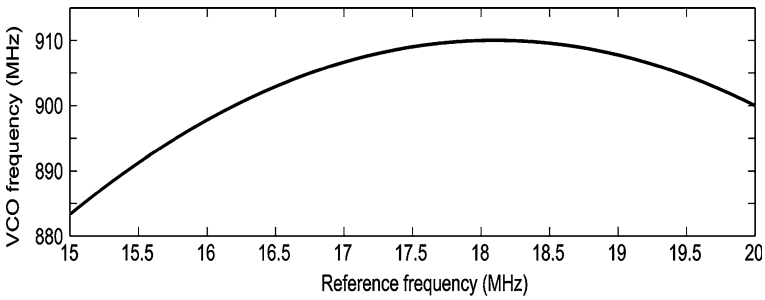

Fig. 19 VCO frequency variation with respect to the reference frequency due to variable feedback division ratio

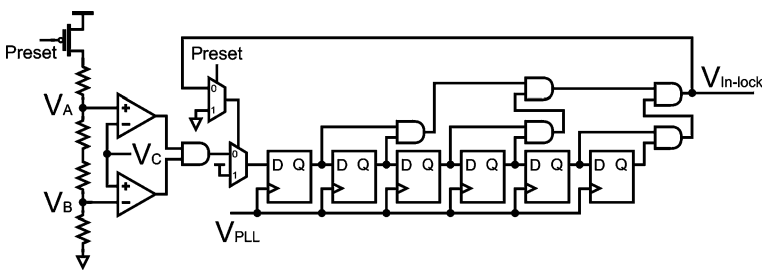

Fig. 20 Schematic of the in-lock detector

fractional-division ratio instead of the variation of the VCO frequency. For the 5 MHz reference frequency range, 112 equal frequency increment ΔF is allocated such that ΔF is approximately 45 kHz. The frequency span of each increment ΔF is,

$$F_{SPAN,m} = [20 - \Delta F \cdot m, 20 - \Delta F \cdot (m-1)], \quad (22)$$

where, m varies from 1 to 112. For the 3-bit MASH modulator, the resolution of the fractional-division ratio is 1/8. Therefore, for each $F_{SPAN,m}$, the corresponding feedback division ratio is set to,

$$D_m = 45 + \frac{m}{8}, \quad (23)$$

and the VCO output frequency is the product of $F_{SPAN,m}$ and D_m. The VCO frequency with respect to the reference frequency plot is shown in Fig. 19, where the VCO frequency varies within ±15 MHz over the targeted reference frequency span. For any interested input frequency between 15 and 20 MHz, the corresponding D_m is applied to the coarse and fine control in Fig. 11. The VCO frequency is forced to be adjusted slightly to compensate for the limited resolution of the MASH modulator, and the settling time of the PLL to lock to the new reference frequency can be greatly improved.

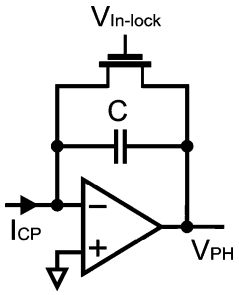

Fig. 22 Schematic of the current integrator

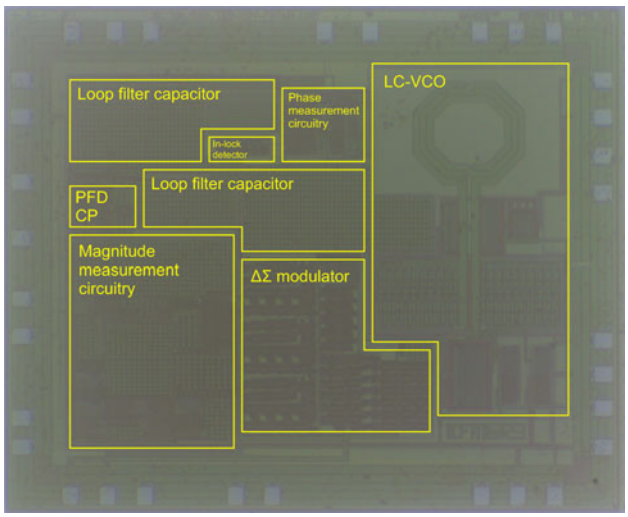

Fig. 23 Die micrograph of the fabricated high-speed LIA in TSMC 0.18 μm technology

4.1.6 *In-lock detector*

An in-lock detector is designed to monitor if the PLL has reached the locked state. The schematic of the in-lock detector is shown in Fig. 20, which takes the VCO control voltage V_C as the input. Since the VCO output frequency span is controlled within a small range, the VCO control voltage variation is also limited. When the PLL is in the locked state, V_C falls between the two boundaries set by V_A and V_B, and the output of the two comparators are both logic-high. Six DFFs are connected in series, where the clock is controlled by V_{PLL}. If V_C is within the range set by V_A and V_B for six consecutive cycles, $V_{In\text{-}lock}$ becomes logic-high to indicate that the PLL has reached the locked state.

When Preset signal is triggered, both V_A and V_B are logic-low, thus $V_{In\text{-}lock}$ is also forced to logic-low. When Preset is set to logic-low and $V_{In\text{-}lock}$ becomes logic-high, the input of the first DFF is also set to logic-high thus $V_{In\text{-}lock}$ is maintained at logic-high.

4.2 Programmable counter

The schematic of the 4-bit programmable counter is shown in Fig. 21. When $V_{In\text{-}lock}$ is at logic-low, the initial conditions of the SR-DFFs are set to $P_{3\text{-}0}$. Therefore, EOC signal is set to logic-low. When $V_{In\text{-}lock}$ is at logic-high and

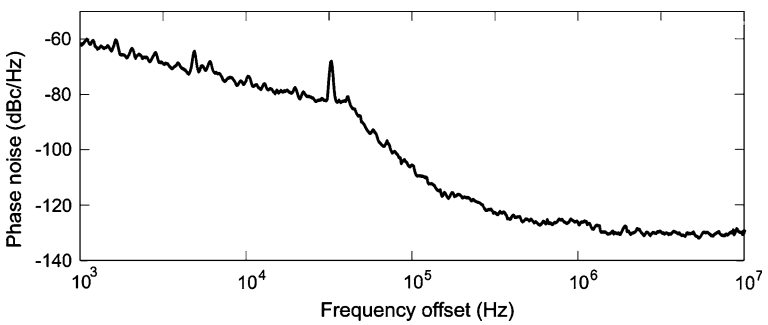

Fig. 24 Measured phase noise of the LC-VCO at 890 MHz output frequency

the counter has reached the 0000 state, EOC becomes logic-high to maintain EOC at logic-high. As a result, V_{PLLX} and V_{REFX} are set to logic-low to disable the downstream phase detector and charge pump.

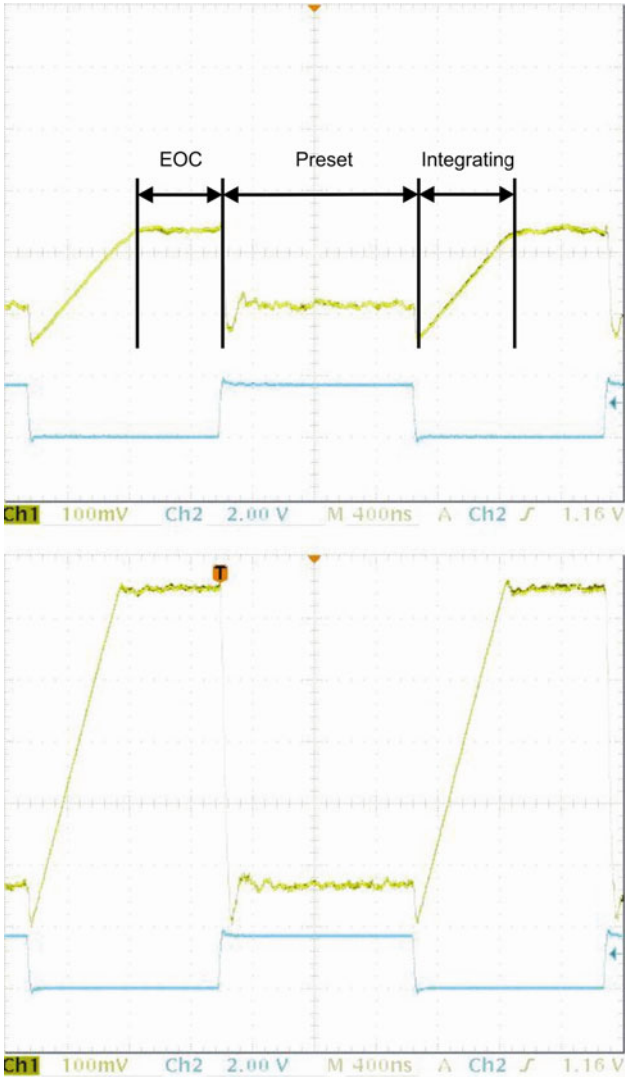

Fig. 25 Measured transient waveforms at the output of the magnitude measurement circuitry. *Top* 100 mV input signal amplitude. *Bottom* 700 mV input signal amplitude. *Yellow* V_{MAG}. *Blue* Preset signal

4.3 Current integrator

The phase difference between V_{PLL} and V_{REF} are measured by the phase detector and the charge pump. The charge pump current I_{CP} charges the current integrator in Fig. 22

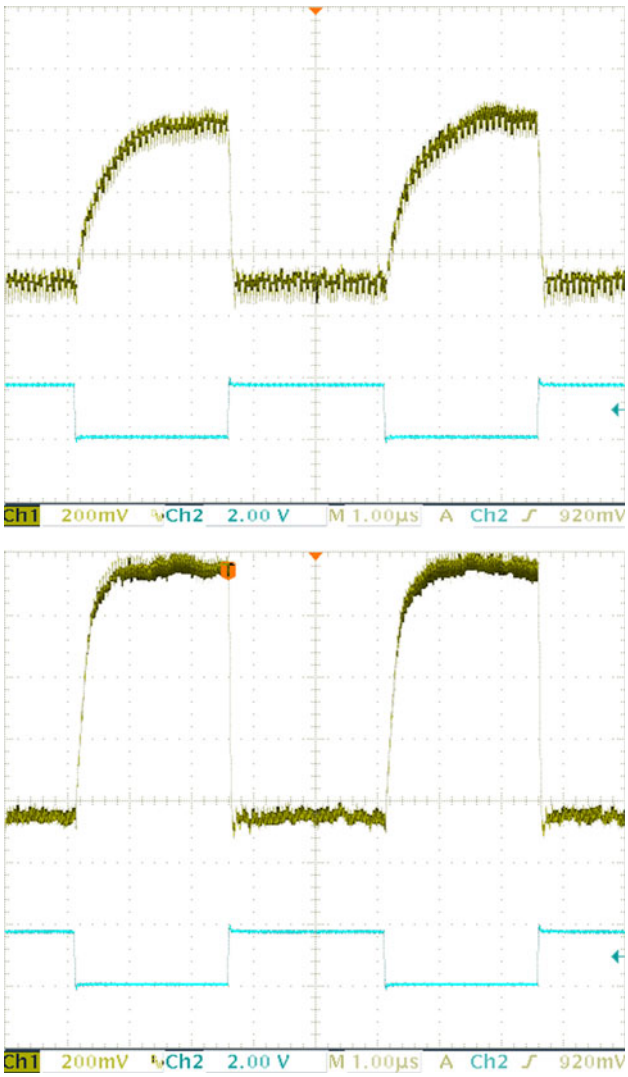

Fig. 27 Measured transient waveforms at the output of the phase measurement circuitry. *Top* 30° phase difference. *Bottom* 90° phase difference. *Yellow* V_{PH}. *Blue* Preset signal

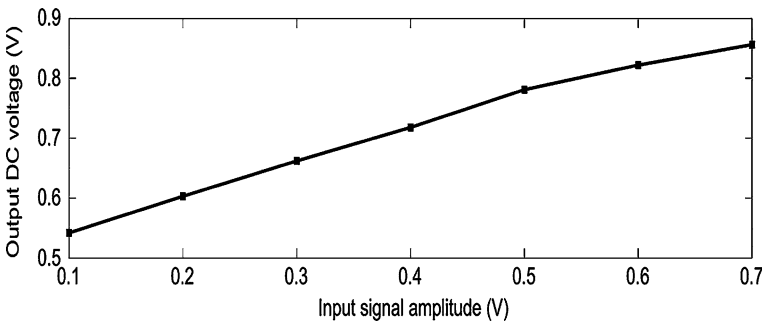

Fig. 26 Measured DC output voltage with respect to the input signal amplitude

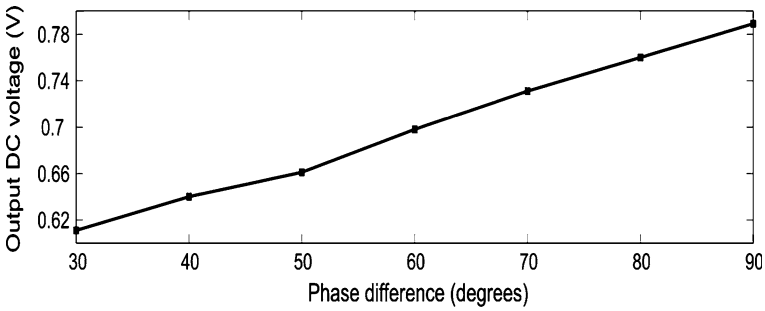

Fig. 28 Measured DC output voltage with respect to the phase difference between the input signal and the reference signal

Table 3 Performance comparison with existing LIA designs

	Frequency	Technology	Dynamic reserve	Power consumption	Output range
[4]	20 kHz	CMOS 0.7 μm	–	25 mW	0.3 to 0.55 V
[5]	30 kHz	CMOS 0.35 μm	40 dB	110 mW	−0.2 to 0.4 V
[22]	1 kHz	CMOS 0.18 μm	–	2 mW	1.04 to 1.18 V
[11]	25 kHz–200 MHz	–	80 dB	70 W	100 nV to 1 V
This work	15–20 MHz	CMOS 0.18 μm	30 dB	37 mW	0.54 to 0.85 V

for N periods set by $P_{3\text{-}0}$ of the programmable counter. The final voltage V_{PH} after N cycles is given by (6), where

$$K_{PH} = \frac{I_{CP}}{2\pi f_{REF} C}. \tag{24}$$

The same phase detector and charge pump in Fig. 12 and 13 are used in the phase measurement circuitry.

5 Measurement results

The designed high-speed integrated LIA is fabricated in TSMC 0.18 μm technology. The die micrograph is shown in Fig. 23, where the chip area is 5 mm^2 including the bond-pads. The die is bond-wired in the CFP80 package provided by Canada Microelectronics Corporation, and the chip is tested with the CFP80 testing fixture. The reference signal and the LC-VCO output are bond-wired externally to test the performance of the PLL. When the reference of the PLL is driven by a high-purity external signal, the measured VCO phase noise is shown in Fig. 24. The measured phase noise at 1 and 3 MHz frequency offset are −125 and −131 dBc/Hz at 890 MHz output frequency, respectively. The PLL loop bandwidth is <100 kHz, and the in-band phase noise is under 80 dBc/Hz.

Both V_{SIG} and V_{NOISE} in Fig. 3 are supplied with external power supply. At −30 dB SNR and 20 MHz input frequency, the measured transient response of V_{MAG} is shown in Fig. 25. During the preset phase, Preset signal is set to logic-high and V_{MAG} is forced to be V_{AGND} as described in Fig. 10. During the integration phase, Preset signal is set to logic-low, and the programmable counter is enabled. Maximum 15 integrating steps increase V_{MAG} to the DC voltage proportional to the amplitude of V_{SIG}. During the EOC phase, the switches of the switch-capacitor integrator are turned off, and V_{MAG} is held constant. The variation of V_{MAG} with respect to the amplitude of V_{SIG} is shown in Fig. 26. Approximately 300 mV variation of V_{MAG} corresponds to 600 mV variation of V_{SIG} amplitude, which translates to 0.5 V/V sensitivity.

Also, the measured transient response of V_{PH} at 20 MHz input frequency is shown in Fig. 27. The measured V_{PH} with respect to the phase difference between V_{SIG} and V_{REF} is shown in Fig. 28, where V_{PH} varies approximately 182 mV for 60 degrees of phase difference. The sensitivity of the phase measurement circuitry is 3 mV/degree at −30 dB SNR.

The performance of the high-speed LIA is compared with the existing designs (including integrated low-speed LIAs and commercial large-sized high-speed LIAs) in Table 3. Compared to the low-speed integrated LIAs from [4, 5, 22], the proposed LIA provides an decent output dynamic range while consuming relatively equivalent amount of power. The commercial large-sized high-speed instrumentation LIA in [11] well exceeds the dynamic reserve and output dynamic range performance compared to the proposed design. On the other hand, the proposed design offers an on-chip integrated approach to realize the magnitude and phase detection capability at much lower power consumption.

6 Conclusions

In this paper, a general-purpose high-speed integrated LIA is designed. The designed LIA consists of the magnitude and phase measurement circuitry components to extract the input signal magnitude and phase where the SNR can be as worse as −30 dB. The magnitude measurement circuitry relies on the band-pass filter and a current integrator to generate the V_{MAG} signal where V_{MAG} is directly proportional to the input signal amplitude. The phase measurement circuitry uses a low-bandwidth PLL and current integrator to generate the V_{PH} where V_{PH} is directly proportional to the phase difference between the input signal and the reference signal. The designed LIA is fully integrated and requires no off-chip components. It consumes 37 mW of power from 1.8 V power supply while providing reasonable output dynamic range, and magnitude and phase measurement sensitivity.

Acknowledgments We would like to acknowledge the financial support from *Natural Sciences and Engineering Research Council* (*NSERC*) of Canada. We would also like to acknowledge the financial support from McGill Engineering Doctoral Award (MEDA) to Hu. We would like to thank Canada Microelectronics Corporation (CMC) for providing the CMOS fabrication services.

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