3 GHz Frequency and Signal Level Meter

Built around a CPLD and a dsPIC microcontroller

This handy instrument measures frequencies from 50 MHz to 3 GHz with an accuracy of 10 ppm and provides an indication of the signal level over a range of –40 dBm to +10 dBm. Readings are displayed on a three-line LCD module, and the instrument is powered by three standard AA cells.

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A convenient battery-powered instrument is very practical for quickly measuring the frequency and level of HF signals. The instrument described here also features very high accuracy for frequency measurement. It has a 50-Ω HF input with a female SMA connector, suitable for connection to a cable or directly to an antenna. Of course, if you connect an antenna to the instrument you need to ensure that the level of the signal you wish to measure is sufficiently high relative to other signals that are also picked up by the antenna.

Basic architecture

The block diagram in **Figure 1** shows the general layout of the meter, with the HF portion and the digital portion distinguished from each other by different shading. The input signal is fed via a passive (resistive) splitter to the input stages of the two branches of the HF circuit: one for frequency measurement and the other for signal level measurement. The signal level measurement circuit essentially consists of a logarithmic

Features

- Frequency measuring range: 10 MHz to 3 GHz
- Frequency measurement error less than 10 ppm (0.001%)
- Signal level measuring range: –40 dBm to +10 dBm (0.1 µW to 10 mW into 50 Ω) over the range of 300 MHz to 2.8 GHz
- 146 readings per minute
- Power source: three 1.5 V AA cells or a 5 V AC mains adapter (min. 180 mA)
- Maximum current consumption at 5 V input: 170 mA
- Battery life with three 2000 mAh NiMH cells: 18 hours continuous operation without LCD backlighting or 11 hours with backlighting

detector IC made by Linear Technology. Frequency measurement requires a more complex circuit. It basically consists of a frequency counter implemented in an Altera CPLD, along with a frequency divider and a reference oscillator. Signal processing, control and display functions are provided by a Microchip dsPIC microcontroller.

Signal level measurement

An LT5538 logarithmic signal detector IC [1] from Linear Technologies is used to measure the signal level. Along with a frequency range of 50 MHz to 3 GHz, the selection criteria for this device were a dynamic range of at least 50 dB, an input sensitivity of –46 dBm, operation over the industrial temperature range of –40 to +85 °C, operation from a 3.3-V supply voltage, and the lowest possible price. Only three ICs meet the dynamic range requirements: the ADL5513, the LT5534 and the LT5538. We chose the LT5538 because it has the largest dynamic range of the three (75 dB).

This IC detects the power of the HF signal and outputs a voltage proportional to the power. This voltage is fed to an A/D converter in the microcontroller, and the digitised value is further processed by the microcontroller.

Unfortunately, the signal level output voltage from the LT5538 is highly frequency dependent. For this reason, we implemented a digital correction function using polynomial approximation. The signal level measurement function can be calibrated using a routine in the microcontroller firmware that is accessed from the display menu.

Frequency measurement

Frequency measurement is essentially based on a counting method implemented in the Altera Max-2 CPLD [2]. During the measurement cycle, one counter counts zero crossings of the signal being measured, while another counter counts zero crossings of the signal from the reference oscillator. The frequency can then be calculated from the counts accumulated by the two counters by using the formula:

frequency = (reference frequency) × (signal count) ÷ (reference count)

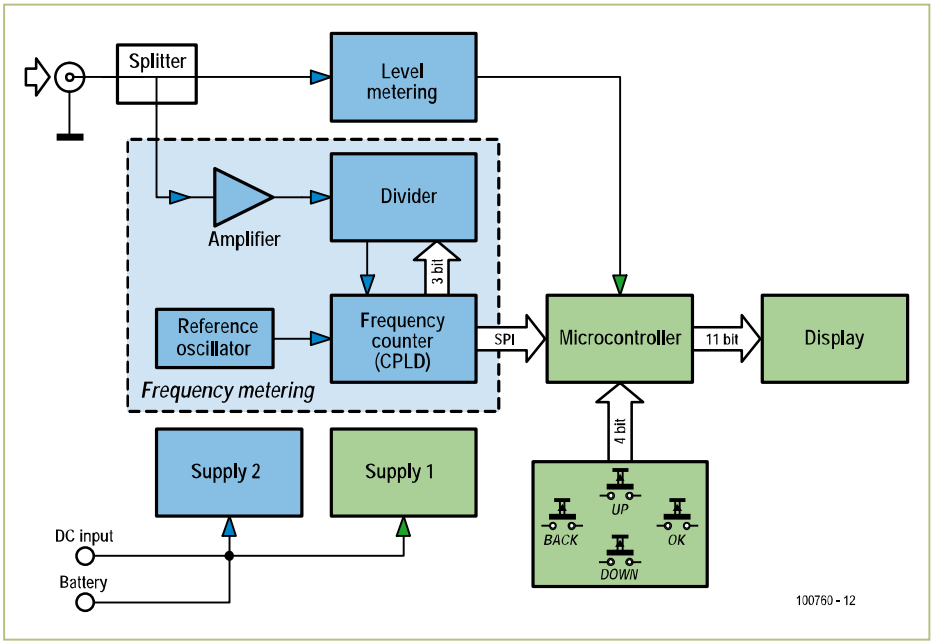


Figure 1. Block diagram of the frequency and signal level meter, with the HF portion shaded blue and the digital portion shaded green.

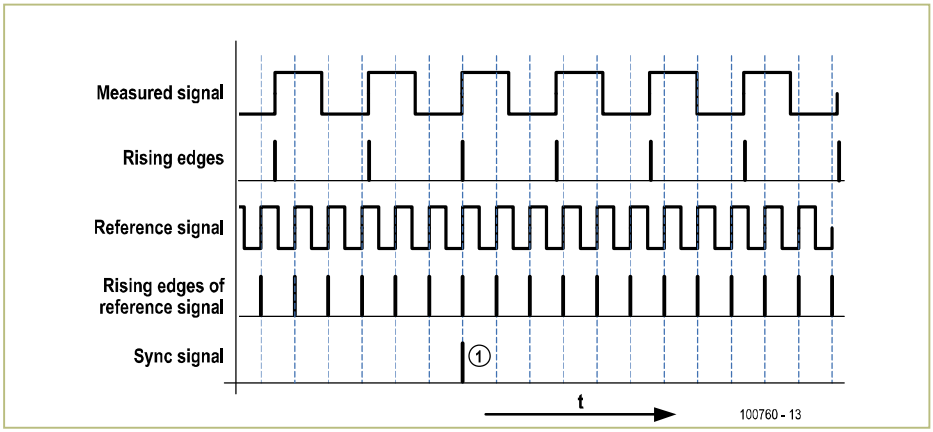


Figure 2. Timing diagram of the synchronisation logic in the CPLD. Frequency measurement using two counters starts and stops when the reference signal and the input signal both have rising edges at the same time.

Elektor Products & Services

- PCB: # 100760-1
- PCB layout files (free PDF download): # 100760-1.zip
- CPLD and dsPIC software (including source code): free download file # 100760-11.zip
- Items accessible through www.elektor.com/100760

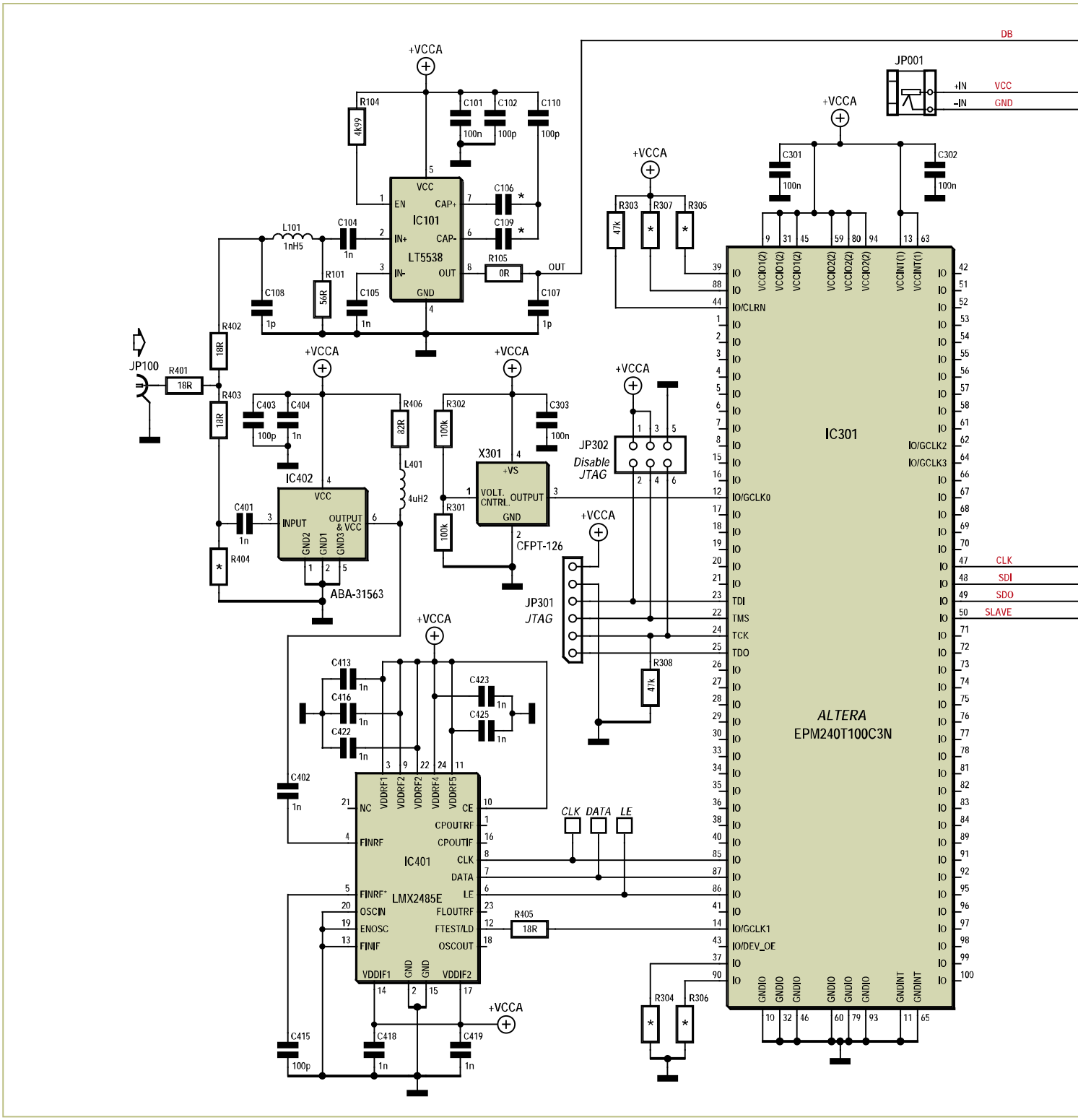
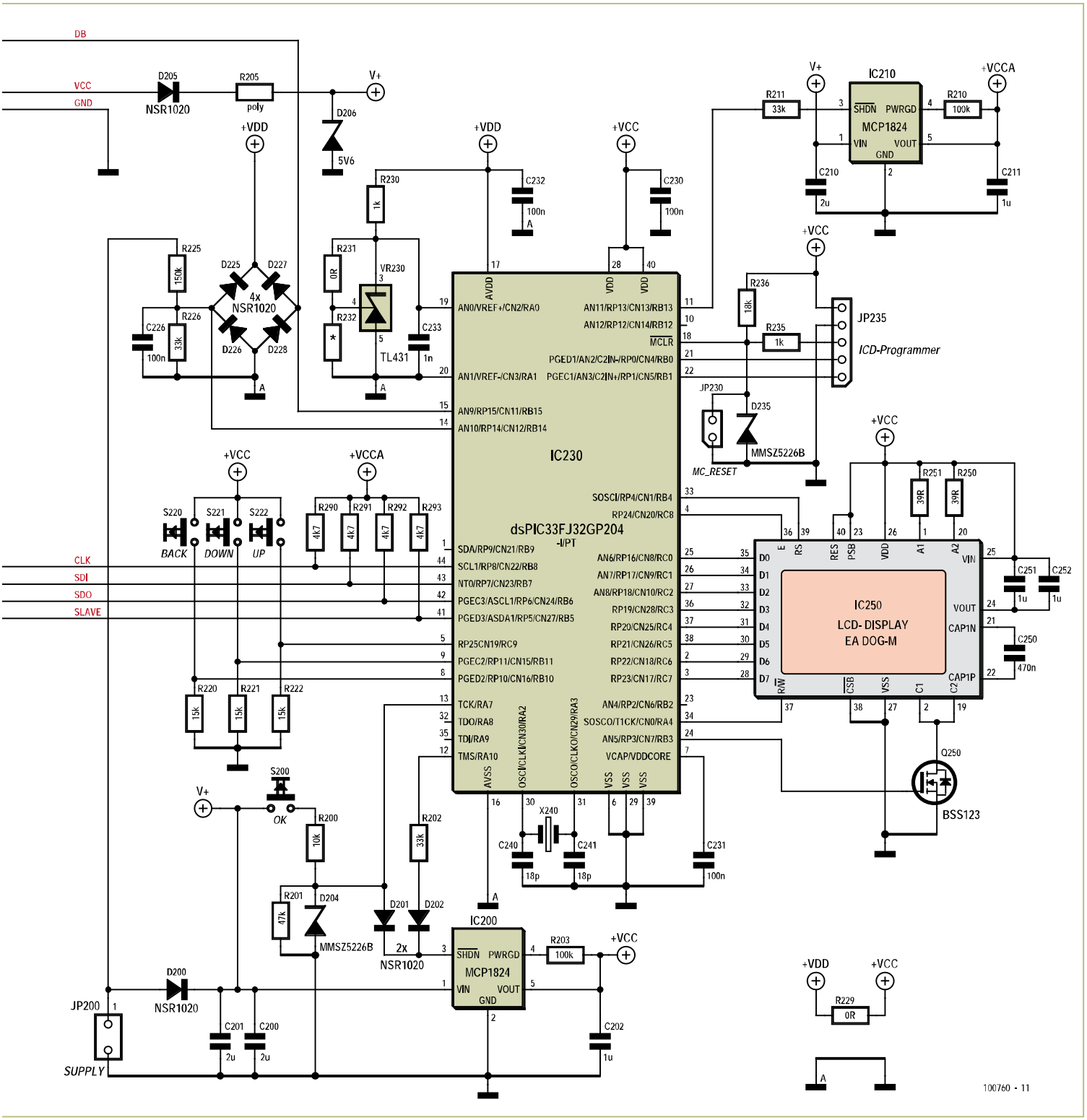


Figure 3. In the actual circuit, the HF portion on the left and the digital portion on the right

Synchronisation logic is programmed in the CPLD to increase the accuracy of frequency measurements. This logic ensures that the two counters used for frequency measurement are both started and stopped when the reference signal and the signal being measured have rising edges at the same time (see **Figure 2**). The counts accumulated by the two counters are sent to the microcontroller over an SPI bus.

The CPLD can process input signals up to approximately 200 MHz. A frequency divider is required to allow higher frequencies to be measured. Naturally, the division factor (in this case 32) is included in the calculation of the frequency. An LMX2485E PLL IC [3] from Linear Technologies is used here as the frequency divider. Only the inte-



are independent functional units with separate supply voltages.

grated frequency divider of this IC is actually used; the PLL function is not utilised. The advantage of this seemingly wasteful approach is that PLL ICs are manufactured in very large volumes and are therefore cheaper than pure HF divider ICs.

The internal settings of the PLL IC (including the division factor) must be configured every time the instrument is powered up. We were able to implement this directly in the CPLD, so the microcontroller is not needed for this function. This allows the frequency measurement portion of the circuit to operate as an independent, self-contained module that simply outputs data from its SPI port and can easily be used for other applications.

To improve the input sensitivity of the instru-

COMPONENT LIST

Resistors
(SMD0603)
R101 = 56Ω
R104 = 4.99kΩ
R105,R229,R231 = 0Ω
R200 = 10kΩ
R201,R303,R308 = 47kΩ
R202,R211,R226 = 33kΩ
R203,R210,R301,R302 = 100kΩ
R220,R221,R222 = 15kΩ
R225 = 150kΩ
R230,R235 = 1kΩ
R232,R293 = not fitted
R236 = 18kΩ
R250,R25 = 39Ω
R290,R291,R292 = 4.7kΩ
R304,R305,R306,R307,R404 = not fitted
R401,R402,R403,R405 = 18Ω
R406 = 82Ω

Capacitors
(SMD0603)
C101,C226,C230,C231,C232,C301,C302,C303 = 100nF
C102,C110,C403,C415 = 100pF
C104,C105,C233,C401,C402,C404,C413,C416,C418,C419,C422,C423,C425 = 1nF
C106,C109 = not fitted
C107,C108 = 1pF
C200,C201,C210 = 2µF
C202,C211,C251,C252 = 1µF
C240,C241 = 18pF
C250 = 470nF

Inductors
(SMD0603)
L101 = 1.5nH
L401 = 4.2µH

Semiconductors
D200,D201,D202,D205,D225,D226,D227,D228 = NSR1020 (SOD323-W)
D204,D235 = 3.3V zener diode (SOD123)
D206 = 5.6V zener diode (SOD123)
IC101 = LT5538
IC200,IC210 = MCP1824 (SOT23-5L)
IC230 = DSPIC33FJ32GP204-I/PT (TQFP44), programmed
IC301 = EPM240T100C3N (TQFP100), CPLD (Altera)
IC401 = LMX2485E (LLP24), PLL (National Semiconductor)
IC402 = ABA-31563 (SOT363), wideband amplifier (Avago)
Q250 = BSS123 or SN7002W (SOT23)
VR230 = TL431 (SOT23-5), voltage reference (TI)

Miscellaneous
IC250 = EA DOGM163W-A, 3.3V-LC-Display, 3x16 characters (Electronic Assembly)
JP001 = DC adaptor socket, PCB mount
JP100 = SMA socket, 142-0711-881 (Emerson/Johnson)
JP200 = (optional) 2-pin pinheader (battery connection)
JP230 = 2-pin pinheader with jumper (if required)
JP235 = 5-pin pinheader, right angled
JP301 = 6-pin pinheader, right angled
JP302 = 6-pin pinheader, 2-row (if required)
R205 = self healing fuse 30V/0.2A (SMD1210), Littlefuse 1210L020WR (e.g. Farnell 1596997)
S200,S220,S221,S222 = pushbutton, 1 make contact, PCB mount
X240 = 18MHz quartz crystal (HC49/SMD)
X301 = CFPT-126 (LF TVXO009920) from IQD, temperature compensated 40MHz SMD quartz oscillator (Farnell #1100757)
Enclosure: Bopla Type BS404 F-7035
PCB # 100760-1 (see www.elekor.com/100760)

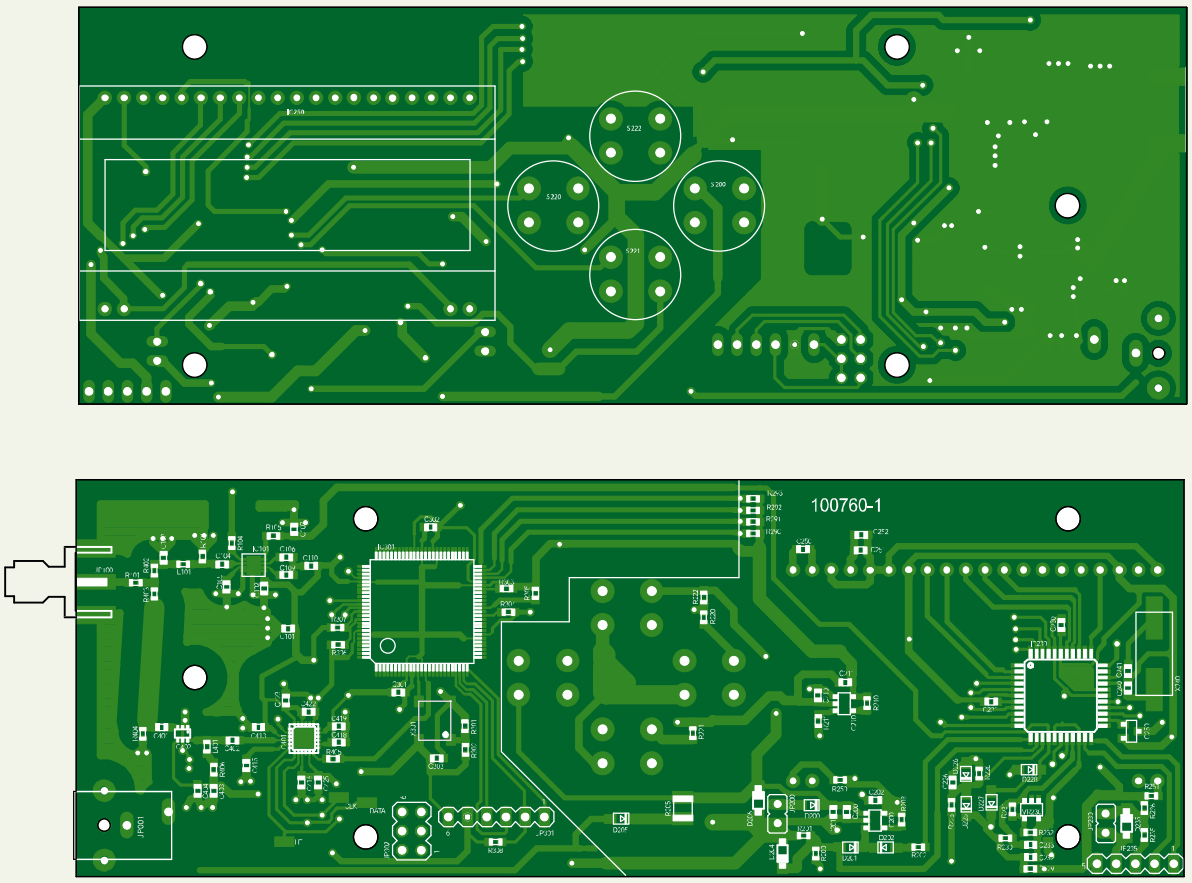


Figure 4. The PCB layout with exclusively SMD components on the bottom side.
Only the buttons and the display module are located on the top side.

ment and compensate for the attenuation of the passive splitter (–6 dB for each leg), a broadband HF amplifier is included ahead of the divider. The Avago ABA-31563 [4] device used for this purpose has 50 Ω input and output impedances and a frequency bandwidth extending from DC to 3.5 GHz, and it provides approximately 20 dB of gain. The HF amplifier operates in the saturation region in the presence of strong input signals.

Accuracy

The frequency measurement accuracy essentially depends on the accuracy of the reference signal. The readings cannot be more accurate than the oscillator frequency. In addition, the accuracy of the frequency measurement depends on the signal level and the frequency being measured. Fundamentally, the accuracy increases with increasing input signal level.
Despite signal level calibration, the signal level measurement can never match the accuracy of the frequency measurement (see the section 'Signal level calibration').
The achievable results are summarised in **Table 1**. From tests, we determined that the frequency measurement accuracy of our prototype unit was 1 ppm at room temperature.

Table 1. Measurement accuracy

Quantity	Accuracy	Range
Frequency	< 10 ppm (< 0.01 %)	50 MHz to 3 GHz –20 dBm to 0 dBm
	< 10 ppm (< 0.01 %)	700 MHz to 2700 MHz –35 dBm to +10 dBm
	< 1000 ppm (< 1 %)	300 MHz to 2700 MHz –40 dBm to +10 dBm
Signal level (calibrated)	4.3 dB	50 MHz to 3 GHz –40 dBm to +10 dBm

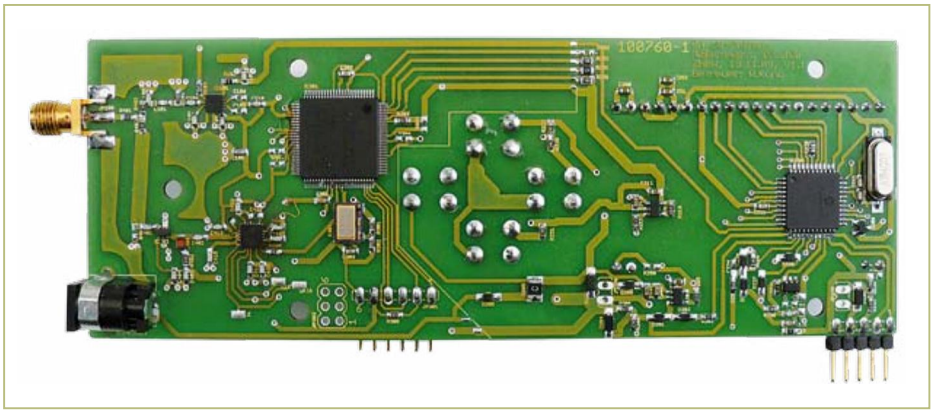


Figure 5. SMD side of the manually assembled Elektor lab prototype board.

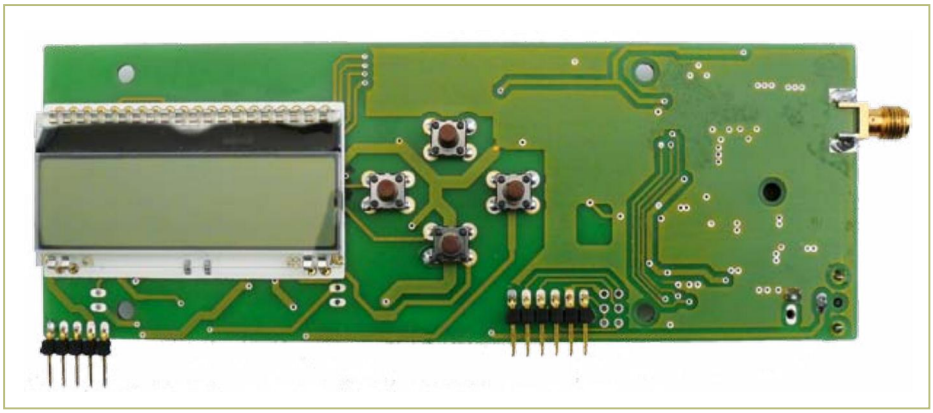


Figure 6. Top side of the Elektor lab prototype board.

Circuit description

The portions of the circuit shown with different shading in the block diagram (HF portion and digital portion) were originally built and tested on separate PCBs. In the course of device development, these two portions were merged on a single board. The corresponding full circuit diagram is shown in **Figure 3**.
Here again the HF portion on the left and the digital portion on the right are separate functional units that can be used independently of each other. To improve supply decoupling, the two portions of the circuit are powered by separate supply rails and voltage regulators, with IC200 for the digital portion and IC210 for the HF portion. Both voltage regulators provide a supply voltage of 3.3 V. The two voltage regulators receive their input voltage either from a battery pack connected to JP200 (three AA cells; voltage 3.6 to 4.8 V) or from a 5-V AC mains adapter connected to JP001. Voltage source selection is automatic: if the voltage on the AC adapter input is higher than the voltage from the battery pack connected to JP200, diode D200 is reverse biased and isolates the battery pack. This diode also provides protection against reverse-polarity battery connection. A series diode in the AC adapter input circuit provides similar reverse polarity protection and prevents reverse current flow. A Polyfuse (self-healing thermal fuse) and Zener diode are connected after this diode. This combination protects the circuit against excessive voltage and limits the current in case of a fault. The HF and digital portions are connected only by the four SPI bus lines and the signal detector output line (and of course by a common ground point). The CPLD sends the counts from the frequency measurement counters to the dsPIC over the SPI bus, and the dsPIC uses this data to generate the frequency reading shown on the LCD module and to apply frequency correction to the

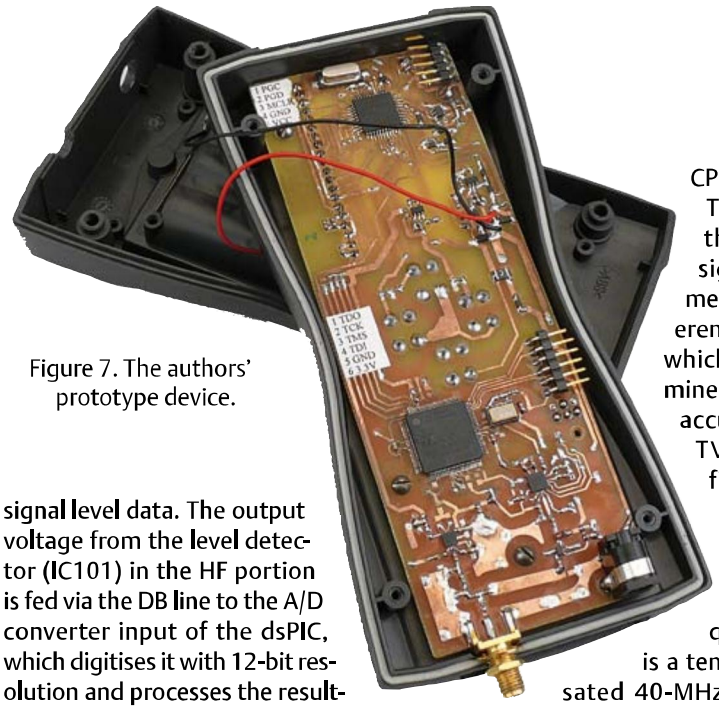


Figure 7. The authors' prototype device.

signal level data. The output voltage from the level detector (IC101) in the HF portion is fed via the DB line to the A/D converter input of the dsPIC, which digitises it with 12-bit resolution and processes the resulting values with the previously mentioned frequency-dependent correction to obtain the readings shown on the LCD module. Diodes D225–D228 limit the voltage on the dsPIC A/D converter input (pin 15) to prevent overdriving. The dsPIC monitors the battery voltage on a separate analogue input (pin 13); this voltage is reduced to a suitable level by a voltage divider (R225/R226). The TL431 reference voltage source (VR230) provides a 2.5-V reference voltage for the A/D converter in the dsPIC.

The user interface consists of four pushbutton switches (S200 and S220–S222) and the three-line LCD module, with the backlight switched via Q250. The LCD module operates from a supply voltage of 3.3 V and features high contrast with automatic adjustment and very low current consumption (just 250 µA without backlighting).

In the HF portion, it's easy to recognise the elements of the block diagram. The signal splitter after the 50-Ω SMA connector consists of just three resistors (R401–R403). Passive splitting of the input signal into two signals for input to the level detection circuit and the frequency measurement circuit results in a loss of 6 dB for each path, which is why an amplifier (IC402) is placed ahead of the input to the PLL IC (IC401), which as already mentioned is used solely as a prescaler (frequency divider). This prescaler must be configured by the CPLD each time the instrument starts up, for which reason the PLL IC's Microwire interface port (which is compatible with SPI) is connected to the CPLD (IC301).

The CPLD receives the reference clock signal for frequency measurement from reference oscillator X301, which effectively determines the measurement accuracy. The type LF TVXO009920 specified in the components list, which is a member of the CFPT 126 family from IQD Frequency Products, is a temperature compensated 40-MHz crystal oscillator with an operating temperature range of -40 °C to 85 °C. It is compatible with 3-V logic and has a frequency stability of ±0.5 ppm, which is equivalent to just 20 Hz at 50 MHz. Of course, this accuracy comes at a price, and if you do not need such high accuracy you can use a more economical oscillator instead.

If you have access to a high-accuracy frequency counter for comparative measurement, you can improve the accuracy of the LF TVXO009920 by trimming the values of resistors R301 and R302. In the second prototype built by the authors, the measured frequency error at 40 MHz was -15 Hz (0.38 ppm) with the standard resistance value of 100 kΩ for R301 and R302. The authors were able to reduce the error to +5 Hz (0.125 ppm) by lowering the value of R302 (with R301 = 94.68 kΩ, R302 = 100 kΩ).

The CPLD is programmed via the JTAG port (JP301). Jumpers on the pin header labelled 'JTAG Disable' are used to select either programming mode or operating mode for the CPLD. If desired, after the CPLD has been programmed you can replace the pin header and jumpers by solder bridges.

JP25 in the digital portion of the circuit is an ICD programming and debugging port for the dsPIC microcontroller. Jumper JP230 can be used to manually reset the microcontroller if necessary.

PCB

All SMD components are fitted on the bottom of the double-sided, through-hole plated PCB (**Figure 4**). Only the four buttons and the display module are located on the top of the board. **Figures 5** and **6** show the fully assembled prototype developed in the Elektor lab, while **Figure 7** gives an impression of the authors' prototype.

In both cases the SMD components were placed and soldered by hand, which is not easy (especially with the PLL IC). However, the advantage of using manual assembly instead of reflow assembly is higher accuracy of the SMD reference oscillator frequency. This means that only electronics enthusiasts who are truly experienced in handling SMD devices should attempt this demanding project.

After the board has been assembled correctly, you need a Byteblaster or USB Blaster programming interface and the Quartus programming environment to program the CPLD. For the dsPIC, you need MPLAB from Microchip and an ICD programmer. Everything else (VHDL code, source code, hex files and programming instructions) are available in the software download package on the Elektor website [5].

Display

The readings are shown on the LCD module in a very straightforward manner. The first line displays the text 'Frequency / Level', the second line displays the frequency in MHz, and the third line displays the signal level in dBm. The display menu also supports calibration of the instrument and viewing status information, such as the battery voltage. The four buttons, whose functions are described in **Table 2**, are used for menu selection and parameter configuration.

The menu scheme is designed to always

Table 2. Menu functions of the pushbutton switches

S200	OK (confirmation) and switching on the instrument
S220	Back (return to previous menu level)
S222	Increase value or move up in menu
S221	Decrease value or move down in menu

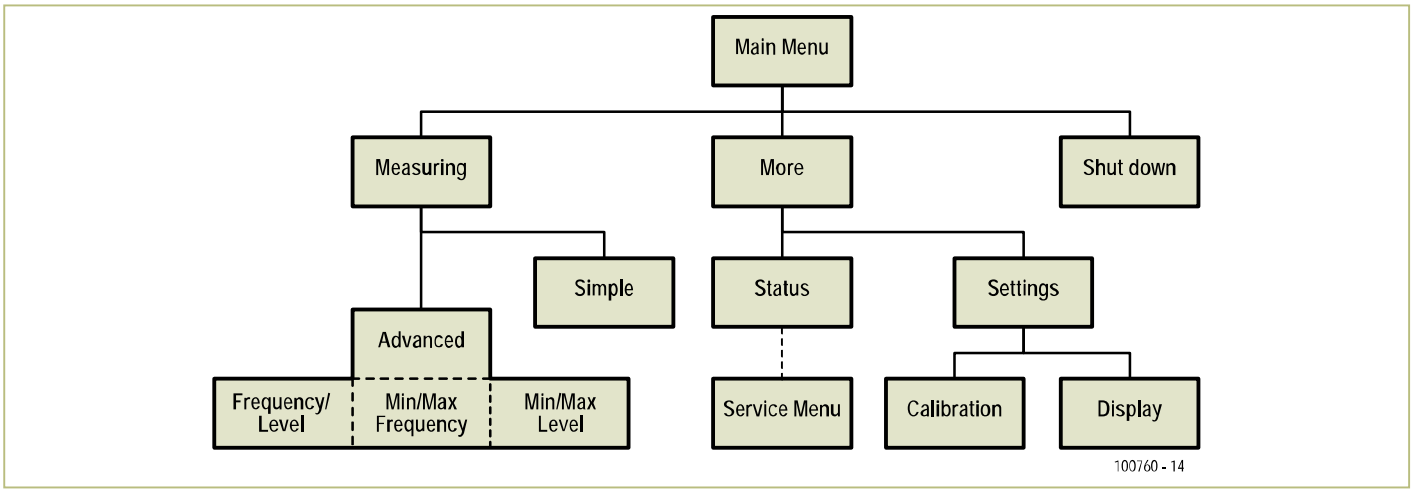


Figure 8. Menu structure of the microcontroller software.

show the name of the currently selected menu in the top line of the display The menu structure of the software is illustrated in **Figure 8**. Here it should be noted that in the 'Measuring / Advanced' menu, switches T3 and T4 can be used to select either 'Frequency / Level', 'Min/Max Frequen.' or 'Min/Max Level'. The 'Service' menu can be selected in the 'Status' menu by pressing buttons T3 and T4 at the same time. In the 'Service' menu you can display the raw signal level data (A/D value) and switch power to the HF portion on or off via IC210, thereby either enabling or disabling the frequency and signal level measurement functions.

Signal level calibration

The LT5538 used for signal level detection has a very large dynamic range, but it has the drawback that the output voltage is highly frequency dependent. Although signal level measurement can be calibrated very precisely within a narrow frequency band, it is rather inaccurate over the desired broad frequency range. Fortunately, the frequency dependence of the detector output can be corrected, at least partially, by taking advantage of the fact that the frequency of the measured signal is known. Using the measured frequency value, the microcontroller can convert the detected signal level to the correct value. For this purpose, the firmware provides a separate 'Calibration' menu. To perform the calibration, which is based on the least squares method, you need a frequency generator with an adjustable frequency range of 100 MHz to 3 GHz and an adjustable signal level range of –40 dBm to +10 dBm.

Use the following procedure to calibrate signal level measurement:

1. Select the 'Calibration' menu.
2. Enter the indicated frequency and signal level.
3. Confirm the entered values.
4. Enter the next set of indicated frequency and signal level values.
5. Repeat this for all of the indicated values
6. After a short computation time, the calibration process is completed and the data is stored permanently in the flash memory of the microcontroller.

Even with this calibration, the signal level readings are less accurate than the frequency readings. The largest measured error was 4.3 dB.

Development potential

In addition to many stimuli for developing your own devices in the domain of truly high frequencies (including PCB layout aspects), this project provides an introduction to CPLD programming. Thanks to the open source software (VHDL code and dsPIC source code in C), you can easily adapt the instrument to meet your specific needs or use it for other applications. The authors used MPLAB IDE v8.30 and the MPLAB C30 C compiler to develop the microcontroller firmware. They also used Quartus II v7.0 to develop and download the CPLD logic.
Expanding the functionality would require a CPLD with more macrocells. Additional pads for a CPLD with more memory are already present on the PCB. If such a device is fitted, 0-Ω resistors must be fitted in positions R304, R305, R306 and R307.
There is also room for improvement in the signal level measurement function, assuming you have access to good test equipment. With regard to the hardware, you could try to minimise reflections at the amplifier input by using an impedance matching network. Possible software modifications include the ability to select different calibration points or more calibration points, and you might want to try using higher-order polynomials for correction of the signal level reading.

(100760-I)

Internet Links

[1] http://cds.linear.com/docs/Datasheet/5538f.pdf (LT5538-1 data sheet)

[2] www.altera.com/literature/hb/max2/max2_mii5v1_01.pdf (MAX II CPLD data sheet)

[3] www.national.com/ds/LM/LMX2485.pdf (LMX2485 data sheet)

[4] www.avagotech.com/docs/AV02-1782EN (ABA-31563 data sheet)

[5] www.elektor.com/10076

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Martin Bachmann and Daniel Schär studied Electrical Engineering at the Zurich University of Applied Sciences Winterthur in Switzerland. They developed the instrument described in this article as part of a project carried out during their studies.