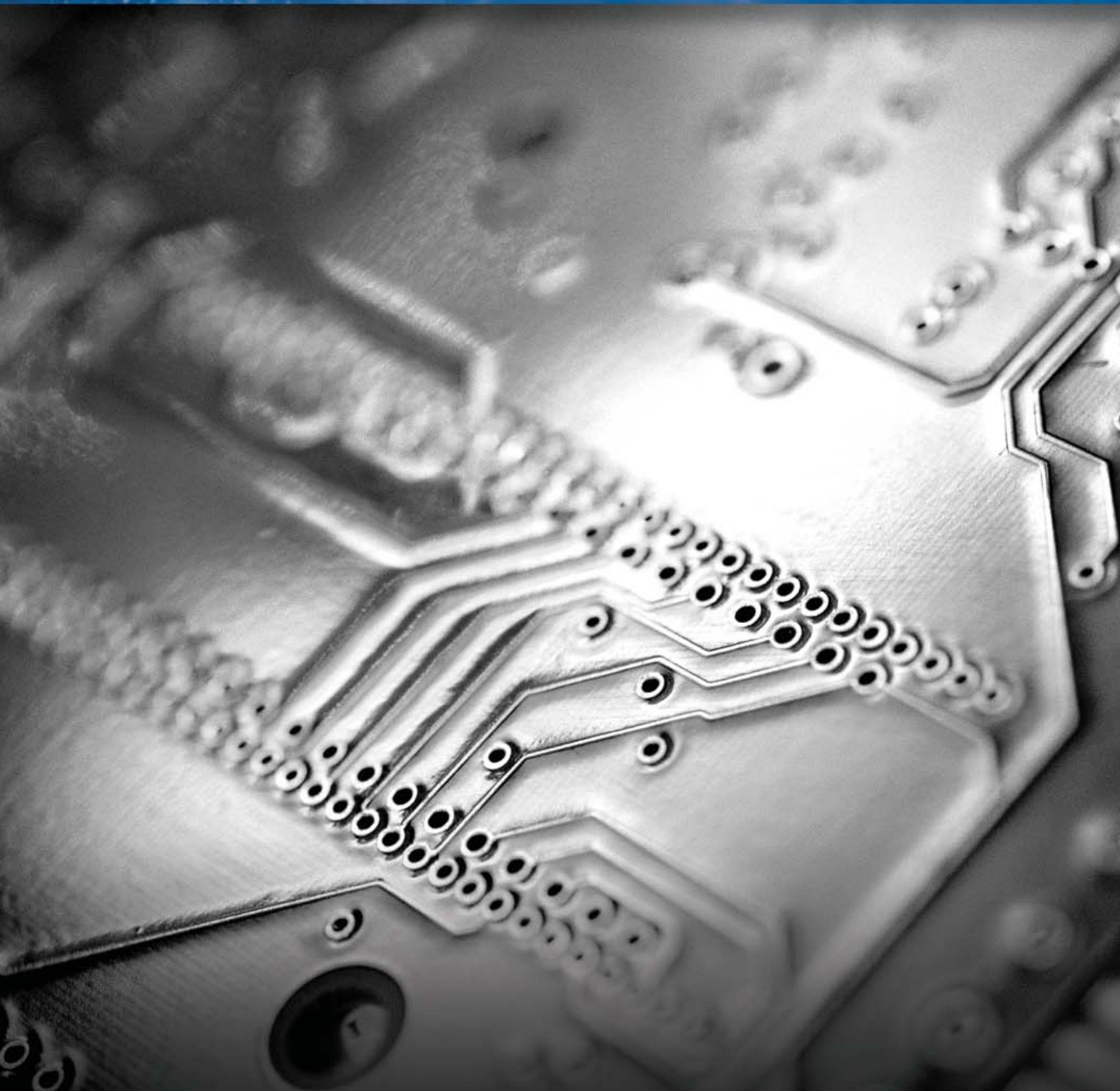
DL131/D
Rev. 5, Jan-2005

ON Semiconductor®

CMOS Logic



CMOS Logic Data

DL131/D
Rev. 5, January−2005

ON Semiconductor™

PUBLICATION ORDERING INFORMATION

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CHAPTER 1
Selector Guide

CMOS Selection Guide by Function

CHAPTER 2
Data Sheets

MC14001B Series

B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin−for−Pin Replacements for Corresponding CD4000 Series B Suffix Devices

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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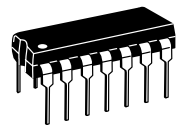
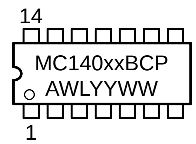
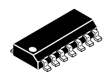
MARKING DIAGRAMS

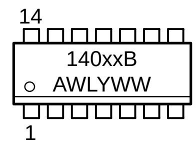


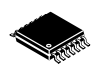
PDIP−14
P SUFFIX
CASE 646



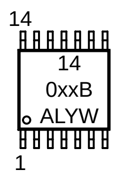


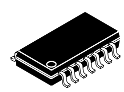
SOIC−14
D SUFFIX
CASE 751A



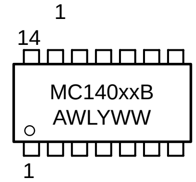


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965



xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

DEVICE INFORMATION

Device	Description
MC14001B	Quad 2−Input NOR Gate
MC14011B	Quad 2−Input NAND Gate
MC14023B	Triple 3−Input NAND Gate
MC14025B	Triple 3−Input NOR Gate
MC14071B	Quad 2−Input OR Gate
MC14073B	Triple 3−Input AND Gate
MC14081B	Quad 2−Input AND Gate
MC14082B	Dual 4−Input AND Gate

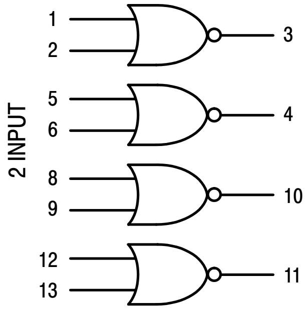
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

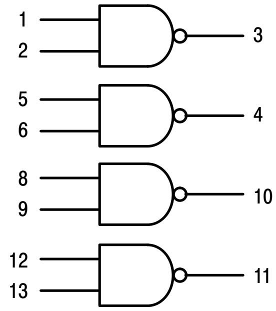
LOGIC DIAGRAMS

NOR | **NAND** | **OR** | **AND**

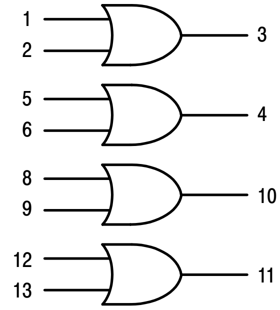
MC14001B
Quad 2−Input NOR Gate



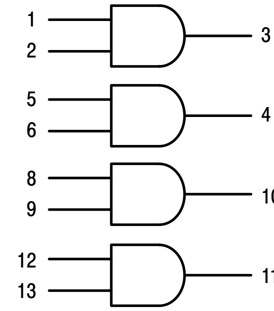
MC14011B
Quad 2−Input NAND Gate



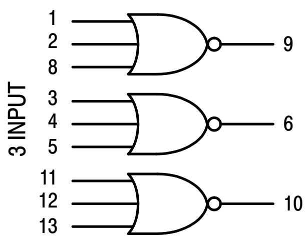
MC14071B
Quad 2−Input OR Gate



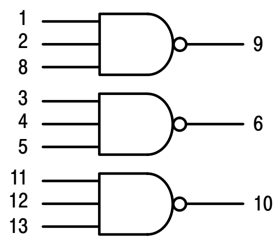
MC14081B
Quad 2−Input AND Gate



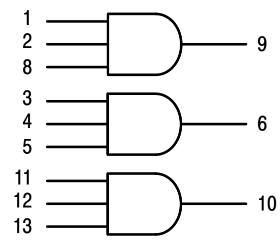
MC14025B
Triple 3−Input NOR Gate



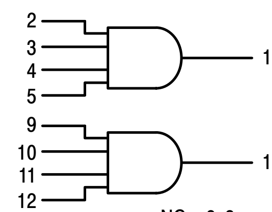
MC14023B
Triple 3−Input NAND Gate



MC14073B
Triple 3−Input AND Gate



MC14082B
Dual 4−Input AND Gate

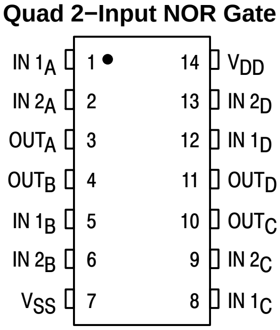


NC = 6, 8

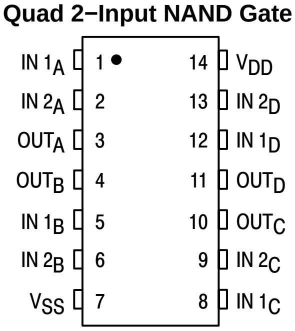
V_{DD} = PIN 14
V_{SS} = PIN 7
FOR ALL DEVICES

PIN ASSIGNMENTS

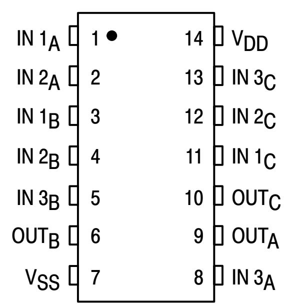
MC14001B
Quad 2−Input NOR Gate



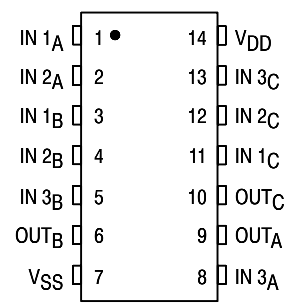
MC14011B
Quad 2−Input NAND Gate



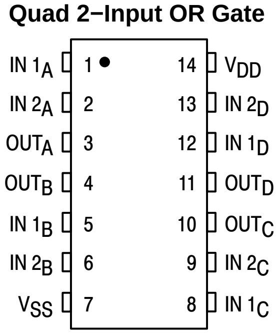
MC14023B
Triple 3−Input NAND Gate



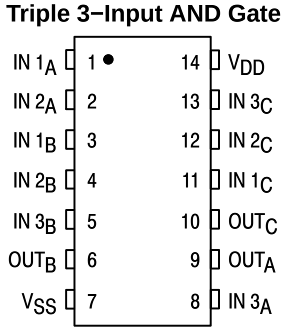
MC14025B
Triple 3−Input NOR Gate



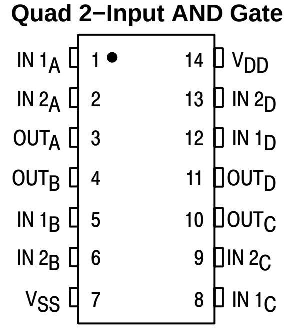
MC14071B
Quad 2−Input OR Gate



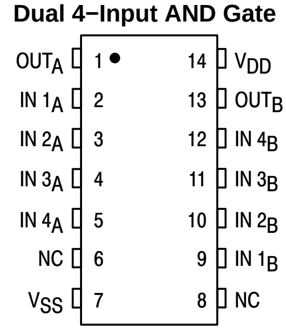
MC14073B
Triple 3−Input AND Gate



MC14081B
Quad 2−Input AND Gate



MC14082B
Dual 4−Input AND Gate



NC = NO CONNECTION

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (3)	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	μAdc
Total Supply Current (4) (5) (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0 10 15	I_T = (0.3 μA/kHz) f + I_{DD}/N I_T = (0.6 μA/kHz) f + I_{DD}/N I_T = (0.9 μA/kHz) f + I_{DD}/N							μAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

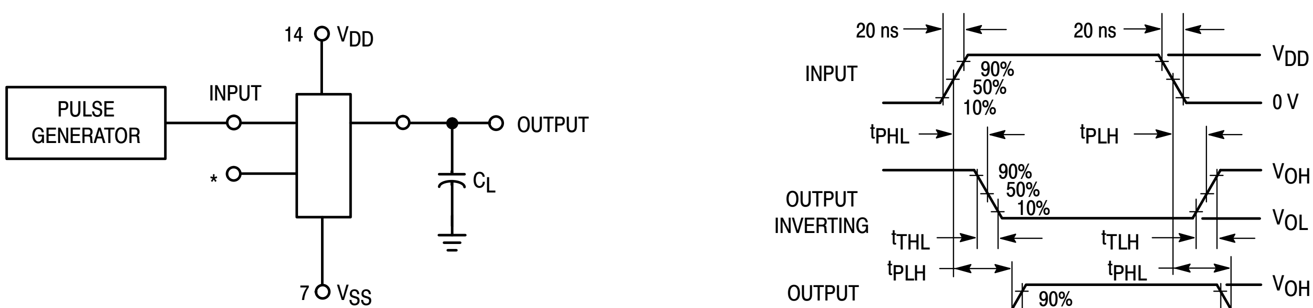
where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

B−SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS (6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7)	Max	Unit
Output Rise Time, All B−Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/PF) C_L + 20 ns		15	—	40	80	
Output Fall Time, All B−Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	—	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	—	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	—	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	—	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	—	50	100	
8−Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	—	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	—	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	—	60	110	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

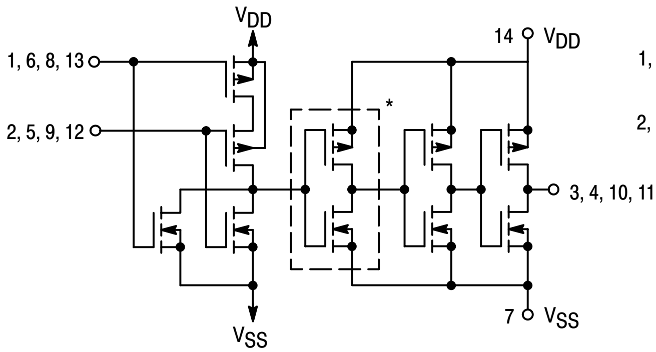


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

Figure 1. Switching Time Test Circuit and Waveforms

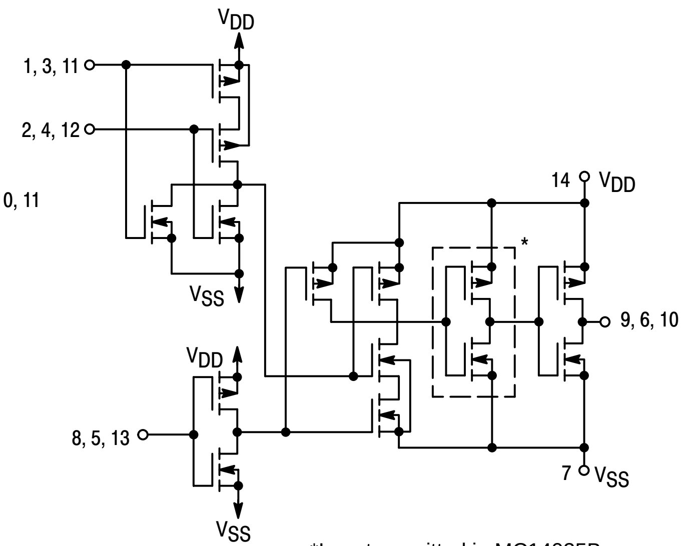
CIRCUIT SCHEMATIC
NOR, OR GATES

MC14001B, MC14071B
One of Four Gates Shown



*Inverter omitted in MC14001B

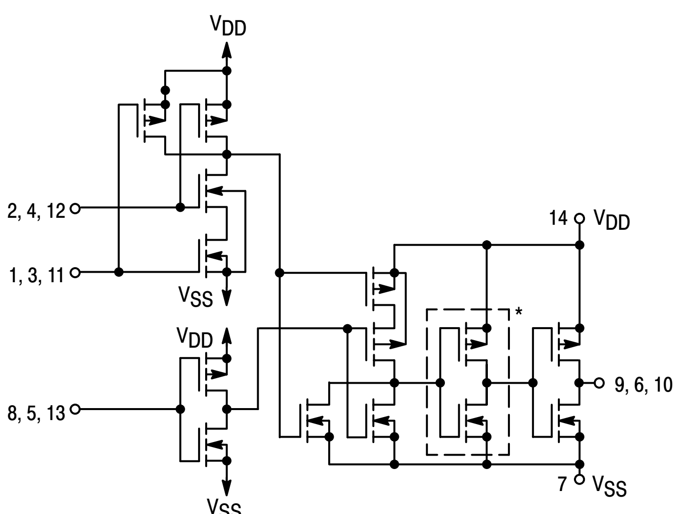
MC14025B
One of Three Gates Shown



*Inverter omitted in MC14025B

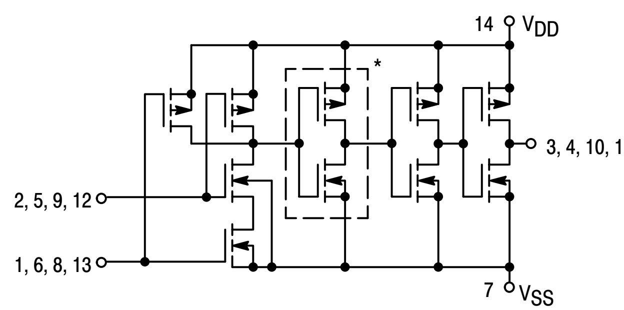
CIRCUIT SCHEMATIC
NAND, AND GATES

MC14023B, MC14073B
One of Three Gates Shown



*Inverter omitted in MC14023B

MC14011B, MC14081B
One of Four Gates Shown



*Inverter omitted in MC14011B

TYPICAL B−SERIES GATE CHARACTERISTICS

N−CHANNEL DRAIN CURRENT (SINK)

P−CHANNEL DRAIN CURRENT (SOURCE)

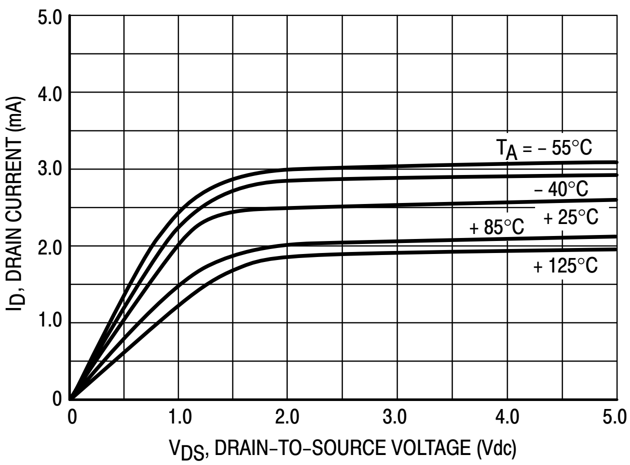


Figure 2. V_{GS} = 5.0 Vdc

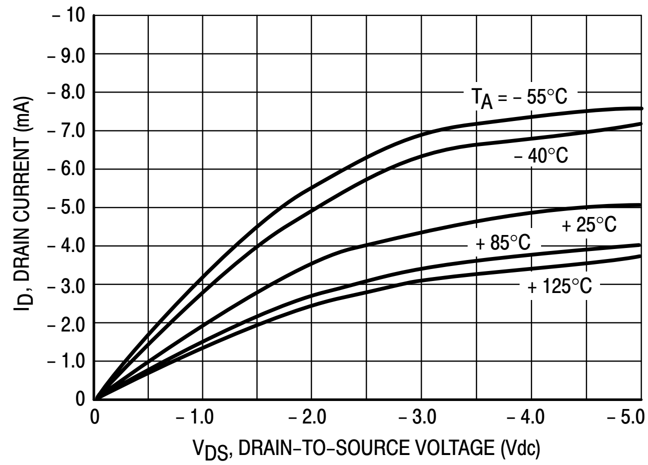


Figure 3. V_{GS} = − 5.0 Vdc

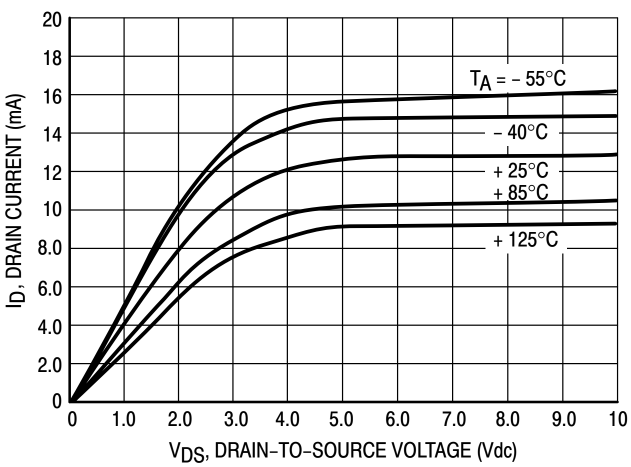


Figure 4. V_{GS} = 10 Vdc

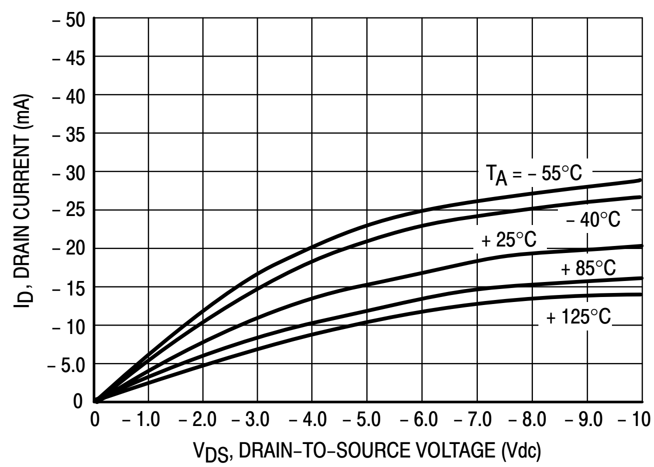


Figure 5. V_{GS} = − 10 Vdc

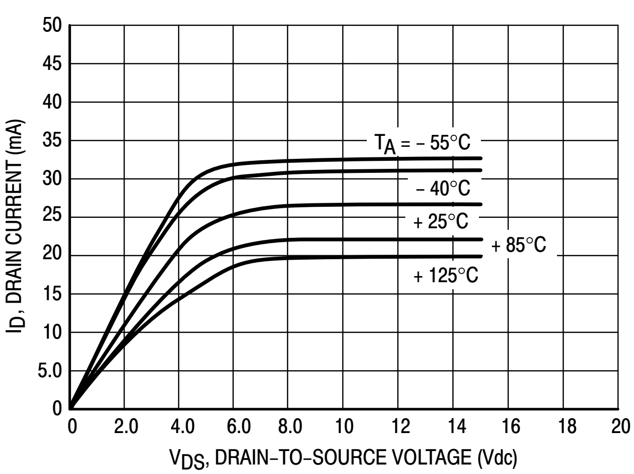


Figure 6. V_{GS} = 15 Vdc

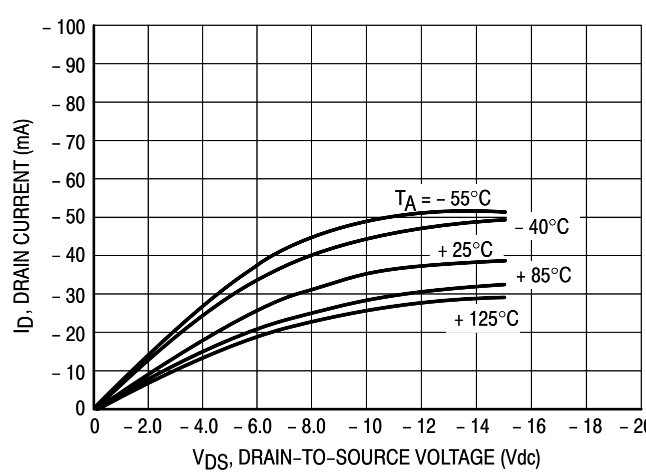


Figure 7. V_{GS} = − 15 Vdc

These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

TYPICAL B−SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

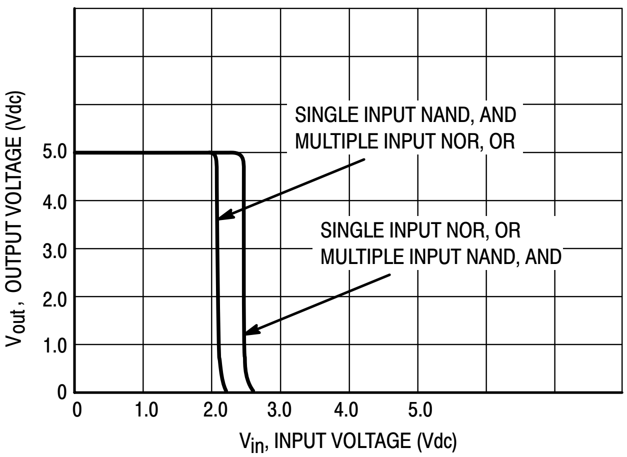


Figure 8. V_{DD} = 5.0 Vdc

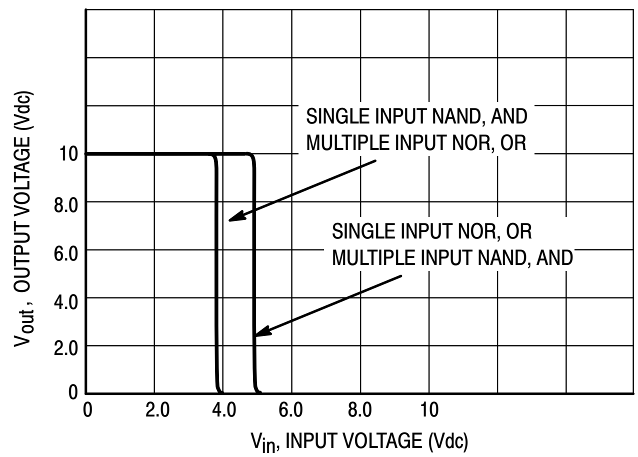


Figure 9. V_{DD} = 10 Vdc

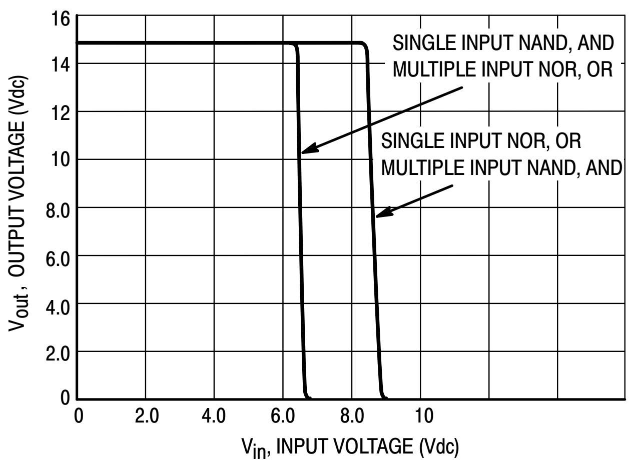


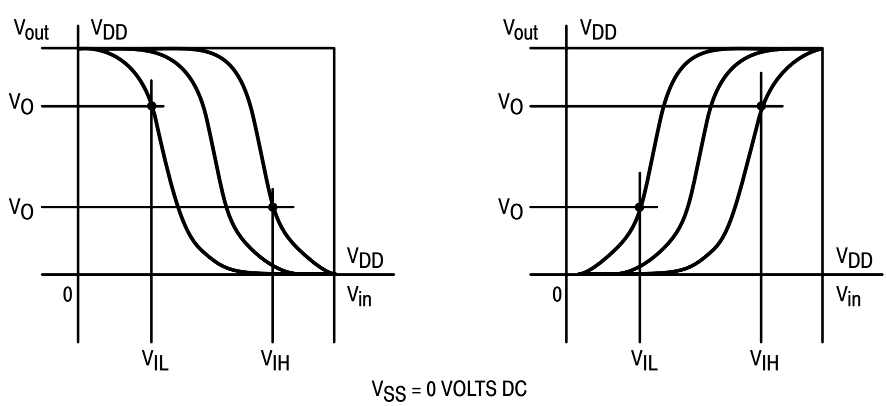
Figure 10. V_{DD} = 15 Vdc

DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

1.0 V with a 5.0 V supply
2.0 V with a 10.0 V supply
2.5 V with a 15.0 V supply



(a) Inverting Function **(b) Non−Inverting Function**

Figure 11. DC Noise Immunity

ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14001BCP	PDIP−14	2000 Units per Box
MC14001BD	SOIC−14	2750 Units per Box
MC14001BDR2	SOIC−14	2500 Units / Tape & Reel
MC14001BDT	TSSOP−14	96 Units per Rail
MC14001BDTR2	TSSOP−14	2500 Units / Tape & Reel
MC14011BCP	PDIP−14	2000 Units per Box
MC14011BD	SOIC−14	2750 Units per Box
MC14011BDR2	SOIC−14	2500 Units / Tape & Reel
MC14011BDT	TSSOP−14	96 Units per Rail
MC14011BDTEL	TSSOP−14	2000 Units / Tape & Reel
MC14011BDTR2	TSSOP−14	2500 Units / Tape & Reel
MC14023BCP	PDIP−14	2000 Units per Box
MC14023BD	SOIC−14	2750 Units per Box
MC14023BDR2	SOIC−14	2500 Units / Tape & Reel
MC14025BCP	PDIP−14	2000 Units per Box
MC14025BD	SOIC−14	2750 Units per Box
MC14025BDR2	SOIC−14	2500 Units / Tape & Reel

ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14071BCP	PDIP−14	2000 Units per Box
MC14071BD	SOIC−14	55 Units per Rail
MC14071BDR2	SOIC−14	2500 Units / Tape & Reel
MC14071BDT	TSSOP−14	96 Units per Rail
MC14071BDTR2	TSSOP−14	2500 Units / Tape & Reel
MC14073BCP	PDIP−14	2000 Units per Box
MC14073BD	SOIC−14	55 Units per Rail
MC14073BDR2	SOIC−14	2500 Units / Tape & Reel
MC14081BCP	PDIP−14	2000 Units per Box
MC14081BD	SOIC−14	55 Units per Rail
MC14081BDR2	SOIC−14	2500 Units / Tape & Reel
MC14081BDT	TSSOP−14	96 Units per Rail
MC14081BDTR2	TSSOP−14	2500 Units / Tape & Reel
MC14082BCP	PDIP−14	2000 Units per Box
MC14082BD	SOIC−14	55 Units per Rail
MC14082BDR2	SOIC−14	2500 Units / Tape & Reel

For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14001UB, MC14011UB

UB-Suffix Series CMOS Gates

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non−buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin−for−Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ON Semiconductor

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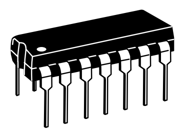
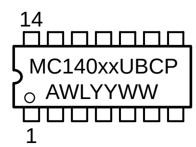
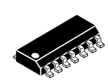
MC14001UB
Quad 2−Input NOR Gate
MC14011UB
Quad 2−Input NAND Gate

MARKING DIAGRAMS

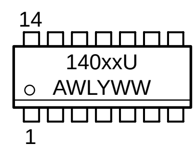


PDIP−14
P SUFFIX
CASE 646





SOIC−14
D SUFFIX
CASE 751A



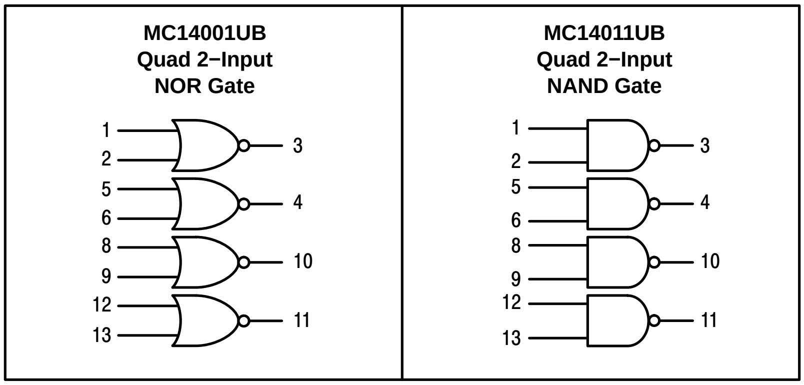
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14001UBCP	PDIP−14	2000/Box
MC14001UBD	SOIC−14	55/Rail
MC14001UBDR2	SOIC−14	2500/Tape & Reel
MC14011UBCP	PDIP−14	2000/Box
MC14011UBD	SOIC−14	55/Rail
MC14011UBDR2	SOIC−14	2500/Tape & Reel

August, 2000 − Rev. 4
Publication Order Number:
MC14001UB/D

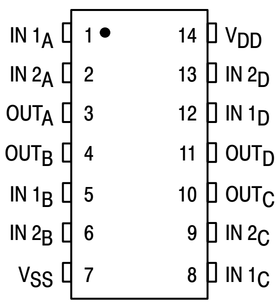
LOGIC DIAGRAMS



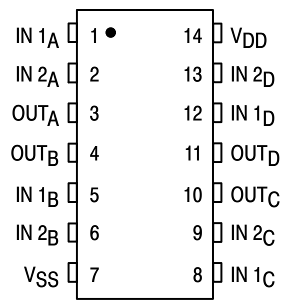
V_{DD} = PIN 14
V_{SS} = PIN 7
FOR ALL DEVICES

PIN ASSIGNMENTS

MC14001UB
Quad 2−Input NOR Gate



MC14011UB
Quad 2−Input NAND Gate



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	“0” Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	“1” Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	“0” Level	V_{IL}	5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	Vdc
(V_O = 0.5 Vdc) (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	“1” Level	I_{IH}	5.0 10 15	4.0 8.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	— — — —	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	— — — —	– 0.7 – 0.14 – 0.35 – 1.1	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Gate C_L = 50 pF)		I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD}/N I_T = (0.6 µA/kHz) f + I_{DD}/N I_T = (0.8 µA/kHz) f + I_{DD}/N							µAdc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

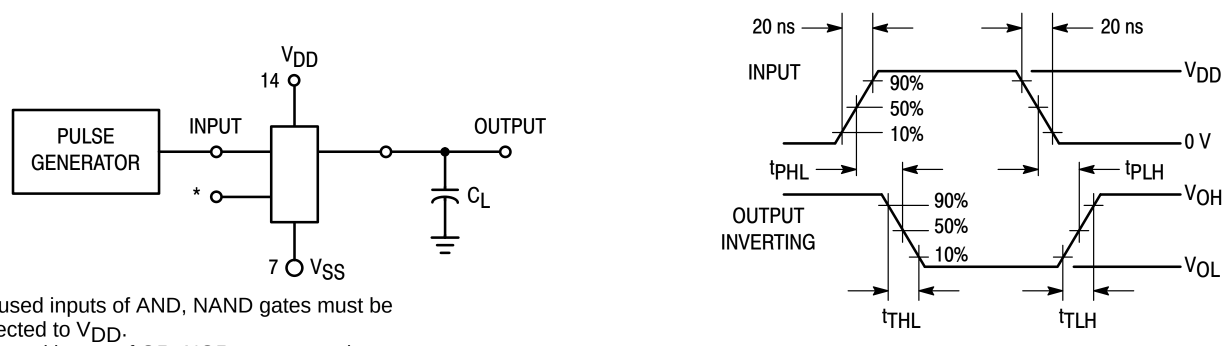
$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\ Vfk$$

where: I_T is in µH (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	—	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	—	40	80	

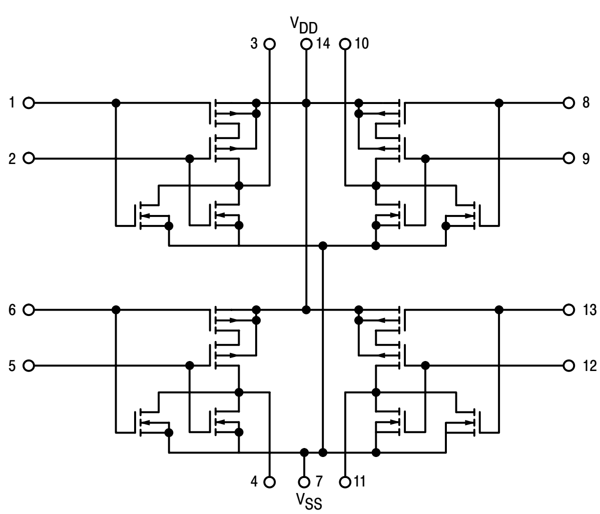
6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



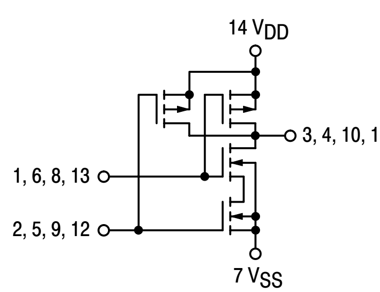
*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

Figure 1. Switching Time Test Circuit and Waveforms

MC14001UB CIRCUIT SCHEMATIC



MC14011UB CIRCUIT SCHEMATIC (1/4 of Device Shown)



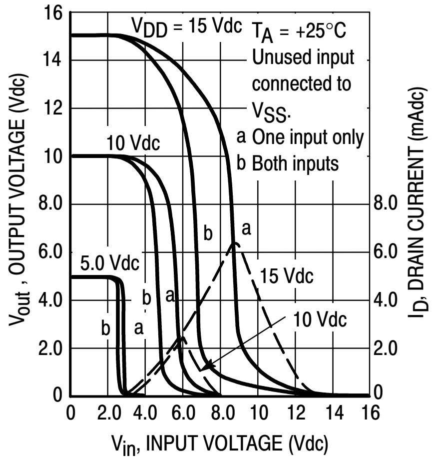


Figure 2. Typical Voltage and Current Transfer Characteristics

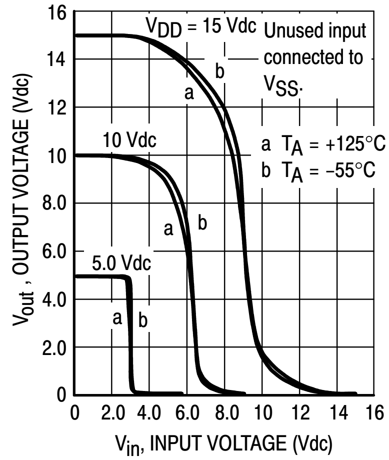


Figure 3. Typical Voltage Transfer Characteristics versus Temperature

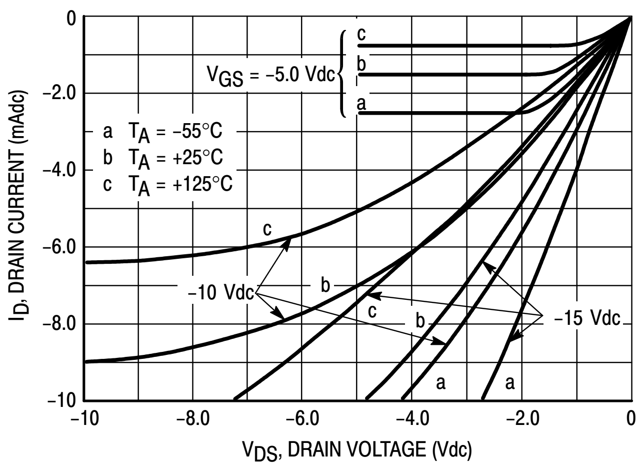


Figure 4. Typical Output Source Characteristics

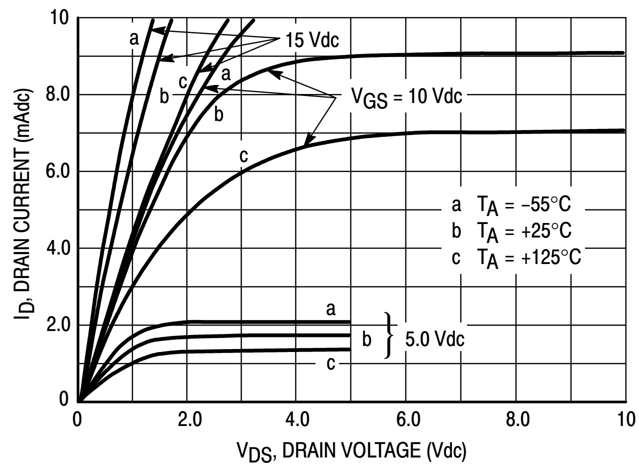


Figure 5. Typical Output Sink Characteristics

MC14007UB

Dual Complementary Pair Plus Inverter

The MC14007UB multipurpose device consists of three N−Channel and three P−Channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse−shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Antistatic precautions must be taken.
- Pb−Free Package is Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 8)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8 second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

8. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C from 65°C 5o 125°C.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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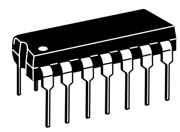
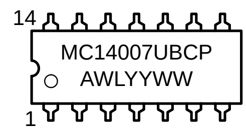
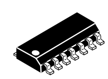
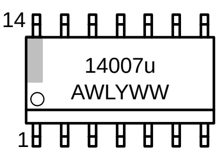
MARKING DIAGRAMS



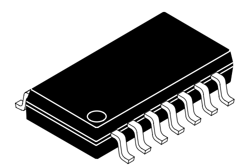


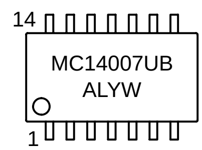
PDIP−14
P SUFFIX
CASE 646





SOIC−14
D SUFFIX
CASE 751A

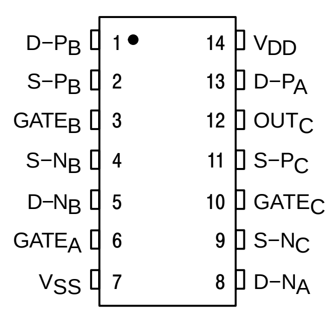




SOEIAJ−14
F SUFFIX
CASE 965

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

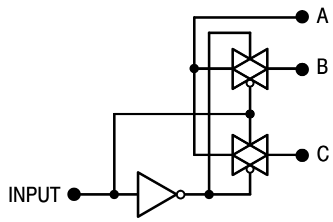
PIN ASSIGNMENT

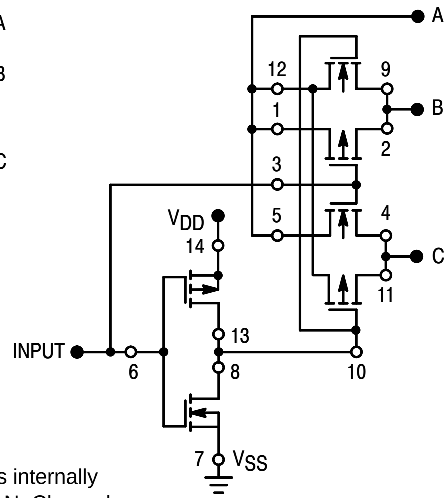


D = DRAIN
S = SOURCE

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 30 of this data sheet.

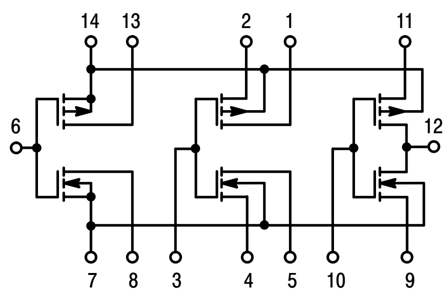




INPUT	OUTPUT CONDITION
1	A = C, B = OPEN
0	A = B, C = OPEN

Substrates of P−Channel devices internally connected to V_{DD}; substrates of N−Channel devices internally connected to V_{SS}.

Figure 1. Typical Application: 2−Input Analog Multiplexer



V_{DD} = PIN 14
V_{SS} = PIN 7

Figure 2. Schematic

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

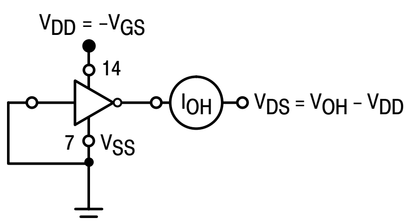
Symbol	Characteristic	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 9)	25°C Max	125°C Min	125°C Max	Unit
V_{OL}	Output Voltage "0" Level V_{in} = V_{DD} or 0	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{OH}	V_{in} = 0 or V_{DD} "1" Level	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
V_{IL}	Input Voltage "0" Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	 5.0 10 15	 – – –	 1.0 2.0 2.5	 – – –	 2.25 4.50 6.75	 1.0 2.0 2.5	 – – –	 1.0 2.0 2.5	Vdc
V_{IH}	(V_O = 0.5 Vdc) "1" Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	5.0 10 15	4.0 8.0 12.5	– – –	4.0 8.0 12.5	2.75 5.50 8.25	– – –	4.0 8.0 12.5	– – –	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	 5.0 5.0 10 15	 –3.0 –0.64 –1.6 –4.2	 – – – –	 –2.4 –0.51 –1.3 –3.4	 –5.0 –1.0 –2.5 –10	 – – – –	 –1.7 –0.36 –0.9 –2.4	 – – – –	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	1.0 2.5 10	– – –	0.36 0.9 2.4	– – –	mAdc
I_{in}	Input Current	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
C_{in}	Input Capacitance (V_{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I_{DD}	Quiescent Current (Per Package)	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	μAdc
I_T	Total Supply Current (Notes 10 and 11) (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	5.0 10 15	I_T = (0.7 μA/kHz) f + I_{DD}/6 I_T = (1.4 μA/kHz) f + I_{DD}/6 I_T = (2.2 μA/kHz) f + I_{DD}/6							μAdc

9. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
10. The formulas given are for the typical characteristics only at 25°C.
11. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$
where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

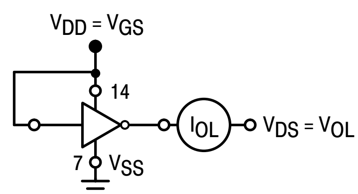
SWITCHING CHARACTERISTICS (Note 12) (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD} Vdc	Min	Typ (Note 13)	Max	Unit
t_{TLH}	Output Rise Time					ns
	t_{TLH} = (1.2 ns/pF) C_L + 30 ns	5.0	–	90	180	
	t_{TLH} = (0.5 ns/pF) C_L + 20 ns	10	–	45	90	
	t_{TLH} = (0.4 ns/pF) C_L + 15 ns	15	–	35	70	
t_{THL}	Output Fall Time					ns
	t_{THL} = (1.2 ns/pF) C_L + 15 ns	5.0	–	75	150	
	t_{THL} = (0.5 ns/pF) C_L + 15 ns	10	–	40	80	
	t_{THL} = (0.4 ns/pF) C_L + 10 ns	15	–	30	60	
t_{PLH}	Turn−Off Delay Time					ns
	t_{PLH} = (1.5 ns/pF) C_L + 35 ns	5.0	–	60	125	
	t_{PLH} = (0.2 ns/pF) C_L + 20 ns	10	–	30	75	
	t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns	15	–	25	55	
t_{PHL}	Turn−On Delay Time					ns
	t_{PHL} = (1.0 ns/pF) C_L + 10 ns	5.0	–	60	125	
	t_{PHL} = (0.3 ns/pF) C_L + 15 ns	10	–	30	75	
	t_{PHL} = (0.2 ns/pF) C_L + 15 ns	15	–	25	55	

12. The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.
13. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



All unused inputs connected to ground.



All unused inputs connected to ground.

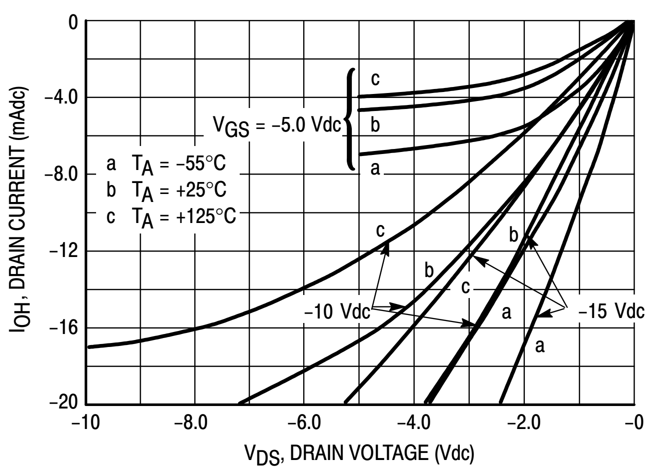


Figure 3. Typical Output Source Characteristics

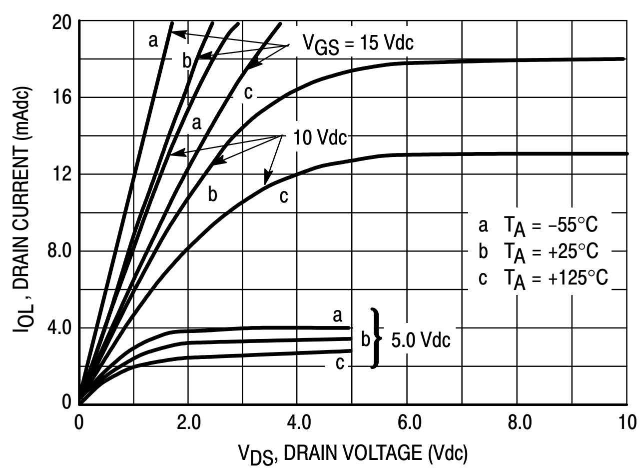


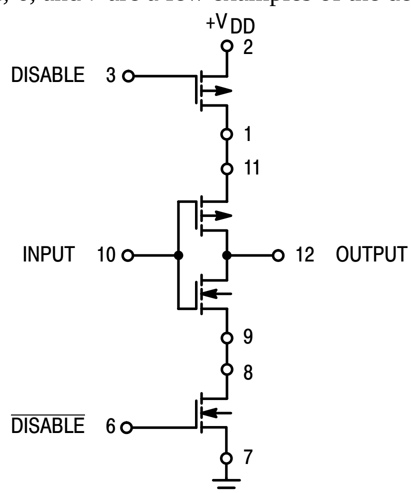
Figure 4. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.
Caution: The maximum current rating is 10 mA per pin.

Figure 5. Switching Time and Power Dissipation Test Circuit and Waveforms

APPLICATIONS

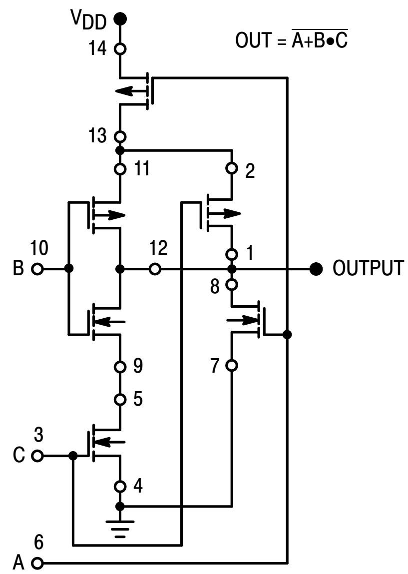
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 6, and 7 are a few examples of the device flexibility.



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don’t Care

Figure 6. 3−State Buffer



Substrates of P−Channel devices internally connected to V_{DD};
Substrates of N−Channel devices internally connected to V_{SS}.

Figure 7. AOI Functions Using Tree Logic

ORDERING INFORMATION

Device	Package	Shipping†
MC14007UBCP	PDIP−14	500 Units / Rail
MC14007UBCPG	PDIP−14 (Pb−Free)	500 Units / Rail
MC14007UBD	SOIC−14	55 Units / Rail
MC14007UBDR2	SOIC−14	2500 / Tape & Reel
MC14007UBFEL	SOEIAJ−14	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14008B

4-Bit Full Adder

The MC14008B 4−bit full adder is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look−ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high−speed operation when used with other adders in a system.

- Look−Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4008B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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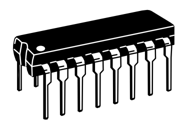
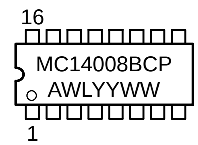
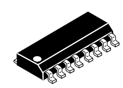
MARKING DIAGRAMS

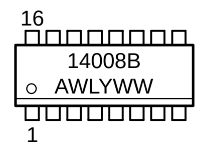


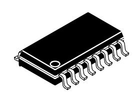
PDIP−16
P SUFFIX
CASE 648



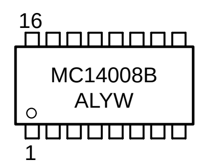


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

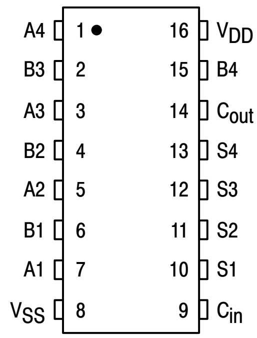
Device	Package	Shipping
MC14008BCP	PDIP−16	2000/Box
MC14008BDR2	SOIC−16	2500/Tape & Reel
MC14008BF	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

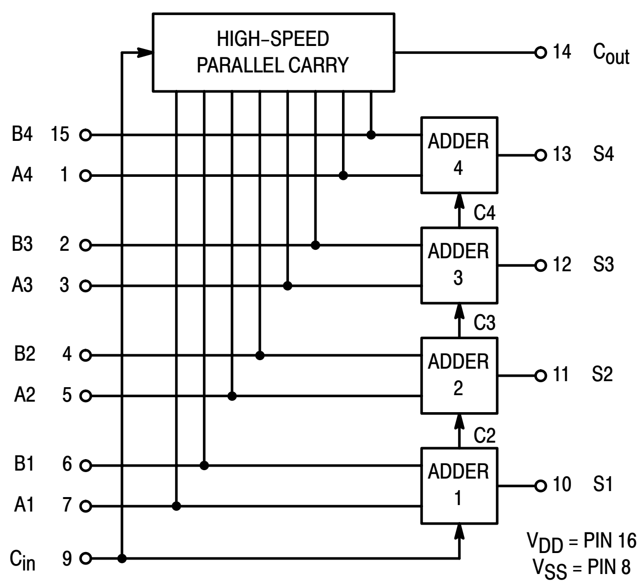
TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

PIN ASSIGNMENT



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ [4.]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.7 µA/kHz) f + I_{DD} I_T = (3.4 µA/kHz) f + I_{DD} I_T = (5.0 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum in to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	—	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	—	160	320	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	—	115	230	
Sum In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	—	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	—	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	—	110	220	
Carry In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 290 ns		5.0	—	375	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	—	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	—	115	230	
Carry In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	—	170	340	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	—	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	—	55	110	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

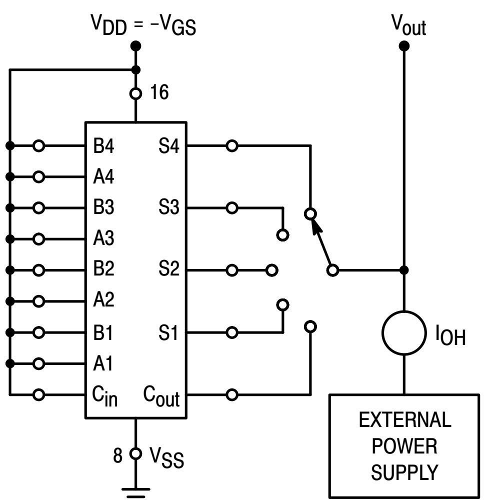


Figure 1. Typical Source Current Characteristics Test Circuit

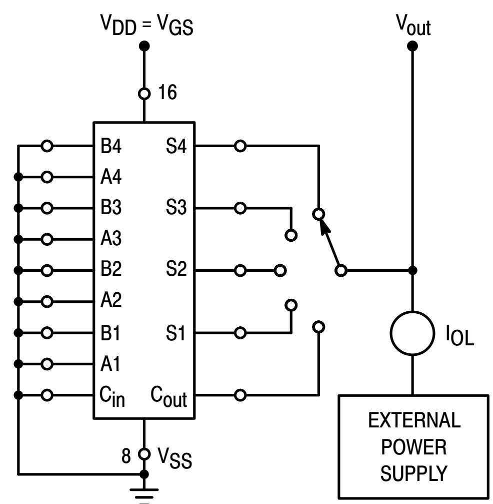


Figure 2. Typical Sink Current Characteristics Test Circuit

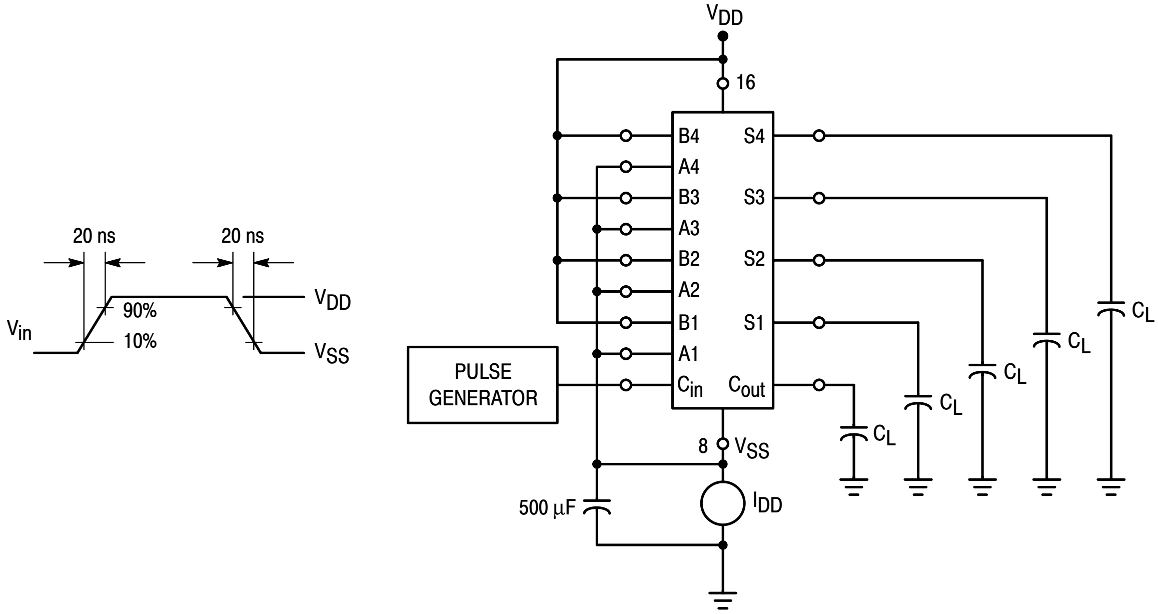


Figure 3. Dynamic Power Dissipation Test Circuit and Waveform

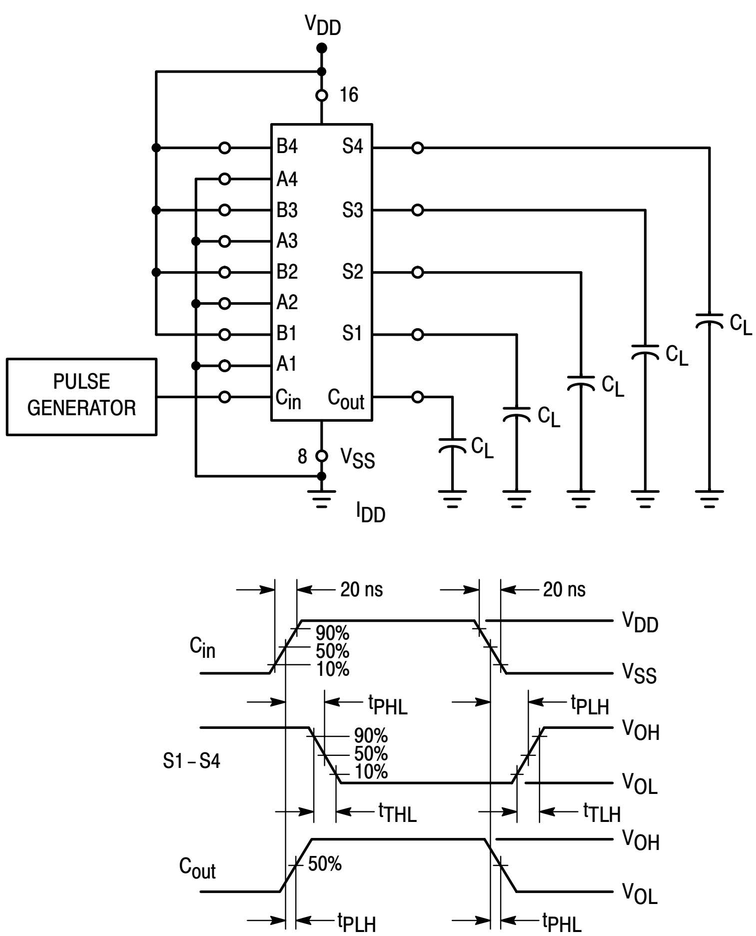


Figure 4. Switching Time Test Circuit and Waveforms

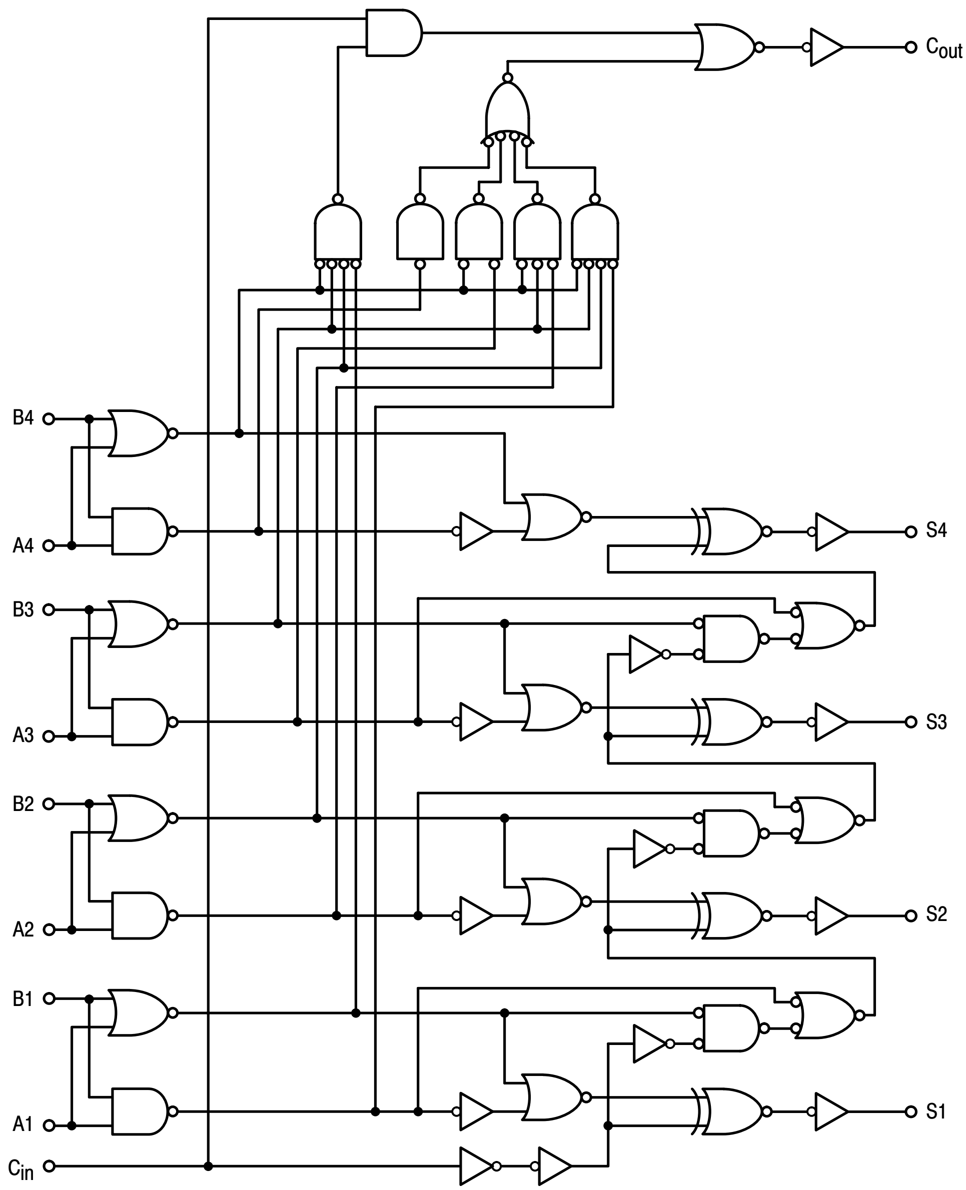
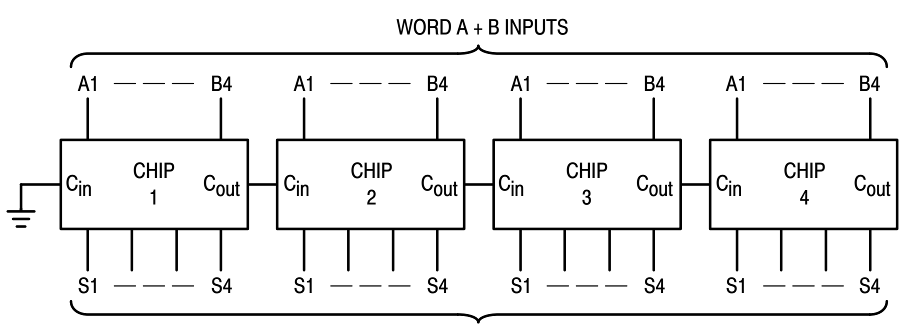


Figure 5. Logic Diagram

TYPICAL APPLICATION



Calculation of 16−bit adder speed:

t_P total = t_P (Sum to Carry) + t_P (Carry to Sum) + 2 t_P (Carry to Carry)

The guaranteed 16−bit adder speed at 10 V, 25°C, C_L = 50 pF is:

t_p total = 290 + 310 + 300 = 900 ns

Figure 6. Using the MC14008B in a 16−Bit Adder Configuration

MC14013B

Dual Type D Flip-Flop

The MC14013B dual type D flip−flop is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each flip−flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip−flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge−Clocked Flip−Flop Design
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive−going edge of the clock pulse
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4013B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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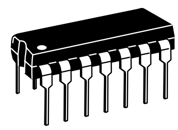
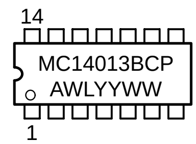
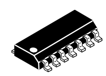
MARKING DIAGRAMS

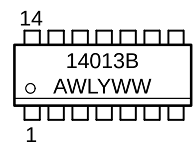


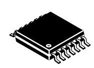
PDIP−14
P SUFFIX
CASE 646



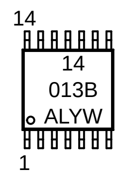


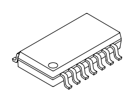
SOIC−14
D SUFFIX
CASE 751A



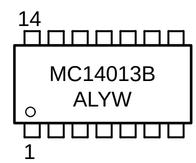


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14013BCP	PDIP−14	2000/Box
MC14013BD	SOIC−14	55/Rail
MC14013BDR2	SOIC−14	2500/Tape & Reel
MC14013BDT	TSSOP−14	96/Rail
MC14013BDTR2	TSSOP−14	2500/Tape & Reel
MC14013BF	SOEIAJ−14	See Note 1.
MC14013BFEL	SOEIAJ−14	See Note 1.

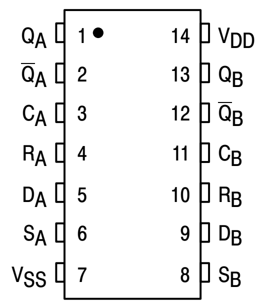
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

TRUTH TABLE

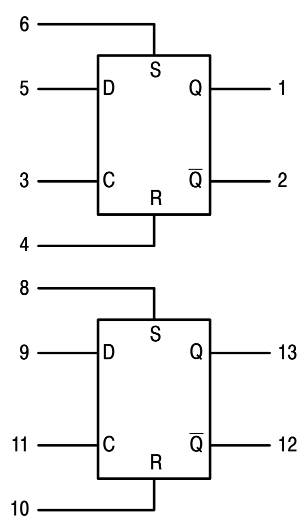
Inputs				Outputs		
Clock†	Data	Reset	Set	Q	$\overline{Q}$	
↑	0	0	0	0	1	
↑	1	0	0	1	0	
↓	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 14
V_{SS} = PIN 7

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 − 1.3 − 3.4	 – 4.2 – 0.88 – 2.25 − 8.8	 — — — —	 – 1.7 − 0.36 – 0.9 − 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.75 µA/kHz) f + I_{DD} I_T = (1.5 µA/kHz) f + I_{DD} I_T = (2.3 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\,Vfk$$

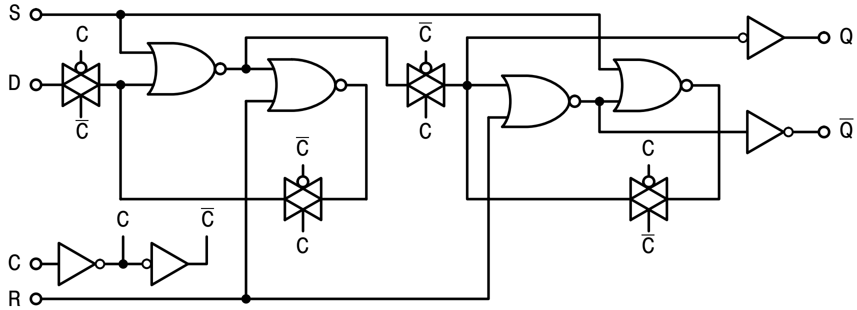
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

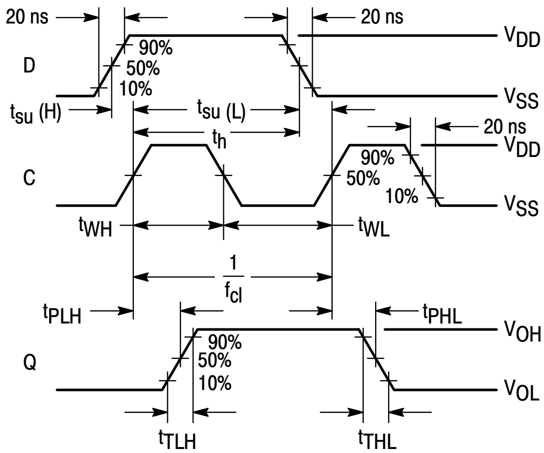
SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}					ns
Clock to Q, $\overline{Q}$	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	—	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	—	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	—	50	100	
Set to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	—	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	—	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	—	50	100	
Reset to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	—	225	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	—	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	—	75	150	
Setup Times (9.)	t_{su}	5.0	40	20	—	ns
		10	20	10	—	
		15	15	7.5	—	
Hold Times (9.)	t_h	5.0	40	20	—	ns
		10	20	10	—	
		15	15	7.5	—	
Clock Pulse Width	t_{WL}, t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	
Clock Pulse Frequency	f_{cl}	5.0	—	4.0	2.0	MHz
		10	—	10	5.0	
		15	—	14	7.0	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5.0	
		15	—	—	4.0	
Set and Reset Pulse Width	t_{WL}, t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	
Removal Times	t_{rem}					ns
Set		5	80	0	—	
		10	45	5	—	
		15	35	5	—	
Reset		5	50	– 35	—	
		10	30	– 10	—	
		15	25	– 5	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
9. Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.

LOGIC DIAGRAM (1/2 of Device Shown)





Inputs R and S low.

Figure 1. Dynamic Signal Waveforms (Data, Clock, and Output)

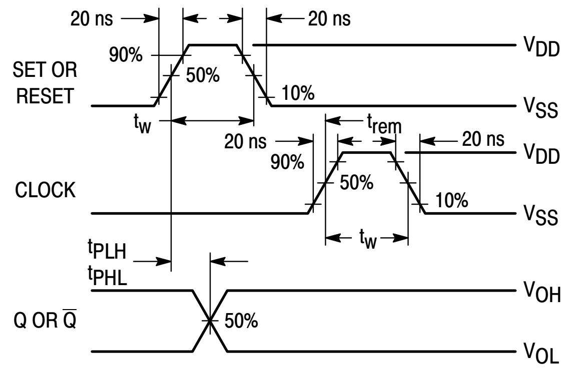
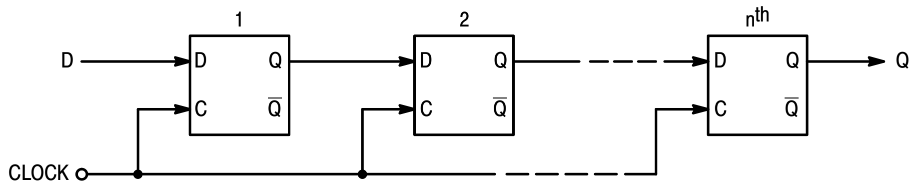


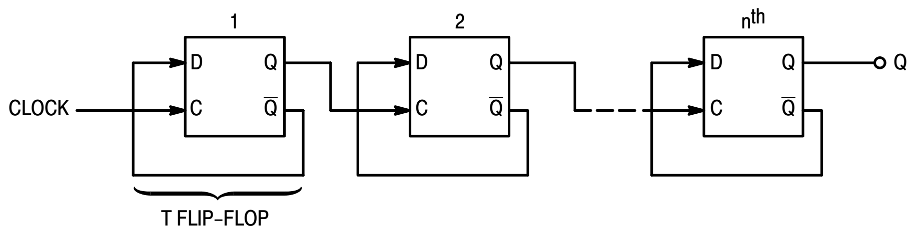
Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)

TYPICAL APPLICATIONS

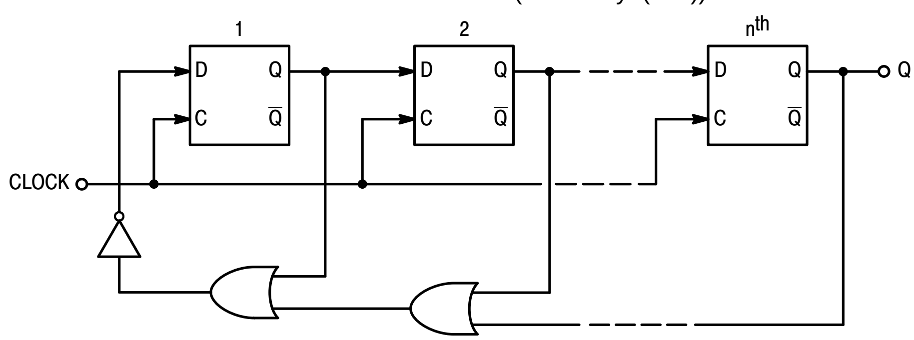
n−STAGE SHIFT REGISTER



BINARY RIPPLE UP−COUNTER (Divide−by−2^n)



MODIFIED RING COUNTER (Divide−by−(n+1))



MC14014B, MC14021B

8-Bit Static Shift Register

The MC14014B and MC14021B 8−bit static shift registers are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel−to−serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- “Q” Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin−for−Pin Replacement for CD4014B
- MC14021B Pin−for−Pin Replacement for CD4021B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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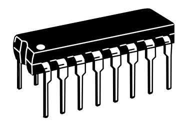
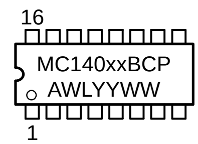
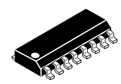
MARKING DIAGRAMS

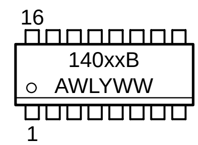


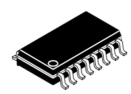
PDIP−16
P SUFFIX
CASE 648



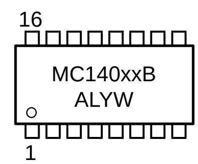


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



xx	=	Specific Device Code
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14014BCP	PDIP−16	2000/Box
MC14014BD	SOIC−16	48/Rail
MC14014BDR2	SOIC−16	2500/Tape & Reel
MC14014BF	SOEIAJ−16	See Note 1.
MC14014BFEL	SOEIAJ−16	See Note 1.
MC14021BCP	PDIP−16	2000/Box
MC14021BD	SOIC−16	48/Rail
MC14021BDR2	SOIC−16	2500/Tape & Reel
MC14021BF	SOEIAJ−16	See Note 1.
MC14021BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

TRUTH TABLE

SERIAL OPERATION:

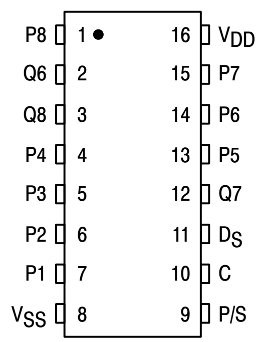
t	Clock	D_S	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n	↑	0	0	0	?	?
n+1	↑	1	0	1	0	?
n+2	↑	0	0	0	1	0
n+3	↑	1	0	1	0	1
	↓	X	0	Q6	Q7	Q8

PARALLEL OPERATION:

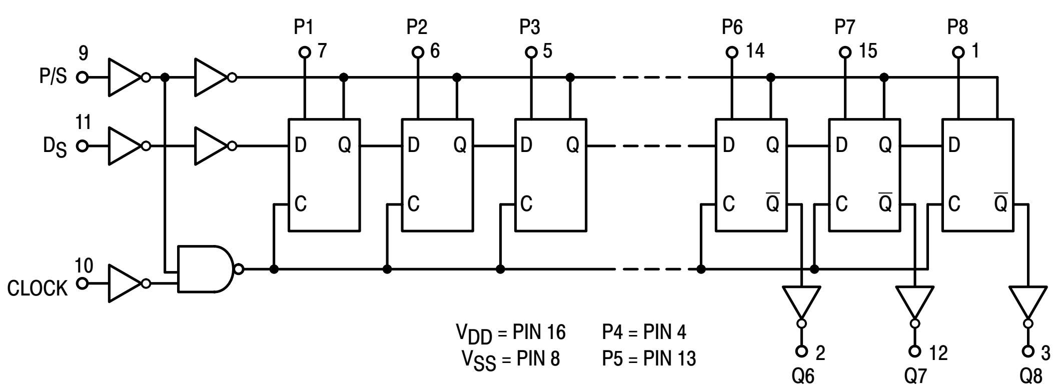
Clock					
MC14014B	MC14021B	D_S	P/S	P_n	$*Q_n$
↑	X	X	1	0	0
↑	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don’t Care

PIN ASSIGNMENT



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 − 1.3 − 3.4	– 4.2 – 0.88 – 2.25 − 8.8	— — — —	– 1.7 − 0.36 – 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 15	— — —	0.005 0.010 0.015	5.0 10 15	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.75 µA/kHz) f + I_{DD} I_T = (1.50 µA/kHz) f + I_{DD} I_T = (2.25 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

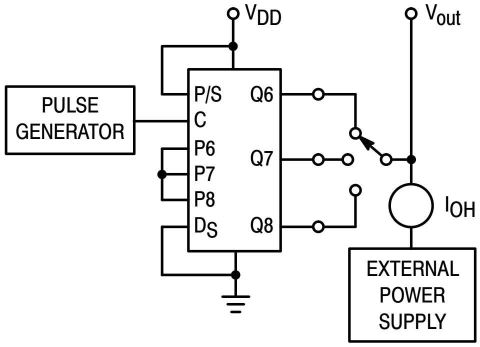
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.0015.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time (Clock to Q, P/S to Q)	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	—	400	800	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	—	170	340	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 90 ns		15	—	115	230	
Clock Pulse Width	t_{WH}	5.0	400	150	—	ns
		10	175	75	—	
		15	135	40	—	
Clock Frequency	f_{cl}	5.0	—	3.0	1.5	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Parallel/Serial Control Pulse Width	t_{WH}	5.0	400	150	—	ns
		10	175	75	—	
		15	135	40	—	
Setup Time P/S to Clock	t_{su}	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	
Hold Time Clock to P/S	t_h	5.0	20	– 2.5	—	ns
		10	20	– 10	—	
		15	25	0	—	
Setup Time Data (Parallel or Serial) to Clock or P/S	t_{su}	5.0	350	150	—	ns
		10	80	50	—	
		15	60	30	—	
Hold Time Clock to D_S	t_h	5.0	45	0	—	ns
		10	35	0	—	
		15	35	5	—	
Hold Time Clock to P_n	t_h	5.0	50	25	—	ns
		10	45	20	—	
		15	45	20	—	
Input Clock Rise Time	$t_{r(cl)}$	5.0	—	—	15	µs
		10	—	—	5	
		15	—	—	4	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



Preset output under test to a logic “1” level.

Figure 1. Output Source Current Test Circuit

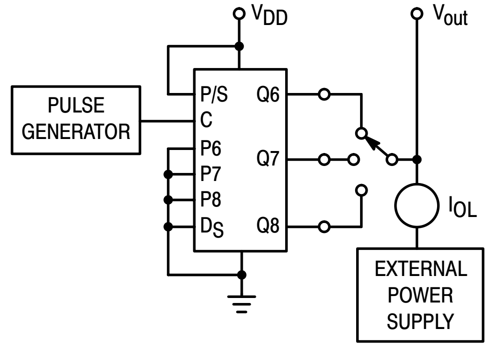


Figure 2. Output Sink Current Test Circuit

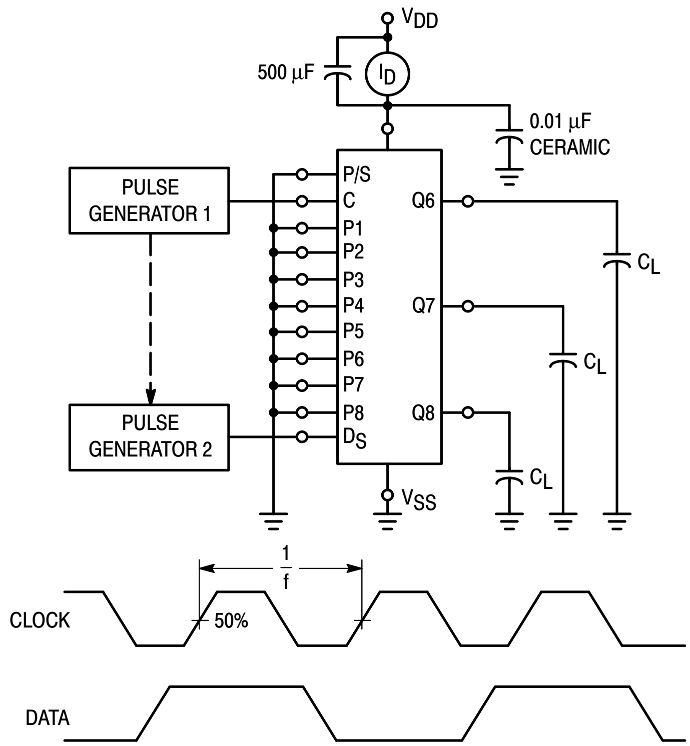


Figure 3. Power Dissipation Test Circuit and Waveform

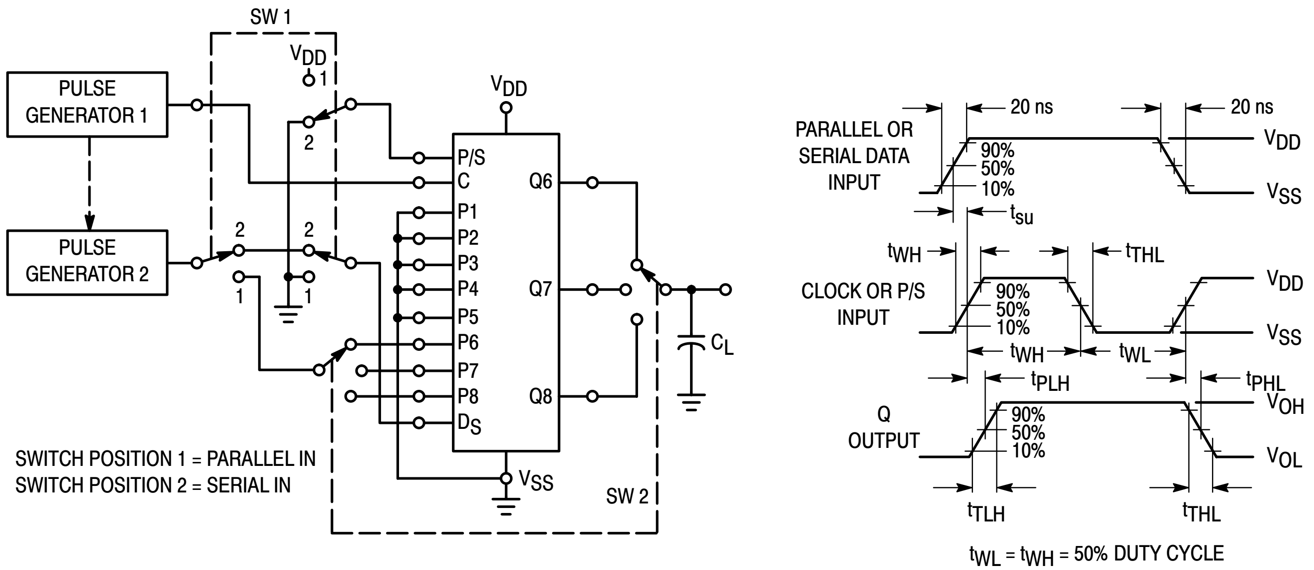


Figure 4. Switching Time Test Circuit and Waveforms

MC14015B

Dual 4-Bit Static Shift Register

ON Semiconductor

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The MC14015B dual 4−bit static shift register is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4−state serial−input/parallel−output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master−slave flip−flops. Data is shifted from one stage to the next during the positive−going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial−to−parallel conversion where low power dissipation and/or noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge−Clocked Flip−Flop Design — Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

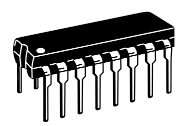
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

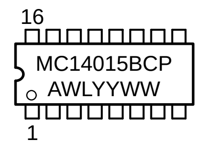
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

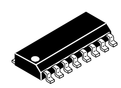
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MARKING DIAGRAMS

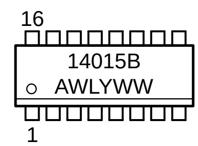


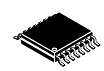
PDIP−16
P SUFFIX
CASE 648



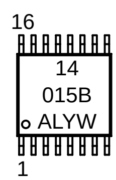


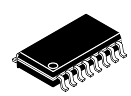
SOIC−16
D SUFFIX
CASE 751B



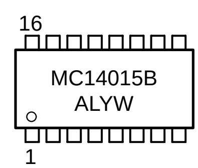


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14015BCP	PDIP−16	2000/Box
MC14015BD	SOIC−16	48/Rail
MC14015BDR2	SOIC−16	2500/Tape & Reel
MC14015BDT	TSSOP−16	2000/Tape & Reel
MC14015BF	SOEIAJ−16	See Note 1.
MC14015BFEL	SOEIAJ−16	See Note 1.

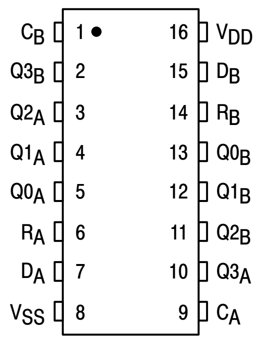
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

TRUTH TABLE

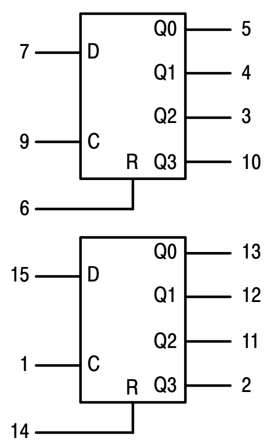
C	D	R	Q0	Q_n
_/¯	0	0	0	Q_{n-1}
_/¯	1	0	1	Q_{n-1}
¯_	X	0	No Change	No Change
X	X	1	0	0

X = Don't Care
Q_n = Q0, Q1, Q2, or Q3, as applicable.
Q_{n-1} = Output of prior stage.

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or .05 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 − 1.3 − 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 − 0.36 – 0.9 − 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.2 µA/kHz)f + I_{DD} I_T = (2.4 µA/kHz)f + I_{DD} I_T = (3.6 µA/kHz)f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\,Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock, Data to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 225 ns		5.0	—	310	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	—	90	170	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 375 ns		5.0	—	460	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	—	180	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	—	120	170	
Clock Pulse Width	t_{WH}	5.0	400	185	—	ns
		10	175	85	—	
		15	135	55	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.0	1.5	MHz
		10	—	6.0	3.0	
		15	—	7.5	3.75	
Clock Pulse Rise and Fall Times	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5	
		15	—	—	4	
Reset Pulse Width	t_{WH}	5.0	400	200	—	ns
		10	160	80	—	
		15	120	60	—	
Setup Time	t_{su}	5.0	350	100	—	ns
		10	100	50	—	
		15	75	40	—	

7. The formulas given are for typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

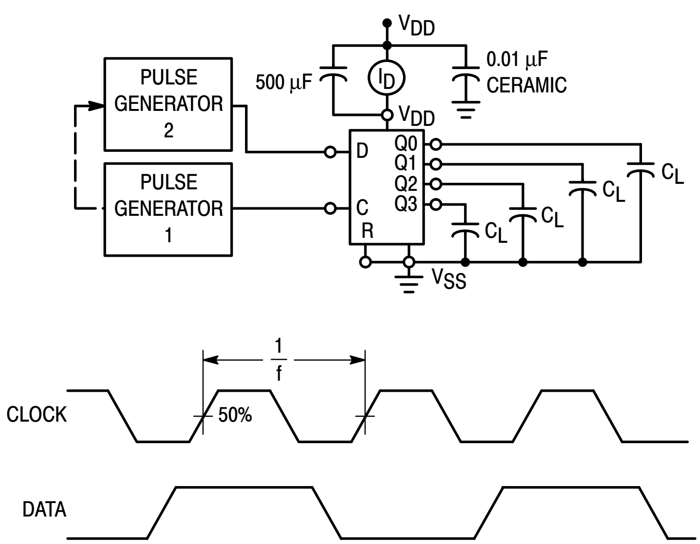


Figure 1. Power Dissipation Test Circuit and Waveform

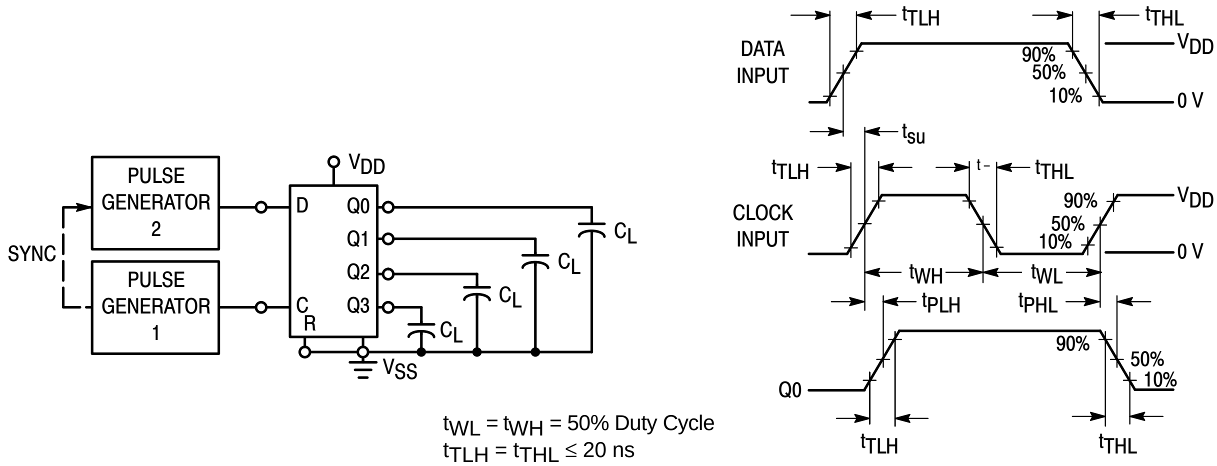


Figure 2. Switching Test Circuit and Waveforms

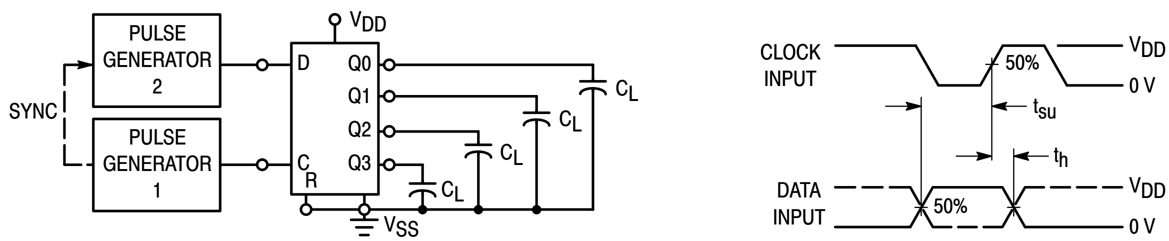
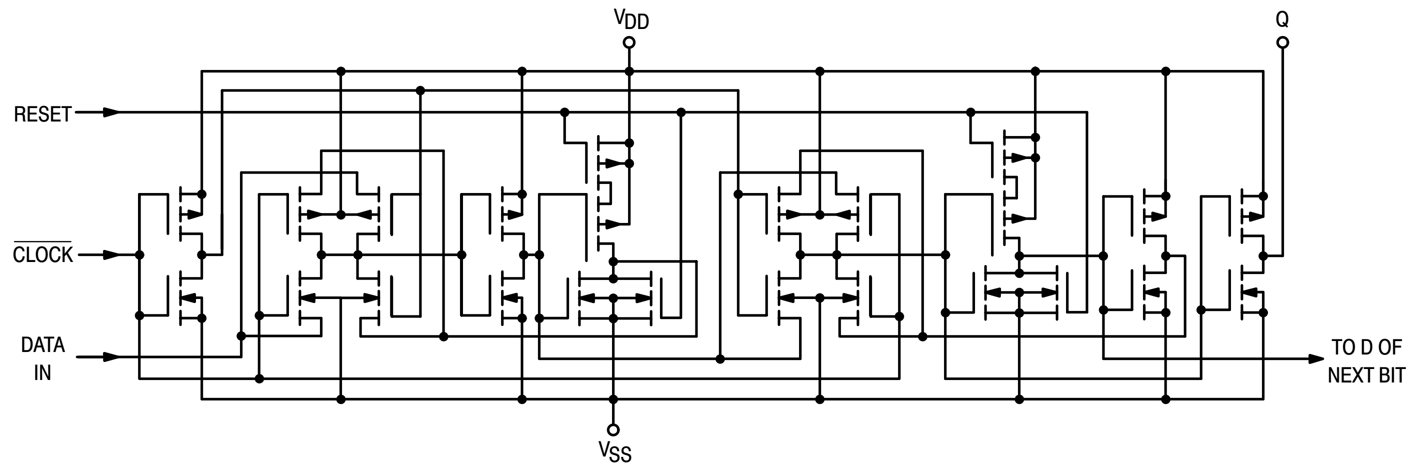


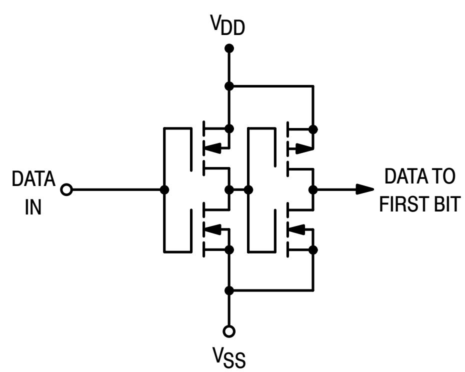
Figure 3. Setup and Hold Time Test Circuit and Waveforms

CIRCUIT SCHEMATICS

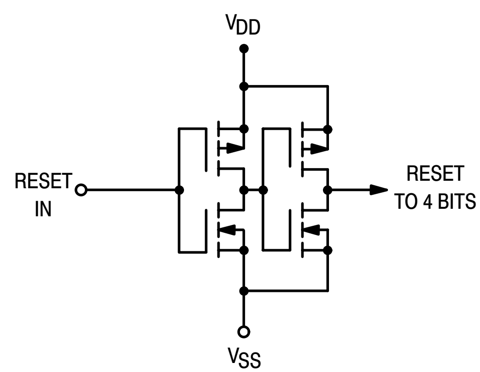
SINGLE BIT



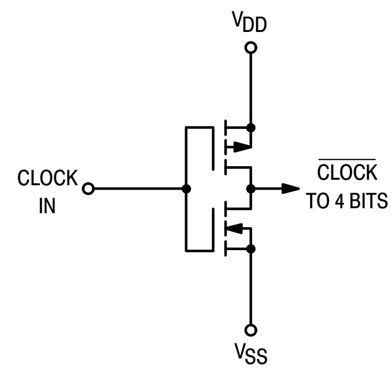
DATA INPUT BUFFER



RESET INPUT BUFFER

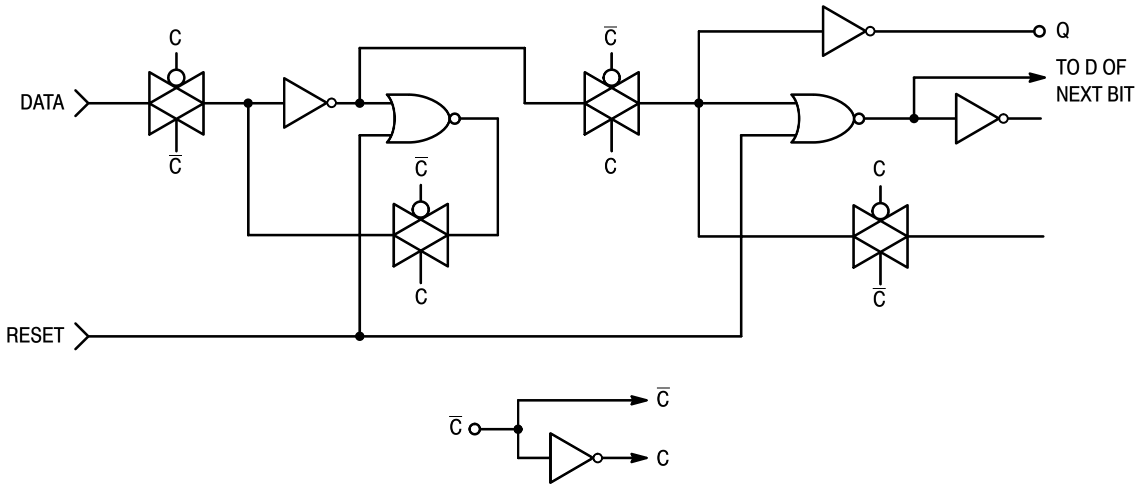


CLOCK INPUT BUFFER

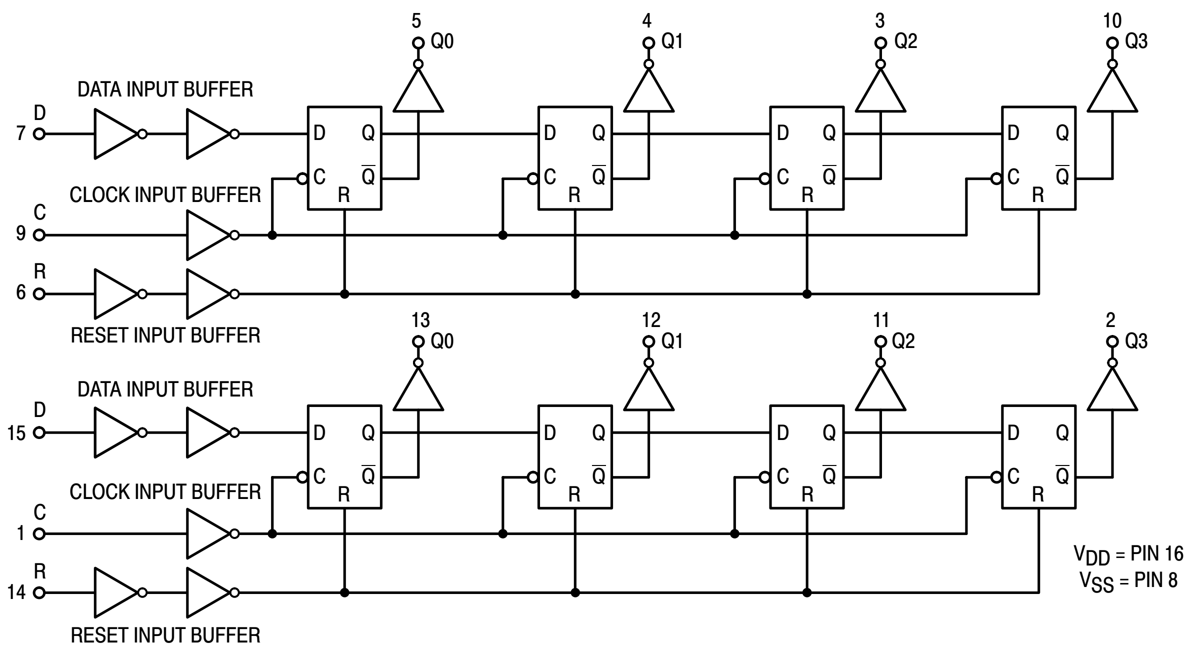


LOGIC DIAGRAMS

SINGLE BIT



COMPLETE DEVICE



MC14016B

Quad Analog Switch/ Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin−for−Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON}, Use The HC4016 High−Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ON Semiconductor

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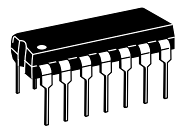
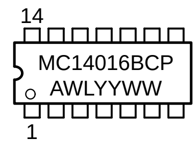
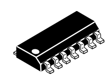
MARKING DIAGRAMS

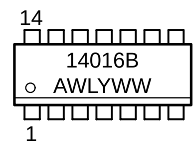


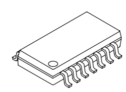
PDIP−14
P SUFFIX
CASE 646



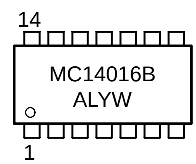


SOIC−14
D SUFFIX
CASE 751A





SOEIAJ−14
F SUFFIX
CASE 965



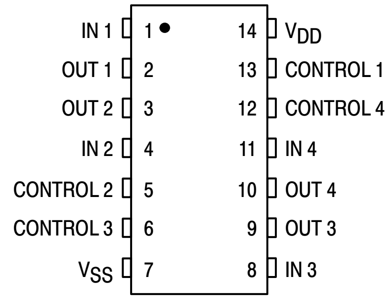
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

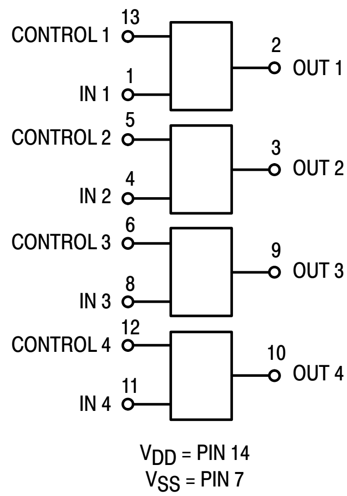
Device	Package	Shipping
MC14016BCP	PDIP−14	2000/Box
MC14016BD	SOIC−14	55/Rail
MC14016BDR2	SOIC−14	2500/Tape & Reel
MC14016BF	SOEIAJ−14	See Note 1.
MC14016BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

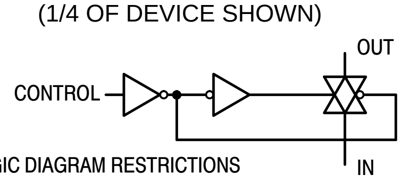


BLOCK DIAGRAM



Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM RESTRICTIONS
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Input Voltage Control Input	1	V_{IL}	5.0 10 15	— — —	— — —	— — —	1.5 1.5 1.5	0.9 0.9 0.9	— — —	— — —	Vdc
		V_{IH}	5.0 10 15	— — —	— — —	3.0 8.0 13	2.0 6.0 11	— — —	— — —	— — —	Vdc
Input Current Control	—	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	± 1.0	µAdc
Input Capacitance	—	C_{in}									pF
Control			—	—	—	—	5.0	—	—	—	
Switch Input			—	—	—	—	5.0	—	—	—	
Switch Output			—	—	—	—	5.0	—	—	—	
Feed Through			—	—	—	—	0.2	—	—	—	
Quiescent Current (Per Package) (5.)	2,3	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
“ON” Resistance	4,5,6	R_{ON}				—			—		Ohms
($V_C = V_{DD}$, R_L = 10 kΩ)						—			—		
(V_{in} = + 5.0 Vdc)				—	600	—	300	660	—	840	
(V_{in} = − 5.0 Vdc) V_{SS} = − 5.0 Vdc				—	600	—	300	660	—	840	
(V_{in} = ± 0.25 Vdc)			5.0	—	600	—	280	660	—	840	
(V_{in} = + 7.5 Vdc)				—	360	—	240	400	—	520	
(V_{in} = − 7.5 Vdc) V_{SS} = − 7.5 Vdc				—	360	—	240	400	—	520	
(V_{in} = ± 0.25 Vdc)			7.5	—	360	—	180	400	—	520	
(V_{in} = + 10 Vdc)				—	600	—	260	660	—	840	
(V_{in} = + 0.25 Vdc) V_{SS} = 0 Vdc				—	600	—	310	660	—	840	
(V_{in} = + 5.6 Vdc)			10	—	600	—	310	660	—	840	
(V_{in} = + 15 Vdc)				—	360	—	260	400	—	520	
(V_{in} = + 0.25 Vdc) V_{SS} = 0 Vdc				—	360	—	260	400	—	520	
(V_{in} = + 9.3 Vdc)			15	—	360	—	300	400	—	520	
Δ “ON” Resistance Between any 2 circuits in a common package ($V_C = V_{DD}$)	—	ΔR_{ON}									Ohms
(V_{in} = ± 5.0 Vdc, V_{SS} = − 5.0 Vdc)			5.0	—	—	—	15	—	—	—	
(V_{in} = ± 7.5 Vdc, V_{SS} = − 7.5 Vdc)			7.5	—	—	—	10	—	—	—	
Input/Output Leakage Current ($V_C = V_{SS}$)	—	—									µAdc
(V_{in} = + 7.5, V_{out} = − 7.5 Vdc)			7.5	—	±0.1	—	±0.0015	±0.1	—	± 1.0	
(V_{in} = − 7.5, V_{out} = + 7.5 Vdc)			7.5	—	±0.1	—	±0.0015	± 0.1	—	± 1.0	

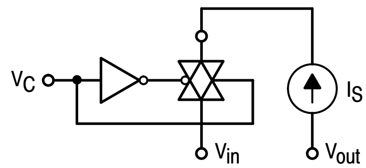
NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

ELECTRICAL CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Propagation Delay Time (V_{SS} = 0 Vdc) V_{in} to V_{out} (V_C = V_{DD}, R_L = 10 kΩ)	7	t_{PLH}, t_{PHL}	5.0 10 15	— — —	15 7.0 6.0	45 15 12	ns
Control to Output (V_{in} ≤ 10 Vdc, R_L = 10 kΩ)	8	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0 10 15	— — —	34 20 15	90 45 35	ns
Crosstalk, Control to Output (V_{SS} = 0 Vdc) (V_C = V_{DD}, R_{in} = 10 kΩ, R_{out} = 10 kΩ, f = 1.0 kHz)	9	—	5.0 10 15	— — —	30 50 100	— — —	mV
Crosstalk between any two switches (V_{SS} = 0 Vdc) (R_L = 1.0 kΩ, f = 1.0 MHz, $\text{crosstalk} = 20\log_{10}\frac{V_{out1}}{V_{out2}}$)	—	—	5.0	—	– 80	—	dB
Noise Voltage (V_{SS} = 0 Vdc) (V_C = V_{DD}, f = 100 Hz)	10,11	—	5.0 10 15	— — —	24 25 30	— — —	nV/√Cycle
(V_C = V_{DD}, f = 100 kHz)			5.0 10 15	— — —	12 12 15	— — —	
Second Harmonic Distortion (V_{SS} = – 5.0 Vdc) (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	—	5.0	—	0.16	—	%
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = − 5.0 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz) $I_{loss} = 20\log_{10}\frac{V_{out}}{V_{in}}$) ($R_L$ = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12	—	5.0	— — — —	2.3 0.2 0.1 0.05	— — — —	dB
Bandwidth (− 3.0 dB) (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = − 5.0 Vdc, RMS centered @ 0.0 Vdc) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12,13	BW	5.0	— — — —	54 40 38 37	— — — —	MHz
OFF Channel Feedthrough Attenuation (V_{SS} = − 5.0 Vdc) (V_C = V_{SS}, $20\log_{10}\frac{V_{out}}{V_{in}} = -50\,\text{dB}$) ($R_L$ = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	—	—	5.0	— — — —	1250 140 18 2.0	— — — —	kHz

6. The formulas given are for typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



V_{IL}: V_C is raised from V_{SS} until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10\ \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH}: When $V_C = V_{IH}$ to V_{DD}, the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

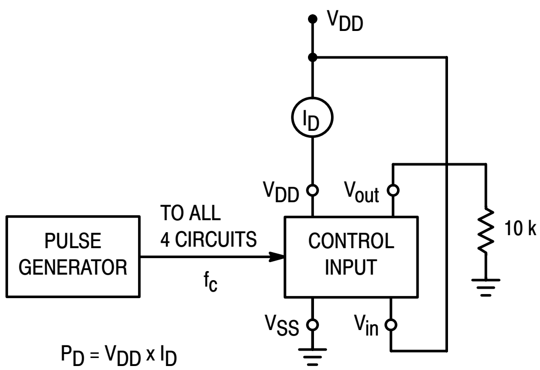


Figure 2. Quiescent Power Dissipation Test Circuit

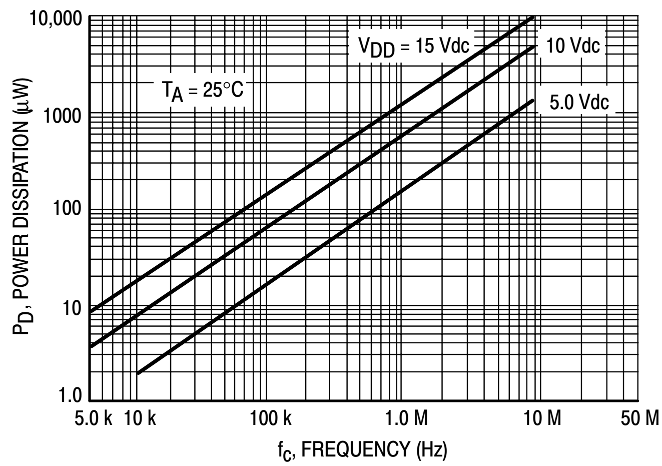


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

TYPICAL R_{ON} versus INPUT VOLTAGE

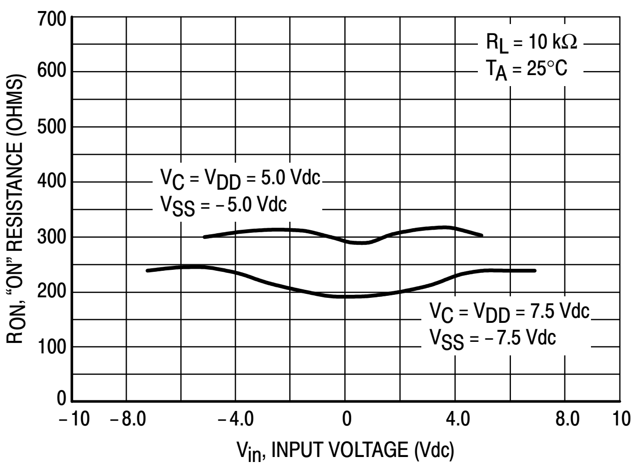


Figure 4. V_{SS} = − 5.0 V and − 7.5 V

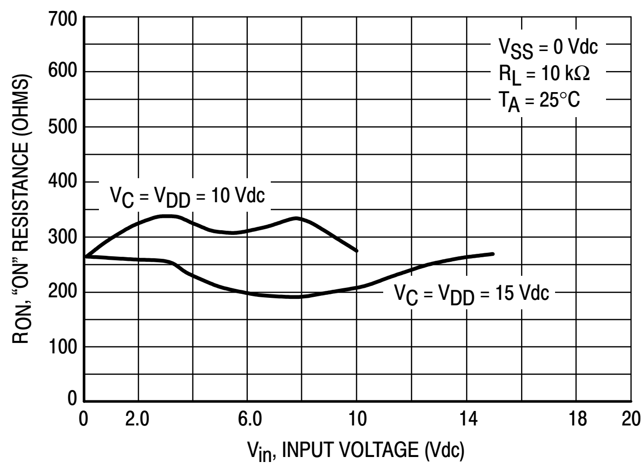


Figure 5. V_{SS} = 0 V

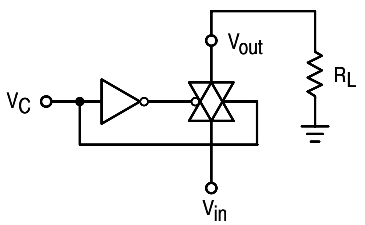


Figure 6. R_{ON} Characteristics Test Circuit

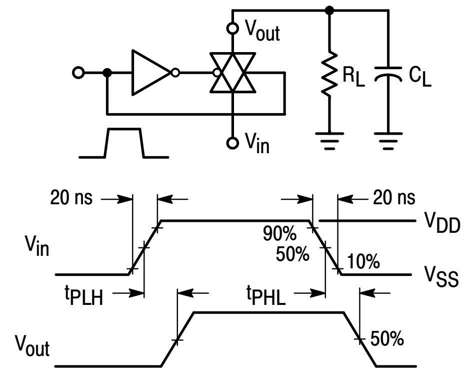


Figure 7. Propagation Delay Test Circuit and Waveforms

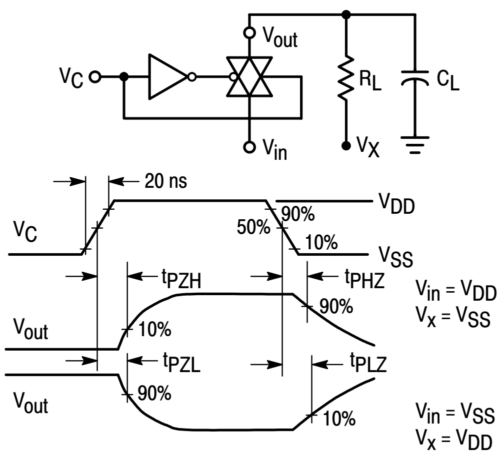


Figure 8. Turn−On Delay Time Test Circuit and Waveforms

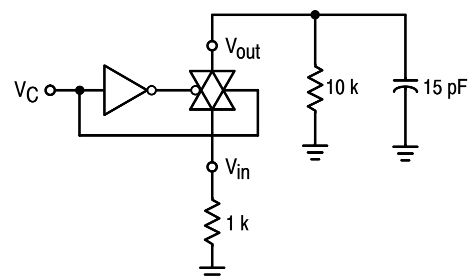


Figure 9. Crosstalk Test Circuit

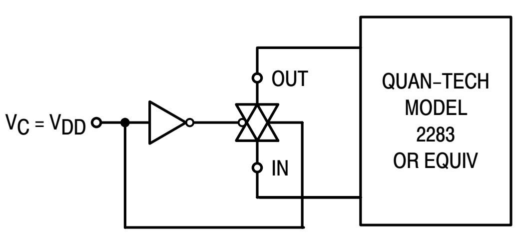


Figure 10. Noise Voltage Test Circuit

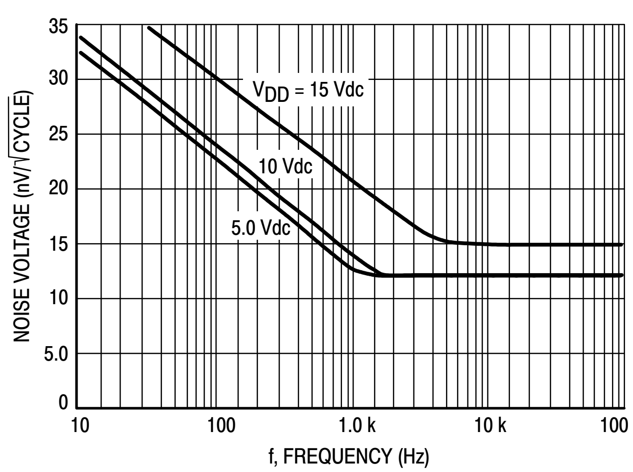


Figure 11. Typical Noise Characteristics

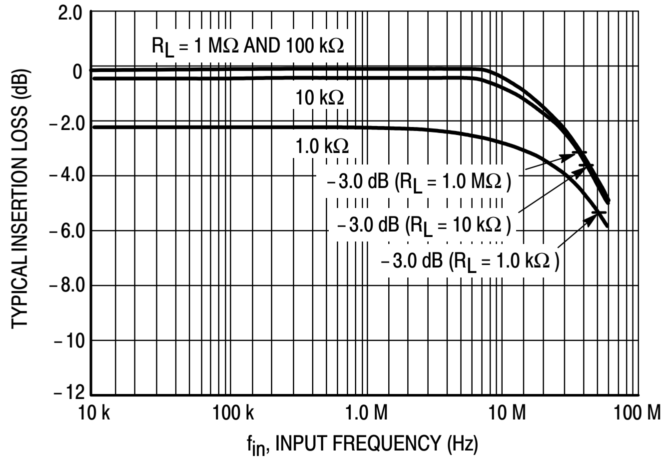


Figure 12. Typical Insertion Loss/Bandwidth Characteristics

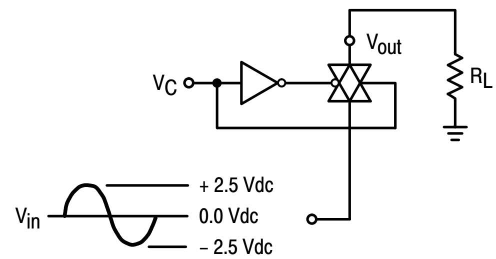


Figure 13. Frequency Response Test Circuit

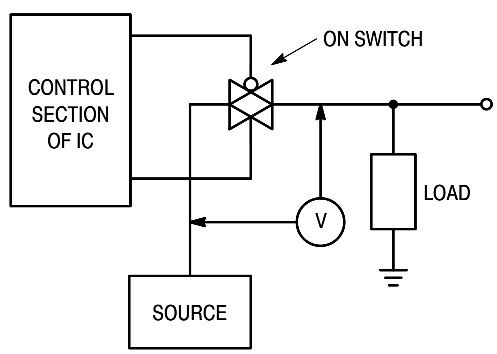


Figure 14. ∆V Across Switch

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0−to−5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V logic high at the control inputs; V_{SS} = GND = 0 V logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

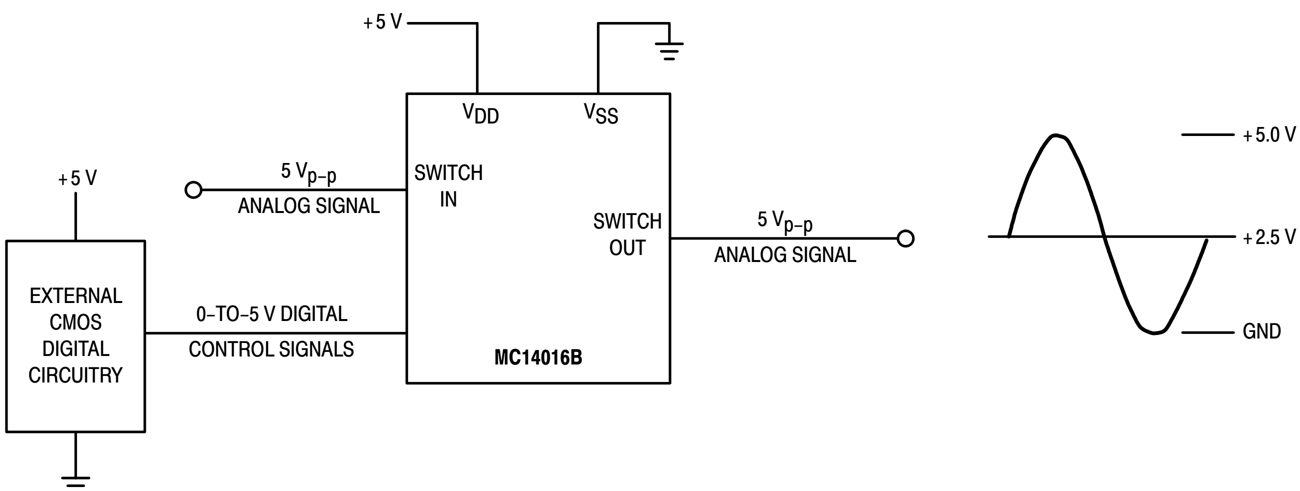


Figure A. Application Example

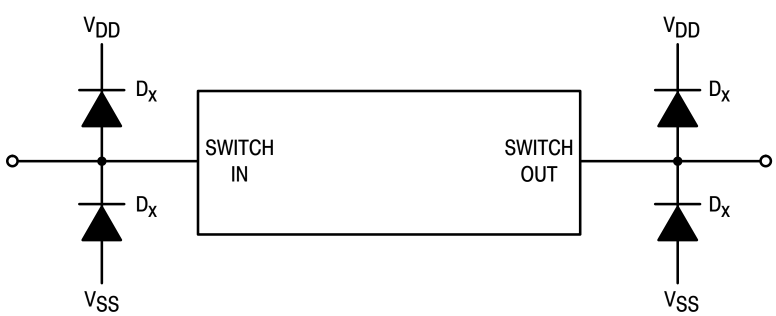


Figure B. External Germanium or Schottky Clipping Diodes

MC14017B

Decade Counter

The MC14017B is a five−stage Johnson decade counter with built−in code converter. High speed operation and spike−free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive−going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide−by−N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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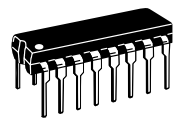
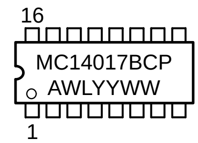
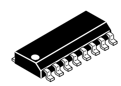
MARKING DIAGRAMS

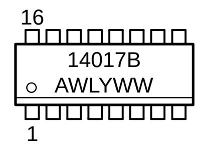


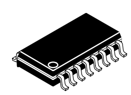
PDIP−16
P SUFFIX
CASE 648



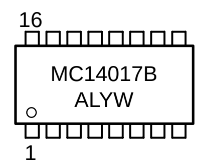


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



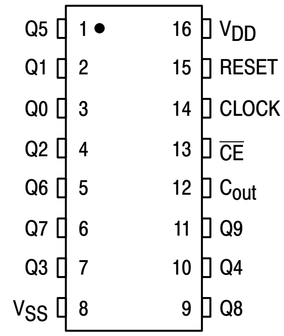
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14017BCP	PDIP−16	2000/Box
MC14017BD	SOIC−16	48/Rail
MC14017BDR2	SOIC−16	2500/Tape & Reel
MC14017BF	SOEIAJ−16	See Note 1.
MC14017BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

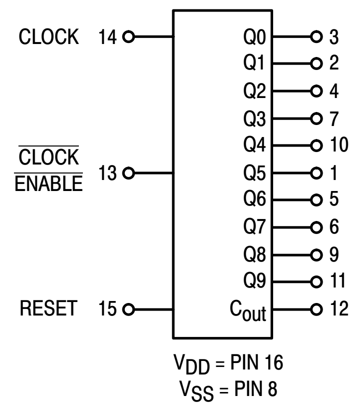


FUNCTIONAL TRUTH TABLE (Positive Logic)

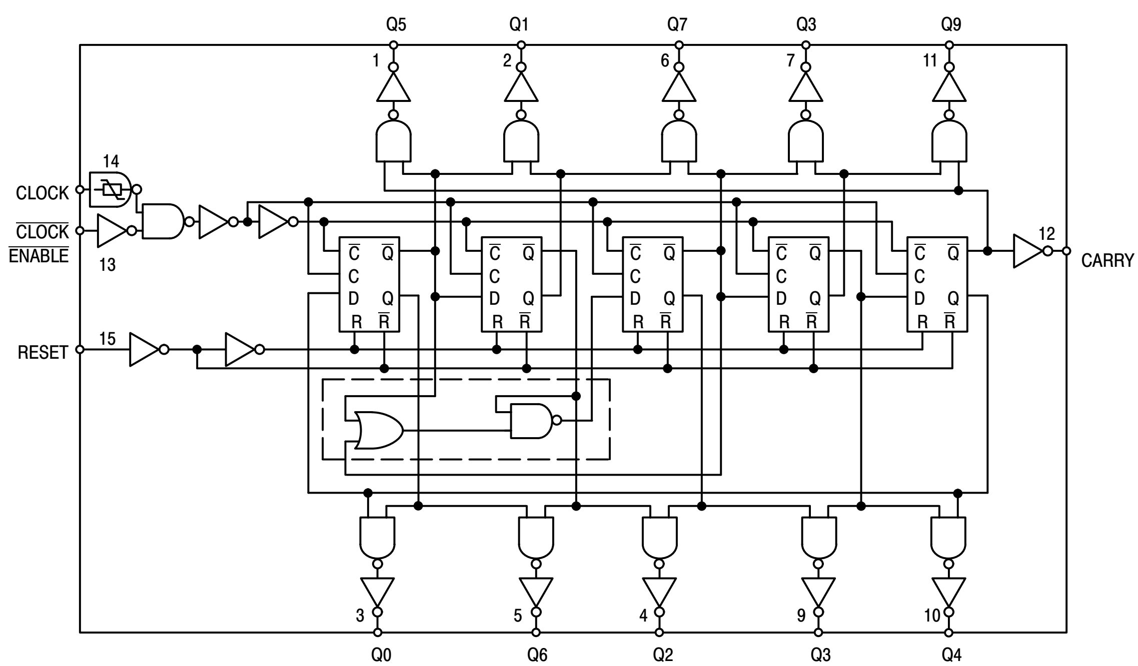
Clock	$\overline{\text{Clock}}$ Enable	Reset	Decode Output=n
0	X	0	n
X	1	0	n
X	X	1	Q0
↑	0	0	n+1
↓	X	0	n
X	↑	0	n
1	↓	0	n+1

X = Don’t Care. If n < 5 Carry = “1”, Otherwise = “0”.

BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.27 µA/kHz) f + I_{DD} I_T = (0.55 µA/kHz) f + I_{DD} I_T = (0.83 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

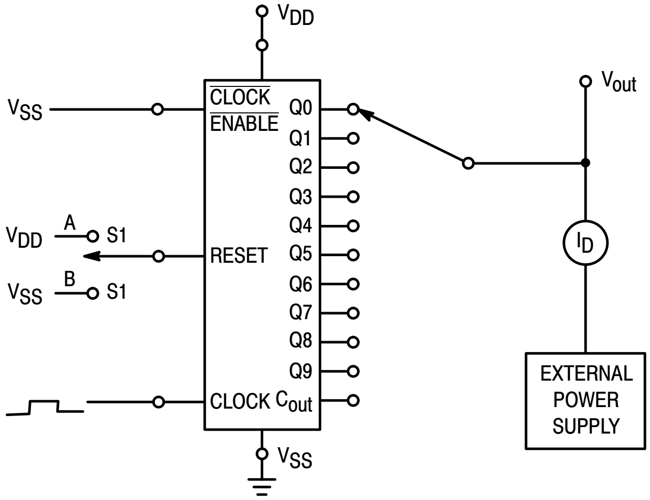
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.0011.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time Reset to Decode Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	—	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/PF) C_L + 197 ns		10	—	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	—	175	350	
Propagation Delay Time Clock to C_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	—	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	—	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	—	125	250	
Propagation Delay Time Clock to Decode Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	—	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	—	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	—	175	350	
Turn−Off Delay Time Reset to C_{out}	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	—	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	—	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	—	125	250	
Clock Pulse Width	$t_{w(H)}$	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	f_{cl}	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	$t_{w(H)}$	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15		No Limit		—
$\overline{\text{Clock Enable}}$ Setup Time	t_{su}	5.0 10 15	350 150 115	175 75 52	— — —	ns
$\overline{\text{Clock Enable}}$ Removal Time	t_{rem}	5.0 10 15	420 200 140	260 100 70	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



	Output Sink Drive	Output Source Drive
Decode Outputs	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

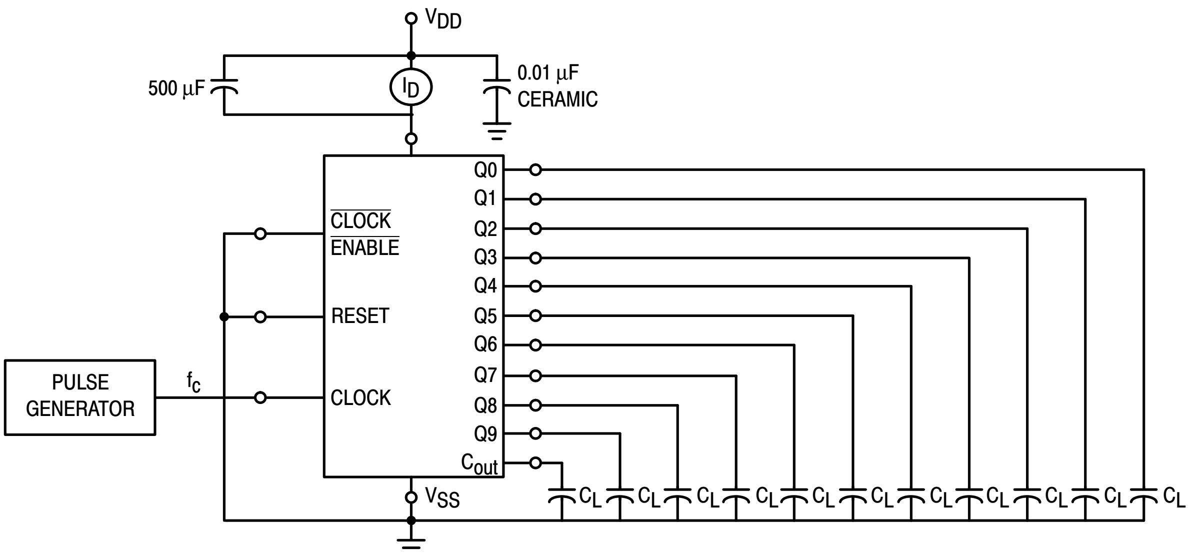


Figure 2. Typical Power Dissipation Test Circuit

APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

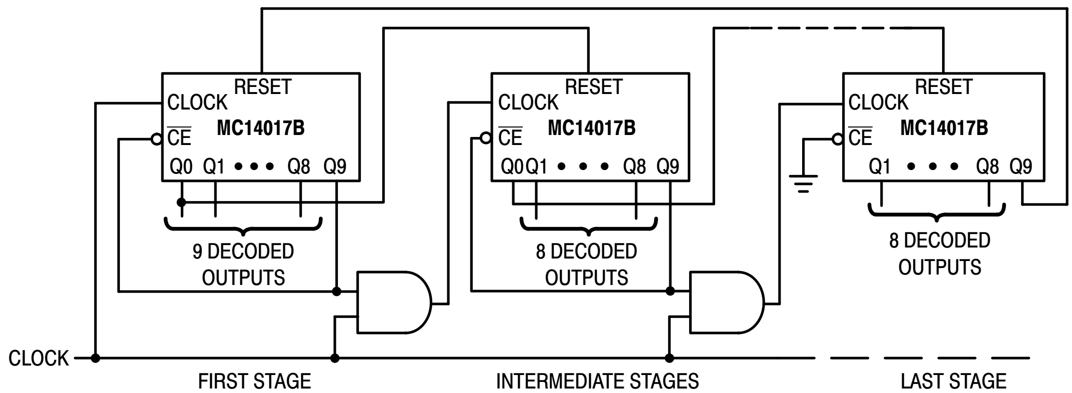


Figure 3. Counter Expansion

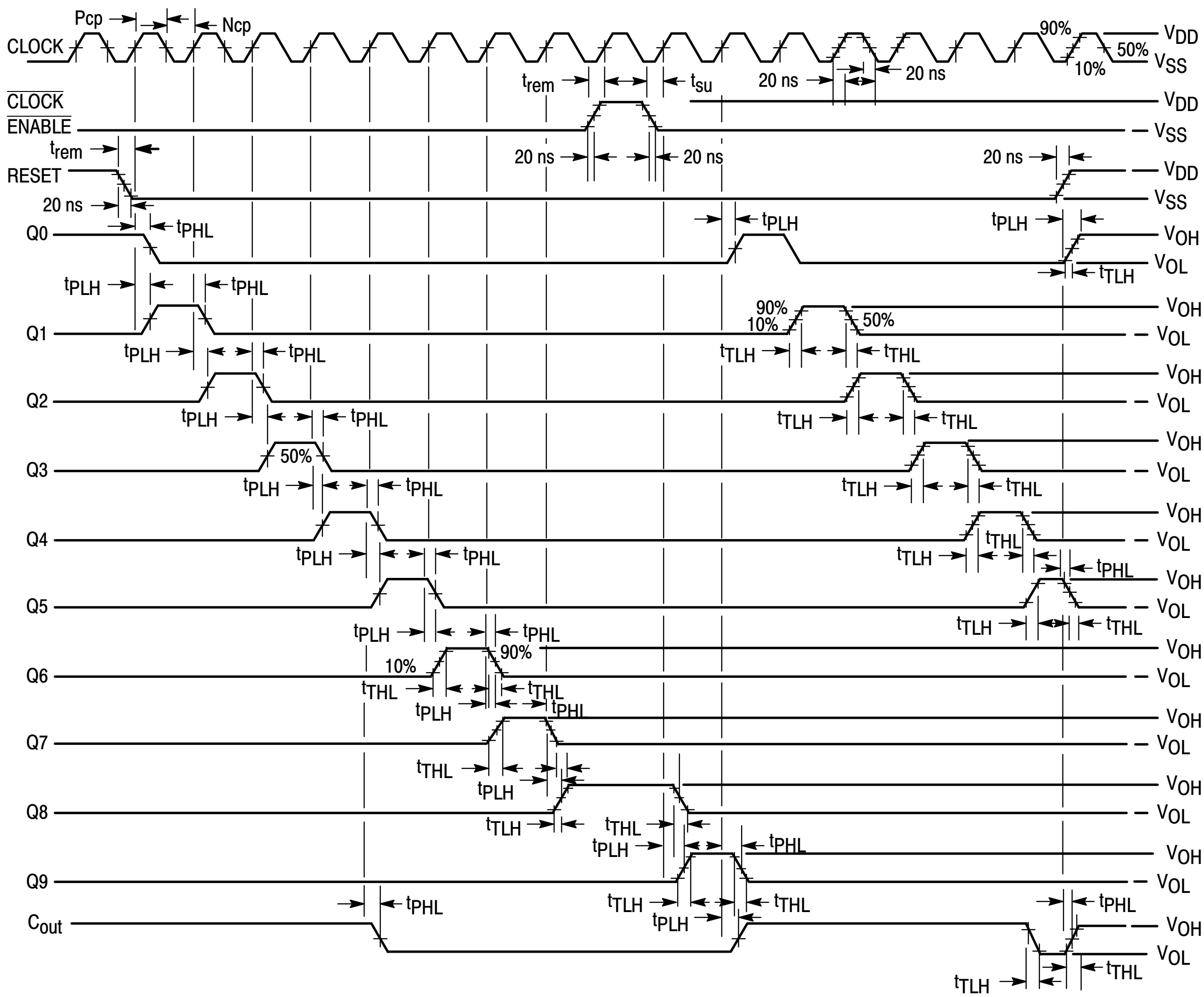


Figure 4. AC Measurement Definition and Functional Waveforms

MC14018B

Presettable Divide-By-N Counter

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti−lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4018B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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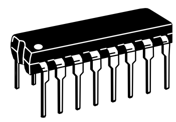
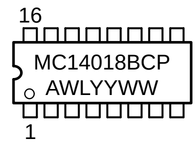
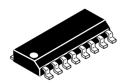
MARKING DIAGRAMS

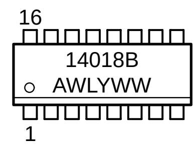


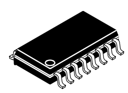
PDIP−16
P SUFFIX
CASE 648



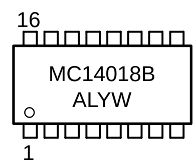


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

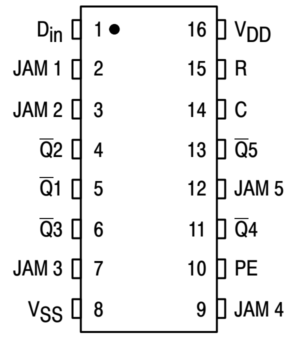
ORDERING INFORMATION

Device	Package	Shipping
MC14018BCP	PDIP−16	2000/Box
MC14018BD	SOIC−16	48/Rail
MC14018BDR2	SOIC−16	2500/Tape & Reel
MC14018BF	SOEIAJ−16	See Note 1.
MC14018BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

August, 2000 − Rev. 4
Publication Order Number:
MC14018B/D

PIN ASSIGNMENT



FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}n$
↓	0	0	X	$\overline{Q}n$
↑	0	0	X	$\overline{D}_n$*
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

*D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	 Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD} I_T = (0.7 µA/kHz) f + I_{DD} I_T = (1.0 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time Clock to $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 265 ns		5.0	—	310	620	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 102 ns		10	—	120	240	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	—	85	170	
Reset to $\overline{Q}$						ns
t_{PLH} = (0.90 ns/pF) C_L + 325 ns		5.0	—	370	740	
t_{PLH} = (0.36 ns/pF) C_L + 132 ns		10	—	150	300	
t_{PLH} = (0.26 ns/pF) C_L + 81 ns		15	—	100	200	
Preset Enable to $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 325 ns		5.0	—	370	740	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 81 ns		15	—	100	200	
Setup Time Data (Pin 1) to Clock	t_{su}	5.0	200	0	—	ns
		10	100	0	—	
		15	80	0	—	
Jam Inputs to Preset Enable		5.0	200	0	—	ns
		10	100	0	—	
		15	80	0	—	
Data (Jam Inputs)−to−Preset Enable Hold Time	t_h	5.0	540	270	—	ns
		10	500	250	—	
		15	480	240	—	
Clock Pulse Width	t_{WH}	5.0	400	200	—	ns
		10	200	100	—	
		15	160	80	—	
Reset or Preset Enable Pulse Width	t_{WH}	5.0	290	145	—	ns
		10	130	65	—	
		15	110	55	—	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.25	MHz
		10	—	6.5	3.25	
		15	—	8.0	4.0	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

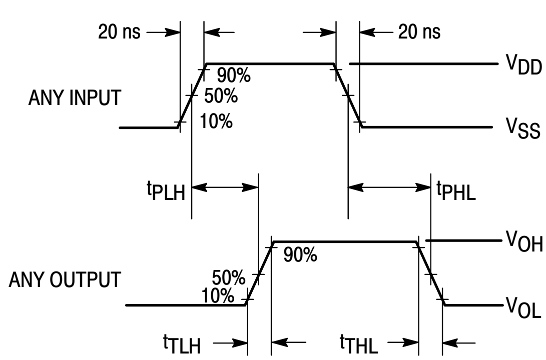
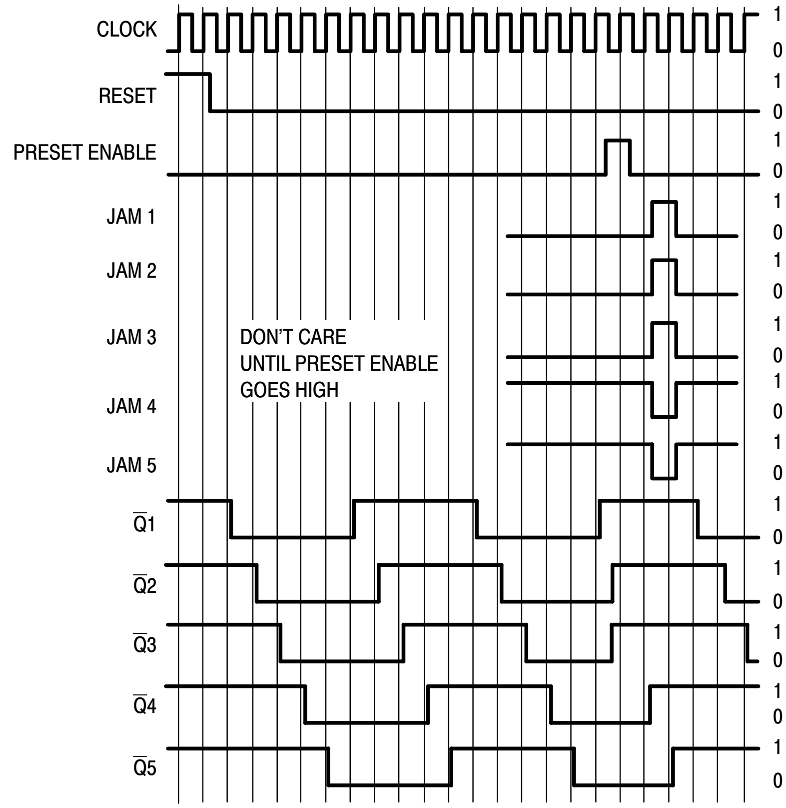


Figure 1. Switching Time Waveforms

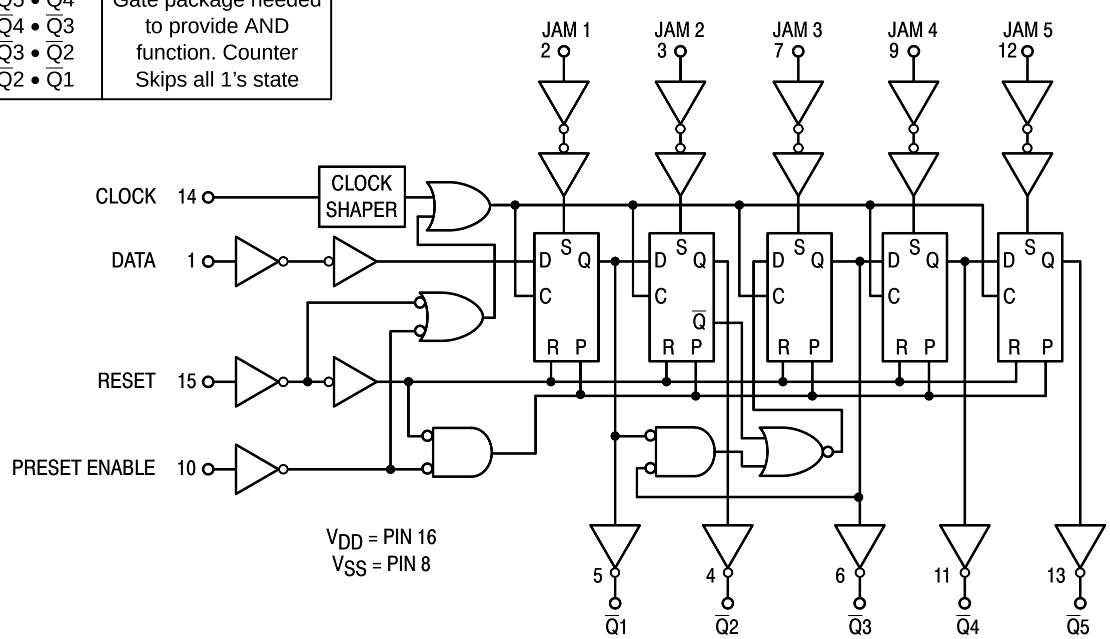
TIMING DIAGRAM
($\overline{Q}5$ Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10 Divide by 8 Divide by 6 Divide by 4 Divide by 2	$\overline{Q}5$ $\overline{Q}4$ $\overline{Q}3$ $\overline{Q}2$ $\overline{Q}1$	No external components needed.
Divide by 9 Divide by 7 Divide by 5 Divide by 3	$\overline{Q}5 \bullet \overline{Q}4$ $\overline{Q}4 \bullet \overline{Q}3$ $\overline{Q}3 \bullet \overline{Q}2$ $\overline{Q}2 \bullet \overline{Q}1$	Gate package needed to provide AND function. Counter Skips all 1's state

LOGIC DIAGRAM



MC14020B

14-Bit Binary Counter

The MC14020B 14−stage binary counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin−for−Pin Replacement for CD4020B

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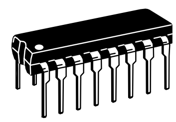
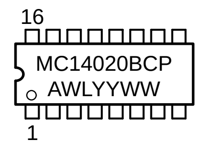
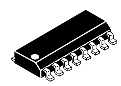
MARKING DIAGRAMS

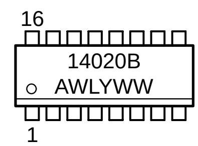


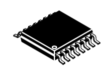
PDIP−16
P SUFFIX
CASE 648



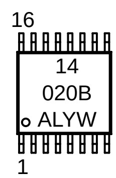


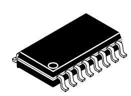
SOIC−16
D SUFFIX
CASE 751B



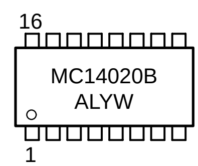


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

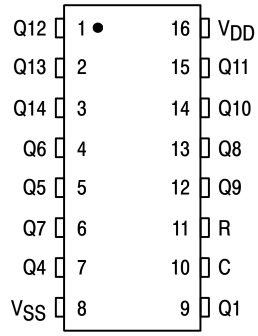
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

Device	Package	Shipping
MC14020BCP	PDIP−16	2000/Box
MC14020BD	SOIC−16	48/Rail
MC14020BDR2	SOIC−16	2500/Tape & Reel
MC14020BDT	TSSOP−16	96/Rail
MC14020BF	SOEIAJ−16	See Note 1.
MC14020BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

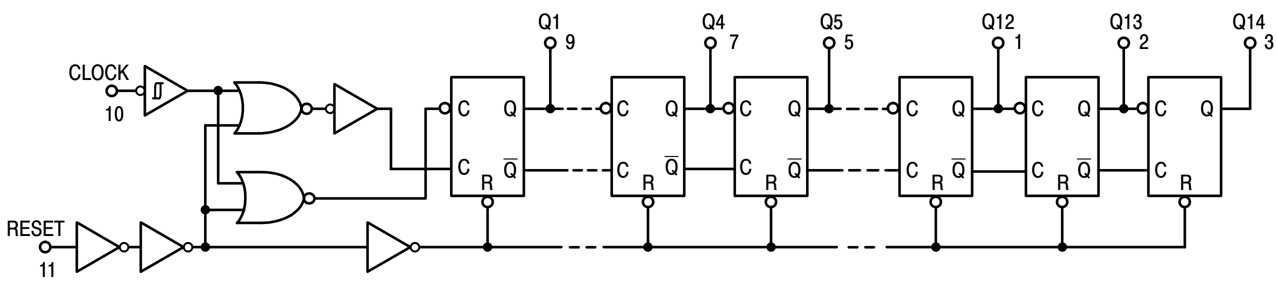


TRUTH TABLE

Clock	Reset	Output State
↑	0	No Change
↓	0	Advance to Next State
X	1	All Outputs are Low

X = Don’t Care

LOGIC DIAGRAM



Q6 = PIN 4
Q7 = PIN 6
Q8 = PIN 13

Q9 = PIN 12
Q10 = PIN 14
Q11 = PIN 15

V_{DD} = PIN 16
V_{SS} = PIN 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.42 µA/kHz)f + I_{DD} I_T = (0.85 µA/kHz)f + I_{DD} I_T = (1.43 µA/kHz)f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time Clock to Q1	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 175 ns		5.0	—	260	520	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 82 ns		10	—	115	230	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 55 ns		15	—	80	160	
Clock to Q14						ns
t_{PHL}, t_{PLH} − (1.7 ns/pF) C_L + 1735 ns		5.0	—	1820	3900	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 772 ns		10	—	805	1725	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 535 ns		15	—	560	1200	
Propagation Delay Time Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 285 ns		5.0	—	370	740	
t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	—	155	310	
t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	—	115	230	
Clock Pulse Width	t_{WH}	5.0	500	140	—	ns
		10	165	55	—	
		15	125	38	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.0	1.0	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0				—
		10		No Limit		
		15				
Reset Pulse Width	t_{WL}	5.0	3000	320	—	ns
		10	550	120	—	
		15	420	80	—	
Reset Removal Time	t_{rem}	5.0	130	65	—	ns
		10	50	25	—	
		15	30	15	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

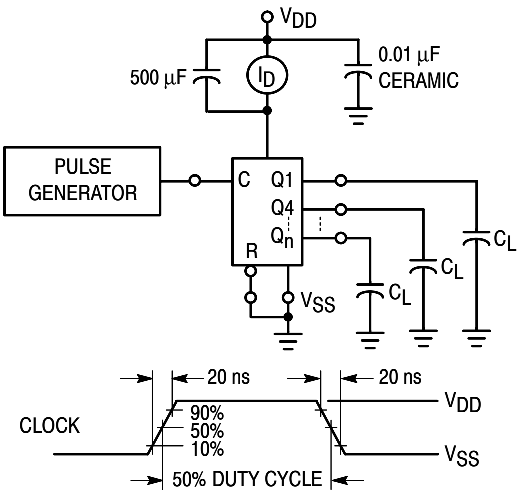


Figure 1. Power Dissipation Test Circuit and Waveform

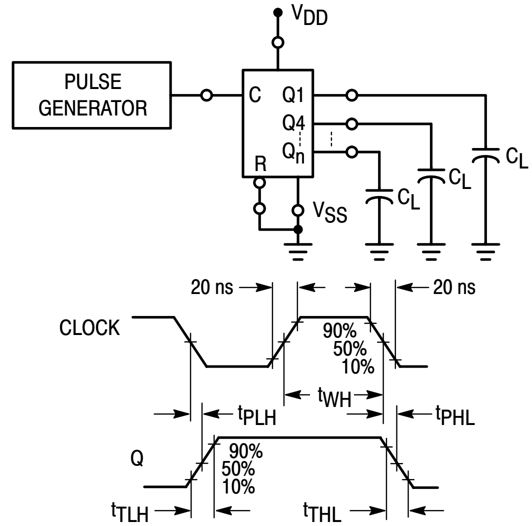


Figure 2. Switching Time Test Circuit and Waveforms

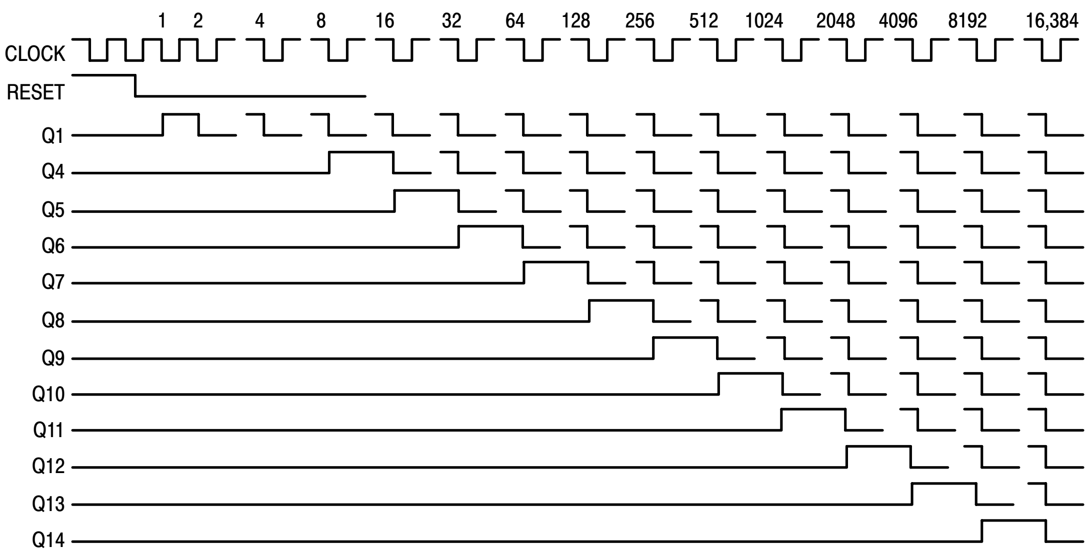


Figure 3. Timing Diagram

MC14022B

Octal Counter

The MC14022B is a four−stage Johnson octal counter with built−in code converter. High−speed operation and spike−free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive−going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4022B
- Triple Diode Protection on All Inputs

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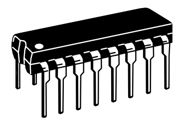
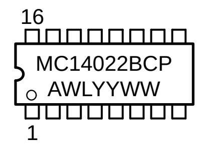
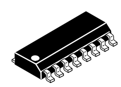
MARKING DIAGRAMS

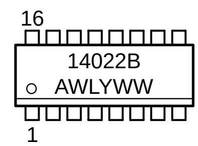


PDIP−16
P SUFFIX
CASE 648





SOIC−16
D SUFFIX
CASE 751B



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14022BCP	PDIP−16	2000/Box
MC14022BD	SOIC−16	2400/Box
MC14022BDR2	SOIC−16	2500/Tape & Reel

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

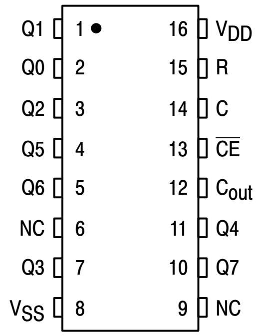
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

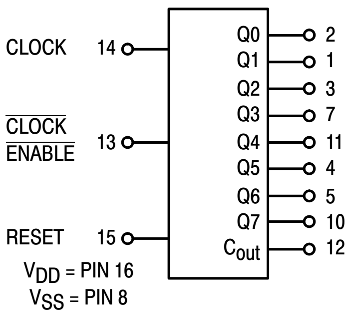
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



NC = NO CONNECTION

BLOCK DIAGRAM



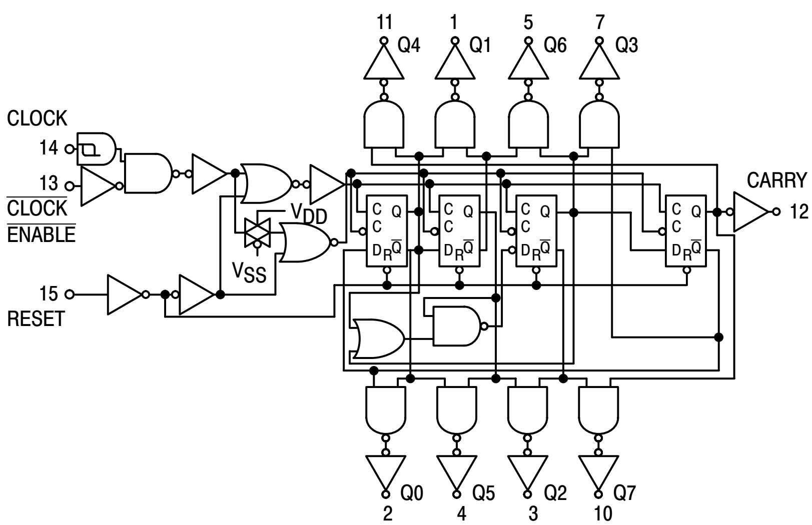
NC = PIN 6, 9

FUNCTIONAL TRUTH TABLE (Positive Logic)

Clock	$\overline{\text{Clock Enable}}$	Reset	Output=n
0	X	0	n
X	1	0	n
↑	0	0	n+1
↓	X	0	n
1	↓	0	n+1
X	↑	0	n
X	X	1	Q0

X = Don’t Care. If n < 4 Carry = 1, Otherwise = 0.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.28 µA/kHz)f + I_{DD}							µAdc
		10	I_T = (0.56 µA/kHz)f + I_{DD}							
		15	I_T = (0.85 µA/kHz)f + I_{DD}							

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

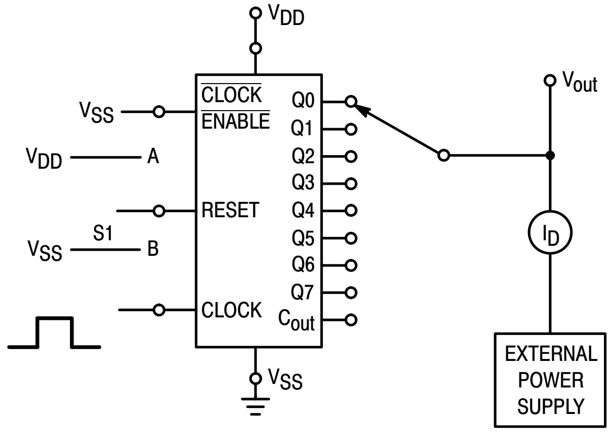
$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.00125.

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [7.]	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time Reset to Decode Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 500 230 175	 1000 460 350	ns
Propagation Delay Time Clock to C_{out} t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 400 175 125	 800 350 250	ns
Propagation Delay Time Clock to Decode Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 275 125 95	 1000 460 350	ns
Turn−Off Delay Time Reset to C_{out} t_{PLH} = (1.7 ns/pF) C_L + 315 ns t_{PLH} = (0.66 ns/pF) C_L + 142 ns t_{PLH} = (0.5 ns/pF) C_L + 100 ns	t_{PLH}	 5.0 10 15	 — — —	 400 175 125	 800 350 250	ns
Clock Pulse Width	t_{WH}	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	f_{cl}	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	t_{WH}	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15		No Limit		—
$\overline{\text{Clock Enable}}$ Setup Time	t_{su}	5.0 10 15	350 150 115	175 75 52	— — —	ns
$\overline{\text{Clock Enable}}$ Removal Time	t_{rem}	5.0 10 15	420 200 140	260 100 70	— — —	ns

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



	Output Sink Drive	**Output Source Drive**
Outputs	**(S1 to A)**	**Clock to desired Output (S1 to B)**
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

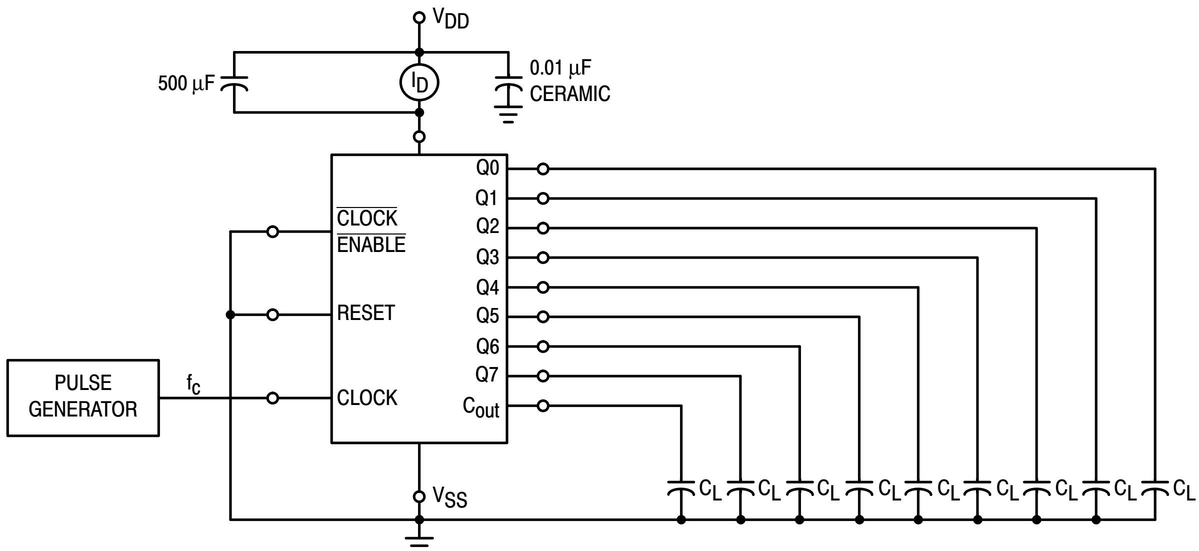


Figure 2. Typical Power Dissipation Test Circuit

APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

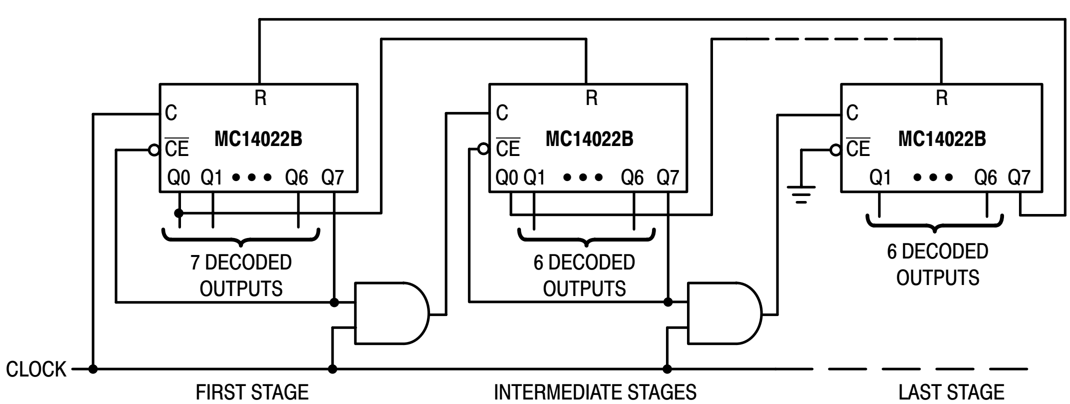


Figure 3. Counter Expansion

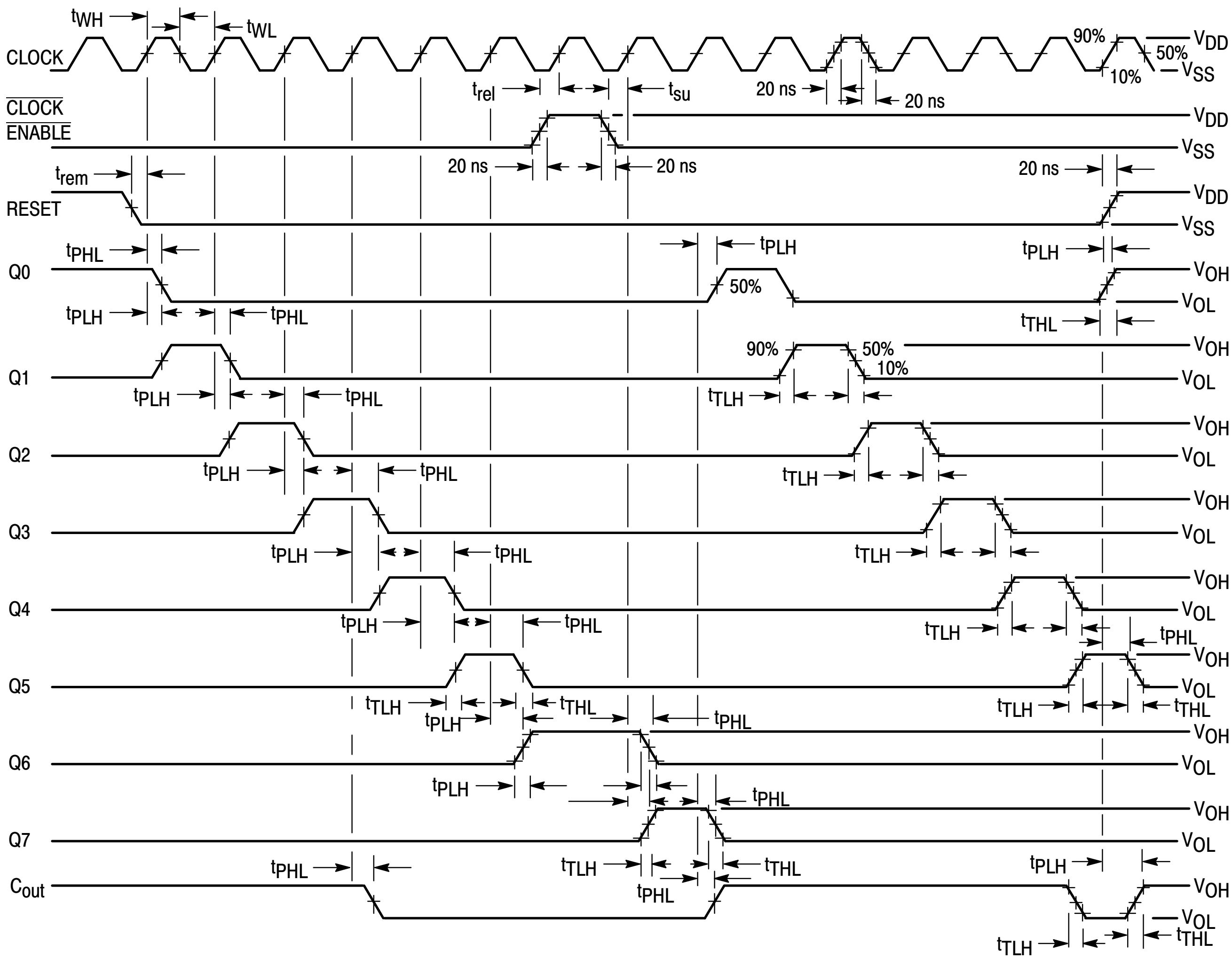


Figure 4. AC Measurement Definition and Functional Waveforms

MC14024B

7-Stage Ripple Counter

The MC14024B is a 7−stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4024B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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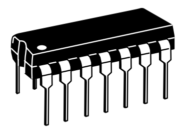
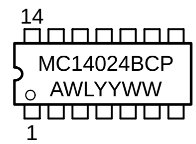
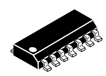
MARKING DIAGRAMS

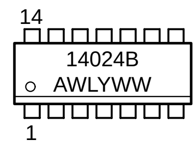


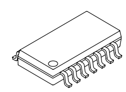
PDIP−14
P SUFFIX
CASE 646



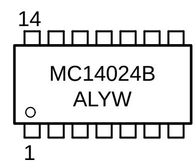


SOIC−14
D SUFFIX
CASE 751A





SOEIAJ−14
F SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

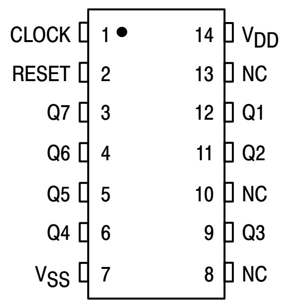
Device	Package	Shipping
MC14024BCP	PDIP−14	2000/Box
MC14024BD	SOIC−14	2750/Box
MC14024BDR2	SOIC−14	2500/Tape & Reel
MC14024BF	SOEIAJ−14	See Note 1.
MC14024BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

TRUTH TABLE

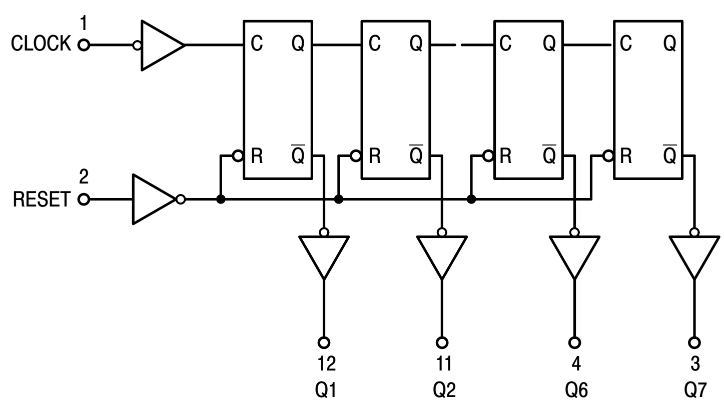
Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
_/‾	0	No Change
_/‾	1	All Outputs Low
‾_	0	Advance One Count
‾_	1	All Outputs Low

PIN ASSIGNMENT



V_{DD} = PIN 14
V_{SS} = PIN 7
NC = NO CONNECTION

LOGIC DIAGRAM



Q3 = PIN 9
Q4 = PIN 6
Q5 = PIN 5

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ [4.]	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.31 μA/kHz) f + I_{DD} I_T = (0.60 μA/kHz) f + I_{DD} I_T = (1.89 μA/kHz) f + I_{DD}							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	—	380	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	—	150	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	—	110	175	
Clock to Q7						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 915 ns		5.0	—	1000	2000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	—	400	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	—	300	565	
Reset to Q_n						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	—	500	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	—	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	—	180	300	
Clock Pulse Width	t_{WH}	5.0	500	200	—	ns
		10	165	60	—	
		15	125	40	—	
Reset Pulse Width	t_{WH}	5.0	600	375	—	ns
		10	350	200	—	
		15	260	150	—	
Reset Removal Time	t_{rem}	5.0	625	250	—	ns
		10	190	75	—	
		15	145	50	—	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	1.0	s
		10	—	—	8.0	ms
		15	—	—	200	µs
Input Pulse Frequency	f_{cl}	5.0	—	2.5	1.0	MHz
		10	—	8.0	3.0	
		15	—	12	4.0	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

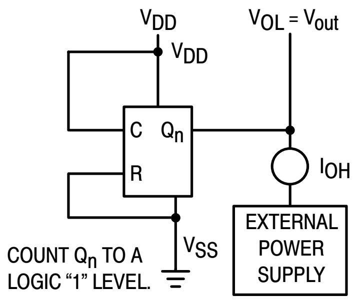


Figure 1. Typical Output Source Characteristics Test Circuit

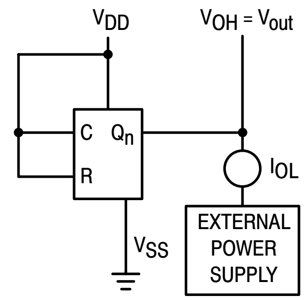


Figure 2. Typical Output Sink Characteristics Test Circuit

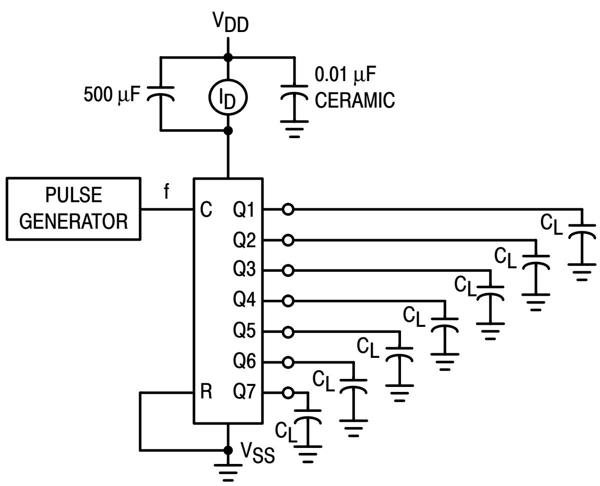
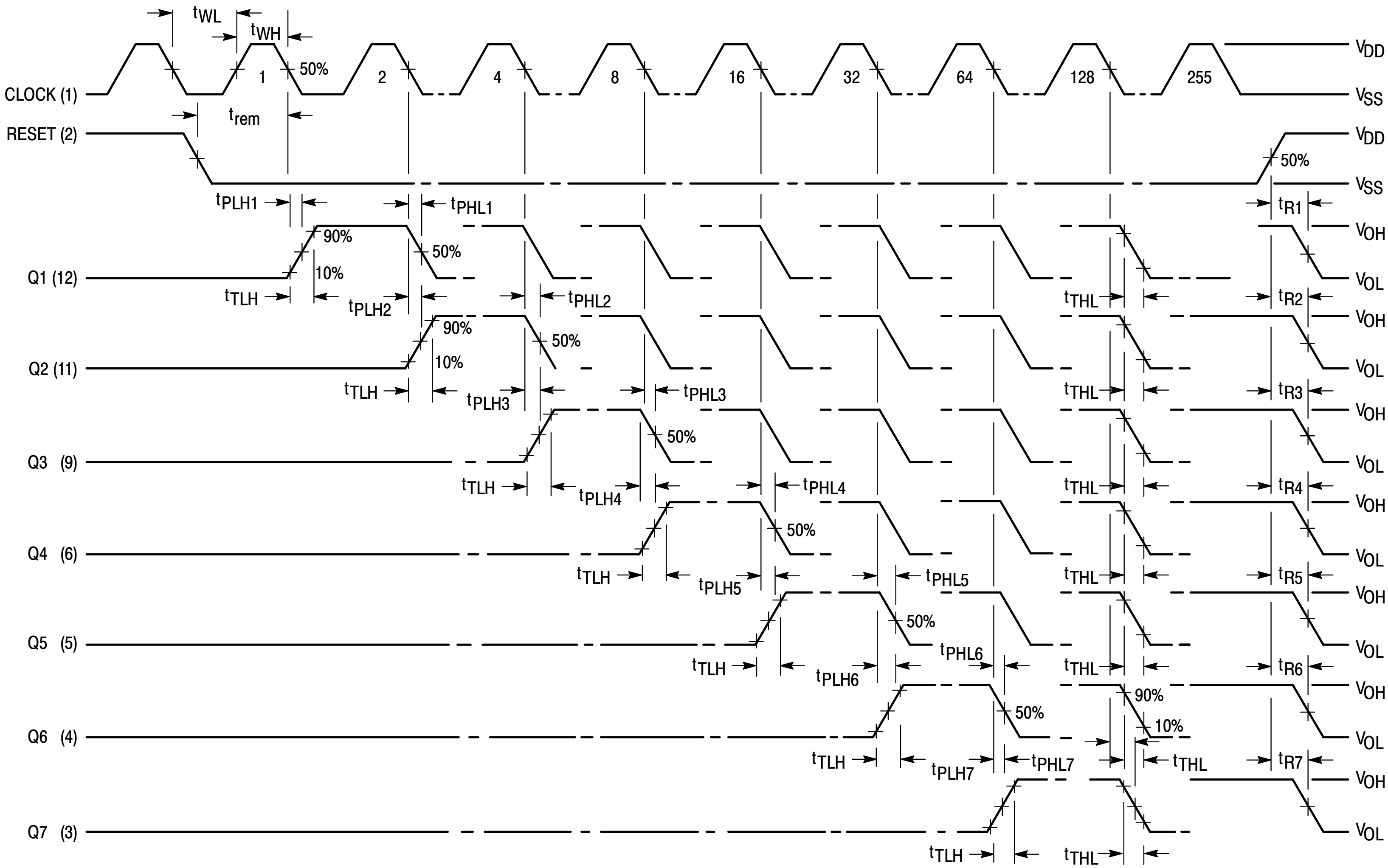


Figure 3. Power Dissipation Test Circuit



Input t_{TLH} and t_{THL} = 20 ns

Figure 4. Functional Waveforms

MC14027B

Dual J-K Flip-Flop

The MC14027B dual J−K flip−flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip−flop. These devices may be used in control, register, or toggle functions.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge−Clocked Flip−Flop Design — Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive−going edge of the clock pulse
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4027B

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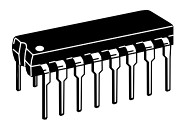
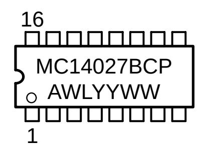
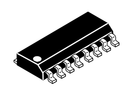
MARKING DIAGRAMS

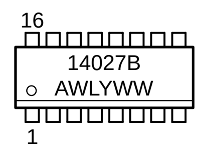


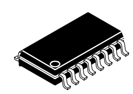
PDIP−16
P SUFFIX
CASE 648



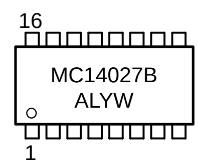


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

Device	Package	Shipping
MC14027BCP	PDIP−16	2000/Box
MC14027BD	SOIC−16	2400/Box
MC14027BDR2	SOIC−16	2500/Tape & Reel
MC14027BF	SOEIAJ−16	See Note 1.
MC14027BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

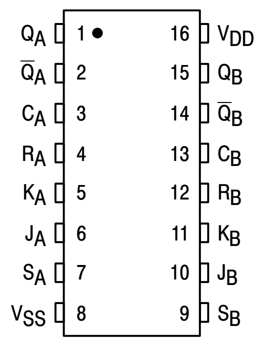
TRUTH TABLE

Inputs						Outputs*	
C†	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$
_/‾	1	X	0	0	0	1	0
_/‾	X	0	0	0	1	1	0
_/‾	0	X	0	0	0	0	1
_/‾	X	1	0	0	1	0	1
_/‾	1	1	0	0	Qo	$\overline{Qo}$	Qo
‾_	X	X	0	0	X	Q_n	$\overline{Q_n}$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

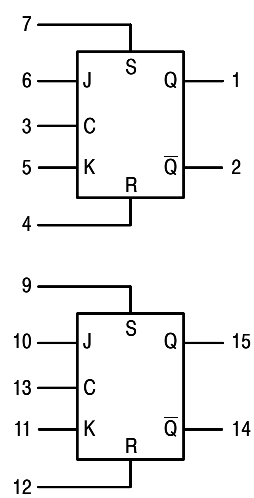
No Change

X = Don't Care
† = Level Change
‡ = Present State
* = Next State

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 − 1.3 − 3.4	 – 4.2 – 0.88 – 2.25 − 8.8	 — — — —	 – 1.7 − 0.36 – 0.9 − 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.8 µA/kHz) f + I_{DD} I_T = (1.6 µA/kHz) f + I_{DD} I_T = (2.4 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

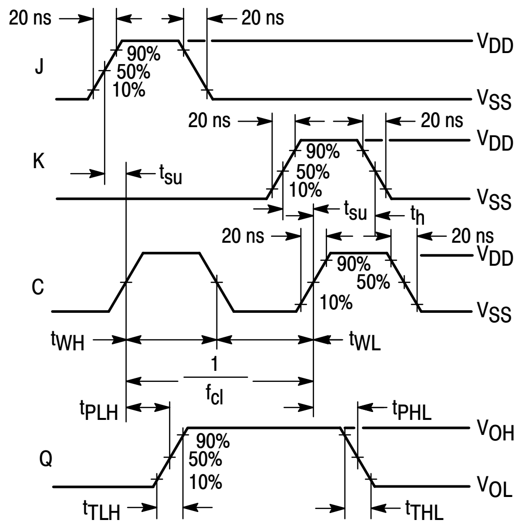
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	—	40	80	
Propagation Delay Times**	t_{PLH}, t_{PHL}					ns
Clock to Q, Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	—	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	—	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	—	50	100	
Set to Q, Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	—	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	—	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	—	50	100	
Reset to Q, Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	—	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	—	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	—	75	150	
Setup Times	t_{su}	5.0	140	70	—	ns
		10	50	25	—	
		15	35	17	—	
Hold Times	t_h	5.0	140	70	—	ns
		10	50	25	—	
		15	35	17	—	
Clock Pulse Width	t_{WH}, t_{WL}	5.0	330	165	—	ns
		10	110	55	—	
		15	75	38	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.0	1.5	MHz
		10	—	9.0	4.5	
		15	—	13	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5.0	
		15	—	—	4.0	
Removal Times	t_{rem}					ns
		5	90	10	—	
Set		10	45	5	—	
		15	35	3	—	
		5	50	– 30	—	
Reset		10	25	– 15	—	
		15	20	– 10	—	
Set and Reset Pulse Width	t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



Inputs R and S low.
For the measurement of t_{WH}, l/f_{cl}, and P_D
the Inputs J and K are kept high.

Figure 1. Dynamic Signal Waveforms (J, K, Clock, and Output)

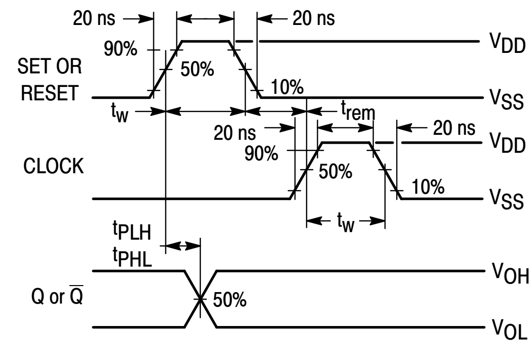
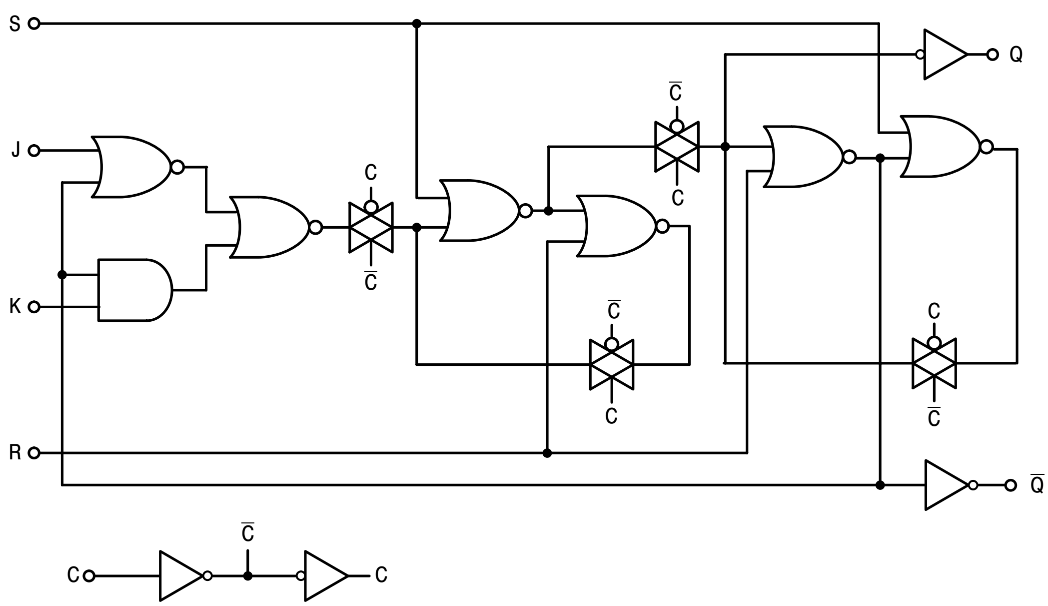


Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)

LOGIC DIAGRAM
(1/2 of Device Shown)



MC14028B

BCD-To-Decimal Decoder Binary-To-Octal Decoder

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one−of−ten) decoded output, while a 3−bit binary input provides a decoded octal (one−of−eight) code output with D forced to a logic “0”. Expanded decoding such as binary−to−hexadecimal (one−of−16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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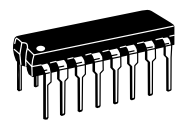
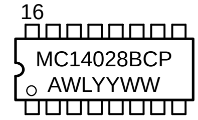
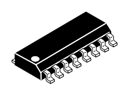
MARKING DIAGRAMS

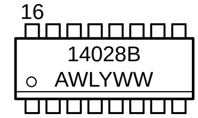


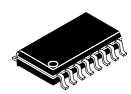
PDIP−16
P SUFFIX
CASE 648



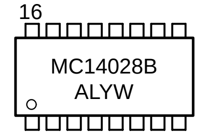


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

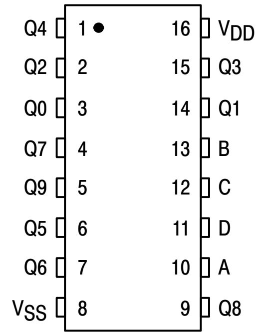
ORDERING INFORMATION

Device	Package	Shipping
MC14028BCP	PDIP−16	2000/Box
MC14028BD	SOIC−16	2400/Box
MC14028BDR2	SOIC−16	2500/Tape & Reel
MC14028BF	SOEIAJ−16	See Note 1.
MC14028BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

August, 2000 − Rev. 4
Publication Order Number:
MC14028B/D

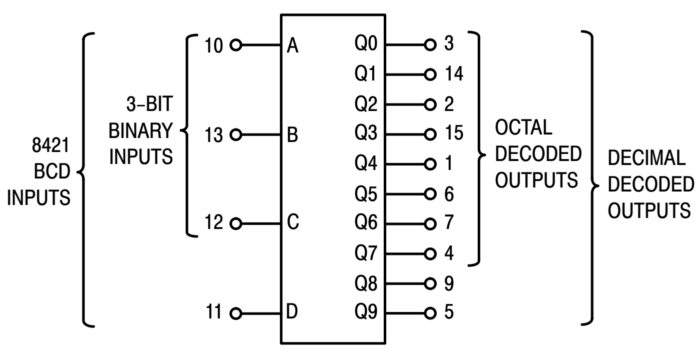
PIN ASSIGNMENT



TRUTH TABLE

D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD} I_T = (0.6 µA/kHz) f + I_{DD} I_T = (0.9 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	300 130 90	600 260 180	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Inputs B, C, and D switching in respect to a BCD code.

All outputs connected to respective C_L loads. f in respect to a system clock.

Inputs A, B, and D low.

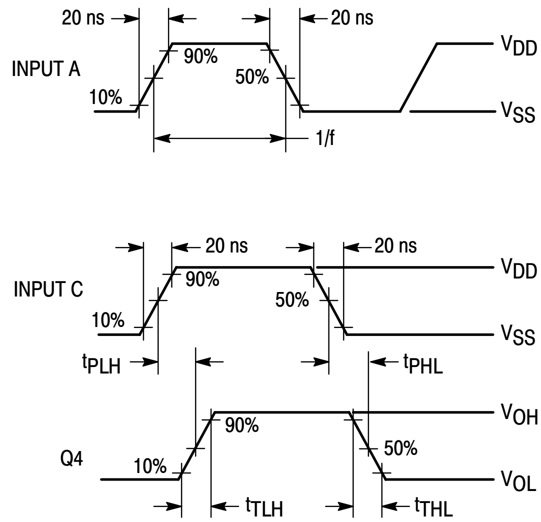
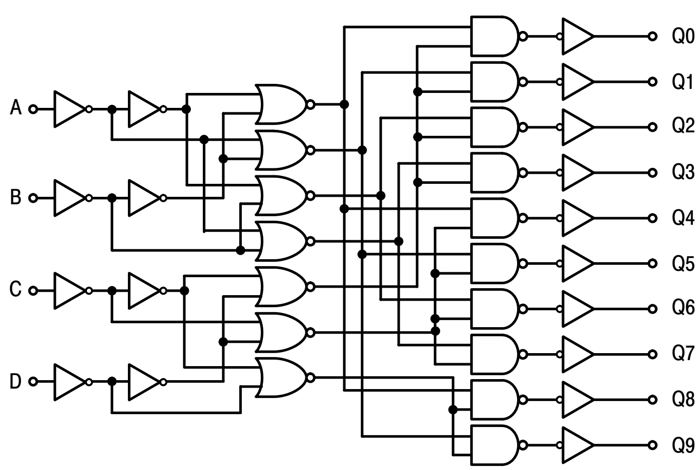


Figure 1. Dynamic Signal Waveforms

LOGIC DIAGRAM



APPLICATIONS INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4−bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4−bit binary, 4−bit gray, excess−3, or excess−3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6−bit binary 1−of−64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

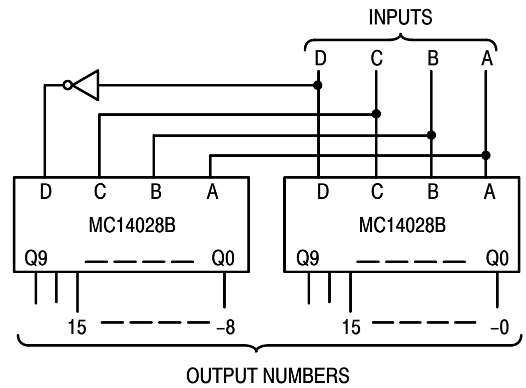


Figure 2. Code Conversion Circuit and Truth Table

Inputs				Output Numbers																Code and Redefined Output Numbers					
																				Hexadecimal			Decimal		
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4−Bit Binary	4−Bit Gray	Excess−3	Excess−3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

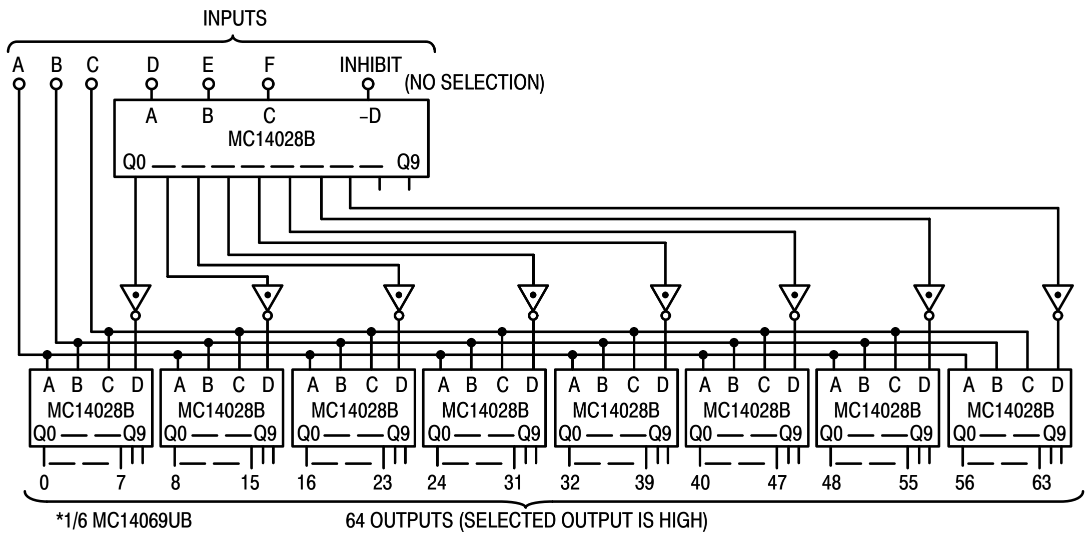


Figure 3. Six−Bit Binary 1−of−64 Decoder

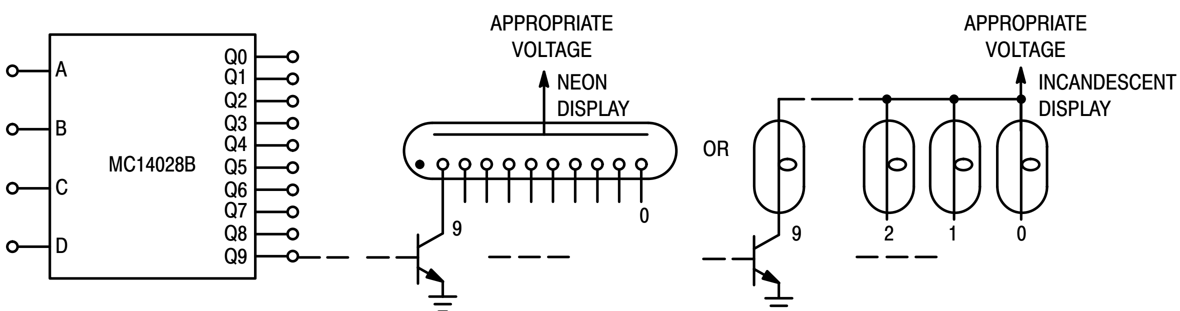


Figure 4. Decimal Digit Display Application

MC14029B

Binary/Decade Up/Down Counter

The MC14029B Binary/Decade up/down counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip−flop stages with a gating structure to provide toggle flip−flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge−Clocked Design — Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacement for CD4029B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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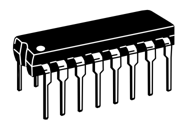
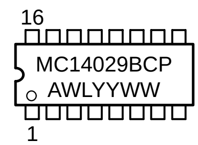
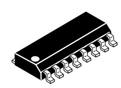
MARKING DIAGRAMS

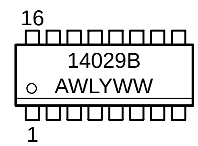


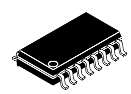
PDIP−16
P SUFFIX
CASE 648



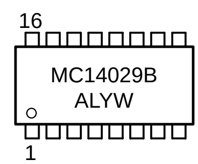


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



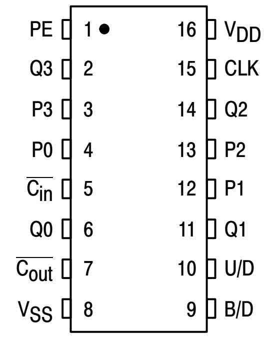
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14029BCP	PDIP−16	2000/Box
MC14029BD	SOIC−16	2400/Box
MC14029BDR2	SOIC−16	2500/Tape & Reel
MC14029BF	SOEIAJ−16	See Note 1.
MC14029BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don’t Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.20 µA/kHz) f + I_{DD}							
		15	I_T = (1.70 µA/kHz) f + I_{DD}							

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time Clk to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	90	180	
Clk to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	85	190	
$\overline{C_{in}}$ to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	—	175	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	—	50	120	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	—	50	100	
PE to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	235	470	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	80	160	
PE to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1. 7 ns/pF) C_L + 465 ns		5.0	—	320	640	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	—	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	—	105	210	
Clock Pulse Width	$t_{W(cl)}$	5.0 10 15	180 80 60	90 40 30	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	4.0 8.0 10	2.0 4.0 5.0	MHz
Preset Removal Time The Preset Signal must be low prior to a positive−going transition of the clock.	t_{rem}	5.0 10 15	160 80 60	80 40 30	— — —	ns
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5.0 10 1 5	— — —	— — —	15 5 4	µs
$\overline{\text{Carry}}$ In Setup Time	t_{su}	5.0 10 15	150 60 40	75 30 20	— — —	ns
Up/Down Setup Time		5.0 10 15	340 140 100	170 70 50	— — —	ns
Binary/Decade Setup Time		5.0 10 15	320 140 100	160 70 50	— — —	ns
Preset Enable Pulse Width	t_W	5.0 10 15	130 70 50	65 35 25	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

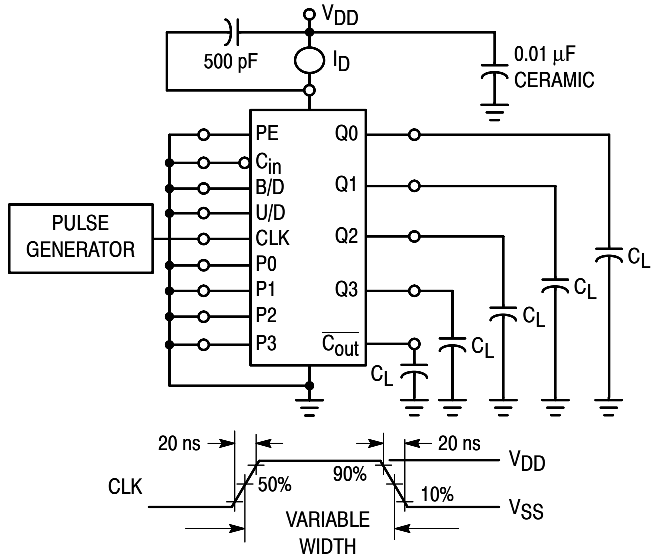


Figure 1. Power Dissipation Test Circuit and Waveform

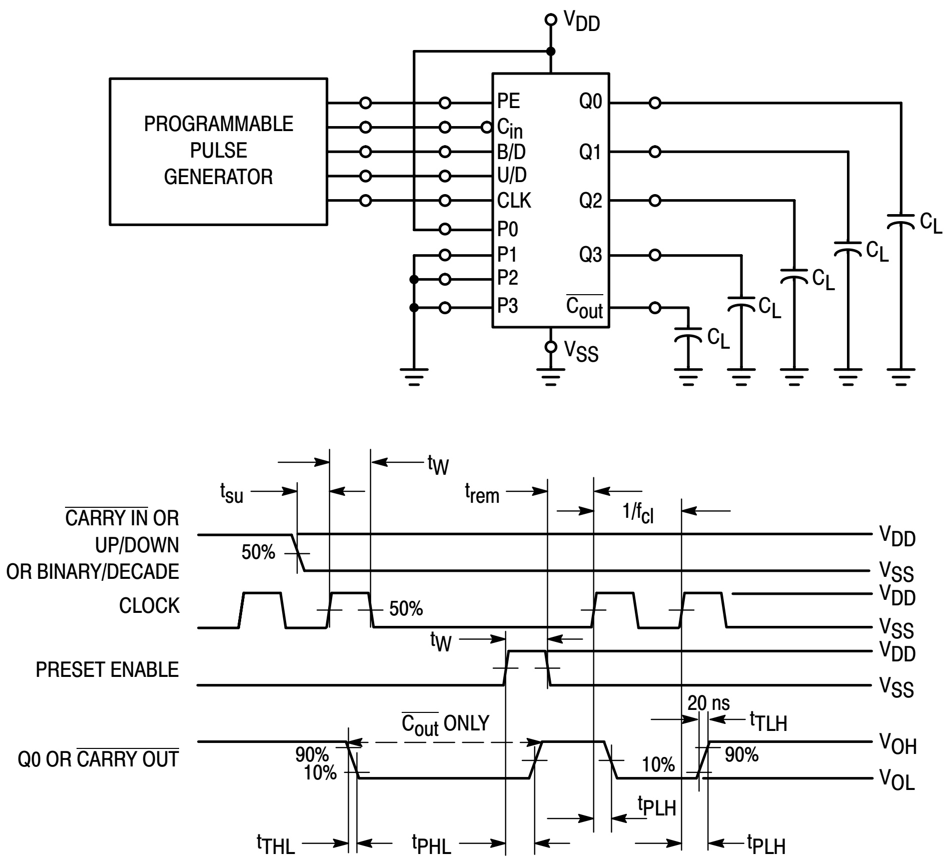
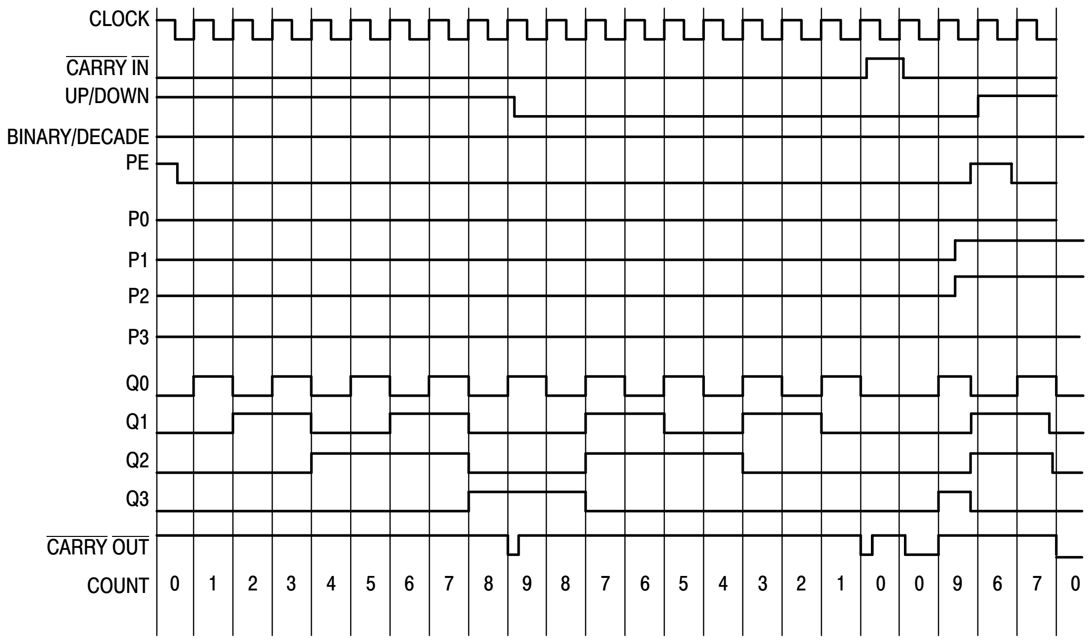
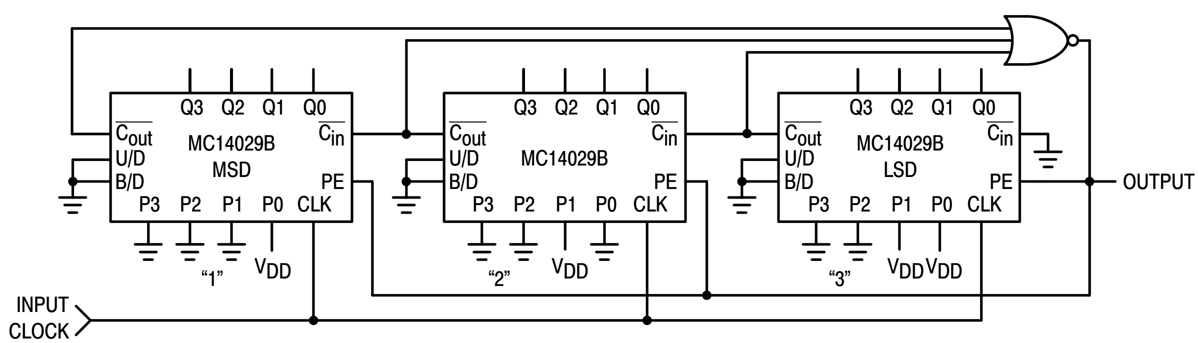
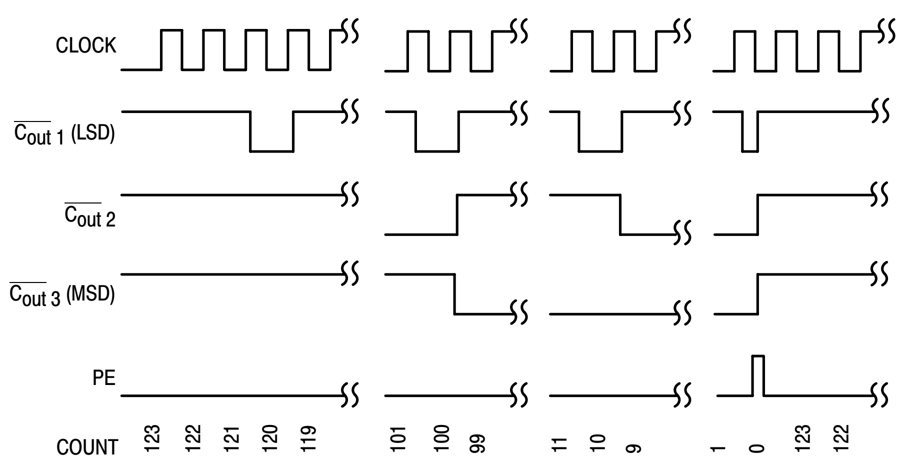


Figure 2. Switching Time Test Circuit and Waveforms

TIMING DIAGRAM



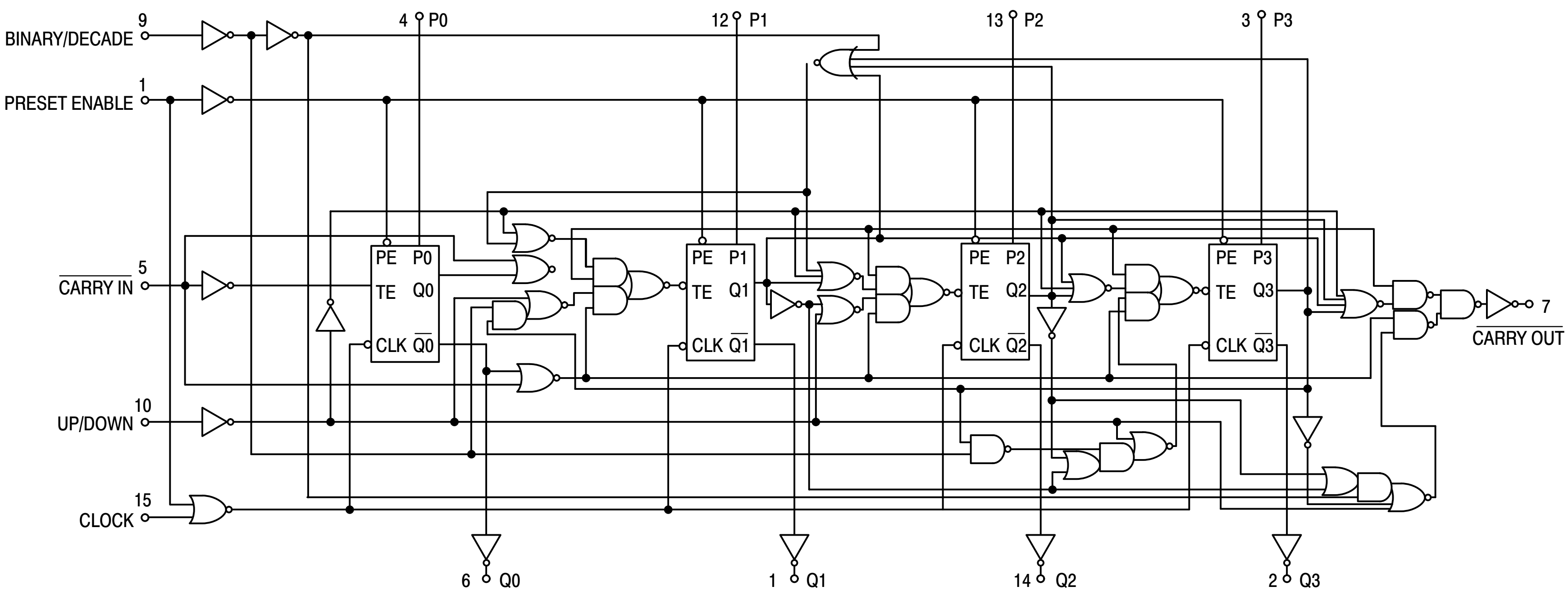




$^{*}t_W \cong 900$ ns @ V_{DD} = 5 V

Figure 3. Divide by N BCD Down Counter and Timing Diagram (Shown for N = 123)

LOGIC DIAGRAM



MC1403, B

Low Voltage Reference

A precision band−gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with D/A converters, up to 12 bits in accuracy, or as a reference for power supply applications.

- Output Voltage: 2.5 V ±25 mV
- Input Voltage Range: 4.5 V to 40 V
- Quiescent Current: 1.2 mA Typical
- Output Current: 10 mA
- Temperature Coefficient: 10 ppm/°C Typical
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8−Pin DIP, and 8−Pin SOIC Package

Typical Applications

- Voltage Reference for 8 to 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference
- Pb−Free Package is Available

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	−65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range MC1403B MC1403	T_A	 −40 to +85 0 to +70	 °C °C

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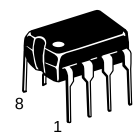
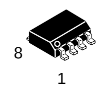
PRECISION LOW VOLTAGE REFERENCE

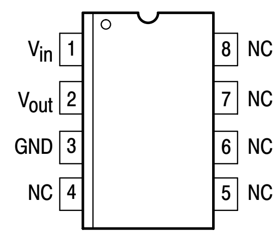


PDIP−8
P1 SUFFIX
CASE 626



SOIC−8
D SUFFIX
CASE 751

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 114 of this data sheet.

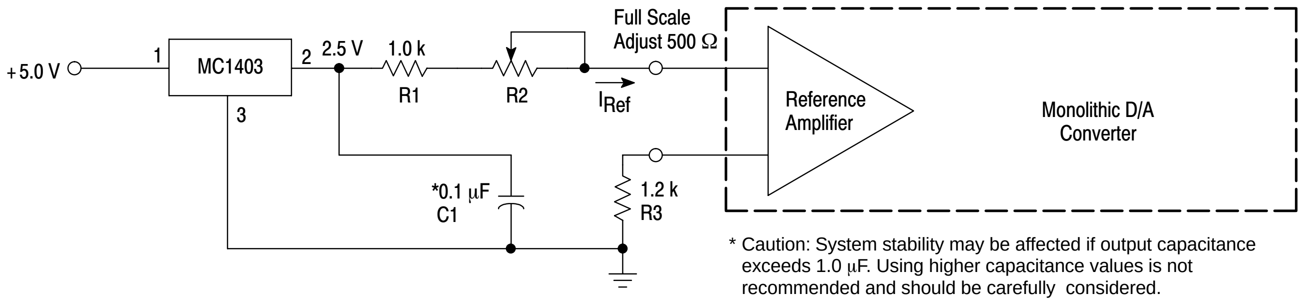


Figure 1. A Reference for Monolithic D/A Converters

Providing the Reference Current for ON Semiconductor Monolithic D/A Converters

The MC1403 makes an ideal reference for many monolithic D/A converters, requiring a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full−scale adjust on the D/A converter.

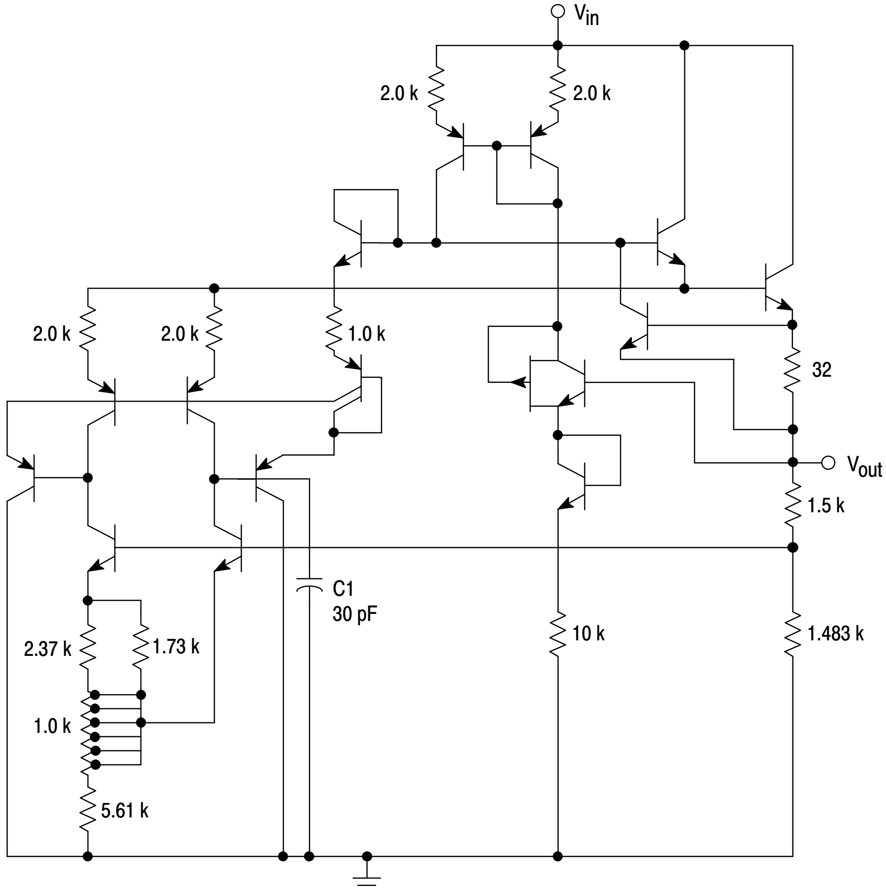
The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_{out}	2.475	2.5	2.525	V
Temperature Coefficient of Output Voltage* MC1403	$\Delta V_O/\Delta T$	−	10	40	ppm/°C
Output Voltage Change* (Over specified temperature range) MC1403 0 to +70°C MC1403B −40 to +85°C	ΔV_O	 − −	 − −	 7.0 12.5	mV
Line Regulation (I_O = 0 mA) (15 V ≤ V_I ≤ 40 V) (4.5 V ≤ V_I ≤ 15 V)	Reg_{line}	 − −	 1.2 0.6	 4.5 3.0	mV
Load Regulation (0 mA < I_O < 10 mA)	Reg_{load}	−	−	10	mV
Quiescent Current (I_O = 0 mA)	I_Q	−	1.2	1.5	mA

*Guaranteed but not tested.



This device contains 15 active transistors.

Figure 2. MC1403, B Schematic

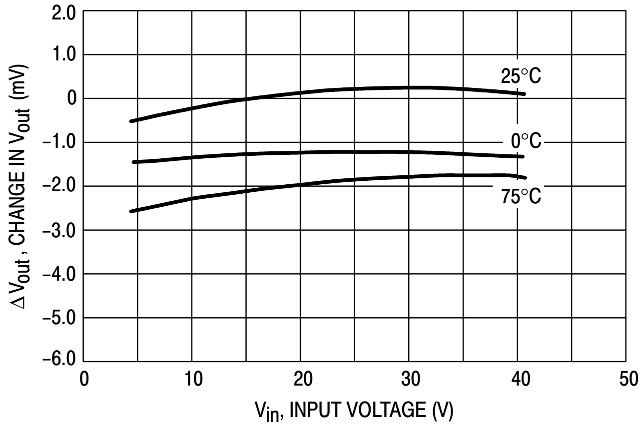


Figure 3. Typical Change in V_{out} versus V_{in}
(Normalized to V_{in} = 15 V @ T_C = 25°C)

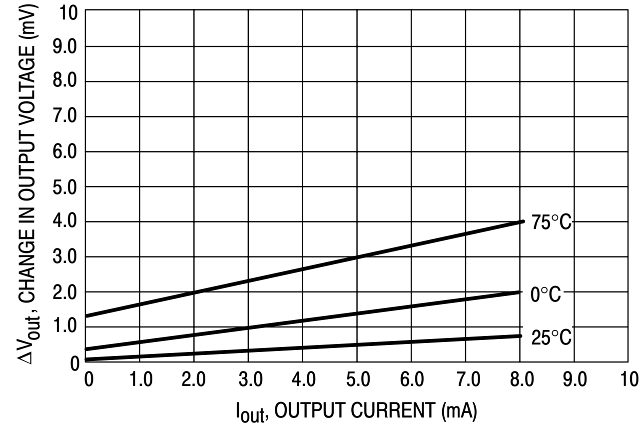


Figure 4. Change in Output Voltage versus Load Current
(Normalized to V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

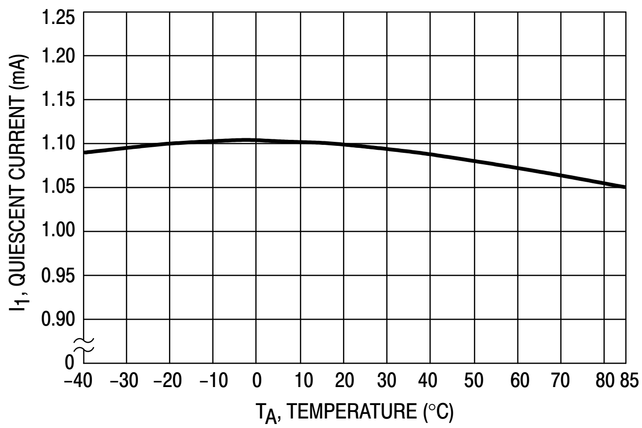


Figure 5. Quiescent Current versus Temperature
(V_{in} = 15 V, I_{out} = 0 mA)

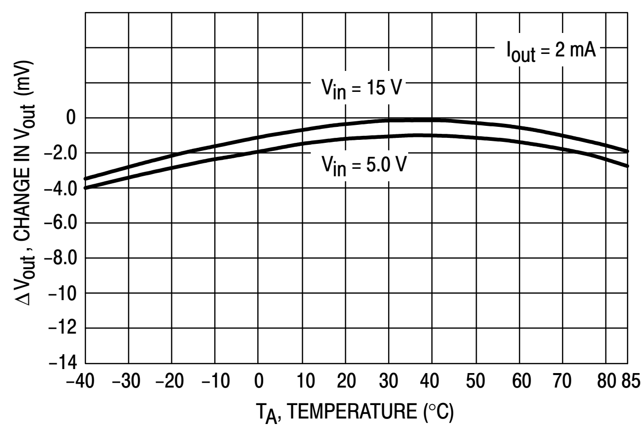


Figure 6. Change in V_{out} versus Temperature
(Normalized to V_{out} @ V_{in} = 15 V)

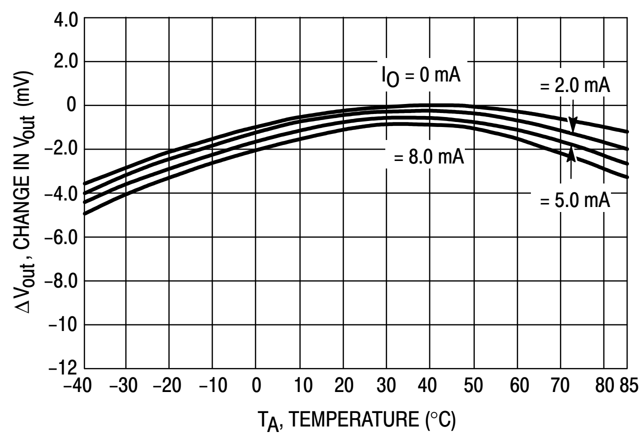


Figure 7. Change in V_{out} versus Temperature
(Normalized to T_A = 25°C, V_{in} = 15 V, I_{out} = 0 mA)

3−1/2−Digit Voltmeter − Common Anode Displays, Flashing Overrange

An example of a 3−1/2−digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2.0 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one−half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip−flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS−A12 Darlington transistors operating in an emitter−follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 Ω in Figure 8.

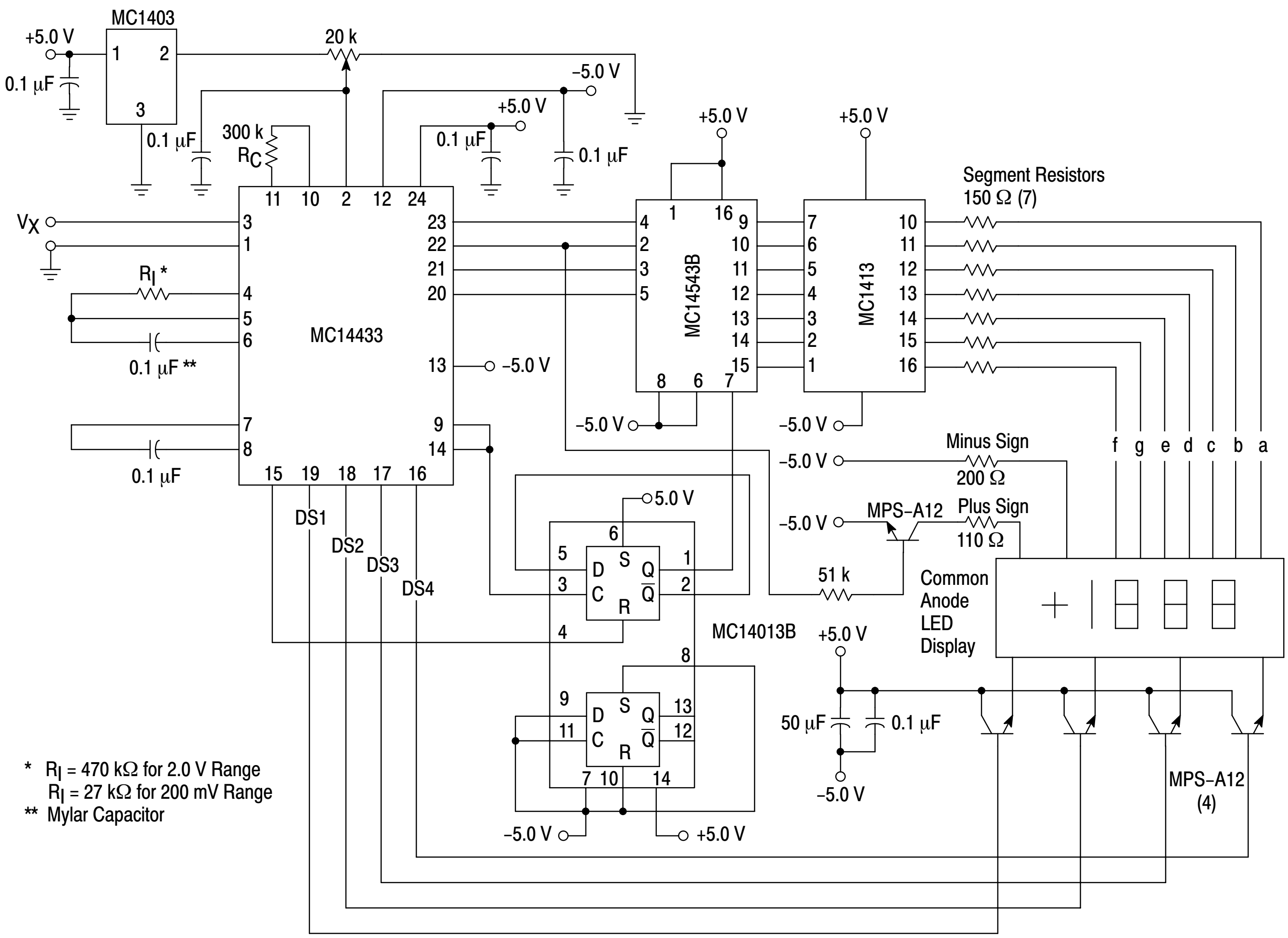


Figure 8. 3−1/2−Digit Voltmeter

ORDERING INFORMATION

Device	Package	Operating Temperature Range	Shipping†
MC1403D	SOIC−8	T_A = 0° to +70°C	98 Units/Rail
MC1403DR2			2500 Tape/Reel
MC1403P1	PDIP−8		1000 Units/Rail
MC1403P1G	PDIP−8 (Pb−Free)		1000 Units/Tubes
MC1403BD	SOIC−8	T_A = −40° to +85°C	98 Units/Rail
MC1403BDR2			2500 Tape/Reel
MC1403BP1	PDIP−8−8		1000 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14040B

12-Bit Binary Counter

The MC14040B 12−stage binary counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−driving circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin−for−Pin Replacement for CD4040B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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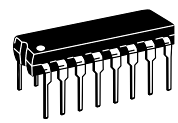
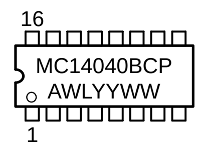
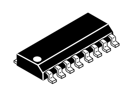
MARKING DIAGRAMS

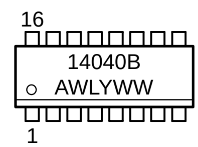


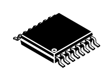
PDIP−16
P SUFFIX
CASE 648



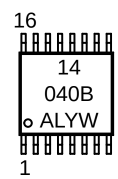


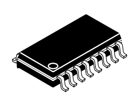
SOIC−16
D SUFFIX
CASE 751B



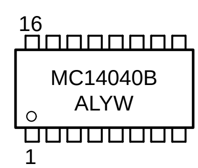


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



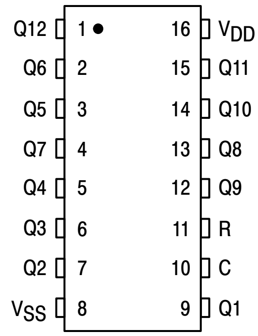
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14040BCP	PDIP−16	2000/Box
MC14040BD	SOIC−16	2400/Box
MC14040BDR2	SOIC−16	2500/Tape & Reel
MC14040BDT	TSSOP−16	96/Rail
MC14040BF	SOEIAJ−16	See Note 1.
MC14040BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

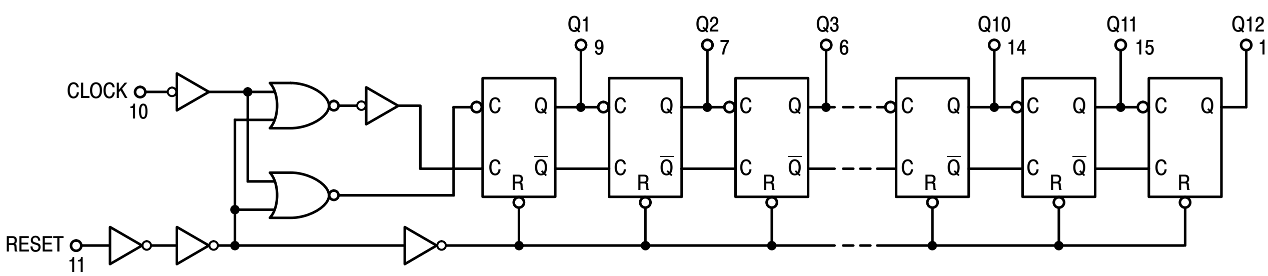


TRUTH TABLE

Clock	Reset	Output State
↑	0	No Change
↓	0	Advance to next state
X	1	All Outputs are low

X = Don’t Care

LOGIC DIAGRAM



Q4 = PIN 5
Q5 = PIN 3
Q6 = PIN 2

Q7 = PIN 4
Q8 = PIN 13
Q9 = PIN 12

V_{DD} = PIN 16
V_{SS} = PIN 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.42 µA/kHz) f + I_{DD} I_T = (0.85 µA/kHz) f + I_{DD} I_T = (1.43 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time Clock to Q1	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	—	260	520	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	—	115	230	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	—	80	160	
Clock to Q12						ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns		5.0	—	1625	3250	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns		10	—	720	1440	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 ns		15	—	500	1000	
Propagation Delay Time Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 485 ns		5.0	—	370	740	
t_{PHL} = (0.86 ns/pF) C_L + 182 ns		10	—	155	310	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	—	115	230	
Clock Pulse Width	t_{WH}	5.0 10 15	385 150 115	140 55 38	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15		No Limit		ns
Reset Pulse Width	t_{WH}	5.0 10 15	960 360 270	320 120 80	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	130 50 30	65 25 15	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

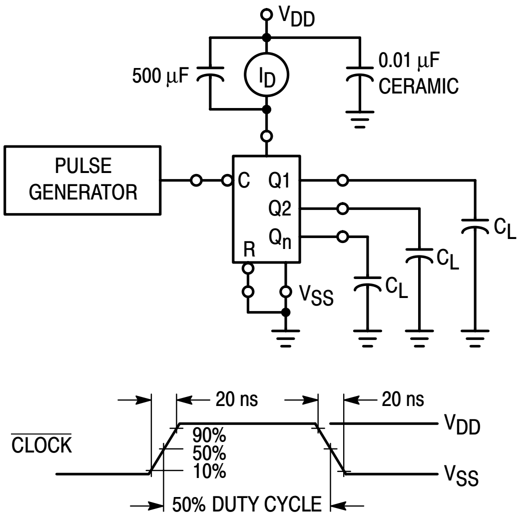


Figure 1. Power Dissipation Test Circuit and Waveform

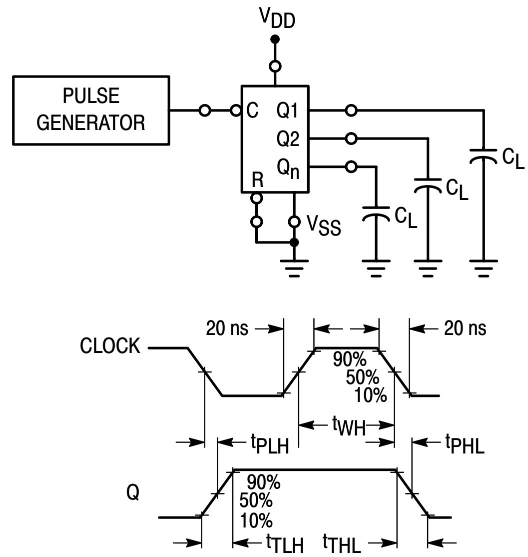


Figure 2. Switching Time Test Circuit and Waveforms

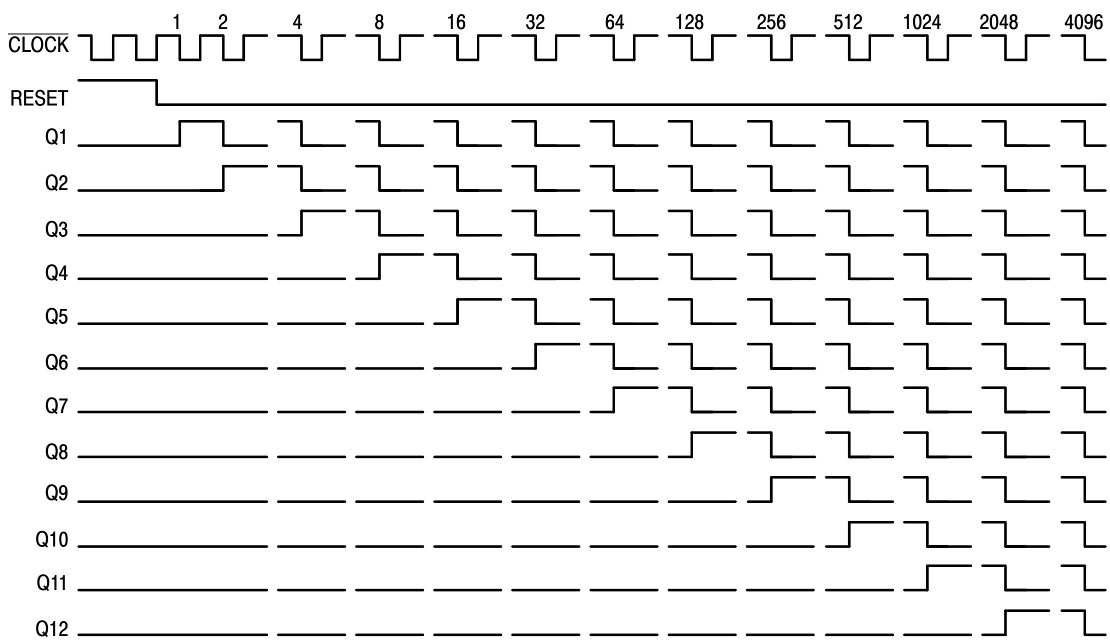


Figure 3. Timing Diagram

APPLICATIONS INFORMATION

TIME−BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

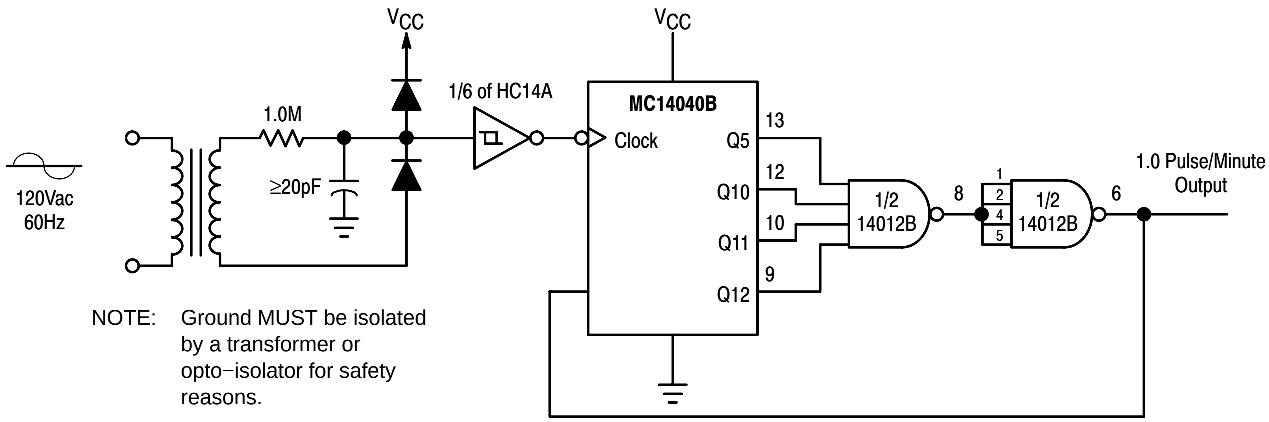


Figure 4. Time−Base Generator

MC14042B

Quad Transparent Latch

The MC14042B Quad Transparent Latch is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic “0” state, data is transferred during the low clock level, and when the polarity input is in the logic “1” state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 1 8 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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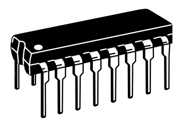
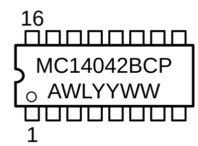
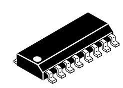
MARKING DIAGRAMS

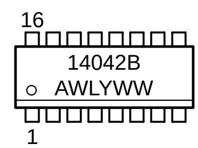


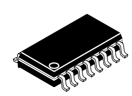
PDIP−16
P SUFFIX
CASE 648



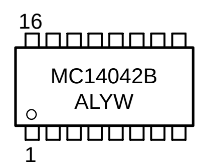


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



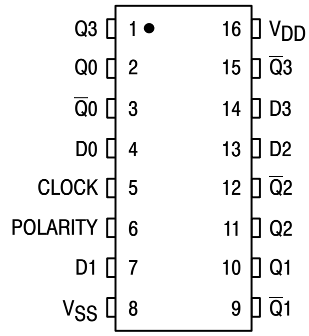
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14042BCP	PDIP−16	2000/Box
MC14042BD	SOIC−16	2400/Box
MC14042BDR2	SOIC−16	2500/Tape & Reel
MC14042BF	SOEIAJ−16	See Note 1.
MC14042BFEL	SOEIAJ−16	See Note 1.
MC14042BFR1	SOEIAJ−16	See Note 1.
MC14042BFR2	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

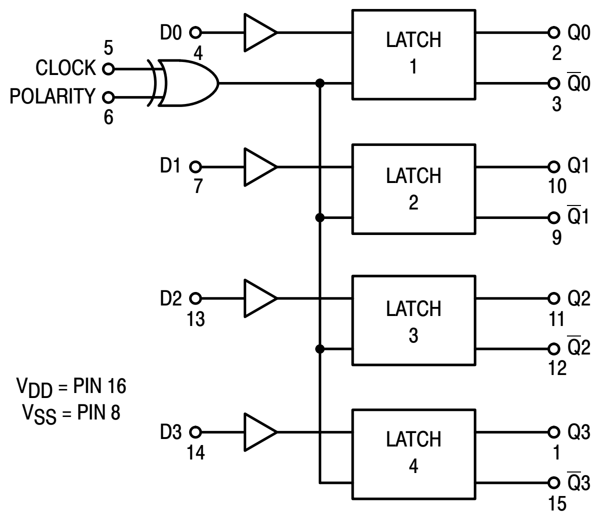
PIN ASSIGNMENT



TRUTH TABLE

Clock	Polarity	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ [4.]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	µAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs all buffers switching)	I_T	5.0 10 15	I_T = (1.0 µA/kHz) f + I_{DD} I_T = (2.0 µA/kHz) f + I_{DD} I_T = (3.0 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time, D to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 220 90 60	 440 180 120	no
Propagation Delay Time, Clock to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 220 90 60	 440 180 120	ns
Clock Pulse Width	t_{WH}	 5.0 10 15	 300 100 80	 150 50 40	 — — —	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 — — —	 15 5.0 4.0	µs
Hold Time	t_h	 5.0 10 15	 100 50 40	 50 25 20	 — — —	ns
Setup Time	t_{su}	 5.0 10 15	 50 30 25	 0 0 0	 — — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

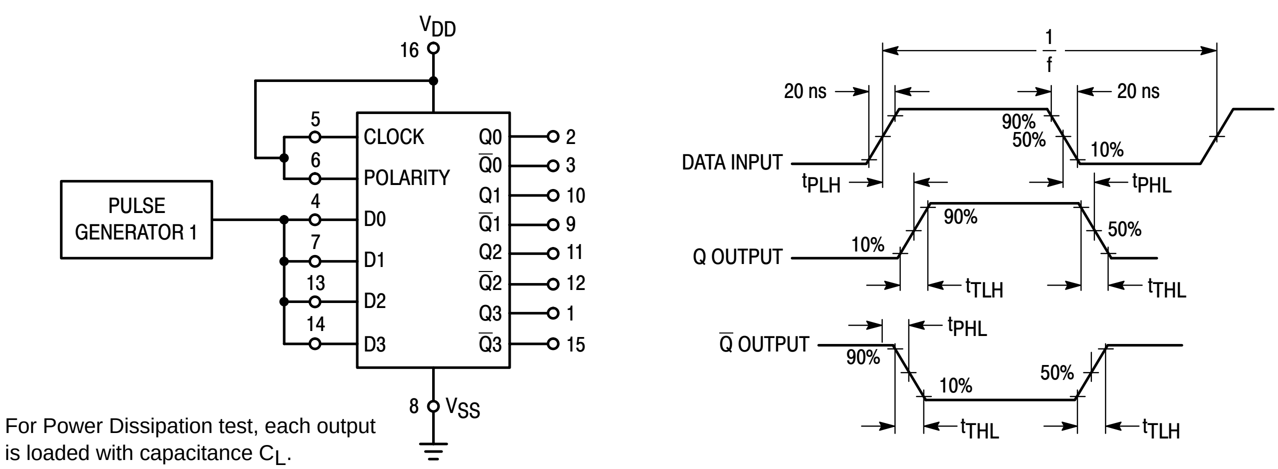
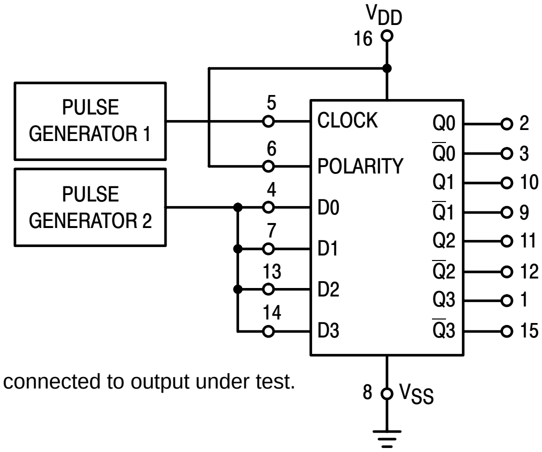
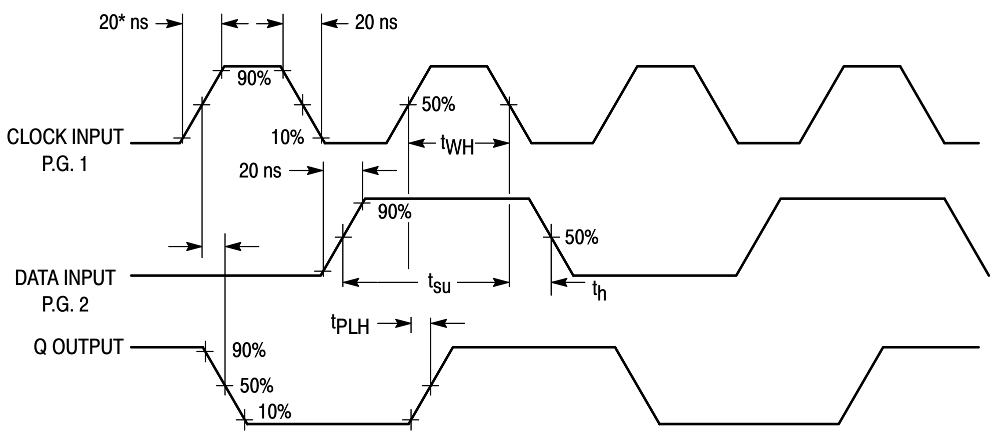


Figure 1. AC and Power Dissipation Test Circuit and Timing Diagram (Data to Output)



NOTE: C_L connected to output under test.



*Input clock rise time is 20 ns except for maximum rise time test.

Figure 2. AC Test Circuit and Timing Diagram (Clock to Output)

MC14043B, MC14044B

CMOS MSI

Quad R−S Latches

The MC14043B and MC14044B quad R−S latches are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three−state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Double Diode Input Protection
- Three−State Outputs with Common Enable
- Outputs Capable of Driving Two Low−power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

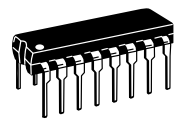
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

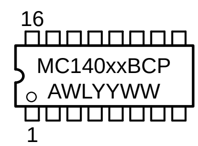
ON Semiconductor

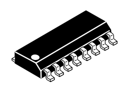
http://onsemi.com

MARKING DIAGRAMS

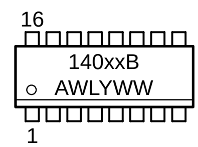


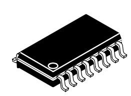
PDIP−16
P SUFFIX
CASE 648



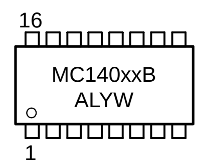


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



xx	=	Specific Device Code
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

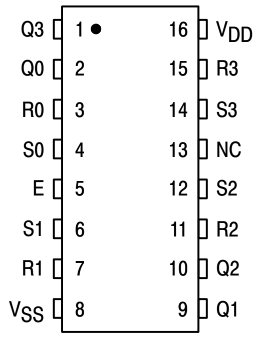
ORDERING INFORMATION

Device	Package	Shipping
MC14043BCP	PDIP−16	2000/Box
MC14043BD	SOIC−16	2400/Box
MC14043BDR2	SOIC−16	2500/Tape & Reel
MC14043BF	SOEIAJ−16	See Note 1.
MC14043BFEL	SOEIAJ−16	See Note 1.
MC14044BCP	PDIP−16	2000/Box
MC14044BD	SOIC−16	2400/Box
MC14044BDR2	SOIC−16	2500/Tape & Reel

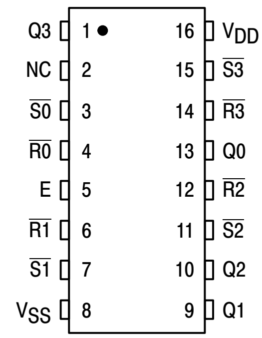
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

MC14043B

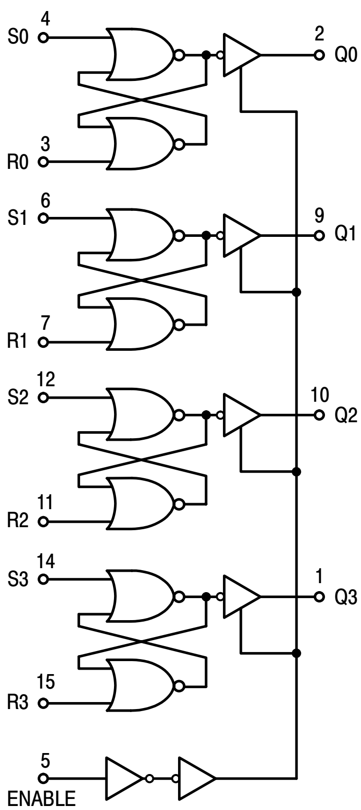


MC14044B



NC = NO CONNECTION

MC14043B



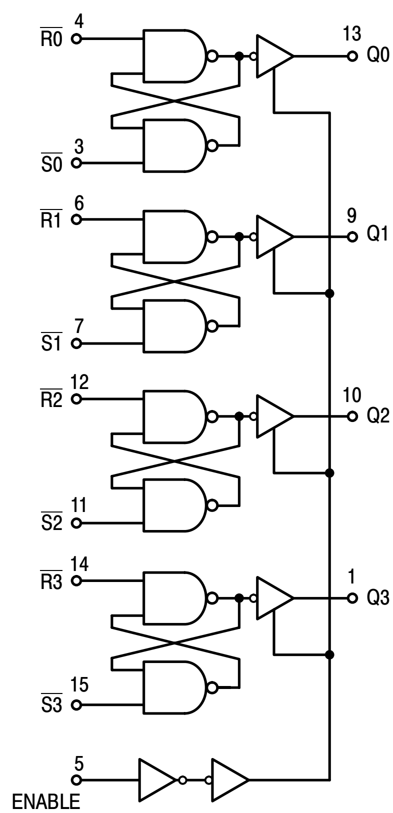
V_{DD} = PIN 16
V_{SS} = PIN 8
NC = PIN 13

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care

MC14044B



V_{DD} = PIN 16
V_{SS} = PIN 8
NC = PIN 2

TRUTH TABLE

$\overline{S}$	$\overline{R}$	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs all buffers switching)		I_T	5.0 10 15	I_T = (0.58 µA/kHz) f + I_{DD} I_T = (1.15 µA/kHz) f + I_{DD} I_T = (1.73 µA/kHz) f + I_{DD}							µAdc
Three−State Output Leakage Current		I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

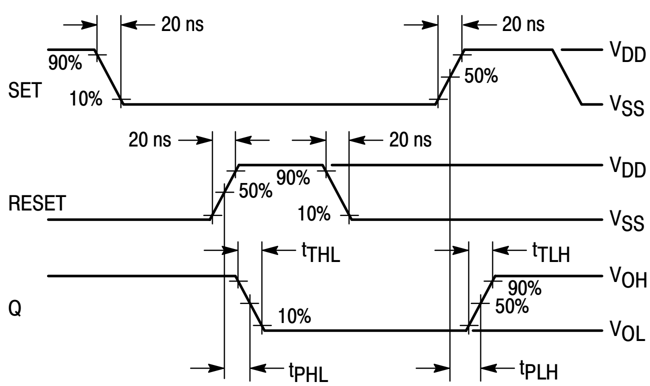
SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 32.5 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.90 ns/pF) C_L + 130 ns		5.0	—	175	350	
t_{PLH} = (0.36 ns/pF) C_L + 57 ns		10	—	75	175	
t_{PLH} = (0.26 ns/pF) C_L + 47 ns		15	—	60	120	
t_{PHL} = (0.90 ns/pF) C_L + 130 ns	t_{PHL}	5.0	—	175	350	ns
t_{PHL} = (0.90 ns/pF) C_L + 57 ns		10	—	75	175	
t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	—	60	120	
Set, $\overline{\text{Set}}$ Pulse Width	t_W	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Reset, $\overline{\text{Reset}}$ Pulse Width	t_W	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Three−State Enable/Disable Delay	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5.0	—	150	300	ns
		10	—	80	160	
		15	—	55	110	

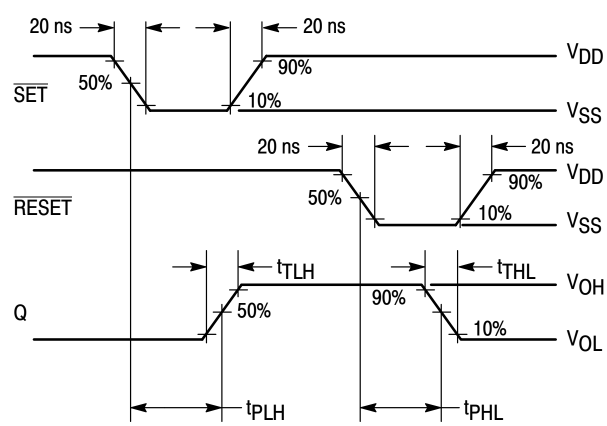
7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC WAVEFORMS

MC14043B



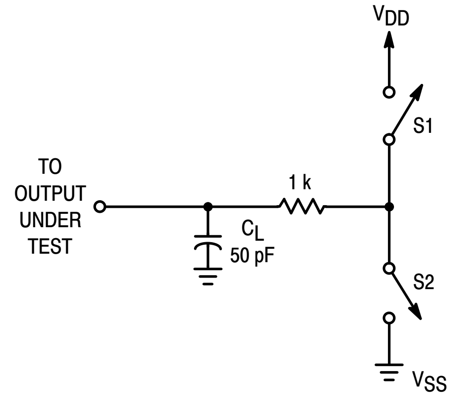
MC14044B

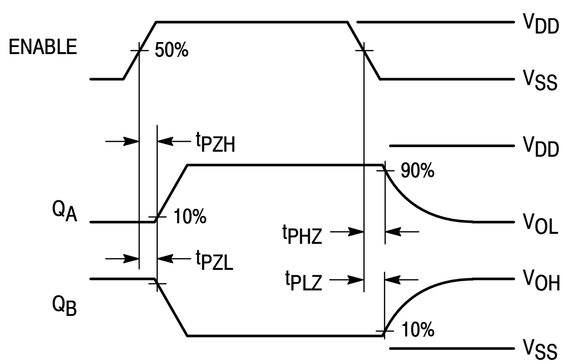


THREE−STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3−State Tests

Test	Enable	S1	S2	Q	MC14043B S	MC14043B R	MC14044B $\overline{S}$	MC14044B $\overline{R}$
t_{PZH}	↑	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PZL}	↑	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}
t_{PHZ}	↓	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PLZ}	↓	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}





MC14046B

Phase Locked Loop

The MC14046B phase locked loop contains two phase comparators, a voltage−controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self−bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, $PC2_{out}$ and LD, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source−follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage−to−frequency conversion and motor speed control.

- Buffered Outputs Compatible with MHTL and Low−Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin−for−Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (All Inputs)	−0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

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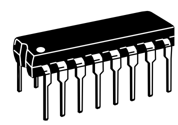
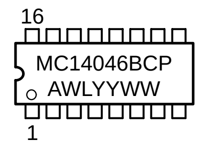
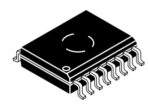
MARKING DIAGRAMS

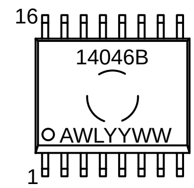


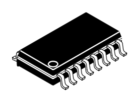
PDIP−16
P SUFFIX
CASE 648



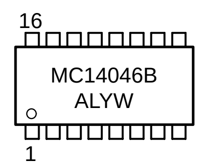


SO−16
DW SUFFIX
CASE 751G





EIAJ SO−16
F SUFFIX
CASE 966



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

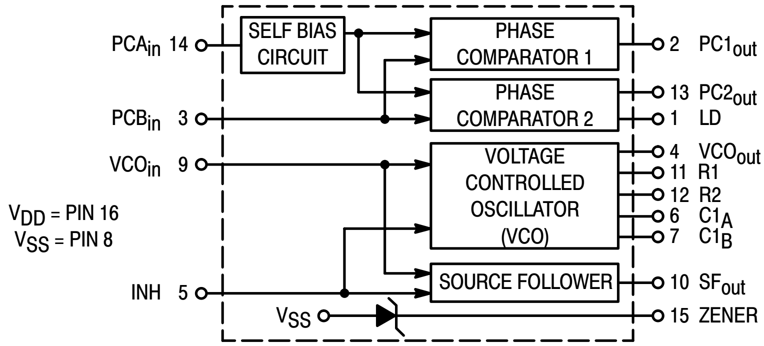
Device	Package	Shipping
MC14046BCP	PDIP−16	2000/Box
MC14046BDW	SO−16	2350/Box
MC14046BDWR2	SO−16	1000/Tape & Reel
MC14046BF	EIAJ SO−16	Refer to Note 1.
MC14046BFEL	EIAJ SO−16	Refer to Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

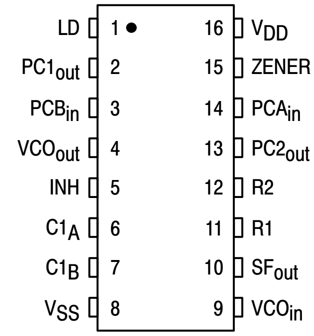
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	“0” Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
$V_{in} = V_{DD}$ or 0			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
	“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
$V_{in} = 0$ or V_{DD}			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (4.)	“0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc)	“1” Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)			10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)			15	11	—	11	8.25	—	11	—	
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	– 1.2	—	– 1.0	– 1.7	—	– 0.7	—	
(V_{OH} = 4.6 Vdc)			5.0	– 0.25	—	– 0.2	– 0.36	—	– 0.14	—	
(V_{OH} = 9.5 Vdc)			10	– 0.62	—	– 0.5	– 0.9	—	– 0.35	—	
(V_{OH} = 13.5 Vdc)			15	– 1.8	—	– 1.5	– 3.5	—	– 1.1	—	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current		I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
(Per Package) Inh = $PCA_{in} = V_{DD}$,			10	—	10	—	0.010	10	—	300	
Zener = VCO_{in} = 0 V, $PCB_{in} = V_{DD}$			15	—	20	—	0.015	20	—	600	
or 0 V, I_{out} = 0 µA											
Total Supply Current (5.)		I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							mAdc
(Inh = “0”, f_o = 10 kHz, C_L = 50 pF,			10	I_T = (2.91 µA/kHz) f + I_{DD}							
R1 = 1.0 MΩ, R2 = ∞ R_{SF} = ∞,			15	I_T = (4.37 µA/kHz) f + I_{DD}							
and 50% Duty Cycle)											

4. Noise immunity specified for worst−case input combination.
   Noise Margin for both “1” and “0” level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
   2.0 Vdc min @ V_{DD} = 10 Vdc
   2.5 Vdc min @ V_{DD} = 15 Vdc
5. To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD}\left(\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right)^{3/4} + 1.6 \times \left(\frac{VCO_{in} - 1.65}{R_{SF}}\right)^{3/4} + 1 \times 10^{-3}\,(C_L + 9)\,V_{DD}\,f +$$

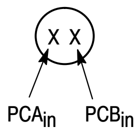
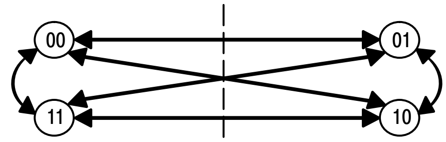
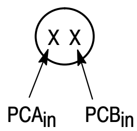
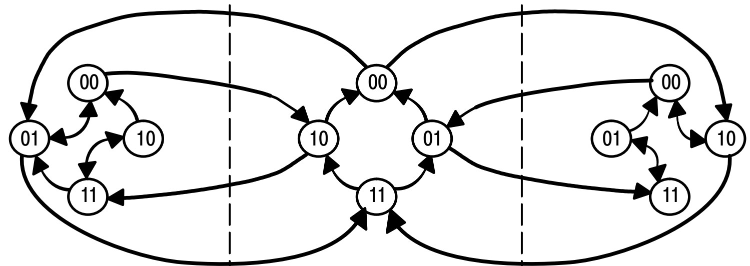
$$1 \times 10^{-1}\,V_{DD}^2\left(\frac{100\%\text{ Duty Cycle of }PCA_{in}}{100}\right) + I_Q$$

where: I_T in µA, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in kHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Minimum Device	Typical	Maximum Device	Units
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	350	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	150	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	110	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	175	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	75	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	37	55	
PHASE COMPARATORS 1 and 2						
Input Resistance — PCA_{in}	R_{in}	5.0	1.0	2.0	—	MΩ
		10	0.2	0.4	—	
		15	0.1	0.2	—	
— PCB_{in}	R_{in}	15	150	1500	—	MΩ
Minimum Input Sensitivity	V_{in}	5.0	—	200	300	mV p–p
AC Coupled — PCA_{in}		10	—	400	600	
C series = 1000 pF, f = 50 kHz		15	—	700	1050	
DC Coupled — PCA_{in}, PCB_{in}	—	5 to 15	See Noise Immunity			
VOLTAGE CONTROLLED OSCILLATOR (VCO)						
Maximum Frequency	f_{max}	5.0	0.5	0.7	—	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF		10	1.0	1.4	—	
R1 = 5.0 kΩ, and R2 = ∞)		15	1.4	1.9	—	
Temperature — Frequency Stability	—	5.0	—	0.12	—	%/°C
(R2 = ∞)		10	—	0.04	—	
		15	—	0.015	—	
Linearity (R2 = ∞)	—					%
(VCO_{in} = 2.5 V ± 0.3 V, R1 > 10 kΩ)		5.0	—	1.0	—	
(VCO_{in} = 5.0 V ± 2.5 V, R1 > 400 kΩ)		10	—	1.0	—	
(VCO_{in} = 7.5 V ± 5.0 V, R1 ≥ 1000 kΩ)		15	—	1.0	—	
Output Duty Cycle	—	5 to 15	—	50	—	%
Input Resistance — VCO_{in}	R_{in}	15	150	1500	—	MΩ
SOURCE−FOLLOWER						
Offset Voltage	—	5.0	—	1.65	2.2	V
(VCO_{in} minus SF_{out}, RSF > 500 kΩ)		10	—	1.65	2.2	
		15	—	1.65	2.2	
Linearity	—					%
(VCO_{in} = 2.5 V ± 0.3 V, R_{SF} > 50 kΩ)		5.0	—	0.1	—	
(VCO_{in} = 5.0 V ± 2.5 V, R_{SF} > 50 kΩ)		10	—	0.6	—	
(VCO_{in} = 7.5 V ± 5.0 V, R_{SF} > 50 kΩ)		15	—	0.8	—	
ZENER DIODE						
Zener Voltage (I_Z = 50 μA)	V_Z	—	6.7	7.0	7.3	V
Dynamic Resistance (I_Z = 1.0 mA)	R_Z	—	—	100	—	Ω

6. The formula given is for the typical characteristics only.

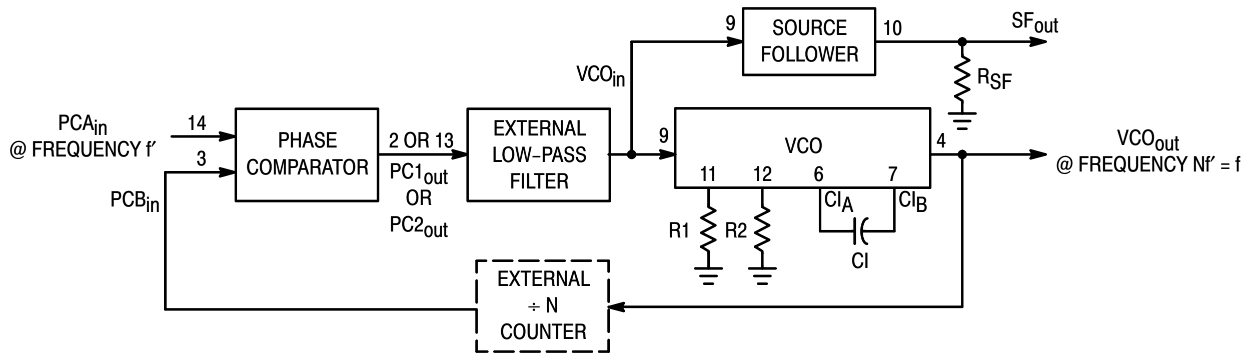
<table>
<tr><td colspan="4">PHASE COMPARATOR 1</td></tr>
<tr><td>Input Stage
</td><td colspan="3"></td></td></tr>
<tr><td>PC1out</td><td>0</td><td colspan="2">1</td></tr>
<tr><td></td><td colspan="3">PHASE COMPARATOR 2</td></tr>
<tr><td>Input Stage
</td><td colspan="3"></td></tr>
<tr><td>PC2out</td><td>0</td><td>3−State
Output Disconnected</td><td>1</td></tr>
<tr><td>LD (Lock Detect)</td><td>0</td><td>1</td><td>0</td></tr>
</table>

Refer to Waveforms in Figure 3.

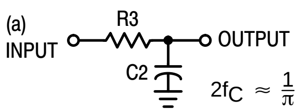
Figure 1. Phase Comparators State Diagrams

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA_{in}.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA_{in} and PCB_{in}.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$)	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low−pass filter characteristics (see Figure 3). $f_C \le f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO_{out}, when VCO_{in} = 1/2 V_{DD}	
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.	$f_{min} = \frac{1}{R_2(C_1 + 32\text{ pF})}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32\text{ pF})} + f_{min}$ (V_{CO} input = V_{DD}) Where: $10K \le R_1 \le 1$ M $10K \le R_2 \le 1$ M $100pF \le C_1 \le .01\ \mu F$	

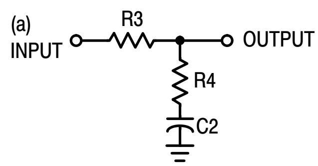
Figure 2. Design Information



Typical Low−Pass Filters



$$2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{R3\,C2}}$$



Typically:

$$R_4\,C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi\,\Delta f}$$

$$(R_3 + 3,000\Omega)\,C_2 = \frac{100N\Delta f}{f_{max}{}^2} - R_4\,C_2$$

$$\Delta f = f_{max} - f_{min}$$

NOTE: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor C_C is then placed from the midpoint to ground. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_n. In Figure B, the ratio of R3 to R4 sets the damping, R4 ≅ (0.1)(R3) for optimum results.

Definitions: N = Total division ratio in feedback loop

$K\phi = V_{DD}/\pi$ for Phase Comparator 1

$K\phi = V_{DD}/4\pi$ for Phase Comparator 2

$$K_{VCO} = \frac{2\pi\,\Delta f_{VCO}}{V_{DD} - 2\,V}$$

for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input)

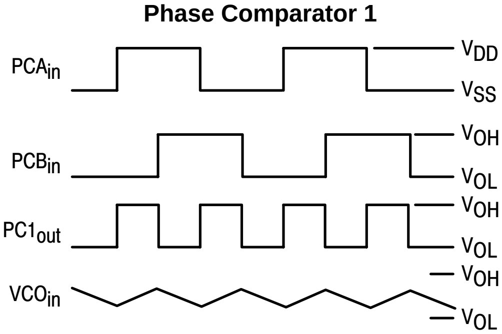
$\zeta \cong 0.707$

LOW−PASS FILTER

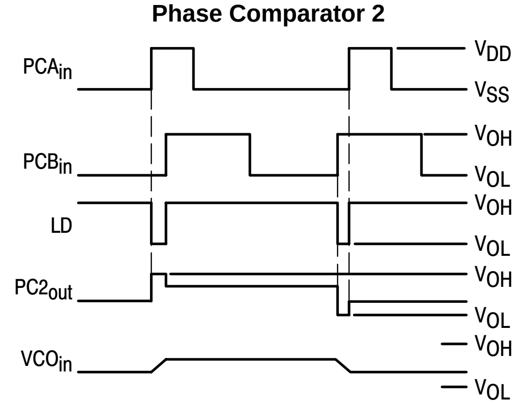
Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{NR_3C_2}}$	$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi K_{VCO}}$	$\zeta = 0.5\,\omega_n\,(R_3C_2 + \frac{N}{K\phi K_{VCO}})$
$F(s) = \frac{1}{R_3C_2S + 1}$	$F(s) = \frac{R_3C_2S + 1}{S(R_3C_2 + R_4C_2) + 1}$

Waveforms

Phase Comparator 1



Phase Comparator 2



Note: for further information, see:
(1) F. Gardner, “Phase−Lock Techniques”, John Wiley and Son, New York, 1966.
(2) G. S. Moschytz, “Miniature RC Filters Using Phase−Locked Loop”, BSTJ, May, 1965.
(3) Garth Nash, “Phase−Lock Loop Design Fundamentals”, AN−535, Motorola Inc.
(4) A. B. Przedpelski, “Phase−Locked Loop Design Articles”, AR254, reprinted by Motorola Inc.

Figure 3. General Phase−Locked Loop Connections and Waveforms

MC14049B, MC14050B

Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, V_{DD}.

The input−signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS−to−TTL/DTL converter (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High−to−Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V_{IN} can exceed V_{DD}
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	±45	mA
P_D	Power Dissipation, per Package (Note 3.) (Plastic) (SOIC)	825 740	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high−impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq$ 18 V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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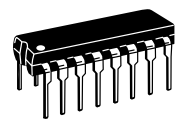
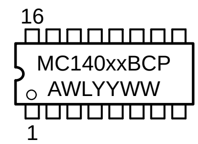
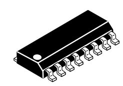
MARKING DIAGRAMS

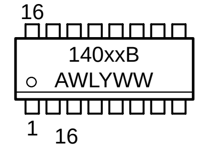


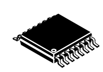
PDIP−16
P SUFFIX
CASE 648



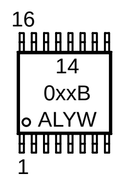


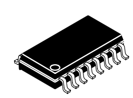
SOIC−16
D SUFFIX
CASE 751B



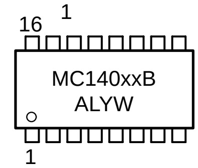


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



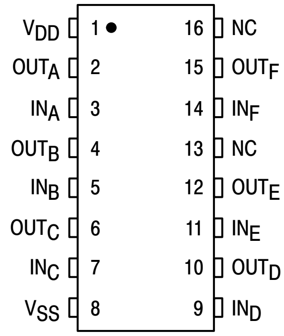
xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

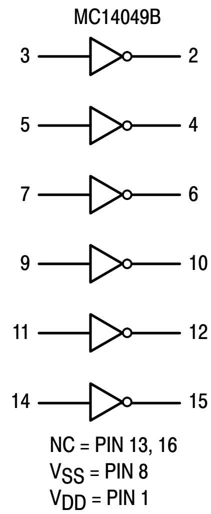
Device	Package	Shipping
MC14049BCP	PDIP−16	2000/Box
MC14049BD	SOIC−16	2400/Box
MC14049BDR2	SOIC−16	2500/Tape & Reel
MC14049BF	SOEIAJ−16	See Note 1.
MC14050BCP	PDIP−16	2000/Box
MC14050BD	SOIC−16	2400/Box
MC14050BDR2	SOIC−16	2500/Tape & Reel
MC14050BDTEL	TSSOP−16	2000/Tape & Reel
MC14050BF	SOEIAJ−16	See Note 1.
MC14050BFEL	SOEIAJ−16	See Note 1.

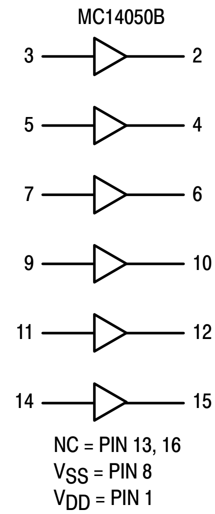
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



LOGIC DIAGRAM





ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	+ 25°C Min	+ 25°C Typ (4.)	+ 25°C Max	+ 125°C Min	+ 125°C Max	Unit
Output Voltage "0" Level, $V_{in} = V_{DD}$	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level, $V_{in} = 0$	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.6	—	– 1.25	– 2.5	—	– 1.0	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.30	– 2.6	—	– 1.0	—	
(V_{OH} = 13.5 Vdc)		15	– 4.7	—	– 3.75	– 10	—	– 3.0	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
(V_{OL} = 0.5 Vdc)		10	10	—	8.0	16	—	6.6	—	
(V_{OL} = 1.5 Vdc)		15	30	—	24	40		19	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	µAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, per package) (C_L = 50 pF on all outputs, all buffers switching	I_T	5.0	I_T = (1.8 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.5 µA/kHz) f + I_{DD}							
		15	I_T = (5.3 µA/kHz) f + I_{DD}							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at + 25°C
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

Where: I_T is in µA (per Package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency and k = 0.002.

AC SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = + 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [8.]	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.7 ns/pF) C_L + 65 ns		5.0	—	100	160	
t_{TLH} = (0.25 ns/pF) C_L + 37.5 ns		10	—	50	80	
t_{TLH} = (0.2 ns/pF) C_L + 30 ns		15	—	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.2 ns/pF) C_L + 30 ns		5.0	—	40	60	
t_{THL} = (0.06 ns/pF) C_L + 17 ns		10	—	20	40	
t_{THL} = (0.04 ns/pF) C_L + 13 ns		15	—	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns		5.0	—	80	140	
t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns		10	—	40	80	
t_{PLH} = (0.06 ns/pF) C_L + 27 ns		15	—	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 30 ns		5.0	—	40	80	
t_{PHL} = (0.1 ns/pF) C_L + 15 ns		10	—	20	40	
t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns		15	—	15	30	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

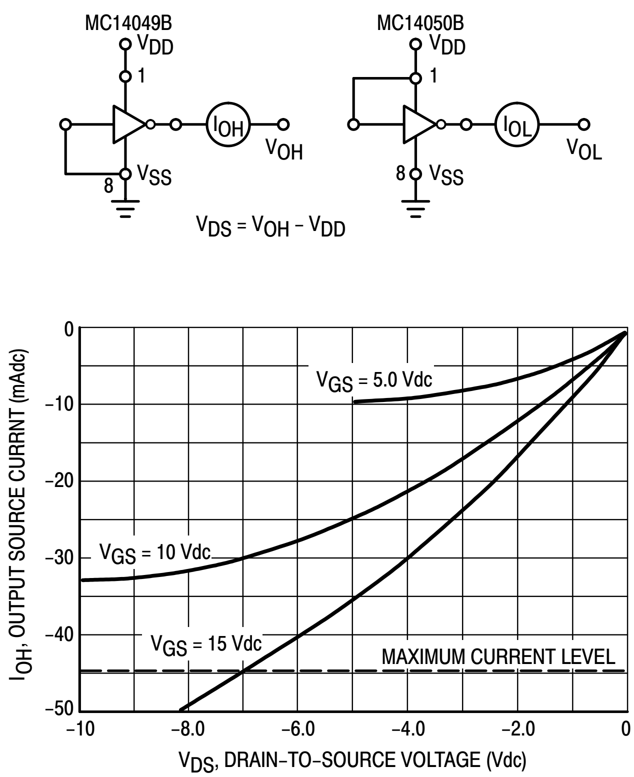


Figure 1. Typical Output Source Characteristics

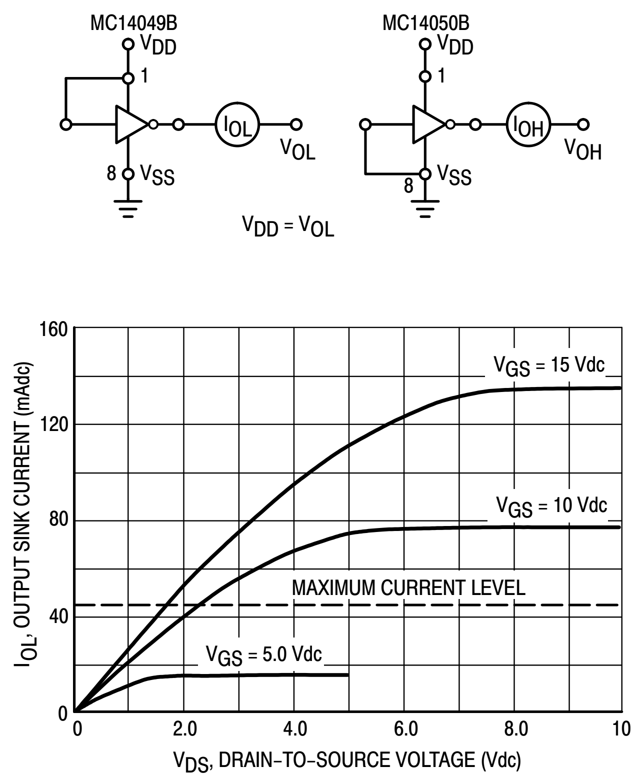


Figure 2. Typical Output Sink Characteristics

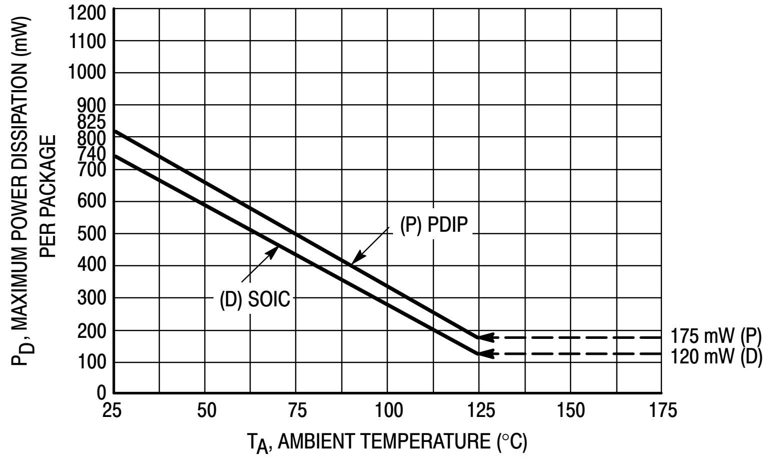


Figure 3. Ambient Temperature Power Derating

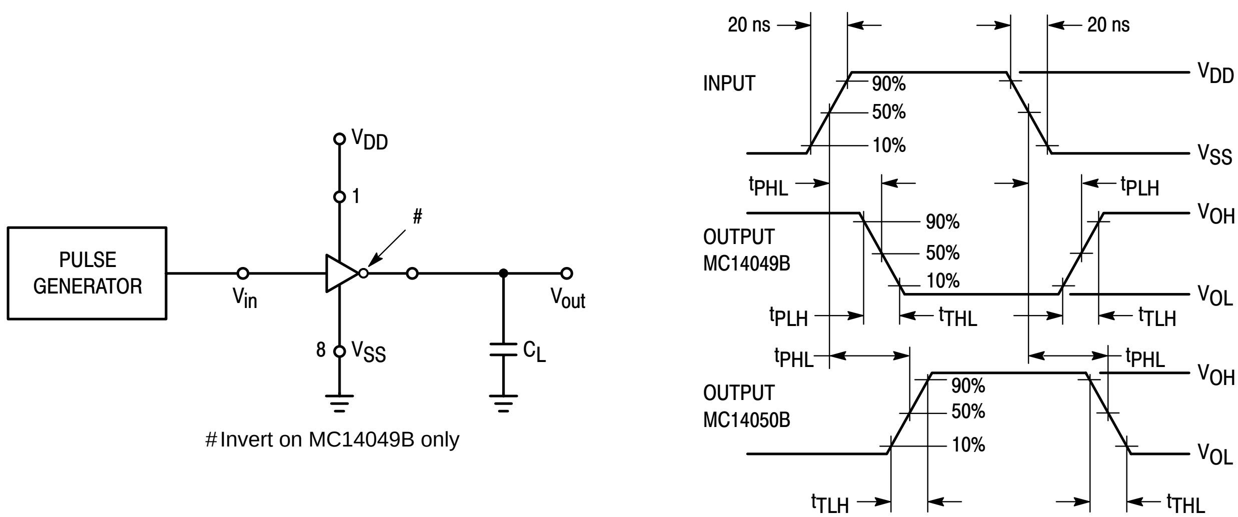


Figure 4. Switching Time Test Circuit and Waveforms

MC14049UB

Hex Buffers

The MC14049UB hex inverter/buffer is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This complementary MOS device finds primary use where low power dissipation and/or high noise immunity is desired. This device provides logic−level conversion using only one supply voltage, V_{DD}. The input−signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic−level conversions. Two TTL/DTL Loads can be driven when the device is used as CMOS−to−TTL/DTL converters (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pins 13 and 16 are not connected internally on this device; consequently connections to these terminals will not affect circuit operation.

Features

- High Source and Sink Currents
- High−to−Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- V_{IN} can exceed V_{DD}
- Improved ESD Protection on All Inputs
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	+45	mA
P_D	Power Dissipation, per Package (Note 14) Plastic SOIC	 825 740	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

14. Temperature Derating: All Packages: See Figure 4.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high−impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq$ 18 V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

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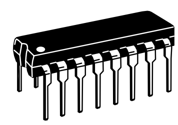
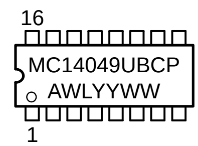
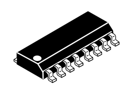
MARKING DIAGRAMS

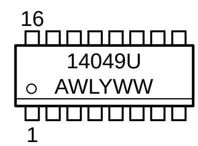


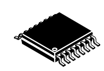
PDIP−16
P SUFFIX
CASE 648



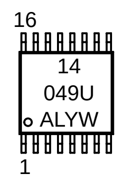


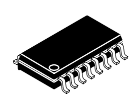
SOIC−16
D SUFFIX
CASE 751B



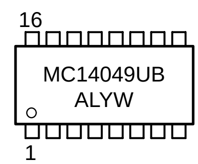


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 145 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

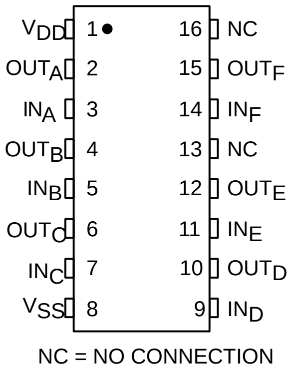


Figure 1. Pin Assignment

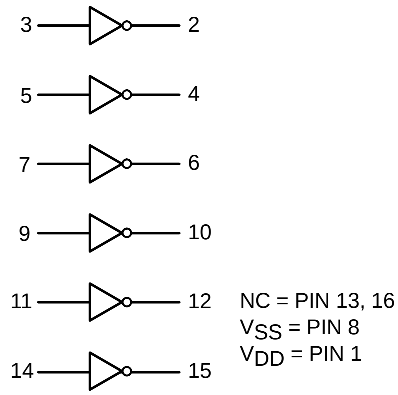


Figure 2. Logic Diagram MC14049UB

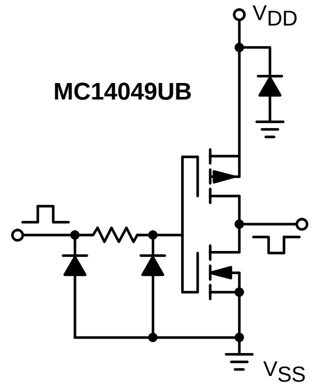


Figure 3. Circuit Schematic
(1/6 of circuit shown)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 15)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	“0” Level	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	“1” Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	“0” Level	V_{IL}	5.0 10 15	− − −	1.0 2.0 2.5	− − −	2.25 4.50 6.75	1.0 2.0 2.5	− − −	1.0 2.0 2.5	Vdc
(V_O = 0.5 Vdc) (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	“1” Level	V_{IH}	5.0 10 15	4.0 8.0 12.5	− − −	4.0 8.0 12.5	2.75 5.50 8.25	− − −	4.0 8.0 12.5	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 10 15	– 1.6 – 1.6 – 4.7	− − −	– 1.25 – 1.3 – 3.75	– 2.5 – 2.6 – 10	− − −	– 1.0 – 1.0 – 3.0	− − −	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	3.75 10 30	− − −	3.2 8.0 24	6.0 16 40	− − −	2.6 6.6 19	− − −	mAdc
Input Current		I_{in}	15	−	± 0.1	−	±0.00001	± 0.1	−	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	−	−	−	−	10	20	−	−	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	− − −	1.0 2.0 4.0	− − −	0.002 0.004 0.006	1.0 2.0 4.0	− − −	30 60 120	µAdc
Total Supply Current (Note 16 and 17) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.8 µA/kHz) f + I_{DD} I_T = (3.5 µA/kHz) f + I_{DD} I_T = (5.3 µA/kHz) f + I_{DD}							µAdc

15. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
16. The formulas given are for the typical characteristics only at 25°C.
17. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (Note 18) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 19)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	50	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/PF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	

18. The formulas given are for the typical characteristics only at 25°C.
19. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14049UBCP	PDIP−16	2,000 Units / Box
MC14049UBCPG	PDIP−16 (Pb−Free)	2,000 Units / Box
MC14049UBD	SOIC−16	2,400 Units / Box
MC14049UBDG	SOIC−16 (Pb−Free)	2,400 Units / Box
MC14049UBDR2	SOIC−16	2,500 / Tape & Reel
MC14049UBDR2G	SOIC−16 (Pb−Free)	2,500 / Tape & Reel
MC14049UBDT	TSSOP−16	96 Units / Rail
MC14049UBDTEL	TSSOP−16*	96 Units / Rail
MC14049UBDTR2	TSSOP−16*	2,500 / Tape & Reel
MC14049UBF	SOEIAJ−16	See Note 20
MC14049UBFEL	SOEIAJ−16	See Note 20

20. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb−Free.

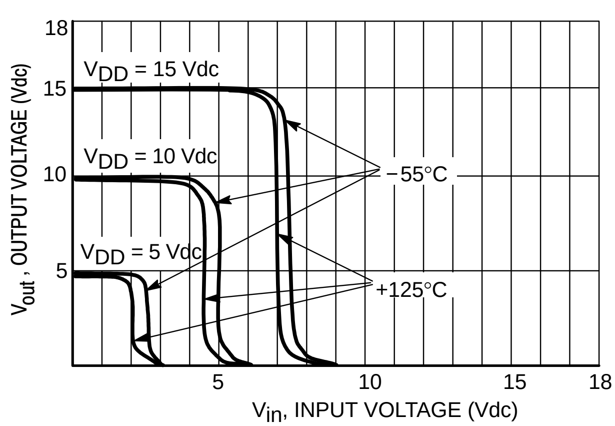


Figure 4. Typical Voltage Transfer Characteristics versus Temperature

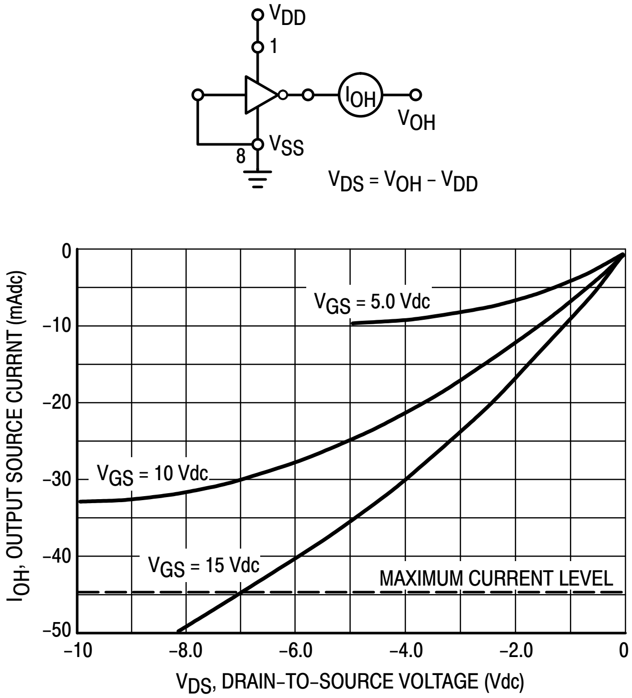


Figure 5. Typical Output Source Characteristics

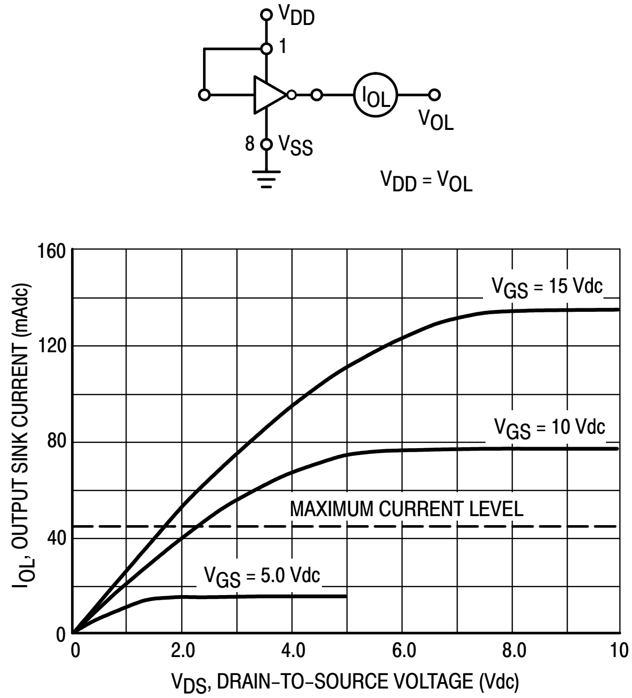


Figure 6. Typical Output Sink Characteristics

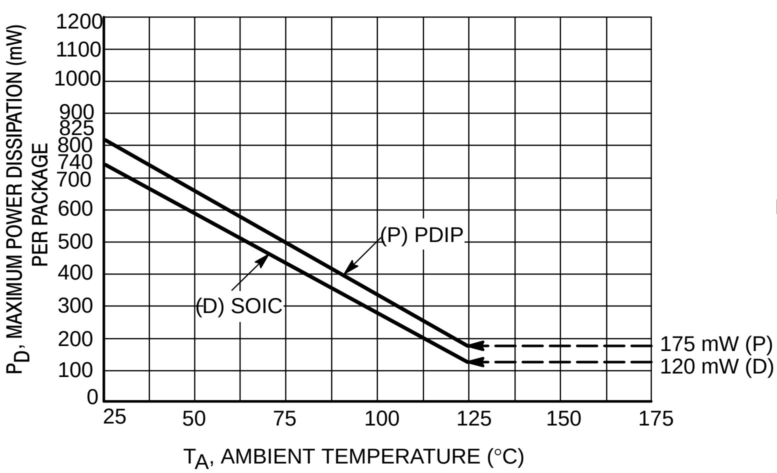


Figure 7. Ambient Temperature Power Derating

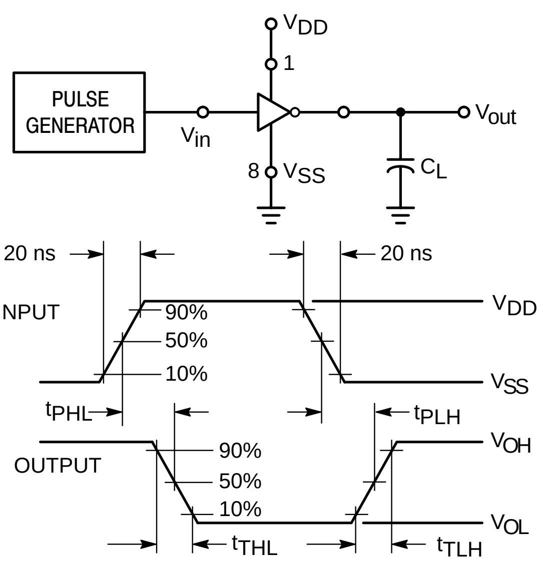


Figure 8. Switching Time Test Circuit and Waveforms

MC14051B, MC14052B, MC14053B

Analog Multiplexers/Demultiplexers

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally−controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

Features

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
  Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low−noise − 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz Typical
- Pin−for−Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON}, Use the HC4051, HC4052, or HC4053 High−Speed CMOS Devices
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	+10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation per Package (Note 21)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

21. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

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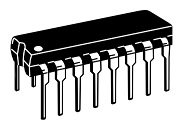
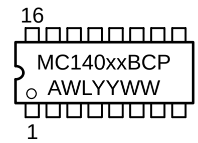
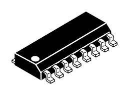
MARKING DIAGRAMS

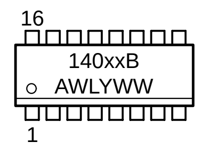


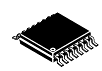
PDIP−16
P SUFFIX
CASE 648



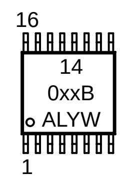


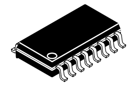
SOIC−16
D SUFFIX
CASE 751B



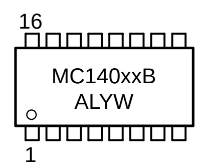


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



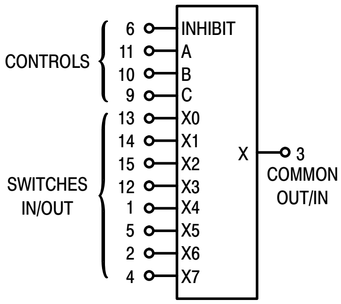
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 155 of this data sheet.

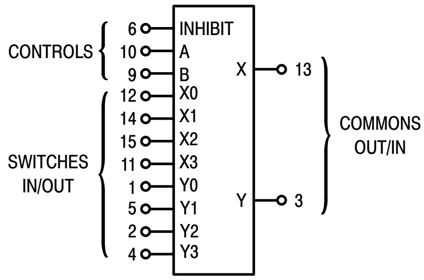
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14051B
8−Channel Analog
Multiplexer/Demultiplexer



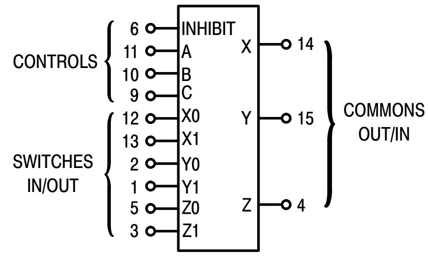
V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

MC14052B
Dual 4−Channel Analog
Multiplexer/Demultiplexer



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

MC14053B
Triple 2−Channel Analog
Multiplexer/Demultiplexer

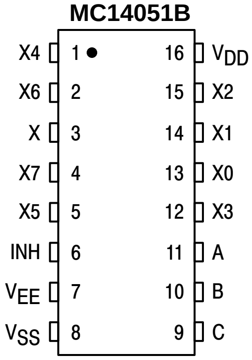


V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

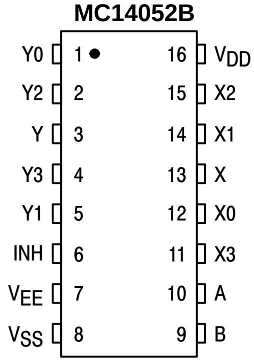
Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

PIN ASSIGMENT

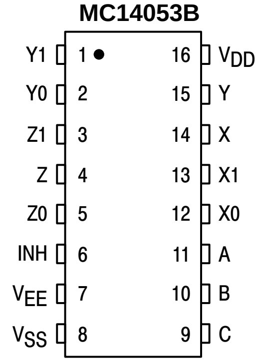
MC14051B



MC14052B



MC14053B



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 22)	Max	Min	Max	
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	–	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq$ 500 mV (Note 23)	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.36 µA/kHz) f + I_{DD}				µA
CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
High−Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	± 0.1	–	±0.00001	± 0.1	–	1.0	µA
Input Capacitance	C_{in}	–		–	–	–	5.0	7.5	–	–	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note 23) (Figure 5)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0 V, No Load	–	–	–	10	–	–	–	µV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq$ 500 mV (Note 23) $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	– – –	800 400 220	– – –	250 120 80	1050 500 280	– – –	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		– – –	70 50 45	– – –	25 10 10	70 50 45	– – –	135 95 65	Ω
Off−Channel Leakage Current (Figure 10)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	–	± 100	–	± 0.05	± 100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	Inhibit = V_{DD}	–	–	–	10	–	–	–	pF
Capacitance, Common O/I	$C_{O/I}$	–	Inhibit = V_{DD} (MC14051B) (MC14052B) (MC14053B)	 – – –	 – – –	 – – –	 60 32 17	 – – –	 – – –	 – – –	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	– –	Pins Not Adjacent Pins Adjacent	– –	– –	– –	0.15 0.47	– –	– –	– –	pF

22. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
23. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (Note 24) (C_L = 50 pF, T_A = 25°C) ($V_{EE} \leq V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Typ (Note 25) All Types	Max	Unit
Propagation Delay Times (Figure 6) Switch Input to Switch Output (R_L = 10 kΩ) MC14051 t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns	t_{PLH}, t_{PHL}	5.0 10 15	35 15 12	90 40 30	ns
MC14052 t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		5.0 10 15	30 12 10	75 30 25	ns
MC14053 t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		5.0 10 15	25 8.0 6.0	65 20 15	ns
Inhibit to Output (R_L = 10 kΩ, V_{EE} = V_{SS}) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level MC14051B	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0 10 15	350 170 140	700 340 280	ns
MC14052B		5.0 10 15	300 155 125	600 310 250	ns
MC14053B		5.0 10 15	275 140 110	550 280 220	ns
Control Input to Output (R_L = 10 kΩ, V_{EE} = V_{SS}) MC14051B	t_{PLH}, t_{PHL}	5.0 10 15	360 160 120	720 320 240	ns
MC14052B		5.0 10 15	325 130 90	650 260 180	ns
MC14053B		5.0 10 15	300 120 80	600 240 160	ns
Second Harmonic Distortion (R_L = 10KΩ, f = 1 kHz) V_{in} = 5 V_{PP}	–	10	0.07	–	%
Bandwidth (Figure 7) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}−V_{EE}) p−p, C_L = 50pF 20 Log (V_{out}/V_{in}) = − 3 dB)	BW	10	17	–	MHz
Off Channel Feedthrough Attenuation (Figure 7) R_L = 1KΩ, V_{in} = 1/2 (V_{DD} − V_{EE}) p−p f_{in} = 4.5 MHz — MC14051B f_{in} = 30 MHz — MC14052B f_{in} = 55 MHz — MC14053B	–	10	– 50	–	dB
Channel Separation (Figure 8) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}−V_{EE}) p−p, f_{in} = 3.0 MHz	–	10	– 50	–	dB
Crosstalk, Control Input to Common O/I (Figure 9) (R_1 = 1 kΩ, R_L = 10 kΩ Control t_{TLH} = t_{THL} = 20 ns, Inhibit = V_{SS})	–	10	75	–	mV

24. The formulas given are for the typical characteristics only at 25°C.
25. Data labelled "Typ" is not lo be used for design purposes but In intended as an indication of the IC's potential performance.

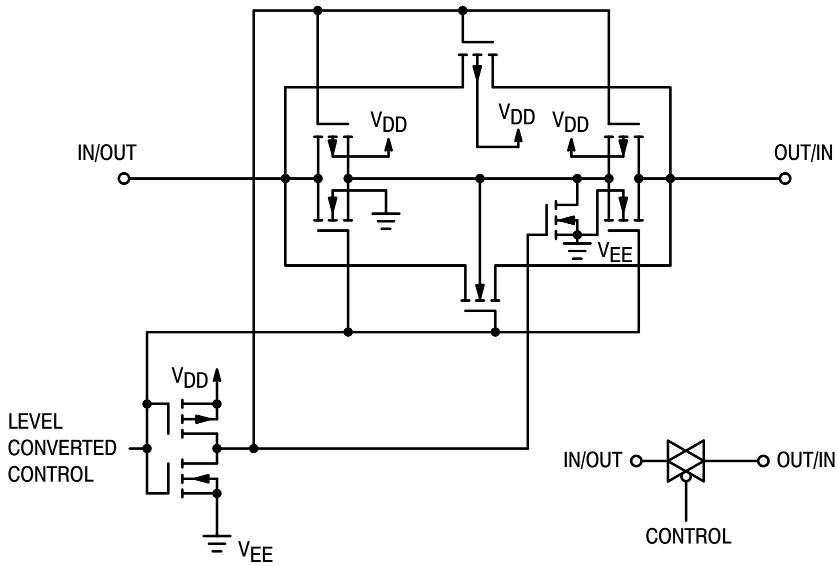


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches					
	Select								
Inhibit	C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for MC14052
x = Don't Care

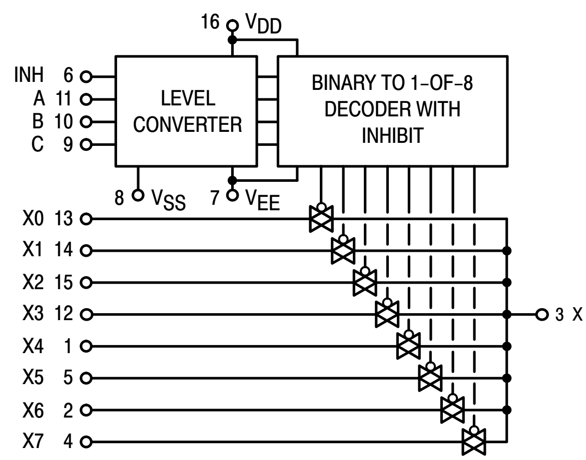


Figure 2. MC14051B Functional Diagram

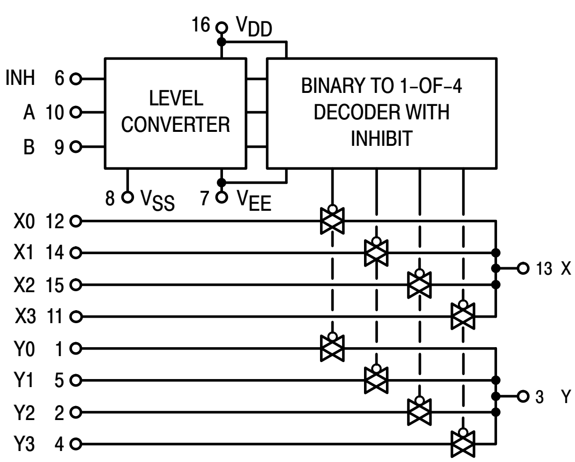


Figure 3. MC14052B Functional Diagram

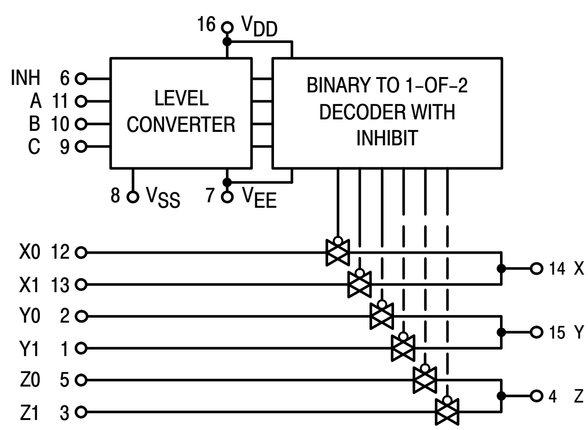


Figure 4. MC14053B Functional Diagram

TEST CIRCUITS

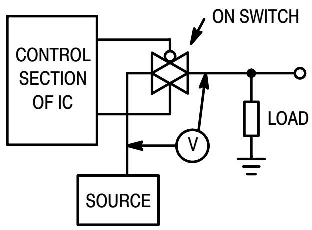


Figure 5. ΔV Across Switch

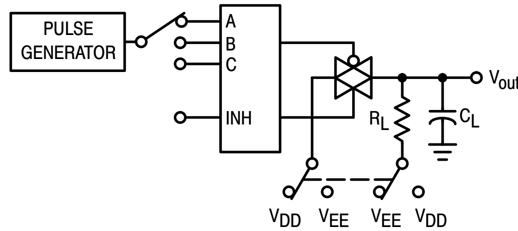


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.

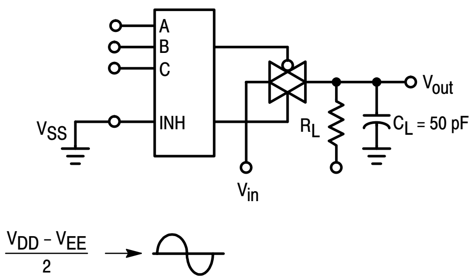


Figure 7. Bandwidth and Off−Channel Feedthrough Attenuation

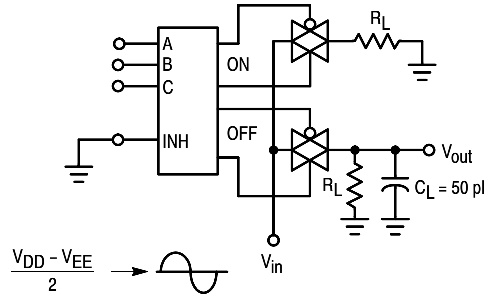


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

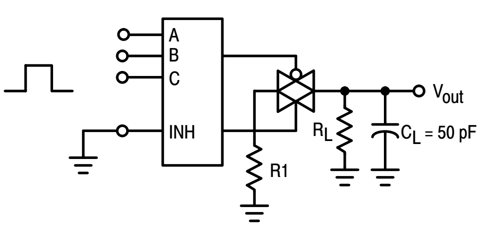


Figure 9. Crosstalk, Control Input to Common O/I

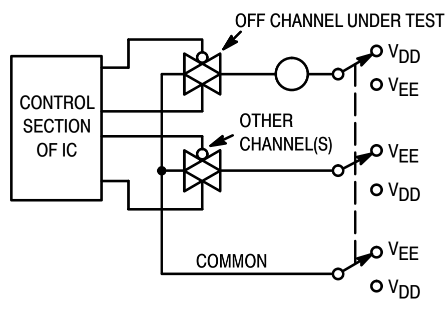


Figure 10. Off Channel Leakage

NOTE: See also Figures 7 and 8 in the MC14016B data sheet.

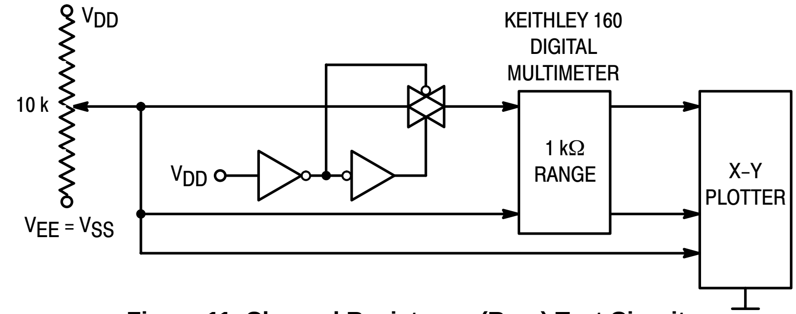


Figure 11. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

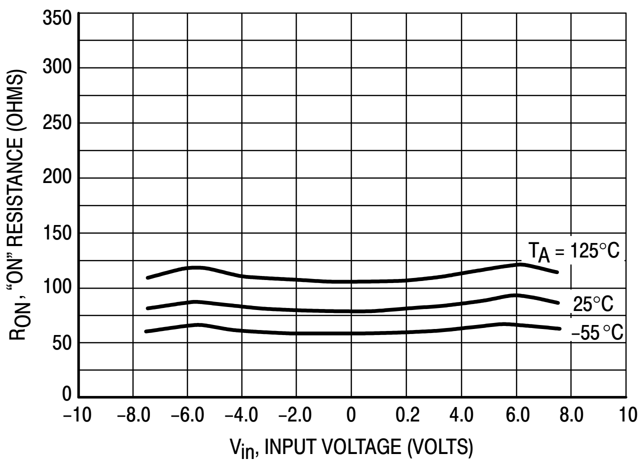


Figure 12. V_{DD} = 7.5 V, V_{EE} = − 7.5 V

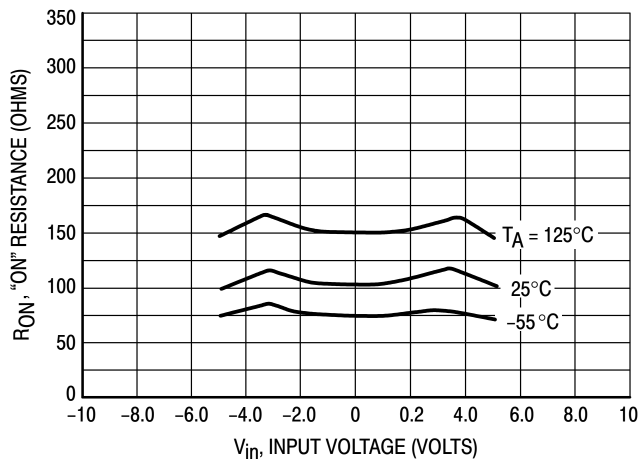


Figure 13. V_{DD} = 5.0 V, V_{EE} = − 5.0 V

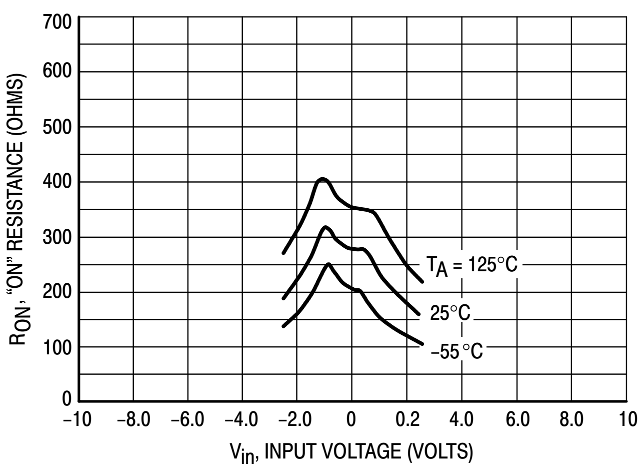


Figure 14. V_{DD} = 2.5 V, V_{EE} = − 2.5 V

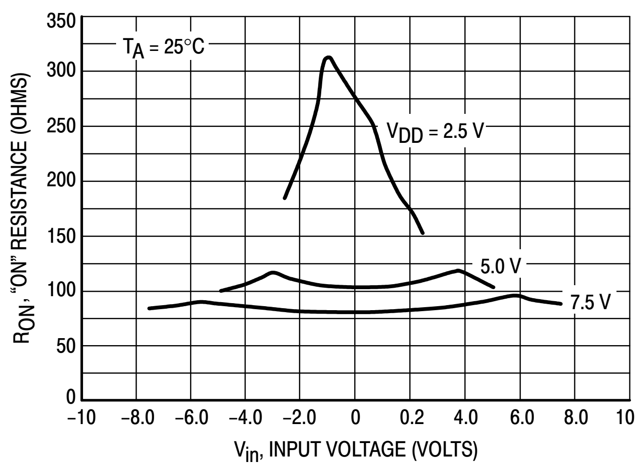


Figure 15. Comparison at 25°C, V_{DD} = −V_{EE}

APPLICATIONS INFORMATION

Figure A illustrates use of the on−chip level converter detailed in Figures 2, 3, and 4. The 0−to−5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 V maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 V, V_{SS} = + 5 V, and V_{EE} – 3 V is acceptable. See the Table below.

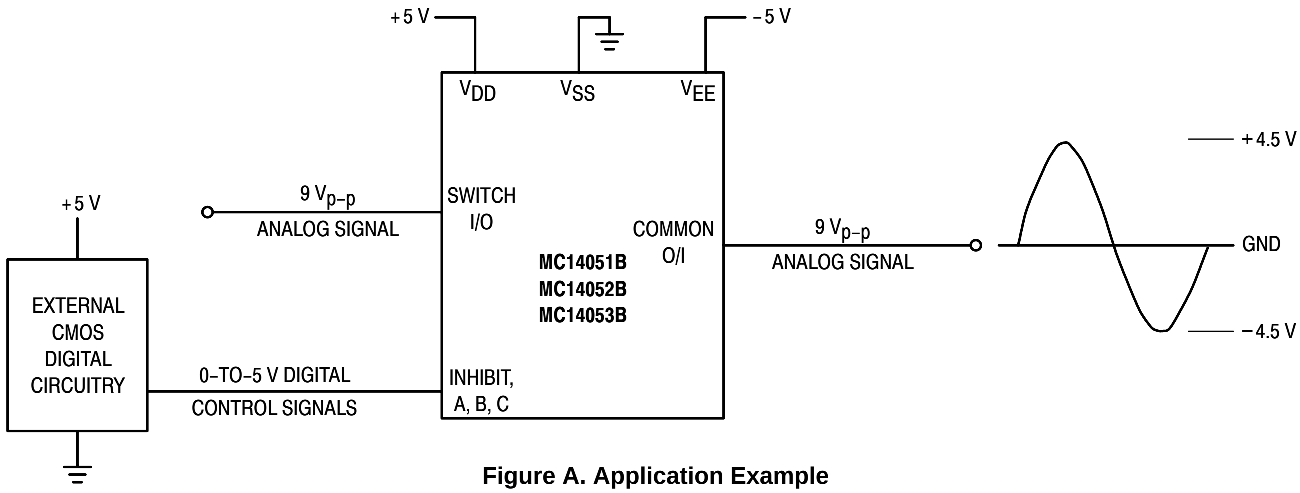


Figure A. Application Example

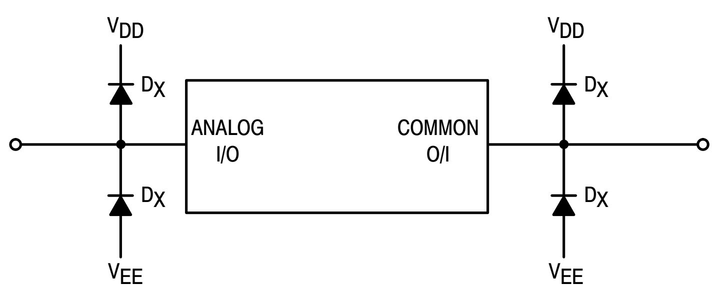


Figure B. External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	– 8	+ 8/0	+ 8 to – 8 = 16 $V_{p–p}$
+ 5	0	– 12	+ 5/0	+ 5 to – 12 = 17 $V_{p–p}$
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 $V_{p–p}$
+ 5	0	– 5	+ 5/0	+ 5 to – 5 = 10 $V_{p–p}$
+ 10	+ 5	– 5	+ 10/ + 5	+ 10 to – 5 = 15 $V_{p–p}$

ORDERING INFORMATION

Device	Package	Shipping†
MC14051BCP	PDIP−16	2,000 Units / Box
MC14051BCPG	PDIP−16 (Pb−Free)	2,000 Units / Box
MC14051BD	SOIC−16	48 Units / Rail
MC14051BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14051BDR2	SOIC−16	2,500 / Tape & Reel
MC14051BDR2G	SOIC−16 (Pb−Free)	2,500 / Tape & Reel
MC14051BDT	TSSOP−16*	96 Units / Rail
MC14051BDTEL	TSSOP−16	2,500 / Tape & Reel
MC14051BDTR2	TSSOP−16*	2,500 / Tape & Reel
MC14051BF	SOEIAJ−16	See Note 26
MC14051BFEL	SOEIAJ−16	See Note 26
MC14052BCP	PDIP−16	2,000 Units / Box
MC1405BCPG	PDIP−16 (Pb−Free)	2,000 Units / Box
MC14052BD	SOIC−16	48 Units / Rail
MC14052BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14052BDR2	SOIC−16	2,500 / Tape & Reel
MC14052BDR2G	SOIC−16 (Pb−Free)	2,500 / Tape & Reel
MC14052BDT	TSSOP−16	96 Units / Rail
MC14052BDTR2	TSSOP−16*	2,500 / Tape & Reel
MC14052BF	SOEIAJ−16	See Note 26
MC14052BFEL	SOEIAJ−16	See Note 26
MC14053BCP	PDIP−16	2,000 Units / Box
MC14053BCPG	PDIP−16 (Pb−Free)	2,000 Units / Box
MC14053BD	SOIC−16	48 Units / Rail
MC14053BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14053BDR2	SOIC−16	2,500 / Tape & Reel
MC14053BDR2G	SOIC−16 (Pb−Free)	2,500 / Tape & Reel
MC14053BDT	TSSOP−16	96 Units / Rail
MC14053BDTR2	TSSOP−16*	2,500 / Tape & Reel
MC14053BF	SOEIAJ−16	See Note 26
MC14053BFEL	SOEIAJ−16	See Note 26

26. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MC14060B

14-Bit Binary Counter and Oscillator

The MC14060B is a 14−stage binary ripple counter with an on−chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin−for−Pin Replacement for CD4060B
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8 Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating: Plastic “P and D/DW” Packages: –7.0 mW/°C from 65°C To 125°C.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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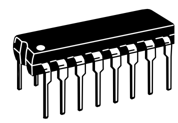
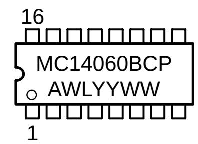
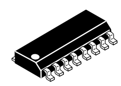
MARKING DIAGRAMS

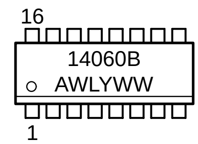


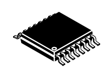
PDIP−16
P SUFFIX
CASE 648



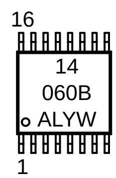


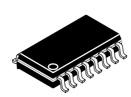
SOIC−16
D SUFFIX
CASE 751B



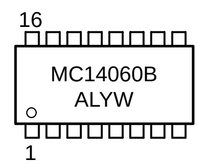


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 161 of this data sheet.

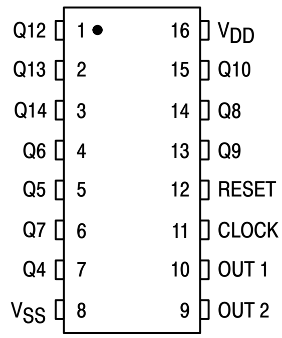


Figure 16. Pin Assignment

Table 1. Truth Table

Clock	Reset	Output State
_/‾	L	No Change
‾_	L	Advance to Next State
H	H	All Outputs are Low

X = Don’t Care

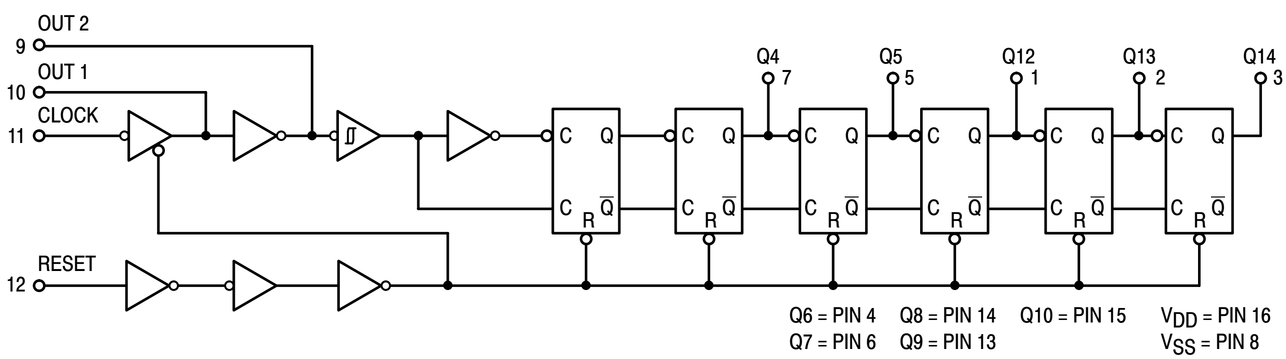


Figure 17. Logic Diagram

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
V_{OL}	Output Voltage "0" Level V_{in} = V_{DD} or 0	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
V_{OH}	V_{in} = 0 or V_{DD} "1" Level	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	V
V_{IL}	Input Voltage "0" Level (V_O = 4.5 or 0.5 V) (V_O = 9.0 or 1.0 V) (V_O = 13.5 or 1.5 V)	 5.0 10 15	 – – –	 1.5 3.0 4.0	 – – –	 2.25 4.50 6.75	 1.5 3.0 4.0	 – – –	 1.5 3.0 4.0	V
V_{IH}	(V_O = 0.5 or 4.5 V) "1" Level (V_O = 1.0 or 9.0 V) (V_O = 1.5 or 13.5 V)	5.0 10 15	3.5 7.0 11.0	– – –	3.5 7.0 11.0	2.75 5.50 8.25	– – –	3.5 7.0 11.0	– – –	V
V_{IL}	Input Voltage "0" Level (V_O = 4.5 Vdc) (For Input 11 (V_O = 9.0 Vdc) and Output 10) (V_O = 13.5 Vdc)	 5.0 10 15	 – – –	 1.0 2.0 2.5	 – – –	 2.25 4.50 6.75	 1.0 2.0 2.5	 – – –	 1.0 2.0 2.5	Vdc
V_{IH}	(V_O = 0.5 Vdc) "1" Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	5.0 10 15	4.0 8.0 12.5	– – –	4.0 8.0 12.5	2.75 5.50 8.25	– – –	4.0 8.0 12.5	– – –	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 V) (Except Source (V_{OH} = 4.6 V) Pins 9 and 10) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	 5.0 5.0 10 15	 –3.0 –0.64 –1.6 – 4.2	 – – – –	 –2.4 –0.51 –1.3 –3.4	 –4.2 –0.88 –2.25 –8.8	 – – – –	 – 1.7 – 0.36 – 0.9 – 2.4	 – – – –	mA
I_{OL}	(V_{OL} = 0.4 V) Sink (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mA
I_{in}	Input Current	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μA
C_{in}	Input Capacitance (V_{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I_{DD}	Quiescent Current (Per Package)	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μA
I_T	Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	5.0 10 15	I_T = (0.25 μA/kHz) f + I_{DD} I_T = (0.54 μA/kHz) f + I_{DD} I_T = (0.85 μA/kHz) f + I_{DD}							μA

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)$ Vfk
where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD} Vdc	Min	Typ (Note 5)	Max	Unit
t_{TLH}	Output Rise Time (Counter Outputs)	5.0 10 15	– – –	40 25 20	200 100 80	ns
t_{THL}	Output Fall Time (Counter Outputs)	5.0 10 15	– – –	50 30 20	200 100 80	ns
t_{PLH} t_{PHL}	Propagation Delay Time Clock to Q4	5.0 10 15	– – –	415 175 125	740 300 200	ns
	Clock to Q14	5.0 10 15	– – –	1.5 0.7 0.4	2.7 1.3 1.0	μs
t_{WH}	Clock Pulse Width	5.0 10 15	100 40 30	65 30 20	– – –	ns
f_{ϕ}	Clock Pulse Frequency	5.0 10 15	– – –	5 14 17	3.5 8 12	MHz
t_{TLH} t_{THL}	Clock Rise and Fall Time	5.0 10 15	No Limit			ns
t_w	Reset Pulse Width	5.0 10 15	120 60 40	40 15 10	– – –	ns
t_{PHL}	Propagation Delay Time Reset to On	5.0 10 15	– – –	170 80 60	350 160 100	ns

5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

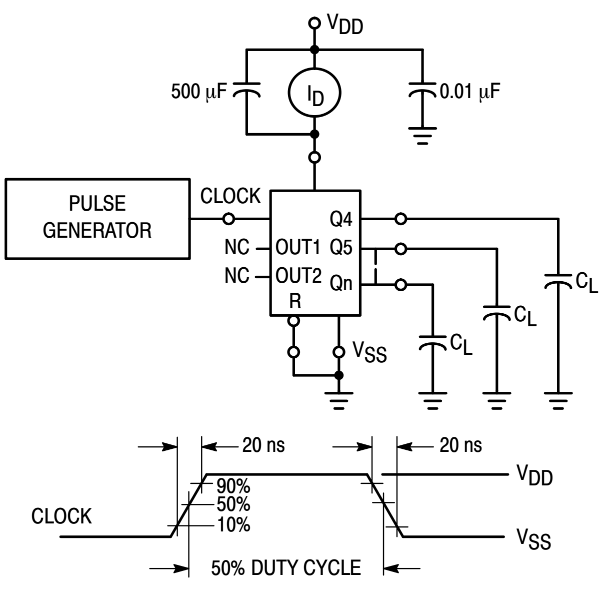


Figure 1. Power Dissipation Test Circuit and Waveform

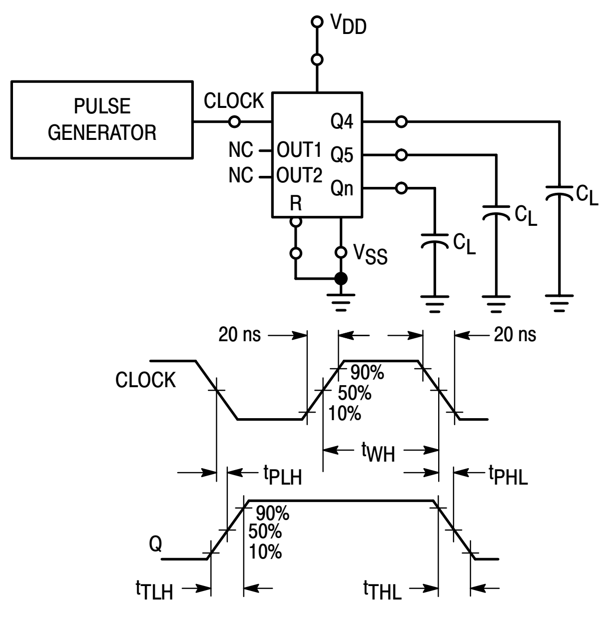
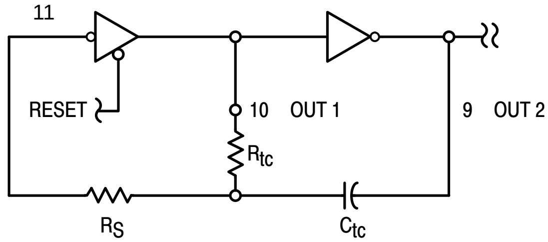


Figure 2. Switching Time Test Circuit and Waveforms



$$f \approx \frac{1}{2.3 R_{tc} C_{tc}}$$

if 1 kHz ≤ f ≤ 100 kHz
and $2R_{tc} < R_S < 10R_{tc}$
(f in Hz, R in ohms, C in farads)

The formula may vary for other frequencies. Recommended maximum value for the resistors in 1 MΩ.

Figure 3. Oscillator Circuit Using RC Configuration

TYPICAL RC OSCILLATOR CHARACTERISTICS

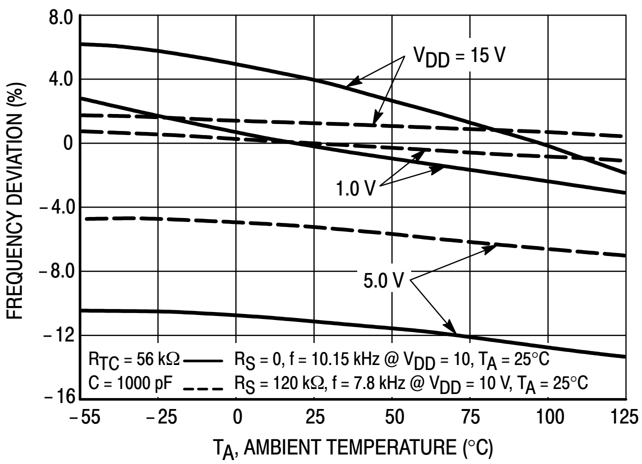


Figure 4. RC Oscillator Stability

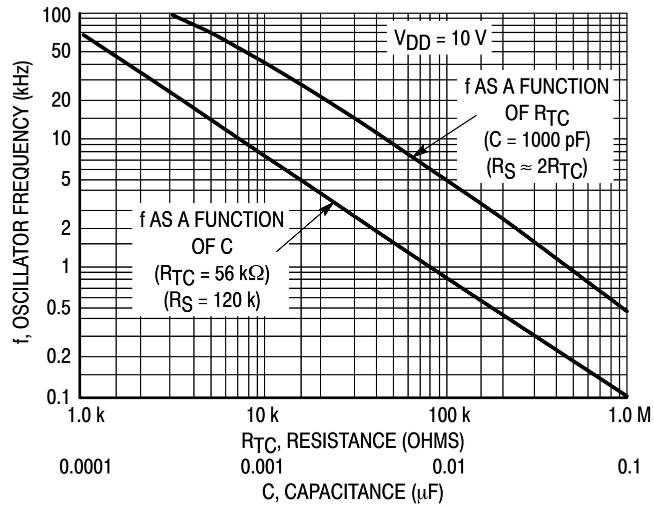


Figure 5. RC Oscillator Frequency as a Function of R_{TC} and C

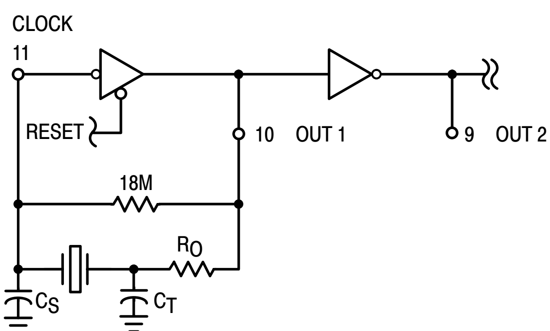


Figure 6. Typical Crystal Oscillator Circuit

Table 2. Typical Data for Crystal Oscillator Circuit

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics Resonant Frequency Equivalent Resistance, R_S	 500 1.0	 32 6.2	 kHz kΩ
External Resistor/Capacitor Values R_O C_T C_S	 47 82 20	 750 82 20	 kΩ pF pF
Frequency Stability Frequency Changes as a Function of V_{DD} (T_A = 25°C) V_{DD} Change from 5.0 V to 10 V V_{DD} Change from 10 V to 15 V	 +6.0 +2.0	 +2.0 +2.0	 ppm ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V) T_A Change from − 55°C to + 25°C Complete Oscillator (Note 6)	 +100	 +120	 ppm
T_A Change from + 25°C to + 125°C Complete Oscillator (Note 6)	–160	–560	ppm

6. Complete oscillator includes crystal, capacitors, and resistors.

ORDERING INFORMATION

Device	Package	Shipping†
MC14060BCP	PDIP−16	500 Units / Rail
MC14060BCPG	PDIP−16 (Pb−Free)	500 Units / Rail
MC14060BD	SOIC−16	48 Units / Rail
MC14060BDR2	SOIC−16	2500 / Tape & Reel
MC14060BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC14060BFEL	SOEIAJ−16 (Pb−Free)	2000 / Tape & Reel
MC14060BDTR2	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14066B

Quad Analog Switch/Quad Multiplexer

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin−for−pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/√Cycle, f ≥ 1.0 kHz typical
- Pin−for−Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON}, Use The HC4066 High−Speed CMOS Device

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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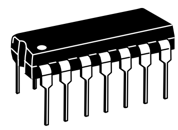
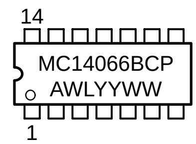
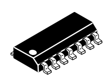
MARKING DIAGRAMS

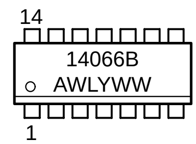


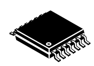
PDIP−14
P SUFFIX
CASE 646



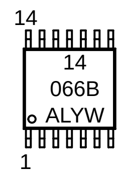


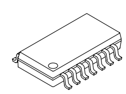
SOIC−14
D SUFFIX
CASE 751A



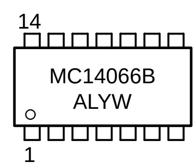


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965



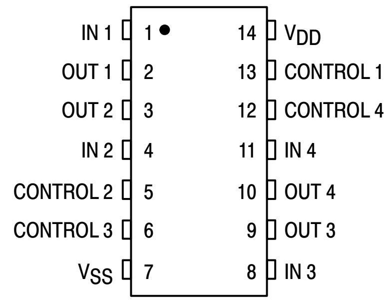
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

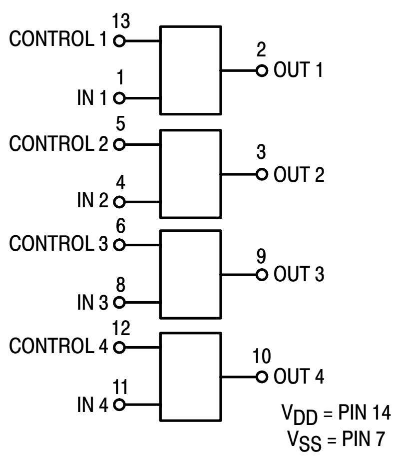
Device	Package	Shipping
MC14066BCP	PDIP−14	2000/Box
MC14066BD	SOIC−14	55/Rail
MC14066BDR2	SOIC−14	2500/Tape & Reel
MC14066BDT	TSSOP−14	96/Rail
MC14066BDTEL	TSSOP−14	2000/Tape & Reel
MC14066BDTR2	TSSOP−14	2500/Tape & Reel
MC14066BF	SOEIAJ−14	See Note 1.
MC14066BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

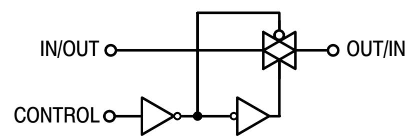


BLOCK DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLE

(1/4 OF DEVICE SHOWN)



Control	Switch
$0 = V_{SS}$	OFF
$1 = V_{DD}$	ON

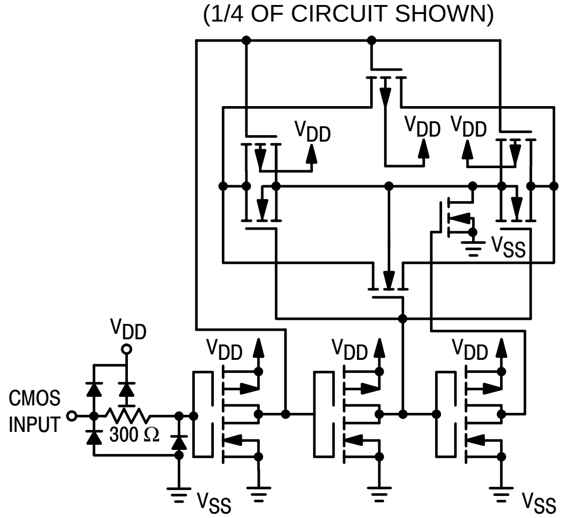
Logic Diagram Restrictions

$V_{SS} \leq V_{in} \leq V_{DD}$

$V_{SS} \leq V_{out} \leq V_{DD}$

CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV (5.)	— — —	0.25 0.5 1.0	— — —	0.005 0.010 0.015	0.25 0.5 1.0	— — —	7.5 15 30	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical (0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.36 µA/kHz) f + I_{DD}							µA
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High−Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	µV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV (5.), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off−Channel Leakage Current (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	± 0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	— —		—	—	—	0.47	—	—	—	pF

4. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
5. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [7.]	Max	Unit
Propagation Delay Times V_{SS} = 0 Vdc	t_{PLH}, t_{PHL}					ns
Input to Output (R_L = 10 kΩ)						
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns		5.0	—	20	40	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns		10	—	10	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		15	—	7.0	15	
Control to Output (R_L = 1 kΩ) (Figure 2)	t_{PHZ}					ns
Output "1" to High Impedance		5.0	—	40	80	
		10	—	35	70	
		15	—	30	60	
Output "0" to High Impedance	t_{PLZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
High Impedance to Output "1"	t_{PZH}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
High Impedance to Output "0"	t_{PZL}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
Second Harmonic Distortion V_{SS} = – 5 Vdc (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) V_{SS} = – 5 Vdc (R_L = 1 kΩ, 20 Log (V_{out}/V_{in}) = − 3 dB, C_L = 50 pF, V_{in} = 5 V_{p-p})	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = – 5 Vdc (V_{in} = 5 V_{p-p}, R_L = 1 kΩ, f_{in} = 1.0 MHz) (Figure 3)	—	5.0	—	– 50	—	dB
Channel Separation (Figure 4) V_{SS} = – 5 Vdc (V_{in} = 5 V_{p-p}, R_L = 1 kΩ, f_{in} = 8.0 MHz) (Switch A ON, Switch B OFF)	—	5.0	—	– 50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) V_{SS} = – 5 Vdc (R_1 = 1 kΩ, R_L = 10 kΩ, Control t_{TLH} = t_{THL} = 20 ns)	—	5.0	—	300	—	mV_{p-p}

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TEST CIRCUITS

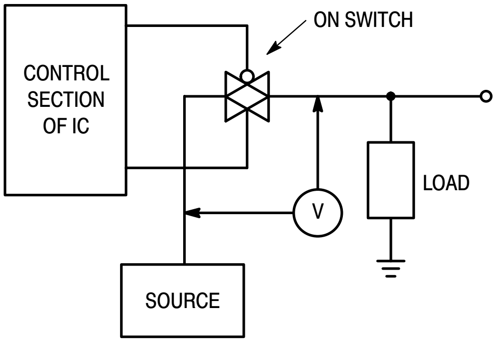


Figure 1. ΔV Across Switch

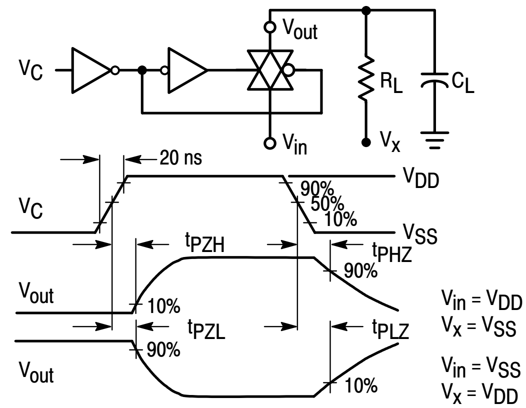


Figure 2. Turn−On Delay Time Test Circuit and Waveforms

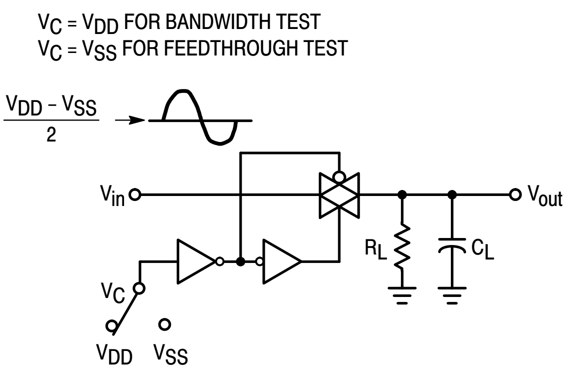


Figure 3. Bandwidth and Feedthrough Attenuation

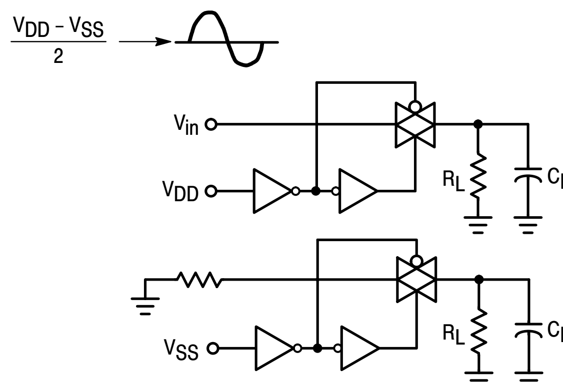


Figure 4. Channel Separation

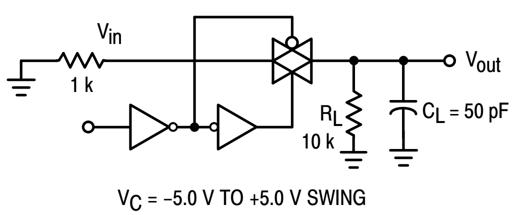


Figure 5. Crosstalk, Control to Output

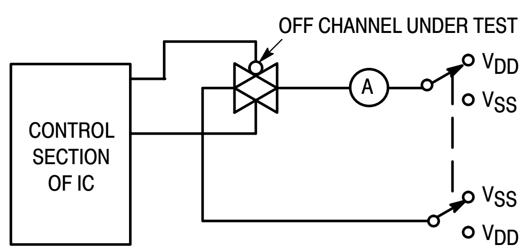


Figure 6. Off Channel Leakage

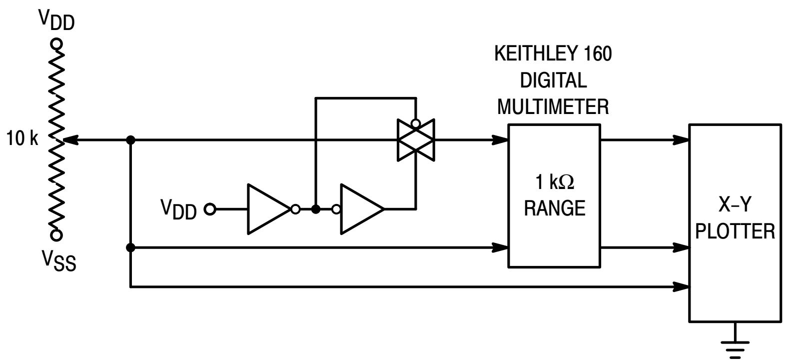


Figure 7. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

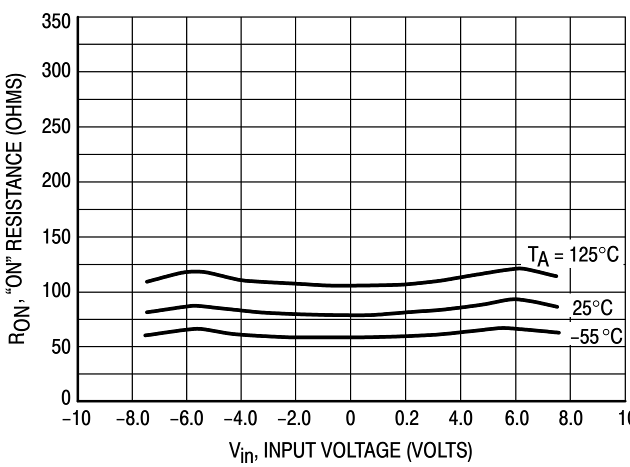


Figure 8. V_{DD} = 7.5 V, V_{SS} = − 7.5 V

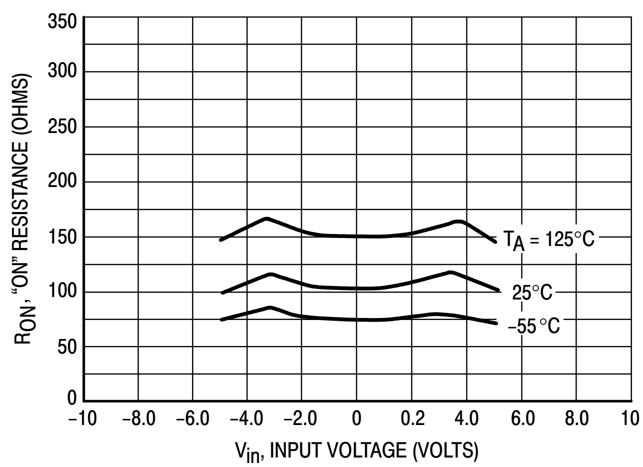


Figure 9. V_{DD} = 5.0 V, V_{SS} = − 5.0 V

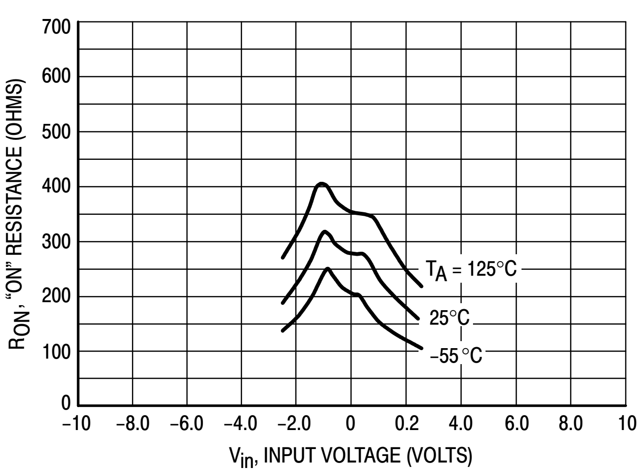


Figure 10. V_{DD} = 2.5 V, V_{SS} = − 2.5 V

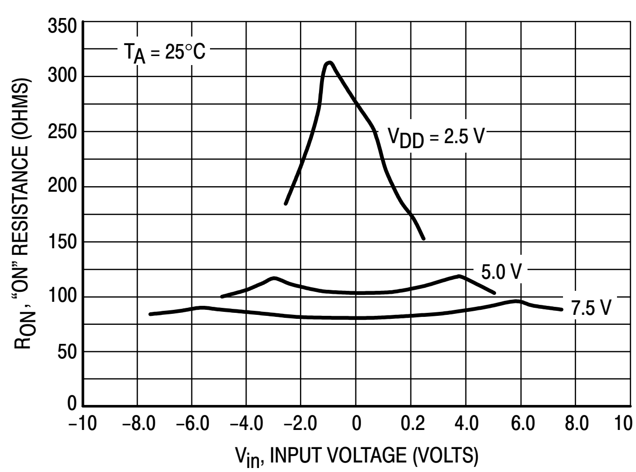


Figure 11. Comparison at 25°C, V_{DD} = −V_{SS}

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0−to−5 volt digital control signal is used to directly control a 5 volt peak−to−peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage, the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 volt peak−to−peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS}.

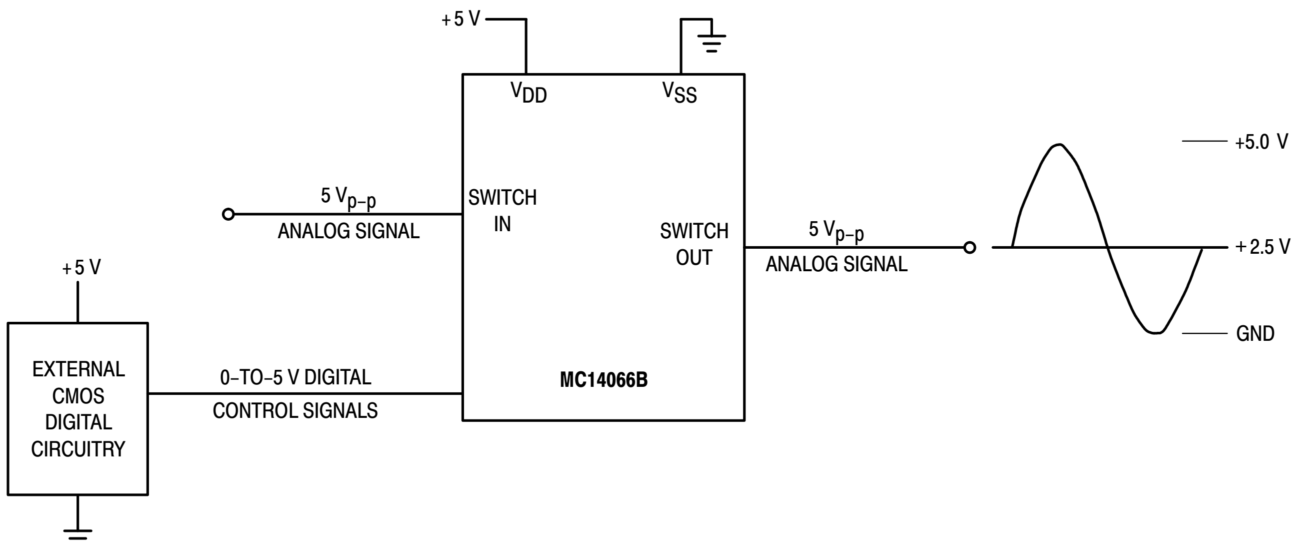


Figure A. Application Example

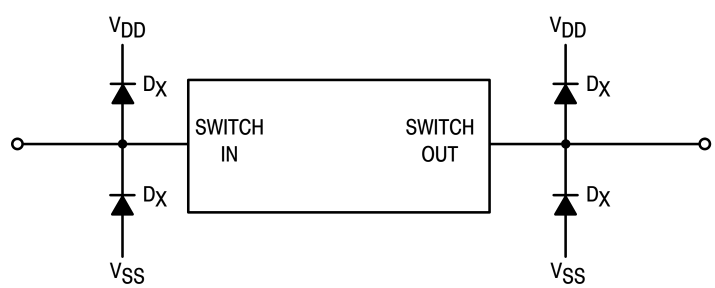


Figure B. External Germanium or Schottky Clipping Diodes

MC14067B

Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

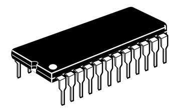
The MC14067 is a 16−channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1−of−16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B

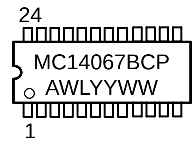
ON Semiconductor

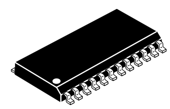
http://onsemi.com

MARKING DIAGRAMS

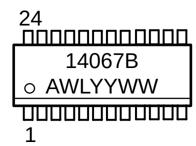


PDIP−24
P SUFFIX
CASE 709





SOIC−24
DW SUFFIX
CASE 751E



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14067BCP	PDIP−24	15/Rail
MC14067BDW	SOIC−24	30/Rail
MC14067BDWR2	SOIC−24	1000/Tape & Reel

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{SW}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	– 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: − 7.0 mW/°C From 65°C To 125°C

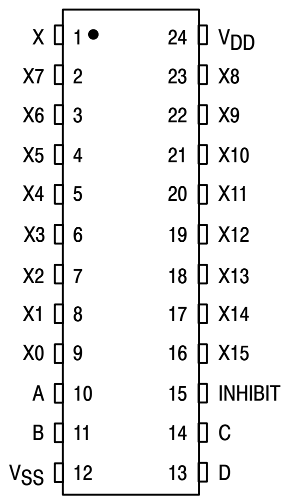
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

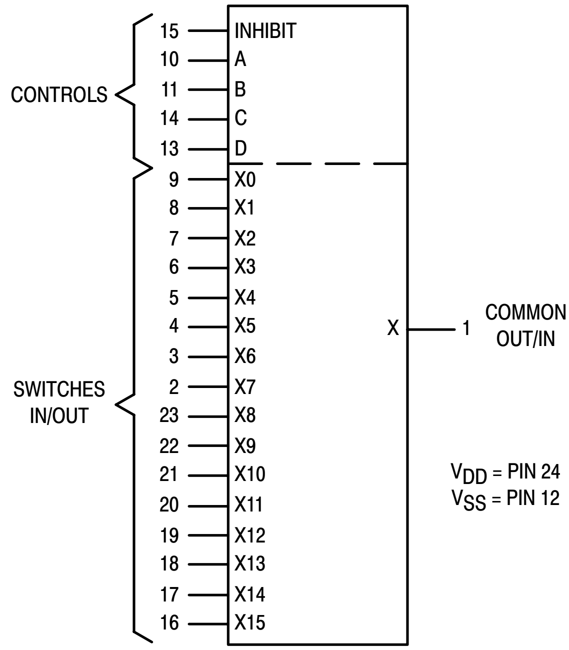
MC14067 TRUTH TABLE

Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

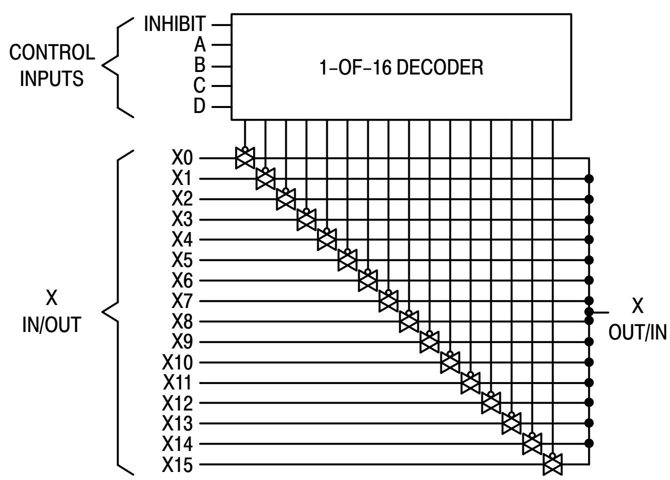
MC14067B
PIN ASSIGNMENT



MC14067B
16−Channel Analog
Multiplexer/Demultiplexer



MC14067 FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ [3.]	Max	Min	Max	
SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: V_{SS} ≤ $V_{I/O}$ ≤ V_{DD}, and ΔV_{switch} ≤ 500 mV [4.]	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, (V_{in} – V_{out})/R_{on}, is not included.)	Typical			(0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.36 µA/kHz) f + I_{DD}				µA
CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High−Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	± 0.1	—	±0.00001	± 0.1	—	1.0	µA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V_{SS})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch [4.] (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	µV
ON Resistance	R_{on}	5.0 10 15	ΔV_{switch} ≤ 500 mV [4.], V_{in} = V_{IL} or V_{IH} (Control), and V_{in} 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off−Channel Leakage Current (Figure 2)	I_{off}	15	V_{in} = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel	—	± 100	—	± 0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD} (MC14067B) (MC14097B)	 — —	 — —	 — —	 100 60	 — —	 — —	 — —	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	—	—	—	0.47	—	—	—	pF

3. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
4. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	$V_{DD} - V_{SS}$ Vdc	Typ (5.)	Max	Unit
Propagation Delay Times Channel Input−to−Channel Output (R_L = 200 kΩ) MC14067B	t_{PLH}, t_{PHL} (Figure 3)	5.0 10 15	35 15 12	90 40 30	ns
Control Input−to−Channel Output Channel Turn−On Time (R_L = 10 kΩ) MC14067B	t_{PZH}, t_{PZL} (Figure 4)	5.0 10 15	240 115 75	600 290 190	ns
Channel Turn−Off Time (R_L = 300 kΩ) MC14067B	t_{PHZ}, t_{PLZ} (Figure 4)	5.0 10 15	250 120 75	625 300 190	ns
Any Pair of Address Inputs to Output MC14067B	t_{PLH}, t_{PHL}	5.0 10 15	280 115 85	700 290 215	ns
Second Harmonic Distortion (R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p})	—	10	0.3	—	%
ON Channel Bandwidth [R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{SS}$) p−p(sine−wave)] 20 Log10 (V_{out}/V_{in}) = − 3 dB MC14067B	BW (Figure 5)	10	15	—	MHz
Off Channel Feedthrough Attenuation [R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD}-V_{SS}$) p−p(sine−wave)] f_{in} = 20 MHz – MC14067B	— (Figure 5)	10	– 40	—	dB
Channel Separation [R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD}-V_{SS}$) p−p (sine−wave)] f_{in} = 20 MHz	— (Figure 6)	10	– 40	—	dB
Crosstalk, Control Inputs−to−Common O/I (R1 = 1 kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns, Inhibit = V_{SS})	— (Figure 7)	10	30	—	mV

5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

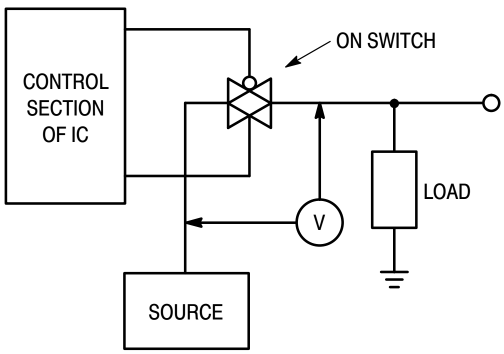


Figure 1. ΔV Across Switch

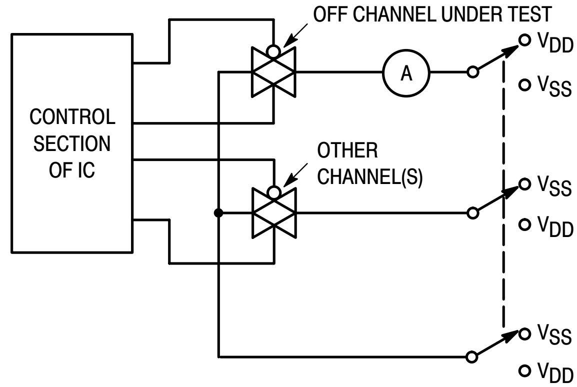


Figure 2. Off Channel Leakage

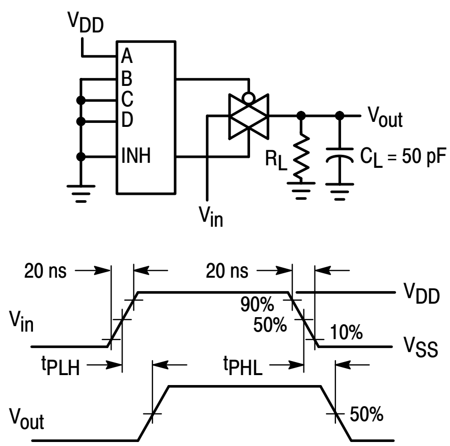


Figure 3. Propagation Delay Test Circuit and Waveforms V_{in} to V_{out}

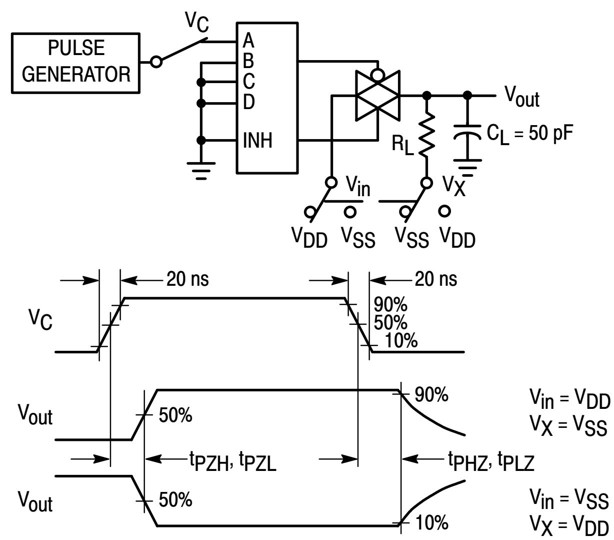


Figure 4. Turn−On and Delay Turn−Off Test Circuit and Waveforms

A, B, and C inputs used to turn ON or OFF the switch under test.

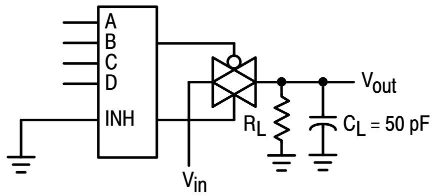


Figure 5. Bandwidth and Off−Channel Feedthrough Attenuation

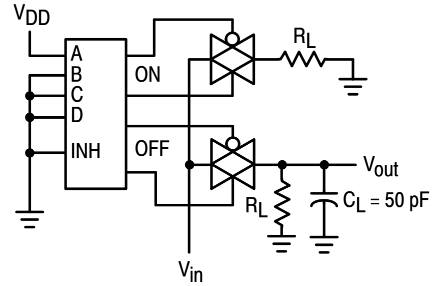


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

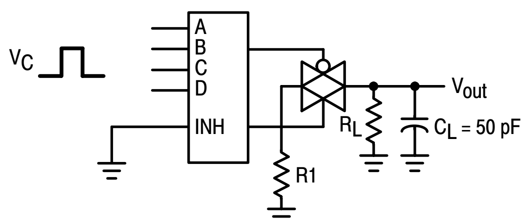


Figure 7. Crosstalk, Control to Common O/I

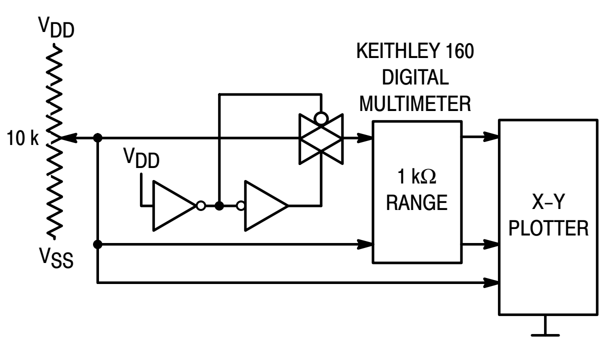


Figure 8. Channel Resistance (R_{ON}) Test Circuit

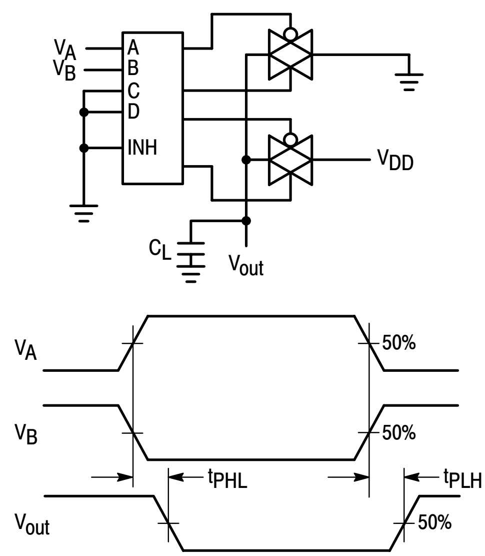


Figure 9. Propagation Delay, Any Pair of Address Inputs to Output

TYPICAL RESISTANCE CHARACTERISTICS

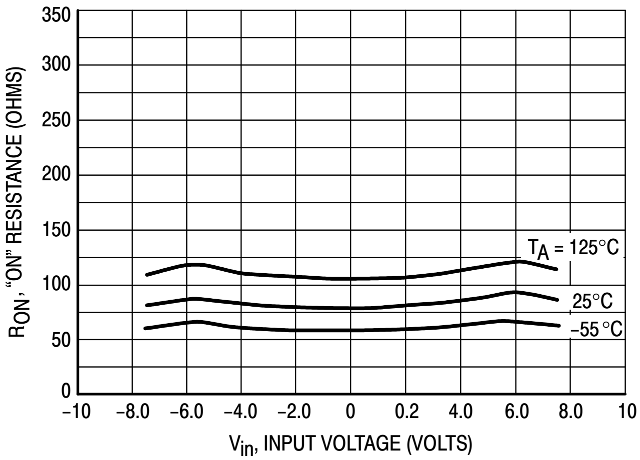


Figure 10. V_{DD} = 7.5 V, V_{SS} = − 7.5 V

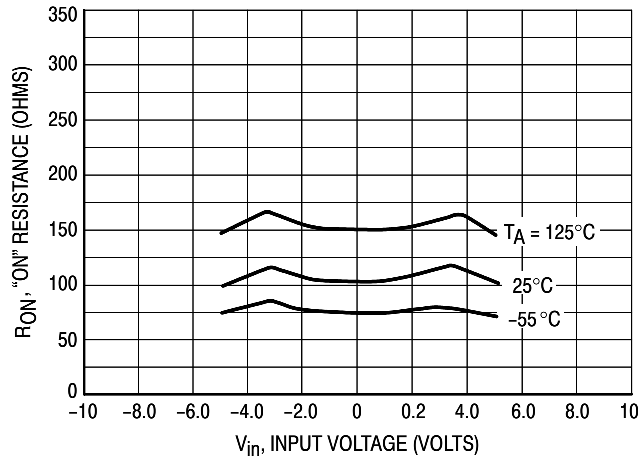


Figure 11. V_{DD} = 5.0 V, V_{SS} = − 5.0 V

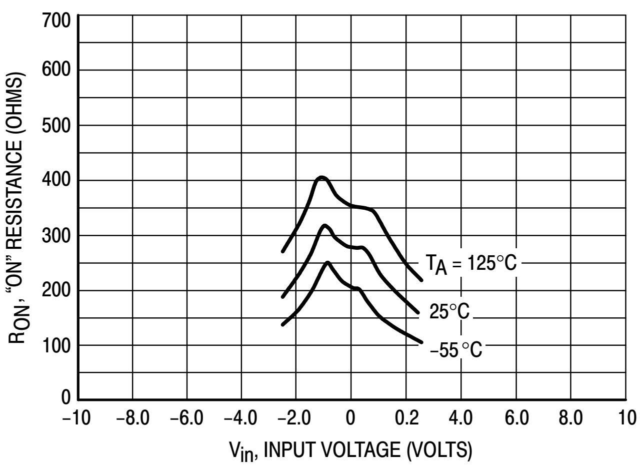


Figure 12. V_{DD} = 2.5 V, V_{SS} = − 2.5 V

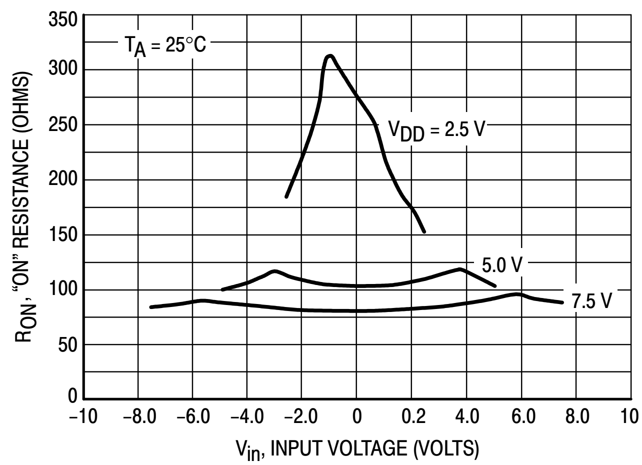


Figure 13. Comparison at 25°C, V_{DD} = −V_{SS}

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/Demultiplexer. The 0−to−5 volt Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example. V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}. The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V_{DD} and V_{SS}.

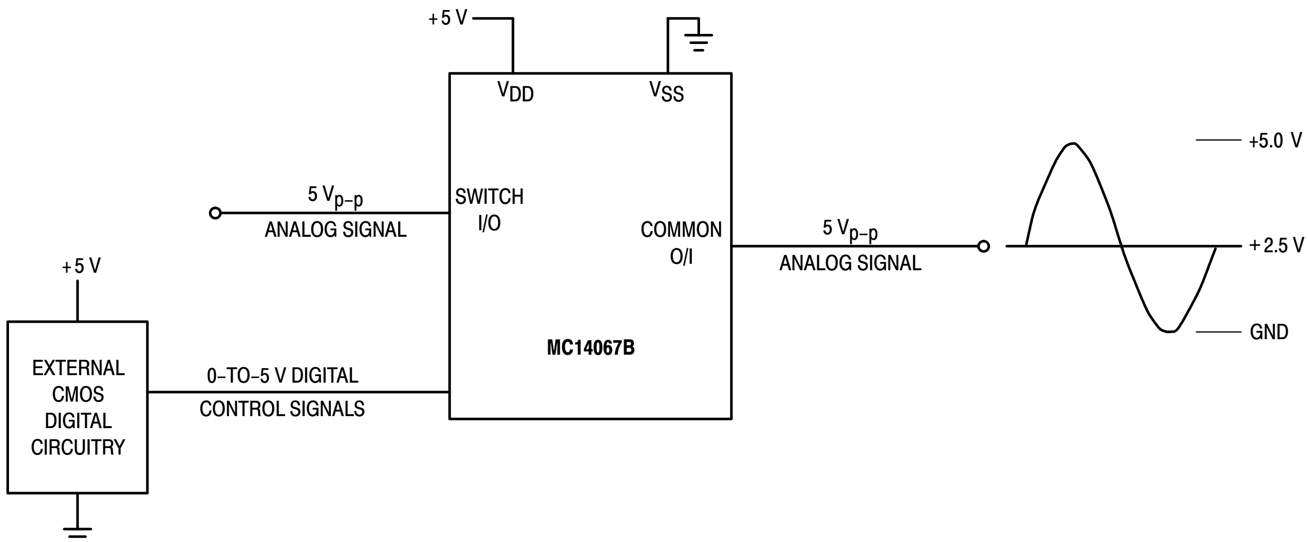


Figure A. Application Example

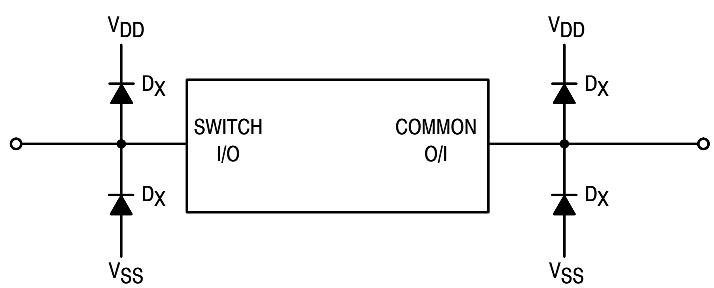


Figure B. External Germanium or Schottky Clipping Diodes

MC14069UB

Hex Inverter

The MC14069UB hex inverter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin−for−Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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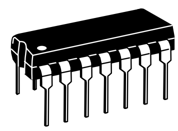
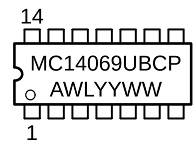
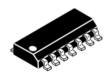
MARKING DIAGRAMS

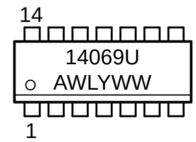


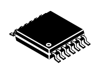
PDIP−14
P SUFFIX
CASE 646



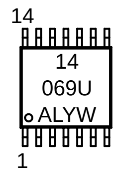


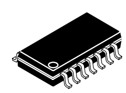
SOIC−14
D SUFFIX
CASE 751A



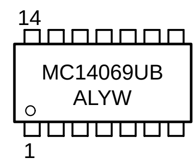


TSSOP−14
DT SUFFIX
CASE 948G





EIAJ SO−14
F SUFFIX
CASE 965



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14069UBCP	PDIP−14	2000/Box
MC14069UBD	SOIC−14	2750/Box
MC14069UBDR2	SOIC−14	2500/Tape & Reel
MC14069UBDT	TSSOP−14	96/Rail
MC14069UBDTEL	TSSOP−14	2000/Tape & Reel
MC14069UBDTR2	TSSOP−14	2500/Tape & Reel
MC14069UBF	EIAJ SO−14	See Note 1.
MC14069UBFEL	EIAJ SO−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

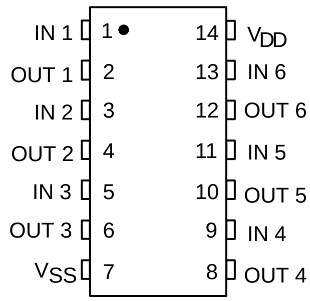


Figure 1. Pin Assignment

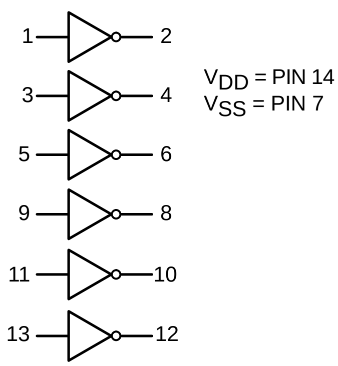
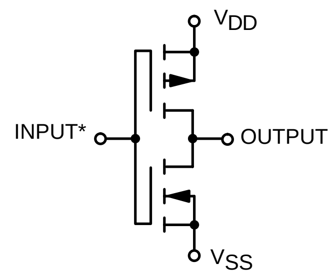


Figure 3. Logic Diagram



*Double diode protection on all inputs not shown

Figure 2. Circuit Schematic

(1/6 of circuit shown)

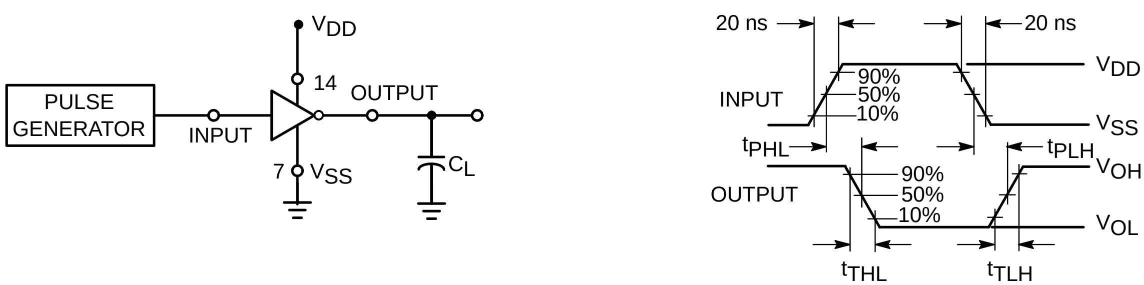


Figure 4. Switching Time Test Circuit and Waveforms

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
$V_{in} = V_{DD}$			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
$V_{in} = 0$	"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage	"0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)			5.0	—	1.0	—	2.25	1.0	—	1.0	
(V_O = 9.0 Vdc)			10	—	2.0	—	4.50	2.0	—	2.0	
(V_O = 13.5 Vdc)			15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)			5.0	4.0	—	4.0	2.75	—	4.0	—	
(V_O = 1.0 Vdc)			10	8.0	—	8.0	5.50	—	8.0	—	
(V_O = 1.5 Vdc)			15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)			5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)			10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)			15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current		I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
(Per Package)			10	—	0.5	—	0.0010	0.5	—	15	
			15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.)		I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/6							µAdc
(Dynamic plus Quiescent,			10	I_T = (0.6 µA/kHz) f + I_{DD}/6							
Per Gate) (C_L = 50 pF)			15	I_T = (0.9 µA/kHz) f + I_{DD}/6							
Output Rise and Fall Times (5.) (C_L = 50 pF)		t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns			5.0	—	—	—	100	200	—	—	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns			10	—	—	—	50	100	—	—	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns			15	—	—	—	40	80	—	—	
Propagation Delay Times (5.) (C_L = 50 pF)		t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns			5.0	—	—	—	65	125	—	—	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 22 ns			10	—	—	—	40	75	—	—	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 17 ns			15	—	—	—	30	55	—	—	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14070B, MC14077B

CMOS SSI

Quad Exclusive “OR” and “NOR” Gates

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B — Replacement for CD4030B and CD4070B Types
- MC14077B — Replacement for CD4077B Type

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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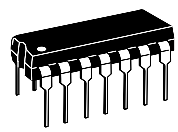
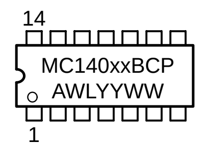
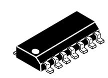
MARKING DIAGRAMS

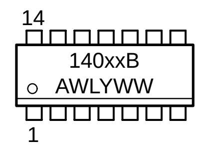


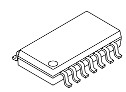
PDIP−14
P SUFFIX
CASE 646



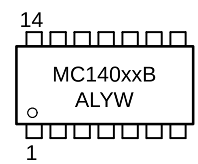


SOIC−14
D SUFFIX
CASE 751A





SOEIAJ−14
F SUFFIX
CASE 965



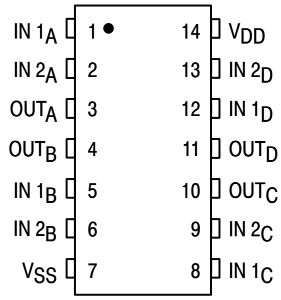
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC140XXBCP	PDIP−14	2000/Box
MC140XXBD	SOIC−14	2750/Box
MC140XXBDR2	SOIC−14	2500/Tape & Reel
MC140XXBF	SOEIAJ−14	See Note 1.
MC140XXBFEL	SOEIAJ−14	See Note 1.

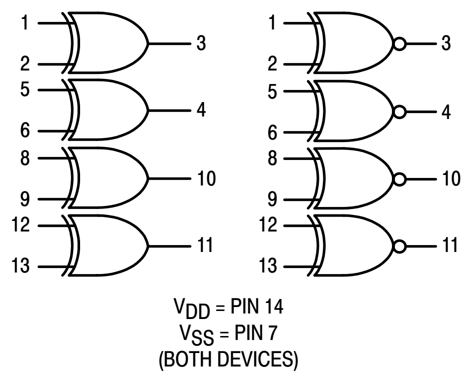
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

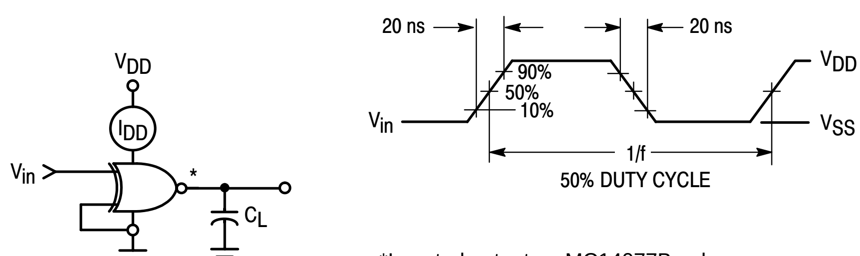
PIN ASSIGNMENT



MC14070B
QUAD Exclusive OR Gate

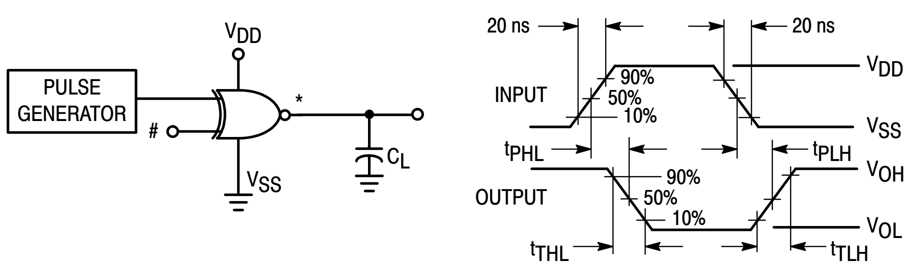
MC14077B
QUAD Exclusive NOR Gate





*Inverted output on MC14077B only.

Figure 1. Power Dissipation Test Circuit and Waveform



*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

Figure 2. Switching Time Test Circuit and Waveforms

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD} I_T = (0.6 µA/kHz) f + I_{DD} I_T = (0.9 µA/kHz) f + I_{DD}							µAdc
Output Rise and Fall Times (5.) (C_L = 50 pF) t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	— — —	100 50 40	200 100 80	— — —	— — —	ns
Propagation Delay Times (5.) (C_L = 50 pF) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 130 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 57 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		t_{PLH}, t_{PHL}	5.0 10 15	— — —	— — —	— — —	175 75 55	350 150 110	— — —	— — —	ns

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\text{ Vfk}$$

where: I_T is in µH (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14076B

4-Bit D-Type Register with Three-State Outputs

The MC14076B 4−Bit Register consists of four D−type flip−flops operating synchronously from a common clock. OR gated output−disable inputs force the outputs into a high−impedance state for use in bus organized systems. OR gated data−disable inputs cause the Q outputs to be fed back to the D inputs of the flip−flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master root is provided to clear all four flip−flops simultaneously independent of the clock or disable inputs.

- Three−State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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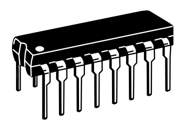
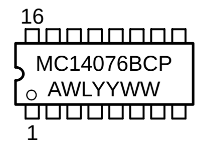
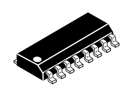
MARKING DIAGRAMS

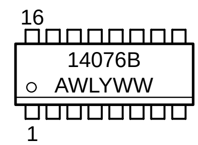


PDIP−16
P SUFFIX
CASE 648





SOIC−16
D SUFFIX
CASE 751B

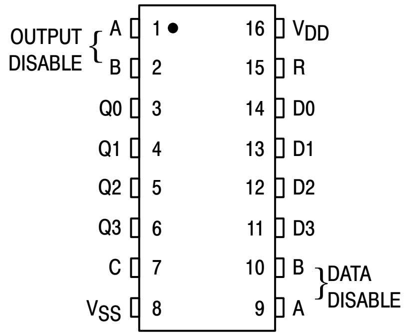


A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

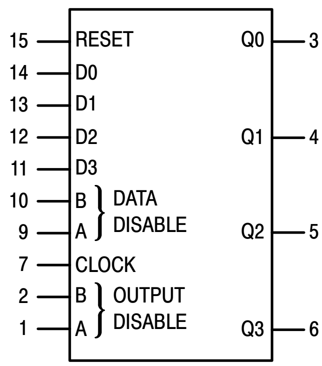
ORDERING INFORMATION

Device	Package	Shipping
MC14076BCP	PDIP−16	2000/Box
MC14076BD	SOIC−16	2400/Box
MC14076BDR2	SOIC−16	2500/Tape & Reel

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

FUNCTION TABLE

Inputs					Output Q
Reset	Clock	Data Disable A	Data Disable B	Data D	
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	⎍ (rising edge)	1	X	X	Q_n
0	⎍ (rising edge)	X	1	X	Q_n
0	⎍ (rising edge)	0	0	0	0
0	⎍ (rising edge)	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high−impedance state; however sequential operation of the flip−flops is not affected.
X = Don’t Care.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.75 µA/kHz) f + I_{DD} I_T = (1.50 µA/kHz) f + I_{DD} I_T = (2.25 µA/kHz) f + I_{DD}							µAdc
Three−State Leakage Current		I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	—	90	180	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	—	90	180	
3−State Propagation Delay, Output “1” or “0” to High Impedance	t_{PHZ}, t_{PLZ}	5.0 10 15	— — —	150 60 45	300 120 90	ns
3−State Propagation Delay, High Impedance to “1” or “0” Level	t_{PZH}, t_{PZL}	5.0 10 15	— — —	200 80 60	400 160 120	ns
Clock Pulse Width	t_{WH}	5.0 10 15	260 110 80	130 55 40	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	370 150 110	185 75 55	— — —	ns
Data Setup Time	t_{su}	5.0 10 15	30 10 4	15 5 2	— — —	ns
Data Hold Time	t_h	5.0 10 15	130 60 50	65 30 25	— — —	ns
Data Disable Setup Time	t_{su}	5.0 10 15	220 80 50	110 40 25	— — —	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	µs
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.6 9.0 12	1.8 4.5 6.0	MHz

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

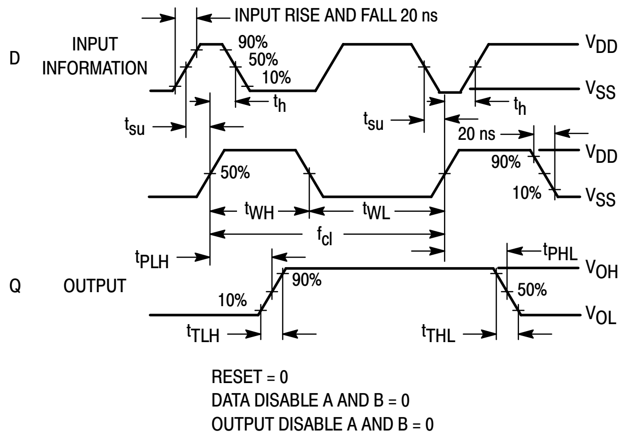


Figure 1. Timing Diagram

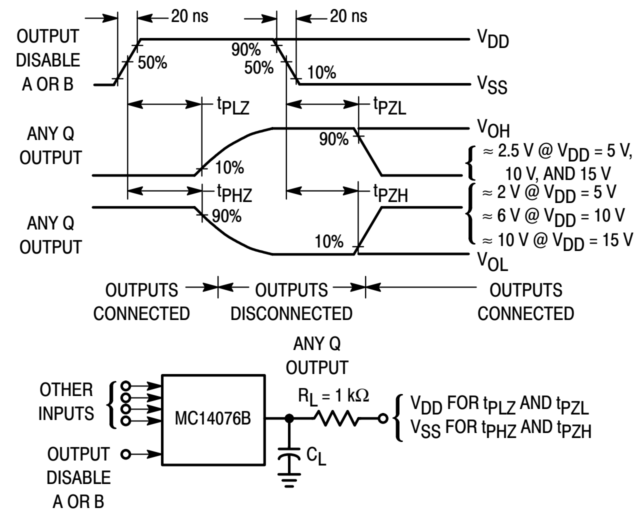
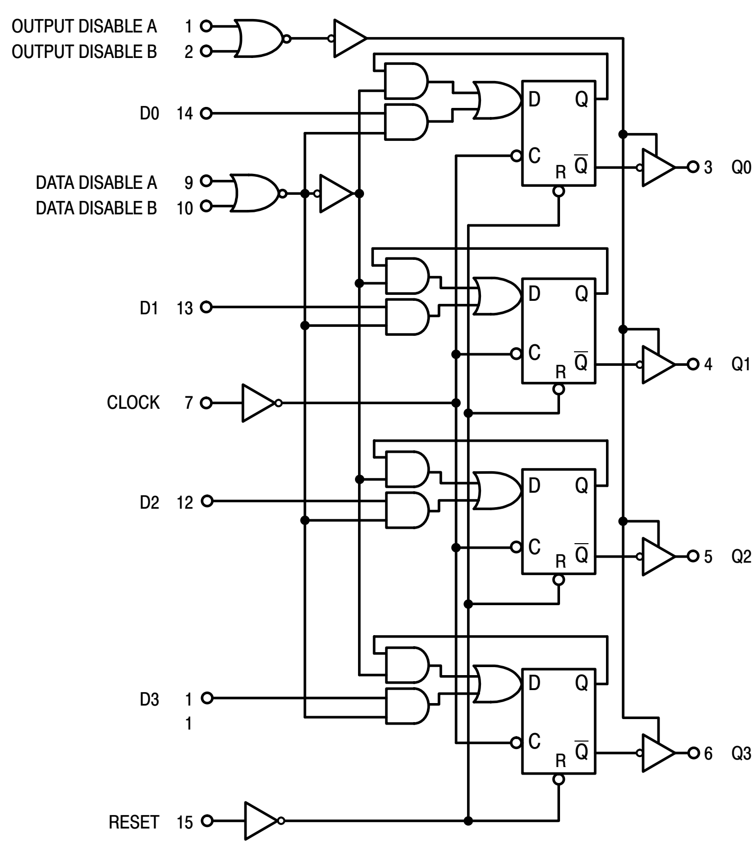


Figure 2. Three−State Propagation Delay Waveshape and Circuit

EQUIVALENT FUNCTIONAL BLOCK DIAGRAM



MC14093B

Quad 2-Input "NAND" Schmitt Trigger

The MC14093B Schmitt trigger is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2−input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin−for−Pin Compatible with CD4093
- Can be Used to Replace MC14011B
- Independent Schmitt−Trigger at each Input

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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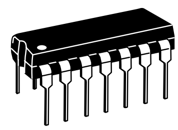
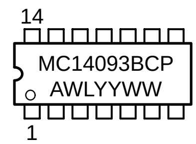
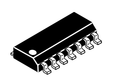
MARKING DIAGRAMS

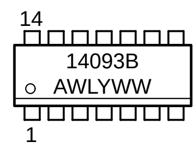


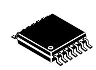
PDIP−14
P SUFFIX
CASE 646



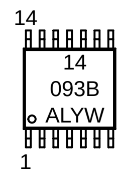


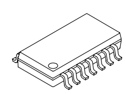
SOIC−14
D SUFFIX
CASE 751A



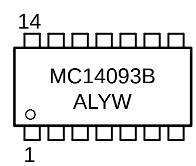


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965



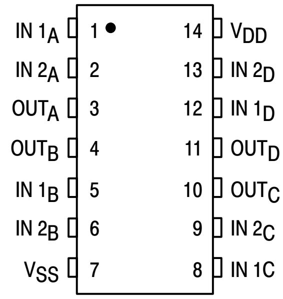
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

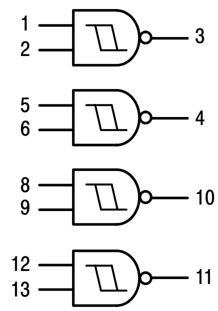
Device	Package	Shipping
MC14093BCP	PDIP−14	2000/Box
MC14093BD	SOIC−14	2750/Box
MC14093BDR2	SOIC−14	2500/Tape & Reel
MC14093BDT	TSSOP−14	96/Rail
MC14093BDTEL	TSSOP−14	2000/Tape & Reel
MC14093BDTR2	TSSOP−14	2500/Tape & Reel
MC14093BF	SOEIAJ−14	See Note 1.
MC14093BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



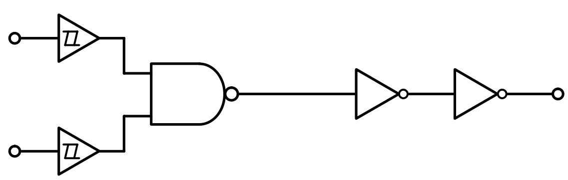
LOGIC DIAGRAM



V_{DD} = PIN 14
V_{SS} = PIN 7

EQUIVALENT CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ [4.]	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15				I_T = (1.2 µA/kHz) f + I_{DD} I_T = (2.4 µA/kHz) f + I_{DD} I_T = (3.6 µA/kHz) f + I_{DD}				µAdc
Hysteresis Voltage	V_H†	5.0 10 15	0.3 1.2 1.6	2.0 3.4 5.0	0.3 1.2 1.6	1.1 1.7 2.1	2.0 3.4 5.0	0.3 1.2 1.6	2.0 3.4 5.0	Vdc
Threshold Voltage Positive−Going	V_{T+}	5.0 10 15	2.2 4.6 6.8	3.6 7.1 10.8	2.2 4.6 6.8	2.9 5.9 8.8	3.6 7.1 10.8	2.2 4.6 6.8	3.6 7.1 10.8	Vdc
Negative−Going	V_{T-}	5.0 10 15	0.9 2.5 4.0	2.8 5.2 7.4	0.9 2.5 4.0	1.9 3.9 5.8	2.8 5.2 7.4	0.9 2.5 4.0	2.8 5.2 7.4	Vdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0 10 15	— — —	125 50 40	250 100 80	ns

7. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

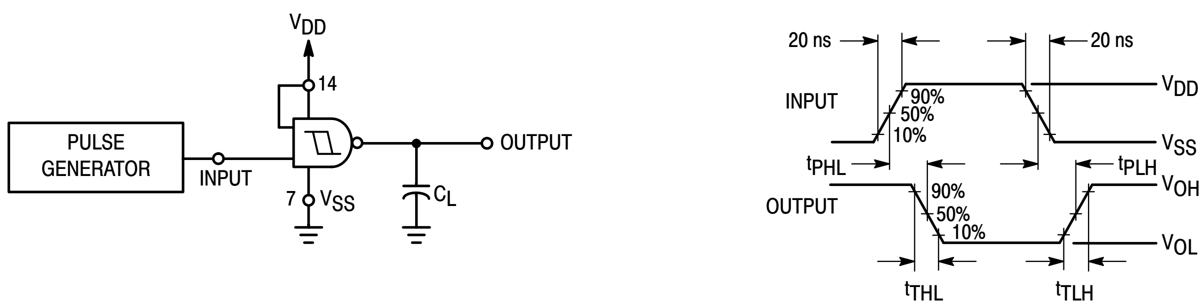
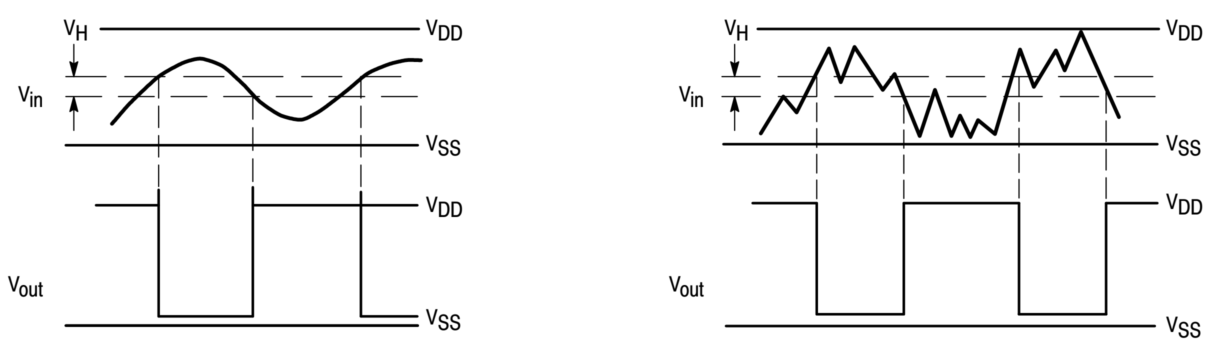


Figure 1. Switching Time Test Circuit and Waveforms



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 2. Typical Schmitt Trigger Applications

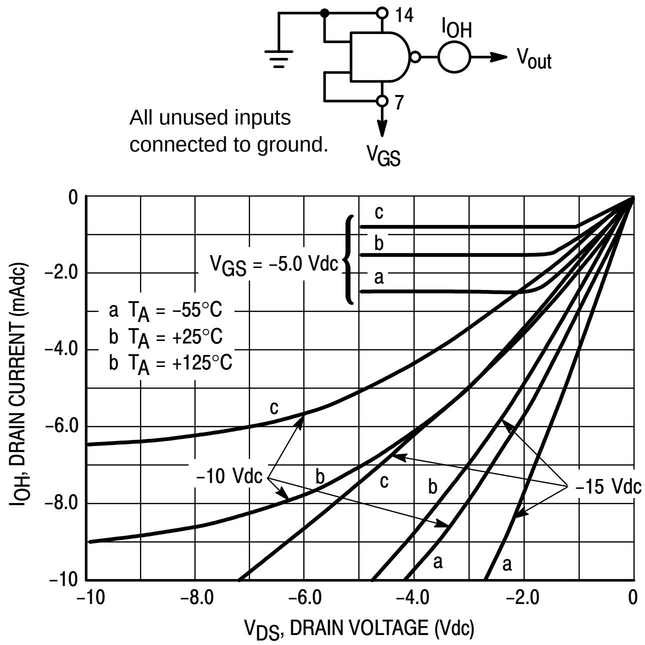


Figure 3. Typical Output Source Characteristics Test Circuit

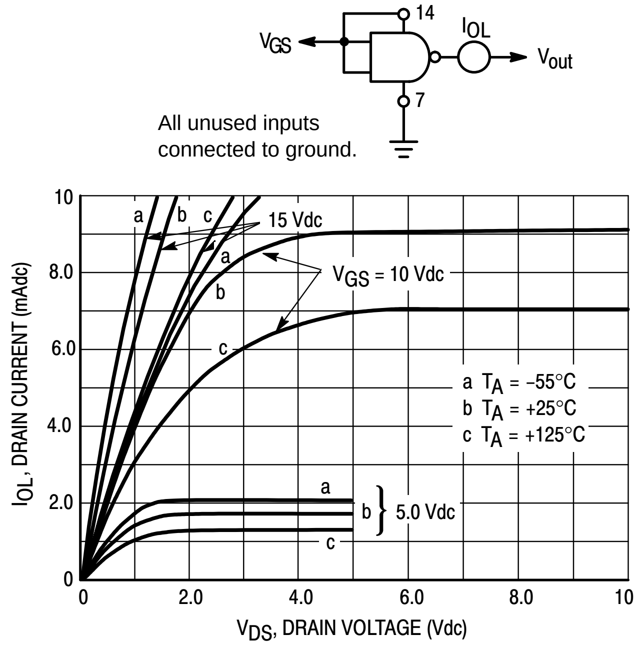


Figure 4. Typical Output Sink Characteristics Test Circuit

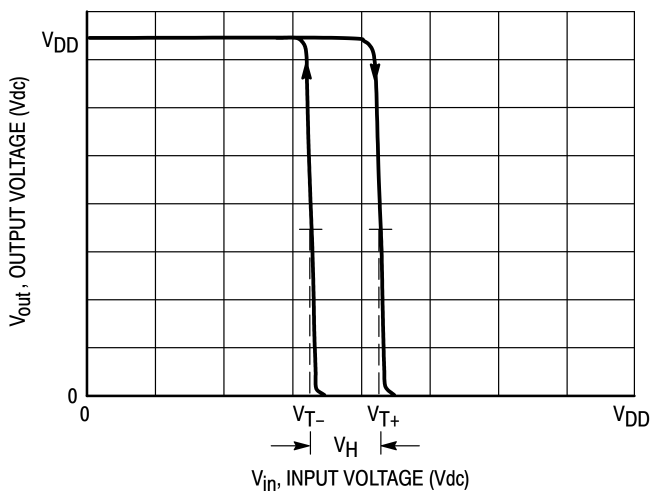


Figure 5. Typical Transfer Characteristics

8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8−stage shift register with a data latch for each stage and a three−state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high−speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low−speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three−state buffers which are placed in the high−impedance state by a logic Low on Output Enable.

- Three−State Outputs
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial−to−Parallel Data Conversion
- Pin−for−Pin Compatible with CD4094B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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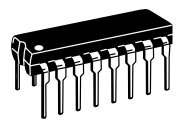
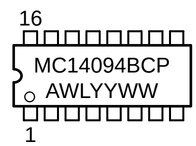
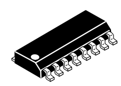
MARKING DIAGRAMS

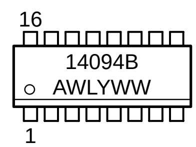


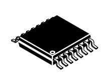
PDIP−16
P SUFFIX
CASE 648



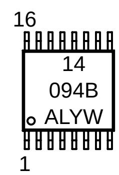


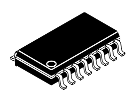
SOIC−16
D SUFFIX
CASE 751B



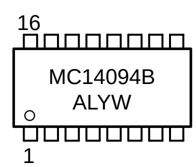


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

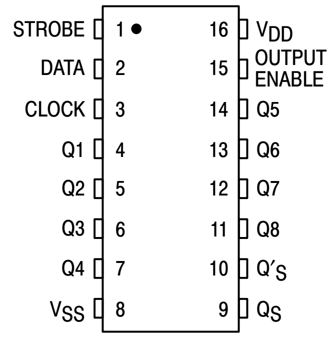
Device	Package	Shipping
MC14094BCP	PDIP−16	2000/Box
MC14094BD	SOIC−16	48/Rail
MC14094BDR2	SOIC−16	2500/Tape & Reel
MC14094BDT	TSSOP−16	96/Rail
MC14094BDTR2	TSSOP−16	2500/Tape & Reel
MC14094BF	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

AUGUST, 2000 − Rev. 4

Publication Order Number:
MC14094B/D

PIN ASSIGNMENT



Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q'_S
_/‾	0	X	X	Z	Z	Q7	No Chg.
‾_	0	X	X	Z	Z	No Chg.	Q7
_/‾	1	0	X	No Chg.	No Chg.	Q7	No Chg.
_/‾	1	1	0	0	Q_N-1	Q7	No Chg.
_/‾	1	1	1	1	Q_N-1	Q7	No Chg.
‾_	1	1	1	No Chg.	No Chg.	No Chg.	Q7

Z = High Impedance X = Don't Care

* At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (4.1 µA/kHz) f + I_{DD} I_T = (14 µA/kHz) f + I_{DD} I_T = (140 µA/kHz) f + I_{DD}							µAdc
3−State Output Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µA

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

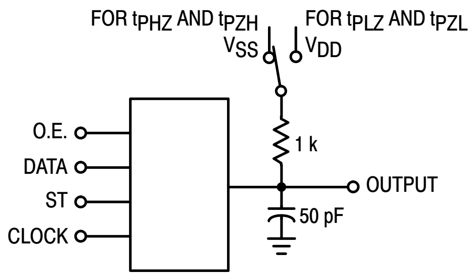
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

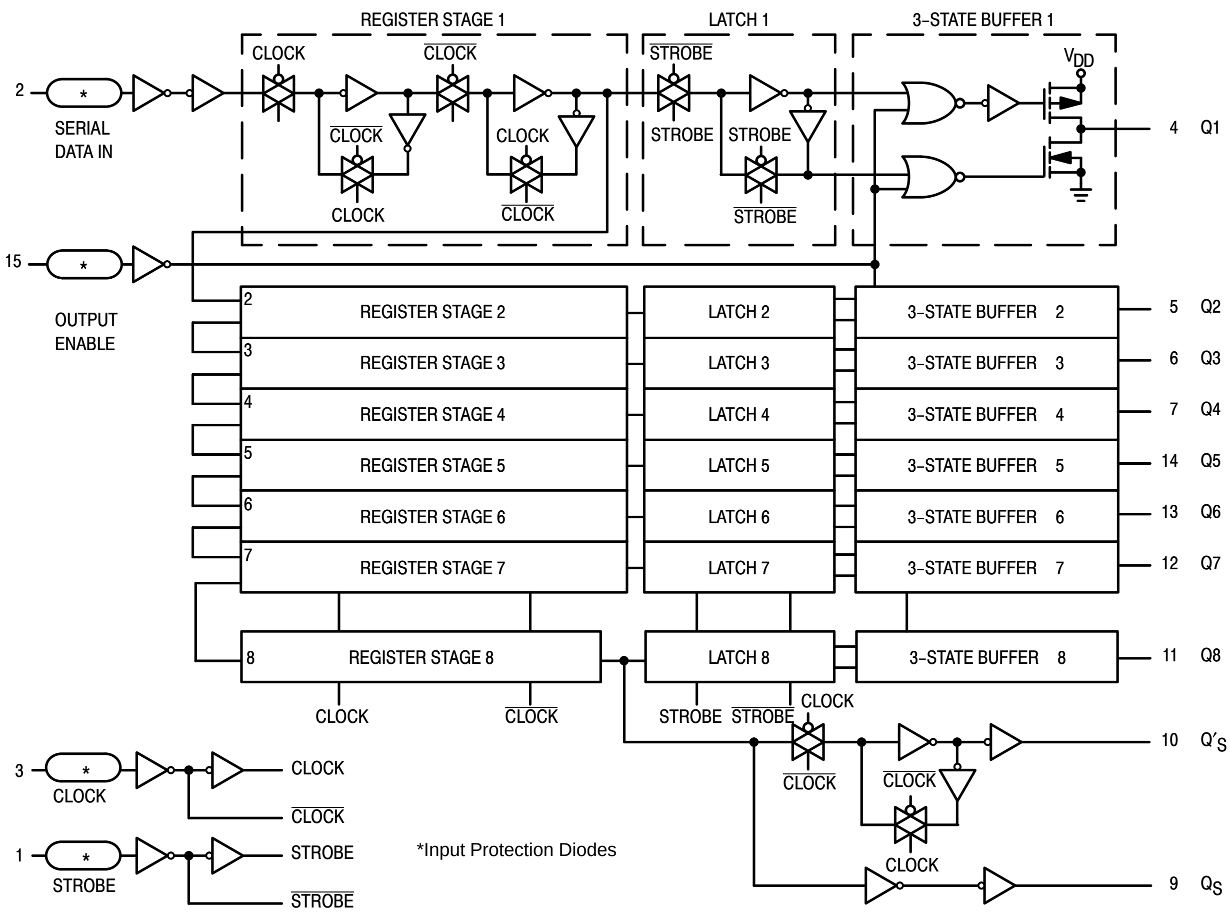
Characteristic	Symbol	V_{DD} Vdc	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Serial out QS						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	—	350	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C L + 82 ns		15	—	95	190	
Clock to Serial out Q'S						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 350 ns		5.0	—	230	460	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 149 ns		10	—	110	220	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	—	75	150	
Clock to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 375 ns		5.0	—	420	840	
t_{PLH}, t_{PHL} = (0.35 ns/pF) C_L + 177 ns		10	—	195	390	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 122 ns		15	—	135	270	
Strobe to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 245 ns		5.0	—	290	580	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C L + 127 ns		10	—	145	290	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	200	
Output Enable to Output						
t_{PHZ}, t_{PZL} = (0.90 ns/pF) C_L + 95 ns	t_{PHZ}, t_{PZL}	5.0	—	140	280	
t_{PHZ}, t_{PZL} = (0.36 ns/PF) C_L + 57 ns		10	—	75	150	
t_{PHZ}, t_{PZL} = (0.26 ns/pF) C_L + 42 ns		15	—	55	110	
t_{PLZ}, t_{PZH} = (0.90 ns/pF) C_L + 180 ns	t_{PLZ}, t_{PZH}	5.0	—	225	450	
t_{PLZ}, t_{PZH} = (0.36 ns/pF) C_L + 77 ns		10	—	95	190	
t_{PLZ}, t_{PZH} = (0.26 ns/pF) C_L + 57 ns		15	—	70	140	
Setup Time Data in to Clock	t_{su}	5.0 10 15	125 55 35	60 30 20	— — —	ns
Hold Time Clock to Data	t_h	5.0 10 15	0 20 20	– 40 – 10 0	— — —	ns
Clock Pulse Width, High	t_{WH}	5.0 10 15	200 100 83	100 50 40	— — —	ns
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5 10 15	— — —	— — —	15 5.0 4.0	µs
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 5.0 6.0	1.25 2.5 3.0	MHz
Strobe Pulse Width	t_{WL}	5.0 10 15	200 80 70	100 40 35	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3−STATE TEST CIRCUIT

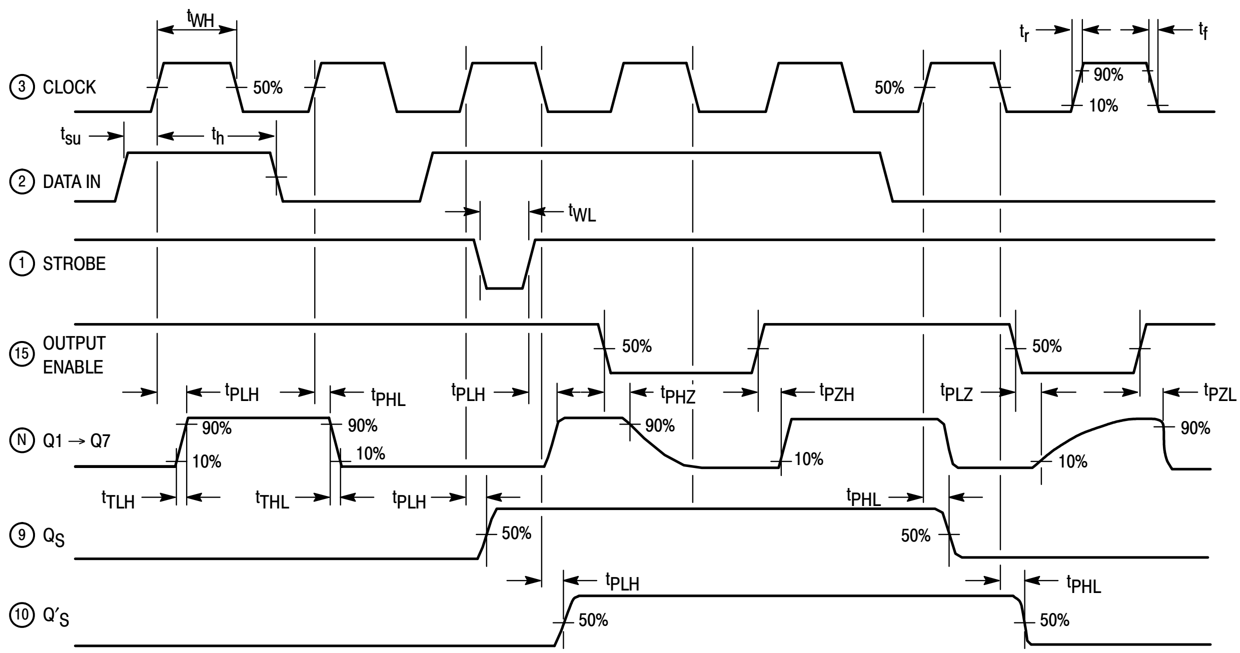


BLOCK DIAGRAM



*Input Protection Diodes

DYNAMIC TIMING DIAGRAM



MC14099B

8-Bit Addressable Latches

The MC14099B is an 8−bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. For the MC14099B the input is a unidirectional write only port.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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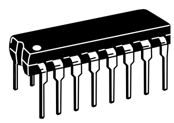
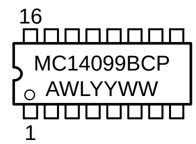
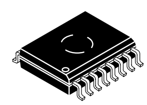
MARKING DIAGRAMS

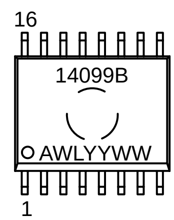


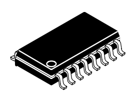
PDIP−16
P SUFFIX
CASE 648



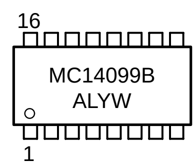


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



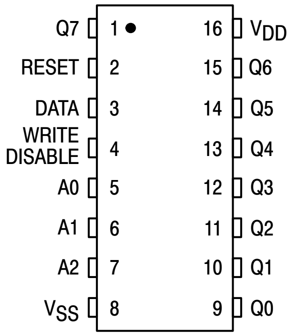
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

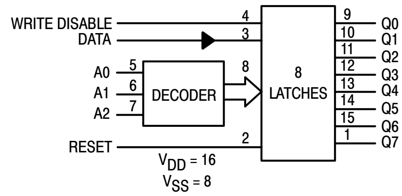
Device	Package	Shipping
MC14099BCP	PDIP−16	2000/Box
MC14099BDW	SOIC−16	2350/Box
MC14099BDWR2	SOIC−16	1000/Tape & Reel
MC14099BF	SOEIAJ−16	See Note 1.
MC14099BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



MC14099B



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	 5.0 10 15	 3.5 7.0 11	 — — —	 3.5 7.0 11	 2.75 5.50 8.25	 — — —	 3.5 7.0 11	 — — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Input Capacitance MC14599B — Data (pin 3) (V_{in} = 0)	C_{in}	—	—	—	—	15	22.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.5 µA/kHz) f + I_{DD} I_T = (3.0 µA/kHz) f + I_{DD} I_T = (4.5 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\ Vfk$$

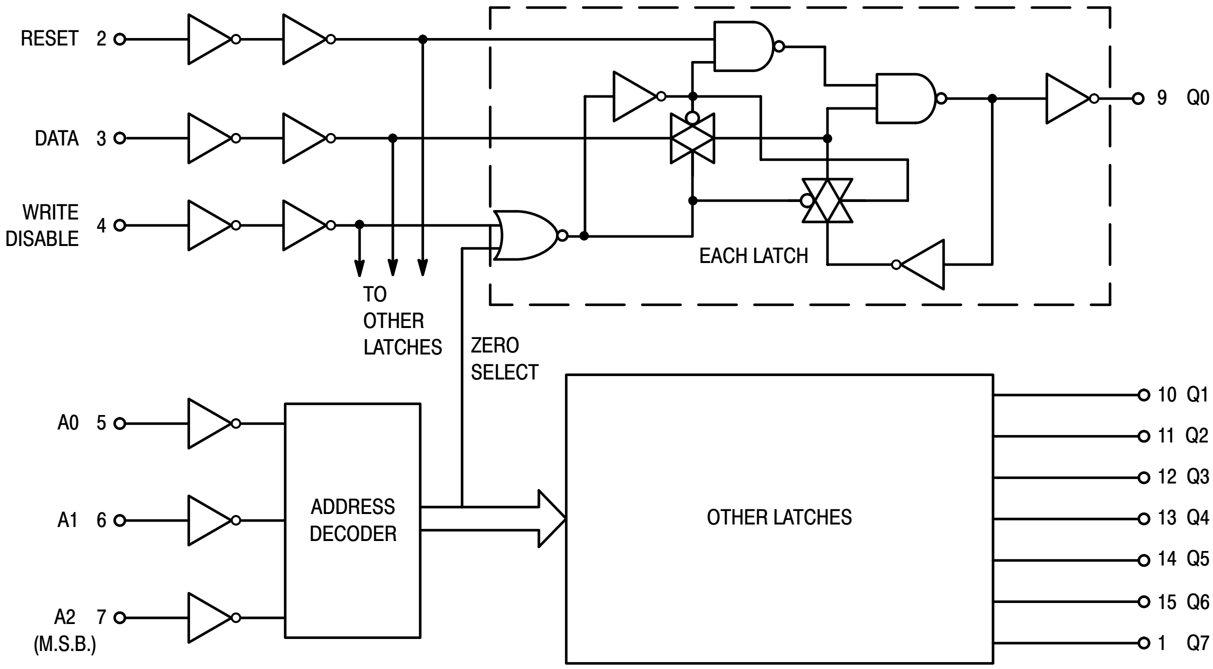
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PHL}, t_{PLH}					ns
Data to Output Q		5.0	—	200	400	
		10	—	75	150	
		15	—	50	100	
Write Disable to Output Q		5.0	—	200	400	ns
		10	—	80	160	
		15	—	60	120	
Reset to Output Q		5.0	—	175	350	ns
		10	—	80	160	
		15	—	65	130	
CE to Output Q (MC14599B only)		5.0	—	225	450	ns
		10	—	100	200	
		15	—	75	150	
Propagation Delay Time, MC14599B only	t_{PHL}, t_{PLH}					ns
Chip Enable, Write/$\overline{\text{Read}}$ to Data		5.0	—	200	400	
		10	—	80	160	
		15	—	65	130	
Address to Data		5.0	—	200	400	ns
		10	—	90	180	
		15	—	75	150	
Pulse Widths	$t_{w(H)}$, $t_{w(L)}$					ns
Reset		5.0	150	75	—	
		10	75	40	—	
		15	50	25	—	
Write Disable		5.0	320	160	—	ns
		10	160	80	—	
		15	120	60	—	
Set Up Time	t_{su}					ns
Data to Write Disable		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Hold Time	t_h					ns
Write Disable to Data		5.0	150	75	—	
		10	75	40	—	
		15	50	25	—	
Set Up Time	t_{su}	5.0	100	45	—	ns
Address to Write Disable		10	80	30	—	
		15	40	10	—	
Removal Time	t_{rem}	5.0	0	– 80	—	ns
Write Disable to Address		10	0	– 40	—	
		15	0	– 40	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

MC14099B
FUNCTION DIAGRAM



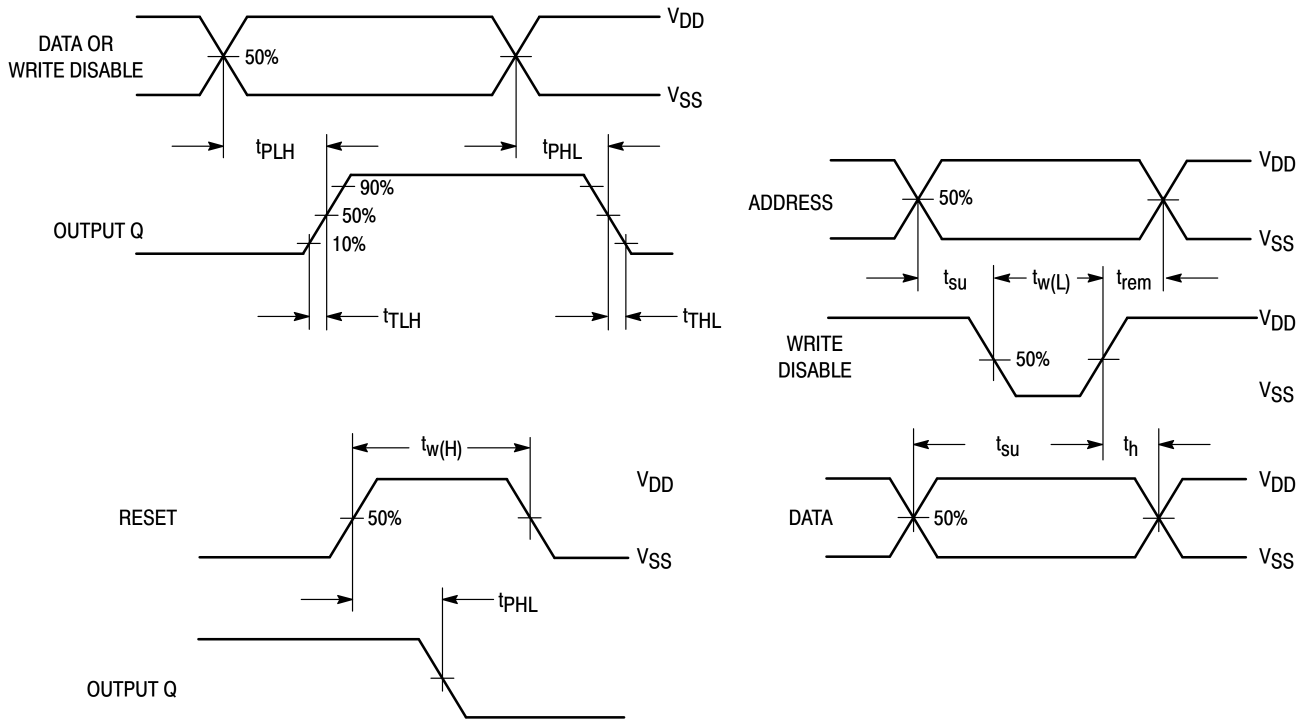
TRUTH TABLE

Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q_n*
0	1	Data	Reset †
1	0	Q_n*	Q_n*
1	1	Reset	Reset

*Q_n is previous state of latch.
†Reset to zero state.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

SWITCHING WAVEFORMS



MC14106B

Hex Schmitt Trigger

The MC14106B hex Schmitt Trigger is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to “square up” slowly changing waveforms.

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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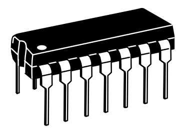
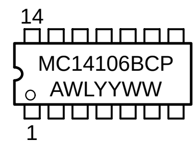
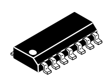
MARKING DIAGRAMS

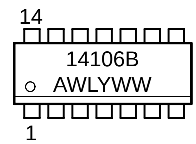


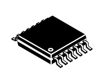
PDIP−14
P SUFFIX
CASE 646



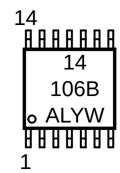


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G

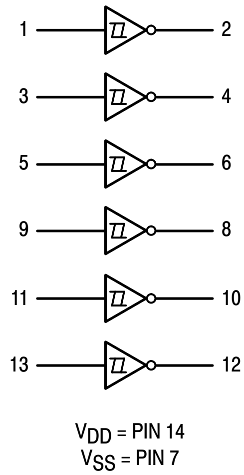


A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

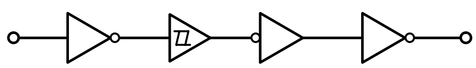
ORDERING INFORMATION

Device	Package	Shipping
MC14106BCP	PDIP−14	2000/Box
MC14106BD	SOIC−14	55/Rail
MC14106BDR2	SOIC−14	2500/Tape & Reel
MC14106BDT	TSSOP−14	96/Rail
MC14106BDTR2	TSSOP−14	2500/Tape & Reel

LOGIC DIAGRAM



EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD}	"0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
V_{in} = 0	"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Hysteresis Voltage		V_H (6.)	5.0	0.3	2.0	0.3	1.1	2.0	0.3	2.0	Vdc
			10	1.2	3.4	1.2	1.7	3.4	1.2	3.4	
			15	1.6	5.0	1.6	2.1	5.0	1.6	5.0	
Threshold Voltage Positive−Going		V_{T+}	5.0	2.2	3.6	2.2	2.9	3.6	2.2	3.6	Vdc
			10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
			15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
Negative−Going		V_{T-}	5.0	0.9	2.8	0.9	1.9	2.8	0.9	2.8	Vdc
			10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
			15	4.0	7.4	4.0	5.8	7.4	4.0	7.4	
Output Drive Current (V_{OH} = 2.5 Vdc)	Source	I_{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
(V_{OH} = 4.6 Vdc)			5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)			10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)			15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
			10	—	0.5	—	0.0010	0.5	—	15	
			15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	I_T = (1.8 µA/kHz) f + I_{DD}							µAdc
			10	I_T = (3.6 µA/kHz) f + I_{DD}							
			15	I_T = (5.4 µA/kHz) f + I_{DD}							

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\text{ Vfk}$$

where I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

6. $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less that $V_{T+\,max} - V_{T-\,min}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0 10 15	— — —	125 50 40	250 100 80	ns

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

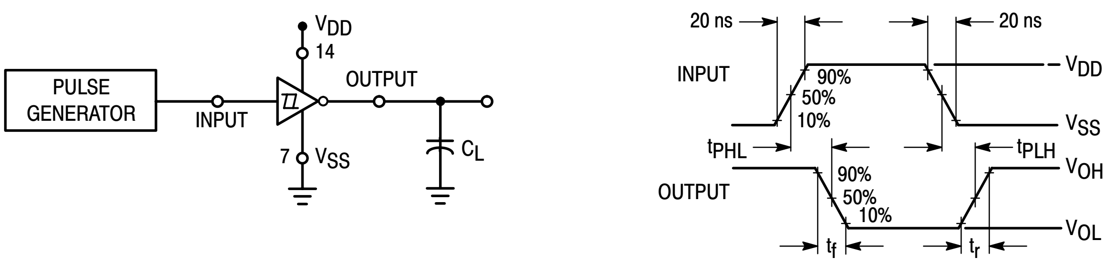


Figure 1. Switching Time Test Circuit and Waveforms

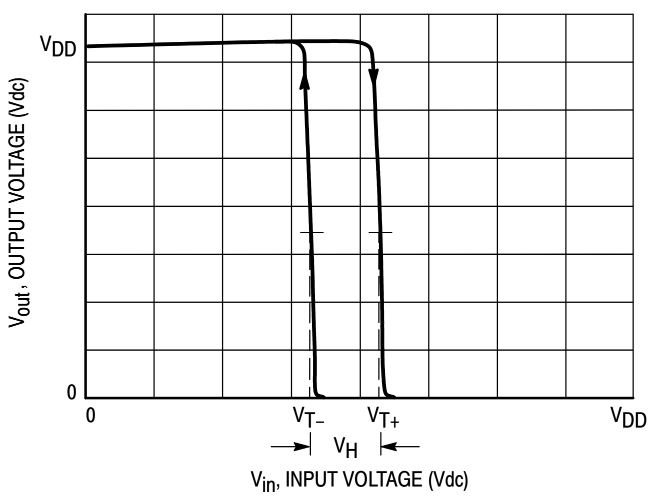
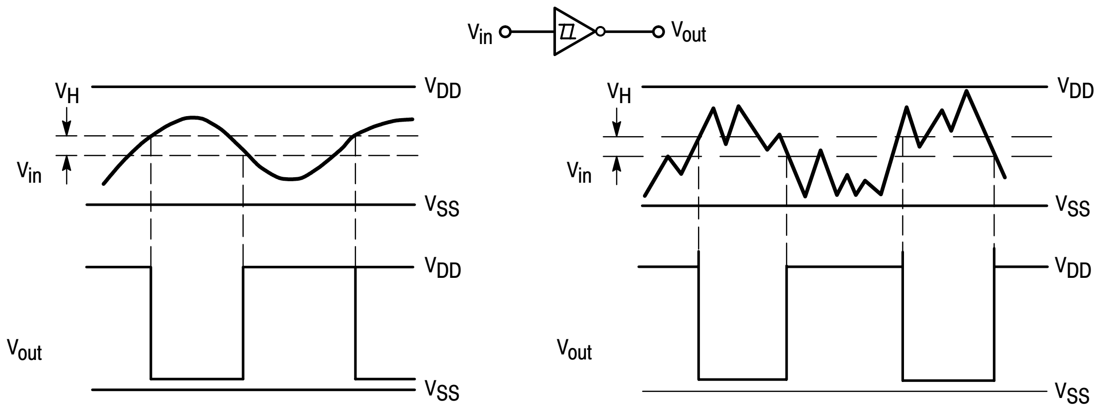


Figure 2. Typical Transfer Characteristics

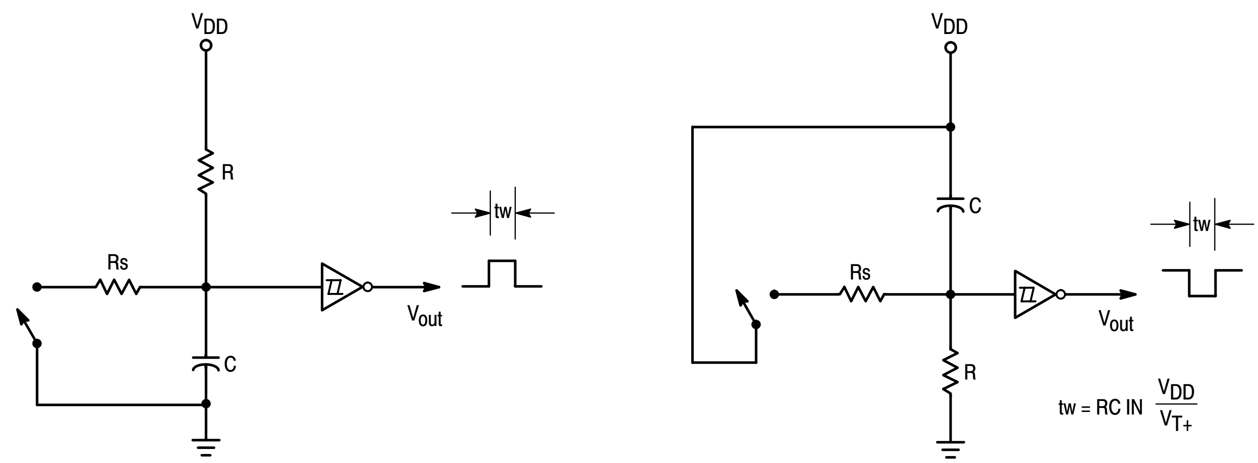
APPLICATIONS



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

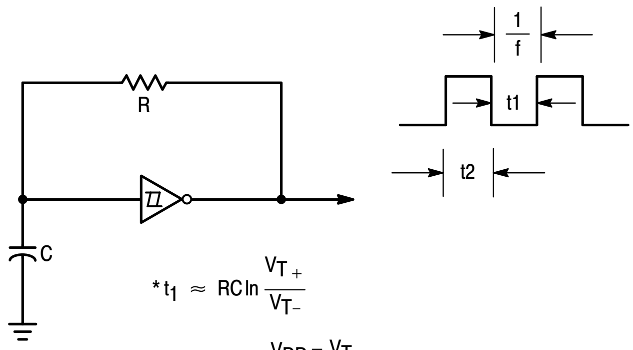
(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 3.



Useful as Pushbutton/Keyboard Debounce Circuit.

Figure 4. Monostable Multivibrator



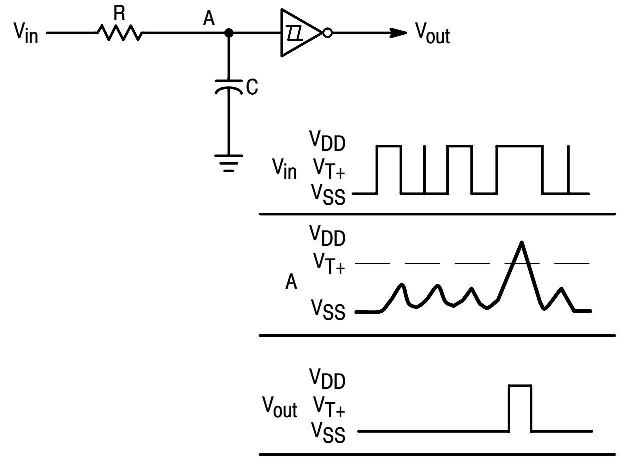
$$^{*}t_1 \approx RC\ln\frac{V_{T+}}{V_{T-}}$$

$$^{*}t_2 \approx RC\ln\frac{V_{DD}-V_{T-}}{V_{DD}-V_{T+}}$$

$$\frac{1}{f} \approx RC\ln\left[\left(\frac{V_{DD}-V_{T-}}{V_{DD}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]$$

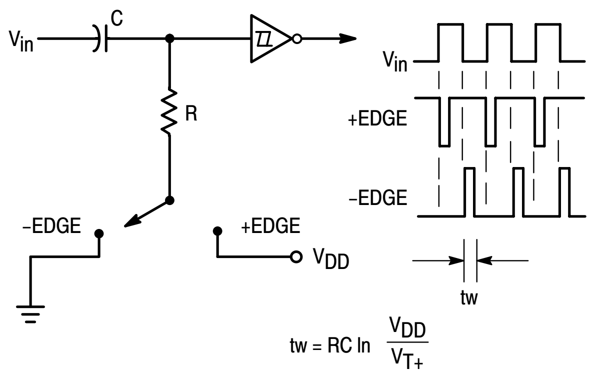
$$^{*}t_1 + t_2 \gg t_{PHL} + t_{PLH}$$

Figure 5. Astable Multivibrator



Useful in discriminating against short pulse durations.

Figure 6. Integrator



Useful as an edge detector circuit.

Figure 7. Differentiator

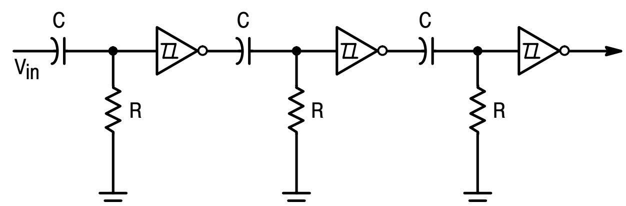


Figure 8. Positive Edge Time Delay Circuit

MC1413, MC1413B, NCV1413B

High Voltage, High Current Darlington Transistor Arrays

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 500 mA permit them to drive incandescent lamps.

The MC1413, B with a 2.7 kΩ series input resistor is well suited for systems utilizing a 5.0 V TTL or CMOS Logic.

Features

- Pb−Free Packages are Available*

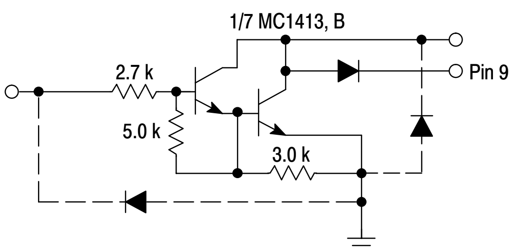
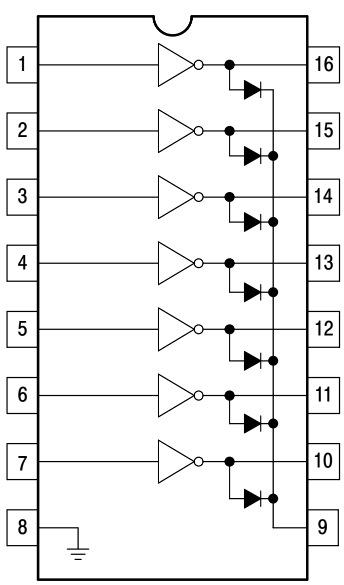


Figure 1. Representative Schematic Diagram



(Top View)

Figure 2. PIN CONNECTIONS

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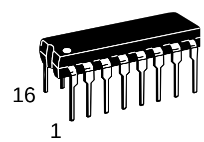
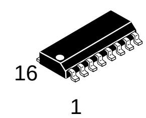


PDIP−16
P SUFFIX
CASE 648



SOIC−16
D SUFFIX
CASE 751B

ORDERING INFORMATION

Device	Package	Shipping†
MC1413D	SOIC−16	48 Units/Rail
MC1413DR2	SOIC−16	2500 Tape & Reel
MC1413DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC1413P	PDIP−16	500 Units/Rail
MC1413PG	PDIP−16 (Pb−Free)	500 Units/Tubes
MC1413BD	SOIC−16	48 Units/Rail
MC1413BDR2	SOIC−16	2500 Tape & Reel
MC1413BDR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC1413BP	PDIP−16	500 Units/Rail
NCV1413BDR2	SOIC−16	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 214 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

April, 2004 − Rev. 6

Publication Order Number:
MC1413/D

MAXIMUM RATINGS (T_A = 25°C, and rating apply to any one device in the package, unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage	V_I	30	V
Collector Current − Continuous	I_C	500	mA
Base Current − Continuous	I_B	25	mA
Operating Ambient Temperature Range MC1413 MC1413B NCV1413B	T_A	 −20 to +85 −40 to +85 −40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C
Thermal Resistance, Junction−to−Ambient Case 648, P Suffix Case 751B, D Suffix	$R\theta_{JA}$	 67 100	°C/W
Thermal Resistance, Junction−to−Case Case 648, P Suffix Case 751B, D Suffix	$R\theta_{JC}$	 22 20	°C/W
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM) Charged Device Model (CDM)	ESD	 2000 400 1500	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (V_O = 50 V, T_A = +85°C) (V_O = 50 V, T_A = +25°C)	 All Types All Types	I_{CEX}	 − −	 − −	 100 50	μA
Collector−Emitter Saturation Voltage (I_C = 350 mA, I_B = 500 μA) (I_C = 200 mA, I_B = 350 μA) (I_C = 100 mA, I_B = 250 μA)	 All Types All Types All Types	$V_{CE(sat)}$	 − − −	 1.1 0.95 0.85	 1.6 1.3 1.1	V
Input Current − On Condition (V_I = 3.85 V)	 MC1413, B	$I_{I(on)}$	 −	 0.93	 1.35	mA
Input Voltage − On Condition (V_{CE} = 2.0 V, I_C = 200 mA) (V_{CE} = 2.0 V, I_C = 250 mA) (V_{CE} = 2.0 V, I_C = 300 mA)	 MC1413, B MC1413, B MC1413, B	$V_{I(on)}$	 − − −	 − − −	 2.4 2.7 3.0	V
Input Current − Off Condition (I_C = 500 μA, T_A = 85°C)	All Types	$I_{I(off)}$	50	100	−	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)		h_{FE}	1000	−	−	−
Input Capacitance		C_I	−	15	30	pF
Turn−On Delay Time (50% E_I to 50% E_O)		t_{on}	−	0.25	1.0	μs
Turn−Off Delay Time (50% E_I to 50% E_O)		t_{off}	−	0.25	1.0	μs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C T_A = +85°C	I_R	− −	− −	50 100	μA
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	−	1.5	2.0	V

NOTE: NCV1413B T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

TYPICAL PERFORMANCE CURVES − T_A = 25°C

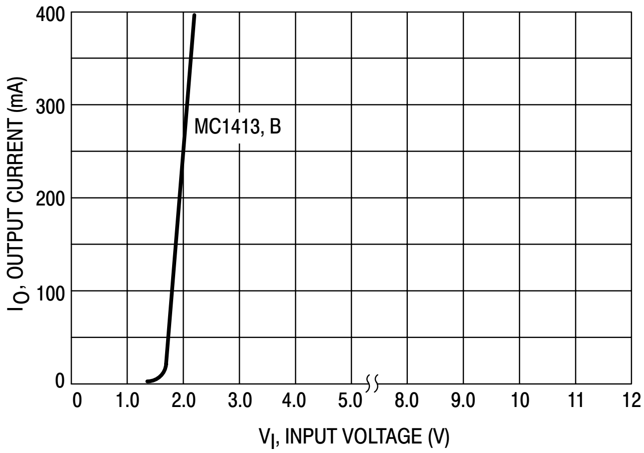


Figure 3. Output Current versus Input Voltage

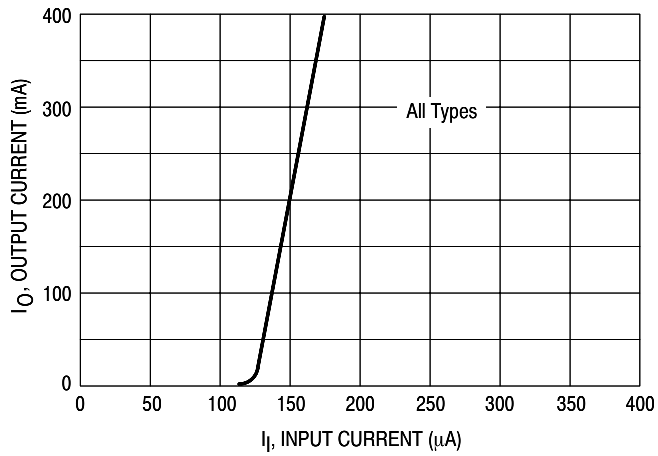


Figure 4. Output Current versus Input Current

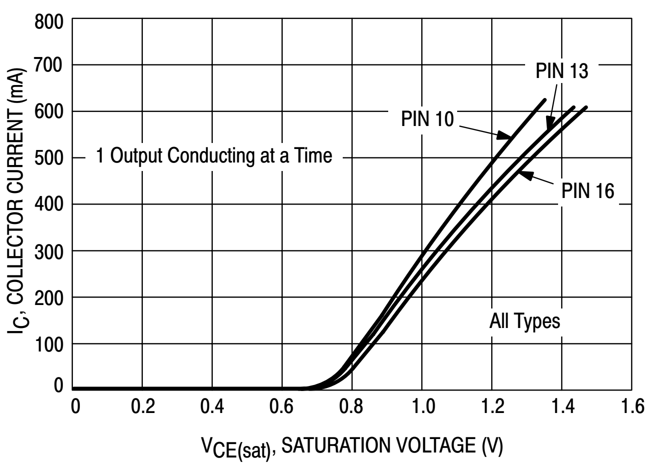


Figure 5. Typical Output Characteristics

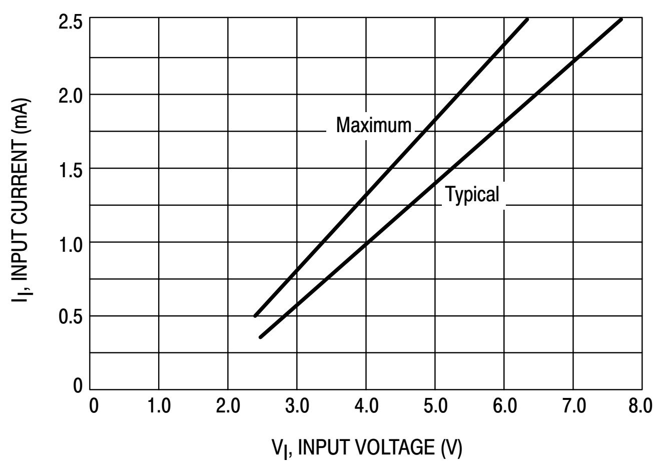


Figure 6. Input Characteristics − MC1413, B

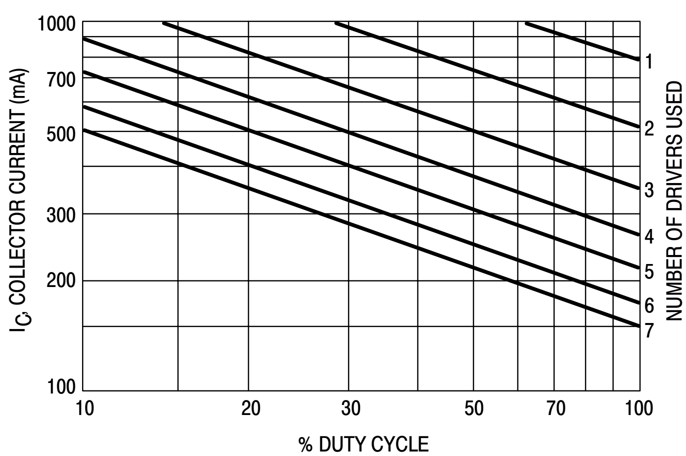
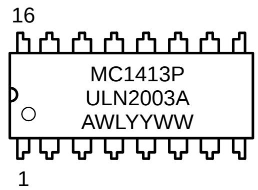
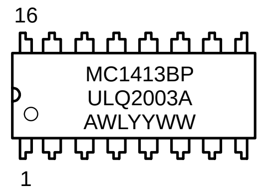


Figure 7. Maximum Collector Current versus Duty Cycle (and Number of Drivers in Use)

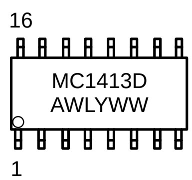
MARKING DIAGRAMS

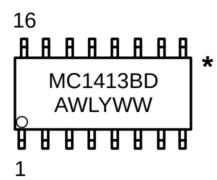
PDIP−16
P SUFFIX
CASE 648





SOIC−16
D SUFFIX
CASE 751B





A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week

*This marking diagram also applies to NCV1413B.

MC14174B

Hex Type D Flip-Flop

The MC14174B hex type D flip−flop is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip−flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- Functional Equivalent to TTL 74174

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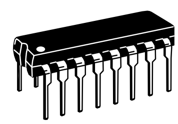
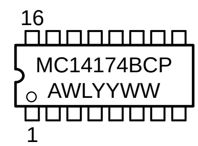
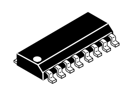
MARKING DIAGRAMS

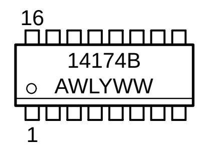


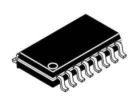
PDIP−16
P SUFFIX
CASE 648



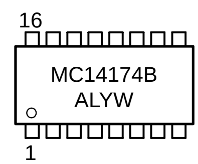


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

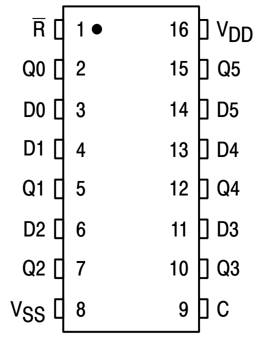
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

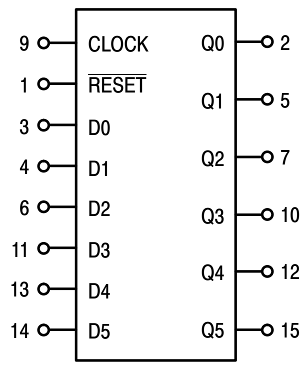
Device	Package	Shipping
MC14174BCP	PDIP−16	2000/Box
MC14174BD	SOIC−16	48/Rail
MC14174BDR2	SOIC−16	2500/Tape & Reel
MC14174BF	SOEIAJ−16	See Note 1.
MC14174BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

TRUTH TABLE
(Positive Logic)

Inputs			Output	
Clock	**Data**	**Reset** (overbar)	**Q**	
↑ (rising edge)	0	1	0	
↑ (rising edge)	1	1	1	
↓ (falling edge)	X	1	Q	No Change
X	X	0	0	

X = Don’t Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.1 µA/kHz) f + I_{DD} I_T = (2.3 µA/kHz) f + I_{DD} I_T = (3.7 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

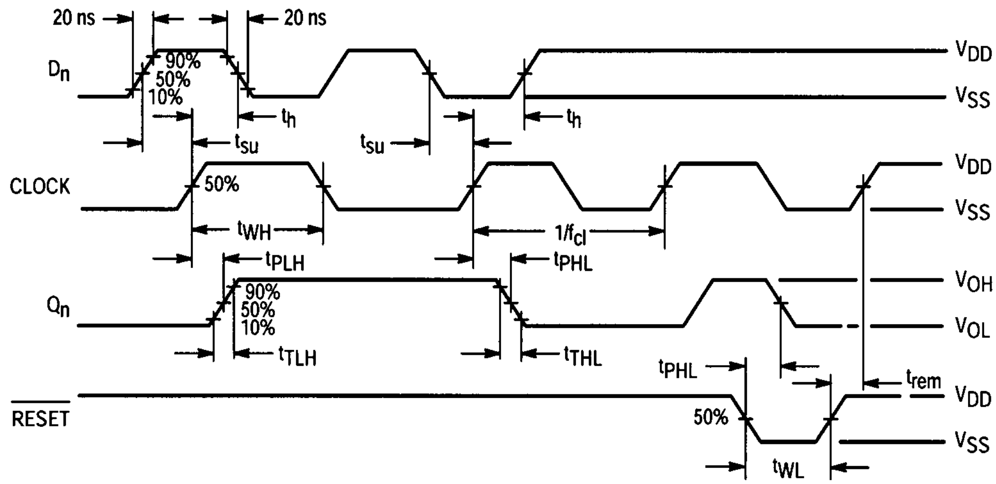
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

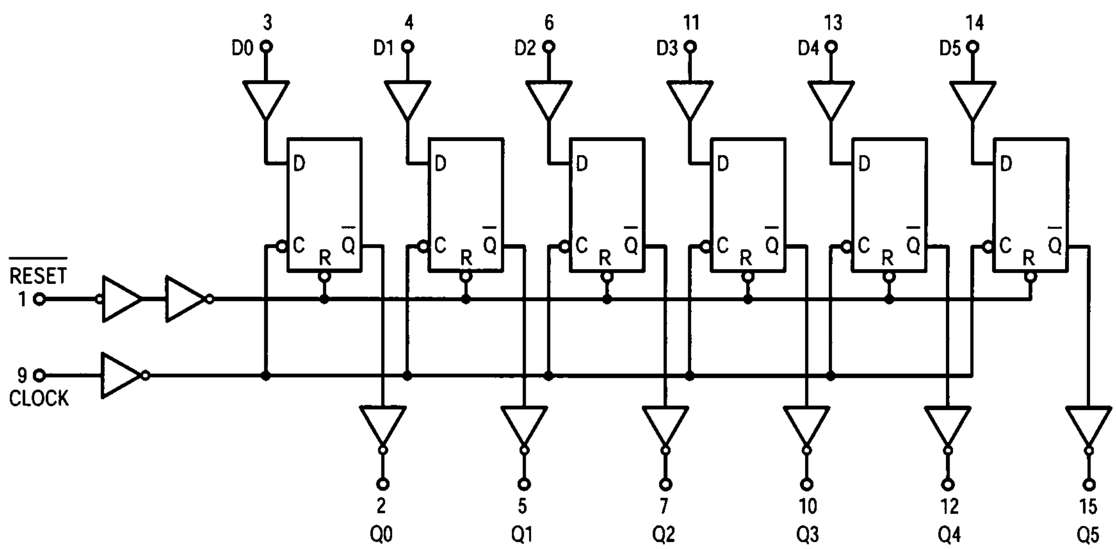
Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time — Clock to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 165 ns		5.0	—	210	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 64 ns		10	—	85	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 52 ns		15	—	65	120	
Propagation Delay Time — Reset to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 205 ns		5.0	—	250	500	
t_{PHL} = (0.36 ns/pF) C_L + 79 ns		10	—	100	200	
t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	—	75	150	
Clock Pulse Width	t_{WH}	5.0	150	75	—	ns
		10	90	45	—	
		15	70	35	—	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	
Clock Pulse Frequency	f_{cl}	5.0	—	7.0	2.0	mHz
		10	—	12	5.0	
		15	—	15.5	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5.0	
		15	—	—	4.0	
Data Setup Time	t_{su}	5.0	40	20	—	ns
		10	20	10	—	
		15	15	0	—	
Data Hold Time	t_h	5.0	80	40	—	ns
		10	40	20	—	
		15	30	15	—	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	250	125	—	ns
		10	100	50	—	
		15	80	40	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MC14175B

Quad Type D Flip-Flop

The MC14175B quad type D flip−flop is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each of the four flip−flops is positive−edge triggered by a common clock input (C). An active−low reset input (R) asynchronously resets all flip−flops. Each flip−flop has independent Data (D) inputs and complementary outputs (Q and Q). These devices may be used as shift register elements or as type T flip−flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low−Power TTL Loads or One Low−Power Schottky TTL Load
- Functional Equivalent to TTL 74175

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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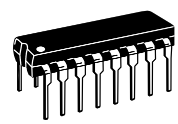
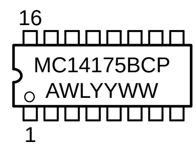
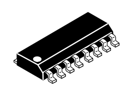
MARKING DIAGRAMS

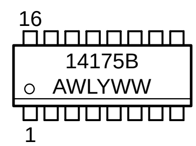


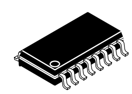
PDIP−16
P SUFFIX
CASE 648



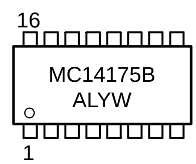


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



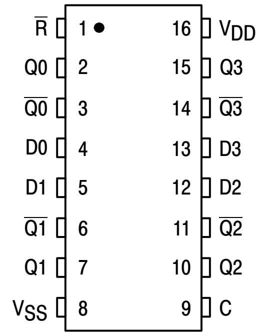
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

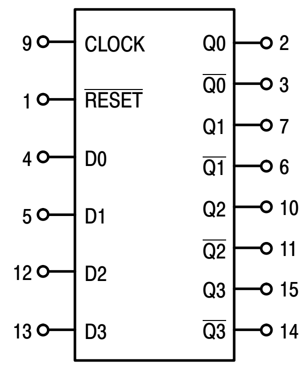
Device	Package	Shipping
MC14175BCP	PDIP−16	2000/Box
MC14175BD	SOIC−16	48/Rail
MC14175BDR2	SOIC−16	2500/Tape & Reel
MC14175BF	SOEIAJ−16	See Note 1.
MC14175BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

TRUTH TABLE

Inputs			Outputs		
Clock	**Data**	**$\overline{\text{Reset}}$**	**Q**	**Q**	
↑	0	1	0	1	
↑	1	1	1	0	
↓	X	1	Q	Q	No Change
X	X	0	0	1	

X = Don't Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.7 µA/kHz) f + I_{DD} I_T = (3.4 µA/kHz) f + I_{DD} I_T = (5.0 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

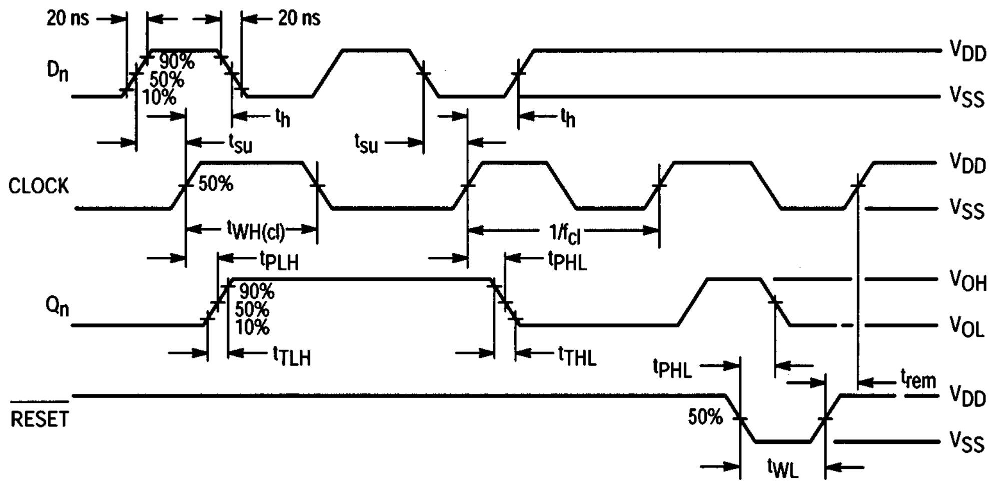
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

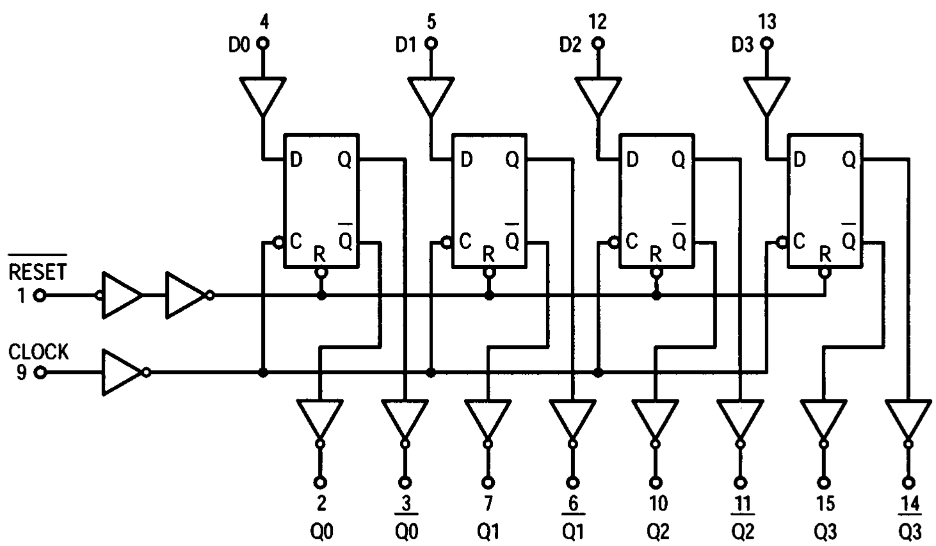
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time — Clock to Q, Q t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 220 90 70	 400 160 120	ns
Propagation Delay Time — Reset to Q, Q t_{PHL} = (0.9 ns/pF) C_L + 280 ns t_{PHL} = (0.36 ns/pF) C_L + 112 ns t_{PHL} = (0.26 ns/pF) C_L + 87 ns	t_{PHL}, t_{PLH}	 5.0 10 15	 — — —	 325 130 100	 500 200 150	ns
Clock Pulse Width	t_{WH}	5.0 10 15	250 100 75	110 45 35	— — —	ns
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0 10 15	200 80 60	100 40 30	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	4.5 11 14	2.0 5.0 6.5	mHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Data Setup Time	t_{su}	5.0 10 15	120 50 40	60 25 20	— — —	ns
Data Hold Time	t_h	5.0 10 15	80 40 30	40 20 15	— — —	ns
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0 10 15	250 100 80	125 50 40	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MC14490

Hex Contact Bounce Eliminator

ON Semiconductor

http://onsemi.com

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the “make” and the “break” of a contact closure. The clock for operation of the MC14490 is derived from an internal R−C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

NOTE: Immediately after power−up, the outputs of the MC14490 are in indeterminate states.

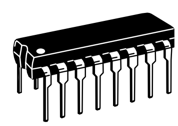
- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R−C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both “Make” and “Break” Contacts
- Does Not Require “Form C” (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

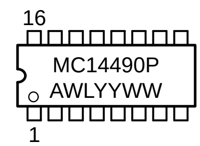
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

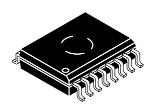
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

MARKING DIAGRAMS

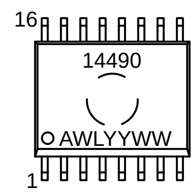


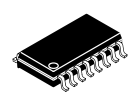
PDIP−16
P SUFFIX
CASE 648



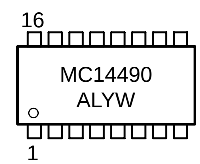


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

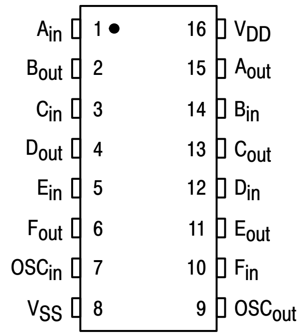
Device	Package	Shipping
MC14490DW	SOIC−16	47/Rail
MC14490DWR2	SOIC−16	1000/Tape & Reel
MC14490F	SOEIAJ−16	See Note 1.
MC14490FEL	SOEIAJ−16	See Note 1.
MC14490P	PDIP−16	25/Rail

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

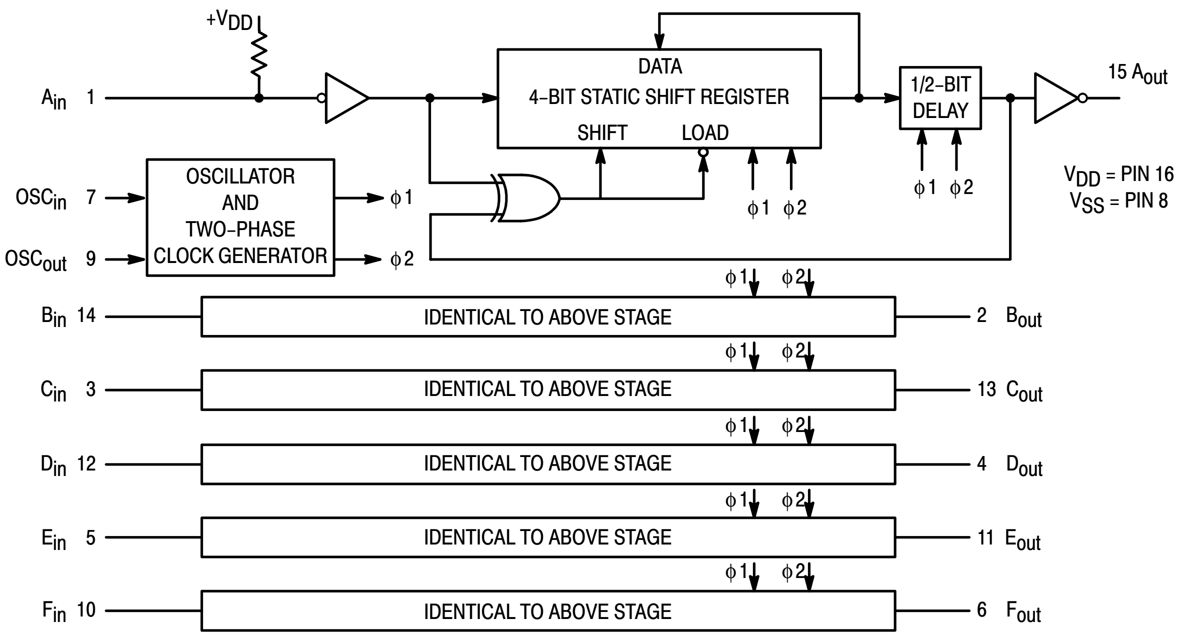
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) "1 Level"	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
Oscillator Output Source										
(V_{OH} = 2.5 V)		5.0	– 0.6	—	– 0.5	– 1.5	—	– 0.4	—	
(V_{OH} = 4.6 V)		5.0	– 0.12	—	– 0.1	– 0.3	—	– 0.08	—	
(V_{OH} = 9.5 V)		10	– 0.23	—	– 0.2	– 0.8	—	– 0.16	—	
(V_{OH} = 13.5 V)		15	– 1.4	—	– 1.2	– 3.0	—	– 1.0	—	
Debounce Outputs										
(V_{OH} = 2.5 V)		5.0	– 0.9	—	– 0.75	– 2.2	—	– 0.6	—	
(V_{OH} = 4.6 V)		5.0	– 0.19	—	– 0.16	– 0.46	—	– 0.12	—	
(V_{OH} = 9.5 V)		10	– 0.6	—	– 0.5	– 1.2	—	– 0.4	—	
(V_{OH} = 13.5 V)		15	1.8	—	– 1.5	– 4.5	—	– 1.2	—	
Oscillator Output Sink	I_{OL}									mAdc
(V_{OL} = 0.4 V)		5.0	0.36	—	0.3	0.9	—	0.24	—	
(V_{OL} = 0.5 V)		10	0.9	—	0.75	2.3	—	0.6	—	
(V_{OL} = 1.5 V)		15	4.2	—	3.5	10	—	2.8	—	
Debounce Outputs										
(V_{OL} = 0.4 V)		5.0	2.6	—	2.2	4.0	—	1.8	—	
(V_{OL} = 0.5 V)		10	4.0	—	3.3	9.0	—	2.7	—	
(V_{OL} = 1.5 V)		15	12	—	10	35	—	8.1	—	
Input Current Debounce Inputs ($V_{in} = V_{DD}$)	I_{IH}	15	—	2.0	—	0.2	2.0	—	11	µAdc
Input Current Oscillator — Pin 7 ($V_{in} = V_{SS}$ or V_{DD})	I_{in}	15	—	± 620	—	± 255	± 400	—	± 250	µAdc
Pullup Resistor Source Current Debounce Inputs ($V_{in} = V_{SS}$)	I_{IL}	5.0	175	375	140	190	255	70	225	µAdc
		10	340	740	280	380	500	145	440	
		15	505	1100	415	570	750	215	660	
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current ($V_{in} = V_{SS}$ or V_{DD}, I_{out} = 0 µA)	I_{SS}	5.0	—	150	—	40	100	—	90	µAdc
		10	—	280	—	90	225	—	180	
		15	—	840	—	225	650	—	550	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS (5.) (C_L = 50 pF, T_A = 25°C)

Characteristic		Symbol	V_{DD} Vdc	Min	Typ (6.)	Max	Unit
Output Rise Time All Outputs		t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time	Oscillator Output	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
	Debounce Outputs	t_{THL}	5.0 10 15	— — —	60 30 20	120 60 40	
Propagation Delay Time Oscillator Input to Debounce Outputs		t_{PHL}	5.0 10 15	— — —	285 120 95	570 240 190	ns
		t_{PLH}	5.0 10 15	— — —	370 160 120	740 320 240	
Clock Frequency (50% Duly Cycle) (External Clock)		f_{cl}	5.0 10 15	— — —	2.8 6 9	1.4 3.0 4.5	MHz
Setup Time (See Figure 1)		t_{su}	5.0 10 15	100 80 60	50 40 30	— — —	ns
Maximum External Clock Input Rise and Fall Time Oscillator Input		t_r, t_f	5.0 10 15	No Limit			ns
Oscillator Frequency OSC_{out} $C_{ext} \geq 100$ pF* Note: These equations are intended to be a design guide. Laboratory experimentation may be required. Formulas are typically ± 15% of actual frequencies.		f_{osc}, typ	5.0 10 15	$\frac{1.5}{C_{ext}\text{ (in }\mu\text{F)}}$ $\frac{4.5}{C_{ext}\text{ (in }\mu\text{F)}}$ $\frac{6.5}{C_{ext}\text{ (in }\mu\text{F)}}$			Hz

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

***POWER−DOWN CONSIDERATIONS**

Large values of C_{ext} may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA, therefore the turn−off time of the power supply must not be faster than $t = (V_{DD} - V_{SS}) \bullet C_{ext} / (10\text{ mA})$. For example, If $V_{DD} - V_{SS} = 15$ V and $C_{ext} = 1\,\mu F$, the power supply must turn off no faster than $t = (15\text{ V}) \bullet (1\,\mu F) / 10\text{ mA} = 1.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

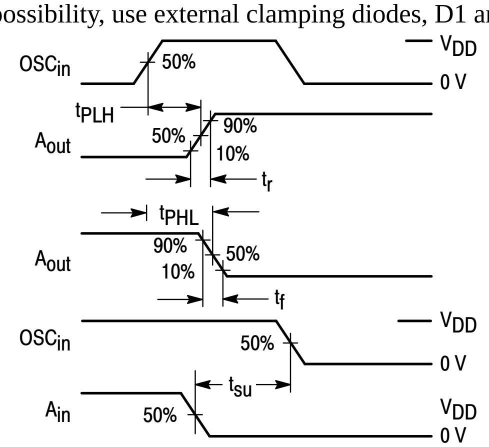


Figure 1. Switching Waveforms

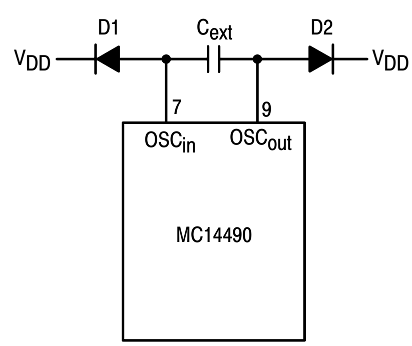


Figure 2. Discharge Protection During Power Down

THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4−1/2−bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is closed, (see Figure 4) the low level is inverted, and the shift register is loaded with a high on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a 3−1/2 to 4−1/2 clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+1 a low is loaded into the first bit. Just after N+1, when the input bounces low, all bits are set to a high. At N+2 nothing happens because the input and output are low and all bits of the shift register are high. At time N+3 and thereafter the input signal is a high, clean signal. At the positive edge of N+6 the output goes high as a result of four lows being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

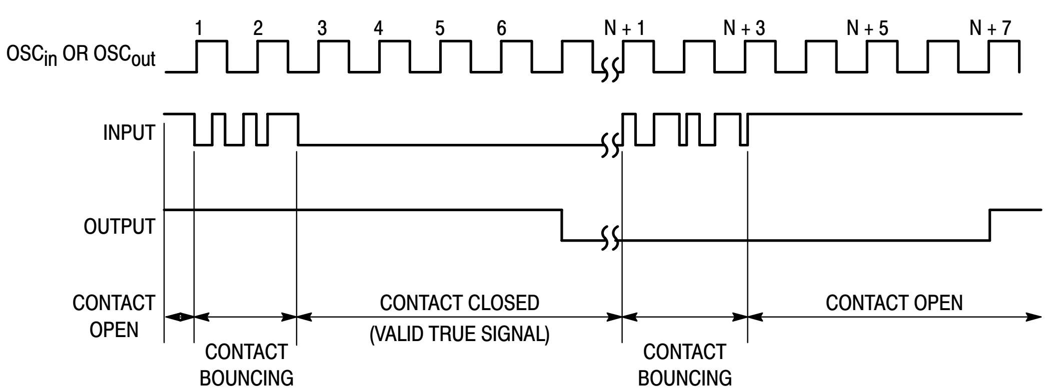


Figure 3. Timing Diagram

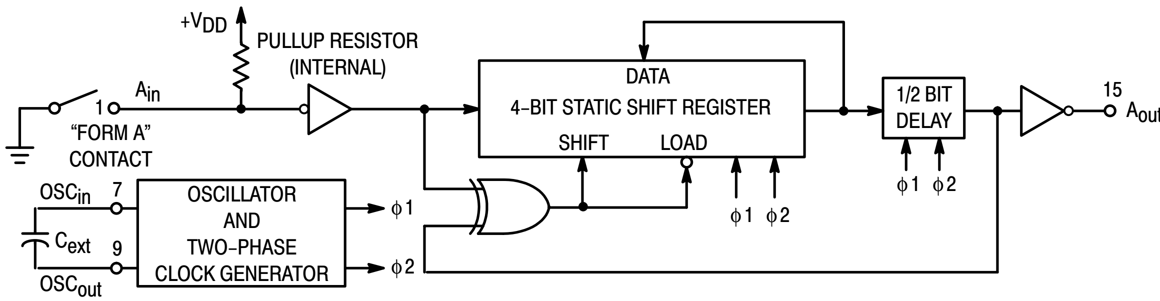


Figure 4. Typical "Form A" Contact Debounce Circuit (Only One Debouncer Shown)

OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

The circuit has a built−in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built−in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

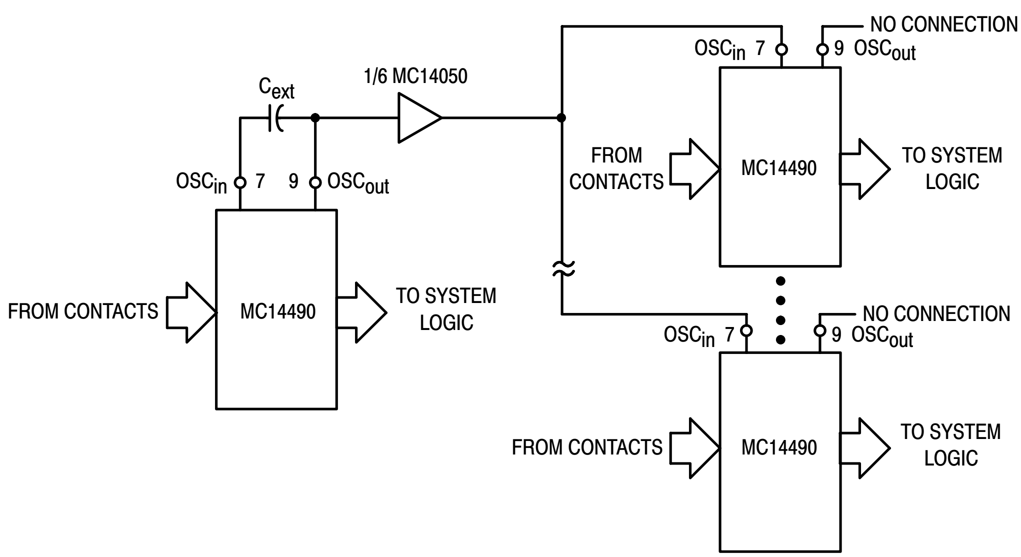


Figure 5. Typical Single Oscillator Debounce System

TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

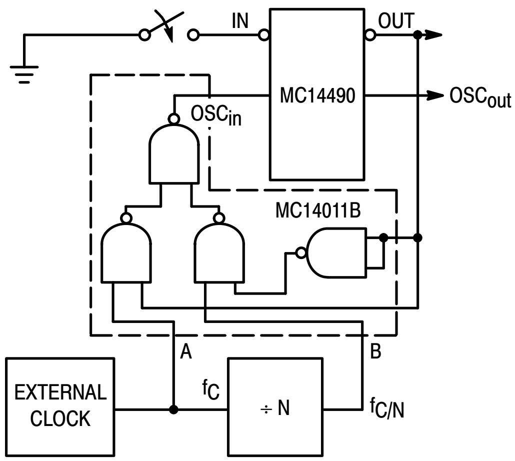


Figure 6. Fast Attack/Slow Release Circuit

LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

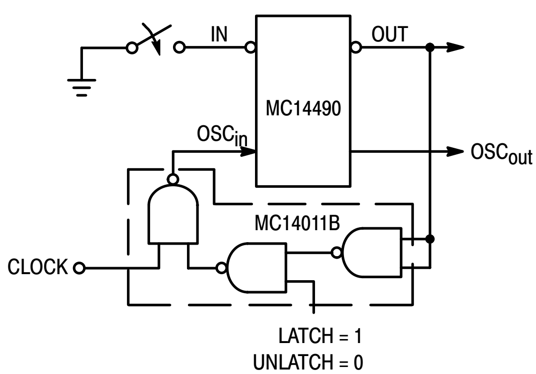


Figure 7. Latched Output Circuit

MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $\overline{A}B$ as shown in Figures 9 and 10. The signal $\overline{A}B$ is four clock periods in length. If the inverter is switched to the A output, the pulse $A\overline{B}$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

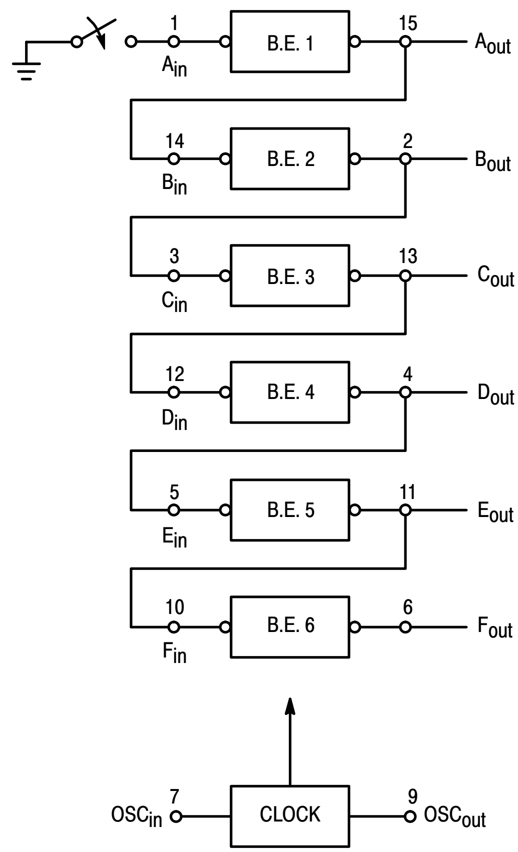


Figure 8. Multiple Timing Circuit Connections

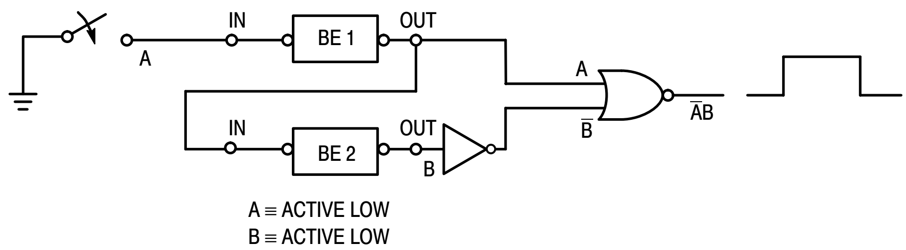


Figure 9. Single Pulse Output Circuit

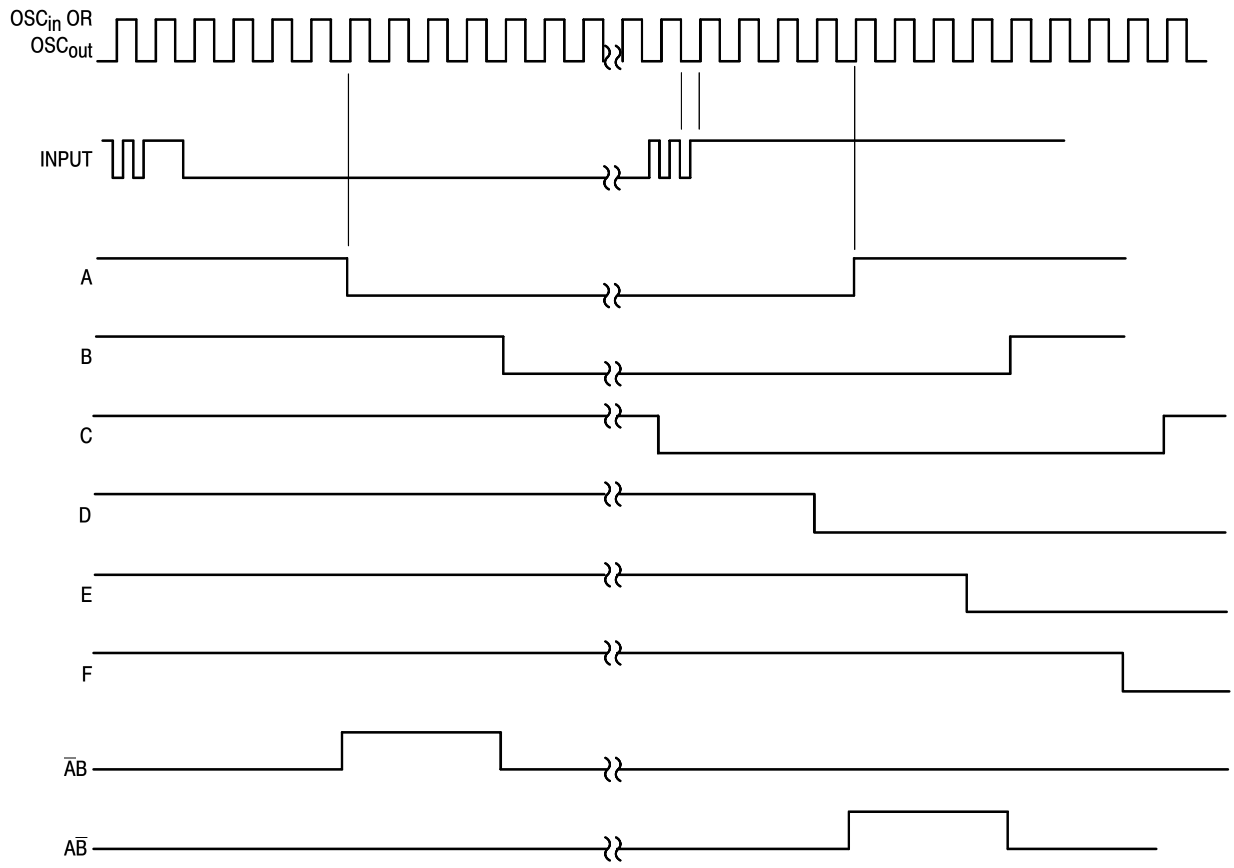


Figure 10. Multiple Output Signal Timing Diagram

MC14503B

Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non−inverting buffer with 3−state outputs, and a high current source and sink capability. The 3−state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3−State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	±25	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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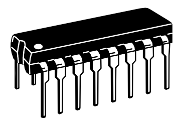
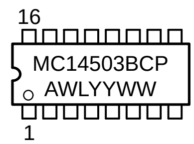
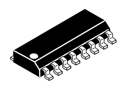
MARKING DIAGRAMS

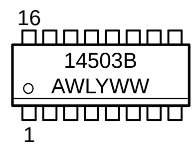


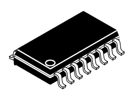
PDIP−16
P SUFFIX
CASE 648



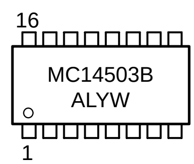


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



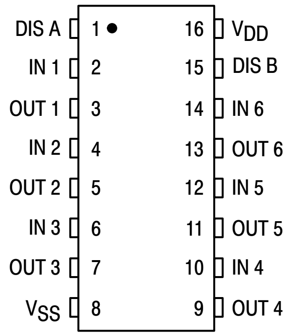
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14503BCP	PDIP−16	2000/Box
MC14503BD	SOIC−16	48/Rail
MC14503BDR2	SOIC−16	2500/Tape & Reel
MC14503BF	SOEIAJ−16	See Note 1.
MC14503BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

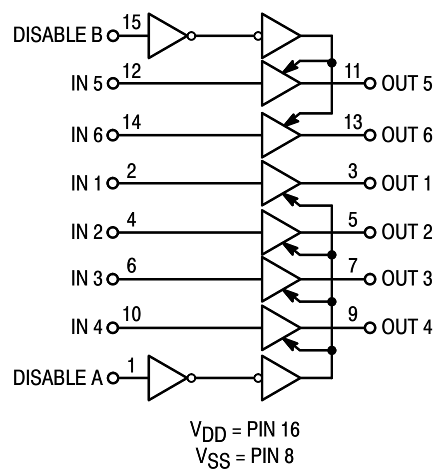


TRUTH TABLE

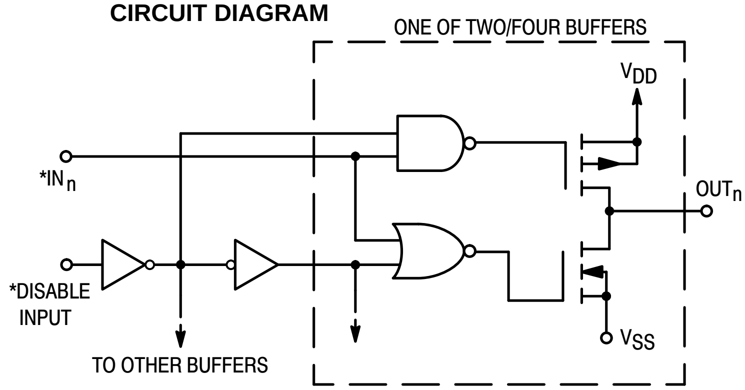
In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM



CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 3.6 or 1.4 Vdc) (V_O = 7.2 or 2.8 Vdc) (V_O = 11.5 or 3.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 1.4 or 3.6 Vdc) (V_O = 2.8 or 7.2 Vdc) (V_O = 3.5 or 11.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	4.5 5.0 5.0 10 15	– 4.3 – 5.8 – 1.2 – 3.1 – 8.2	— — — — —	– 3.6 – 4.8 – 1.02 – 2.6 – 6.8	– 5.0 – 6.1 – 1.4 – 3.7 – 14.1	— — — — —	– 2.5 – 3.0 – 0.7 – 1.8 – 4.8	— — — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	4.5 5.0 10 15	2.2 2.6 6.5 19.2	— — — —	1.8 2.1 5.5 16.1	2.1 2.3 6.2 25	— — — —	1.2 1.3 3.8 11.2	— — — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_Q	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)	I_T	5.0 10 15	I_T = (2.5 µA/kHz) f + I_{DD} I_T = (6.0 µA/kHz) f + I_{DD} I_T = (10 µA/kHz) f + I_{DD}							µAdc
Three−State Output Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ (8.)	All Types Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn−Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn−On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3−State Propagation Delay Time Output “1” to High Impedance	t_{PHZ}	5.0 10 15	75 40 35	150 80 70	ns
Output “0” to High Impedance	t_{PLZ}	5.0 10 15	80 40 35	160 80 70	ns
High Impedance to “1” Level	t_{PZH}	5.0 10 15	65 25 20	130 50 40	ns
High Impedance to “0” Level	t_{PZL}	5.0 10 15	100 35 25	200 70 50	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

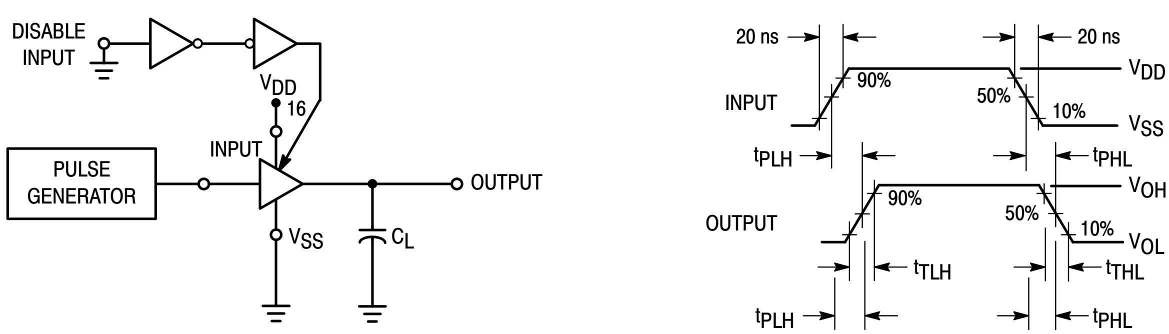


Figure 1. Switching Time Test Circuit and Waveforms (t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

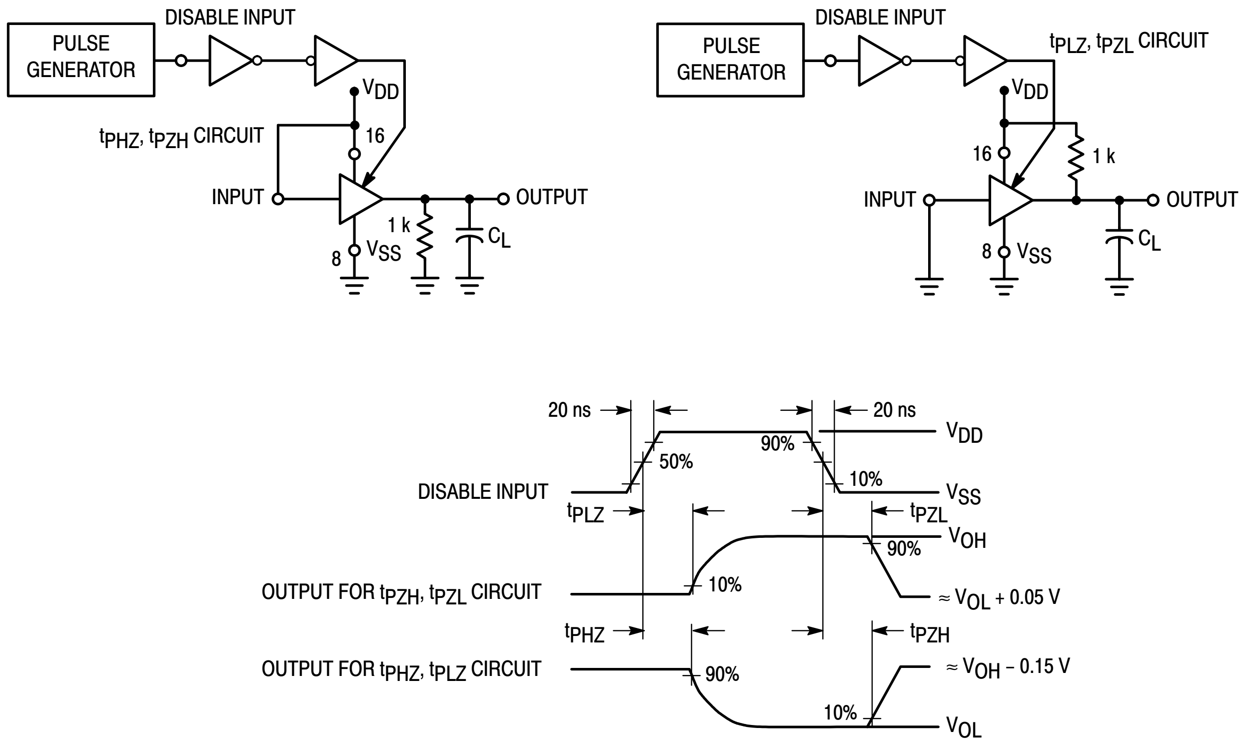


Figure 2. 3−State AC Test Circuit and Waveforms
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})

Hex Level Shifter for TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non−inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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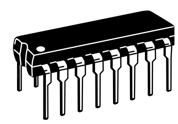
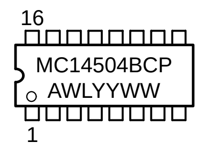
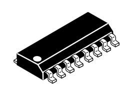
MARKING DIAGRAMS

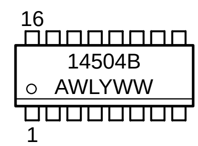


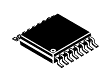
PDIP−16
P SUFFIX
CASE 648



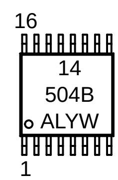


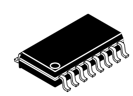
SOIC−16
D SUFFIX
CASE 751B



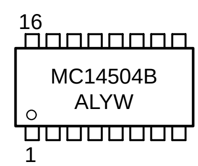


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



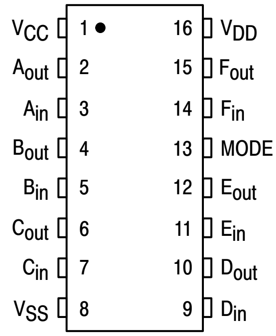
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

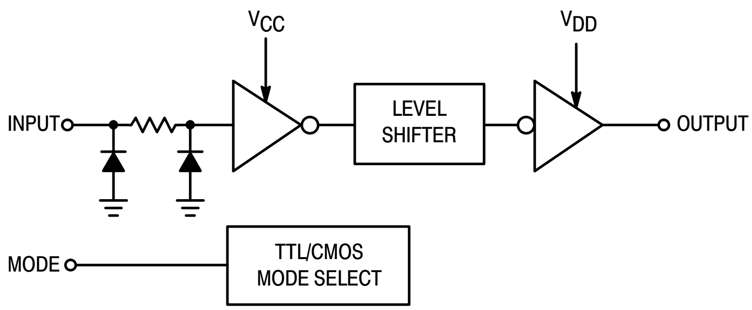
Device	Package	Shipping
MC14504BCP	PDIP−16	2000/Box
MC14504BD	SOIC−16	48/Rail
MC14504BDR2	SOIC−16	2500/Tape & Reel
MC14504BDT	TSSOP−16	96/Rail
MC14504BF	SOEIAJ−16	See Note 1.
MC14504BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = 0 V	V_{OL}	—	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		—	10	—	0.05	—	0	0.05	—	0.05	
		—	1 5	—	0.05	—	0	0.05	—	0.05	
“1” Level V_{in} = V_{CC}	V_{OH}	—	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		—	10	9.95	—	9.95	10	—	9.95	—	
		—	15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL−CMOS		5.0	10	—	0.8	—	1.3	0.8	—	0.8	
(V_{OL} = 1.5 Vdc) TTL−CMOS		5.0	15	—	0.8	—	1.3	0.8	—	0.8	
(V_{OL} = 1.0 Vdc) CMOS−CMOS		5.0	10	—	1.5	—	2.25	1.5	—	1.4	
(V_{OL} = 1.5 Vdc) CMOS−CMOS		5.0	15	—	1.5	—	2.25	1.5	—	1.5	
(V_{OL} = 1.5 Vdc) CMOS−CMOS		10	15	—	3.0	—	4.5	3.0	—	2.9	
Input Voltage “1” Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL−CMOS		5.0	10	2.0	—	2.0	1.5	—	2.0	—	
(V_{OH} = 13.5 Vdc) TTL−CMOS		5.0	15	2.0	—	2.0	1.5	—	2.0	—	
(V_{OH} = 9.0 Vdc) CMOS−CMOS		5.0	10	3.6	—	3.5	2.75	—	3.5	—	
(V_{OH} = 13.5 Vdc) CMOS−CMOS		5.0	15	3.6	—	3.5	2.75	—	3.5	—	
(V_{OH} = 13.5 Vdc) CMOS−CMOS		10	15	7.1	—	7.0	5.5	—	7.0	—	
Output Drive Current	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		—	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		—	5.0	–0.64	—	–0.51	– 0.88	—	–0.36	—	
(V_{OH} = 9.5 Vdc)		—	10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		—	15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	—	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		—	10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		—	15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	—	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) CMOS−CMOS Mode	I_{DD} or I_{CC}	—	5.0	—	0.05	—	0.0005	0.05	—	1.5	µAdc
		—	10	—	0.10	—	0.0010	0.10	—	3.0	
		—	15	—	0.20	—	0.0015	0.20	—	6.0	
Quiescent Current (Per Package) TTL−CMOS Mode	I_{DD}	5.0	5.0	—	0.5	—	0.0005	0.5	—	3.8	µAdc
		5.0	10	—	1.0	—	0.0010	1.0	—	7.5	
		5.0	15	—	2.0	—	0.0015	2.0	—	15	
Quiescent Current (Per Package) TTL−CMOS Mode	I_{CC}	5.0	5.0	—	5.0	—	2.5	5.0	—	6.0	mAdc
		5.0	10	—	5.0	—	2.5	5.0	—	6.0	
		5.0	15	—	5.0	—	2.5	5.0	—	6.0	

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits			Unit
					Min	Typ (5.)	Max	
Propagation Delay, High to Low	t_{PHL}	TTL – CMOS V_{DD} > V_{CC}	5.0 5.0	10 15	— —	140 140	280 280	ns
		CMOS – CMOS V_{DD} > V_{CC}	5.0 5.0 10	10 15 15	— — —	120 120 70	240 240 140	
		CMOS – CMOS V_{CC} > V_{DD}	10 15 15	5.0 5.0 10	— — —	185 185 175	370 370 350	
Propagation Delay, Low to High	t_{PLH}	TTL – CMOS V_{DD} > V_{CC}	5.0 5.0	10 15	— —	170 160	340 320	ns
		CMOS – CMOS V_{DD} > V_{CC}	5.0 5.0 10	10 15 15	— — —	170 170 100	340 340 200	
		CMOS – CMOS V_{CC} > V_{DD}	10 15 15	5.0 5.0 10	— — —	275 275 145	550 550 290	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	— — —	5.0 10 15	— — —	100 50 40	200 100 80	ns

5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

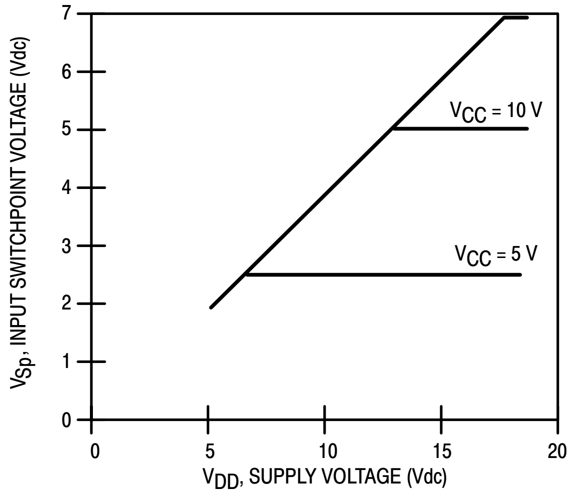


Figure 1. Input Switchpoint CMOS to CMOS Mode

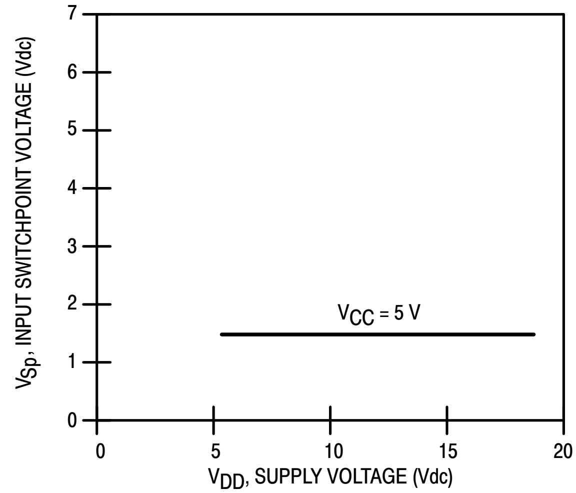


Figure 2. Input Switchpoint TTL to CMOS Mode

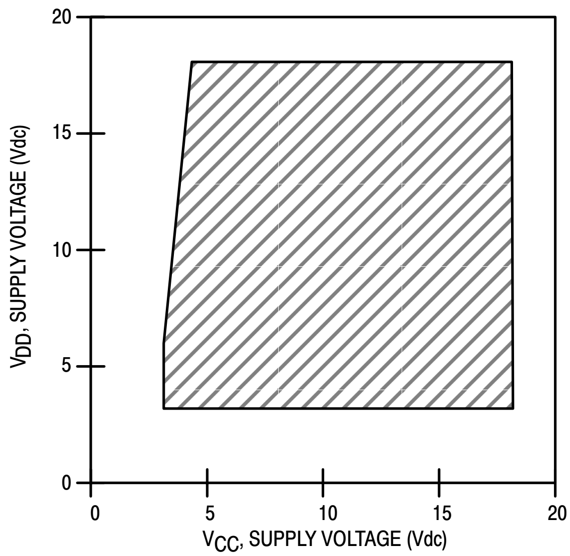


Figure 3. Operating Boundary CMOS to CMOS Mode

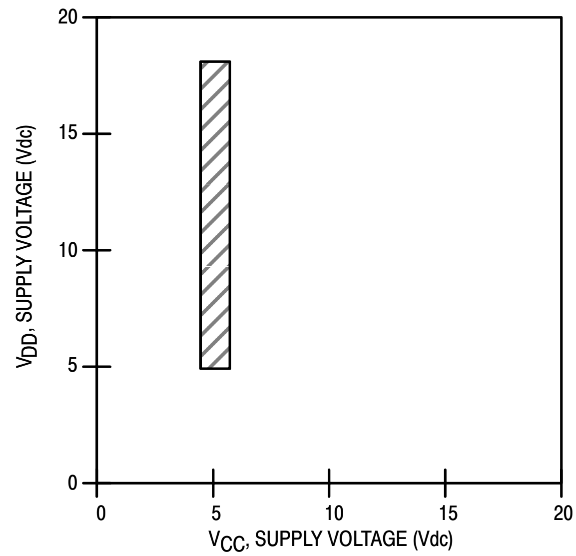


Figure 4. Operating Boundary TTL to CMOS Mode

MC14511B

BCD-To-Seven Segment Latch/Decoder/Driver

The MC14511B BCD−to−seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4−bit storage latch, an 8421 BCD−to−seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn−off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven−segment light−emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High−Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low−power TTL Loads, One Low−power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	−0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Input Pin	10	mA
P_D	Power Dissipation, per Package (Note 3)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
I_{OHmax}	Maximum Output Drive Current (Source) per Output	25	mA
P_{OHmax}	Maximum Continuous Output Power (Source) per Output (Note 4)	50	mA

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
4. $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

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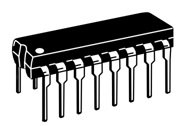
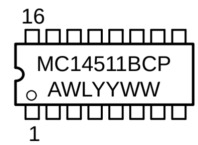
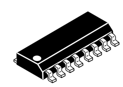
MARKING DIAGRAMS

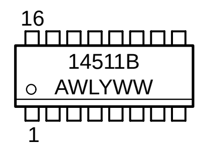


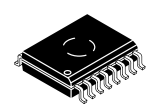
PDIP−16
P SUFFIX
CASE 648



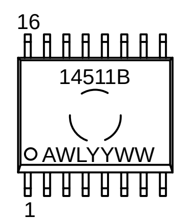


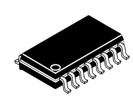
SOIC−16
D SUFFIX
CASE 751B



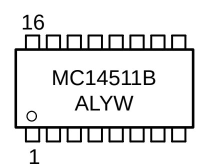


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14511BCP	PDIP−16	2000/Box
MC14511BD	SOIC−16	48/Rail
MC14511BDW	SOIC−16	47/Rail
MC14511BDWR2	SOIC−16	1000/Tape & Reel
MC14511BF	SOEIAJ−16	See Note 1
MC14511BFEL	SOEIAJ−16	See Note 1

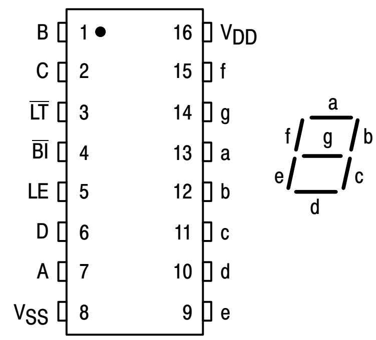
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high−impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

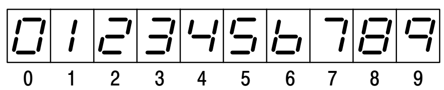
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs							Outputs							
LE	**BI**	**LT**	**D**	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	1	1	0	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don’t Care

*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 5)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.1 9.1 14.1	— — —	4.1 9.1 14.1	4.57 9.58 14.59	— — —	4.1 9.1 14.1	— — —	Vdc
Input Voltage # (V_O = 3.8 or 0.5 Vdc) (V_O = 8.8 or 1.0 Vdc) (V_O = 13.8 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 3.8 Vdc) (V_O = 1.0 or 8.8 Vdc) (V_O = 1.5 or 13.8 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Voltage (I_{OH} = 0 mA) (I_{OH} = 5.0 mA) (I_{OH} = 10 mA) (I_{OH} = 15 mA) (I_{OH} = 20 mA) (I_{OH} = 25 mA)	Source	V_{OH}	5.0	4.1 — 3.9 — 3.4 —	— — — — — —	4.1 — 3.9 — 3.4 —	4.57 4.24 4.12 3.94 3.70 3.54	— — — — — —	4.1 — 3.5 — 3.0 —	— — — — — —	Vdc
(I_{OH} = 0 mA) (I_{OH} = 5.0 mA) (I_{OH} = 10 mA) (I_{OH} = 15 mA) (I_{OH} = 20 mA) (I_{OH} = 25 mA)			10	9.1 — 9.0 — 8.6 —	— — — — — —	9.1 — 9.0 — 8.6 —	9.58 9.26 9.17 9.04 8.90 8.70	— — — — — —	9.1 — 8.6 — 8.2 —	— — — — — —	Vdc
(I_{OH} = 0 mA) (I_{OH} = 5.0 mA) (I_{OH} = 10 mA) (I_{OH} = 15 mA) (I_{OH} = 20 mA) (I_{OH} = 25 mA)			15	14.1 — 14 — 13.6 —	— — — — — —	14.1 — 14 — 13.6 —	14.59 14.27 14.18 14.07 13.95 13.70	— — — — — —	14.1 — 13.6 — 13.2 —	— — — — — —	Vdc
Output Drive Current (V_{OL} = 0.4 V) (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 µA		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (Notes 6 & 7) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.9 µA/kHz) f + I_{DD} I_T = (3.8 µA/kHz) f + I_{DD} I_T = (5.7 µA/kHz) f + I_{DD}							µAdc

5. Noise immunity specified for worst−case input combination.
   Noise Margin for both "1" and "0" level =
   1.0 Vdc min @ V_{DD} = 5.0 Vdc
   2.0 Vdc min @ V_{DD} = 10 Vdc
   2.5 Vdc min @ V_{DD} = 15 Vdc
6. The formulas given are for the typical characteristics only at 25°C.
7. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

SWITCHING CHARACTERISTICS (Note 8) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		5.0	—	40	80	
t_{TLH} = (0.25 ns/pF) C_L + 17.5 ns		10	—	30	60	
t_{TLH} = (0.20 ns/pF) C_L + 15 ns		15	—	25	50	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	—	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	—	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	—	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	—	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	—	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	—	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	—	720	1440	
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	—	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	—	200	400	
$\overline{\text{Blank}}$ Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 585 ns		5.0	—	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 187.5 ns		I0	—	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 142.5 ns		15	—	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	—	485	970	
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	—	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	—	160	320	
$\overline{\text{Lamp Test}}$ Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	—	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	—	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	—	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	—	313	625	
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	—	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	—	90	180	
Setup Time	t_{su}	5.0	100	—	—	ns
		10	40	—	—	
		15	30	—	—	
Hold Time	t_h	5.0	60	—	—	ns
		10	40	—	—	
		15	30	—	—	
Latch Enable Pulse Width	t_{WL}	5.0	520	260	—	ns
		10	220	110	—	
		15	130	65	—	

8. The formulas given are for the typical characteristics only.

Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

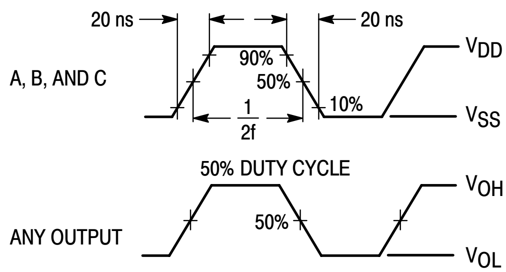
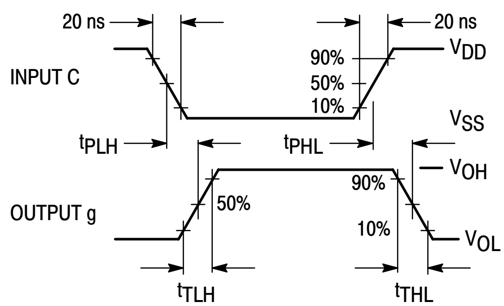
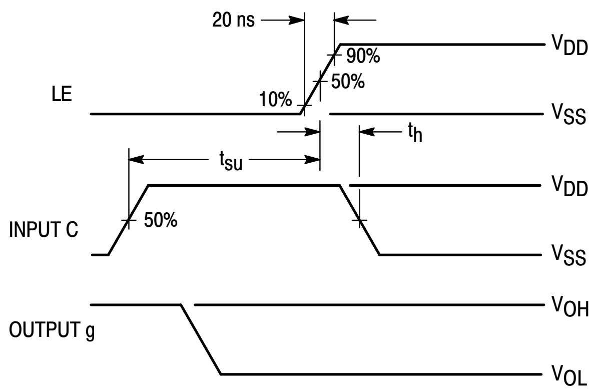


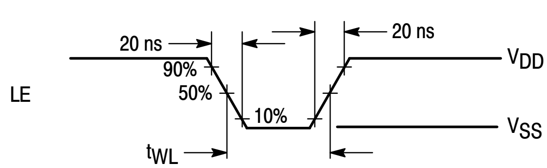
Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

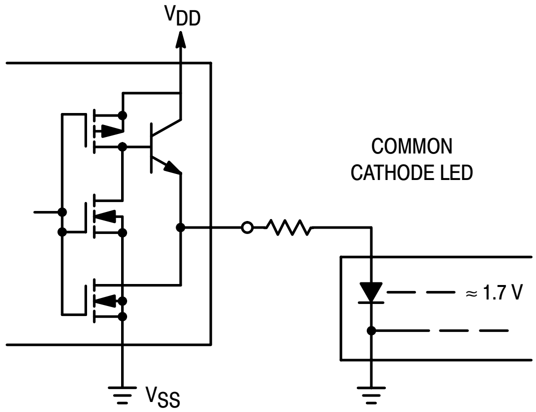


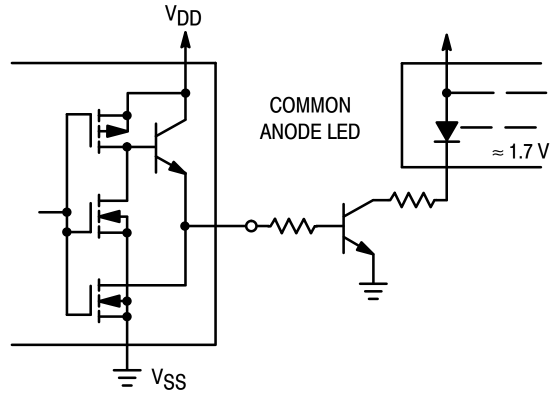
(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

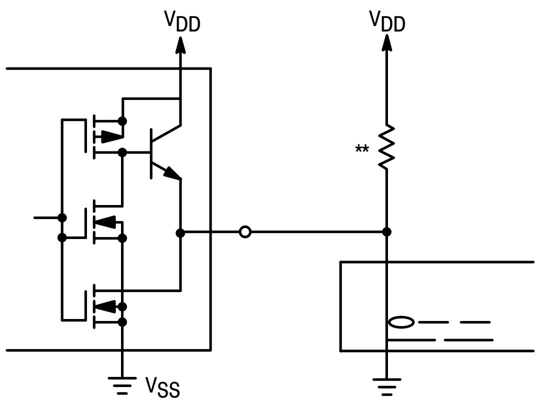
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

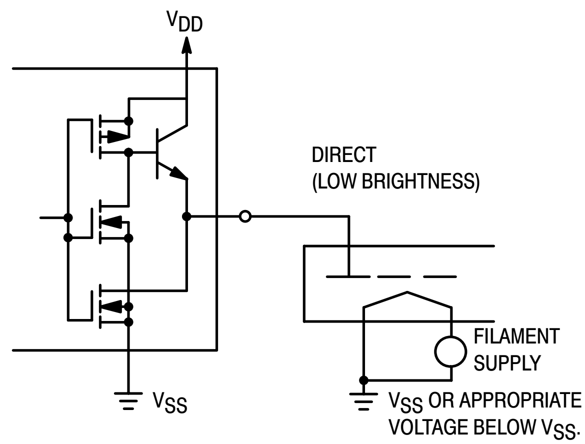




INCANDESCENT READOUT

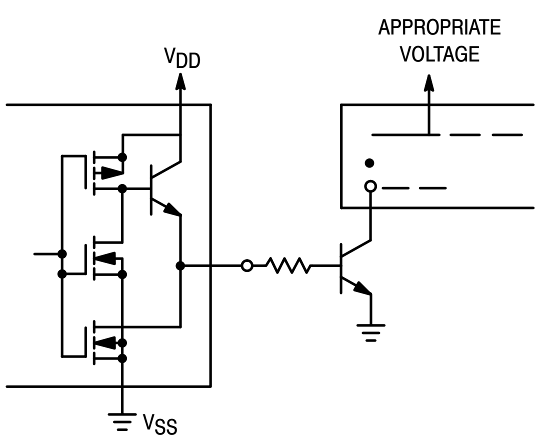


FLUORESCENT READOUT

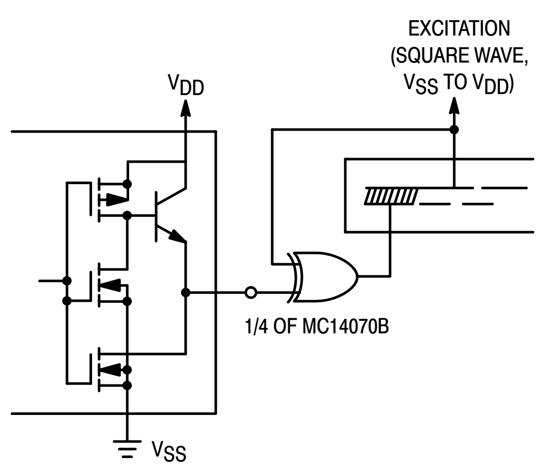


(CAUTION: Maximum working voltage = 18.0 V)

GAS DISCHARGE READOUT



LIQUID CRYSTAL (LCD) READOUT



** A filament pre−warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD’s not recommended for life of LCD readouts.

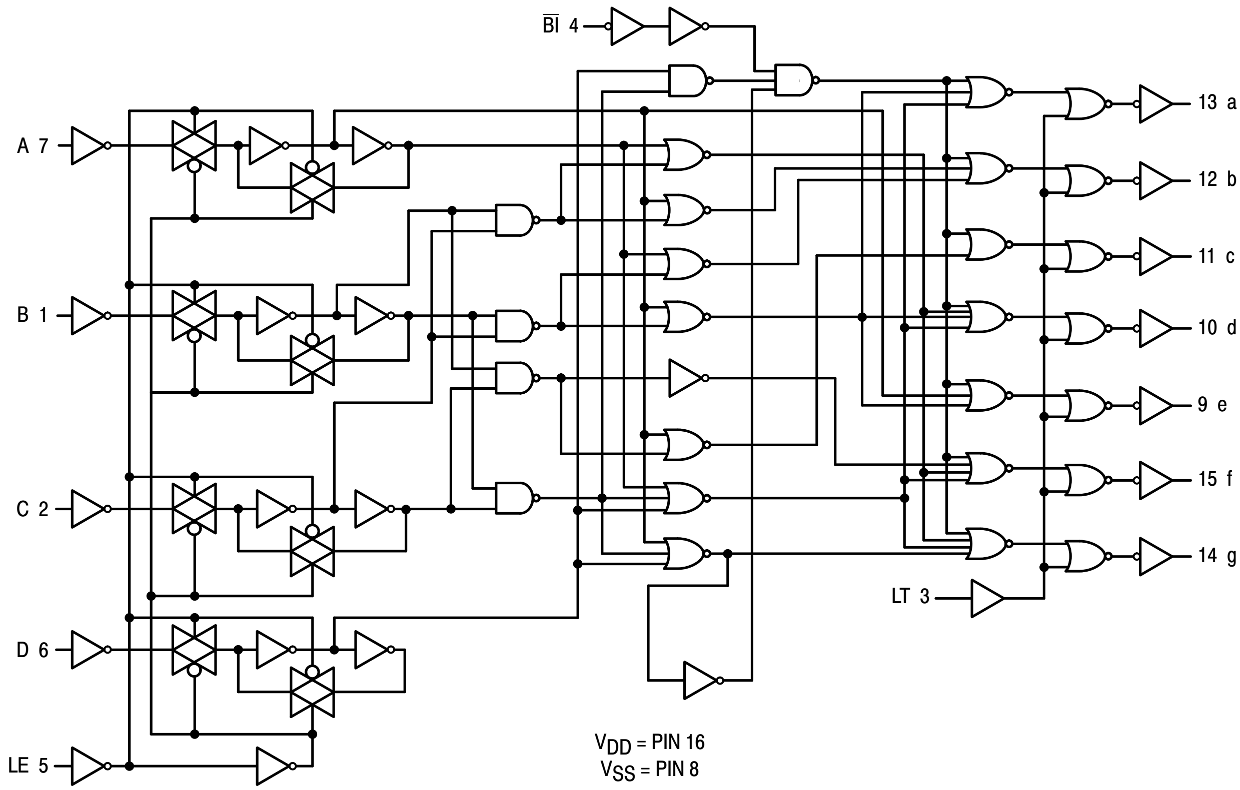


Figure 3. Logic Diagram

MC14512B

8-Channel Data Selector

The MC14512B is an 8−channel data selector constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3−State Output (Logic “1”, Logic “0”, High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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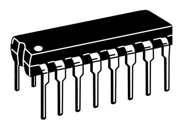
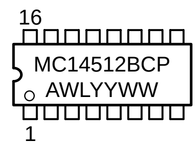
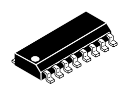
MARKING DIAGRAMS

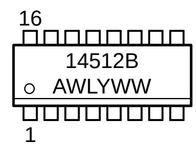


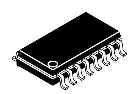
PDIP−16
P SUFFIX
CASE 648



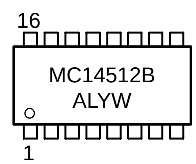


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14512BCP	PDIP−16	2000/Box
MC14512BD	SOIC−16	48/Rail
MC14512BDR2	SOIC−16	2500/Tape & Reel
MC14512BF	SOEIAJ−16	See Note 1.
MC14512BFL1	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

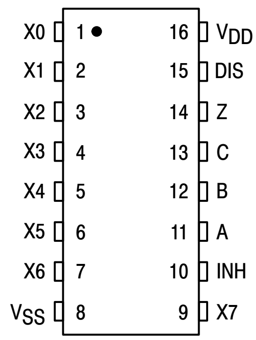
August, 2000 − Rev. 4
Publication Order Number:
MC14512B/D

TRUTH TABLE

C	B	A	Inhibit	Disable	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

X = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	 5.0 10 15	 3.5 7.0 11	 — — —	 3.5 7.0 11	 2.75 5.50 8.25	 — — —	 3.5 7.0 11	 — — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.8 µA/kHz) f + I_{DD} I_T = (1.6 µA/kHz) f + I_{DD} I_T = (2.4 µA/kHz) f + I_{DD}							µAdc
Three−State Leakage Current		I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L – 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V_{DD}	All Types Typ (8.)	All Types Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}				ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	40	80	
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PLH}	5.0	330	650	ns
		10	125	250	
		15	85	170	
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PHL}	5.0	330	650	ns
		10	125	250	
		15	85	170	
3−State Output Delay Times (Figure 3) “1” or “0” to High Z, and High Z to “1” or “0”	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0	60	150	ns
		10	35	100	
		15	30	75	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

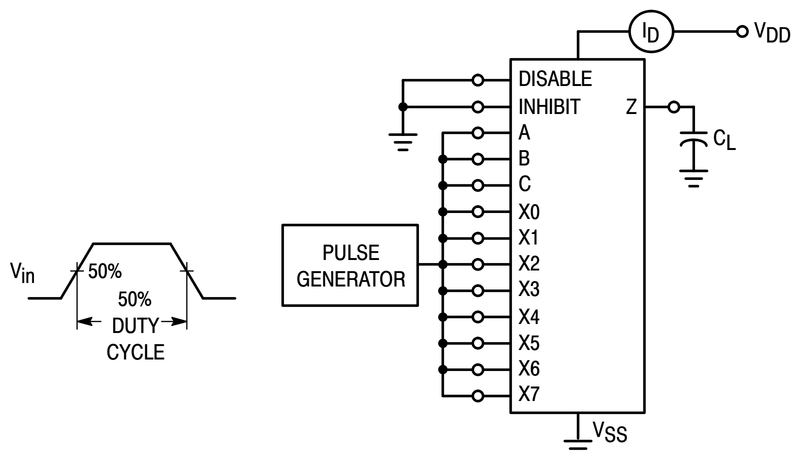
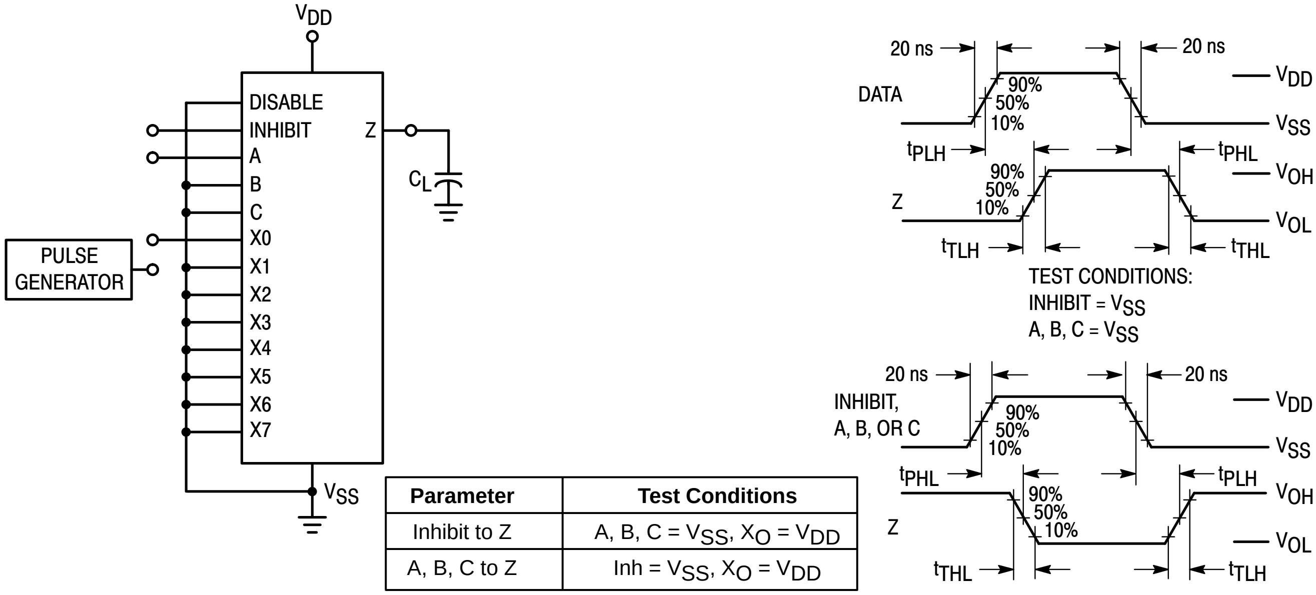
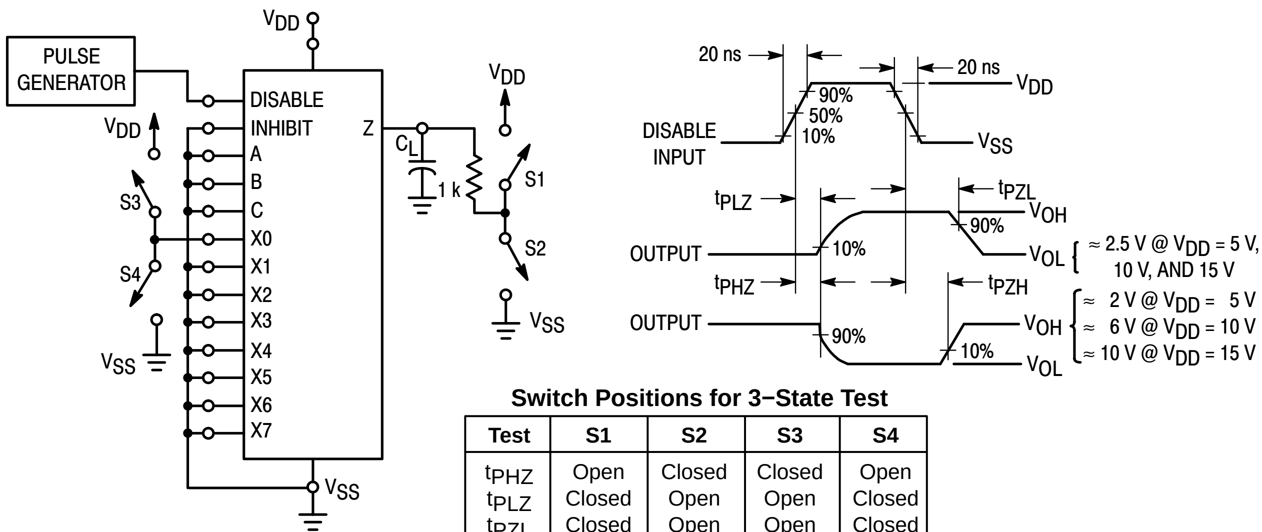


Figure 1. Power Dissipation Test Circuit and Waveform



Parameter	Test Conditions
Inhibit to Z	A, B, C = V_{SS}, X_O = V_{DD}
A, B, C to Z	Inh = V_{SS}, X_O = V_{DD}

Figure 2. AC Test Circuit and Waveforms

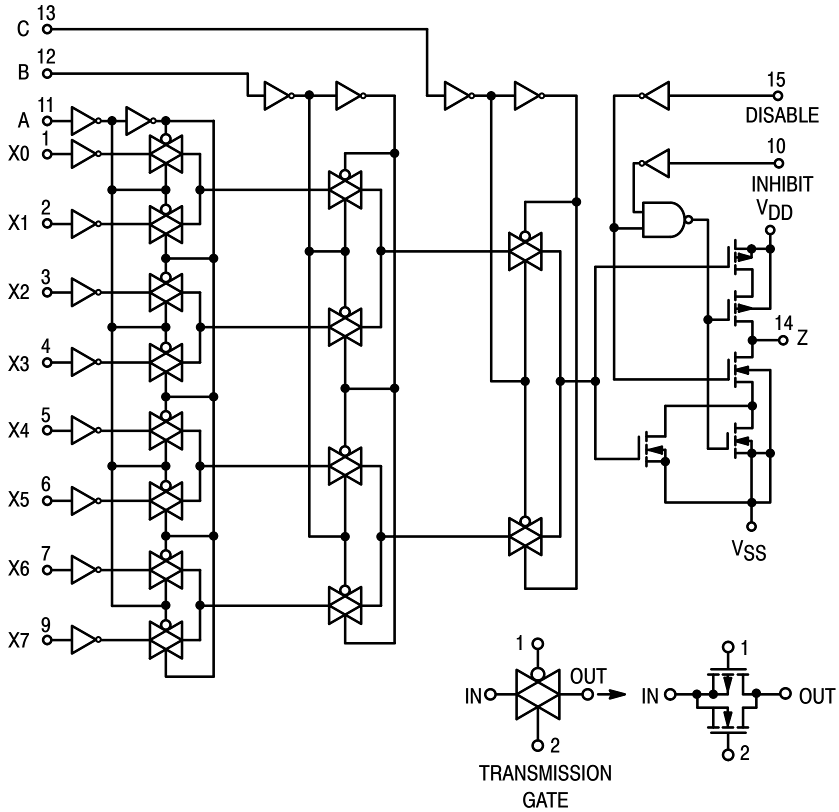


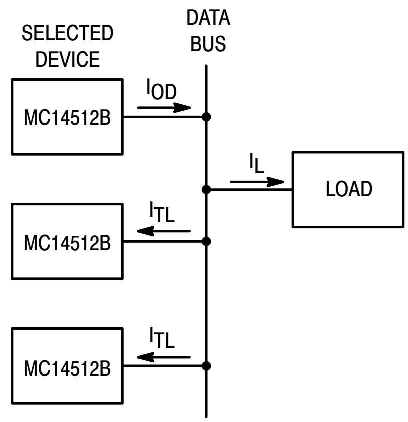
Switch Positions for 3−State Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

Figure 3. 3−State AC Test Circuit and Waveform

LOGIC DIAGRAM





3−STATE MODE OF OPERATION

Output terminals of several MC14512B 8−Bit Data Selectors can be connected to a single date bus as shown. One MC14512B is selected by the 3−state control, and the remaining devices are disabled into a high−impedance “off” state. The number of 8−bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3−state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

MC14513B

BCD-To-Seven Segment Latch/Decoder/Driver

CMOS MSI (Low−Power Complementary MOS)

The MC14513B BCD−to−seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4−bit storage latch, an 8421 BCD−to−seven segment decoder, and has output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn−off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven−segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High−current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low−Power TTL Loads, One Low−power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	−0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Input Pin	10	mA
P_D	Power Dissipation, per Package (2.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
I_{OHmax}	Maximum Continuous Output Drive Current (Source) per Output	25	mA
P_{OHmax}	Maximum Continuous Output Power (Source) per Output (3.)	50	mW

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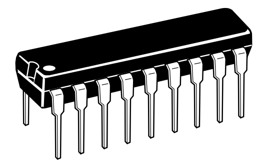
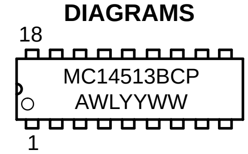


MARKING DIAGRAMS

PDIP−18
P SUFFIX
CASE 707



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14513BCP	PDIP−18	20/Rail

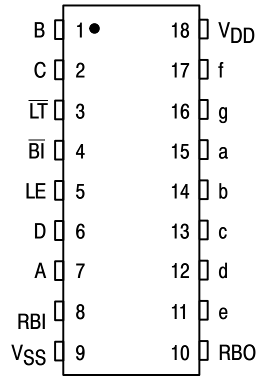
This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high−impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

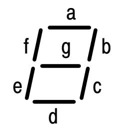
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

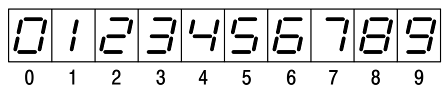
1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
3. $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

PIN ASSIGNMENT





DISPLAY



TRUTH TABLE

Inputs								Outputs								
RBI	**LE**	**$\overline{BI}$**	**$\overline{LT}$**	**D**	**C**	**B**	**A**	**RBO**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	+	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	†				*				*

X = Don’t Care

†RBO = RBI ($\overline{D}$ $\overline{C}$ $\overline{B}$ $\overline{A}$), indicated by other rows of table

*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage — Segment Outputs	V_{OL}									Vdc
“0” Level		5.0	—	0.05	—	0	0.05	—	0.05	
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	5.0	4.1	—	4.1	5.0	—	4.1	—	Vdc
V_{in} = 0 or V_{DD}		10	9.1	—	9.1	10	—	9.1	—	
		15	14.1	—	14.1	15	—	14.1	—	
Output Voltage — RBO Output	V_{OL}									Vdc
“0” Level		5.0	—	0.05	—	0	0.05	—	0.05	
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (4.) “0” Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 8.8 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 3.8 Vdc) “1” Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 8.8 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.8 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Voltage — Segments	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	4.1	—	4.1	4.57	—	4.1	—	
(I_{OH} = 5.0 mA)			—	—	—	4.24	—	—	—	
(I_{OH} = 10 mA)			3.9	—	3.9	4.12	—	3.5	—	
(I_{OH} = 15 mA)			—	—	—	3.94	—	—	—	
(I_{OH} = 20 mA)			3.4	—	3.4	3.70	—	3.0	—	
(I_{OH} = 25 mA)			—	—	—	3.54	—	—	—	
(I_{OH} = 0 mA)		10	9.1	—	9.1	9.58	—	9.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	9.26	—	—	—	
(I_{OH} = 10 mA)			9.0	—	9.0	9.17	—	8.6	—	
(I_{OH} = 15 mA)			—	—	—	9.04	—	—	—	
(I_{OH} = 20 mA)			8.6	—	8.6	8.90	—	8.2	—	
(I_{OH} = 25 mA)			—	—	—	8.75	—	—	—	
(I_{OH} = 0 mA)		15	14.1	—	14.1	14.59	—	14.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	14.27	—	—	—	
(I_{OH} = 10 mA)			14	—	14	14.18	—	13.6	—	
(I_{OH} = 15 mA)			—	—	—	14.07	—	—	—	
(I_{OH} = 20 mA)			13.6	—	13.6	13.95	—	13.2	—	
(I_{OH} = 25 mA)			—	—	—	13.80	—	—	—	

(continued)

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Drive Current — RBO Output Source (V_{OH} = 2.5 V) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	I_{OH}	5.0 10 15	– 0.40 – 0.21 – 0.81	— — —	– 0.32 – 0.17 – 0.66	– 0.64 – 0.34 – 1.30	— — —	– 0.22 – 0.12 – 0.46	— — —	mAdc
Sink (V_{OL} = 0.4 V) (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0 10 15	0.18 0.47 1.80	— — —	0.15 0.38 1.50	0.29 0.75 2.90	— — —	0.10 0.26 1.0	— — —	mAdc
Output Drive Current — Segments Sink (V_{OL} = 0.4 V) (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 µA	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.9 µA/kHz) f + I_{DD} I_T = (3.8 µA/kHz) f + I_{DD} I_T = (5.7 µA/kHz) f + I_{DD}							µAdc

4. Noise immunity specified for worst−case input combination.
   Noise Margin for both “1” and “0” level =
   1.0 Vdc min @ V_{DD} = 5.0 Vdc
   2.0 Vdc min @ V_{DD} = 10 Vdc
   2.5 Vdc min @ V_{DD} = 15 Vdc
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3}\ (C_L - 50)\ V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

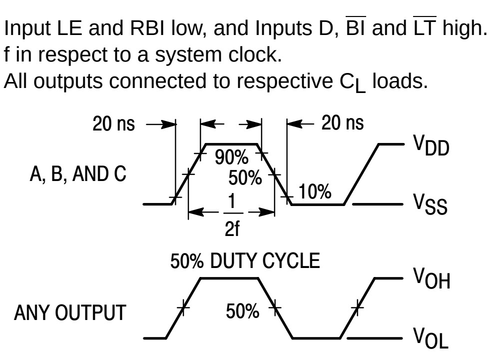
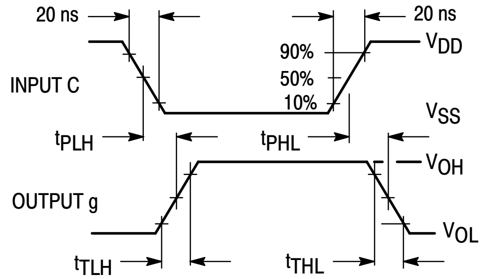


Figure 1. Dynamic Power Dissipation Signal Waveforms

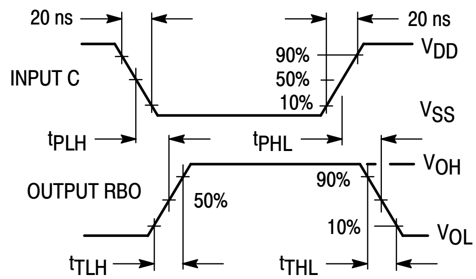
SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise Time — Segment Outputs	t_{TLH}	5.0 10 15	— — —	40 30 25	80 60 50	ns
Output Rise Time — RBO Output	t_{TLH}	5.0 10 15	— — —	480 240 190	960 480 380	ns
Output Fall Time — Segment Outputs [7.] t_{THL} = (1.5 ns/pF) C_L + 50 ns t_{THL} = (0.75 ns/pF) C_L + 37.5 ns t_{THL} = (0.55 ns/pF) C_L + 37.5 ns	t_{THL}	5.0 10 15	— — —	125 75 65	250 150 130	ns
Output Fall Time — RBO Outputs t_{THL} = (3.25 ns/pF) C_L + 107.5 ns t_{THL} = (1.35 ns/pF) C_L + 67.5 ns t_{THL} = (0.95 ns/pF) C_L + 62.5 ns	t_{THL}	5.0 10 15	— — —	270 135 110	540 270 220	ns
Propagation Delay Time — A, B, C, D Inputs [7.] t_{PLH} = (0.40 ns/pF) C_L + 620 ns t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns t_{PLH} = (0.20 ns/pF) C_L + 165 ns	t_{PLH}	5.0 10 15	— — —	640 250 175	1280 500 350	ns
t_{PHL} = (1.3 ns/pF) C_L + 655 ns t_{PHL} = (0.60 ns/pF) C_L + 260 ns t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns	t_{PHL}	5.0 10 15	— — —	720 290 200	1440 580 400	ns
Propagation Delay Time — RBI and $\overline{BI}$ Inputs [7.] t_{PLH} = (1.05 ns/pF) C_L + 547.5 ns t_{PLH} = (0.45 ns/pF) C_L + 177.5 ns t_{PLH} = (0.30 ns/pF) C_L + 135 ns	t_{PLH}	5.0 10 15	— — —	600 200 150	750 300 220	ns
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns	t_{PHL}	5.0 10 15	— — —	485 200 160	970 400 320	ns
Propagation Delay Time — $\overline{LT}$ Input [7.] t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns t_{PLH} = (0.20 ns/pF) C_L + 80 ns	t_{PLH}	5.0 10 15	— — —	313 125 90	625 250 180	ns
t_{PHL} = (1.3 ns/pF) C_L + 248 ns t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns	t_{PHL}	5.0 10 15	— — —	313 125 90	625 250 180	ns
Setup Time	t_{su}	5.0 10 15	100 40 30	— — —	— — —	ns
Hold Time	t_h	5.0 10 15	60 40 30	— — —	— — —	ns
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0 10 15	520 220 130	260 110 65	— — —	ns

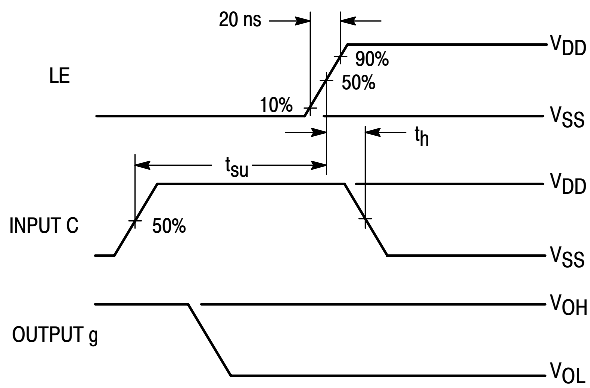
7. The formulas given are for the typical characteristics only.



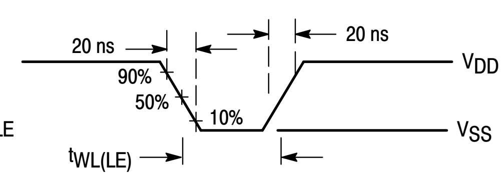
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{BI}$ and $\overline{LT}$ high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

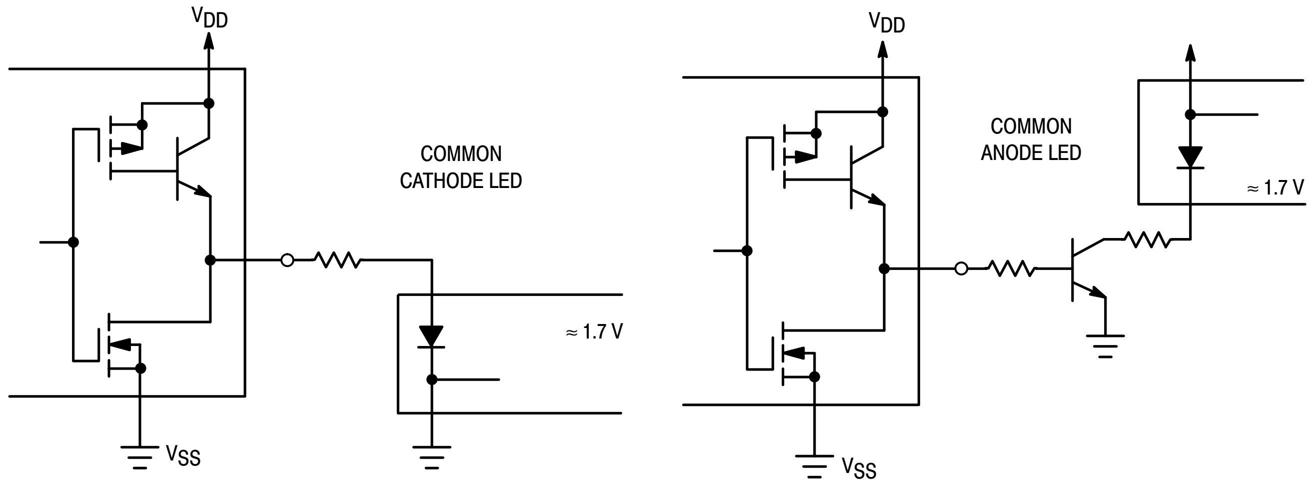


d. Pulse Width: Data DCBA strobed into latches.

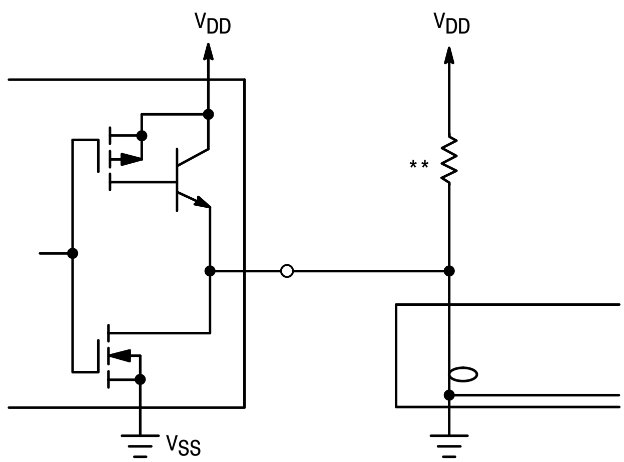
Figure 2. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

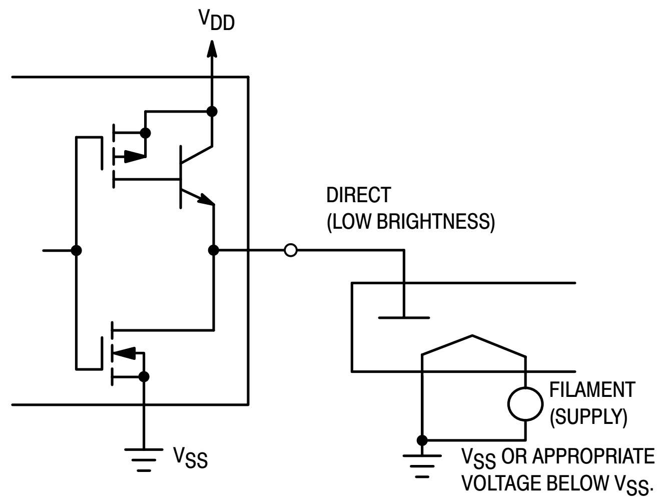
LIGHT EMITTING DIODE (LED) READOUT



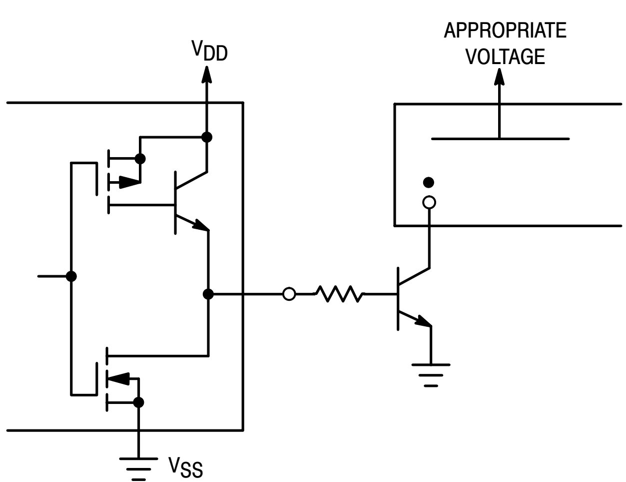
INCANDESCENT READOUT



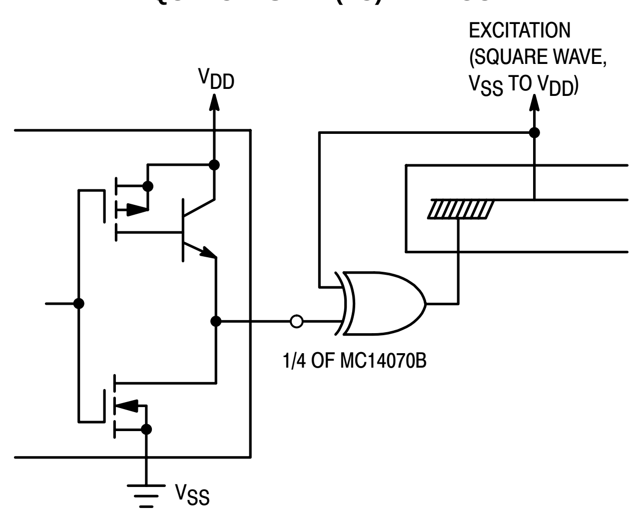
FLUORESCENT READOUT



GAS DISCHARGE READOUT



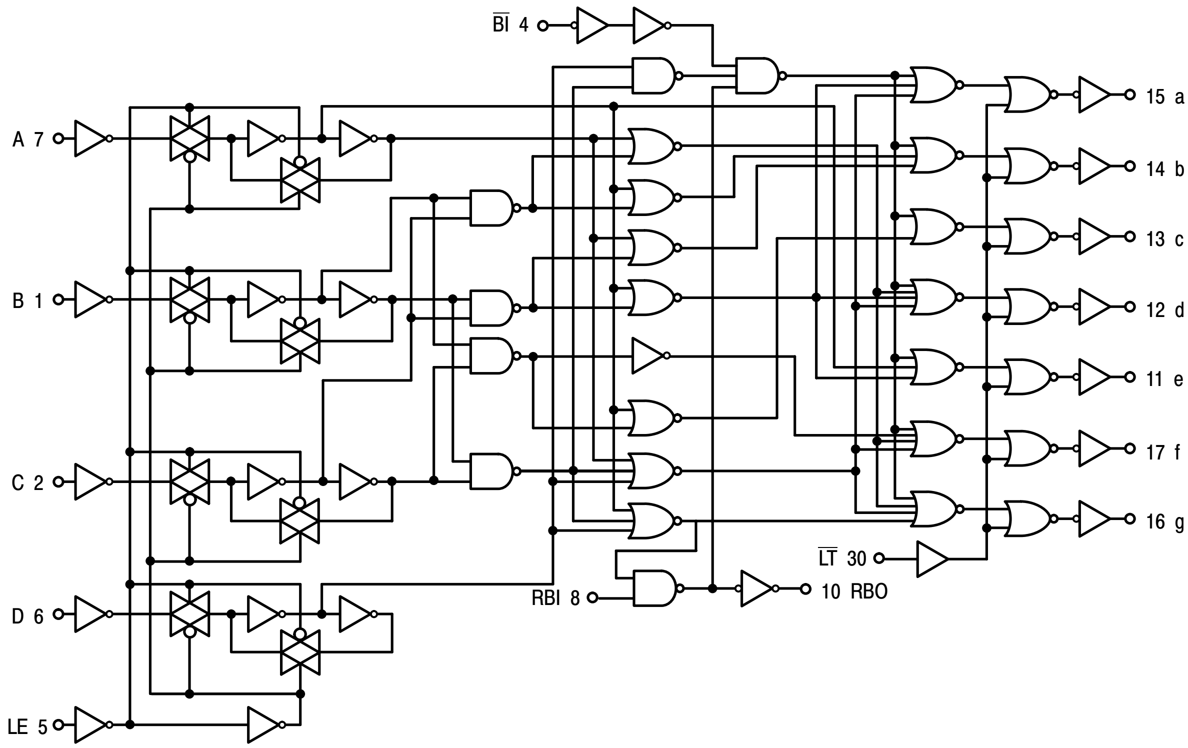
LIQUID CRYSTAL (LC) READOUT



** A filament pre−warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

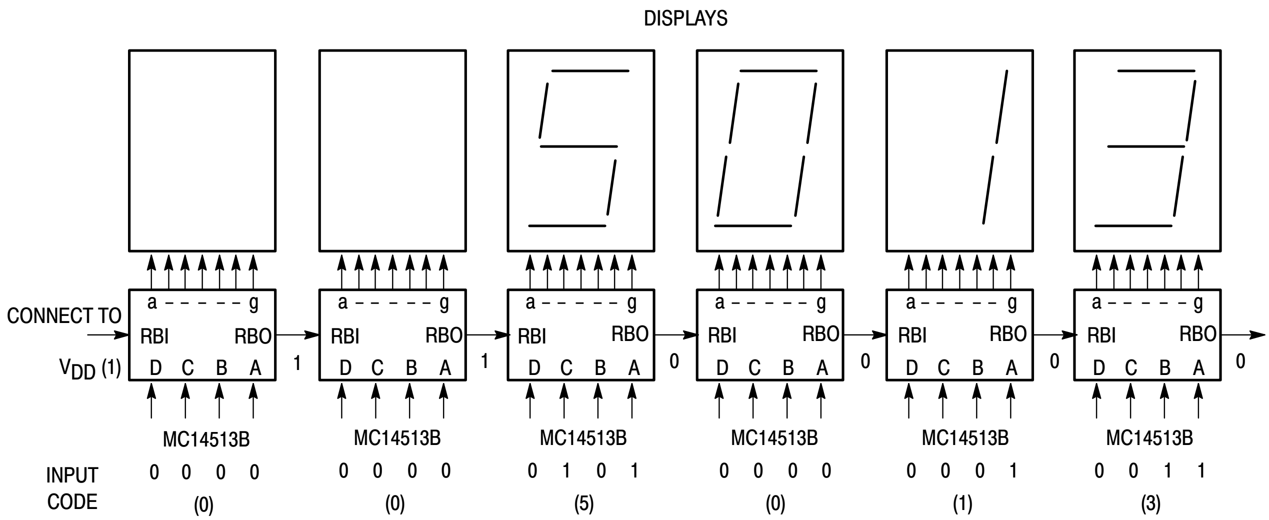
Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM

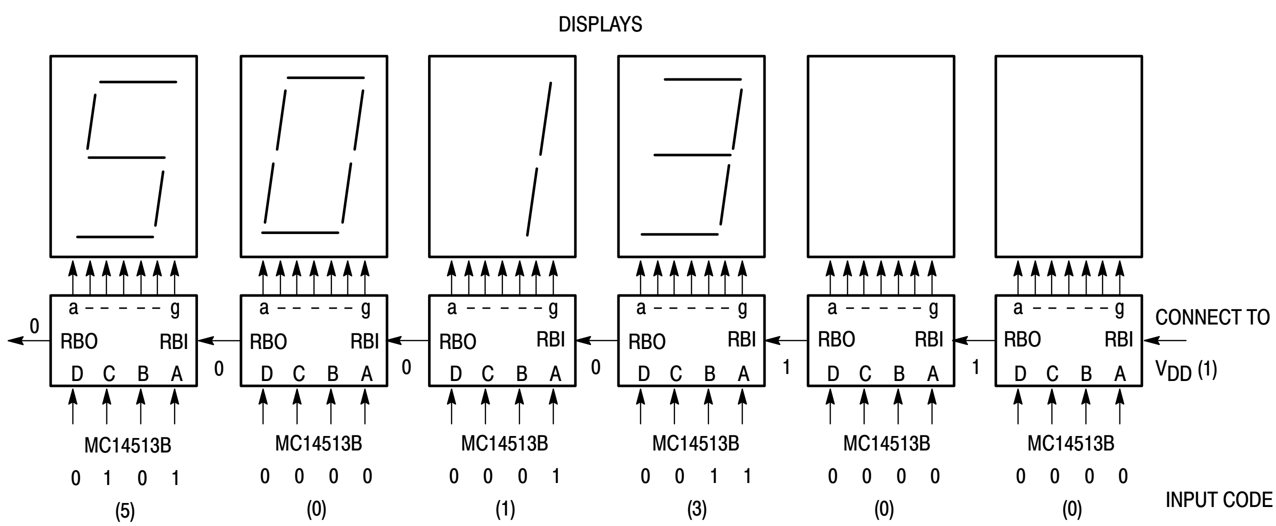


TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



TRAILING EDGE ZERO SUPPRESSION



MC14514B, MC14515B

4-Bit Transparent Latch/4-to-16 Line Decoder

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical “1” at the selected output, whereas the MC14515B (output active low option) presents a logical “0” at the selected output. The latches are R−S type flip−flops which hold the last input data presented prior to the strobe transition from “1” to “0”. These high and low options of a 4−bit latch/4 to 16 line decoder are constructed with N−channel and P−channel enhancement mode devices in a single monolithic structure. The latches are R−S type flip−flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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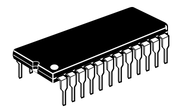
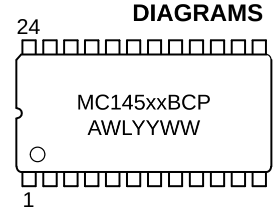
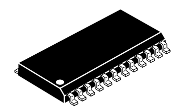


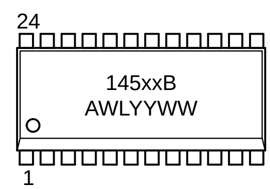
MARKING DIAGRAMS

PDIP−24
P SUFFIX
CASE 709





SOIC−24
DW SUFFIX
CASE 751E



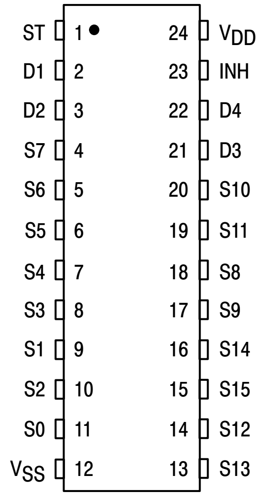
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14514BCP	PDIP−24	15/Rail
MC14514BDW	SOIC−24	30/Rail
MC14514BDWR2	SOIC−24	1000/Tape & Reel
MC14515BCP	PDIP−24	15/Rail
MC14515BDW	SOIC−24	30/Rail
MC14515BDWR2	SOIC−24	1000/Tape & Reel

August, 2000 − Rev. 4
Publication Order Number:
MC14514B/D

PIN ASSIGNMENT

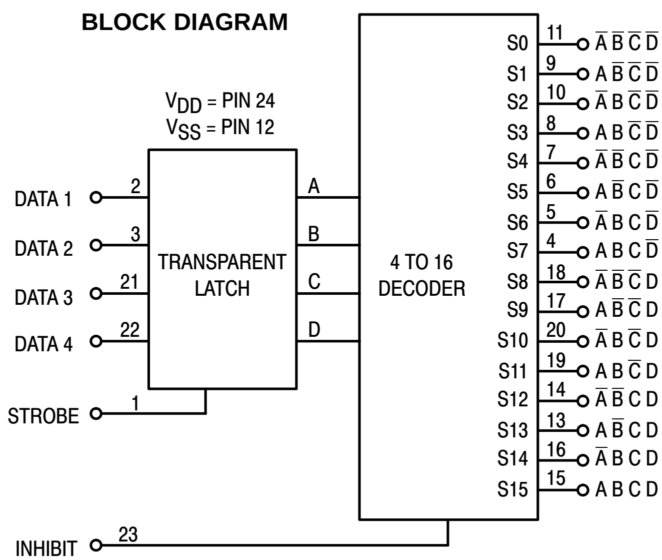


DECODE TRUTH TABLE (Strobe = 1)*

Inhibit	Data Inputs D	C	B	A	Selected Output MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care
*Strobe = 0, Data is latched

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	 5.0 10 15	 3.5 7.0 11	 — — —	 3.5 7.0 11	 2.75 5.50 8.25	 — — —	 3.5 7.0 11	 — — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 – 1.2 – 0.25 – 0.62 – 1.8	 — — — —	 – 1.0 – 0.2 – 0.5 – 1.5	 – 1.7 – 0.36 – 0.9 – 3.5	 — — — —	 – 0.7 – 0.14 – 0.35 – 1.1	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_{TL}	5.0 10 15	I_T = (1.35 µA/kHz) f + I_{DD} I_T = (2.70 µA/kHz) f + I_{DD} I_T = (4.05 µA/kHz) f + I_{DD}							µAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\,Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ (7.)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time; Data, Strobe to S	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	—	550	1100	
t_{PLH}, t_{PHL} = (0.86 ns/pF) C_L + 192 ns		10	—	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	—	150	300	
Inhibit Propagation Delay Times	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	—	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
Setup Time	t_{su}					ns
Data to Strobe		5.0	250	125	—	
		10	100	50	—	
		15	75	38	—	
Hold Time	t_h	5.0	– 20	– 100	—	ns
Strobe to Data		10	0	– 40	—	
		15	10	– 30	—	
Strobe Pulse Width	t_{WH}					ns
		5.0	350	175	—	
		10	100	50	—	
		15	75	38	—	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

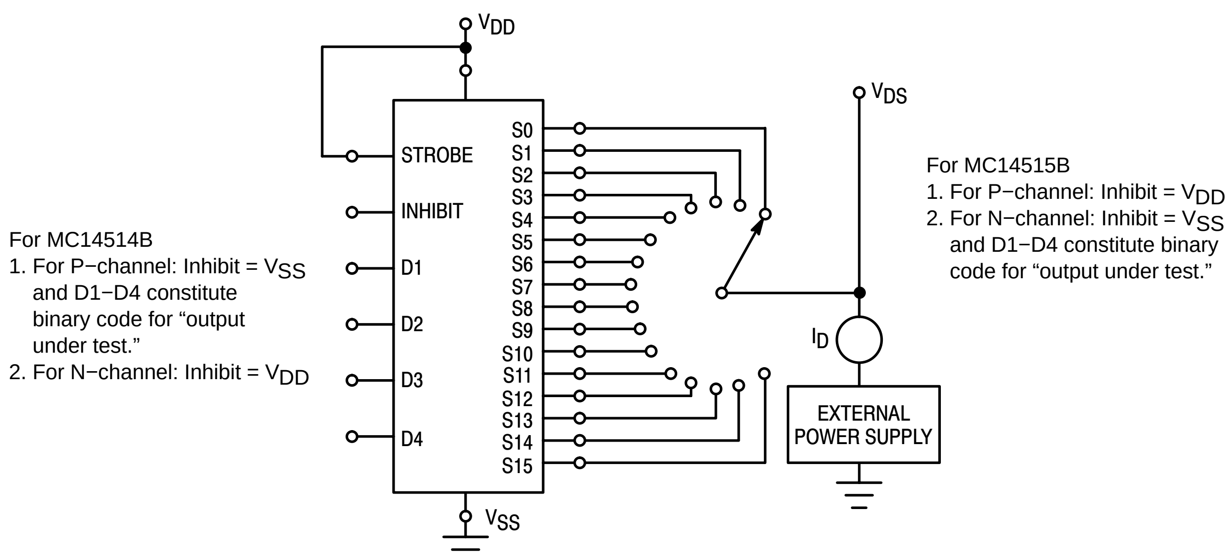


Figure 1. Drain Characteristics Test Circuit

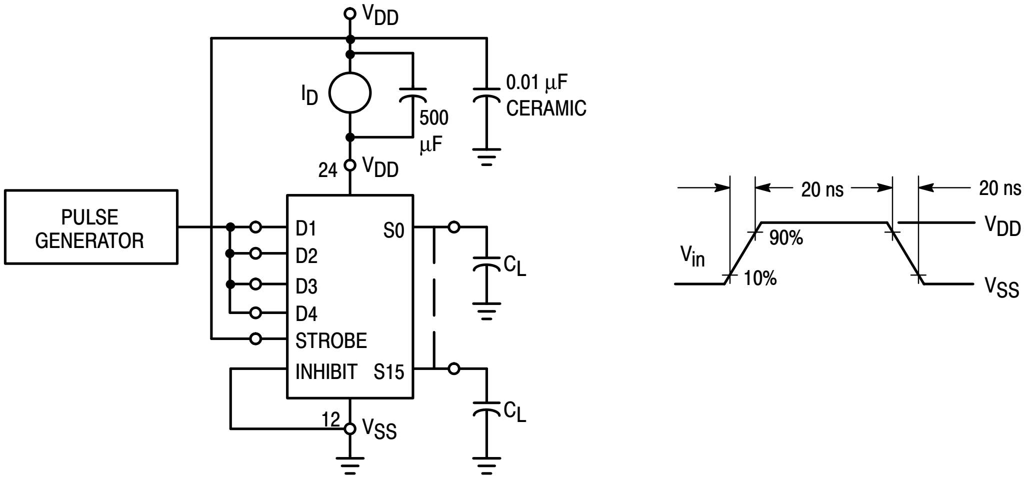


Figure 2. Dynamic Power Dissipation Test Circuit and Waveform

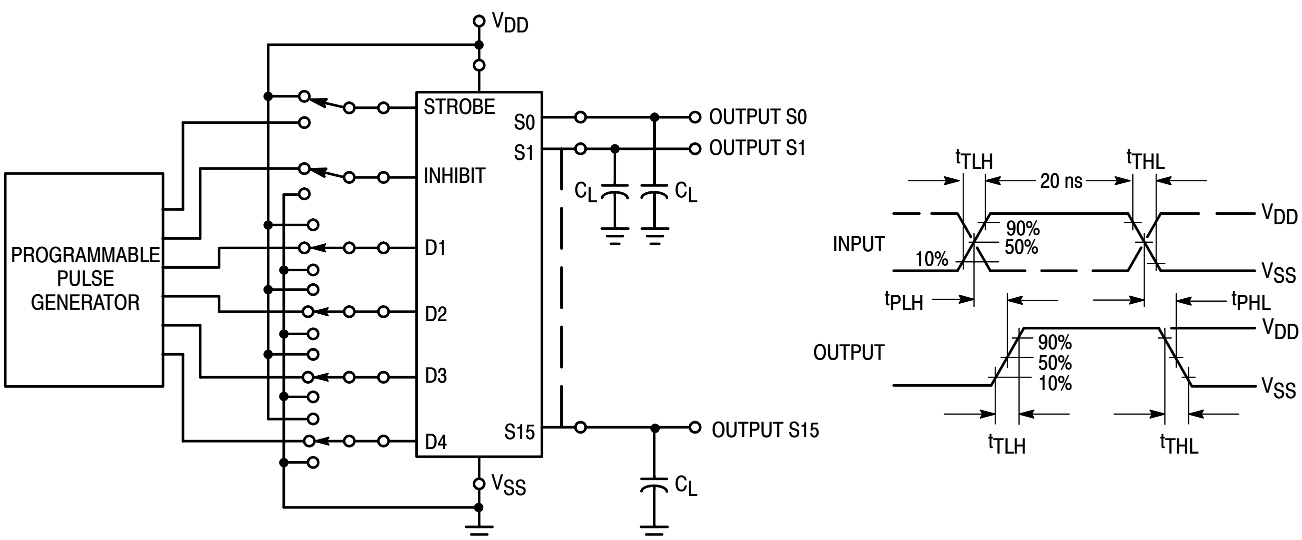
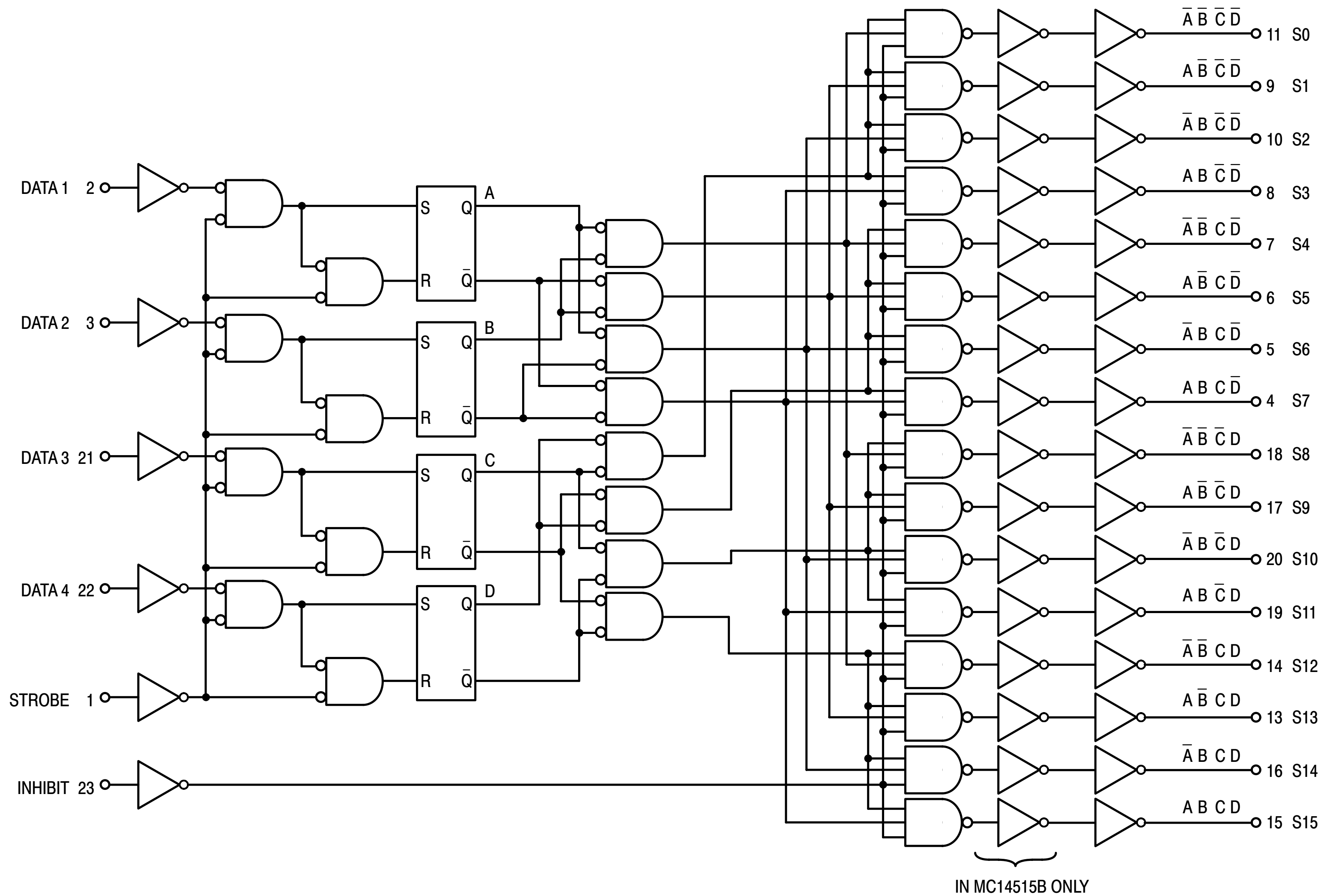


Figure 3. Switching Time Test Circuit and Waveforms

LOGIC DIAGRAM



COMPLEX DATA ROUTING

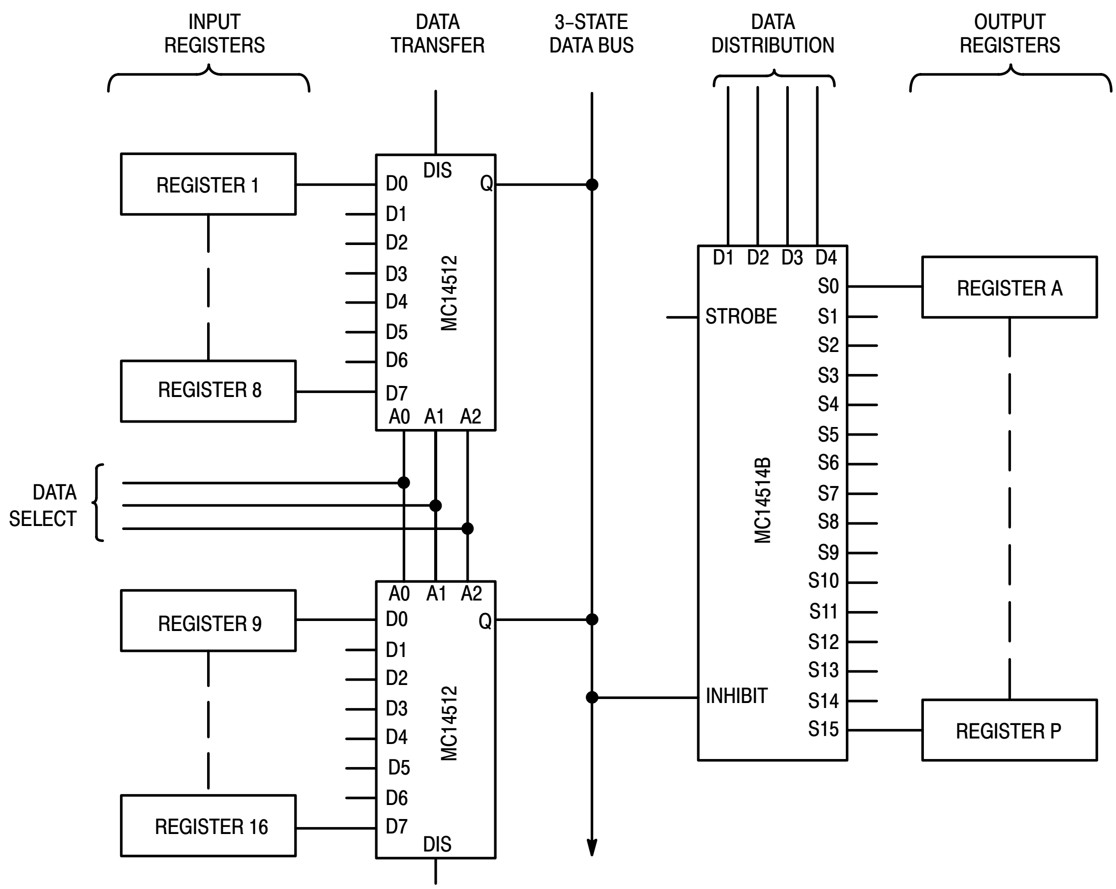
Two MC14512 eight−channel data selectors are used here with the MC14514B four−bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3−state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re−routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3−state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster then the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3−state bus is redistributed by the MC14514B four−bit latch/decoder. Using the four−bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM



MC14516B

Binary Up/Down Counter

The MC14516B synchronous up/down binary counter is constructed with MOS P−channel and N−channel enhancement mode devices in a monolithic structure.

This counter can be preset by applying the desired value, in binary, to the Preset inputs (P0, P1, P2, P3) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the $\overline{\text{Carry Out}}$ to the $\overline{\text{Carry In}}$ of the next stage while clocking each counter in parallel. The outputs (Q0, Q1, Q2, Q3) can be reset to a low state by applying a high to the reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog−to−digital and digital−to−analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge−Clocked Design — Count Occurs on Positive Going Edge of Clock
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

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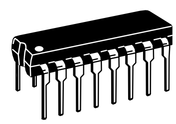
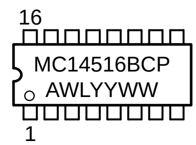
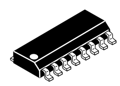
MARKING DIAGRAMS

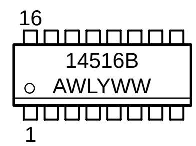


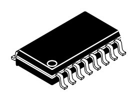
PDIP−16
P SUFFIX
CASE 648



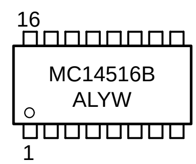


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14516BCP	PDIP−16	2000/Box
MC14516BD	SOIC−16	48/Rail
MC14516BDR2	SOIC−16	2500/Tape & Reel
MC14516BF	SOEIAJ−16	See Note 1.
MC14516BFEL	SOEIAJ−16	See Note 1.

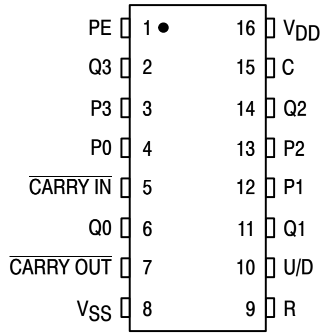
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

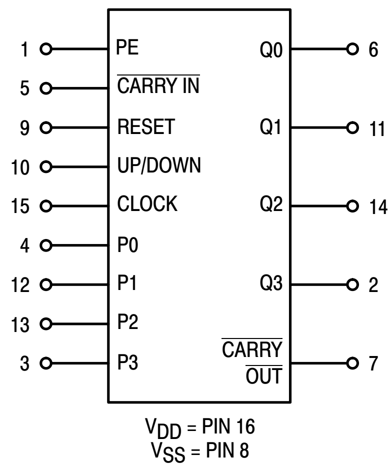
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

August, 2000 − Rev. 4
Publication Order Number:
MC14516B/D

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0	↑	Count Up
0	0	0	0	↑	Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

NOTE: When counting up, the $\overline{\text{Carry Out}}$ signal is normally high and is low only when Q0 through Q3 are high and $\overline{\text{Carry In}}$ is low. When counting down, $\overline{\text{Carry Out}}$ is low only when Q0 through Q3 and $\overline{\text{Carry In}}$ are low.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.58 µA/kHz) f + I_{DD} I_T = (1.20 µA/kHz) f + I_{DD} I_T = (1.70 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ (8.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 260 200	ns
Clock to $\overline{\text{Carry Out}}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 260 200	ns
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	180 80 60	360 160 120	ns
Preset or Reset to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 360 200	ns
Preset or Reset to $\overline{\text{Carry Out}}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	550 225 150	1100 450 300	ns
Reset Pulse Width	t_w	5.0 10 15	380 200 160	190 100 80	— — —	ns
Clock Pulse Width	t_{WH}	5.0 10 15	350 170 140	200 100 75	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an Indication of the IC’s potential performance.

SWITCHING CHARACTERISTICS [9.] (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ [10.]	All Types Max	Unit
Preset or Reset Removal Time The Preset or Reset signal must be low prior to a positive−going transition of the clock.	t_{rem}	5.0 10 15	650 230 180	325 115 90	— —	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	µs
Setup Time Carry In to Clock	t_{su}	5.0 10 15	260 120 100	130 60 50	— — —	ns
Hold Time Clock to Carry In	t_h	5.0 10 15	0 20 20	– 60 – 20 0	— — —	ns
Setup Time Up/Down to Clock	t_{su}	5.0 10 15	500 200 150	250 100 75	— — —	ns
Hold Time Clock to Up/Down	t_h	5.0 10 15	– 70 – 10 0	– 160 – 60 – 40	— — —	ns
Setup Time Pn to PE	t_{su}	5.0 10 15	– 40 – 30 – 25	– 120 – 70 – 50	— — —	ns
Hold Time PE to Pn	t_h	5.0 10 15	480 420 420	240 210 210	— — —	ns
Preset Enable Pulse Width	t_{WH}	5.0 10 15	200 100 80	100 50 40	— — —	ns

9. The formulas given are for the typical characteristics only at 25°C.
10. Data labelled “Typ” is not to be used for design purposes but is intended as an Indication of the IC’s potential performance.

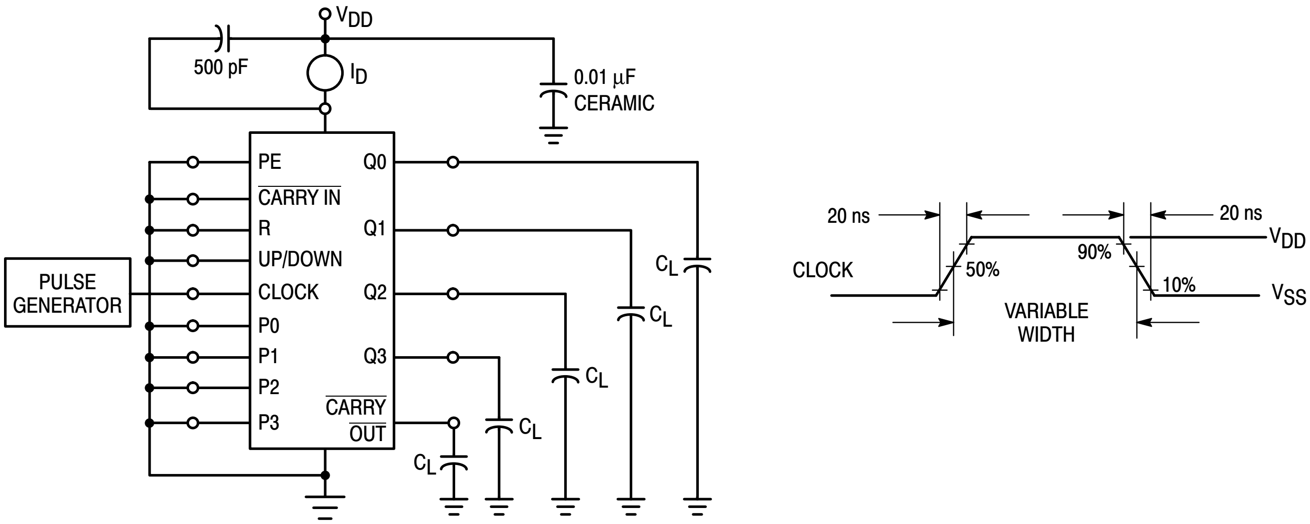
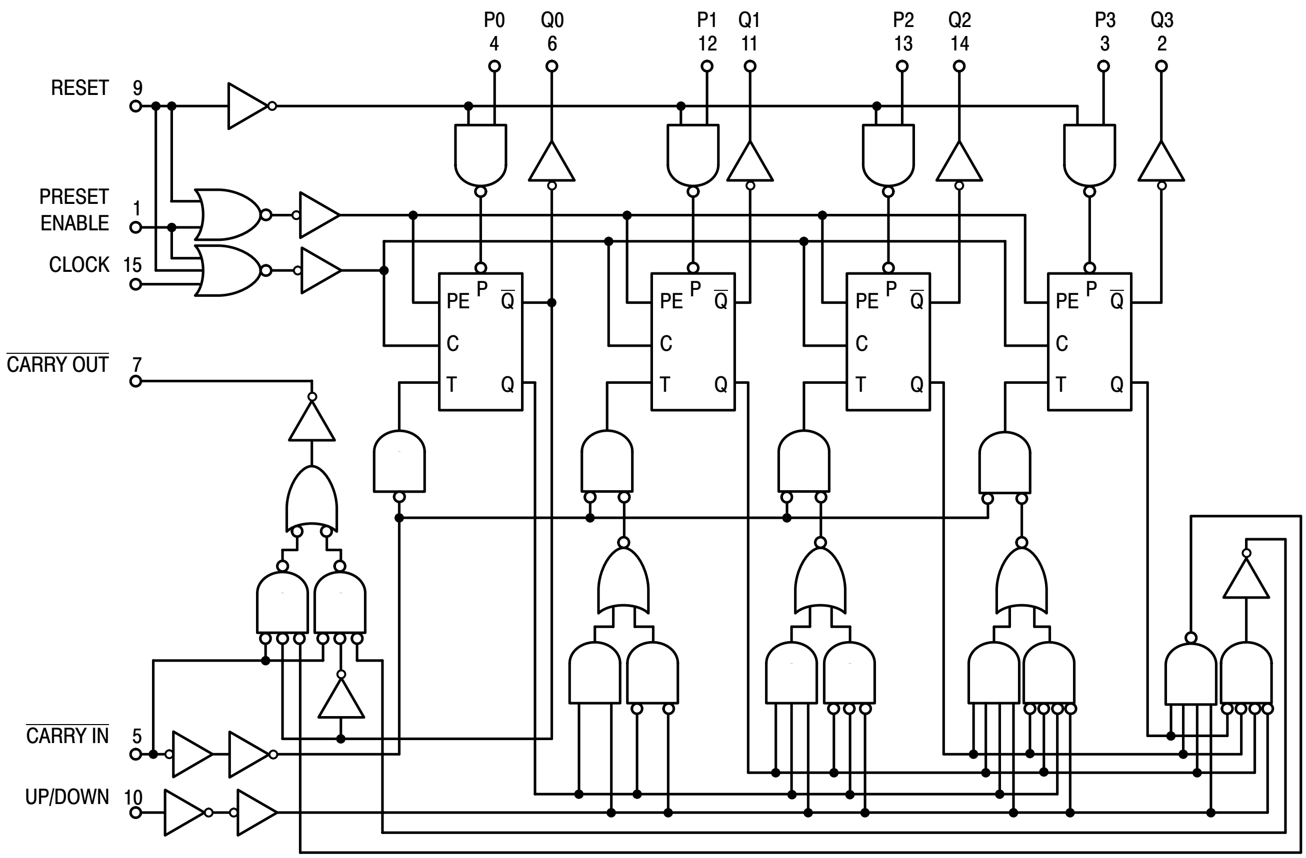
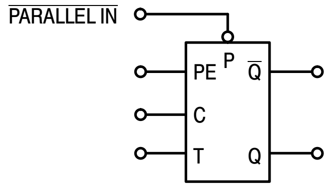


Figure 1. Power Dissipation Test Circuit and Waveform

LOGIC DIAGRAM



TOGGLE FLIP−FLOP



FLIP−FLOP FUNCTIONAL TRUTH TABLE

Preset Enable	Clock	T	Q_{n+1}
1	X	X	Parallel In
0	rising edge	0	Q_n
0	rising edge	1	$\overline{Q}_n$
0	falling edge	X	Q_n

X = Don't Care

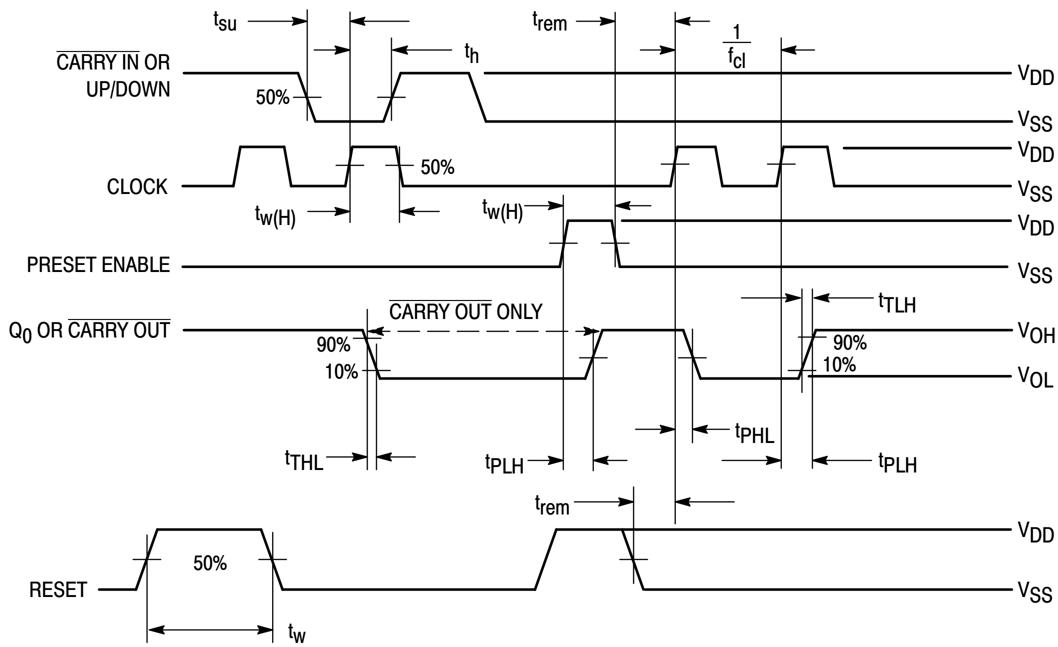


Figure 2. Switching Time Waveforms

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

$\overline{\text{Carry In}}$, (Pin 5) — This active−low input is used when Cascading stages. $\overline{\text{Carry In}}$ is usually connected to $\overline{\text{Carry Out}}$ of the previous stage. While high, Clock is inhibited.

Clock, (Pin 15) — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

OUTPUTS

Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2) — Binary data is present on these outputs with Q0 corresponding to the least significant bit.

$\overline{\text{Carry Out}}$, (Pin 7) — Used when cascading stages, $\overline{\text{Carry Out}}$ is usually connected to $\overline{\text{Carry In}}$ of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable, (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

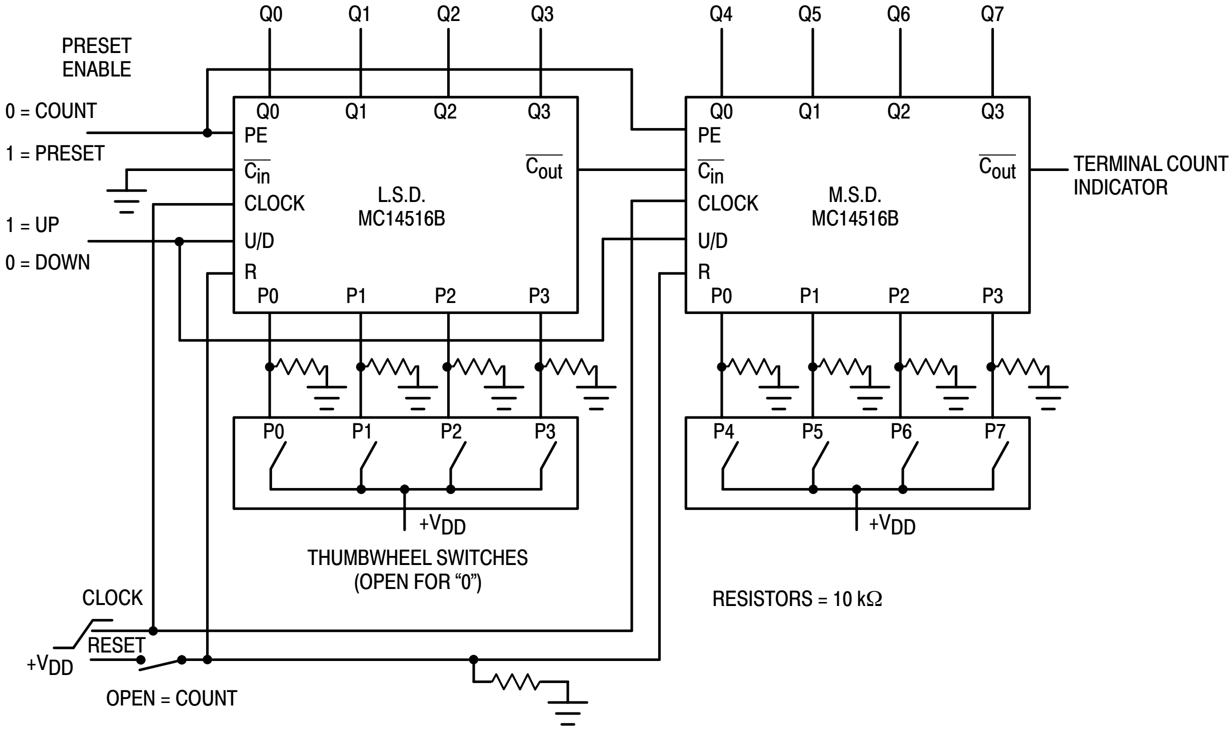
R, Reset, (Pin 9) — Asynchronously resets the Q out−puts to a low state. This pin is active high and inhibits the clock when high.

Up/Down, (Pin 10) — Controls the direction of count, high for up count, low for down count.

SUPPLY PINS

V_{SS}, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

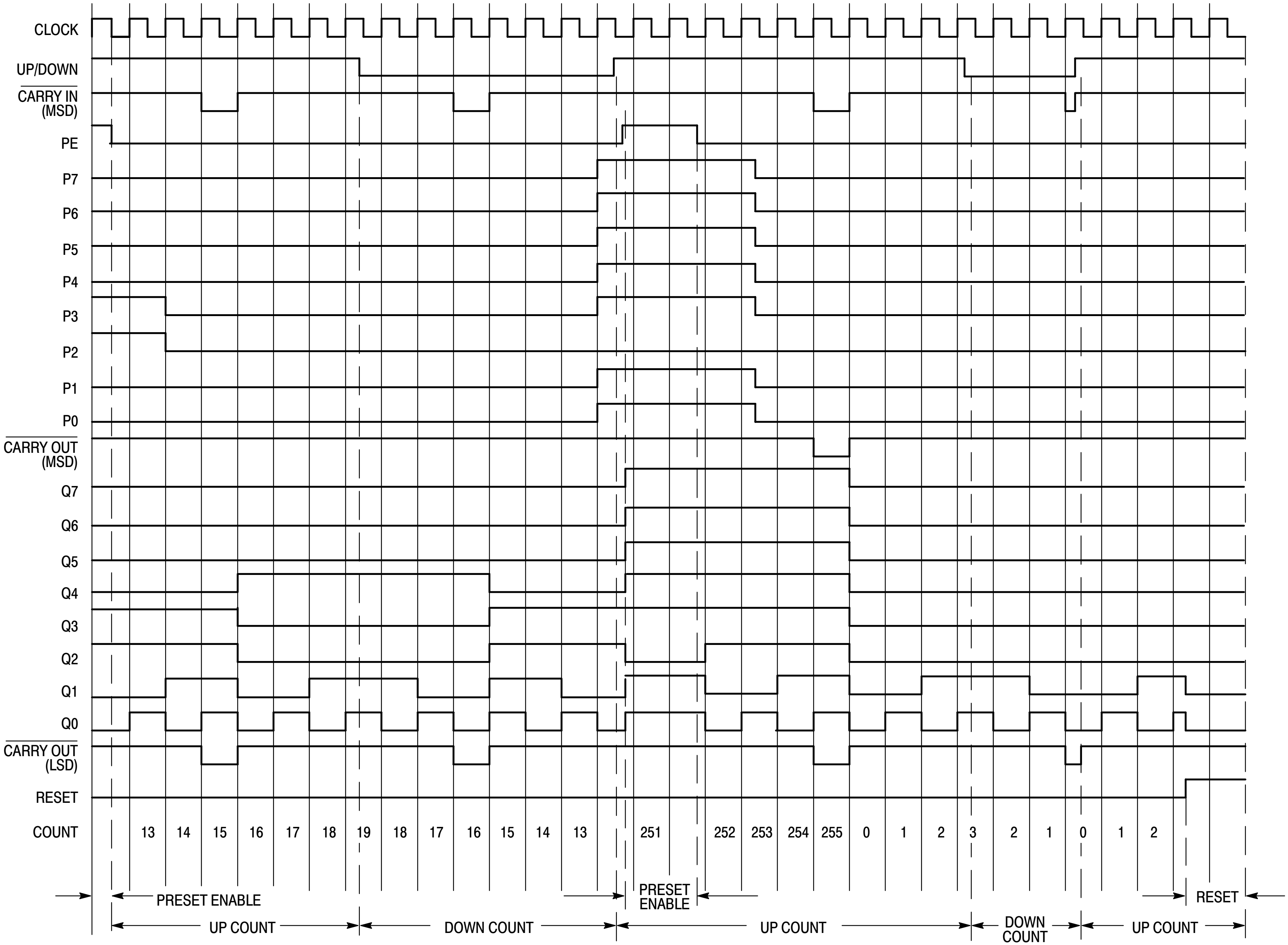
V_{DD}, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

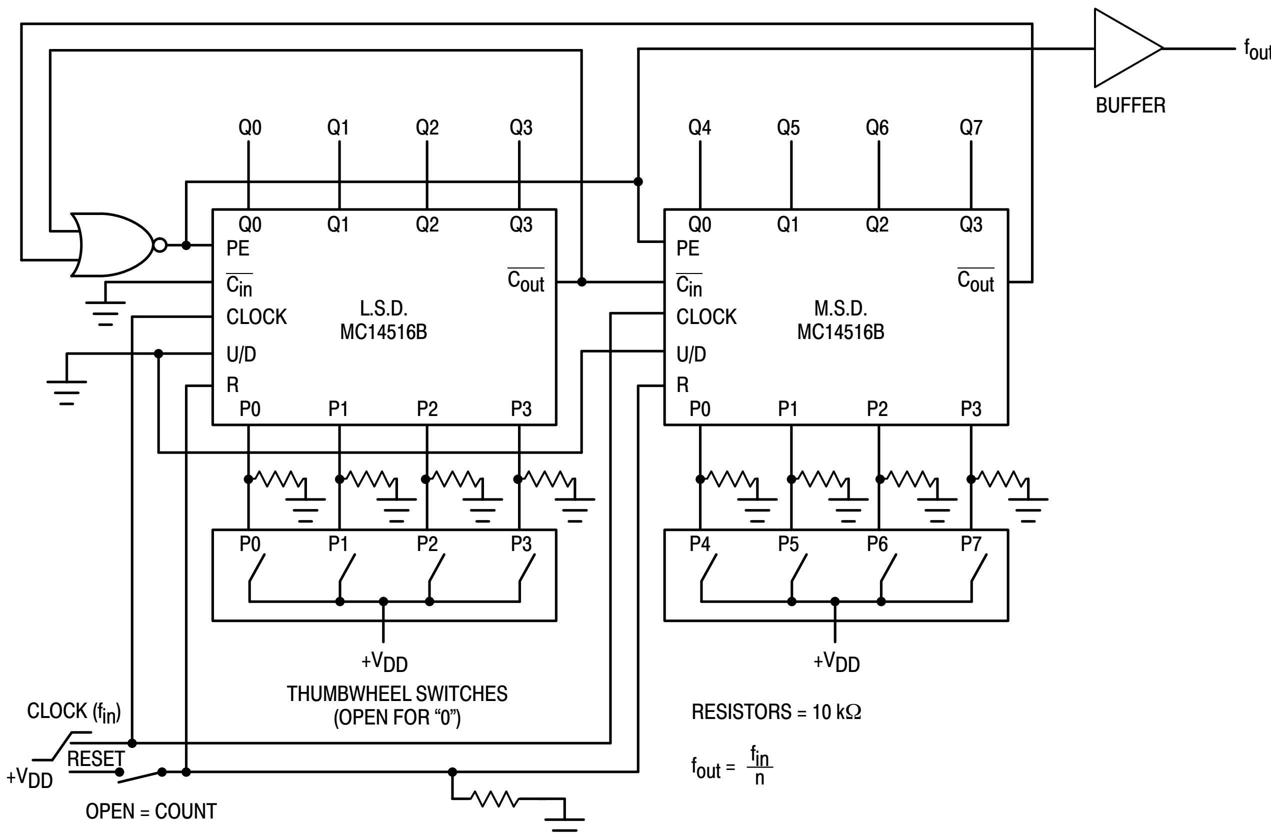


NOTE: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while $\overline{C_{in}}$ is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode), $\overline{C_{out}}$ goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.

Figure 3. Presettable Cascaded 8−Bit Up/Down Counter

TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8–BIT UP/DOWN COUNTER





NOTE: The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.

Figure 4. Programmable Cascaded Frequency Divider

MC14517B

Dual 64-Bit Static Shift Register

The MC14517B dual 64−bit static shift register consists of two identical, independent, 64−bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16−bit, 32−bit, and 48−bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3−State Output at 64th−Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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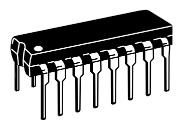
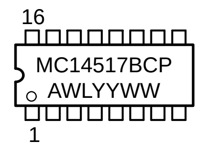
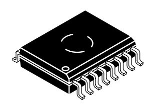
MARKING DIAGRAMS

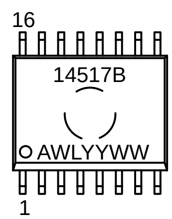


PDIP−16
P SUFFIX
CASE 648





SOIC−16
DW SUFFIX
CASE 751G

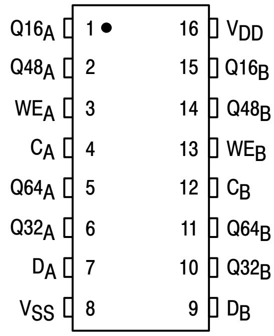


A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14517BCP	PDIP−16	2000/Box
MC14517BDW	SOIC−16	47/Rail
MC14517BDWR2	SOIC−16	1000/Tape & Reel

PIN ASSIGNMENT



FUNCTIONAL TRUTH TABLE (X = Don’t Care)

Clock	Write Enable	Data	16−Bit Tap	32−Bit Tap	48−Bit Tap	64−Bit Tap
0	0	X	Content of 16−Bit Displayed	Content of 32−Bit Displayed	Content of 48−Bit Displayed	Content of 64−Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16−Bit Displayed	Content of 32−Bit Displayed	Content of 48−Bit Displayed	Content of 64−Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
_/‾	0	Data entered into 1st Bit	Content of 16−Bit Displayed	Content of 32−Bit Displayed	Content of 48−Bit Displayed	Content of 64−Bit Displayed
_/‾	1	Data entered into 1st Bit	Data at tap entered into 17−Bit	Data at tap entered into 33−Bit	Data at tap entered into 49−Bit	High Impedance
‾_	0	X	Content of 16−Bit Displayed	Content of 32−Bit Displayed	Content of 48−Bit Displayed	Content of 64−Bit Displayed
‾_	1	X	High Impedance	High Impedance	High Impedance	High Impedance

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (4.2 µA/kHz) f + I_{DD} I_T = (8.8 µA/kHz) f + I_{DD} I_T = (13.7 µA/kHz) f + I_{DD}							µAdc
Three−State Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (7.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.65 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 475 210 140	 770 300 215	ns
Clock Pulse Width	t_{WH}	5.0 10 15	330 125 100	170 75 60	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 6.7 8.3	1.5 4.0 5.3	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	See Note (8.)			—
Data to Clock Setup Time	t_{su}	5.0 10 15	0 10 15	– 40 – 15 0	— — —	ns
Data to Clock Hold Time	t_h	5.0 10 15	150 75 35	75 25 10	— — —	ns
Write Enable to Clock Setup Time	t_{su}	5.0 10 15	400 200 110	170 65 50	— — —	ns
Write Enable to Clock Release Time	t_{rel}	5.0 10 15	380 180 100	160 55 40	— — —	ns

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
8. When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

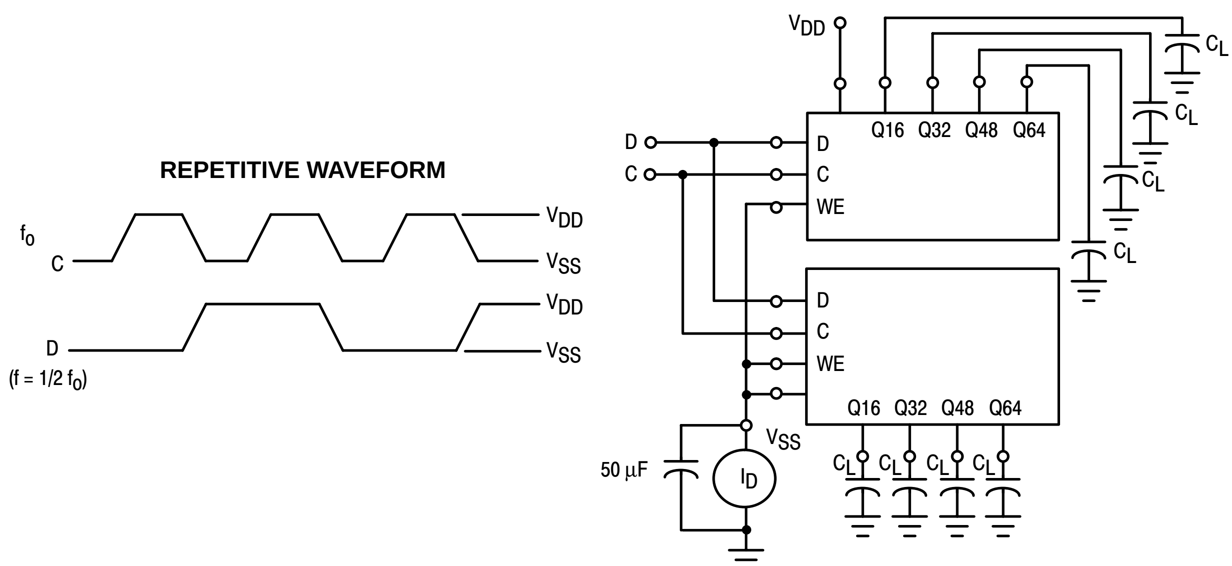
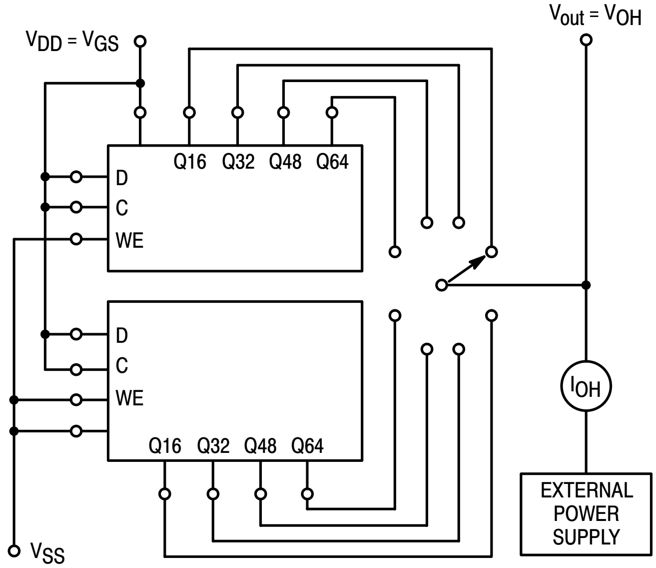
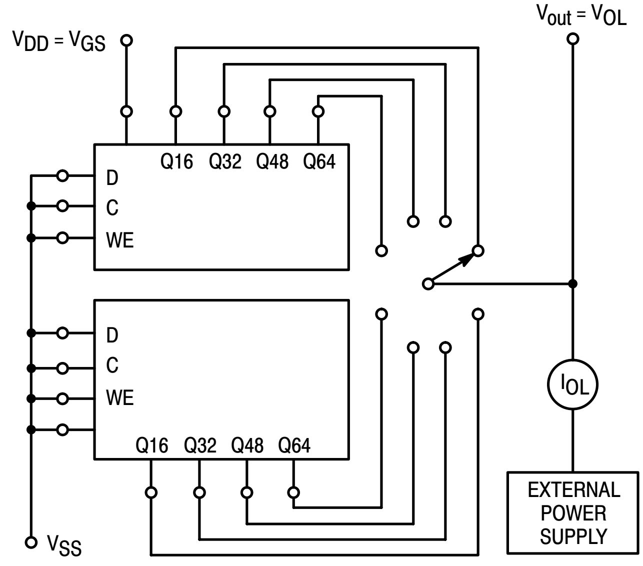


Figure 1. Power Dissipation Test Circuit and Waveform



(Output being tested should be in the high−logic state)

Figure 2. Typical Output Source Current Characteristics Test Circuit



(Output being tested should be in the low−logic state)

Figure 3. Typical Output Sink Current Characteristics Test Circuit

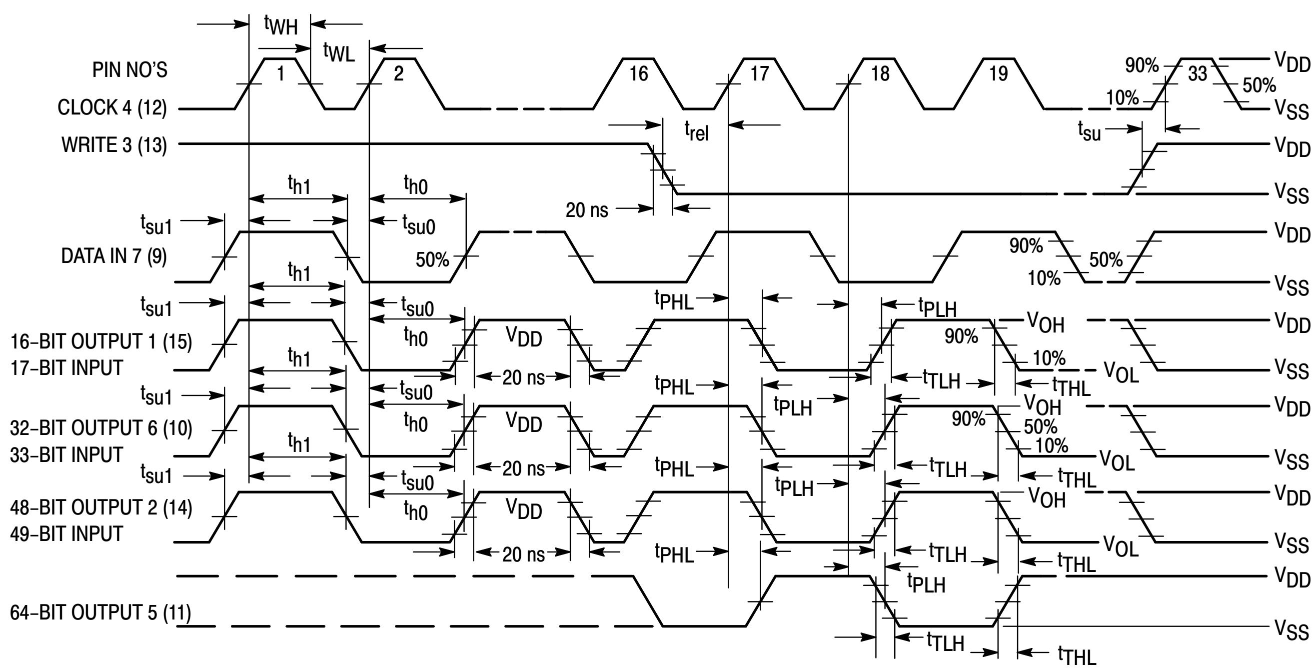
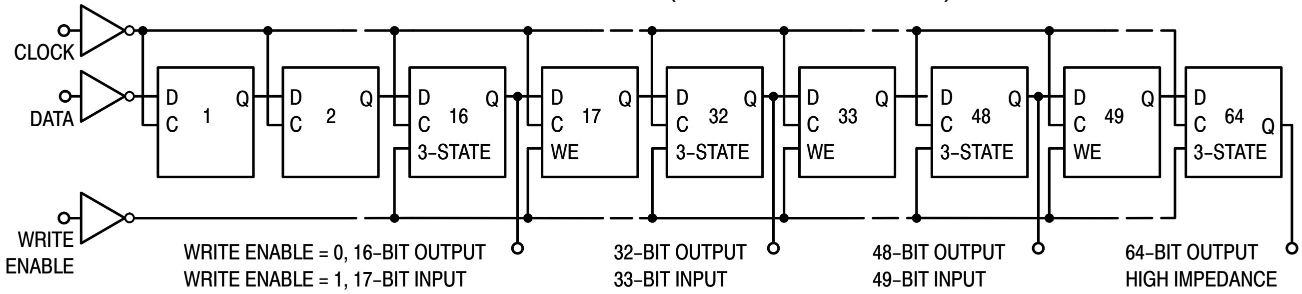


Figure 4. AC Test Waveforms

EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



MC14518B

Dual Up Counters

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4−stage counters. The counter stages are type D flip−flops, with interchangeable Clock and Enable lines for incrementing on either the positive−going or negative−going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi−stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge−Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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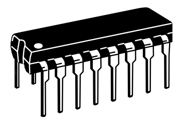
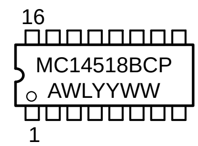
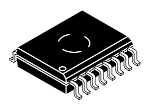
MARKING DIAGRAMS

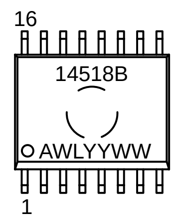


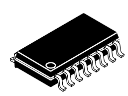
PDIP−16
P SUFFIX
CASE 648



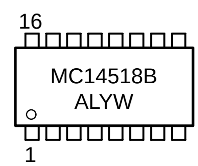


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



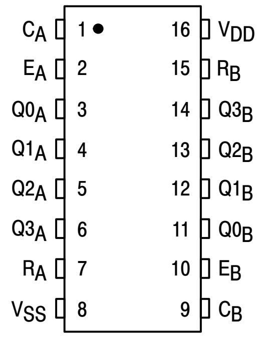
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

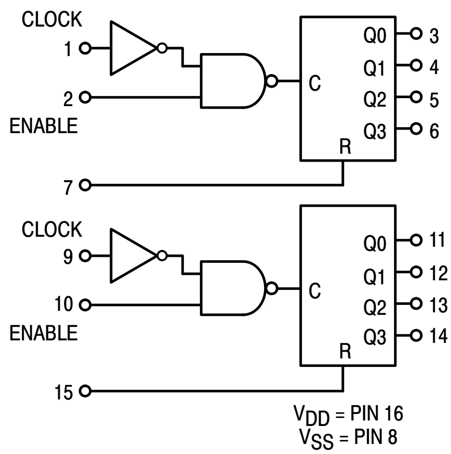
Device	Package	Shipping
MC14518BCP	PDIP−16	2000/Box
MC14518BDW	SOIC−16	47/Rail
MC14518BDWR2	SOIC−16	1000/Tape & Reel
MC14518BF	SOEIAJ−16	See Note 1.
MC14518BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

Clock	Enable	Reset	Action
_/‾	1	0	Increment Counter
0	‾_	0	Increment Counter
‾_	X	0	No Change
X	_/‾	0	No Change
_/‾	0	0	No Change
1	‾_	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don’t Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.6 µA/kHz) f + I_{DD} I_T = (1.2 µA/kHz) f + I_{DD} I_T = (1.7 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time Clock to Q/Enable to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	—	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	80	160	
Reset to Q	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	—	330	650	
t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	—	130	230	
t_{PHL} = (0.66 ns/pF) C_L + 95 ns		15	—	90	170	
Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$	5.0 10 15	200 100 70	100 50 35	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 6.0 8.0	1.5 3.0 4.0	MHz
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0 10 15	— — —	— — —	15 5 4	µs
Enable Pulse Width	$t_{WH(E)}$	5.0 10 15	440 200 140	220 100 70	— — —	ns
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	280 120 90	125 55 40	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	– 5 15 20	– 45 – 15 – 5	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

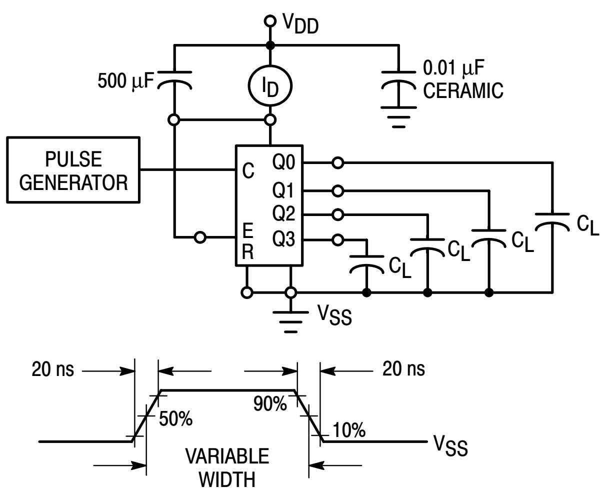


Figure 1. Power Dissipation Test Circuit and Waveform

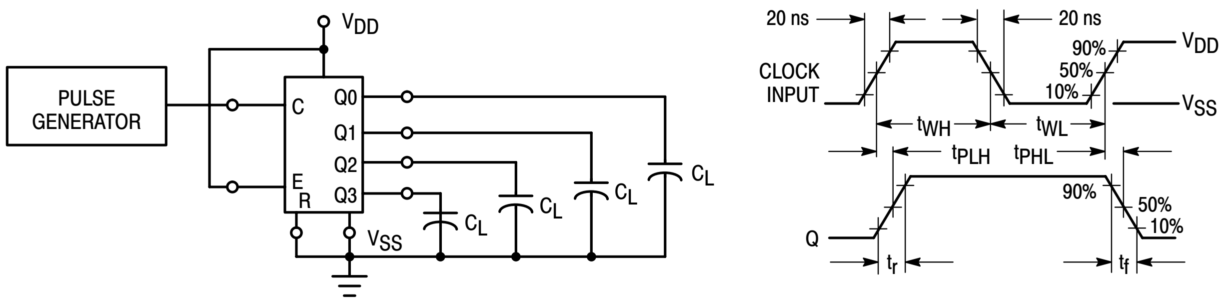


Figure 2. Switching Time Test Circuit and Waveforms

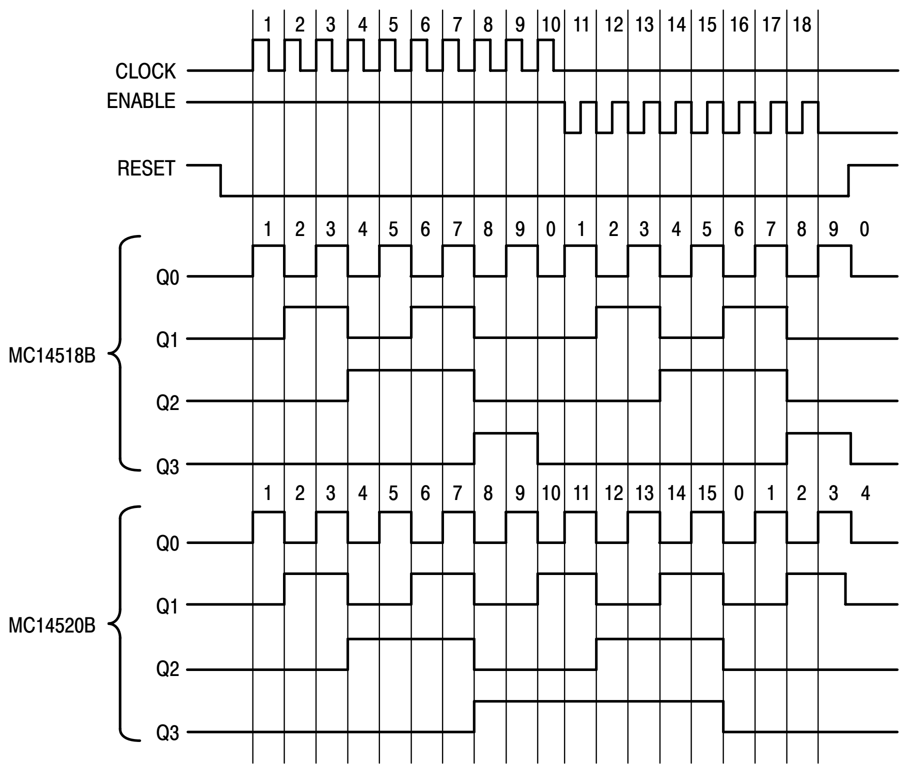


Figure 3. Timing Diagram

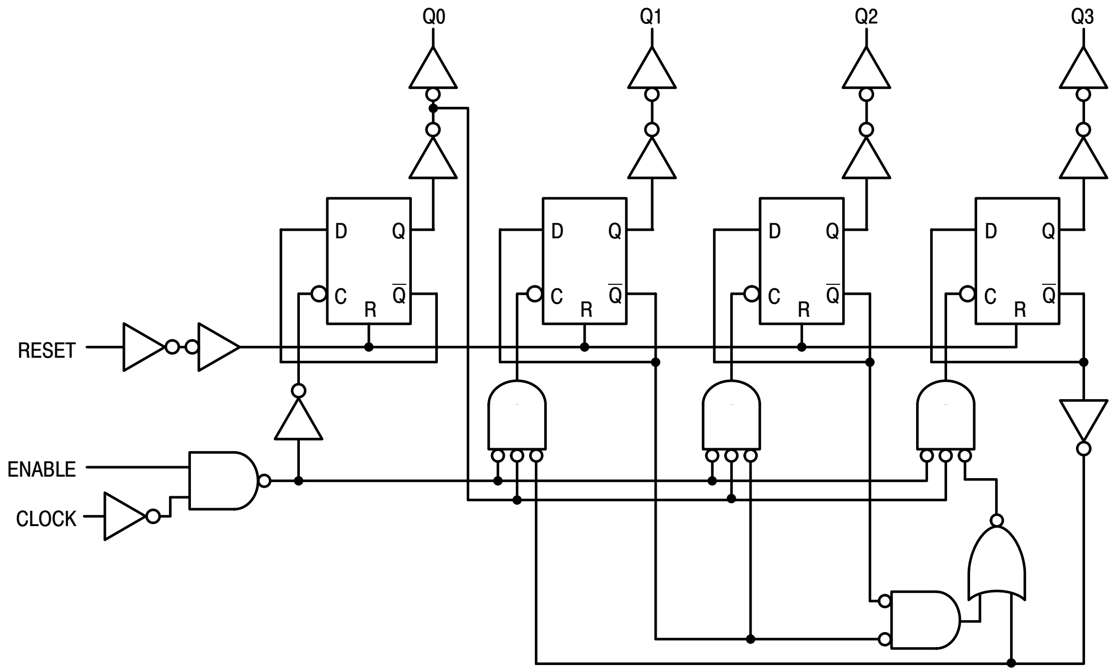


Figure 4. Decade Counter (MC14518B) Logic Diagram (1/2 of Device Shown)

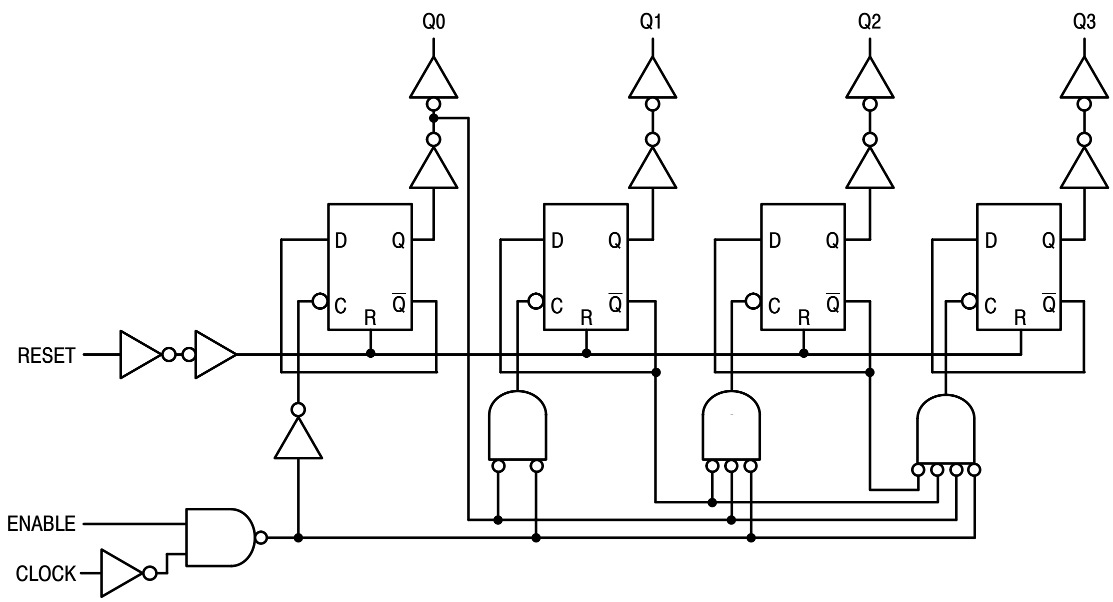


Figure 5. Binary Counter (MC14520B) Logic Diagram (1/2 of Device Shown)

MC14521B

24-Stage Frequency Divider

The MC14521B consists of a chain of 24 flip−flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip−flop divides the frequency of the previous flip−flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven−stages are available for added flexibility.

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low−Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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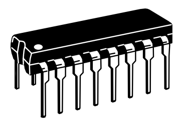
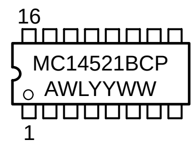
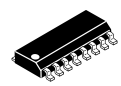
MARKING DIAGRAMS

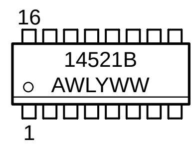


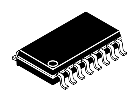
PDIP−16
P SUFFIX
CASE 648



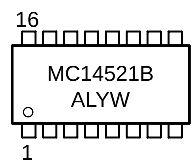


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



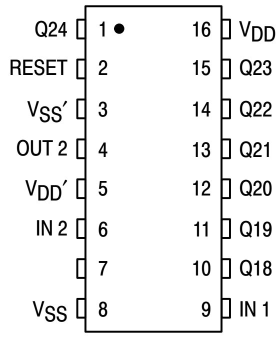
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

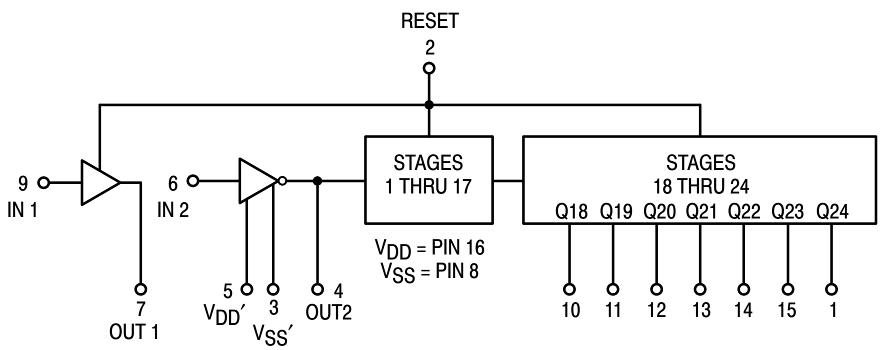
Device	Package	Shipping
MC14521BCP	PDIP−16	2000/Box
MC14521BD	SOIC−16	48/Rail
MC14521BDR2	SOIC−16	2500/Tape & Reel
MC14521BF	SOEIAJ−16	See Note 1.
MC14521BFEL	SOEIAJ−16	See Note 1.
MC14521BFR2	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



BLOCK DIAGRAM



Output	Count Capacity
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) Pins 4 & 7 (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	— — — —	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	— — — —	– 0.7 – 0.14 – 0.35 – 1.1	— — — —	mAdc
(V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) Pins 1, 10, (V_{OH} = 9.5 Vdc) 11, 12, 13, 14 (V_{OH} = 13.5 Vdc) and 15		5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.42 µA/kHz) f + I_{DD} I_T = (0.85 µA/kHz) f + I_{DD} I_T = (1.40 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

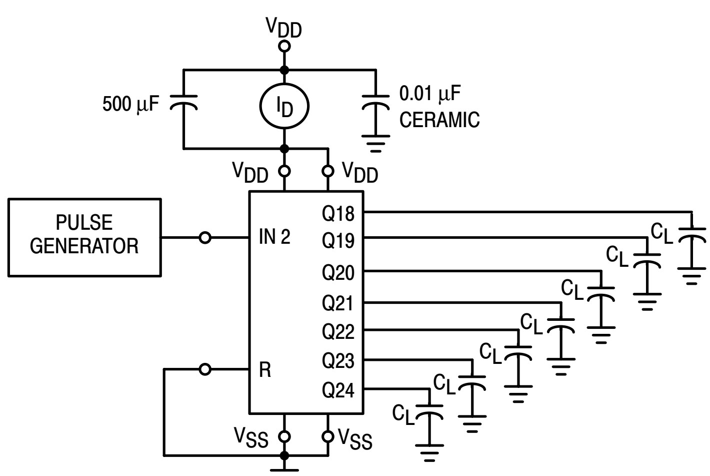
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time (Counter Outputs)	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	—	40	80	
Propagation Delay Time	t_{PHL}, t_{PLH}					µs
Clock to Q18						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	—	4.5	9.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	—	1.7	3.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1275 ns		15	—	1.3	2.7	
Clock to Q24						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	—	6.0	12	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	—	2.2	4.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1675 ns		15	—	1.7	3.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	—	1300	2600	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	—	500	1000	
t_{PHL} = (0.5 ns/pF) C_L + 350 ns		15	—	375	750	
Clock Pulse Width	$t_{WH(cl)}$	5.0	385	140	—	ns
		10	150	55	—	
		15	120	40	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.5	2.0	MHz
		10	—	9.0	5.0	
		15	—	12	6.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5.0	
		15	—	—	4.0	
Reset Pulse Width	$t_{WH(R)}$	5.0	1400	700	—	ns
		10	600	300	—	
		15	450	225	—	
Reset Removal Time	t_{rem}	5.0	30	– 200	—	ns
		10	0	– 160	—	
		15	– 40	– 110	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



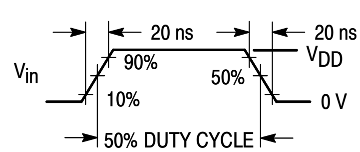


Figure 1. Power Dissipation Test Circuit and Waveform

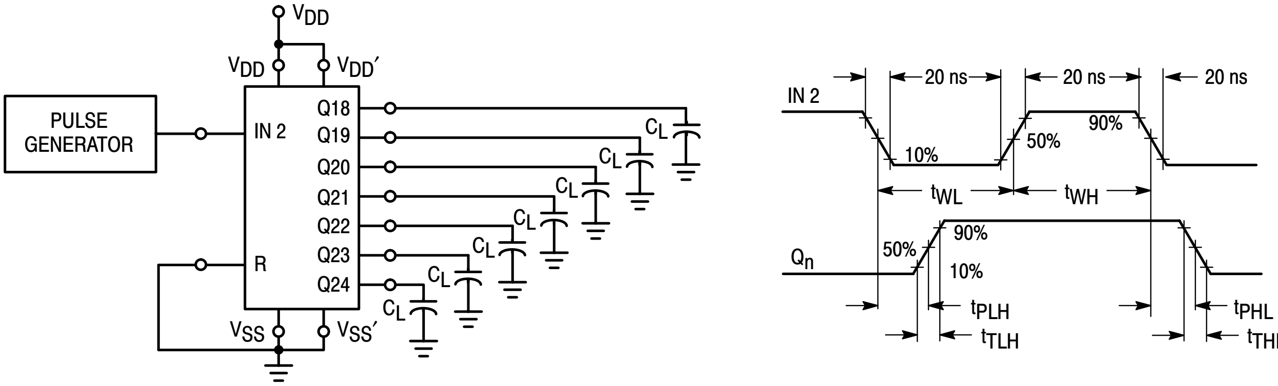
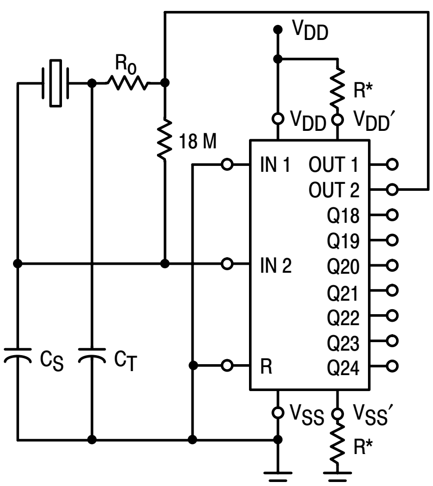


Figure 2. Switching Time Test Circuit and Waveforms



*Optional for low power operation,
10 kΩ ≤ R ≤ 70 kΩ.

Figure 3. Crystal Oscillator Circuit

Characteristic	500 kHz Circuit	50 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+ 6.0	+ 2.0	ppm
V_{DD} Change from 10 V to 15 V	+ 2.0	+ 2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from – 55°C to + 25°C			
MC14521 only	– 4.0	– 2.0	ppm
Complete Oscillator*	+ 100	+ 120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	– 2.0	– 2.0	ppm
Complete Oscillator*	– 160	– 560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

Figure 4. Typical Data for Crystal Oscillator Circuit

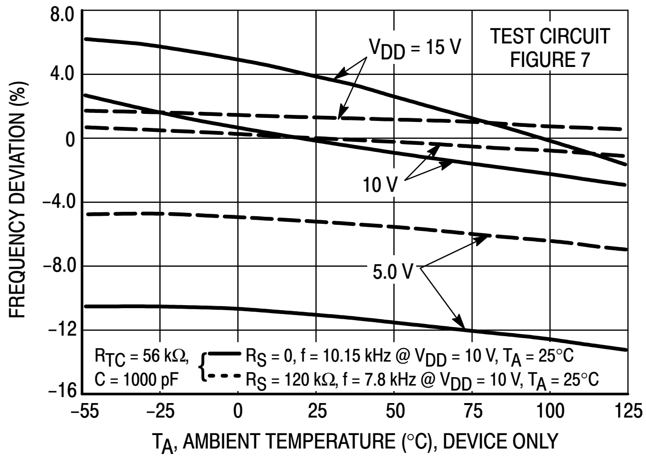


Figure 5. RC Oscillator Stability

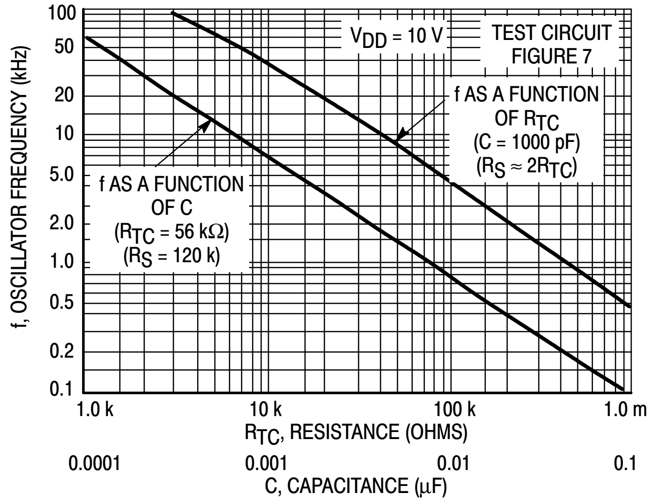


Figure 6. RC Oscillator Frequency as a Function of R_{TC} and C

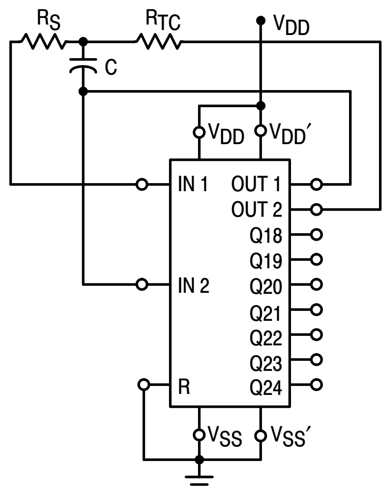


Figure 7. RC Oscillator Circuit

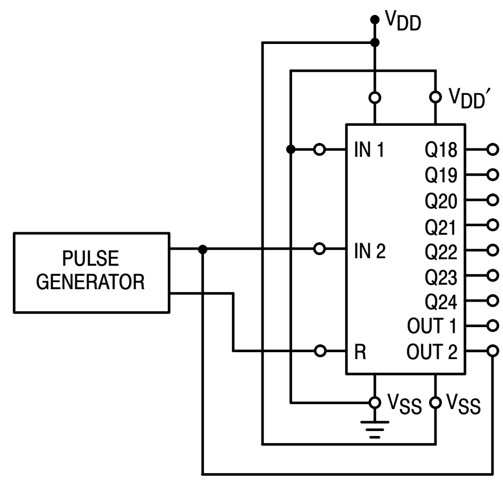


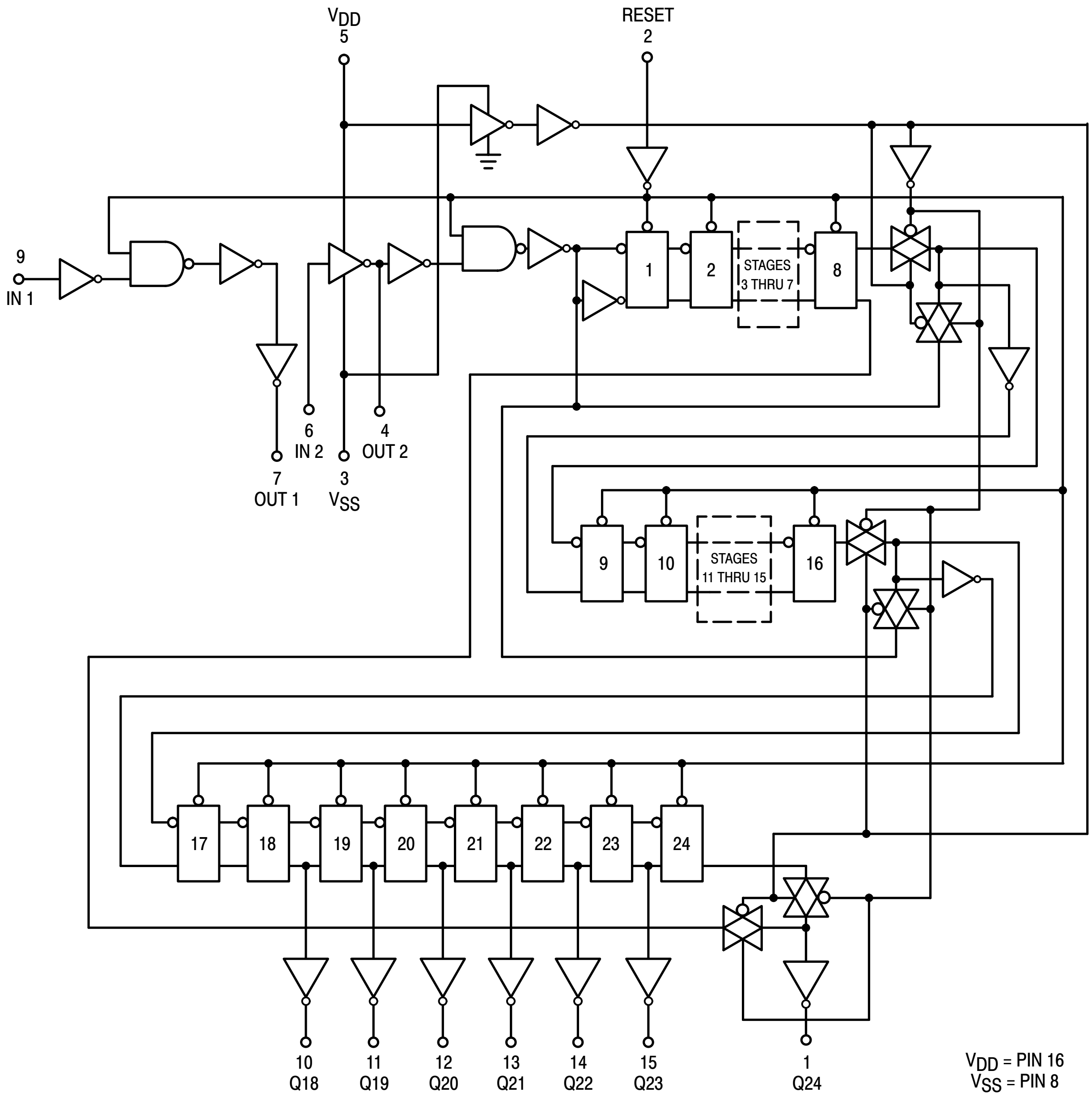
Figure 8. Functional Test Circuit

FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8−stage sections, and 255 counts are loaded in each of the 8−stage sections in parallel. All flip−flops are now at a logic “1”. The counter is now returned to the normal 24−stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all “1” state to an all “0” state.

Inputs		Outputs				Comments
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	Counter is in three 8−stage sections in parallel mode
1	0	0	V_{DD}	Gnd	0	Counter is reset. In 2 and Out 2 are connected together
0	1	1	↓	↓		First “0” to “1” transition on In 2, Out 2 node.
	0 1 — — —	0 1 — — —				255 “0” to “1” transitions are clocked into this In 2, Out 2 node.
	1	1			1	The 255th “0” to “1” transition.
	0 0	0 0	Gnd		1 1	
	1	0		V_{DD}	1	Counter converted back to 24−stages in series mode.
	1	0			1	Out 2 converts back to an output.
↓	0	1	↓	↓	0	Counter ripples from an all “1” state to an all “0” stage.

LOGIC DIAGRAM



MC14526B

Presettable 4-Bit Down Counters

The MC14526B binary counter is constructed with MOS P−channel and N−channel enhancement mode devices in a monolithic structure.

This device is presettable, cascadable, synchronous down counter with a decoded “0” state output for divide−by−N applications. In single stage applications the “0” output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide−by−N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

This complementary MOS counter can be used in frequency synthesizers, phase−locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge−Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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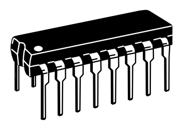
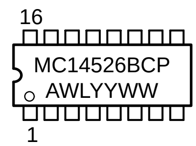
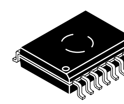
MARKING DIAGRAMS

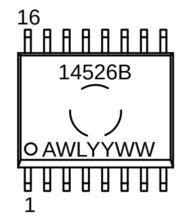


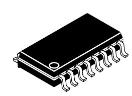
PDIP−16
P SUFFIX
CASE 648



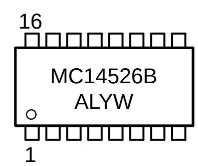


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



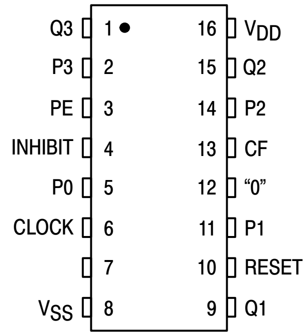
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14526BCP	PDIP−16	2000/Box
MC14526BDW	SOIC−16	47/Rail
MC14526BDWR2	SOIC−16	1000/Tape & Reel
MC14526BF	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
_/¯	L	H	L	X	L	Decrement inhibited
L	L	¯_	L	X	L	Decrement inhibited
¯_	L	L	L	L	L	No change** (inactive edge)
H	L	_/¯	L	L	L	No change** (inactive edge)
_/¯	L	L	L	L	L	Decrement**
H	L	¯_	L	L	L	Decrement**

X = Don't Care
NOTES:
 * Output "0" is low when reset goes high only it PE and CF are low.
** Output "0" is high when reset is low, only if CF is high and count is 0000.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.7 µA/kHz) f + I_{DD} I_T = (3.4 µA/kHz) f + I_{DD} I_T = (5.1 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL} (Figures 4, 5)	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time (Inhibit Used as Negative Edge Clock) Clock or Inhibit to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns	t_{PLH}, t_{PHL} (Figures 4, 5, 6)	 5.0 10 15	 — — —	 550 225 160	 1100 450 320	ns
Clock or Inhibit to “0” t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 155 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		 5.0 10 15	 — — —	 240 130 100	 480 260 200	
Propagation Delay Time Pn to Q	t_{PLH}, t_{PHL} (Figures 4, 7)	5.0 10 15	— — —	260 120 100	520 240 200	ns
Propagation Delay Time Reset to Q	t_{PHL} (Figure 8)	5.0 10 15	— — —	250 110 80	500 220 160	ns
Propagation Delay Time Preset Enable to “0”	t_{PHL}, t_{PLH} (Figures 4, 9)	5.0 10 15	— — —	220 100 80	440 200 160	ns
Clock or Inhibit Pulse Width	t_W (Figures 5, 6)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Clock Pulse Frequency (with PE = low)	f_{max} (Figures 4, 5, 6)	5.0 10 15	— — —	2.0 5.0 6.6	1.5 3.0 4.0	MHz
Clock or Inhibit Rise and Fall Time	t_r, t_f (Figures 5, 6)	5.0 10 15	— — —	— — —	15 5 4	µs
Setup Time Pn to Preset Enable	t_{su} (Figure 10)	5.0 10 15	90 50 40	40 15 10	— — —	ns
Hold Time Preset Enable to Pn	t_h (Figure 10)	5.0 10 15	30 30 30	– 15 – 5 0	— — —	ns
Preset Enable Pulse Width	t_W (Figure 10)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Reset Pulse Width	t_W (Figure 8)	5.0 10 15	350 250 200	175 125 100	— — —	ns
Reset Removal Time	t_{rem} (Figure 8)	5.0 10 15	10 20 30	– 110 – 30 – 20	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

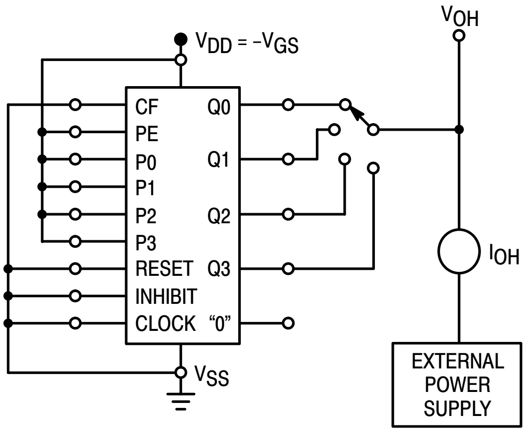


Figure 1. Typical Output Source Characteristics Test Circuit

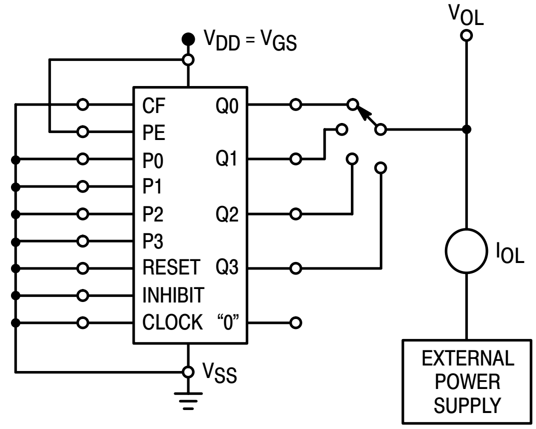


Figure 2. Typical Output Sink Characteristics Test Circuit

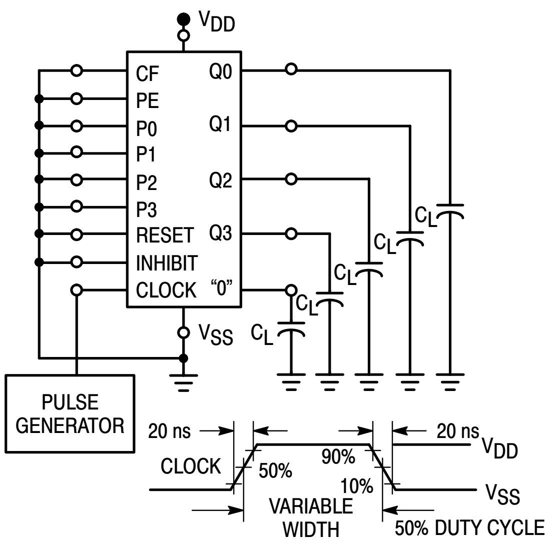
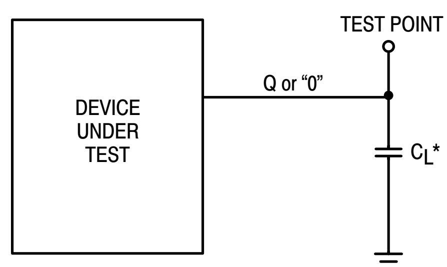


Figure 3. Power Dissipation



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

SWITCHING WAVEFORMS

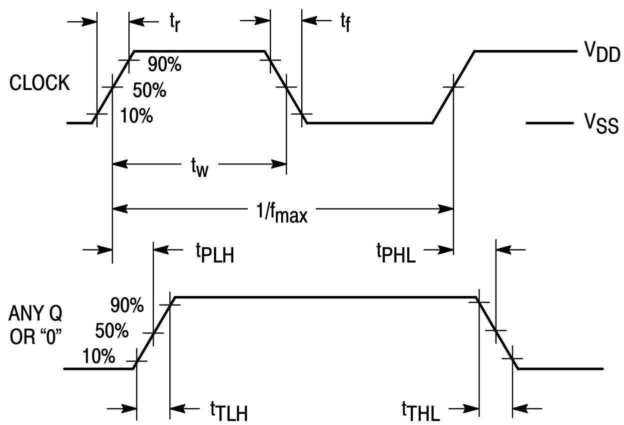


Figure 5.

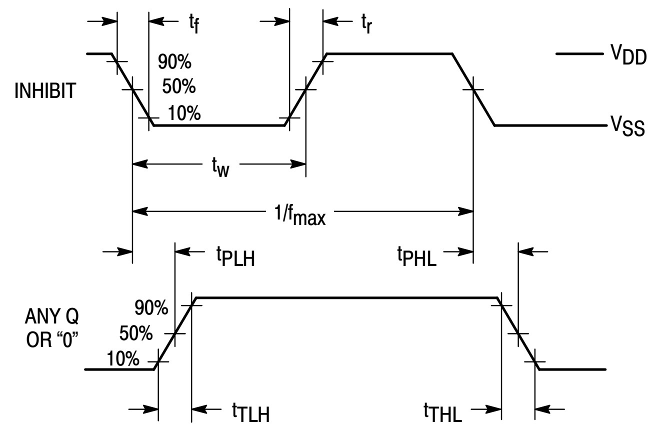


Figure 6.

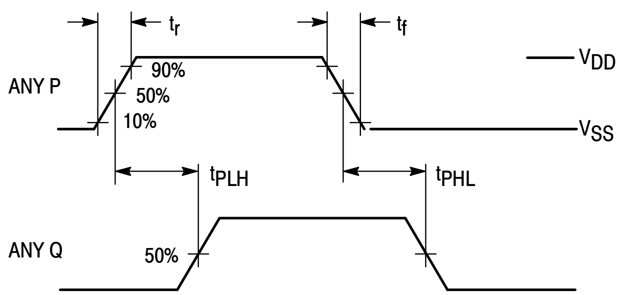


Figure 7.

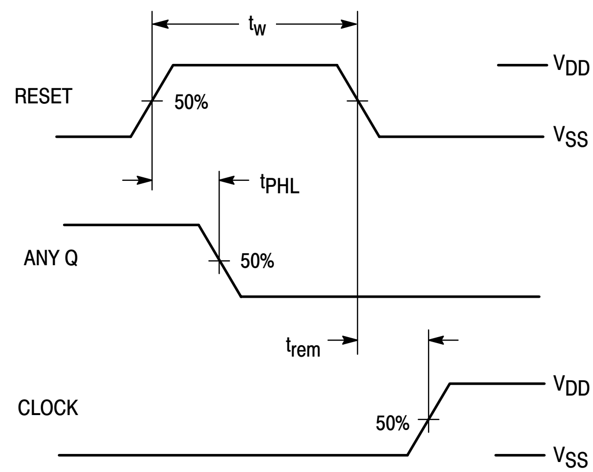


Figure 8.

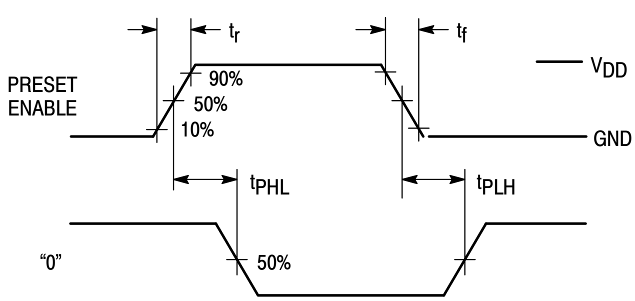


Figure 9.

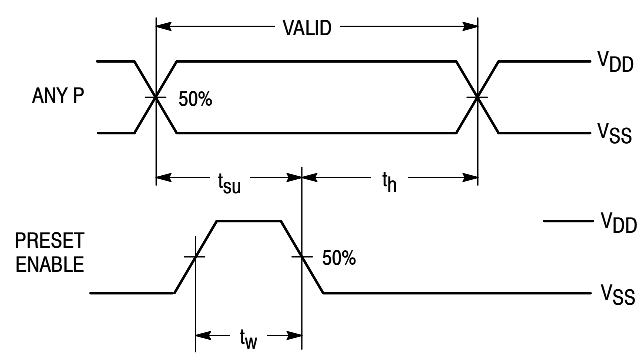


Figure 10.

PIN DESCRIPTIONS

Preset Enable (Pin 3) — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

Inhibit (Pin 4) — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the “0” output to go high.

“0” (Pin 12) — The “0” (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the counter to a value other than all zeroes, the “0” output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the “0” output when the count is all zeroes. If Cascade Feedback is low, the “0” output depends on the Preset Enable input level. See the Function Table.

P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

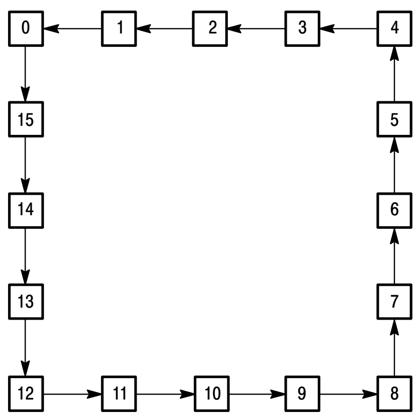
Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

V_{SS} (Pin 8) — The most negative power supply potential. This pin is usually ground.

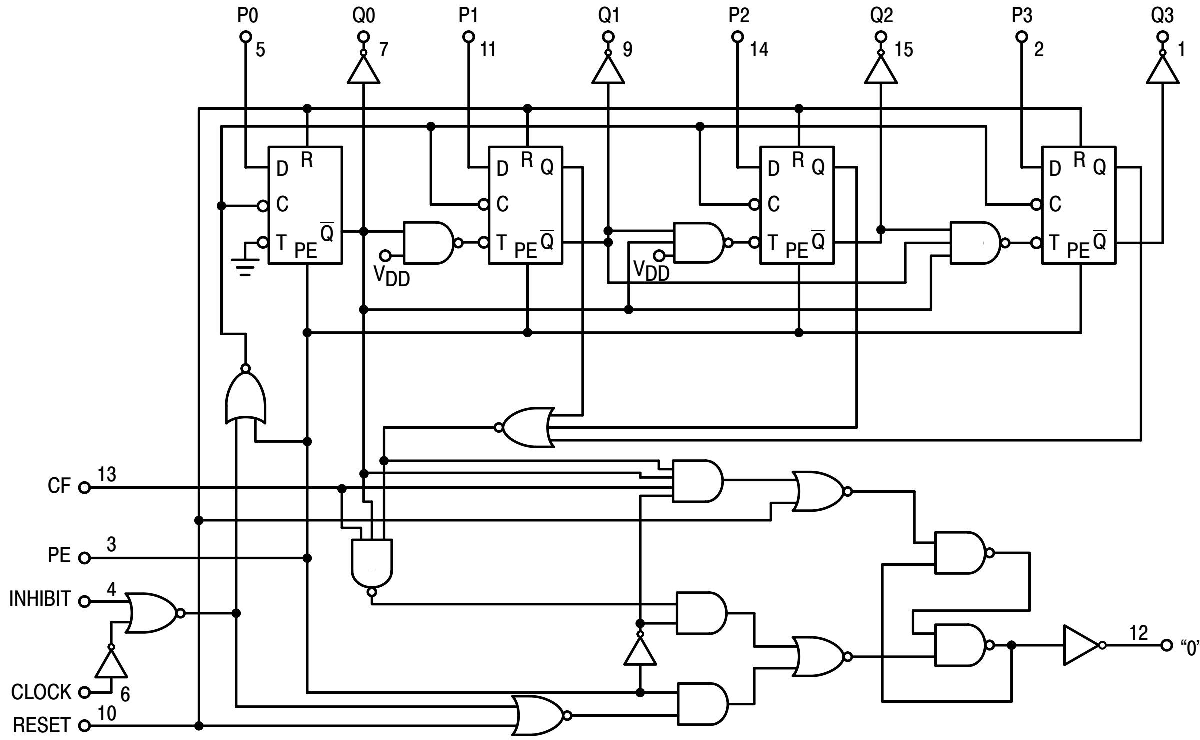
V_{DD} (Pin 16) — The most positive power supply potential. V_{DD} may range from 3 to 18 V with respect to V_{SS}.

STATE DIAGRAM

MC14526B



MC14526B LOGIC DIAGRAM (Binary Down Counter)



APPLICATIONS INFORMATION

Divide−By−N, Single Stage

Figure 11 shows a single stage divide−by−N application. To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presettable Divide−By−N

Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non−zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one (i.e. N = 1).

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.

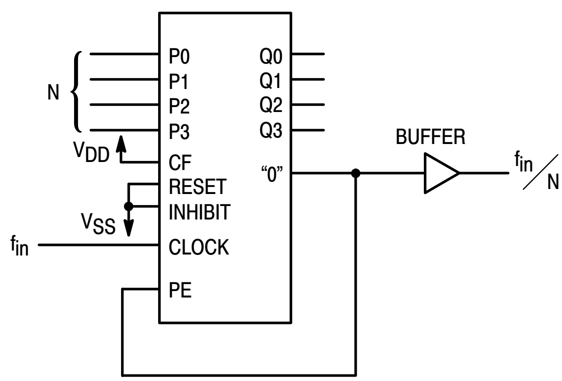


Figure 11. ÷ N Counter

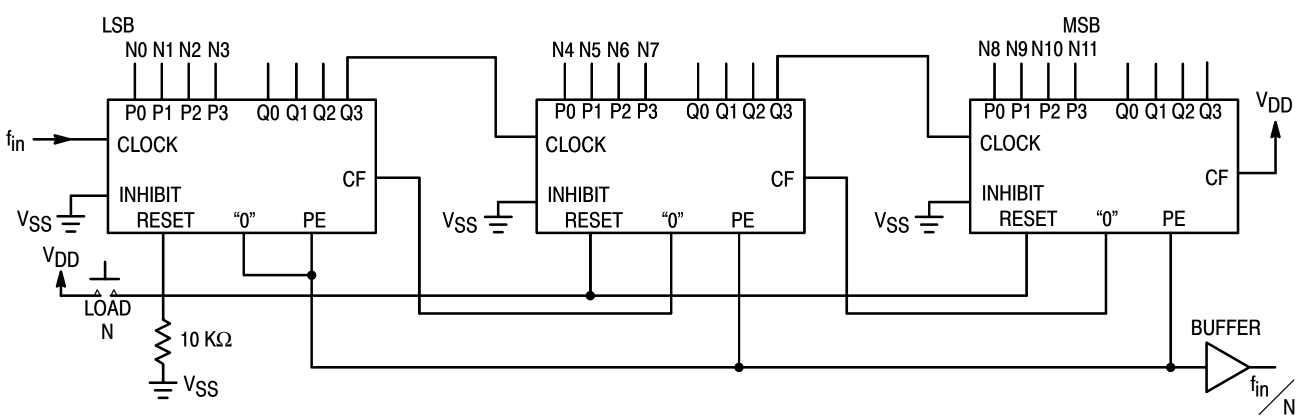


Figure 12. 3 Stages Cascaded

MC14528B

Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- This part should only be used in new designs where the pulse width is < 10 μs.
  Note: For designs requiring a pulse width > 10 μs, please see the MC14538, which is pin−for−pin compatible.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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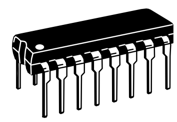
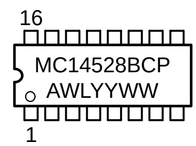
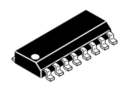
MARKING DIAGRAMS

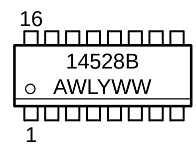


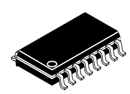
PDIP−16
P SUFFIX
CASE 648



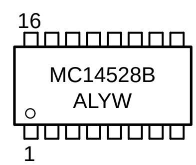


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



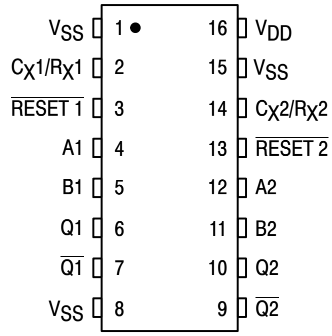
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

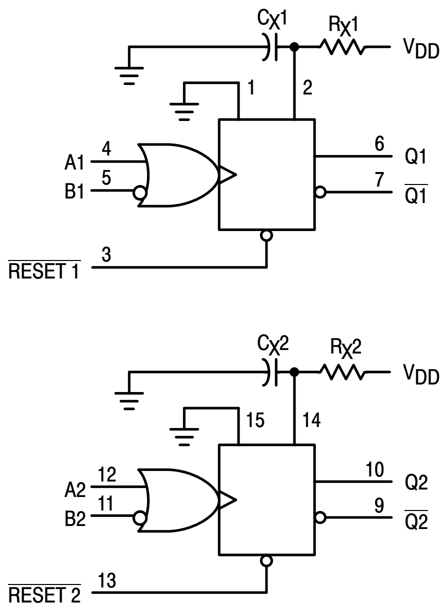
Device	Package	Shipping
MC14528BCP	PDIP−16	2000/Box
MC14528BD	SOIC−16	48/Rail
MC14528BDR2	SOIC−16	2500/Tape & Reel
MC14528BF	SOEIAJ−16	See Note 1.
MC14528BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

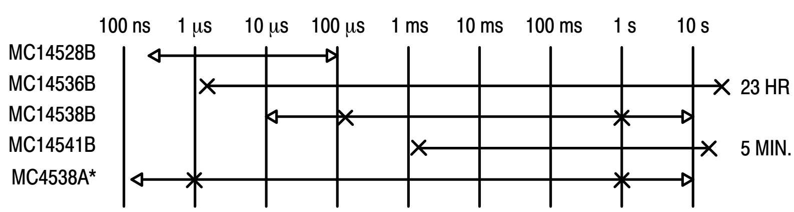


BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 1, PIN 8, PIN 15
R_X AND C_X ARE EXTERNAL COMPONENTS

ONE−SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2−6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ◁——▷
RECOMMENDED PULSE WIDTH RANGE ×——×

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.64 – 1.6 – 4.2	— — — —	– 1.0 – 0.51 – 1.3 – 3.4	– 1.7 – 0.88 – 2.25 – 8.8	— — — —	– 0.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula — (5.)	I_T	—	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2x10^{-8}$ $R_X C_X (V_{DD}{}^{-2})^2 f] \times 10^{-3}$ where: I_T in µA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (8.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ (9.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}	—	—					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	—	40	80	
Turn−Off, Turn−On Delay Time — A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns				5.0	—	325	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	—	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	—	90	180	
Turn−Off, Turn−On Delay Time — A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	—	705	—	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns				10	—	290	—	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	—	210	—	
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0	150	70	—	ns
				10	75	30	—	
				15	55	30	—	
	t_{WL}	1000	10	5.0	—	70	—	ns
				10	—	30	—	
				15	—	30	—	
Output Pulse Width — Q or $\overline{Q}$ (For C_X < 0.01 µF use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0	—	550	—	ns
				10	—	350	—	
				15	—	300	—	
Output Pulse Width — Q or $\overline{Q}$ (For C_X > 0.01 µF use formula: $t_W = 0.2\ R_X\ C_X\ Ln\ [V_{DD} - V_{SS}]$) (6.)	t_W	10,000	10	5.0	15	30	45	µs
				10	10	50	90	
				15	15	55	95	
Pulse Width Match between Circuits in the same package	t1 – t2	10,000	10	5.0	—	6.0	25	%
				10	—	8.0	35	
				15	—	8.0	35	
Reset Propagation Delay — $\overline{\text{Reset}}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	—	325	600	ns
				10	—	90	225	
				15	—	60	170	
		1000	10	5.0	—	1000	—	ns
				10	—	300	—	
				15	—	250	—	
Retrigger Time	t_{rr}	15	5.0	5.0	0	—	—	ns
				10	0	—	—	
				15	0	—	—	
		1000	10	5.0	0	—	—	ns
				10	0	—	—	
				15	0	—	—	
External Timing Resistance	R_X	—	—	—	5.0	—	1000	kΩ
External Timing Capacitance	C_X	—	—	—	No Limits (7.)			µF

6. R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.
7. If C_X > 15 µF, Use Discharge Protection Diode D_X, per Fig. 9.
8. The formulas given are for the typical characteristics only at 25°C.
9. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{\text{Q}}$
H	↑	H	⊓	⊔
H	L	↓	⊓	⊔
H	↑ ↓	L	Not Triggered	
H	H	↑ ↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓ ↑	X	X	Not Triggered	

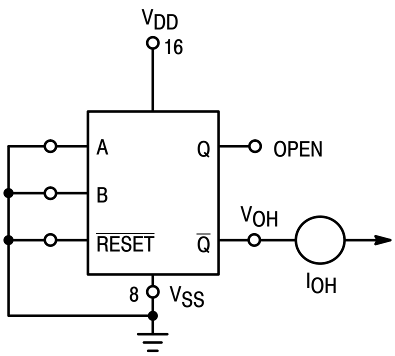


Figure 1. Output Source Current Test Circuit

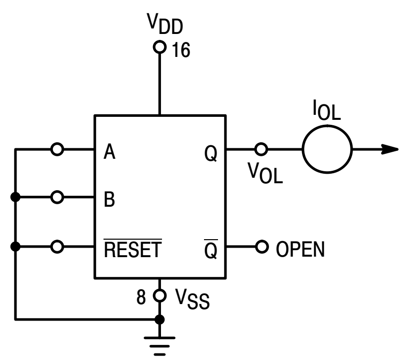


Figure 2. Output Sink Current Test Circuit

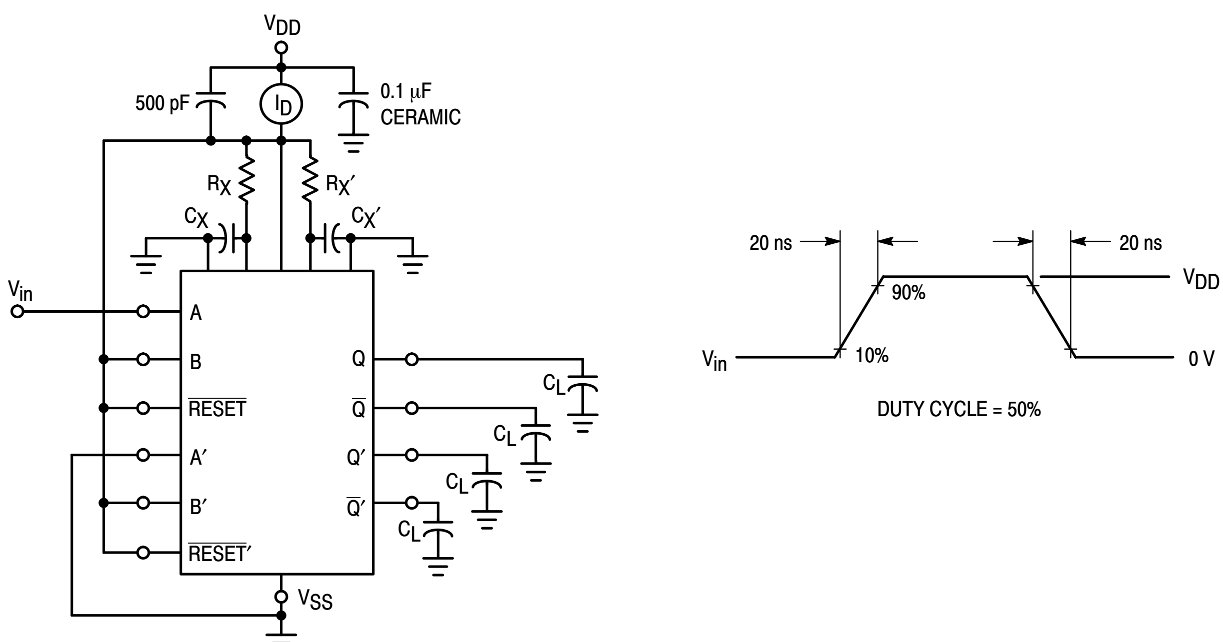
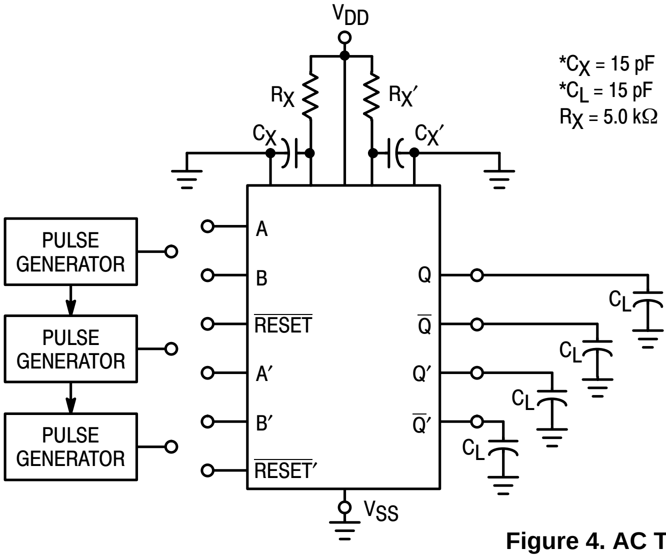


Figure 3. Power Dissipation Test Circuit and Waveforms



INPUT CONNECTIONS

Characteristics	$\overline{\text{Reset}}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

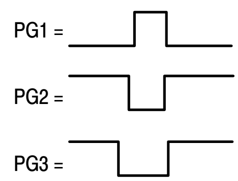


Figure 4. AC Test Circuit

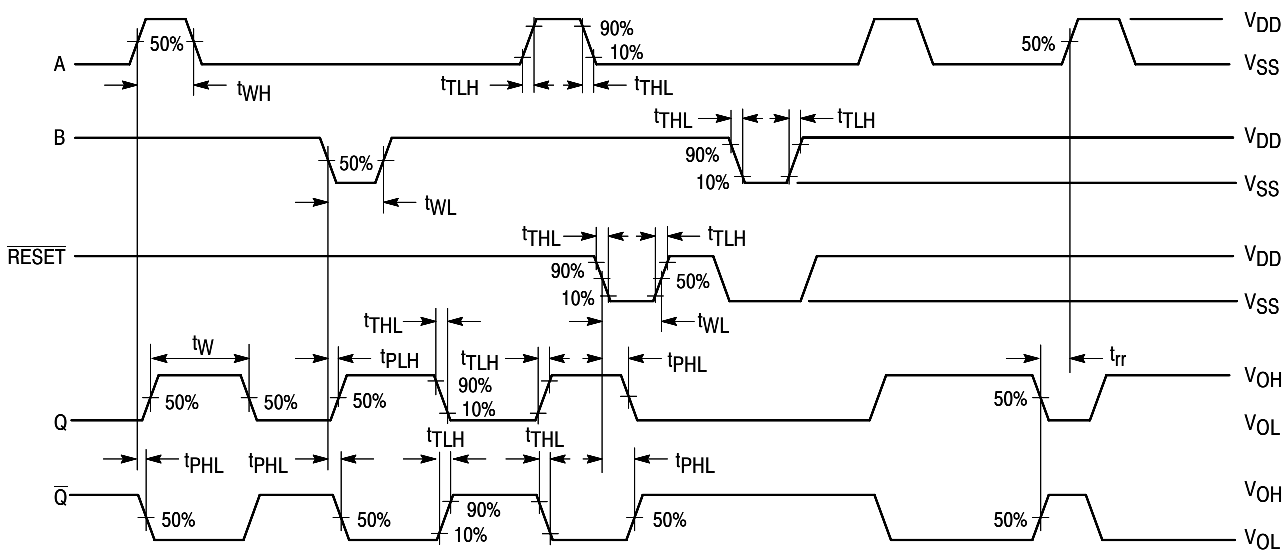


Figure 5. AC Test Waveforms

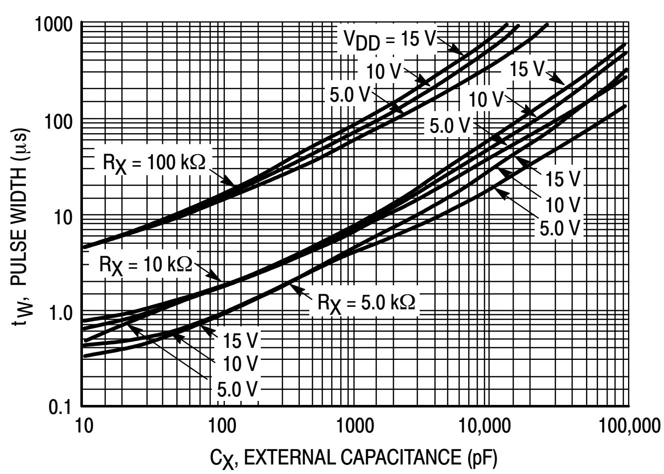


Figure 6. Pulse Width versus C_X

TYPICAL APPLICATIONS

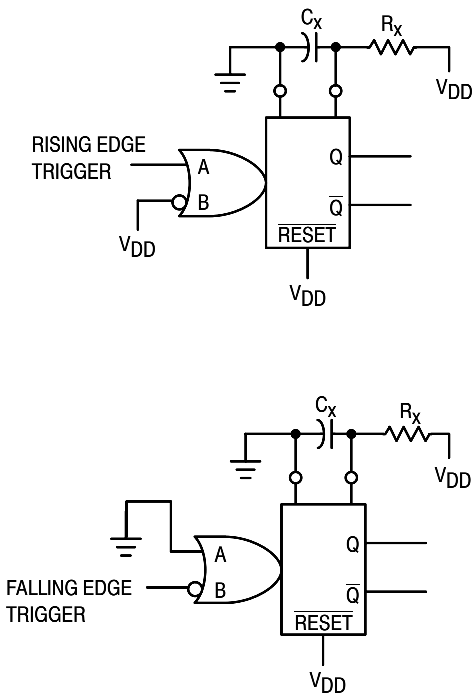


Figure 7. Retriggerable Monostables Circuitry

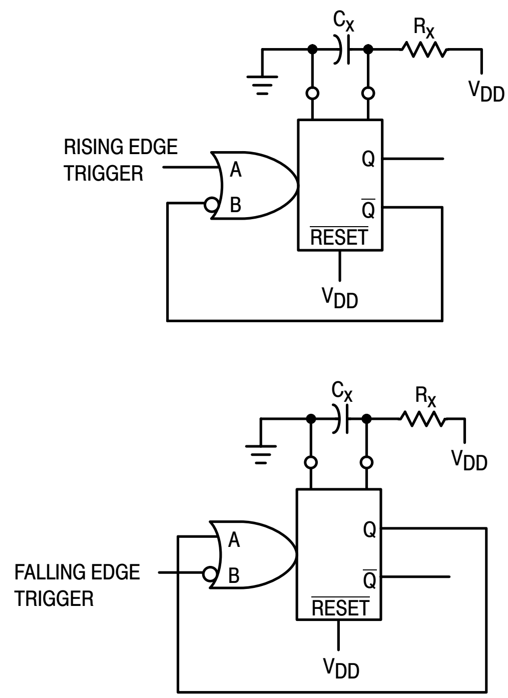


Figure 8. Non−Retriggerable Monostables Circuitry

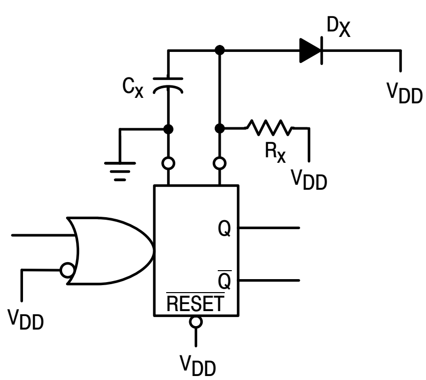


Figure 9. Use of a Diode to Limit Power Down Current Surge

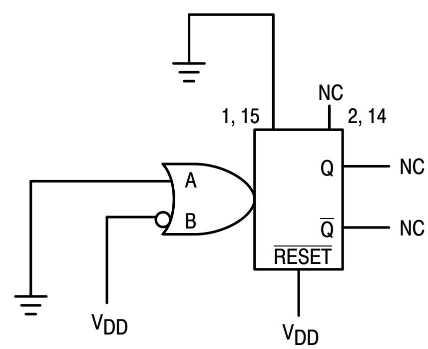


Figure 10. Connection of Unused Sections

MC14532B

8-Bit Priority Encoder

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range

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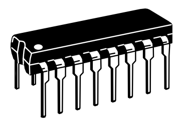
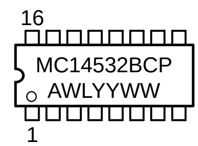
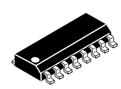
MARKING DIAGRAMS

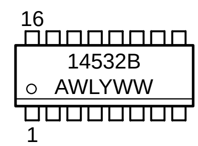


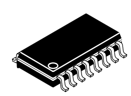
PDIP−16
P SUFFIX
CASE 648



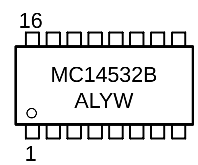


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

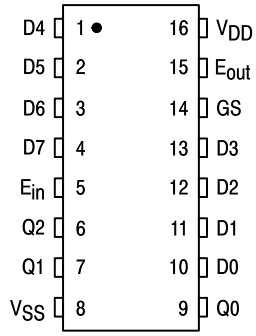
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

Device	Package	Shipping
MC14532BCP	PDIP−16	2000/Box
MC14532BD	SOIC−16	48/Rail
MC14532BDR2	SOIC−16	2500/Tape & Reel
MC14532BF	SOEIAJ−16	See Note 1.
MC14532BFEL	SOEIAJ−16	See Note 1.
MC14532BFR1	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



TRUTH TABLE

Input									Output				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don’t Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.74 µA/kHz) f + I_{DD} I_T = (3.65 µA/kHz) f + I_{DD} I_T = (5.73 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

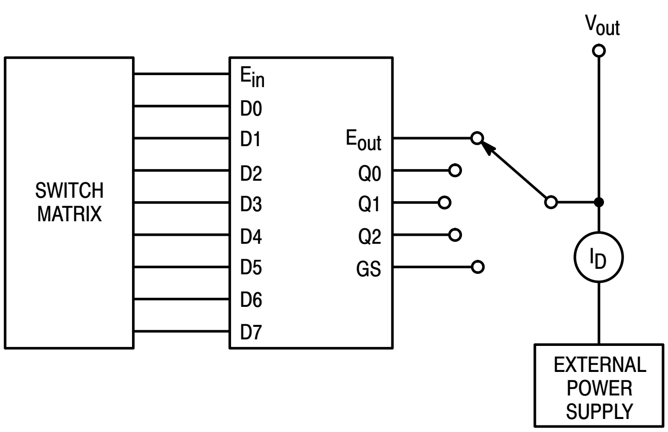
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time — E_{in} to E_{out} t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 120 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 205 110 80	 410 220 160	ns
Propagation Delay Time — E_{in} to GS t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L 57 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 175 90 65	 350 180 130	ns
Propagation Delay Time — E_{in} to Q_n t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PHL}, t_{PLH}	 5.0 10 15	 — — —	 280 140 100	 560 280 200	ns
Propagation Delay Time — D_n to Q_n t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 137 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 300 170 110	 600 340 220	ns
Propagation Delay Time — D_n to GS t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 280 140 100	 560 280 200	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



Output Under Test	$V_{GS} = V_{DD}$, $V_{DS} = V_{out}$ Sink Current		$V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$ Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

Figure 1. Typical Sink and Source Current Characteristics

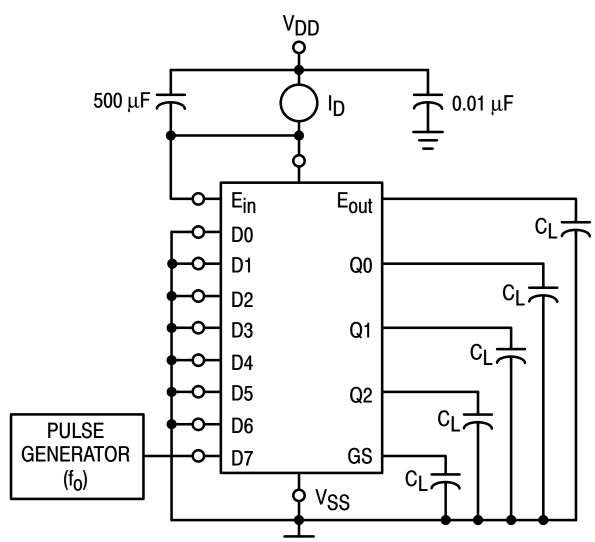


Figure 2. Typical Power Dissipation Test Circuit

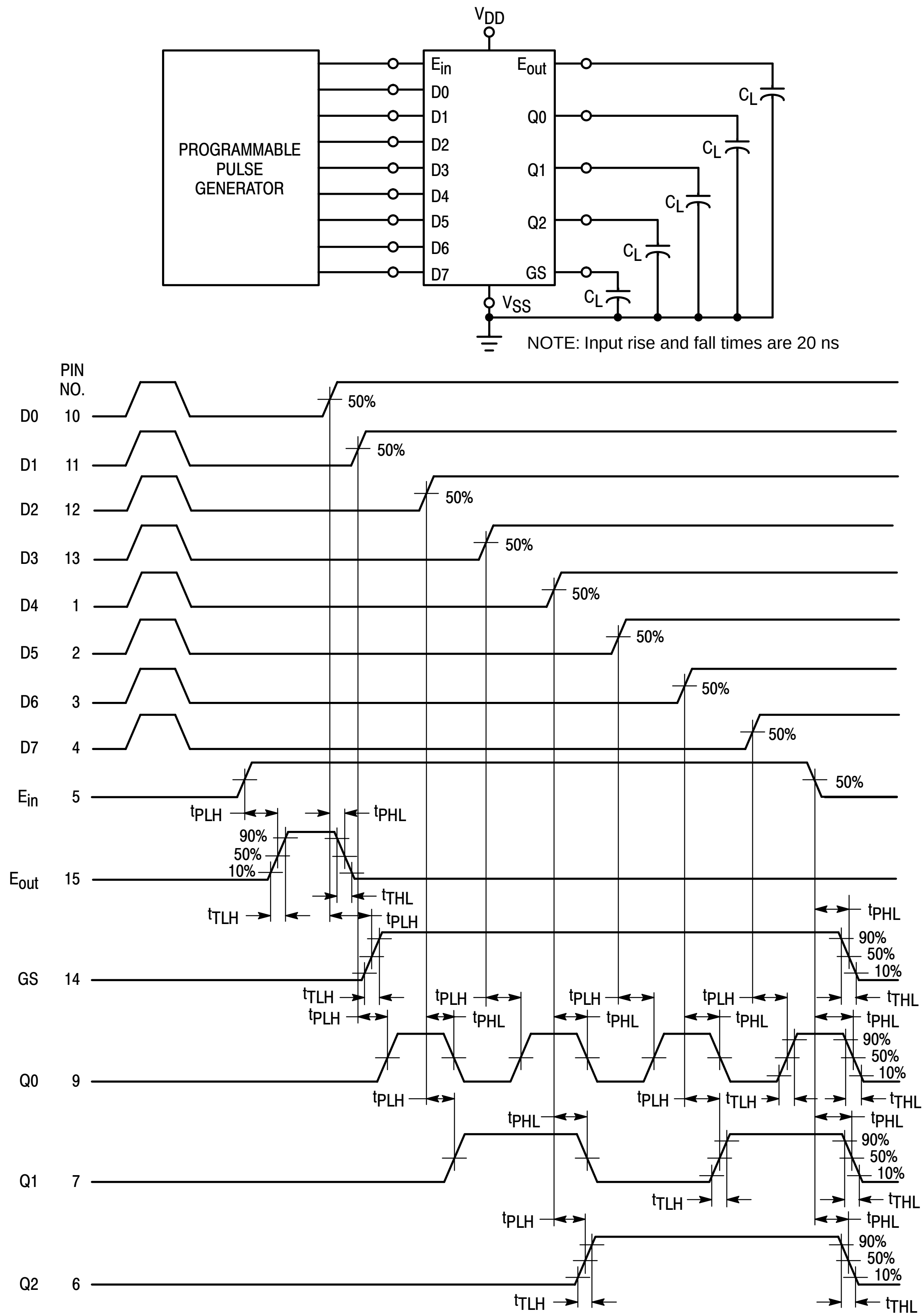


Figure 3. AC Test Circuit and Waveforms

LOGIC DIAGRAM
(Positive Logic)

LOGIC EQUATIONS

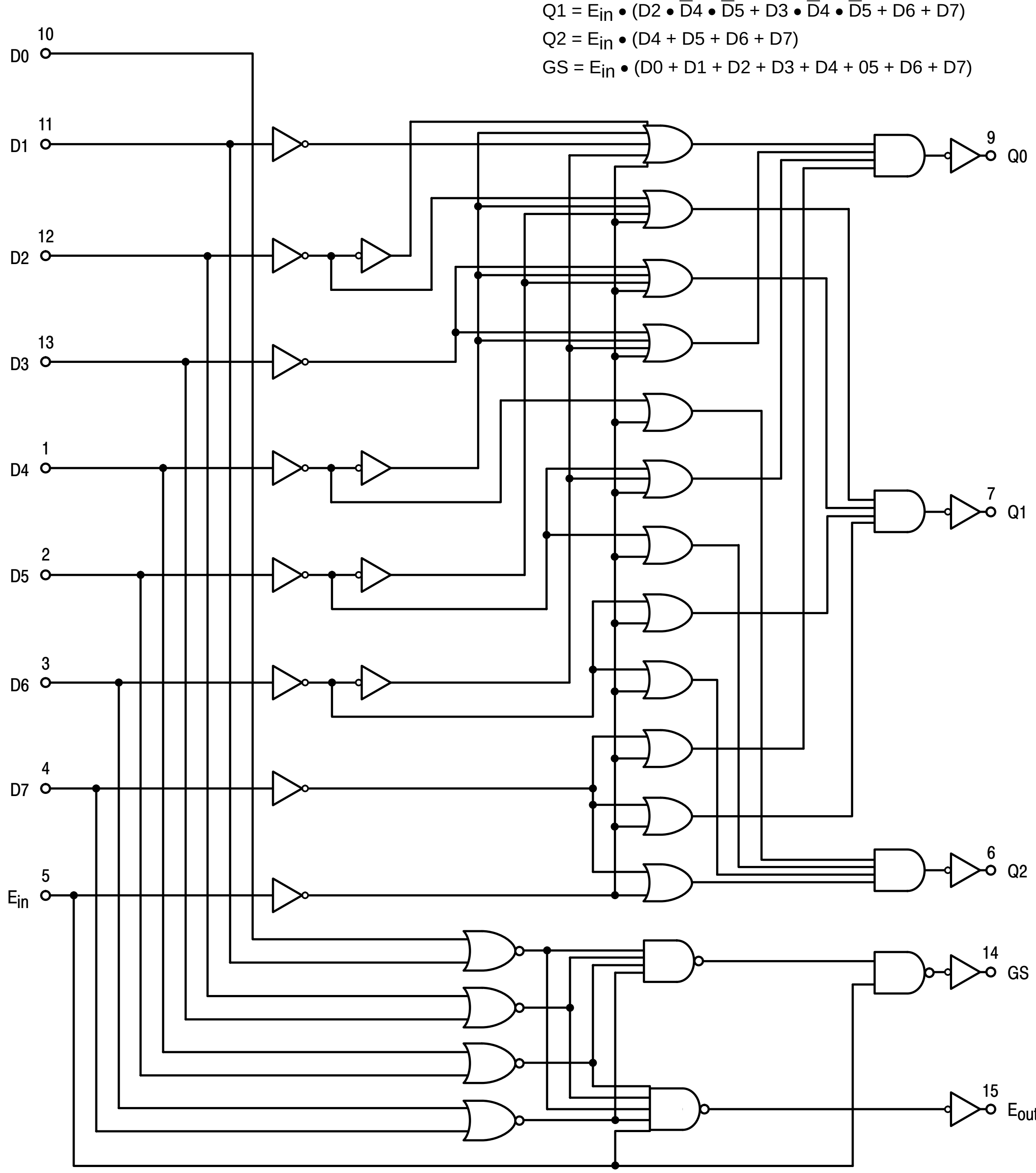
$E_{out} = E_{in} \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet \overline{D6} \bullet \overline{D7}$

$Q0 = E_{in} \bullet (D1 \bullet \overline{D2} \bullet \overline{D4} \bullet \overline{D6} + D3 \bullet \overline{D4} \bullet \overline{D6} + D5 \bullet \overline{D6} + D7)$

$Q1 = E_{in} \bullet (D2 \bullet \overline{D4} \bullet \overline{D5} + D3 \bullet \overline{D4} \bullet \overline{D5} + D6 + D7)$

$Q2 = E_{in} \bullet (D4 + D5 + D6 + D7)$

$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + 05 + D6 + D7)$



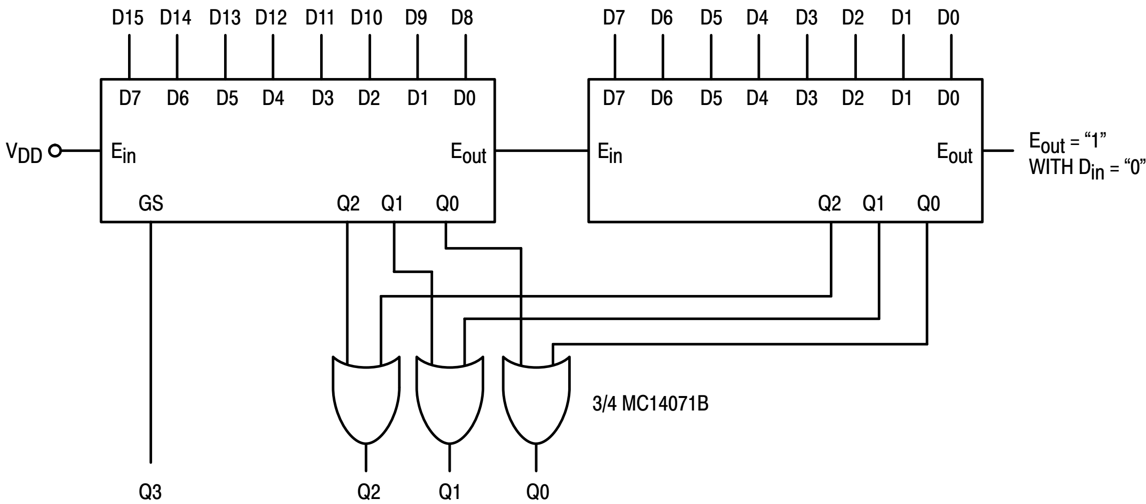


Figure 4. Two MC14532B's Cascaded for 4−Bit Output

DIGITAL TO ANALOG CONVERSION

The digital eight−bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520B. A compromise between I_{bias} for the MC1710 and ΔR between N and P−channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C $\approx$ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight−bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

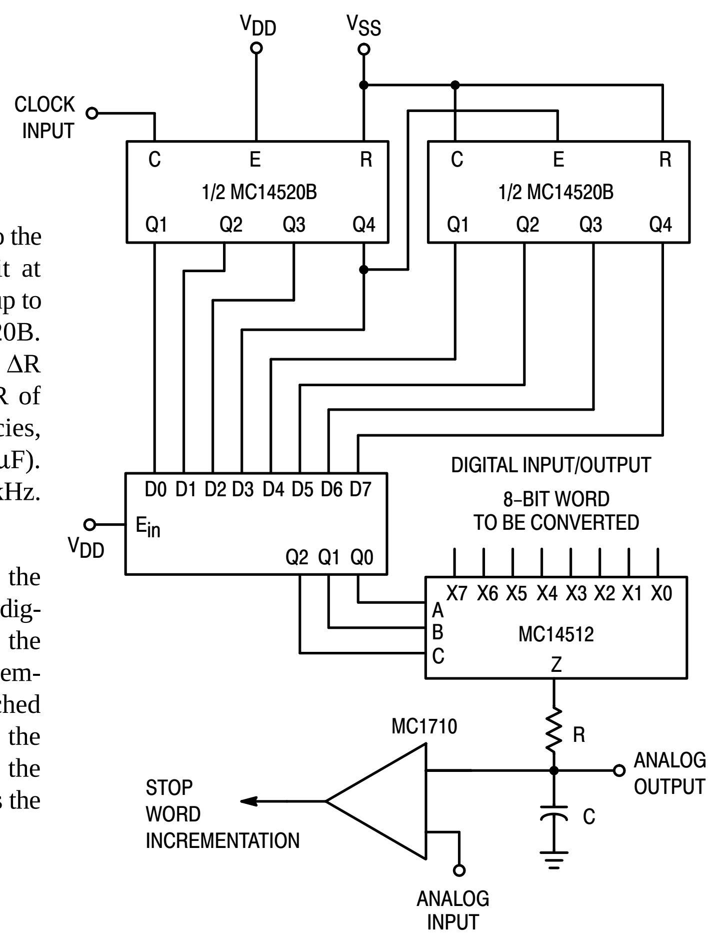


Figure 5. Digital to Analog and Analog to Digital Converter

MC14536B

Programmable Timer

The MC14536B programmable timer is a 24−stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on−chip RC oscillator or an external clock are provided. An on−chip monostable circuit incorporating a pulse−type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

- 24 Flip−Flop Stages − Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four−Bit Select Code
- 8−Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On−Chip RC Oscillator Provisions
- On−Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C from 65°C to 125°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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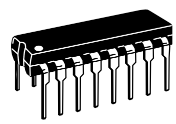
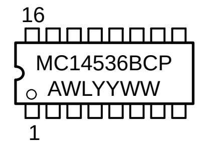
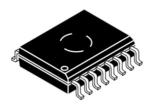
MARKING DIAGRAMS

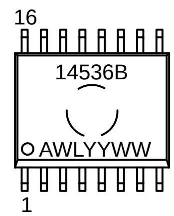


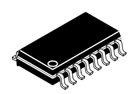
PDIP−16
P SUFFIX
CASE 648



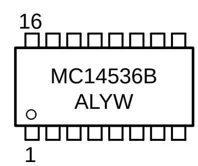


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MC14536BCP	PDIP−16	2000/Box
MC14536BDW	SOIC−16	47 Units/Rail
MC14536BDWR2	SOIC−16	1000 Tape & Reel
MC14536BF	SOEIAJ−16	See below*

*For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

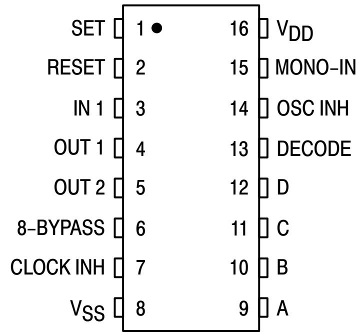


Figure 1. Pin Assignment

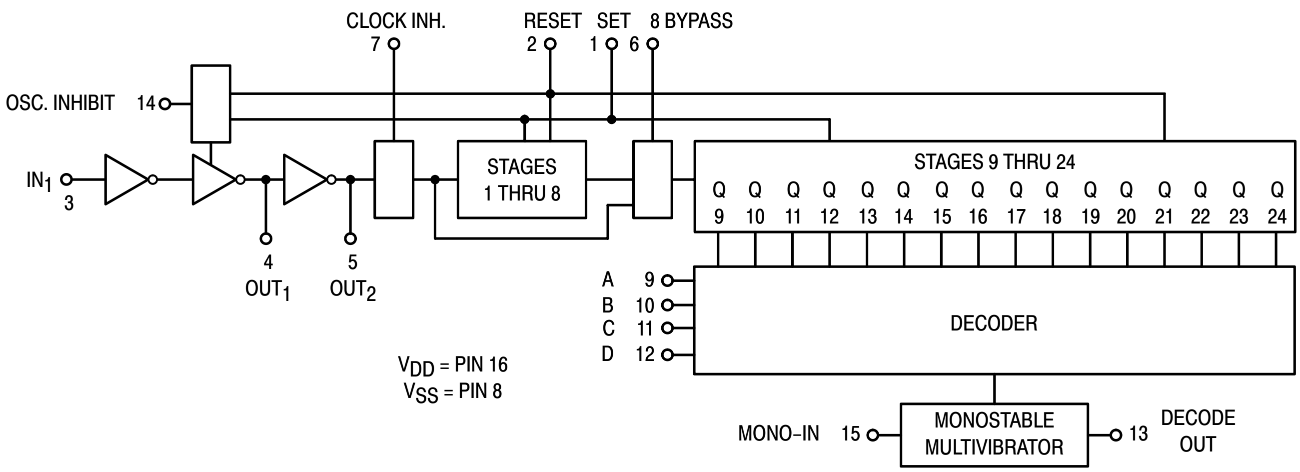


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 3)	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	−	4.95	5.0	−	4.95	−	Vdc
		10	9.95	−	9.95	10	−	9.95	−	
		15	14.95	−	14.95	15	−	14.95	−	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	−	1.5	−	2.25	1.5	−	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	−	3.0	−	4.50	3.0	−	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	−	4.0	−	6.75	4.0	−	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	−	3.5	2.75	−	3.5	−	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	−	7.0	5.50	−	7.0	−	
(V_O = 1.5 or 13.5 Vdc)		15	11	−	11	8.25	−	11	−	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.2	−	– 1.0	– 1.7	−	– 0.7	−	
(V_{OH} = 4.6 Vdc) Pins 4 & 5		5.0	– 0.25	−	– 0.25	– 0.36	−	– 0.14	−	
(V_{OH} = 9.5 Vdc)		10	– 0.62	−	– 0.5	– 0.9	−	– 0.35	−	
(V_{OH} = 13.5 Vdc)		15	– 1.8	−	– 1.5	– 3.5	−	– 1.1	−	
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	−	– 2.4	– 4.2	−	– 1.7	−	mAdc
(V_{OH} = 4.6 Vdc) Pin 13		5.0	– 0.64	−	– 0.51	– 0.88	−	– 0.36	−	
(V_{OH} = 9.5 Vdc)		10	– 1.6	−	– 1.3	– 2.25	−	– 0.9	−	
(V_{OH} = 13.5 Vdc)		15	– 4.2	−	– 3.4	– 8.8	−	– 2.4	−	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	−	0.51	0.88	−	0.36	−	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	−	1.3	2.25	−	0.9	−	
(V_{OL} = 1.5 Vdc)		15	4.2	−	3.4	8.8	−	2.4	−	
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0	−	5.0	−	0.010	5.0	−	150	µAdc
		10	−	10	−	0.020	10	−	300	
		15	−	20	−	0.030	20	−	600	
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.50 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.30 µA/kHz) f + I_{DD}							
		15	I_T = (3.55 µA/kHz) f + I_{DD}							

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L – 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 7)	Max	Unit
Output Rise and Fall Time (Pin 13)	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1, 8−Bypass (Pin 6) High						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	–	1800	3600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	–	650	1300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	1000	
Clock to Q1, 8−Bypass (Pin 6) Low	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns		5.0	–	3.8	7.6	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	–	1.1	2.3	
Clock to Q16	t_{PLH}, t_{PHL}					μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns		5.0	–	7.0	14	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	–	3.0	6.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	–	2.2	4.5	
Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	–	1500	3000	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	–	600	1200	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	900	
Clock Pulse Width	t_{WH}	5.0 10 15	600 200 170	300 100 85	– – –	ns
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0 10 15	– – –	1.2 3.0 5.0	0.4 1.5 2.0	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	No Limit			–
Reset Pulse Width	t_{WH}	5.0 10 15	1000 400 300	500 200 150	– – –	ns

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

PIN DESCRIPTIONS

INPUTS

SET (Pin 1) − A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip−flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on IN_1 causes Decode Out to go low. The counter's flip−flop stages begin counting on the second negative clock transition of IN_1. When Set is high, the on−chip RC oscillator is disabled. This allows for very low−power standby operation.

RESET (Pin 2) − A high on Reset asynchronously forces Decode Out to a low level; all 24 flip−flop stages are also reset to a low level. Like the Set input, Reset disables the on−chip RC oscillator for standby operation.

IN_1 (Pin 3) − The device's internal counters advance on the negative−going edge of this input. IN_1 may be used as an external clock input or used in conjunction with OUT_1 and OUT_2 to form an RC oscillator. When an external clock is used, both OUT_1 and OUT_2 may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

8−BYPASS (Pin 6) − A high on this input causes the first 8 flip−flop stages to be bypassed. This device essentially becomes a 16−stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

CLOCK INHIBIT (Pin 7) − A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator start−up time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at IN_1.

OSC INHIBIT (Pin 14) − A high level on this pin stops the RC oscillator which allows for very low−power standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

MONO−IN (Pin 15) − Used as the timing pin for the on−chip monostable multivibrator. If the Mono−In input is connected to V_{SS}, the monostable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono−In and V_{DD}. This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to V_{SS}, the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 kΩ to 100 kΩ and the capacitor value should be limited to a maximum of 1000 pf. (See figures 5, 6, 7, and 12).

A, B, C, D (Pins 9, 10, 11, 12) − These inputs select the flip−flop stage to be connected to Decode Out. (See the truth tables.)

OUTPUTS

OUT_1, OUT_2 (Pin 4, 5) − Outputs used in conjunction with IN_1 to form an RC oscillator. These outputs are buffered and may be used for 2^0 frequency division of an external clock.

DECODE OUT (Pin 13) − Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

TEST MODE

The test mode configuration divides the 24 flip−flop stages into three 8−stage sections to facilitate a fast test sequence. The test mode is enabled when 8−Bypass, Set and Reset are at a high level. (See Figure 10.)

TRUTH TABLES

Input					Stage Selected for Decode Out
8−Bypass	D	C	B	A	
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
0	1	1	0	0	21
0	1	1	0	1	22
0	1	1	1	0	23
0	1	1	1	1	24

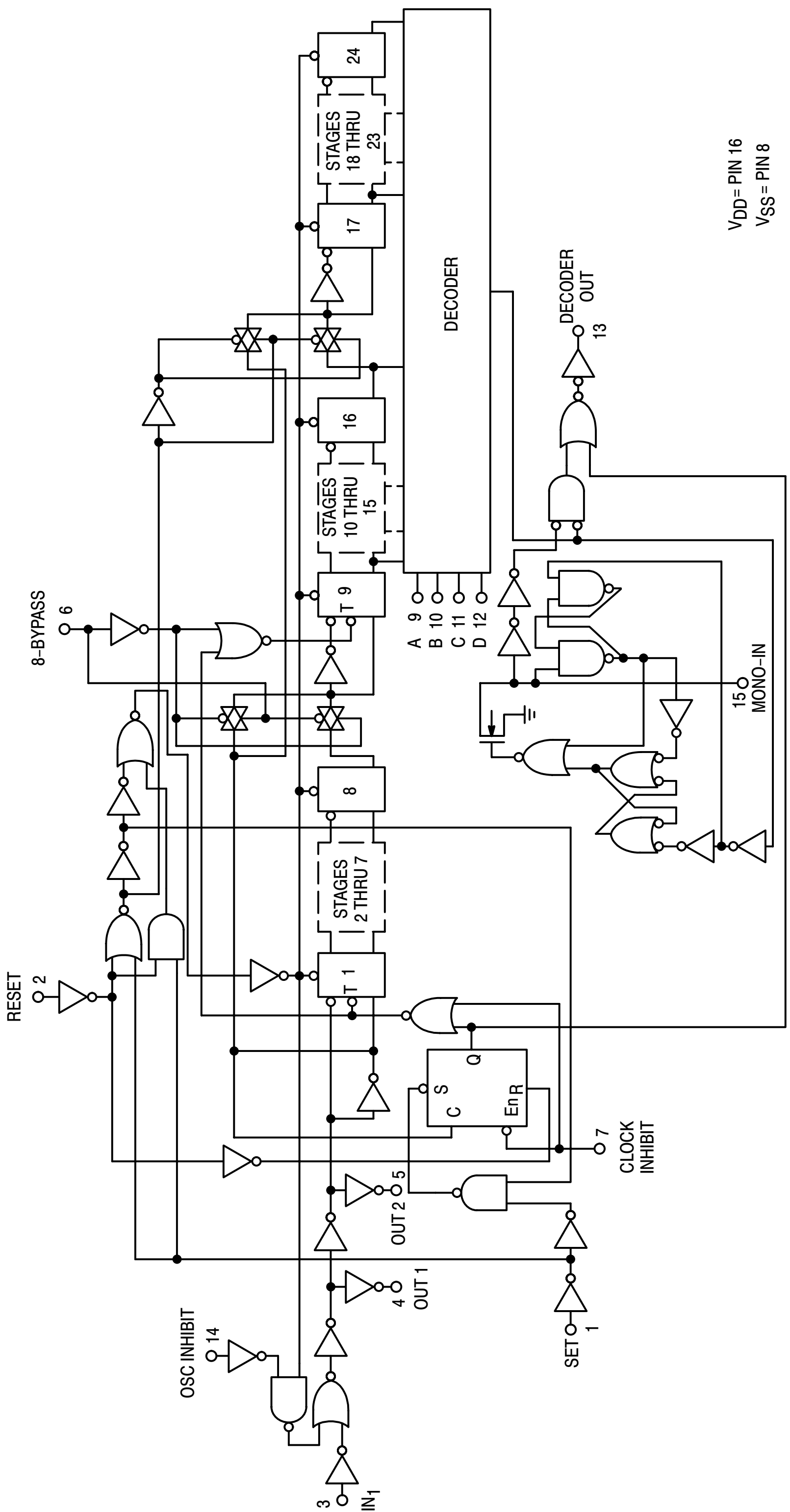
Input					Stage Selected for Decode Out
8−Bypass	D	C	B	A	
1	0	0	0	0	1
1	0	0	0	1	2
1	0	0	1	0	3
1	0	0	1	1	4
1	0	1	0	0	5
1	0	1	0	1	6
1	0	1	1	0	7
1	0	1	1	1	8
1	1	0	0	0	9
1	1	0	0	1	10
1	1	0	1	0	11
1	1	0	1	1	12
1	1	1	0	0	13
1	1	1	0	1	14
1	1	1	1	0	15
1	1	1	1	1	16

FUNCTION TABLE

In_1	Set	Reset	Clock Inh	OSC Inh	Out 1	Out 2	Decode Out
_/‾	0	0	0	0	_/‾	‾_	No Change
‾_	0	0	0	0	‾_	_/‾	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0	−	−	No Change
X	0	0	0	1	0	1	No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	_/‾	‾_	_/‾	Advance to next state

X = Don’t Care

LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 13 In Application)

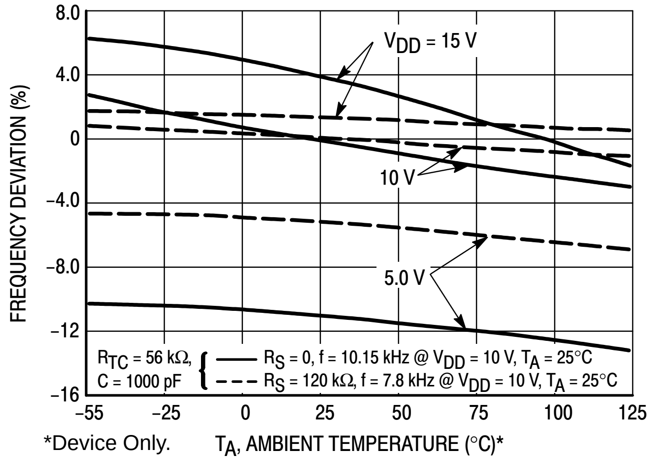


Figure 3. RC Oscillator Stability

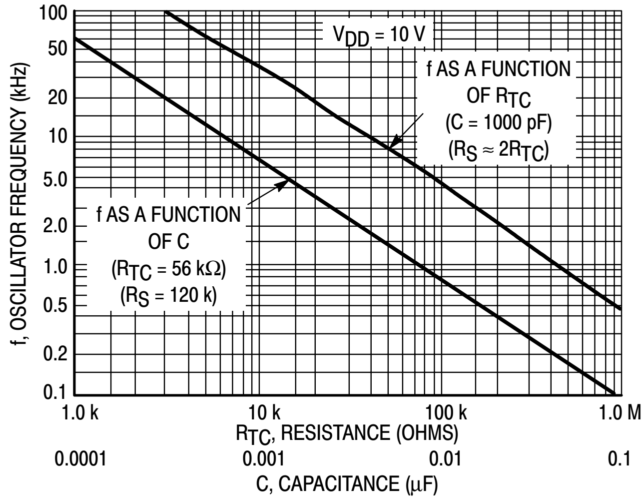


Figure 4. RC Oscillator Frequency as a Function of R_{TC} and C

MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 12 In Application)

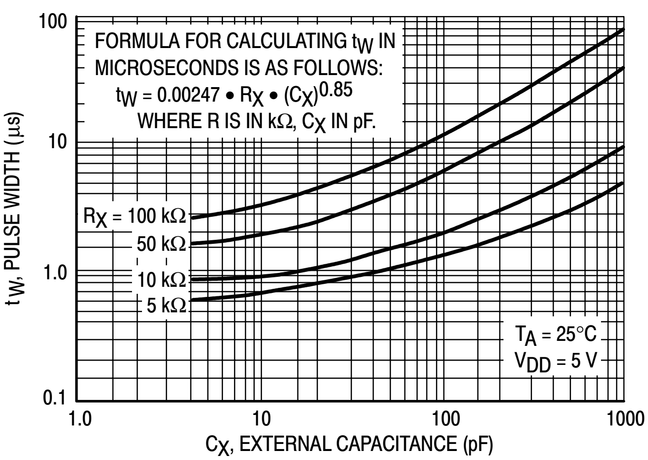


Figure 5. Typical C_X versus Pulse Width @ V_{DD} = 5.0 V

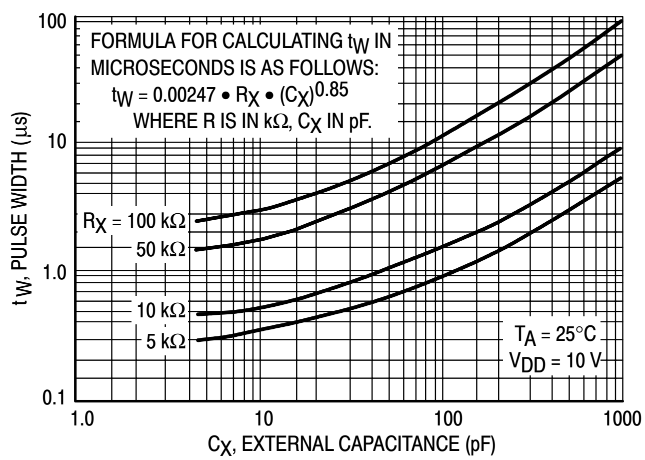


Figure 6. Typical C_X versus Pulse Width @ V_{DD} = 10 V

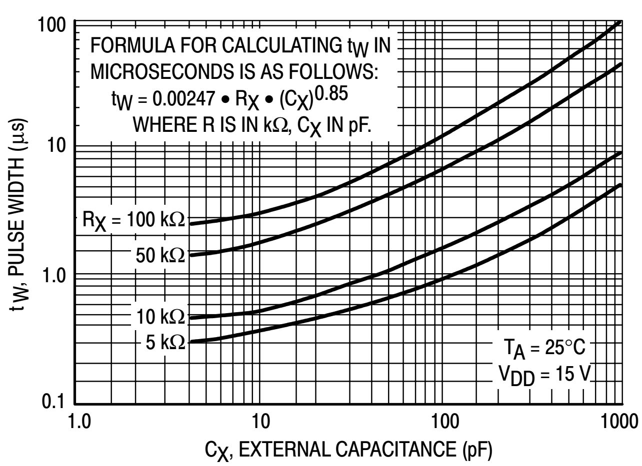


Figure 7. Typical C_X versus Pulse Width @ V_{DD} = 15 V

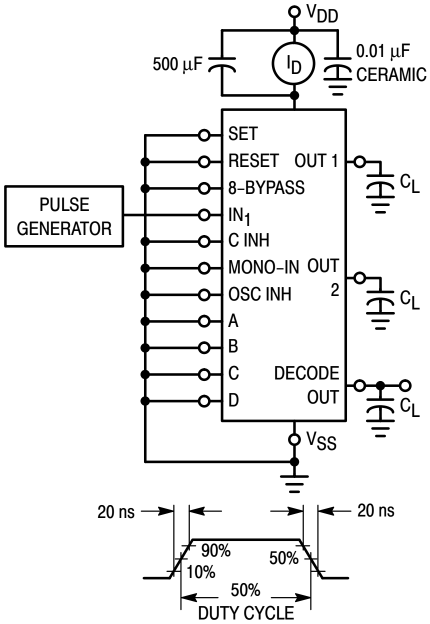


Figure 8. Power Dissipation Test Circuit and Waveform

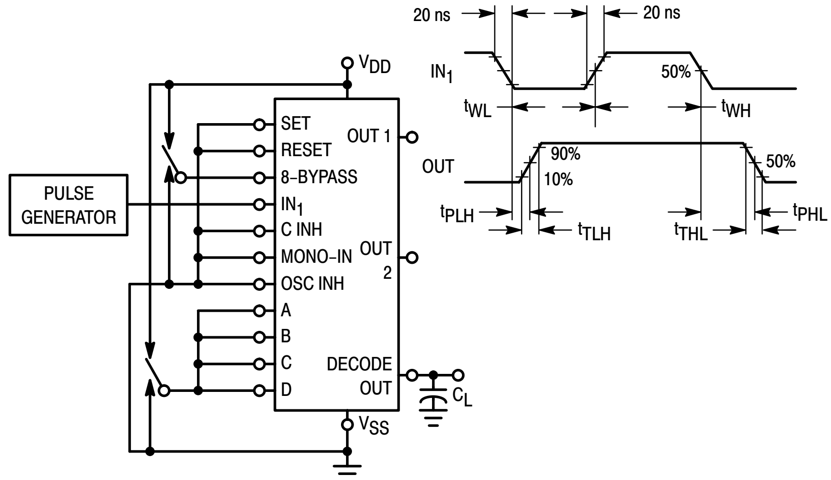


Figure 9. Switching Time Test Circuit and Waveforms

FUNCTIONAL TEST SEQUENCE

Test function (Figure 10) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8−stage sections and 255 counts are loaded in each of the 8−stage sections in parallel. All flip−flops are now at a “1”. The counter is now returned to the normal 24−stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all “1” state to an all “0” state.

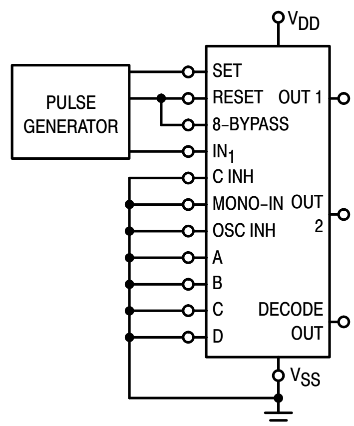
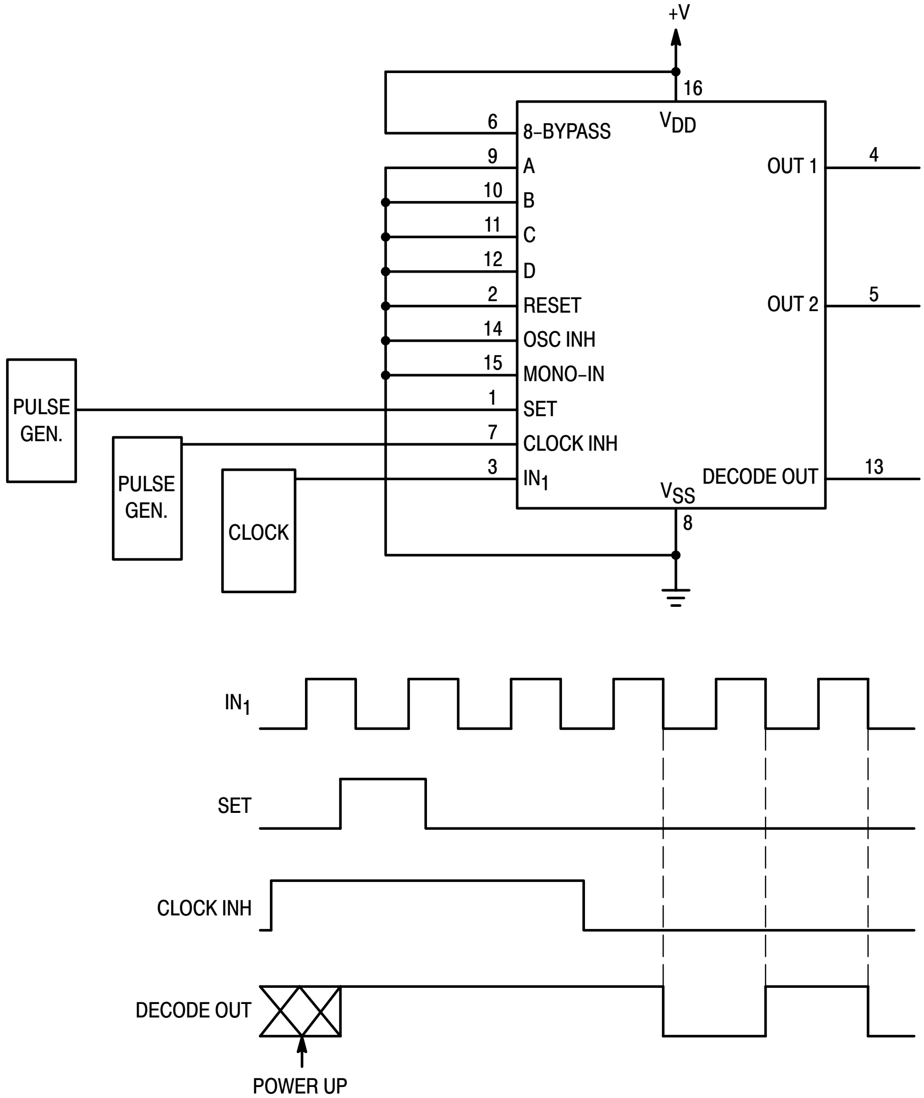


Figure 10. Functional Test Circuit

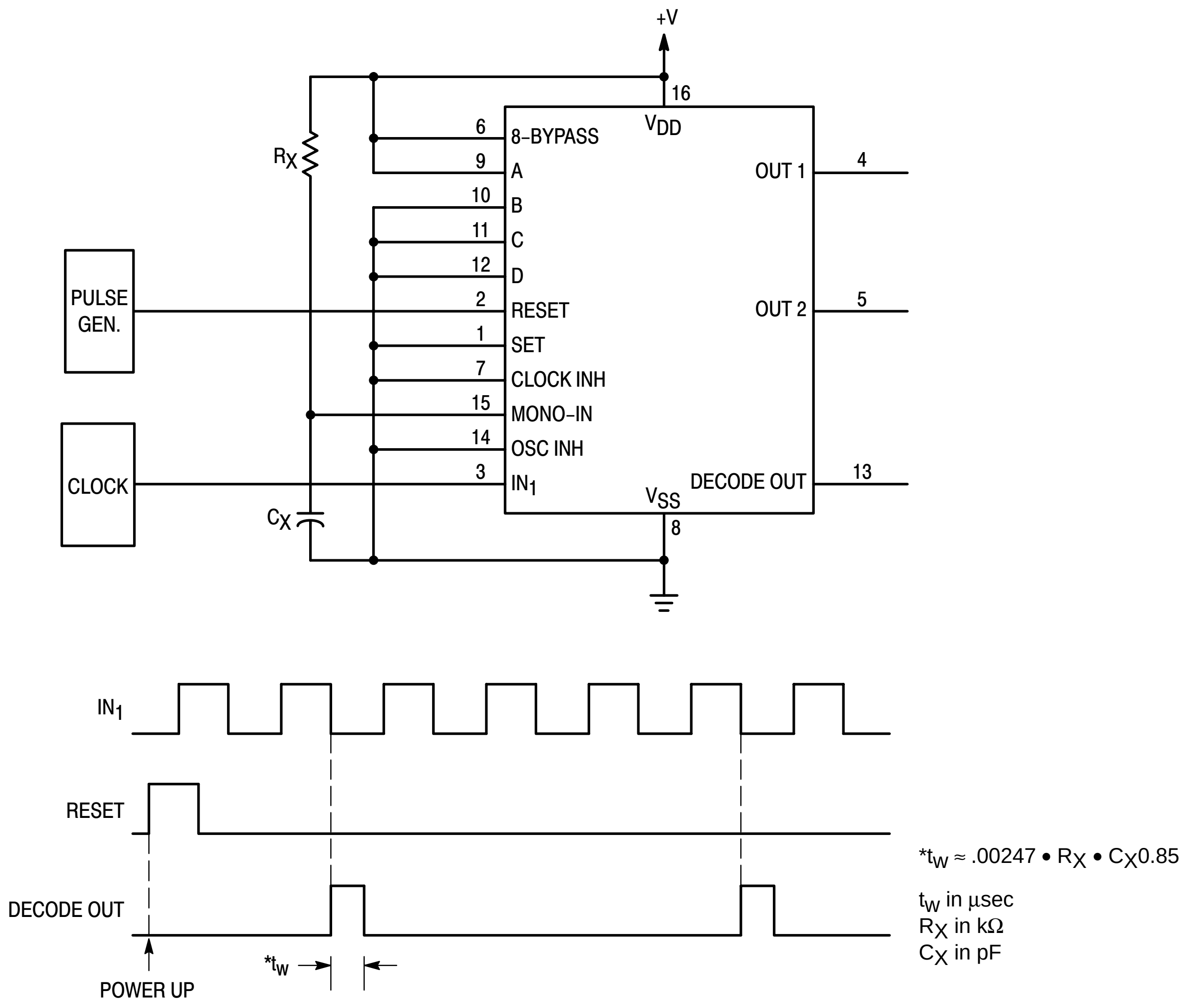
FUNCTIONAL TEST SEQUENCE

Inputs				Outputs	Comments
In_1	Set	Reset	8−Bypass	Decade Out Q1 thru Q24	All 24 stages are in Reset mode.
1	0	1	1	0	
1	1	1	1	0	Counter is in three 8 stage sections in parallel mode.
0	1	1	1	0	First “1” to “0” transition of clock.
1 0 − − −	1	1	1		255 “1” to “0” transitions are clocked in the counter.
0	1	1	1	1	The 255 “1” to “0” transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from “1” to “0”.
1	0	0	0	1	In_1 Switches to a “1”.
0	0	0	0	0	Counter Ripples from an all “1” state to an all “0” state.



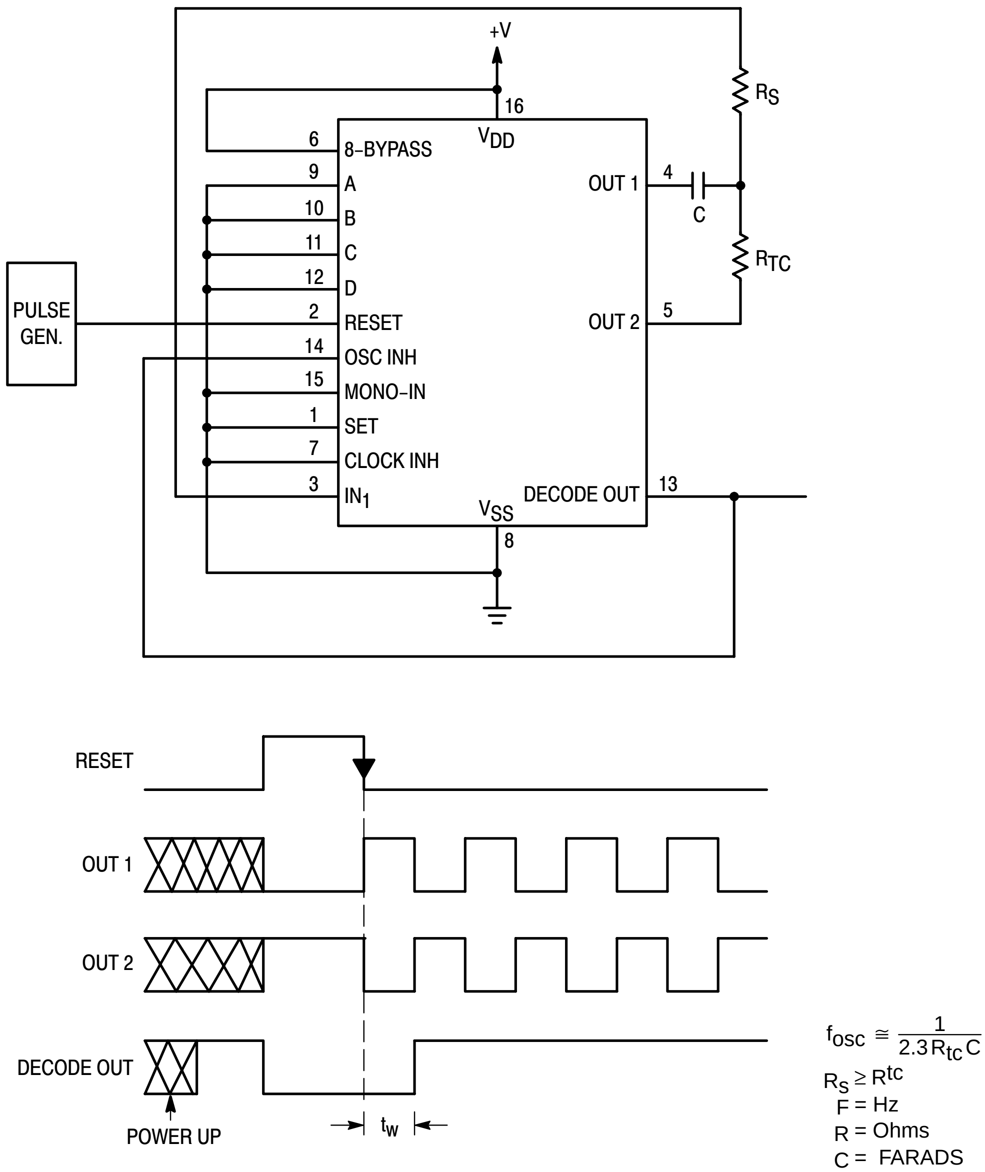
NOTE: When power is first applied to the device, DECODE OUT can be either at a high or low state. On the rising edge of a SET pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because CLOCK INH is held high, the clock source on the input pin has no effect on the output. Once CLOCK INH is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8−BYPASS, A, B, C, and D inputs, and the clock input period. A 2^n frequency division (where n = the number of stages selected from the truth table) is obtainable at DECODE OUT. A 2^0–divided output of IN_1 can be obtained at OUT_1 and OUT_2.

Figure 11. Time Interval Configuration Using an External Clock, Set, and Clock Inhibit Functions (Divide−by−2 Configured)



NOTE: When Power is first applied to the device with the RESET input going high, DECODE OUT initializes low. Bringing the RESET input low enables the chip's internal counters. After RESET goes low, the $2^n/2$ negative transition of the clock input causes DECODE OUT to go high. Since the MONO−IN input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at 2^n x (the clock period) intervals where n = the number of stages selected from the truth table.

Figure 12. Time Interval Configuration Using an External Clock, Reset, and Output Monostable to Achieve a Pulse Output (Divide−by−4 Configured)



NOTE: This circuit is designed to use the on−chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, DECODE OUT initializes to a high state. Because this output is tied directly to the OSC INH input, the oscillator is disabled. This puts the device in a low−current standby condition. The rising edge of the RESET pulse will cause the output to go low. This in turn causes OSC INH to go low. However, while RESET is high, the oscillator is still disabled (i.e.: standby condition). After RESET goes low, the output remains low for $2^n/2$ of the oscillator's period. After the part times out, the output again goes high.

Figure 13. Time Interval Configuration Using On−Chip RC Oscillator and Reset Input to Initiate Time Interval (Divide−by−2 Configured)

MC14538B

Dual Precision Retriggerable/Resettable Monostable Multivibrator

ON Semiconductor

http://onsemi.com

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

Output Pulse Width $T = R_X \cdot C_X$ (secs)
$R_X = \Omega$
C_X = Farads

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 µs to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative−Going Edge (B−Input)
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10 µs with Supplies Up to 6 V.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

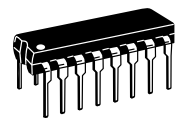
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

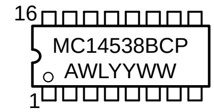
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

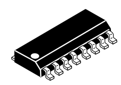
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MARKING DIAGRAMS

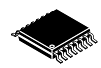


PDIP−16
P SUFFIX
CASE 648

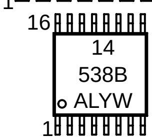


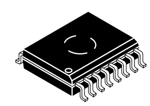


SOIC−16
D SUFFIX
CASE 751B

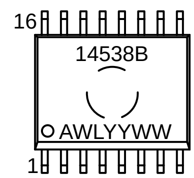


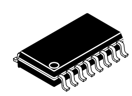
TSSOP−16
DT SUFFIX
CASE 948F



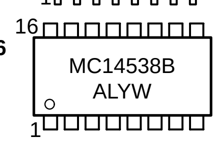


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



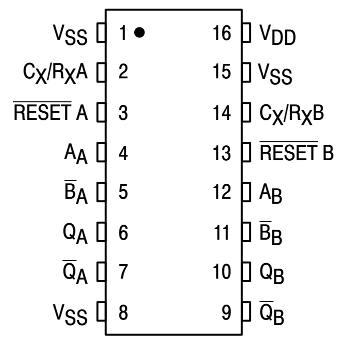
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

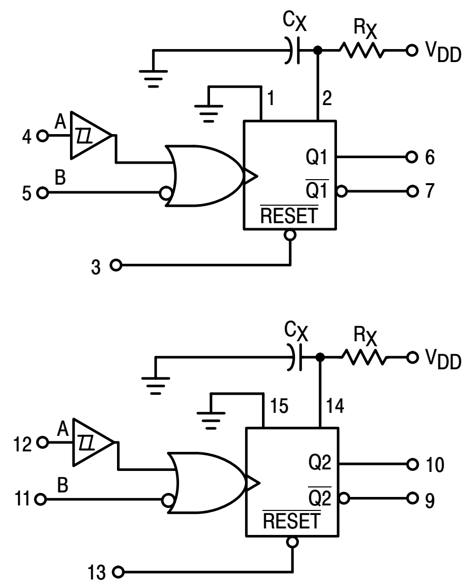
Device	Package	Shipping
MC14538BCP	PDIP−16	2000/Box
MC14538BD	SOIC−16	48/Rail
MC14538BDR2	SOIC−16	2500/Tape & Reel
MC14538BDT	TSSOP−16	96/Rail
MC14538BDTR2	TSSOP−16	2500/Tape & Reel
MC14538BDW	SOIC−16	47/Rail
MC14538BDWR2	SOIC−16	1000/Tape & Reel
MC14538BF	SOEIAJ−16	See Note 1.
MC14538BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

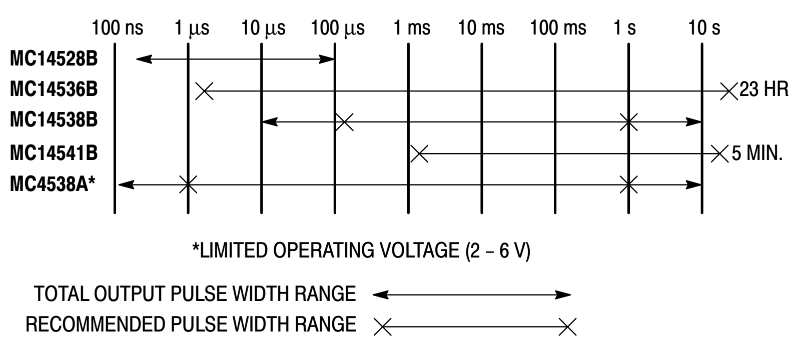


BLOCK DIAGRAM



R_X AND C_X ARE EXTERNAL COMPONENTS.
V_{DD} = PIN 16
V_{SS} = PIN 8, PIN 1, PIN 15

ONE−SHOT SELECTION GUIDE



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current, Pin 2 or 14		I_{in}	15	—	±0.05	—	±0.00001	±0.05	—	±0.5	µAdc
Input Current, Other Inputs		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance, Pin 2 or 14		C_{in}	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) Q = Low, $\overline{Q}$ = High		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Quiescent Current, Active State (Both) (Per Package) Q = High, $\overline{Q}$ = Low		I_{DD}	5.0 10 15	— — —	2.0 2.0 2.0	— — —	0.04 0.08 0.13	0.20 0.45 0.70	— — —	2.0 2.0 2.0	mAdc
Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X) (5.)		I_T	5.0 10	$I_T = (3.5 \times 10^{-2})\ R_XC_Xf + 4C_Xf + 1 \times 10^{-5}\ C_Lf$ $I_T = (8.0 \times 10^{-2})\ R_XC_Xf + 9C_Xf + 2 \times 10^{-5}\ C_Lf$ $I_T = (1.25 \times 10^{-1})\ R_XC_Xf + 12C_Xf + 3 \times 10^{-5}\ C_Lf$ where: I_T in µA (one monostable switching only), C_X in µF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ (7.)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	220	
$\overline{\text{Reset}}$ to Q or $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns		5.0	—	250	500	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	—	95	190	
Input Rise and Fall Times $\overline{\text{Reset}}$	t_r, t_f	5	—	—	15	µs
		10	—	—	5	
		15	—	—	4	
B Input		5	—	300	1.0	ms
		10	—	1.2	0.1	
		15	—	0.4	0.05	
A Input		5	No Limit			—
		10				
		15				
Input Pulse Width A, B, or Reset	t_{WH}, t_{WL}	5.0	170	85	—	ns
		10	90	45	—	
		15	80	40	—	
Retrigger Time	t_{rr}	5.0	0	—	—	ns
		10	0	—	—	
		15	0	—	—	
Output Pulse Width — Q or $\overline{Q}$ Refer to Figures 8 and 9	T					µs
C_X = 0.002 µF, R_X = 100 kΩ		5.0	198	210	230	
		10	200	212	232	
		15	202	214	234	
C_X = 0.1 µF, R_X = 100 kΩ		5.0	9.3	9.86	10.5	ms
		10	9.4	10	10.6	
		15	9.5	10.14	10.7	
C_X = 10 µF, R_X = 100 kΩ		5.0	0.91	0.965	1.03	s
		10	0.92	0.98	1.04	
		15	0.93	0.99	1.06	
Pulse Width Match between circuits in the same package. C_X = 0.1 µF, R_X = 100 kΩ	100 $[(T_1 - T_2)/T_1]$	5.0	—	± 1.0	± 5.0	%
		10	—	± 1.0	± 5.0	
		15	—	± 1.0	± 5.0	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	—	5.0	—	(8.)	kΩ
External Timing Capacitance	C_X	—	0	—	No Limit (9.)	µF

8. The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for R_X > 1 MΩ..
9. If C_X > 15 µF, use discharge protection diode per Fig. 11.

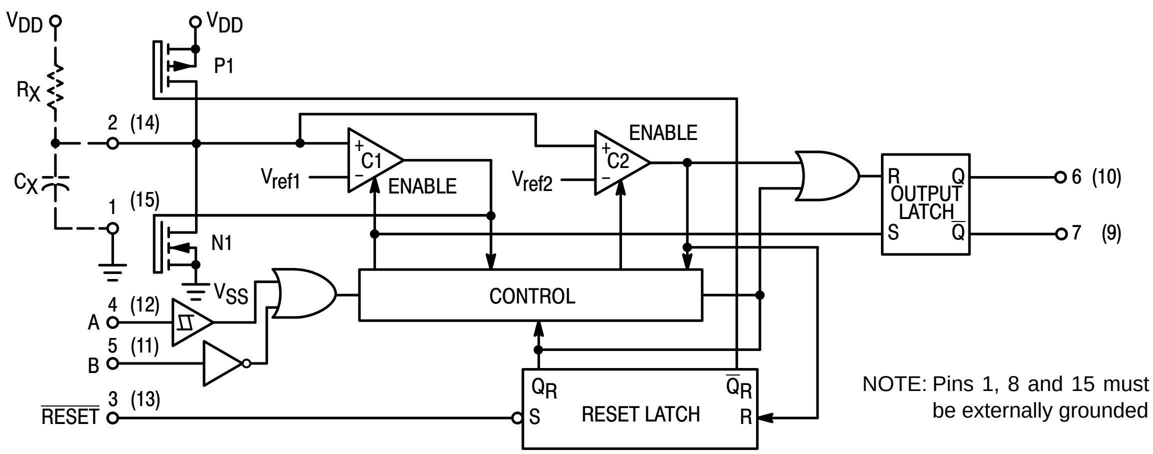


Figure 1. Logic Diagram
(1/2 of DevIce Shown)

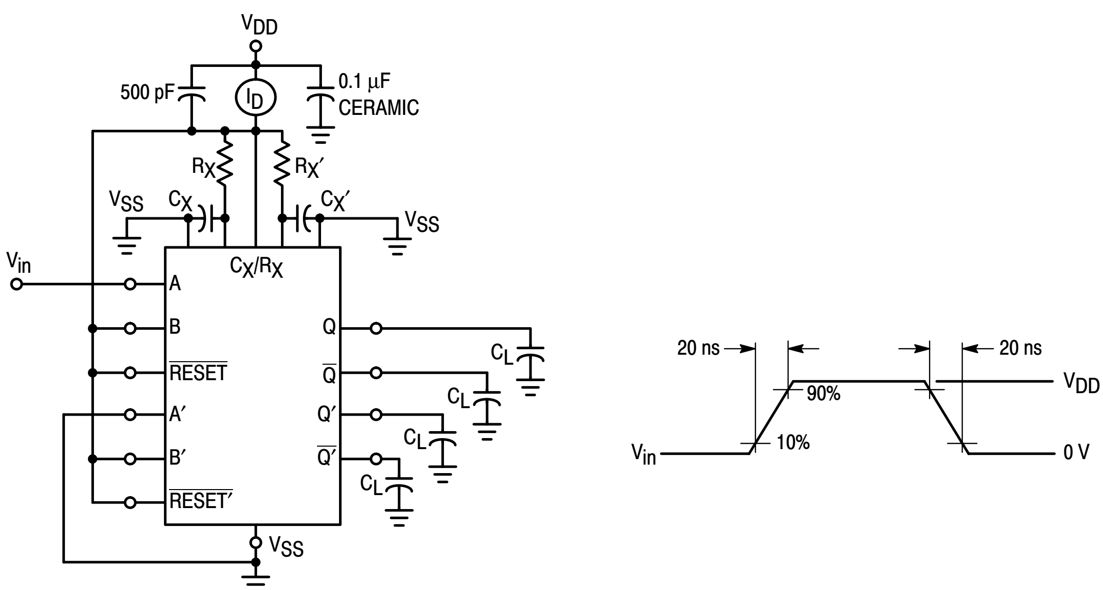
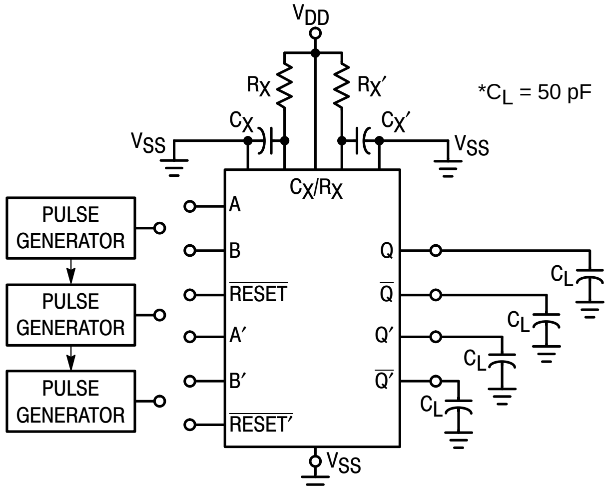


Figure 2. Power Dissipation Test Circuit and Waveforms



INPUT CONNECTIONS

Characteristics	Reset	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown In Figure 4.

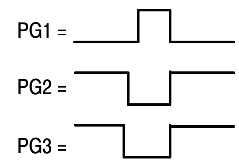


Figure 3. Switching Test Circuit

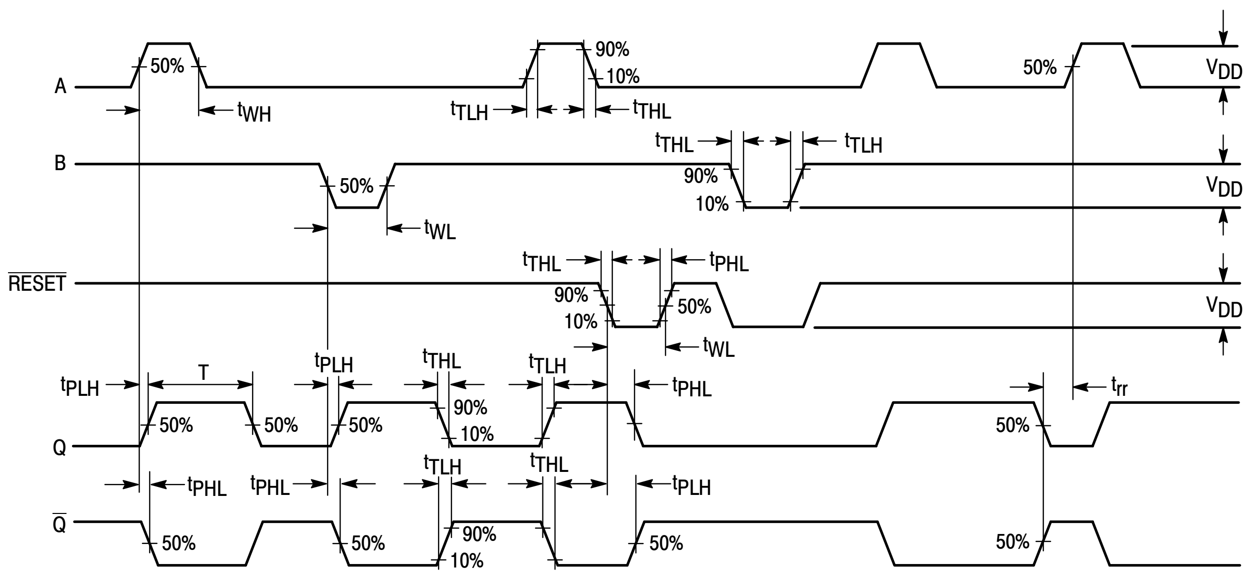


Figure 4. Switching Test Waveforms

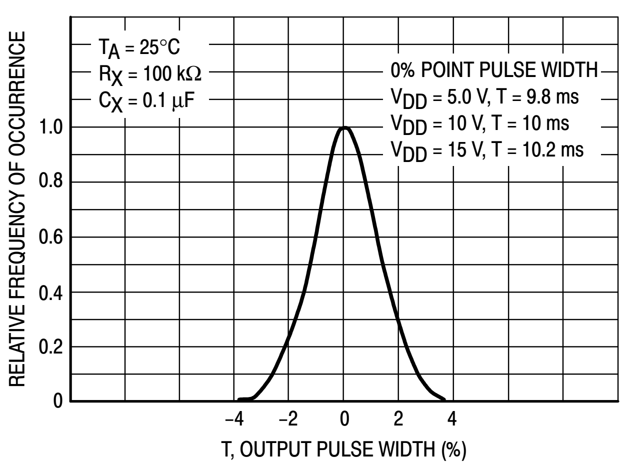


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

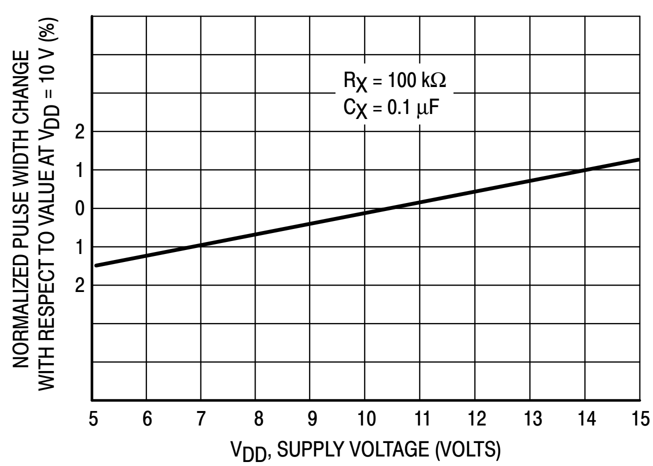


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

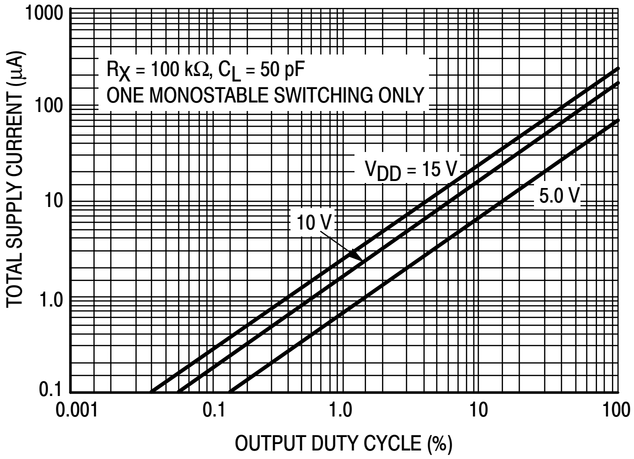


Figure 7. Typical Total Supply Current versus Output Duty Cycle

FUNCTION TABLE

Inputs			Outputs	
Reset (overbar)	**A**	**B**	**Q**	**Q̄**
H	↑	H	⊓	⊔
H	L	↓	⊓	⊔
H	↑ ↓	L	Not Triggered	
H	H	↑ ↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓ ↑	X	X	Not Triggered	

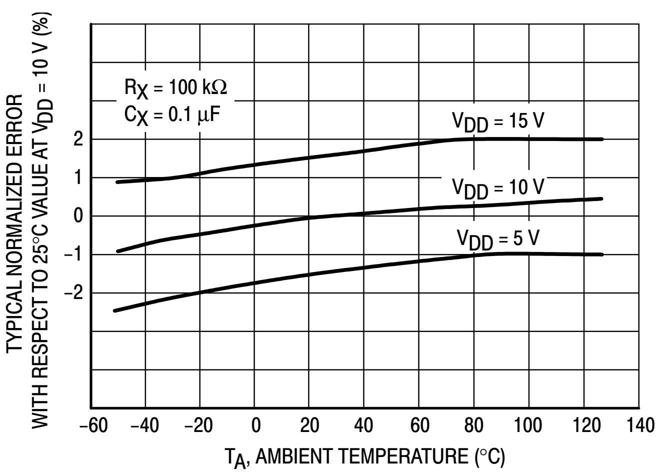


Figure 8. Typical Error of Pulse Width Equation versus Temperature

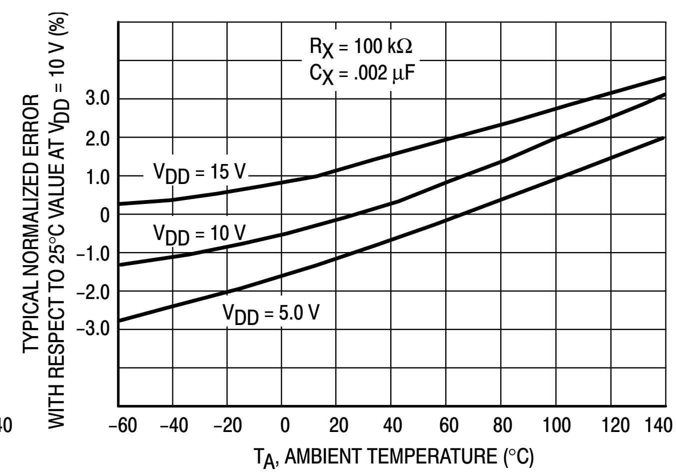


Figure 9. Typical Error of Pulse Width Equation versus Temperature

THEORY OF OPERATION

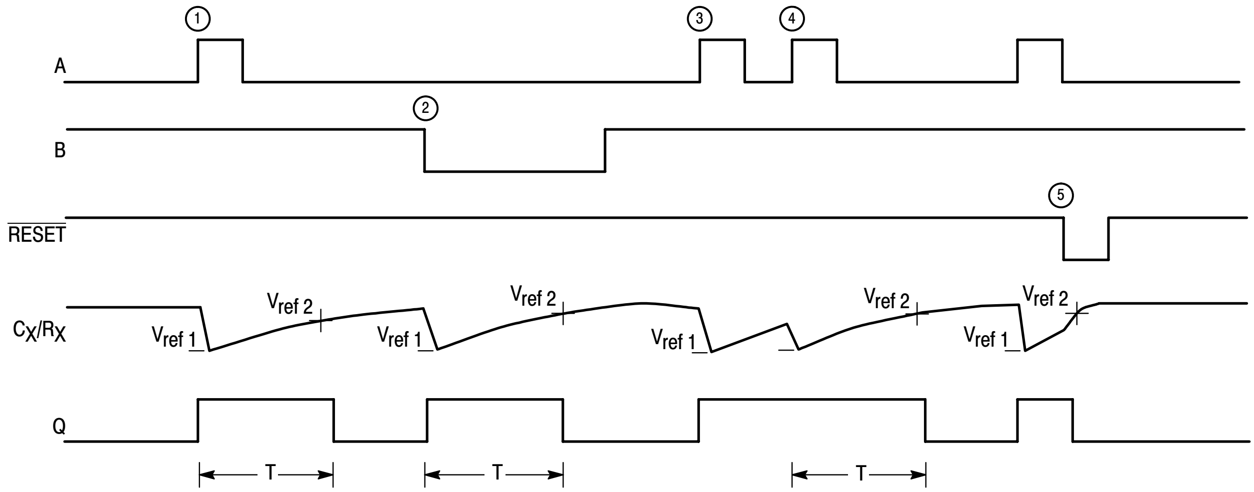


Figure 10. Timing Operation

TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{\text{Reset}}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N−channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{ref1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{ref2}, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are “off” with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at C_X/R_X will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $\overline{\text{Reset}}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 ⑤. When the voltage on the capacitor reaches $V_{ref\ 2}$, the reset latch will clear, and will then be ready to accept another pulse. It the $\overline{\text{Reset}}$ input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{\text{Q}}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $\overline{\text{Reset}}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER−DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than (V_{DD}). (C)/(10 mA). For example, if V_{DD} = 10 V and C_X = 10 μF, the V_{DD} supply should discharge no faster than (10 V) x (10 μF)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X, connected as shown in Fig. 11.

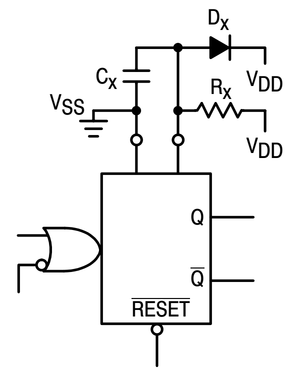


Figure 11. Use of a Diode to Limit Power Down Current Surge

TYPICAL APPLICATIONS

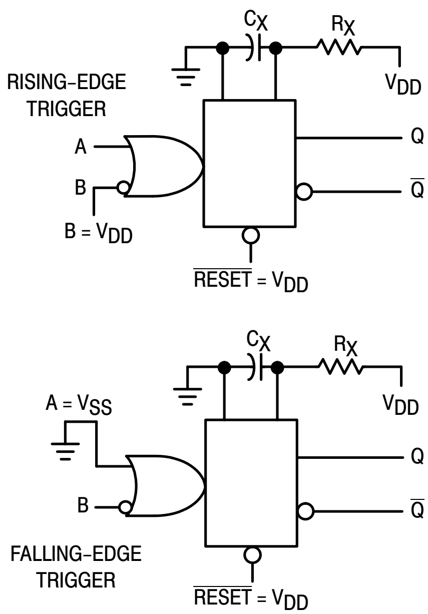


Figure 12. Retriggerable Monostables Circuitry

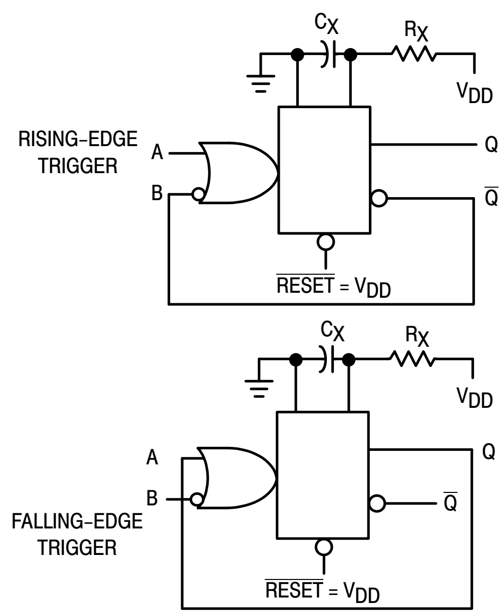


Figure 13. Non−Retriggerable Monostables Circuitry

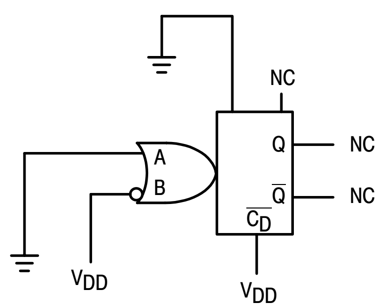


Figure 14. Connection of Unused Sections

MC14541B

Programmable Timer

The MC14541B programmable timer consists of a 16−stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power−on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power−on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16−stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Built−in Low Power RC Oscillator (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- $Q/\overline{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 = V_{DD})
  = 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = V_{SS})

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient)	±10 (per Pin)	mA
I_{out}	Output Current (DC or Transient)	±45 (per Pin)	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

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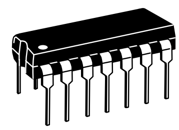
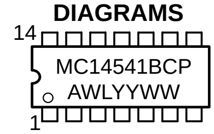
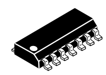
http://onsemi.com

MARKING DIAGRAMS

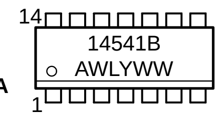


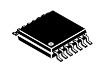
PDIP−14
P SUFFIX
CASE 646



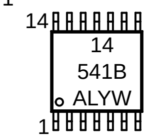


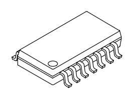
SOIC−14
D SUFFIX
CASE 751A



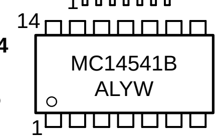


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

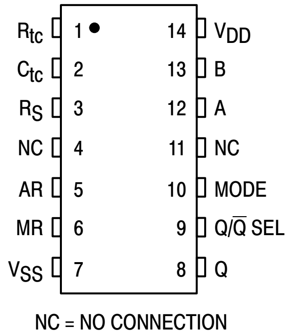
Device	Package	Shipping
MC14541BCP	PDIP−14	2000/Box
MC14541BD	SOIC−14	55/Rail
MC14541BDR2	SOIC−14	2500/Tape & Reel
MC14541BDT	TSSOP−14	96/Rail
MC14541BDTR2	TSSOP−14	2500/Tape & Reel
MC14541BF	SOEIAJ−14	See Note 1.
MC14541BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 7.96	—	– 6.42	– 12.83	—	– 4.49	—	
(V_{OH} = 9.5 Vdc)		10	– 4.19	—	– 3.38	– 6.75	—	– 2.37	—	
(V_{OH} = 13.5 Vdc)		15	– 16.3	—	– 13.2	– 26.33	—	− 9.24	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	—	1.56	3.12	—	1.09	—	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	—	4.0	8.0	—	2.8	—	
(V_{OL} = 1.5 Vdc)		15	19.3	—	15.6	31.2	—	10.9	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Auto Reset Quiescent Current (Pin 5 is low)	I_{DDR}	10	—	250	—	30	250	—	1500	µAdc
		15	—	500	—	82	500	—	2000	
Supply Current (5.) (6.) (Dynamic plus Quiescent)	I_D	5.0	I_D = (0.4 µA/kHz) f + I_{DD}							µAdc
		10	I_D = (0.8 µA/kHz) f + I_{DD}							
		15	I_D = (1.2 µA/kHz) f + I_{DD}							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. When using the on chip oscillator the total supply current (in µAdc) becomes: $I_T = I_D + 2\ C_{tc}\ V_{DD}\ f \times 10^{-3}$ where I_D is in µA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see Fig. 3) Dissipation during power−on with automatic reset enabled is typically 50 µA @ V_{DD} = 10 Vdc.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay, Clock to Q (2^8 Output)	t_{PLH}, t_{PHL}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns		5.0	—	3.5	10.5	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns		10	—	1.25	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns		15	—	0.9	2.9	
Propagation Delay, Clock to Q (2^{16} Output)	t_{PHL}, t_{PLH}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	—	6.0	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns		10	—	3.5	10	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2475 ns		15	—	2.5	7.5	
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0 10 15	— — —	1.5 4.0 6.0	0.75 2.0 3.0	MHz
MR Pulse Width	$t_{WH(R)}$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Master Reset Removal Time	t_{rem}	5.0 10 15	420 200 200	210 100 100	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

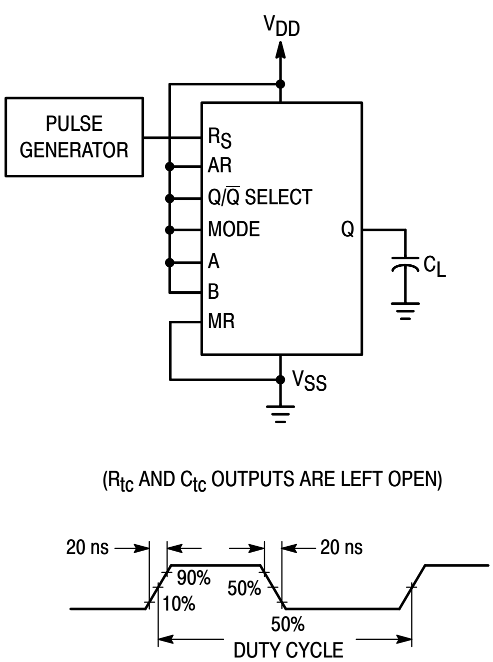


Figure 1. Power Dissipation Test Circuit and Waveform

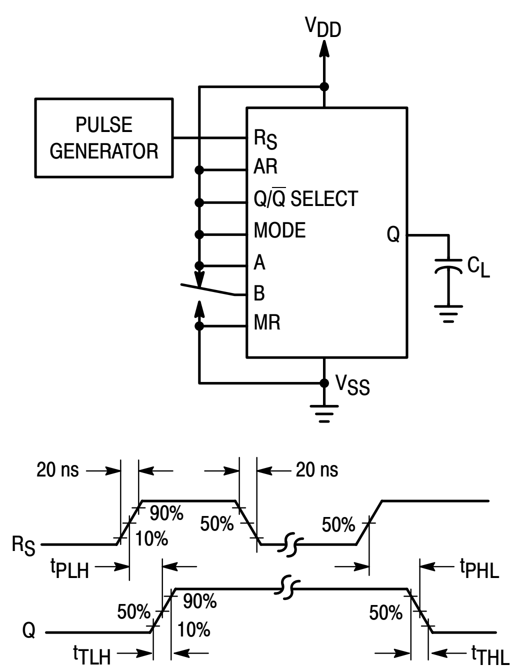
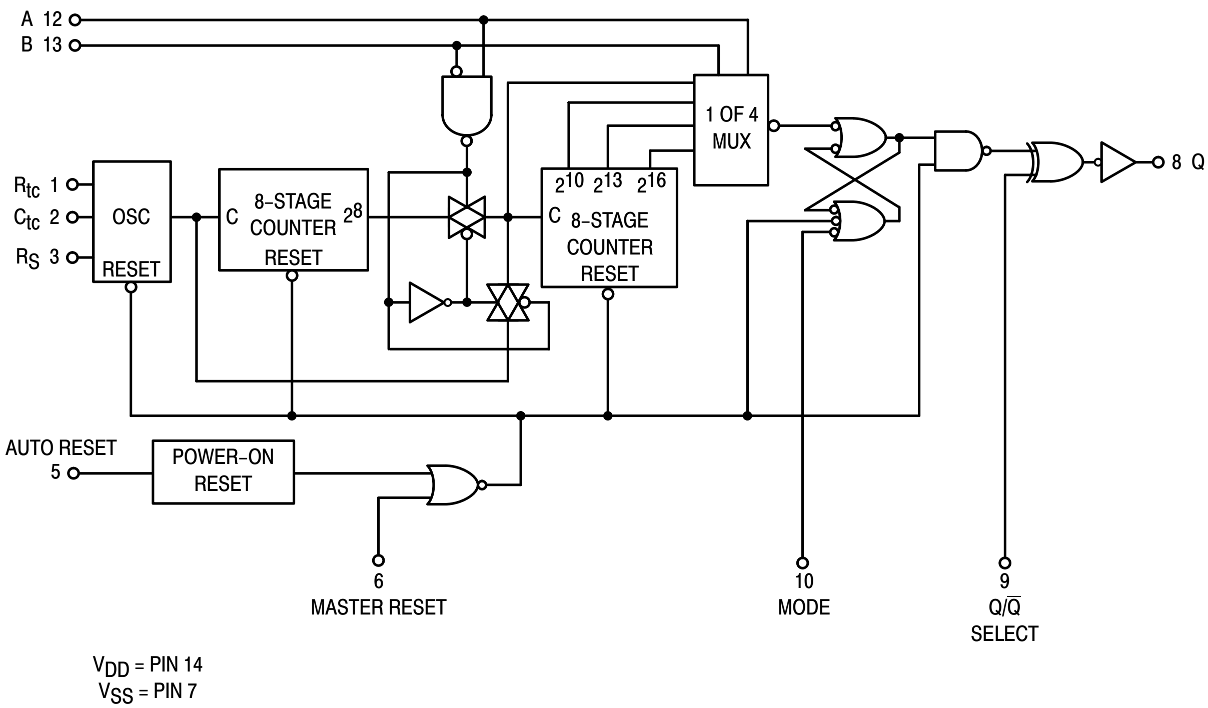


Figure 2. Switching Time Test Circuit and Waveforms

EXPANDED BLOCK DIAGRAM



FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State 0	State 1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
Q/$\overline{Q}$, 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

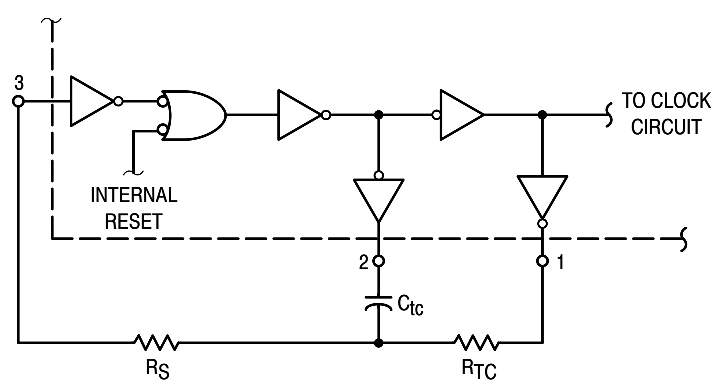


Figure 3. Oscillator Circuit Using RC Configuration

TYPICAL RC OSCILLATOR CHARACTERISTICS

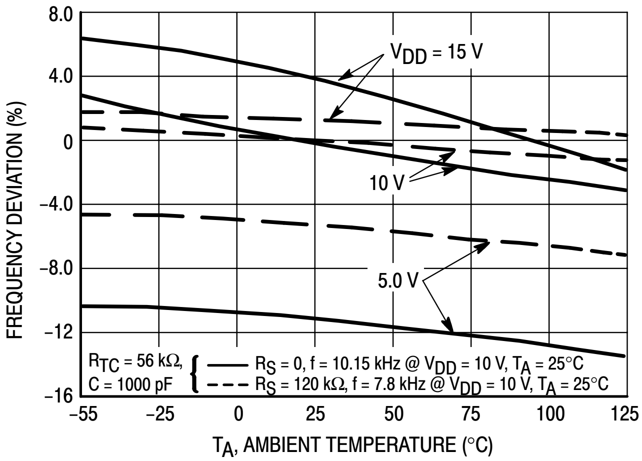


Figure 4. RC Oscillator Stability

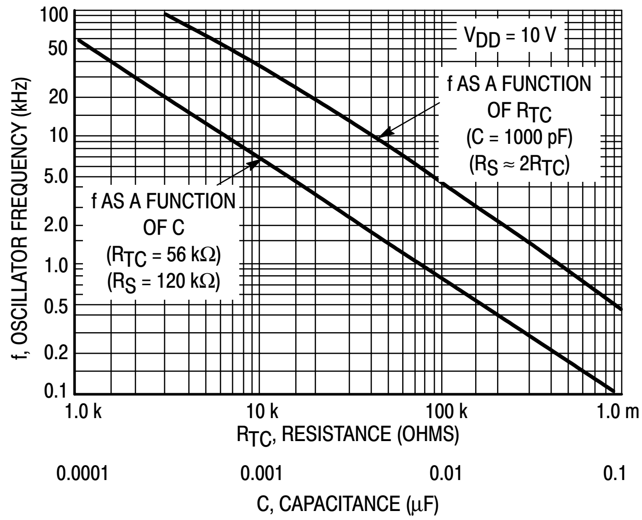


Figure 5. RC Oscillator Frequency as a Function of R_{tc} and C_{tc}

OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a “1” provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\, R_{tc} C_{tc}} \qquad \text{if } (1\text{ kHz} \le f \le 100\text{ kHz})$$

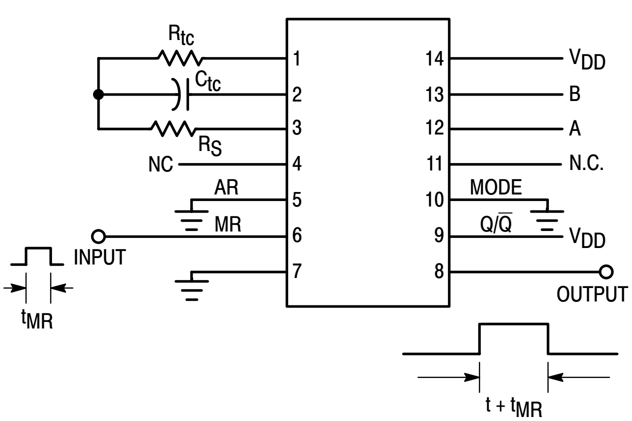
and $R_S \approx 2\, R_{tc}$ where $R_S \ge 10\ k\Omega$

The time select inputs (A and B) provide a two−bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is “1”, 2^{16} is selected for both states of B. However, when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a “0” the Q output is a “0”, correspondingly when Q/$\overline{Q}$ select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the R_S flip−flop (see Expanded Block Diagram) resets, counting commences, and after 2^{n-1} counts the R_S flip−flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This “one shot” is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

MC14543B

BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

The MC14543B BCD−to−seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4−bit storage latch and an 8421 BCD−to−seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light−emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving 2 Low−power TTL Loads, 1 Low−power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).
- Chip Complexity: 207 FETs or 52 Equivalent Gates

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	−0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
I_{OHmax} I_{OLmax}	Maximum Continuous Output Drive Current (Source or Sink)	10 (per Output)	mA
P_{OHmax} P_{OLmax}	Maximum Continuous Output Power (Source or Sink) (4.)	70 (per Output)	mW

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
4. $P_{OHmax} = I_{OH} (V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL} (V_{OL} - V_{SS})$

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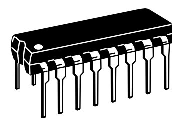
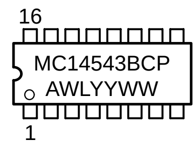
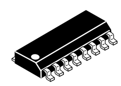
MARKING DIAGRAMS

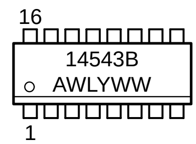


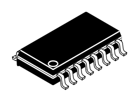
PDIP−16
P SUFFIX
CASE 648



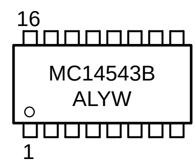


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

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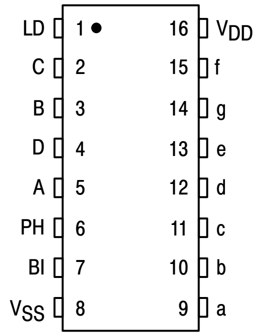
MC14543BD	SOIC−16	48/Rail
MC14543BDR2	SOIC−16	2500/Tape & Reel
MC14543BF	SOEIAJ−16	See Note 1.
MC14543BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



TRUTH TABLE

Inputs							Outputs							
LD	**BI**	**Ph***	**D**	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	†	†				Inverse of Output Combinations Above							Display as above

X = Don’t care

† = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph
For common cathode LED readouts, select Ph = 0
For common anode LED readouts, select Ph = 1

** = Depends upon the BCD code previously applied when LD = 1

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (5.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 0.5 Vdc)		10	—	—	—	– 10.1	—	—	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 9.5 Vdc)		10	—	—	—	10.1	—	—	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4		
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
(Per Package) V_{in} = 0 or V_{DD},		10	—	10	—	0.010	10	—	300	
I_{out} = 0 µA		15	—	20	—	0.015	20	—	600	
Total Supply Current (6.) (7.)	I_T	5.0	I_T = (1.6 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent,		10	I_T = (3.1 µA/kHz) f + I_{DD}							
Per Package)		15	I_T = (4.7 µA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)										

5. Noise immunity specified for worst−case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

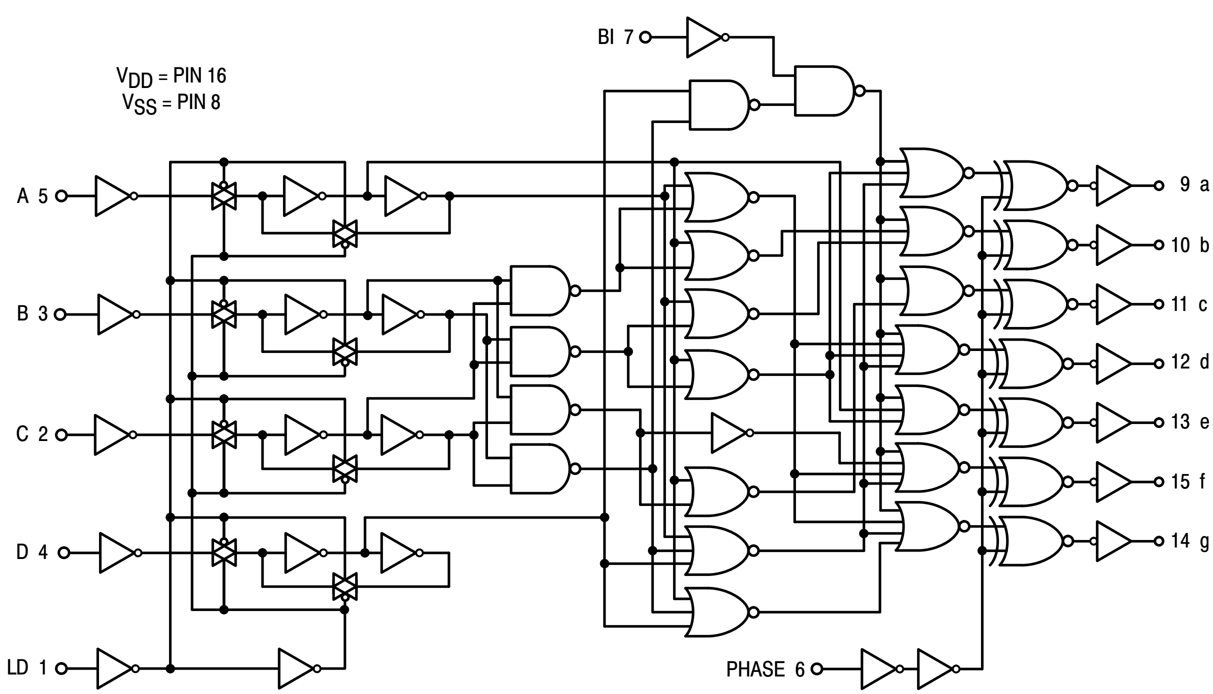
7. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS [8.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	—	40	80	
Turn−Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	—	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	—	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	—	185	370	
Turn−On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	—	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	—	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	—	155	495	
Setup Time	t_{su}	5.0	350		—	ns
		10	450		—	
		15	500		—	
Hold Time	t_h	5.0	40		—	ns
		10	30		—	
		15	20		—	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	80	40	—	

8. The formulas given are for the typical characteristics only.

LOGIC DIAGRAM



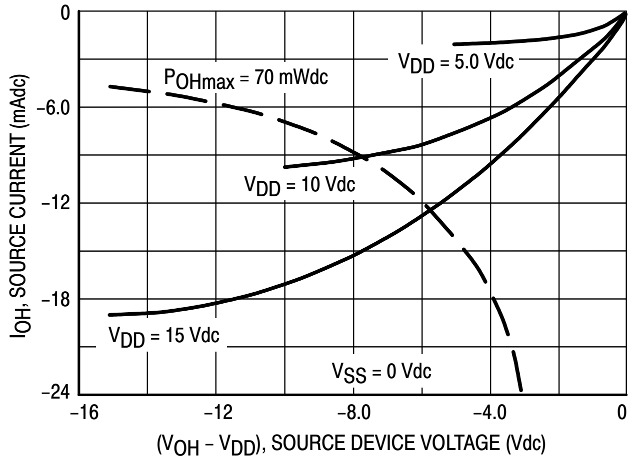


Figure 1. Typical Output Source Characteristics

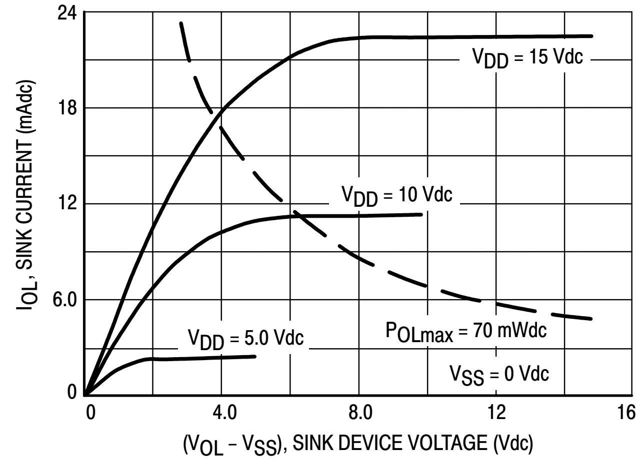


Figure 2. Typical Output Sink Characteristics

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

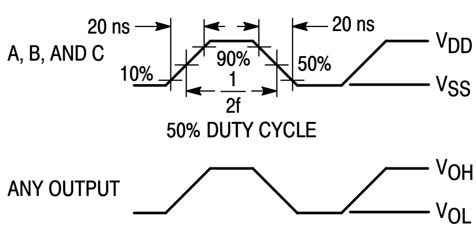
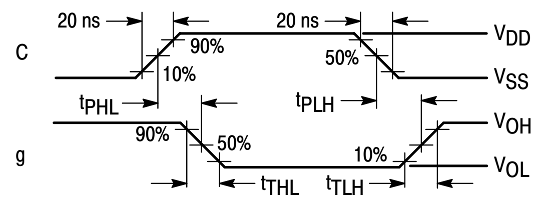
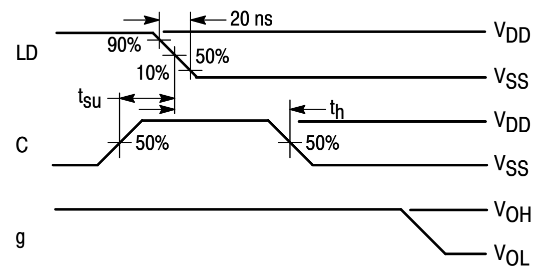


Figure 3. Dynamic Power Dissipation Signal Waveforms

(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches

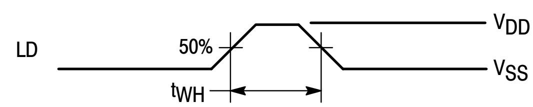
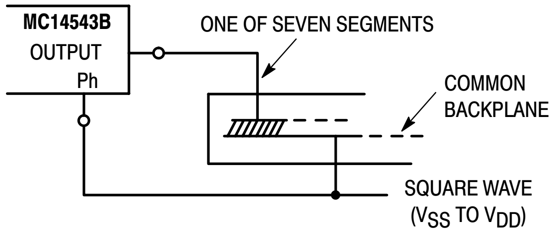


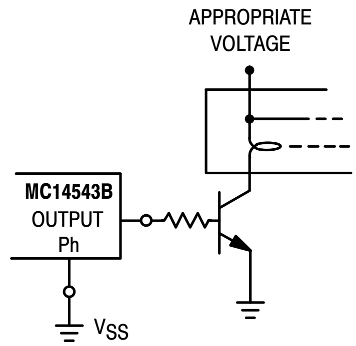
Figure 4. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

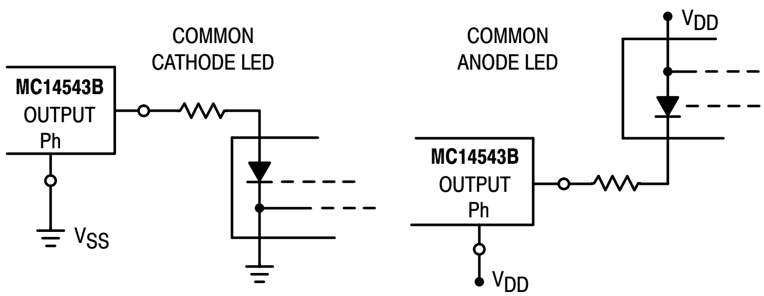
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

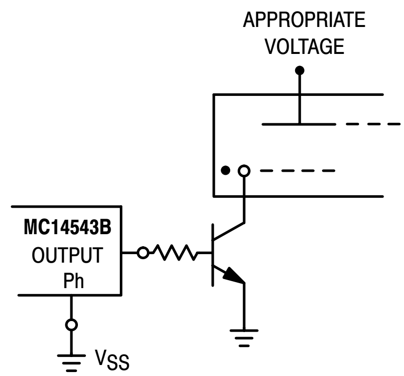


LIGHT EMITTING DIODE (LED) READOUT

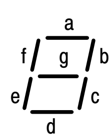


NOTE: Bipolar transistors may be added for gain (for $V_{DD} \leq 10$ V or $I_{out} \geq 10$ mA).

GAS DISCHARGE READOUT

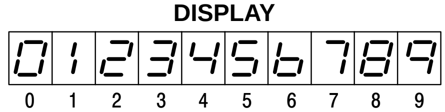


CONNECTIONS TO SEGMENTS



V_{DD} = PIN 16
V_{SS} = PIN 8

DISPLAY



MC14549B, MC14559B

Successive Approximation Registers

The MC14549B and MC14559B successive approximation registers are 8−bit registers providing all the digital control and storage necessary for successive approximation analog−to−digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when more than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End−of−Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog−to−digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8−Bit D/A Converter
- All Control Inputs Positive−Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 2 Low−Power TTL Loads, 1 Low−Power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Chip Complexity: 488 FETs or 122 Equivalent Gates

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	−0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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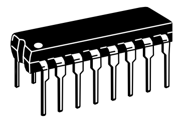
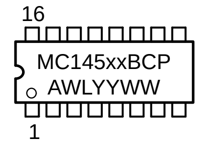
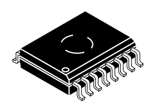
MARKING DIAGRAMS

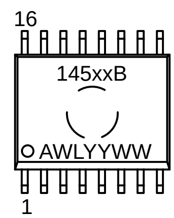


PDIP−16
P SUFFIX
CASE 648





SOIC−16
DW SUFFIX
CASE 751G

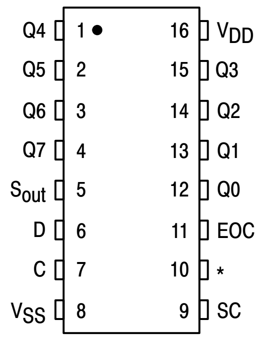


xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14549BCP	PDIP−16	25/Rail
MC14549BDWR2	SOIC−16	1000/Tape & Reel
MC14559BCP	PDIP−16	25/Rail
MC14559BDWR2	SOIC−16	1000/Tape & Reel

PIN ASSIGNMENT



*For MC14549B Pin 10 is MR input.
For MC14559B Pin 10 is FF input.

TRUTH TABLES

MC14549B

SC	SC$_{(t-1)}$	MR	MR$_{(t-1)}$	Clock	Action
X	X	X	X	↓	None
X	X	1	X	↑	Reset
1	0	0	0	↑	Start Conversion
1	X	0	1	↑	Start Conversion
1	1	0	0	↑	Continue Conversion
0	X	0	X	↑	Continue Previous Operation

X = Don’t Care t−1 = State at Previous Clock ↑

MC14559B

SC	SC$_{(t-1)}$	EOC	Clock	Action
X	X	X	↓	None
1	0	0	↑	Start Conversion
X	1	0	↑	Continue Conversion
0	0	0	↑	Continue Conversion
0	X	1	↑	Retain Conversion Result
1	X	1	↑	Start Conversion

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (3.) (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 1.2 – 0.25 – 0.62 – 1.8	 — — — —	 – 1.0 – 0.2 – 0.5 – 1.5	 – 1.7 – 0.36 – 0.9 – 3.5	 — — — —	 – 0.7 – 0.14 – 0.35 – 1.1	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink Q Outputs	I_{OL}	5.0 10 15	1.28 3.2 8.4	— — —	1.02 2.6 6.8	1.76 4.5 17.6	— — —	0.72 1.8 4.8	— — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink Pin 5, 11 only		5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) (Clock = 0 V, Other Inputs = V_{DD} or 0 V, I_{out} = 0 µA)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.8 µA/kHz) f + I_{DD} I_T = (1.6 µA/kHz) f + I_{DD} I_T = (2.4 µA/kHz) f + I_{DD}							µAdc

3. Noise immunity specified for worst−case input combination.
   Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
   2.0 V min @ V_{DD} = 10 V
   2.5 V min @ V_{DD} = 15 V
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

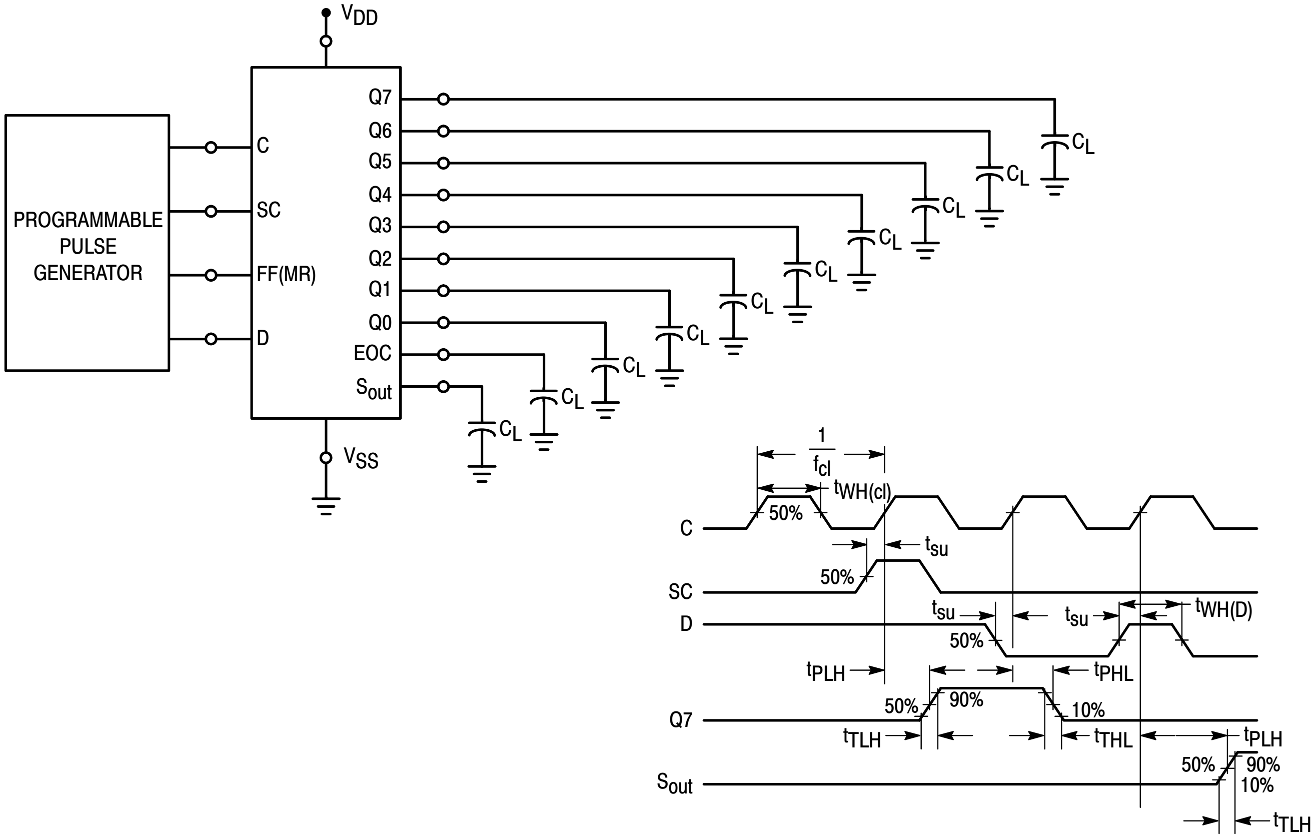
5. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	—	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	—	210	420	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	—	155	310	
Clock to S_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	—	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 277 ns		10		310	620	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	—	220	440	
Clock to EOC						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
SC, D, FF or MR Setup Time	t_{su}	5.0	250	125	—	ns
		10	100	50	—	
		15	80	40	—	
Clock Pulse Width	$t_{WH(cl)}$	5.0	700	350	—	ns
		10	270	135	—	
		15	200	100	—	
Pulse Width — D, SC, FF or MR	t_{WH}	5.0	500	250	—	ns
		10	200	100	—	
		15	160	80	—	
Clock Rise and Fall Time	t_{TLH},	5.0	—		15	µs
	t_{THL}	10	—		1.0	
		15	—	—	0.5	
Clock Pulse Frequency	f_{cl}	5.0	—	1.5	0.8	MHz
		10	—	3.0	1.5	
		15	—	4.0	2.0	

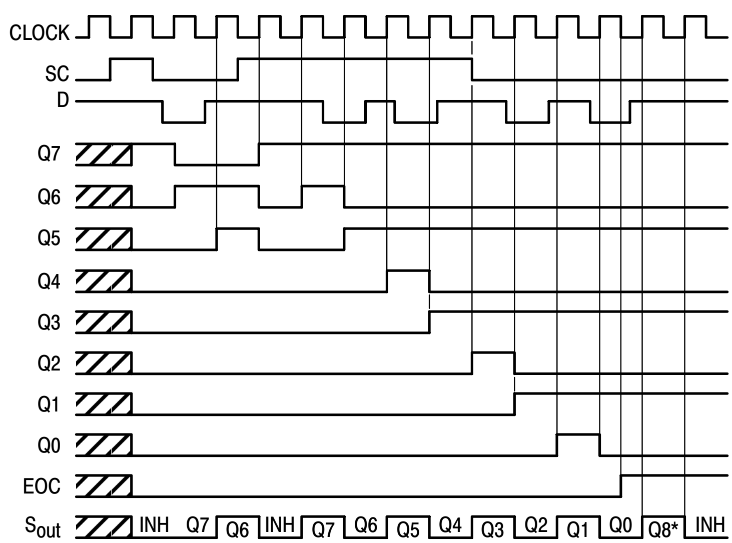
6. The formulas given are for the typical characteristics only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Pin 10 = V_{SS}

TIMING DIAGRAM



— Don't care condition

INH — Indicates Serial Out is inhibited low.

* — Q8 is ninth−bit of serial information available from 8−bit register.

NOTE: Pin 10 = V_{SS}

OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the “free run” or “strobed operation” mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock — A positive−going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert — A conversion sequence is initiated on the positive−going transition of the SC input on succeeding clock cycles.

D = Data in — Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive−going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B Only) — Resets all output to 0 on positive−going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B Only) — Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6−bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded.

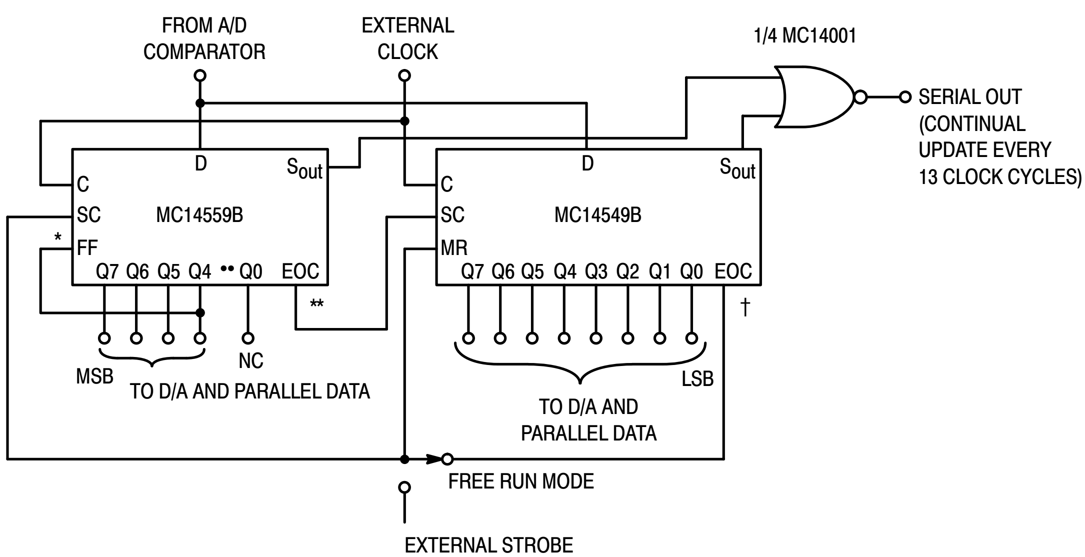
For 8−bit operation, FF is tied to V_{SS}.

For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (S_{out}) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while S_{out} of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs — After a conversion is initiated the Q’s on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert — This output goes high on the negative−going transition of the clock following FF = 1 (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out — Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.



* FF allows EOC to activate as if in 4−stage register.
** Cascading using EOC guaranteed; no stable unfunctional state.
† Completion of conversion automatically re−initiates cycle in free run mode.

Figure 1. 12−Bit Conversion Scheme

TYPICAL APPLICATIONS

Externally Controlled 6−Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8−Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12−Bit ADC (Figure 4)

Because each successive approximation register (SAR) has a capability of handling only an eight−bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch−on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non−functional condition.

This 12−bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of the 12−bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

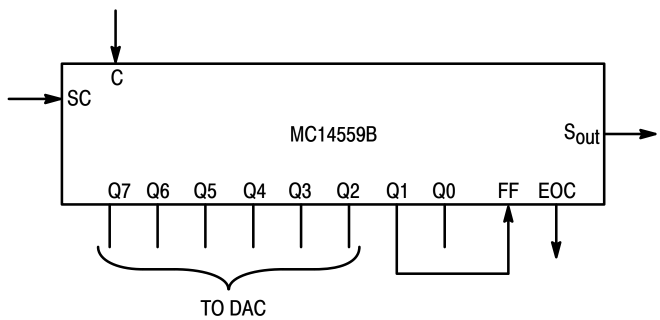


Figure 2. Externally Controlled 6−Bit ADC

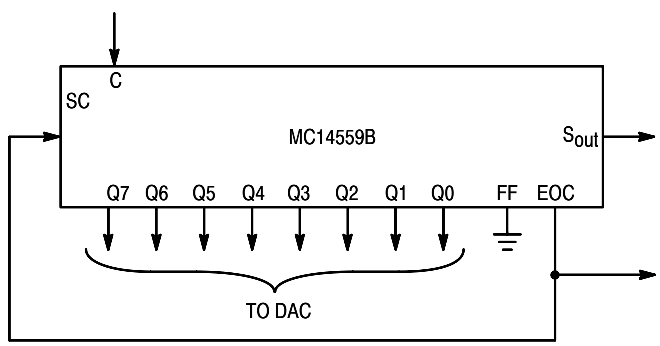


Figure 3. Continuously Cycling 8−Bit ADC

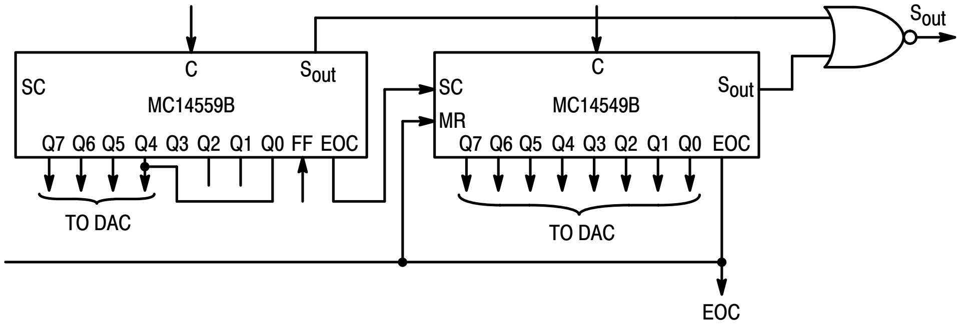


Figure 4. Continuously Cycling 12−Bit ADC

Externally Controlled 12−Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

Additional Motorola Parts for Successive Approximation ADC

Monolithic digital−to−analog converters — The MC1408/1508 converter has eight−bit resolution and is available with 6, 7, and 8−bit accuracy. **The amplifier−comparator block —** The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA−ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN−716.

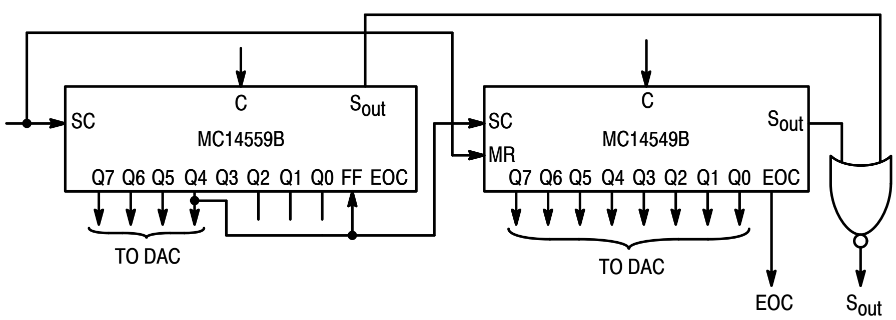


Figure 5. Externally Controlled 12−Bit ADC

MC14551B

Quad 2-Channel Analog Multiplexer/Demultiplexer

The MC14551B is a digitally−controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
  Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low Noise — 12 nV$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- For Low R_{ON}, Use The HC4051, HC4052, or HC4053 High−Speed CMOS Devices
- Switch Function is Break Before Make

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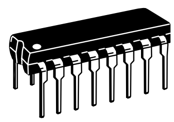
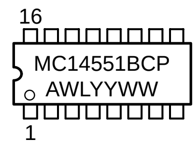
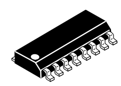
MARKING DIAGRAMS

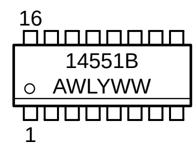


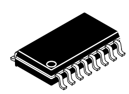
PDIP−16
P SUFFIX
CASE 648



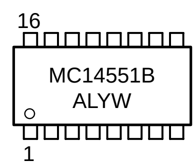


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

MAXIMUM RATINGS (2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Input & V_{EE} for Switch I/O)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (3.)	500	mW
T_A	Ambient Temperature Range	– 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for Switch I/O.

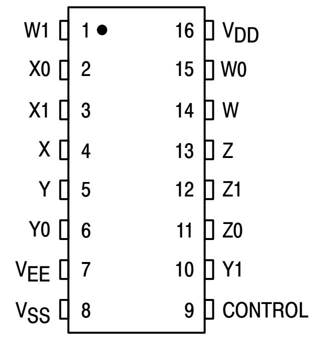
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

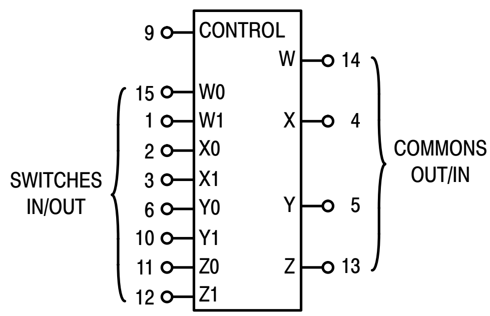
ORDERING INFORMATION

Device	Package	Shipping
MC14551BCP	PDIP−16	2000/Box
MC14551BD	SOIC−16	48/Rail
MC14551BDR2	SOIC−16	2500/Tape & Reel
MC14551BF	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT





V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

NOTE: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq$ V_{SS}.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} – 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq$ 500 mV (5.)	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} – V_{out})/R_{on}$, is not included.)			Typical	(0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.36 µA/kHz) f + I_{DD}				µA
CONTROL INPUT (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High−Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	µA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — W, X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	$V_{p–p}$
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 3)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	µV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq$ 500 mV (5.), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off−Channel Leakage Current (Figure 8)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

4. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
5. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, V_{EE} ≤ V_{SS})

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ (6.)	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ) t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 35 15 12	 90 40 30	ns
Control Input to Output (R_L = 10 kΩ) V_{EE} = V_{SS} (Figure 4)	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 350 140 100	 875 350 250	ns
Second Harmonic Distortion R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p}	—	10	—	0.07	—	%
Bandwidth (Figure 5) R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p–p, 20 Log (V_{out}/V_{in}) = − 3 dB, C_L = 50 pF	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p–p, f_{in} = 55 MHz	—	10	—	– 50	—	dB
Channel Separation (Figure 6) R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p–p, f_{in} = 3 MHz	—	10	—	– 50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 R1 = 1 kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns	—	10	—	75	—	mV

6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

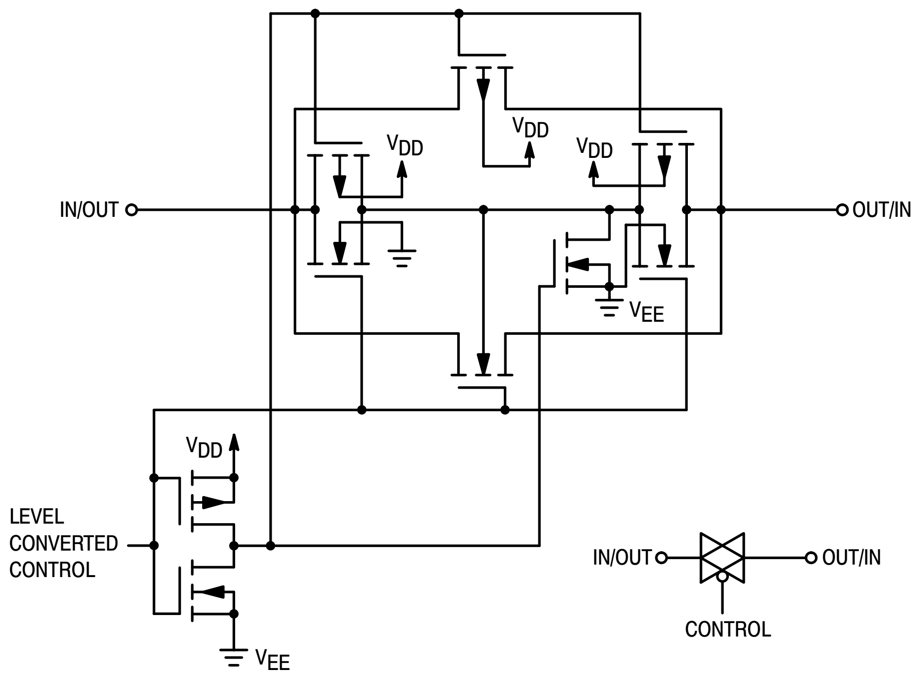


Figure 1. Switch Circuit Schematic

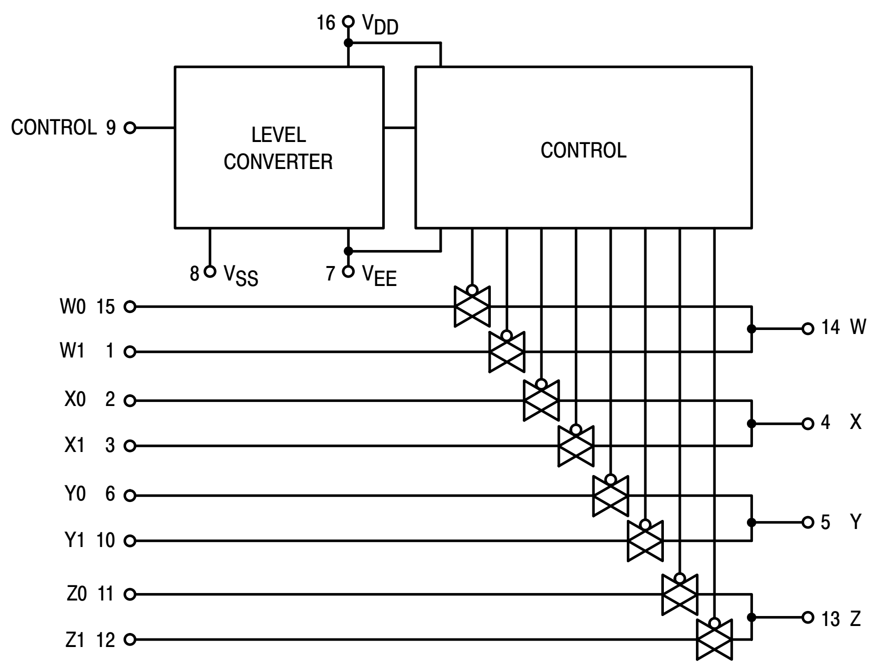


Figure 2. MC14551B Functional Diagram

TEST CIRCUITS

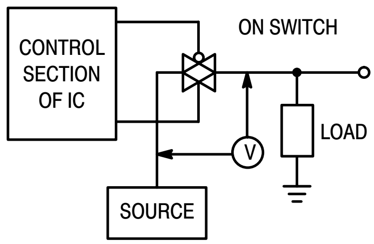


Figure 3. ΔV Across Switch

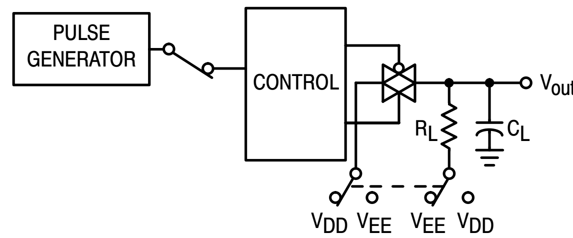


Figure 4. Propagation Delay Times, Control to Output

Control input used to turn ON or OFF the switch under test.

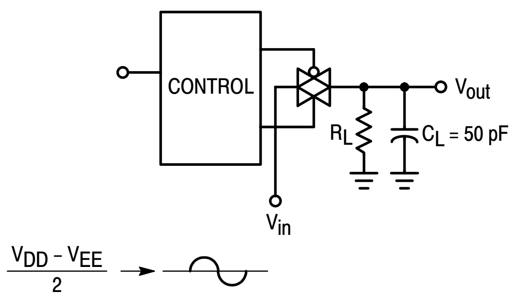


Figure 5. Bandwidth and Off−Channel Feedthrough Attenuation

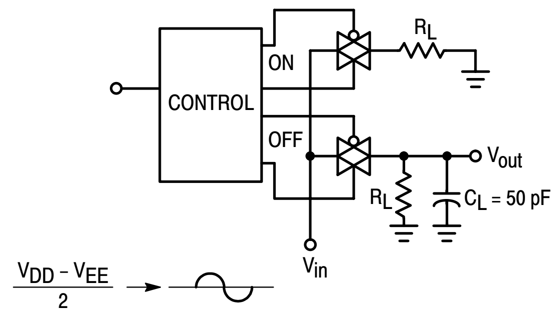


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

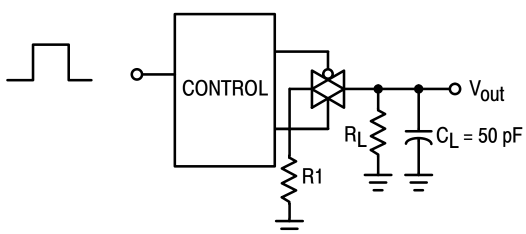


Figure 7. Crosstalk, Control Input to Common O/I

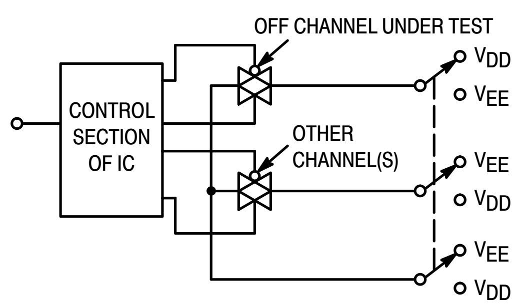


Figure 8. Off Channel Leakage

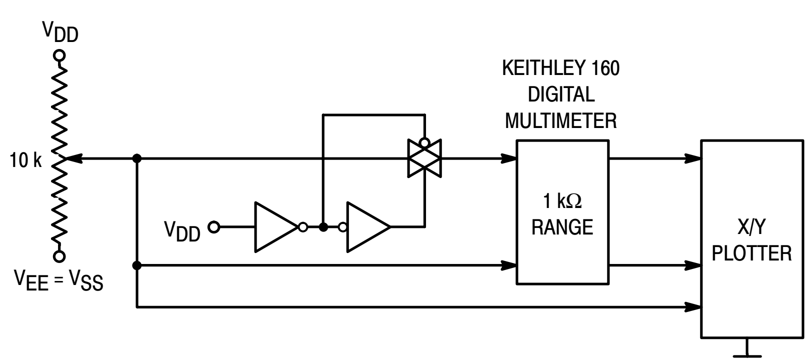


Figure 9. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

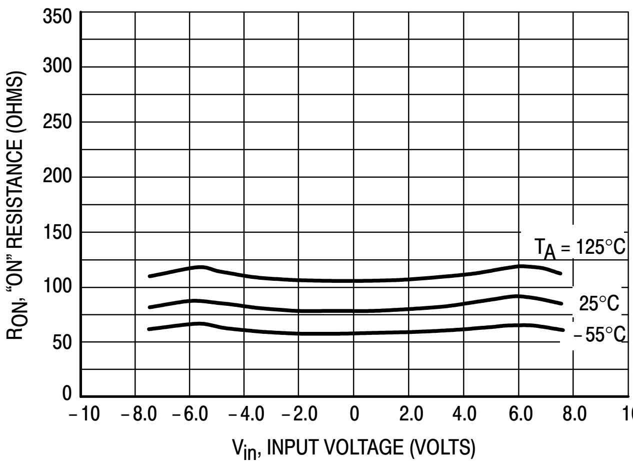


Figure 10. V_{DD} @ 7.5 V, V_{EE} @ – 7.5 V

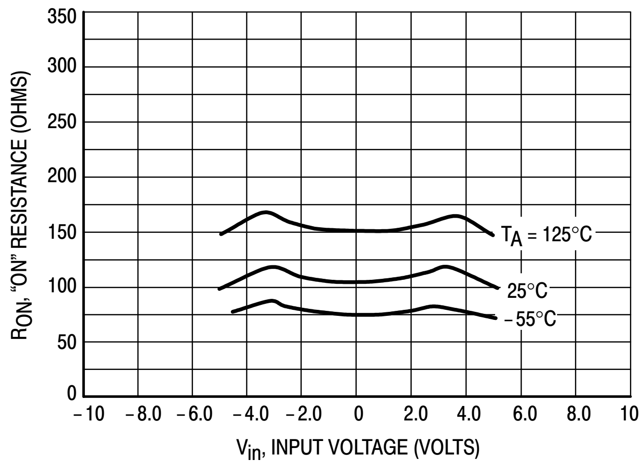


Figure 11. V_{DD} @ 5.0 V, V_{EE} @ – 5.0 V

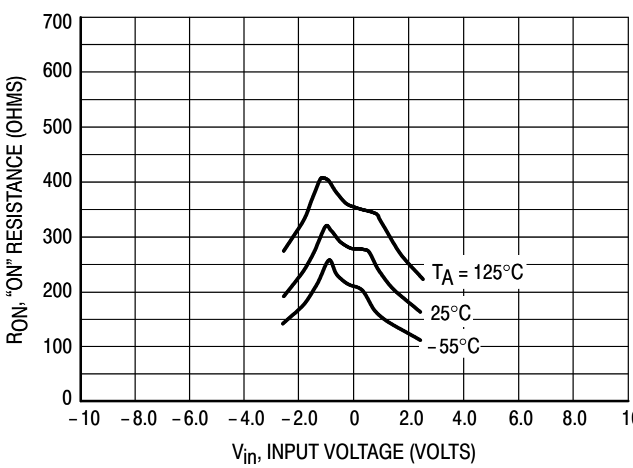


Figure 12. V_{DD} @ 2.5 V, V_{EE} @ – 2.5 V

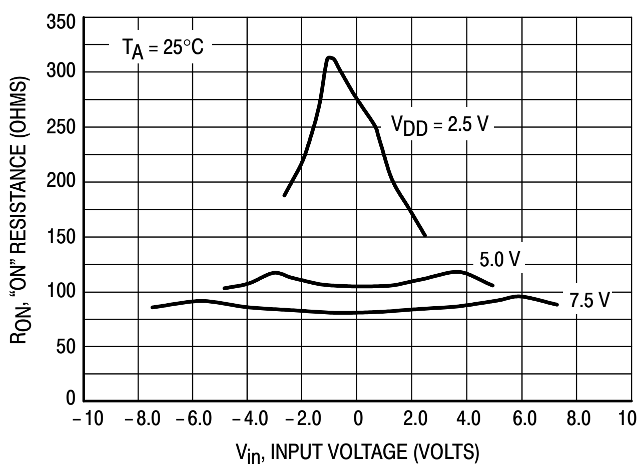


Figure 13. Comparison at 25°C, V_{DD} @ – V_{EE}

APPLICATIONS INFORMATION

Figure A illustrates use of the on−chip level converter detailed in Figure 2. The 0−to−5 volt Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 volt maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 volt maximum swing below V_{SS}. The example shows a ± 4.5 volt signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{EE} is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 volts, V_{SS} = + 5 volts, and V_{EE} = – 3 volts is acceptable. See the table below.

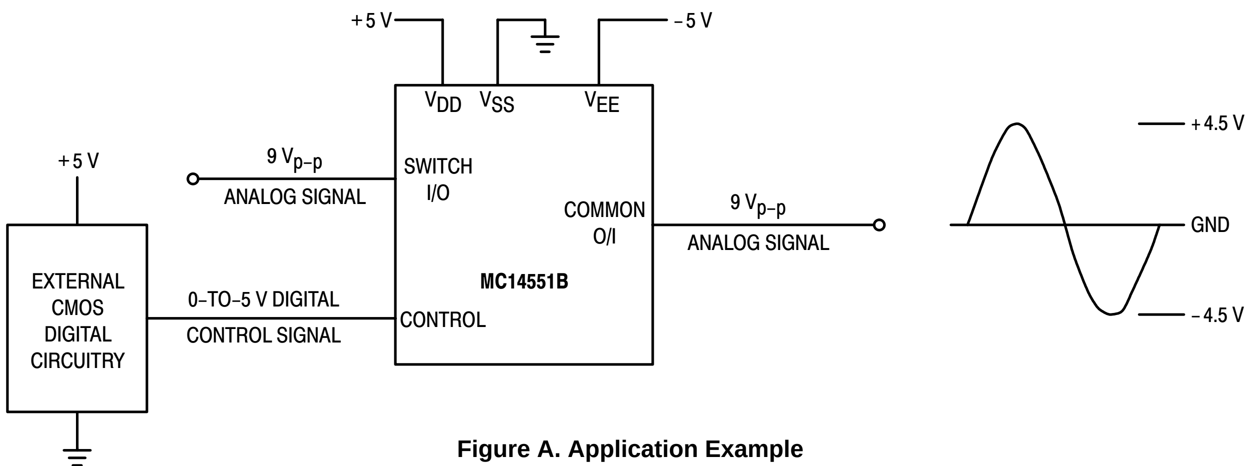


Figure A. Application Example

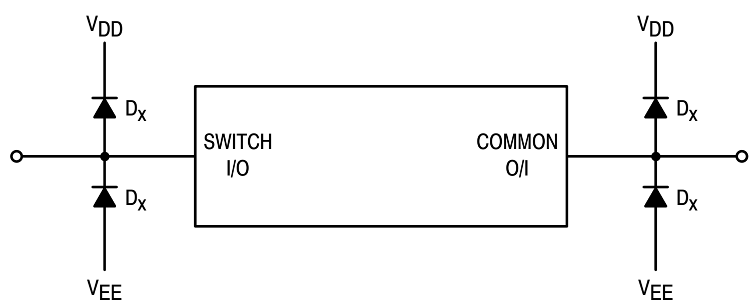


Figure B. External Schottky or Germanium Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	– 8	+ 8/0	+ 8 to – 8 = 16 V_{p-p}
+ 5	0	– 12	+ 5/0	+ 5 to – 12 = 17 V_{p-p}
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V_{p-p}
+ 5	0	– 5	+ 5/0	+ 5 to – 5 = 10 V_{p-p}
+ 10		– 5	+ 10/ + 5	+ 10 to – 5 = 15 V_{p-p}

MC14553B

3-Digit BCD Counter

The MC14553B 3−digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on−chip oscillator provides the low−frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On−Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

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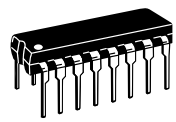
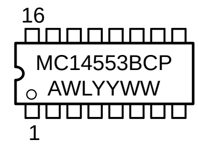
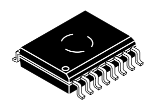
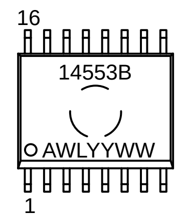


PDIP−16
P SUFFIX
CASE 648





SOIC−16
DW SUFFIX
CASE 751G



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14553BCP	PDIP−16	25/Rail
MC14553BDW	SOIC−16	47/Rail

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	+20	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

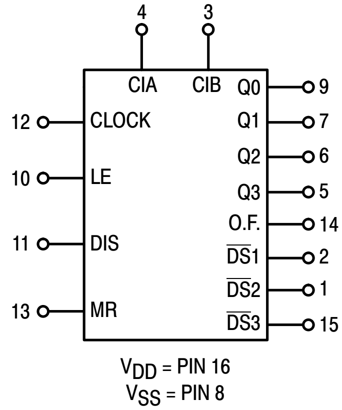


Figure 1. Block Diagram

TRUTH TABLE

Inputs				
Master Reset	**Clock**	**Disable**	**LE**	**Outputs**
0	↑	0	0	No Change
0	↓	0	0	Advance
0	X	1	X	No Change
0	1	↑	0	Advance
0	1	↓	0	No Change
0	0	X	X	No Change
0	X	X	↑	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don’t Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 3.)	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source —		5.0	– 0.25	—	– 0.2	– 0.36	—	−0.14	—	
(V_{OH} = 9.5 Vdc) Pin 3		10	– 0.62	—	– 0.5	– 0.9	—	−0.35	—	
(V_{OH} = 13.5 Vdc)		15	– 1.8	—	– 1.5	– 3.5	—	−1.1	—	
(V_{OH} = 4.6 Vdc) Source —		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	mAdc
(V_{OH} = 9.5 Vdc) Other		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc) Outputs		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink —	I_{OL}	5.0	0.5	—	0.4	0.88	—	0.28	—	mAdc
(V_{OL} = 0.5 Vdc) Pin 3		10	1.1	—	0.9	2.25	—	0.65	—	
(V_{OL} = 1.5 Vdc)		15	1.8	—	1.5	8.8	—	1.20	—	
(V_{OL} = 0.4 Vdc) Sink — Other		5.0	3.0	—	2.5	4.0	—	1.6	—	mAdc
(V_{OL} = 0.5 Vdc) Outputs		10	6.0	—	5.0	8.0	—	3.5	—	
(V_{OL} = 1.5 Vdc)		15	18	—	15	20	—	10	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	—	5.0	—	0.010	5.0	—	150	µAdc
(Per Package)		10	—	10	—	0.020	10	—	300	
MR = V_{DD}		15	—	20	—	0.030	20	—	600	
Total Supply Current (Note 4., 5.)	I_T	5.0	I_T = (0.35 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package)		10	I_T = (0.85 µA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)		15	I_T = (1.50 µA/kHz) f + I_{DD}							

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L – 50)\text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (Note 6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ (Note 7.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	2a	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Clock to BCD Out	2a	t_{PLH}, t_{PHL}	5.0 10 15	— — —	900 500 200	1800 1000 400	ns
Clock to Overflow	2a	t_{PHL}	5.0 10 15	— — —	600 400 200	1200 800 400	ns
Reset to BCD Out	2b	t_{PHL}	5.0 10 15	— — —	900 500 300	1800 1000 600	ns
Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time	2b	t_{su}	5.0 10 15	600 400 200	300 200 100	— — —	ns
Removal Time Latch Enable to Clock	2b	t_{rem}	5.0 10 15	– 80 – 10 0	– 200 – 70 – 50	— — —	ns
Clock Pulse Width	2a	$t_{WH(cl)}$	5.0 10 15	550 200 150	275 100 75	— — —	ns
Reset Pulse Width	2b	$t_{WH(R)}$	5.0 10 15	1200 600 450	600 300 225	— — —	ns
Reset Removal Time	—	t_{rem}	5.0 10 15	– 80 0 20	– 180 – 50 – 30	— — —	ns
Input Clock Frequency	2a	f_{cl}	5.0 10 15	— — —	1.5 5.0 7.0	0.9 2.5 3.5	MHz
Input Clock Rise Time	2b	t_{TLH}	5.0 10 15		No Limit		ns
Disable, MR, Latch Enable Rise and Fall Times	—	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	µs
Scan Oscillator Frequency (C1 measured in µF)	1	f_{osc}	5.0 10 15	— — —	1.5/C1 4.2/C1 7.0/C1	— — —	Hz

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

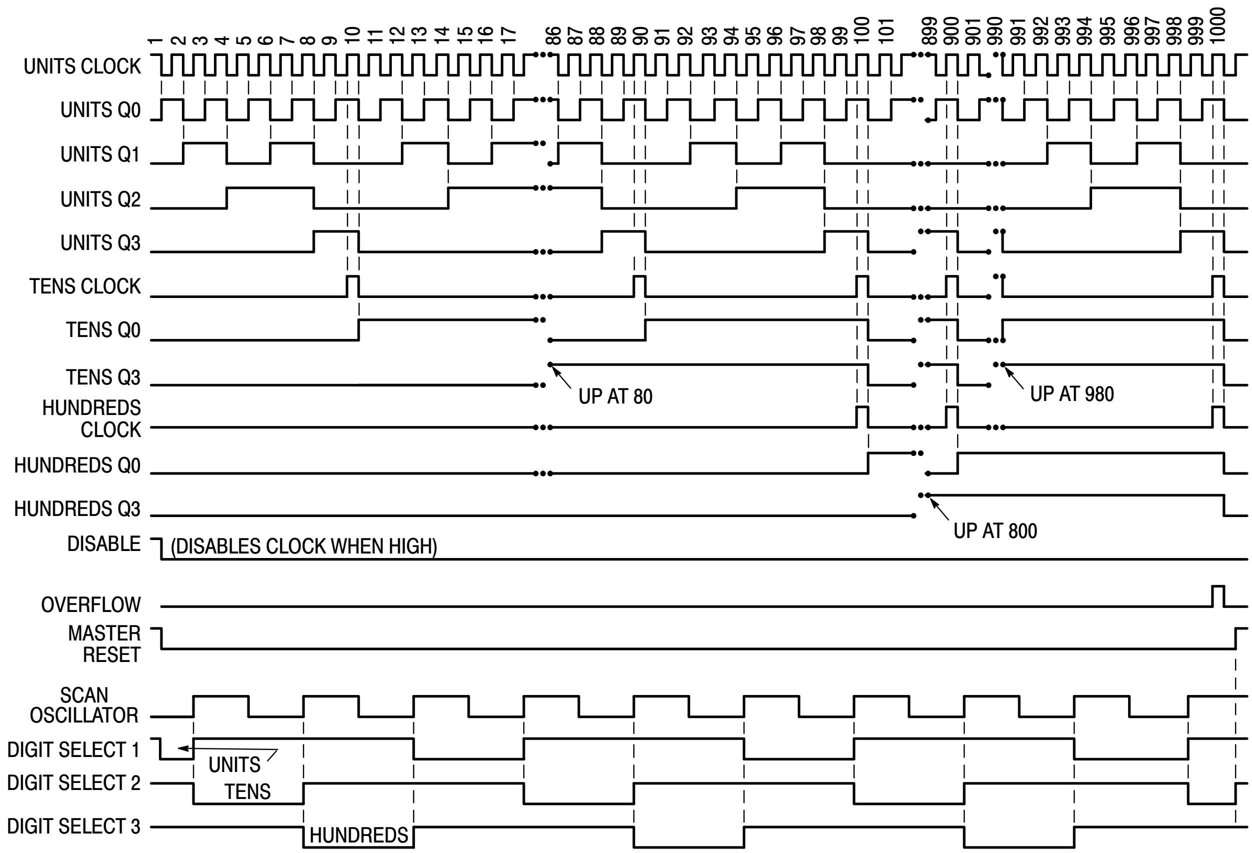


Figure 2. 3−Digit Counter Timing Diagram (Reference Figure 4)

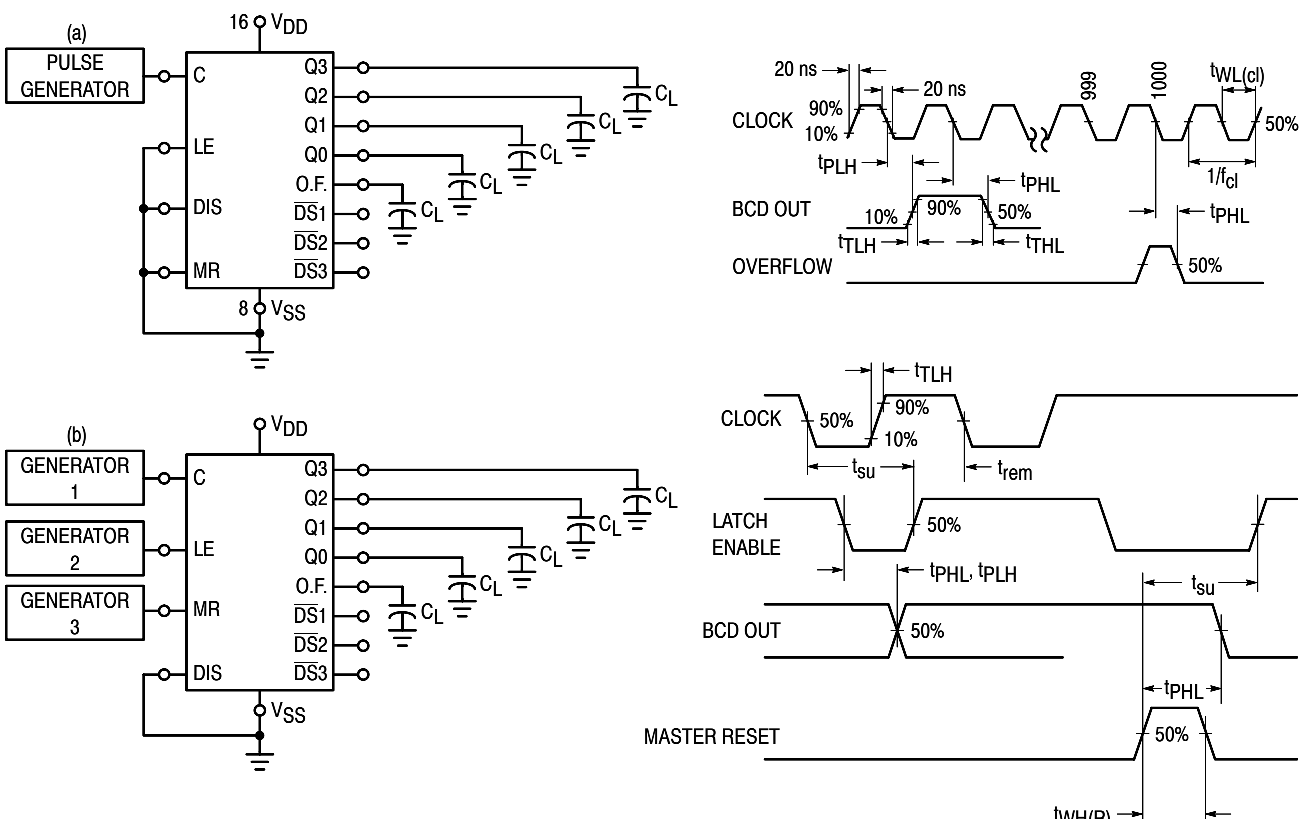


Figure 3. Switching Time Test Circuits and Waveforms

OPERATING CHARACTERISTICS

The MC14553B three−digit counter, shown in Figure 4, consists of three negative edge−triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on−chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

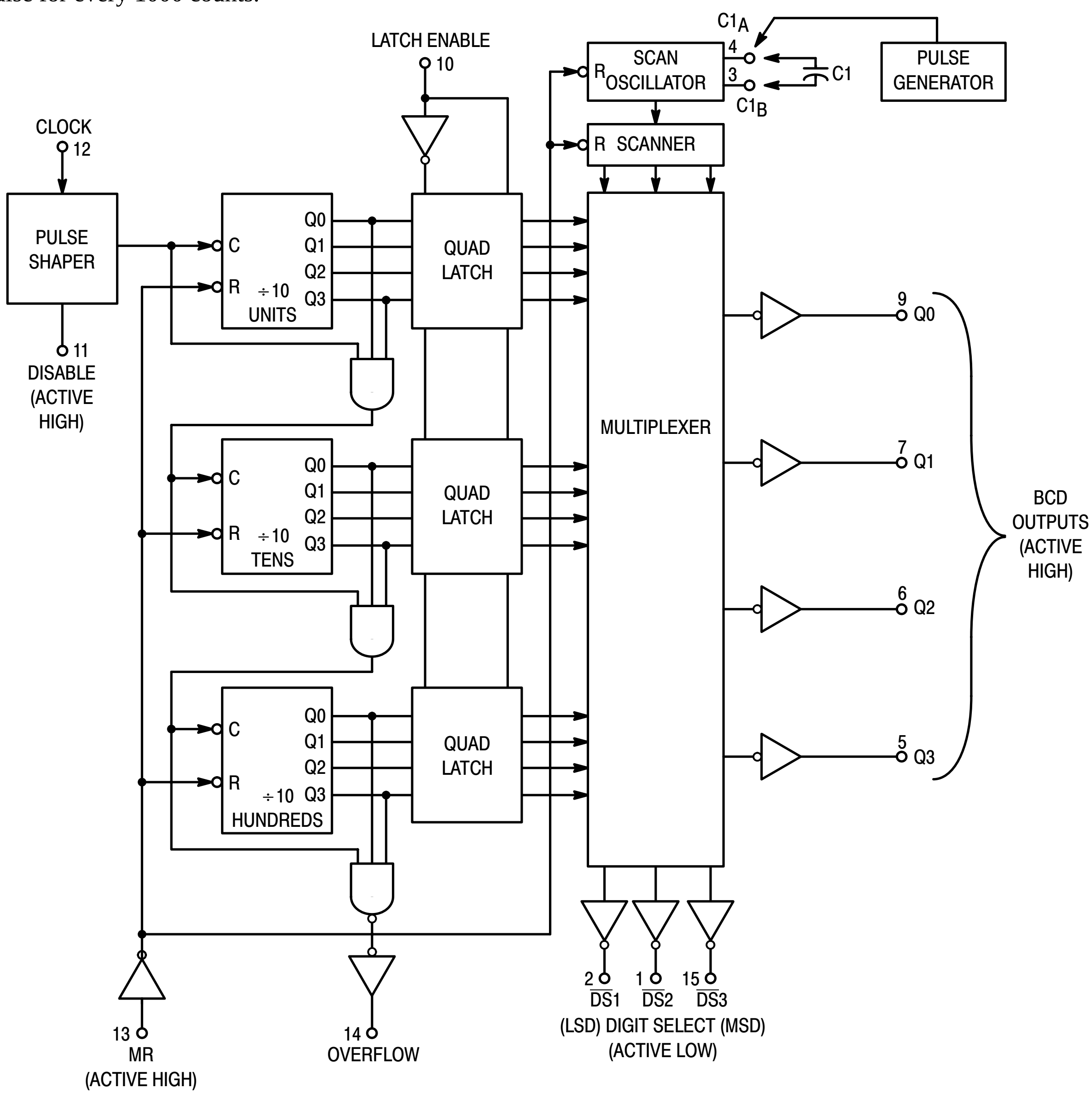


Figure 4. Expanded Block Diagram

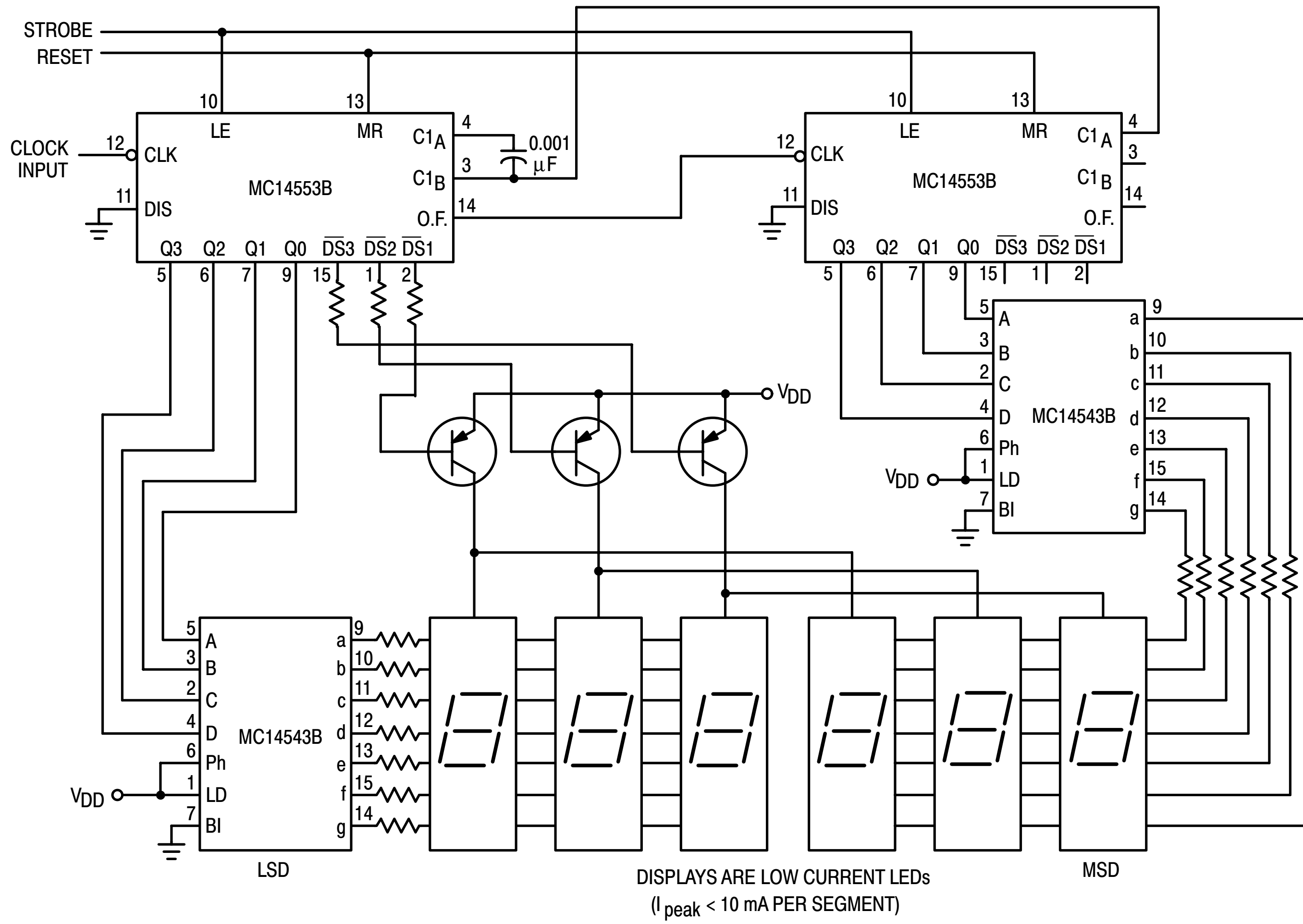


Figure 5. Six–Digit Display

MC14555B, MC14556B

Dual Binary to 1-of-4 Decoder/Demultiplexer

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the “high” state, and the MC14556B has the selected output go to the “low” state. Expanded decoding such as binary−to−hexadecimal (1−of−16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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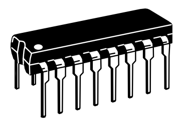
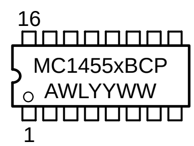
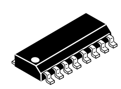
MARKING DIAGRAMS

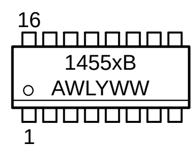


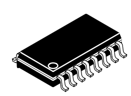
PDIP−16
P SUFFIX
CASE 648



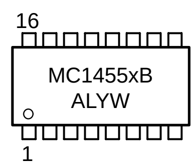


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



x	=	Specific Device Code
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

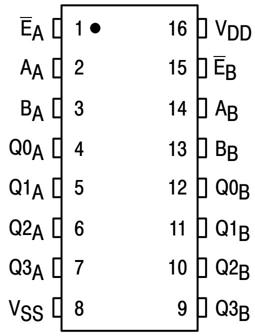
ORDERING INFORMATION

Device	Package	Shipping
MC14555BCP	PDIP−16	2000/Box
MC14555BD	SOIC−16	48/Rail
MC14555BDR2	SOIC−16	2500/Tape & Reel
MC14555BF	SOEIAJ−16	See Note 1
MC14555BFEL	SOEIAJ−16	See Note 1
MC14556BCP	PDIP−16	2000/Box
MC14556BD	SOIC−16	48/Rail
MC14556BDR2	SOIC−16	2500/Tape & Reel
MC14556BF	SOEIAJ−16	See Note 1
MC14556BFEL	SOEIAJ−16	See Note 1

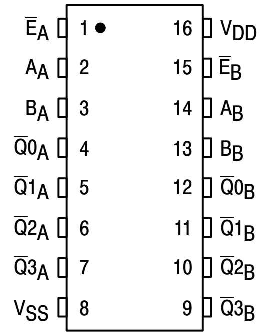
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENTS

MC14555B



MC14556B

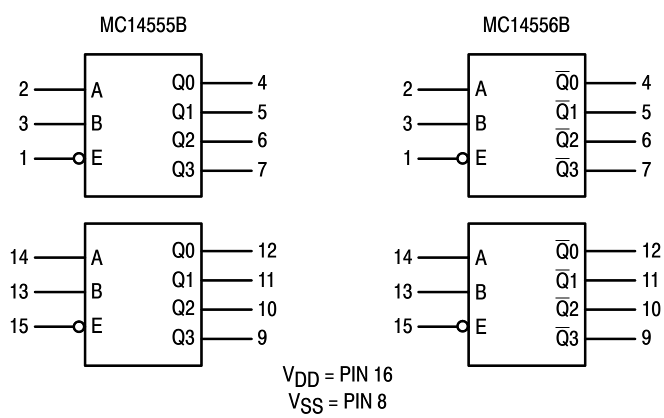


TRUTH TABLE

Inputs			Outputs							
Enable	Select		MC14555B				MC14556B			
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	– – – –	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	– – – –	– 1.7 – 0.36 – 0.9 – 2.4	– – – –	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μAdc
Total Supply Current (5) (6) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.85 μA/kHz) f + I_{DD} I_T = (1.70 μA/kHz) f + I_{DD} I_T = (2.60 μA/kHz) f + I_{DD}							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (7) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time − A, B to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	190	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Propagation Delay Time − E to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	–	85	170	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	130	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

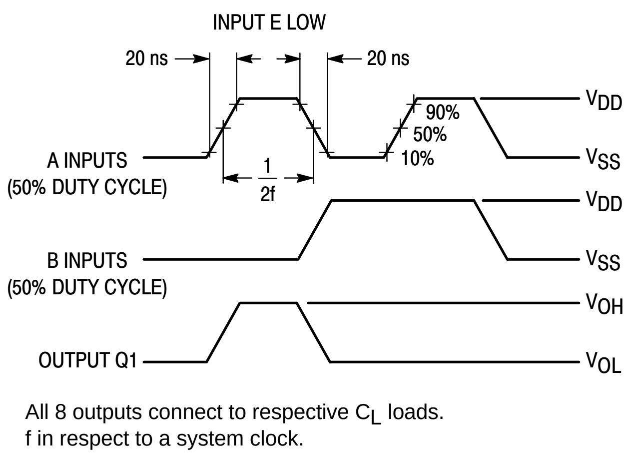


Figure 1. Dynamic Power Dissipation Signal Waveforms

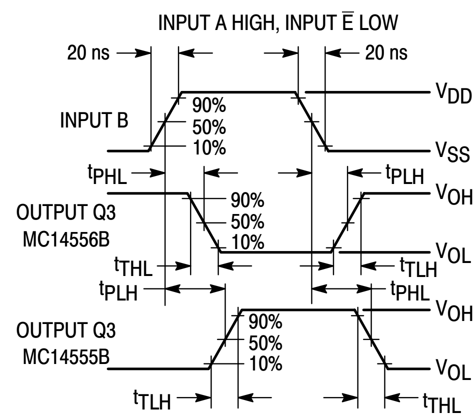
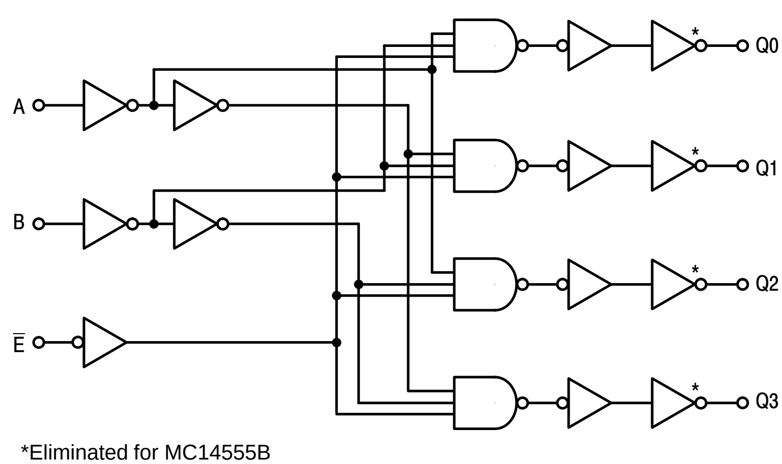


Figure 2. Dynamic Signal Waveforms

LOGIC DIAGRAM
(1/2 of Dual)



MC14557B

1-to-64 Bit Variable Length Shift Register

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1−64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or one Low−power Schottky TTL Load Over the Rated Temperature Range
- Pb−Free Packages are Available

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
2. Temperature Derating: Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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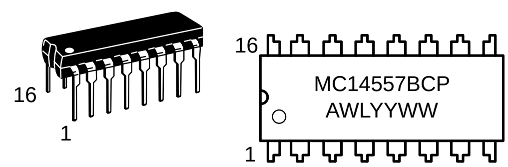
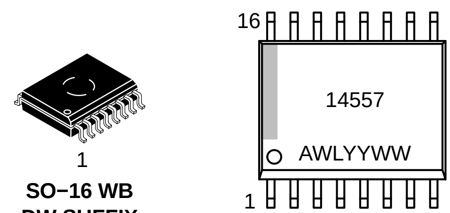
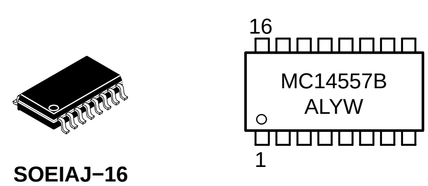
MARKING DIAGRAMS



PDIP−16
P SUFFIX
CASE 648



SO−16 WB
DW SUFFIX
CASE 751G



SOEIAJ−16
F SUFFIX
CASE 966

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 391 of this data sheet.

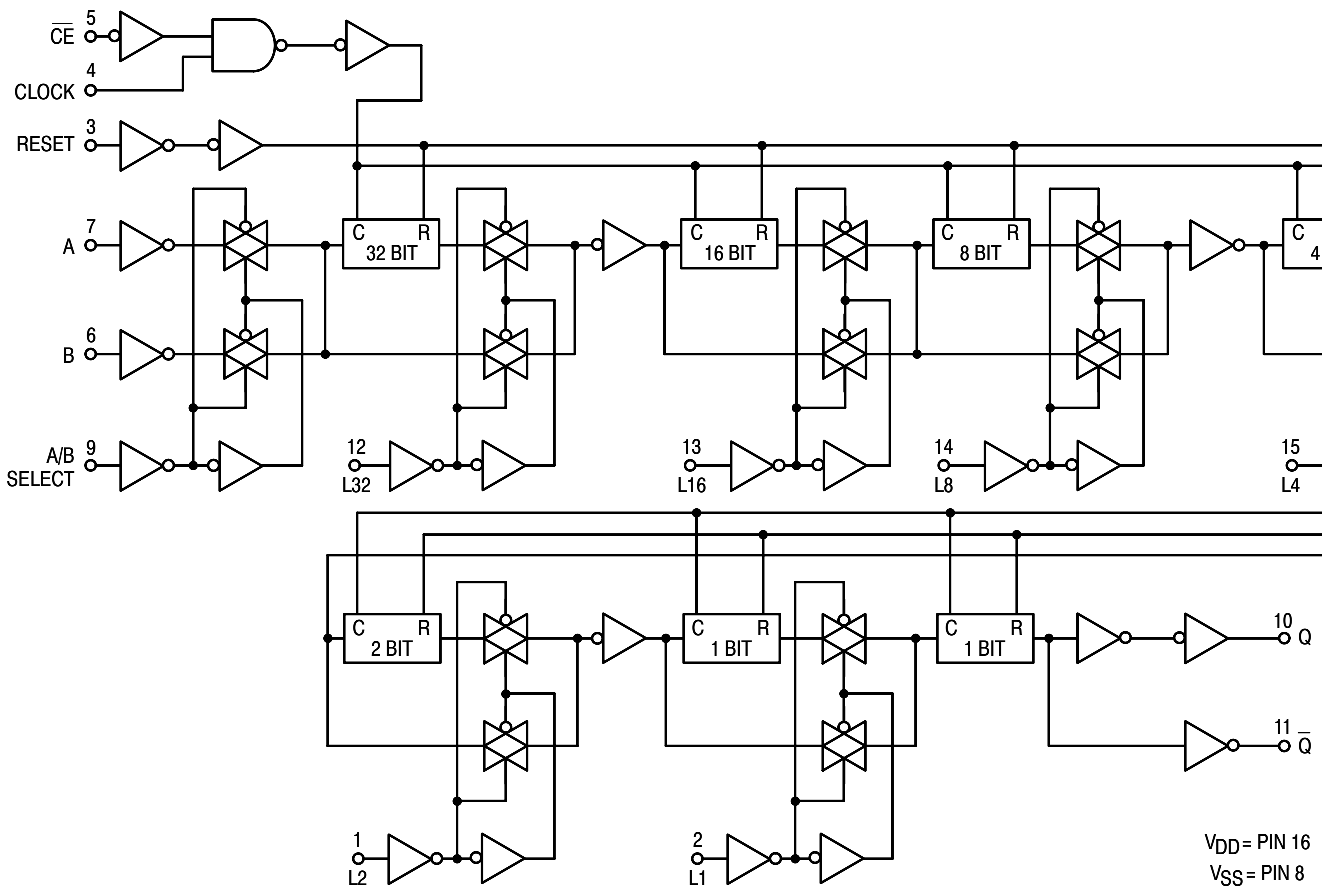


Figure 1. Logic Diagram

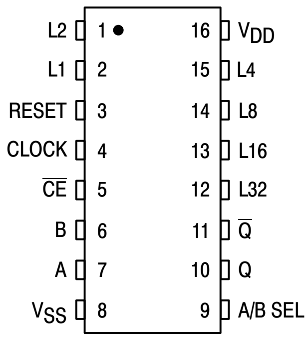


Figure 2. Pin Assignment

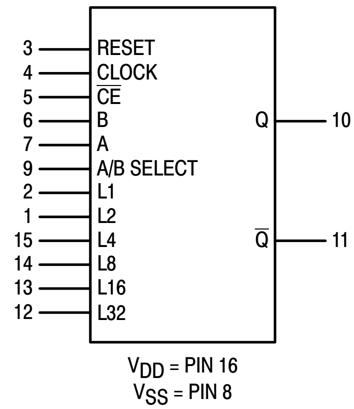


Figure 3. Block Diagram

TRUTH TABLE

Inputs				Output
Rst	A/B	Clock	$\overline{CE}$	Q
0	0	↑	0	B
0	1	↑	0	A
0	0	1	↓	B
0	1	1	↓	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1 Bit
0	0	0	0	0	1	2 Bits
0	0	0	0	1	0	3 Bits
0	0	0	0	1	1	4 Bits
0	0	0	1	0	0	5 Bits
0	0	0	1	0	1	6 Bits
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34 Bits
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	1	1	0	0	61 Bits
1	1	1	1	0	1	62 Bits
1	1	1	1	1	0	63 Bits
1	1	1	1	1	1	64 Bits

NOTE: Length equals the sum of the binary length control subscripts plus one.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic		V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 3)	25°C Max	125°C Min	125°C Max	Unit
V_{OL}	Output Voltage V_{in} = V_{DD} or 0	“0” Level	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{OH}	V_{in} = 0 or V_{DD}	“1” Level	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
V_{IL}	Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	“0” Level	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
V_{IH}	(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	“1” Level	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	5.0 5.0 10 15	–3.0 –0.64 –1.6 –4.2	– – – –	–2.4 –0.51 –1.3 –3.4	–4.2 –0.88 –2.25 –8.8	– – – –	–1.7 –0.36 –0.9 –2.4	– – – –	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	
I_{in}	Input Current		15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
C_{in}	Input Capacitance (V_{in} = 0)		–	–	–	–	5.0	7.5	–	–	pF
I_{DD}	Quiescent Current (Per Package)		5.0 10 15	– – –	5.0 10 20	– – –	0.010 0.020 0.030	5.0 10 20	– – –	150 300 600	µAdc
I_T	Total Supply Current (Notes 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		5.0 10 15	I_T = (1.75 µA/kHz) f + I_{DD} I_T = (3.50 µA/kHz) f + I_{DD} I_T = (5.25 µA/kHz) f + I_{DD}							µAdc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)$ Vfk where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Min	Typ (Note 7)	Max	Unit
t_{TLH}, t_{THL}	Rise and Fall Time, Q or $\overline{Q}$ Output					ns
	t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	5	–	100	200	
	t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns	10	–	50	100	
	t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	15	–	40	80	
t_{PLH}, t_{PHL}	Propagation Delay, Clock or $\overline{CE}$ to Q or $\overline{Q}$					ns
	t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	5	–	300	600	
	t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns	10	–	130	260	
	t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns	15	–	90	180	
t_{PLH}, t_{PHL}	Propagation Delay, Reset to Q or $\overline{Q}$					ns
	t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	5	–	300	600	
	t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns	10	–	130	260	
	t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 70 ns	15	–	95	190	
$t_{WH(cl)}$	Pulse Width, Clock	5	200	95	–	ns
		10	100	45	–	
		15	75	35	–	
$t_{WH(rst)}$	Pulse Width, Reset	5	300	150	–	ns
		10	140	70	–	
		15	100	50	–	
f_{cl}	Clock Frequency (50% Duty Cycle)	5	–	3.0	1.7	MHz
		10	–	7.5	5.0	
		15	–	13.0	6.7	
t_{su}	Setup Time, A or B to Clock or $\overline{CE}$					ns
	Worst case condition: L1 = L2 = L4 = L8 =	5	700	350	–	
	L16 = L32 = V_{SS} (Register Length = 1)	10	290	130	–	
		15	145	85	–	
	Best case condition: L32 = V_{DD}, L1 through L16 =	5	400	45	–	
	Don't Care (Any register length from 33 to 64)	10	165	5	–	
		15	60	0	–	
t_h	Hold Time, Clock or $\overline{CE}$ to A or B					ns
	Best case condition: L1 = L2 = L4 = L8 = L16 =	5	200	–150	–	
	L32 = V_{SS} (Register Length = 1)	10	100	–60	–	
		15	10	–50	–	
	Worst case condition: L32 = V_{DD}, L1 through L16 =	5	400	50	–	
	Don't Care (Any register length from 33 to 64)	10	185	25	–	
		15	85	22	–	
t_r, t_f	Rise and Fall Time, Clock	5				–
		10		No Limit		
		15				
t_r, t_f	Rise and Fall Time, Reset or $\overline{CE}$	5	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
t_{rem}	Removal Time, Reset to Clock or $\overline{CE}$	5	160	80	–	ns
		10	80	40	–	
		15	70	35	–	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

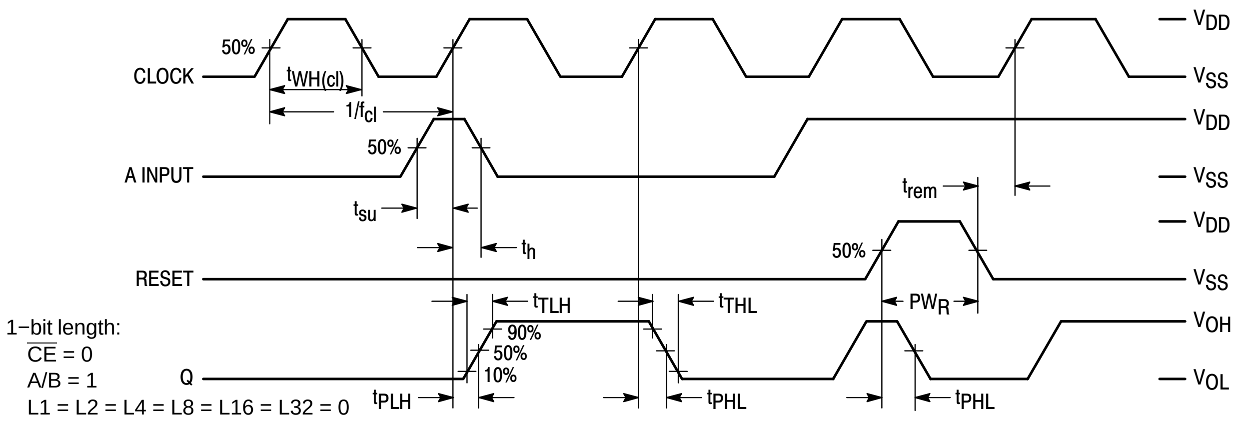


Figure 4. Timing Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC14557BF	SOEIAJ−16 (Pb−Free)	50 Units / Rail
MC14557BCP	PDIP−16	500 Units / Rail
MC14557BFEL	SOEIAJ−16 (Pb−Free)	2000 / Tape & Reel
MC14557BDWR2	SO−16 (WB)	1000 / Tape & Reel
MC14557BCPG	PDIP−16 (Pb−Free)	500 Units / Rail
MC14557BDW	SO−16 (WB)	47 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC1455, MC1455B, NCV1455B

Timers

The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode, time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free−running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally ON or Normally OFF Output

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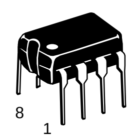
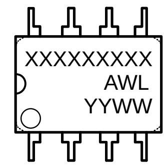
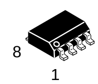
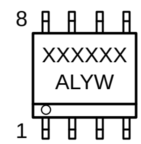
MARKING DIAGRAMS





P1 SUFFIX
PLASTIC PACKAGE
CASE 626



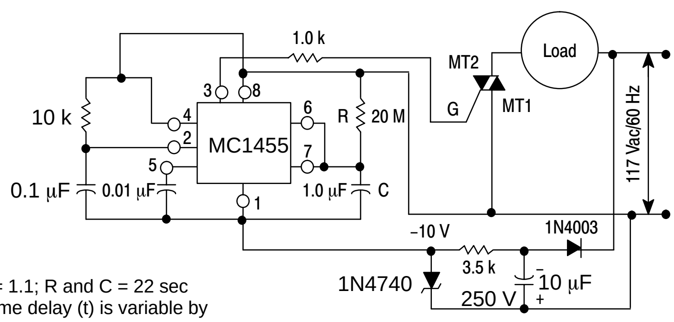


D SUFFIX
PLASTIC PACKAGE
CASE 751

xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page ___ of this data sheet.
(Create − Named − OrderingInfoText.)



t = 1.1; R and C = 22 sec
Time delay (t) is variable by changing R and C (see Figure 16).

Figure 1. 22 Second Solid State Time Delay Relay Circuit

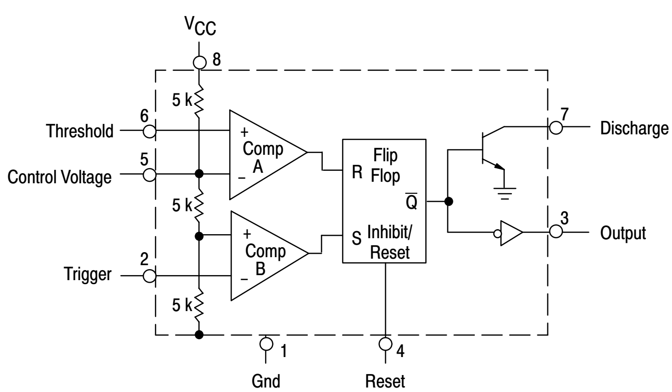
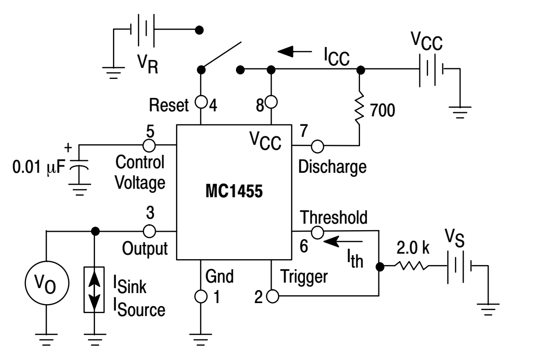


Figure 2. Representative Block Diagram



Test circuit for measuring DC parameters (to set output and measure parameters):
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, Pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V_{CC}.

Figure 3. General Test Circuit

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation) P1 Suffix, Plastic Package Derate above T_A = +25°C D Suffix, Plastic Package Derate above T_A = +25°C	P_D P_D	625 5.0 625 160	mW mW/°C mW °C/W
Operating Temperature Range (Ambient) MC1455B MC1455 NCV1455B	T_A	−40 to +85 0 to +70 −40 to +125	°C
Maximum Operating Die Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	4.5	–	16	V
Supply Current V_{CC} = 5.0 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞, Low State (Note 1)	I_{CC}	– –	3.0 10	6.0 15	mA
Timing Error (R = 1.0 kΩ to 100 kΩ) (Note 2) Initial Accuracy C = 0.1 μF Drift with Temperature Drift with Supply Voltage		– – –	1.0 50 0.1	– – –	% PPM/°C %/V
Threshold Voltage/Supply Voltage	V_{th}/V_{CC}	–	2/3	–	
Trigger Voltage V_{CC} = 15 V V_{CC} = 5.0 V	V_T	– –	5.0 1.67	– –	V
Trigger Current	I_T	–	0.5	–	μA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	μA
Discharge Leakage Current (Pin 7)	I_{dischg}	–	–	100	nA
Control Voltage Level V_{CC} = 15 V V_{CC} = 5.0 V	V_{CL}	9.0 2.6	10 3.33	11 4.0	V
Output Voltage Low I_{Sink} = 10 mA (V_{CC} = 15 V) I_{Sink} = 50 mA (V_{CC} = 15 V) I_{Sink} = 100 mA (V_{CC} = 15 V) I_{Sink} = 200 mA (V_{CC} = 15 V) I_{Sink} = 8.0 mA (V_{CC} = 5.0 V) I_{Sink} = 5.0 mA (V_{CC} = 5.0 V)	V_{OL}	– – – – – –	0.1 0.4 2.0 2.5 – 0.25	0.25 0.75 2.5 – – 0.35	V
Output Voltage High V_{CC} = 15 V (I_{Source} = 200 mA) V_{CC} = 15 V (I_{Source} = 100 mA) V_{CC} = 5.0 V (I_{Source} = 100 mA)	V_{OH}	– 12.75 2.75	12.5 13.3 3.3	– – –	V
Rise Time Differential Output	t_r	–	100	–	ns
Fall Time Differential Output	t_f	–	100	–	ns

1. ‘Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V Monostable mode.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 MΩ.
4. T_{low} = 0°C for MC1455, T_{low} = −40°C for MC1455B, NCV1455B
   T_{high} = +70°C for MC1455, T_{high} = +85°C for MC1455B, T_{high} = +125°C for NCV1455B
5. NCV prefix is for Automotive and other applications requiring site and change control.

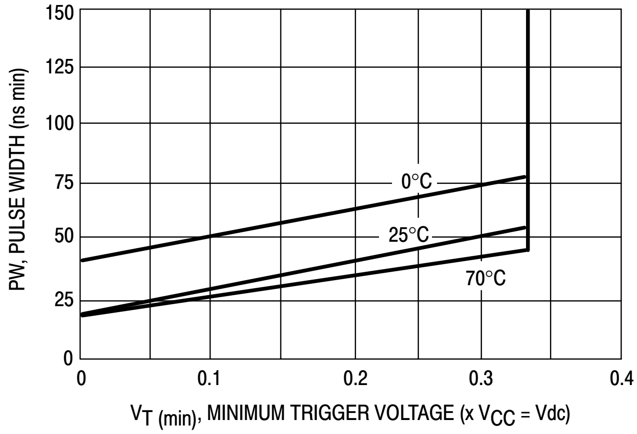


Figure 4. Trigger Pulse Width

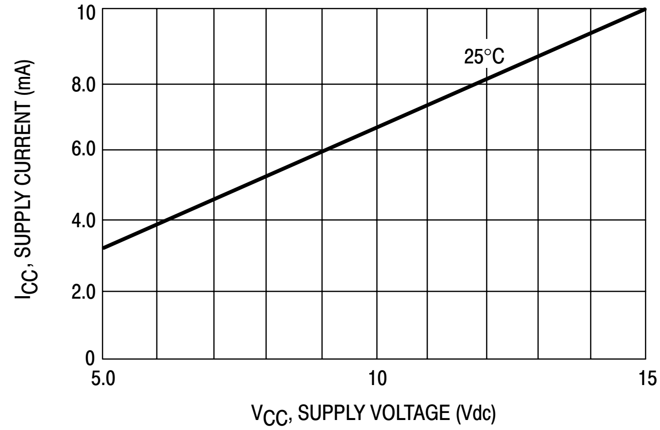


Figure 5. Supply Current

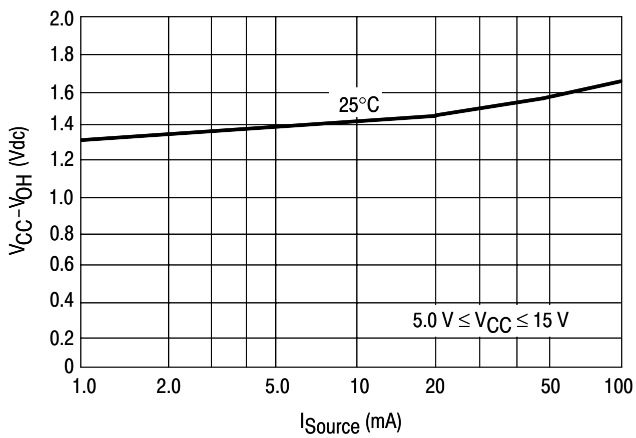


Figure 6. High Output Voltage

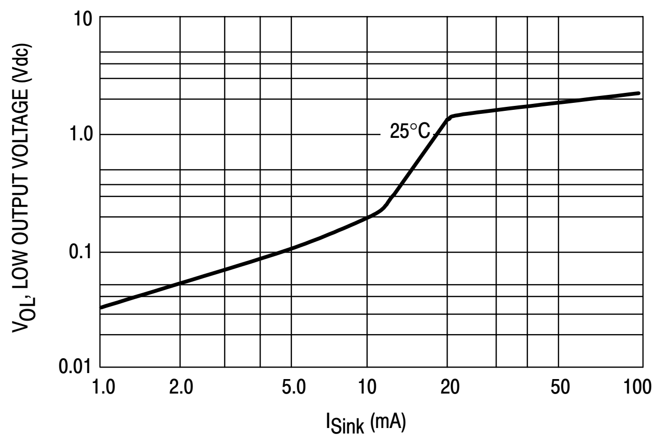


Figure 7. Low Output Voltage @ V_{CC} = 5.0 Vdc

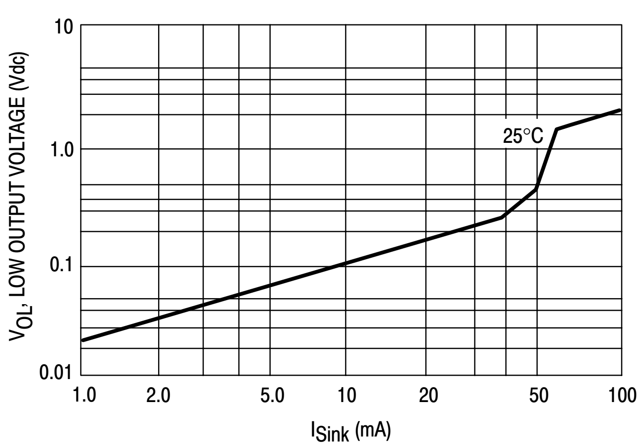


Figure 8. Low Output Voltage @ V_{CC} = 10 Vdc

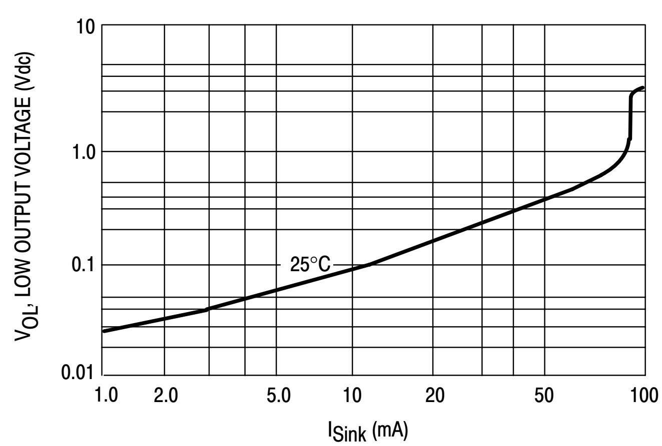


Figure 9. Low Output Voltage @ V_{CC} = 15 Vdc

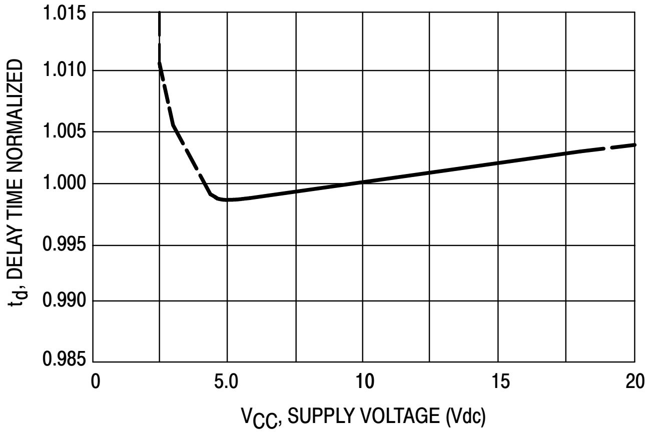


Figure 10. Delay Time versus Supply Voltage

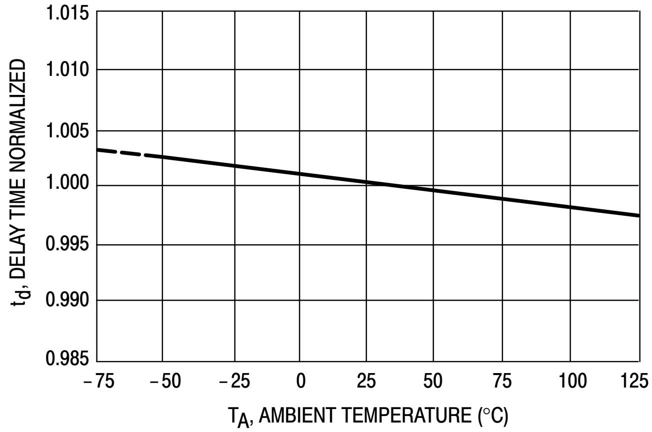


Figure 11. Delay Time versus Temperature

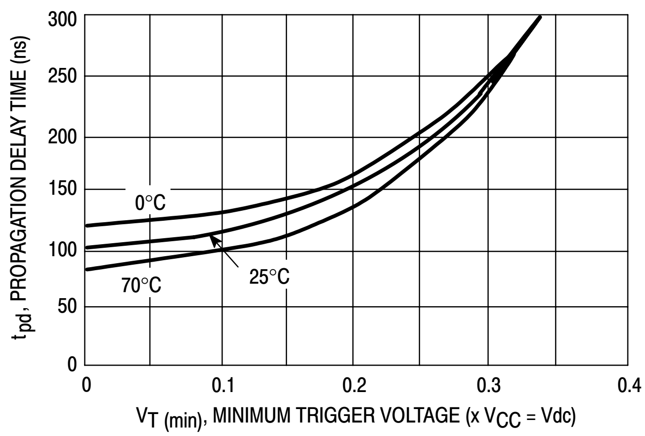


Figure 12. Propagation Delay versus Trigger Voltage

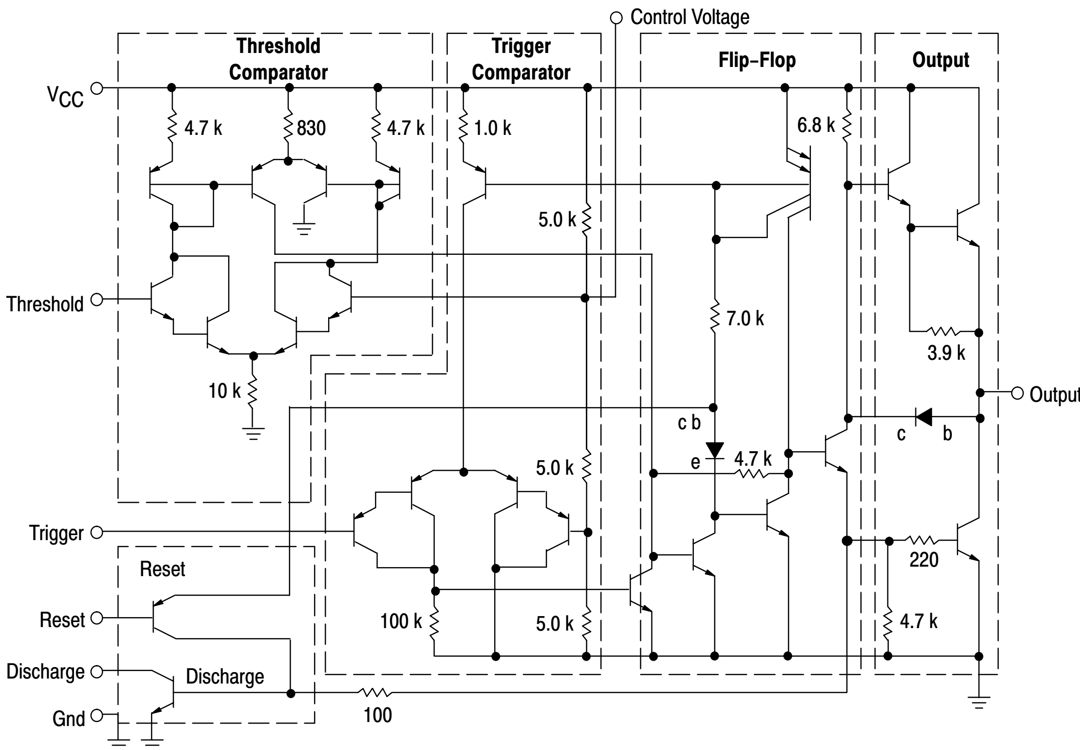


Figure 13. Representative Circuit Schematic

GENERAL OPERATION

The MC1455 is a monolithic timing circuit which uses an external resistor − capacitor network as its timing element. It can be used in both the monostable (one−shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip−flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode (refer to circuit in Figure 14). When the input voltage to the trigger comparator falls below 1/3 V_{CC}, the comparator output triggers the flip−flop so that its output sets low. This turns the capacitor discharge transistor “off” and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC}, the threshold comparator resets the flip−flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip−flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor, thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned “on” and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

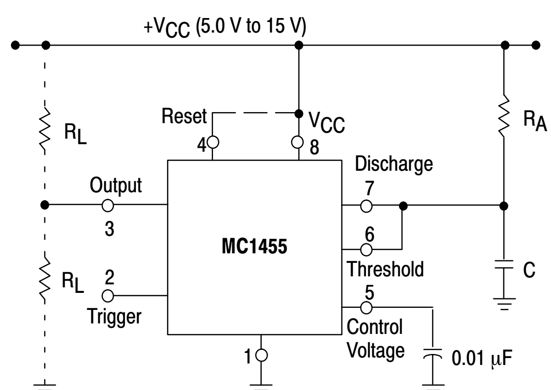
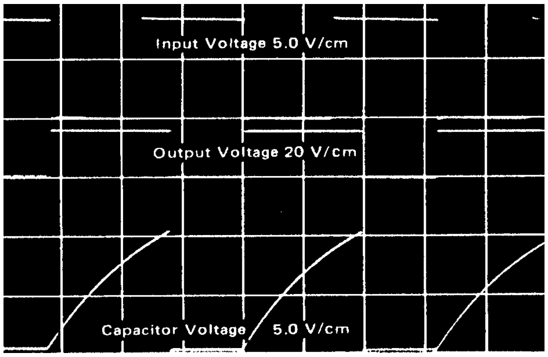


Figure 14. Monostable Circuit



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

Figure 15. Monostable Waveforms

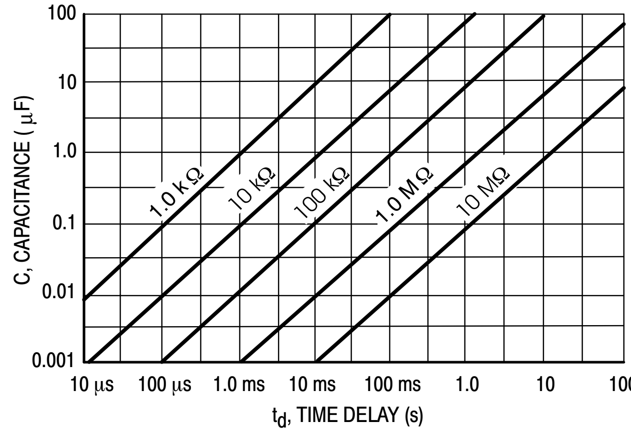


Figure 16. Time Delay

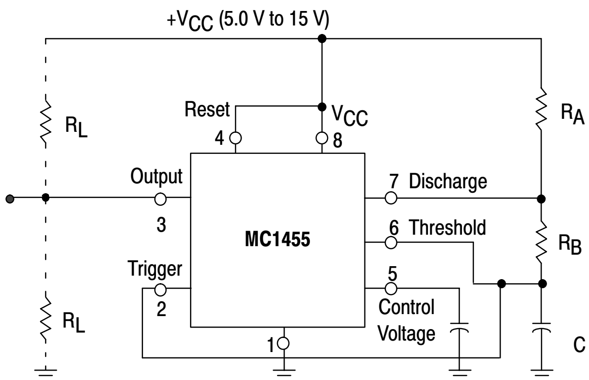
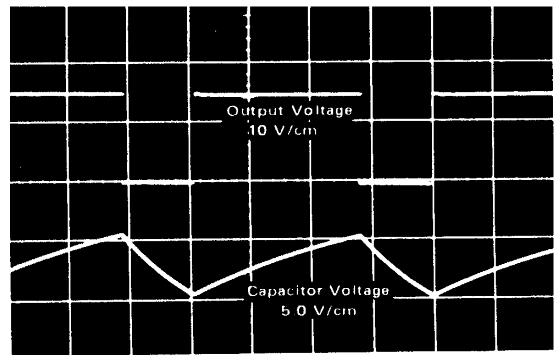


Figure 17. Astable Circuit



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ; R_B = 3.9 kΩ, V_{CC} = 15 V)

Figure 18. Astable Waveforms

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor changes to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.695(R_A + R_B)C$$

The discharge time (output low) is given by:

$$t_2 = 0.695(R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695(R_A + 2R_B)C$$

The frequency of oscillation is then: $$f = \frac{1}{1} = \frac{1.44}{(R_A + 2R_B)C}$$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $$DC = \frac{R_B}{R_A + 2R_B}$$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}(Vdc)}{I7\ (A)} \geq \frac{V_{CC}(Vdc)}{0.2}$$

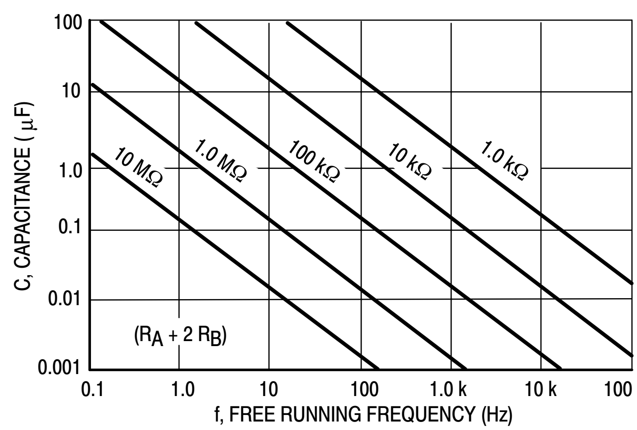


Figure 19. Free Running Frequency

APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 V_{CC} to 2/3 V_{CC}. The linear ramp time is given by:

$$t = \frac{2}{3}\,\frac{V_{CC}}{I}, \quad \text{where } I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$$

If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

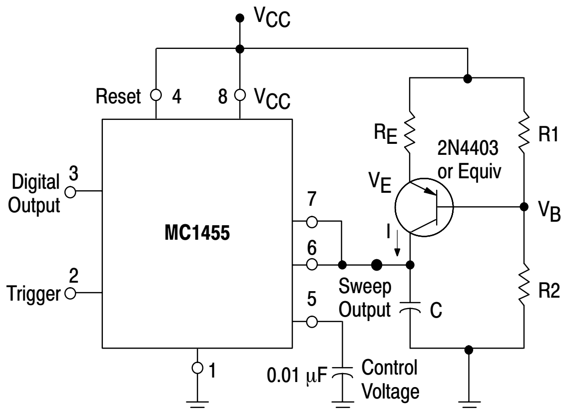


Figure 20. Linear Voltage Sweep Circuit

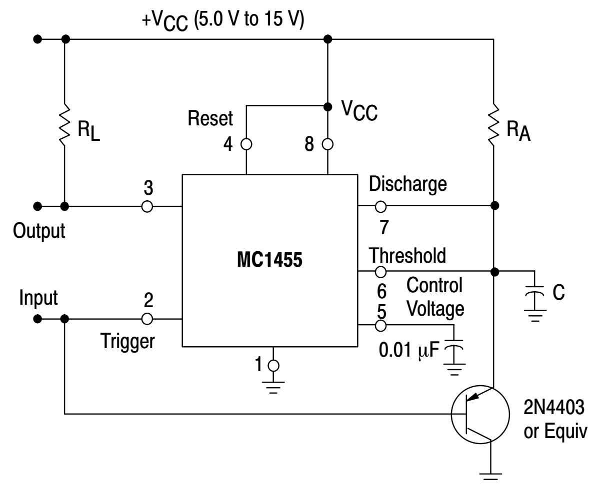
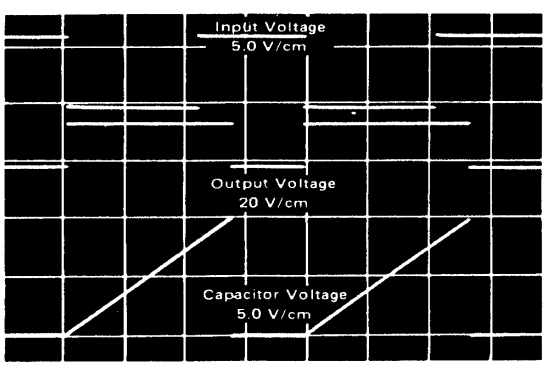


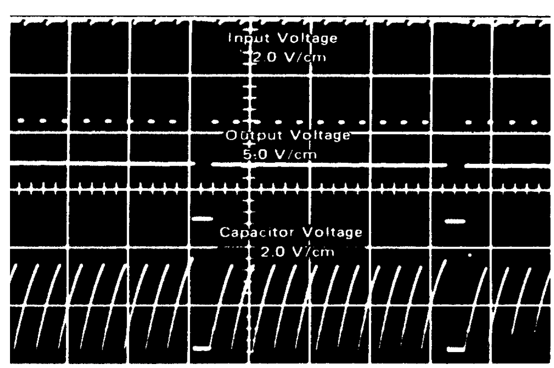
Figure 21. Missing Pulse Detector



t = 100 µs/cm

(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Figure 22. Linear Voltage Ramp Waveforms



t = 500 µs/cm

(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Figure 23. Missing Pulse Detector Waveforms

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

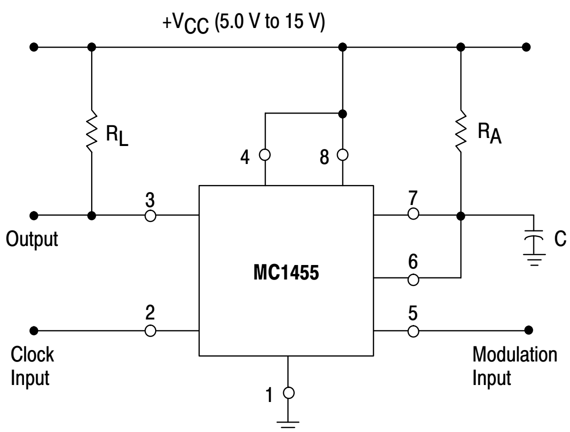
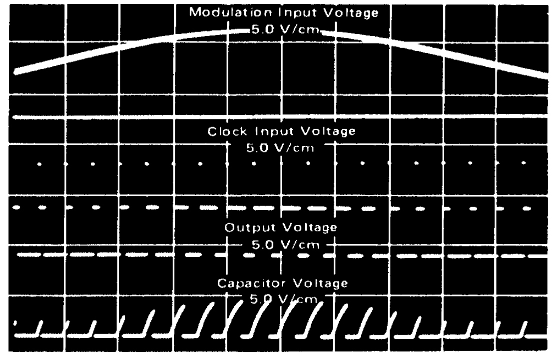


Figure 24. Pulse Width Modulator



t = 0.5 ms/cm

(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)

Figure 25. Pulse Width Modulation Waveforms

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

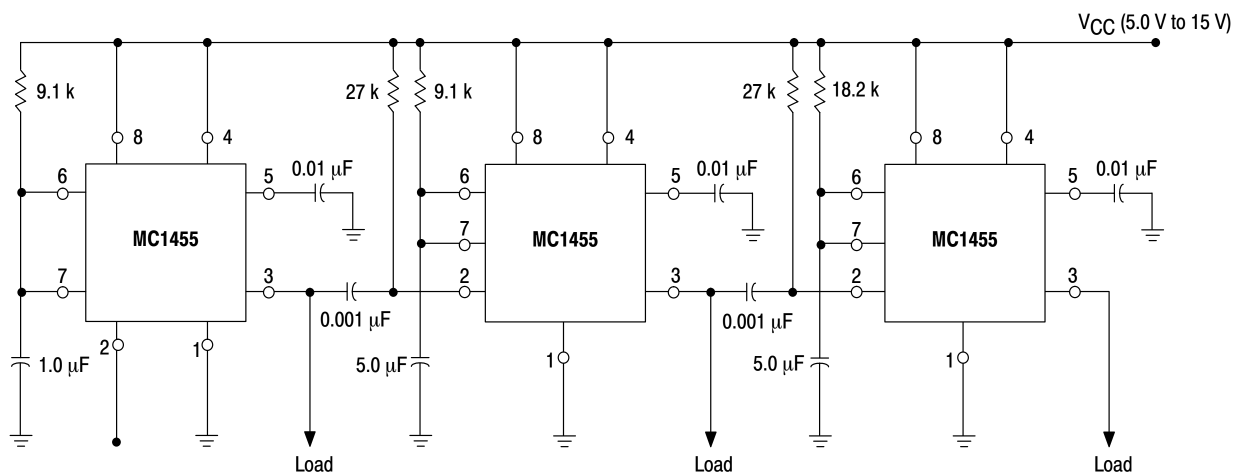


Figure 26. Sequential Timer

DEVICE ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
MC1455P1	T_A = 0°C to +70°C	Plastic Dip	50 Units/Rail
MC1455D	T_A = 0°C to +70°C	SO−8	98 Units/Rail
MC1455BD	T_A = −40°C to +85°C	SO−8	98 Units/Rail
MC1455BP1	T_A = −40°C to +85°C	Plastic Dip	50 Units/Rail
NCV1455BDR2*	T_A = −40°C to +125°C	SO−8	2500/Tape & Rail

*NCV prefix is for automotive and other applications requiring site and control changes.

MC14562B

128-Bit Static Shift Register

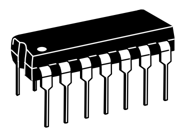
The MC14562B is a 128−bit static shift register constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Fully Static Operation
- Cascadable to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range

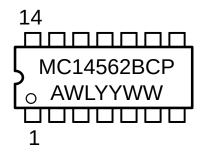
ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS



PDIP−14
P SUFFIX
CASE 646



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

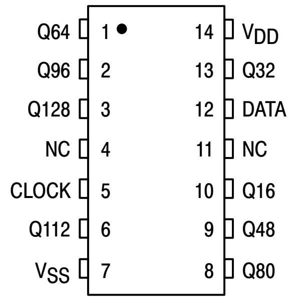
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

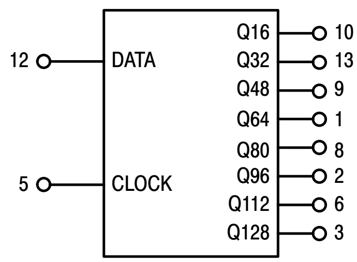
Device	Package	Shipping
MC14562BCP	PDIP−14	25/Rail

PIN ASSIGNMENT



NC = NO CONNECTION

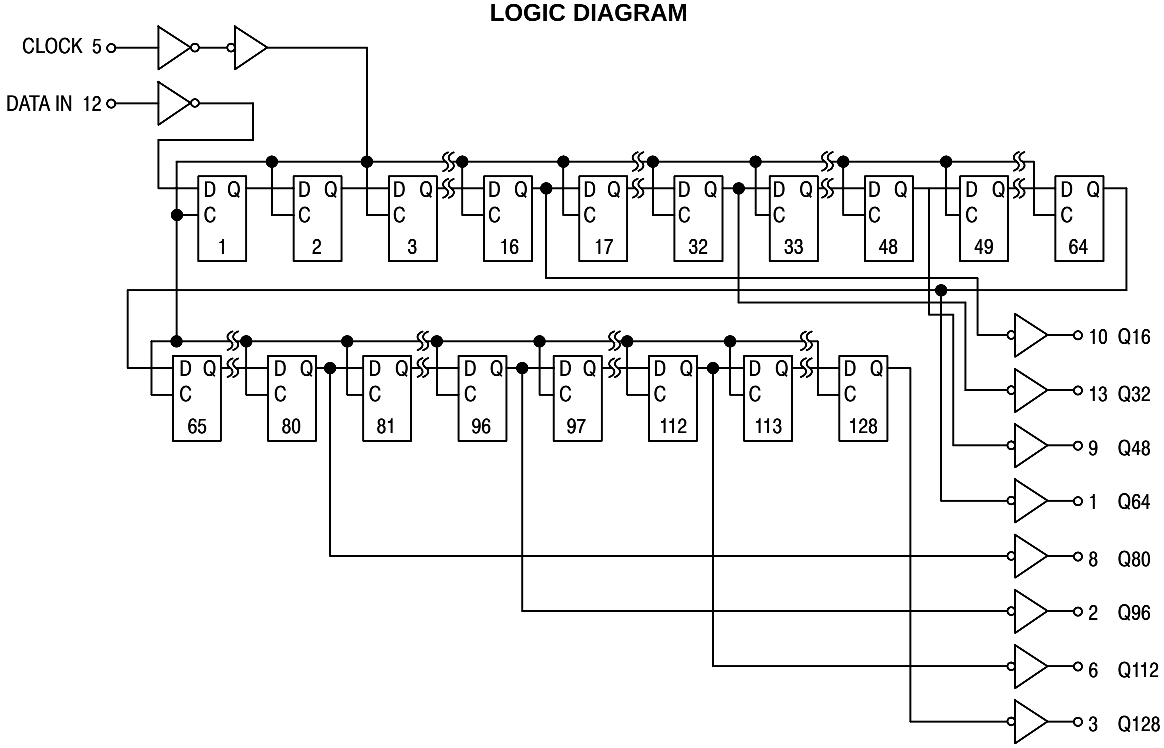
BLOCK DIAGRAM



Pins 4 and 11 not used.

V_{DD} = PIN 14
V_{SS} = PIN 7

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 05 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.010 0.020 0.030	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.94 µA/kHz) f + I_{DD} I_T = (3.81 µA/kHz) f + I_{DD} I_T = (5.52 µA/kHz) f + I_{DD}							µAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (7.)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time Clock to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 515 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 600 250 170	 1200 500 340	ns
Clock Pulse Width (50% Duty Cycle)	t_{WH}	5.0 10 15	600 220 150	300 110 75	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	1.9 5.6 8.0	1.1 3.0 4.0	MHz
Data to Clock Setup Time	$t_{su(1)}$	5.0 10 15	– 20 – 10 0	– 170 – 64 – 60	— — —	ns
	$t_{su(0)}$	5.0 10 15	– 20 – 10 0	– 91 – 58 – 48	— — —	ns
Data to Clock Hold Time	$t_{h(1)}$	5.0 10 15	350 165 155	263 109 100	— — —	ns
	$t_{h(0)}$	5.0 10 15	350 200 140	267 140 93	— — —	ns
Clock Input Rise and Fall Times	t_r, t_f	5.0 10 15	— — —	— — —	15 5 4	µs

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

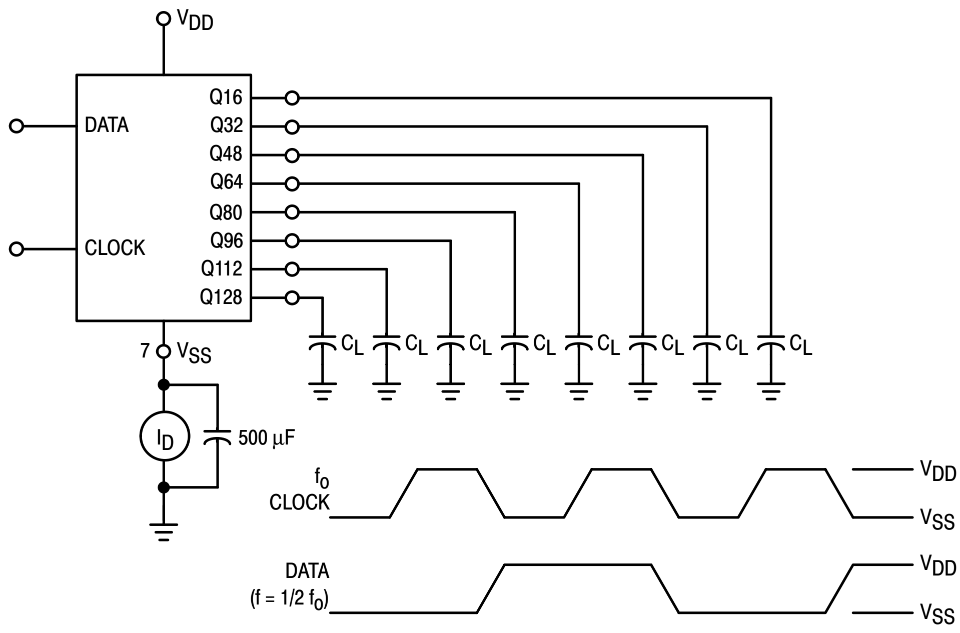
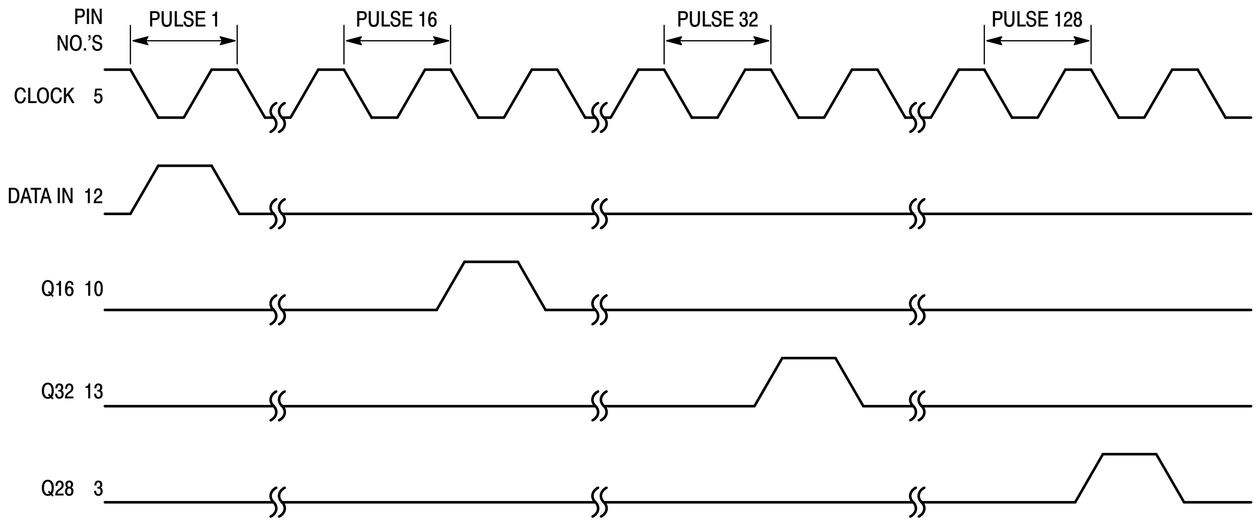
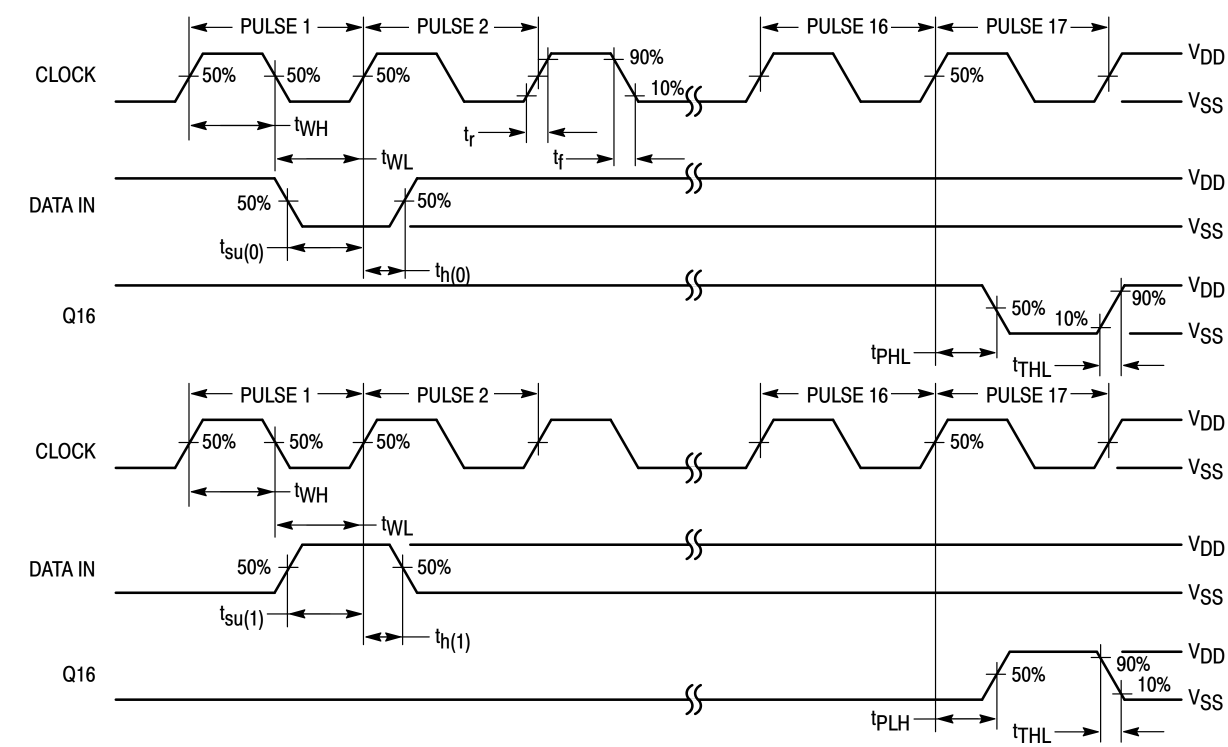


Figure 1. Power Dissipation Test Circuit and Waveforms

TIMING DIAGRAM



AC TEST WAVEFORMS



NOTE: The remaining Data−Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

MC14569B

Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

ON Semiconductor

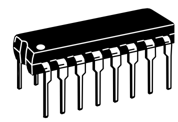
http://onsemi.com

The MC14569B is a programmable divide−by−N dual 4−bit binary or BCD down counter constructed with MOS P−channel and N−channel enhancement mode devices (complementary MOS) in a monolithic structure.

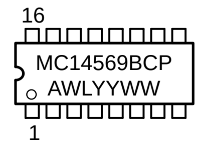
This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase−locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

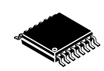
- Speed−up Circuitry for Zero Detection
- Each 4−Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

MARKING DIAGRAMS

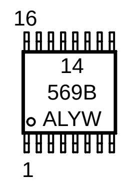


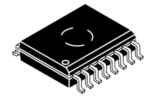
PDIP−16
P SUFFIX
CASE 648



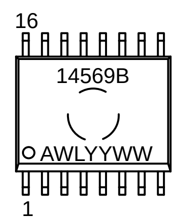


TSSOP−16
DT SUFFIX
CASE 948F





SOIC−16
DW SUFFIX
CASE 751G



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14569BCP	PDIP−16	2000/Box
MC14569BDT	TSSOP−16	96/Rail
MC14569BDW	SOIC−16	47/Rail
MC14569BDWR2	SOIC−16	1000/Tape & Reel

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

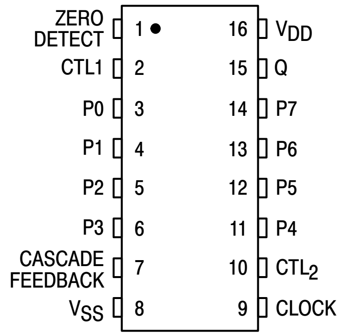
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

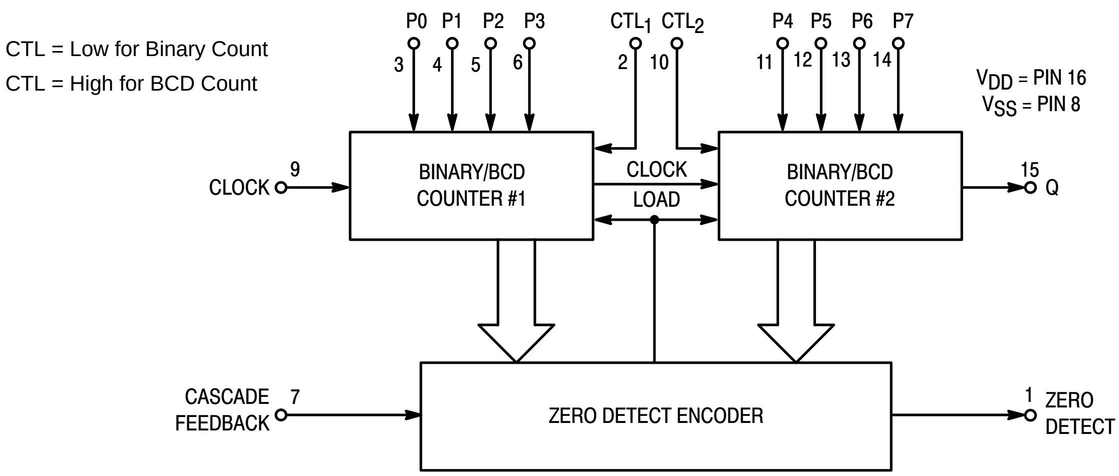
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	 5.0 10 15	 — — —	 1.5 3.0 4.0	 — — —	 2.25 4.50 6.75	 1.5 3.0 4.0	 — — —	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	 5.0 5.0 10 15	 – 3.0 – 0.64 – 1.6 – 4.2	 — — — —	 – 2.4 – 0.51 – 1.3 – 3.4	 – 4.2 – 0.88 – 2.25 – 8.8	 — — — —	 – 1.7 – 0.36 – 0.9 – 2.4	 — — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.58 µA/kHz) f + I_{DD} I_T = (1.20 µA/kHz) f + I_{DD} I_T = (1.95 µA/kHz) f + I_{DD}							µAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ (6.)	Max	Unit
Output Rise Time	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn−On Delay Time Zero Detect Output	t_{PLH}	5.0 10 15	— — —	420 175 125	700 300 250	ns
Q Output		5.0 10 15	— — —	675 285 200	1200 500 400	ns
Turn−Off Delay Time Zero Detect Output	t_{PHL}	5.0 10 15	— — —	380 150 100	600 300 200	ns
Q Output		5.0 10 15	— — —	530 225 155	1000 400 300	ns
Clock Pulse Width	t_{WH}	5.0 10 15	300 150 115	100 45 30	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.5 9.5 13.0	2.1 5.1 7.8	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	NO LIMIT			µs

6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

SWITCHING WAVEFORMS

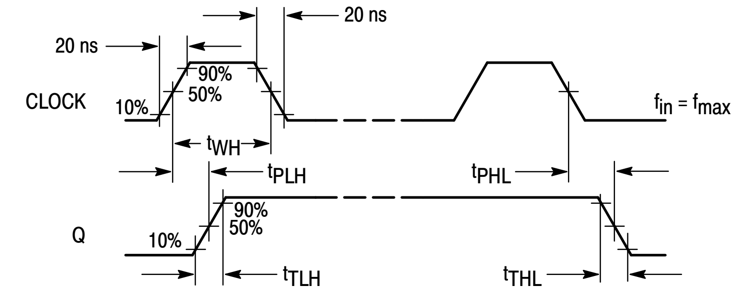


Figure 1.

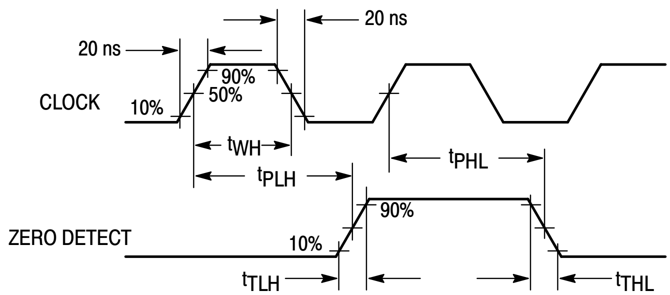


Figure 2.

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL_1 (Pin 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL_2 (Pin 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

V_{DD} (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

OPERATING CHARACTERISTICS

The MC14569B is a programmable divide−by−N dual 4−bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL_1 and CTL_2.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.

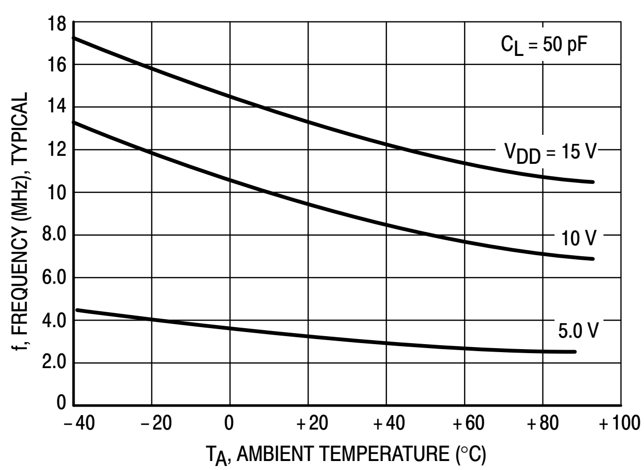


Table 1Mode Controls (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL_1	**CTL_2**	**Zero Detect**	**Q**
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

NOTE: Data Preset Inputs (P0−P7) are “Don’t Cares” while Cascade Feedback is Low.

Table 2Mode Controls (CTL_1 = Low, CTL_2 = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**Zero Detect**	**Q**	**Comments**
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
1	0	0	0	1	0	0	0	136	136	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
1	1	1	1	1	1	1	1	255	255	↓
2^7 128	2^6 64	2^5 32	2^4 16	2^3 8	2^2 4	2^1 2	2^0 1			Bit Value
Counter #2 Binary				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

Table 3Mode Controls (CTL$_1$ = High, CTL$_2$ = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**Zero Detect**	**Q**	**Comments**
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	0	0	1	19	X	
0	0	1	0	0	0	0	0	20	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	0	0	0	0	0	60	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
1	0	0	1	0	0	0	0	90	90	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
1	1	1	1	0	0	0	0	150	150	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	↓
1	1	1	1	1	0	0	1	159	159	↓
80	40	20	10	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

Table 4Mode Controls (CTL_1 = Low, CTL_2 = High, Cascade Feedback = High)

Preset Values								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	48	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active ↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	144	144	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	1	1	1	159	159	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

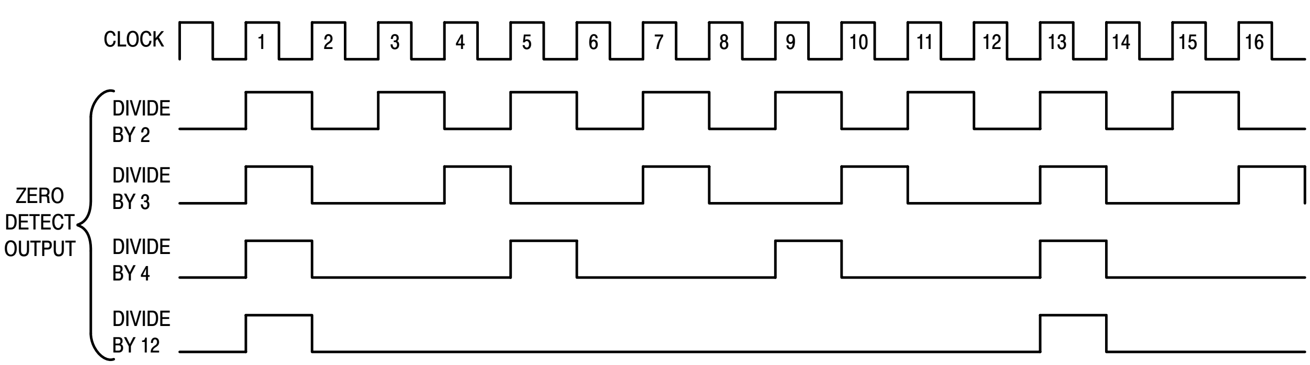
X = No Output (Always Low)

Table 5Mode Controls (CTL1 = High, CTL2 = High, Cascade Feedback = High)

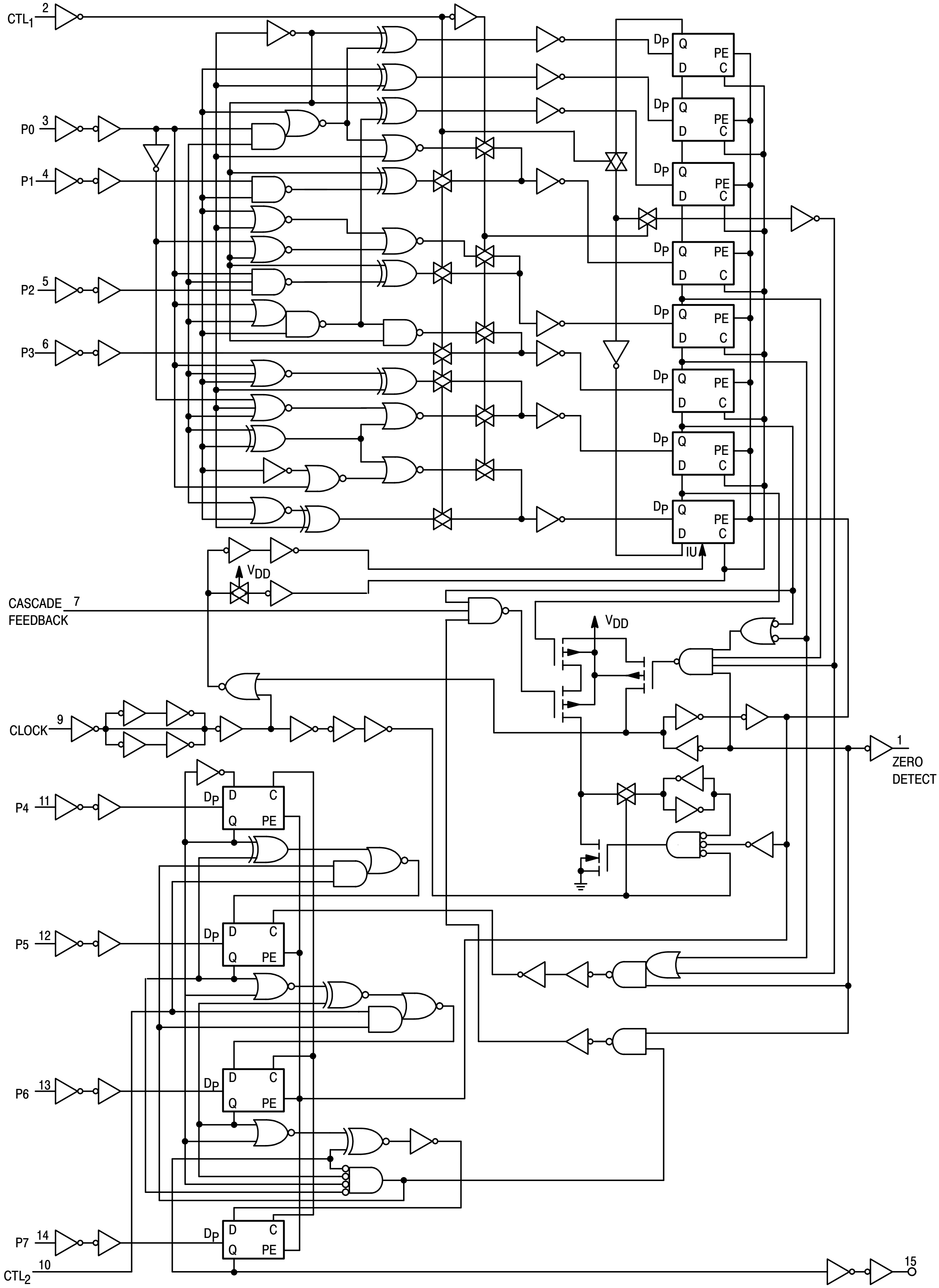
Preset Values								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	X	X	illegal state
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	0	0	1	99	99	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

TIMING DIAGRAM MC14569B



LOGIC DIAGRAM



TYPICAL APPLICATIONS

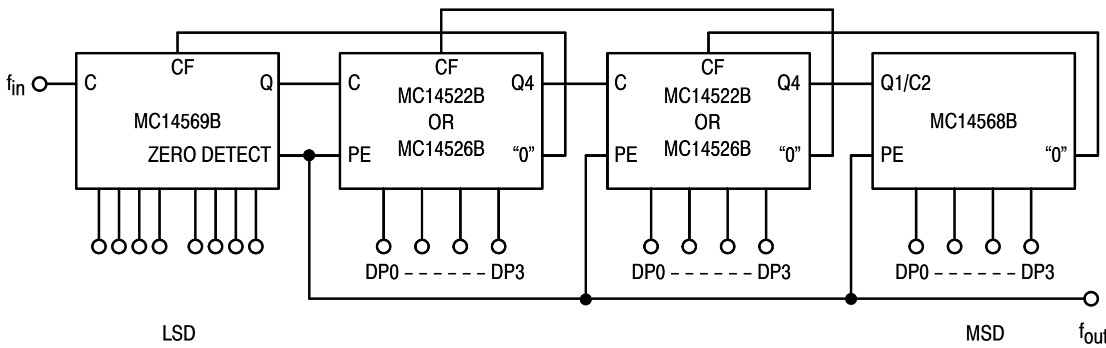


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

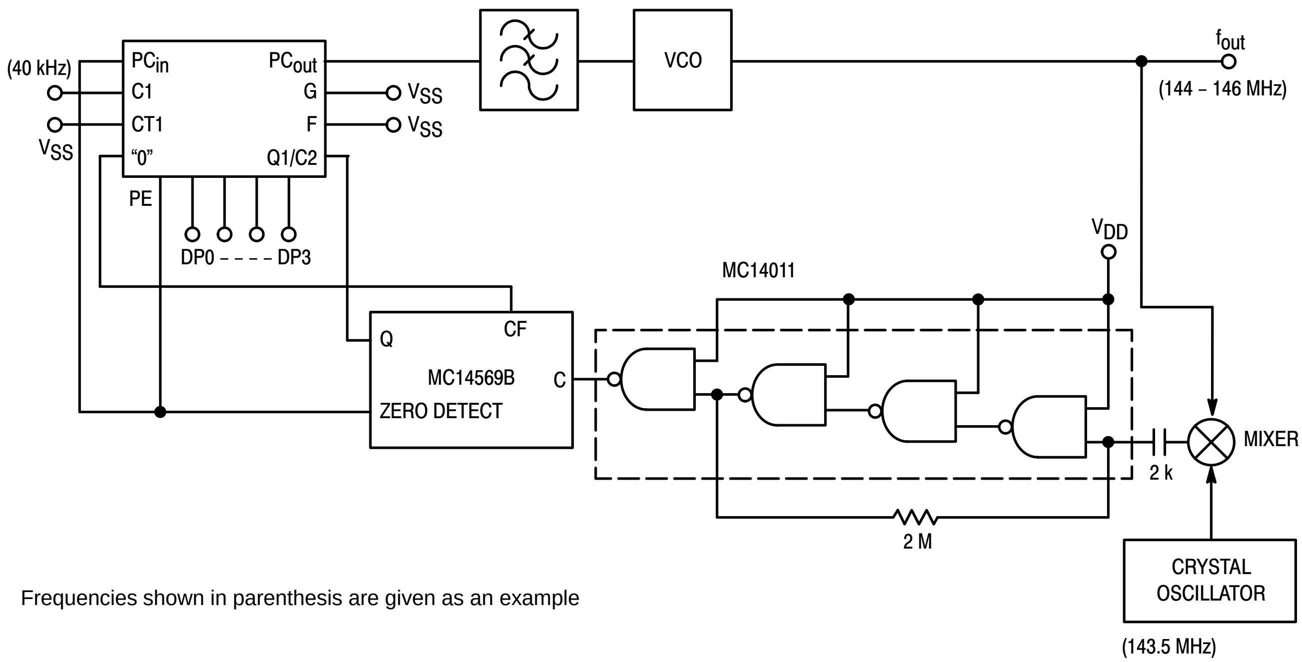


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

MC14572UB

Hex Gate

The MC14572UB hex functional gate is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low−power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range

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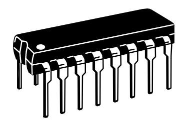
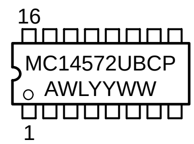
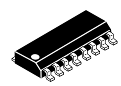
MARKING DIAGRAMS

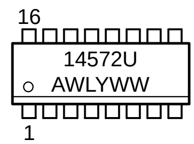


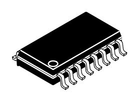
PDIP−16
P SUFFIX
CASE 648



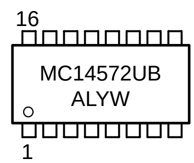


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14572UBCP	PDIP−16	2000/Box
MC14572UBD	SOIC−16	48/Rail
MC14572UBDR2	SOIC−16	2500/Tape & Reel
MC14572UBF	SOEIAJ−16	See Note 1.
MC14572UBFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

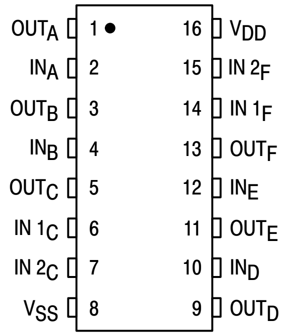
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

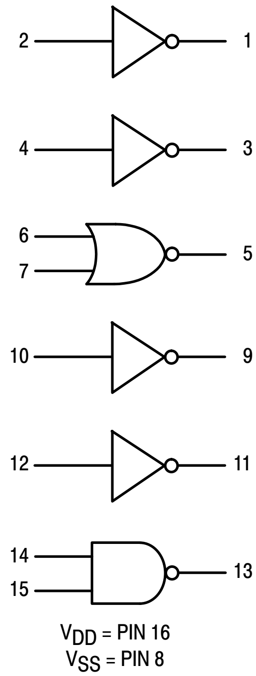
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

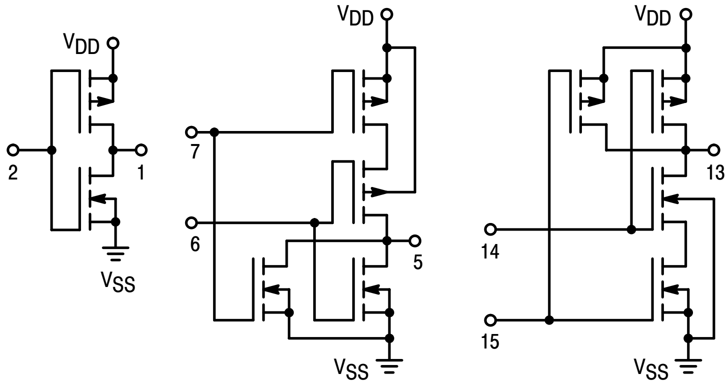
PIN ASSIGNMENT



LOGIC DIAGRAM



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	4.0 8.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	— — — —	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	— — — —	– 0.7 – 0.14 – 0.35 – 1.1	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (1.89 µA/kHz) f + I_{DD} I_T = (3.80 µA/kHz) f + I_{DD} I_T = (5.68 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 5 ns	t_{PHL}	5.0	—	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 17 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 15 ns		15	—	40	80	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

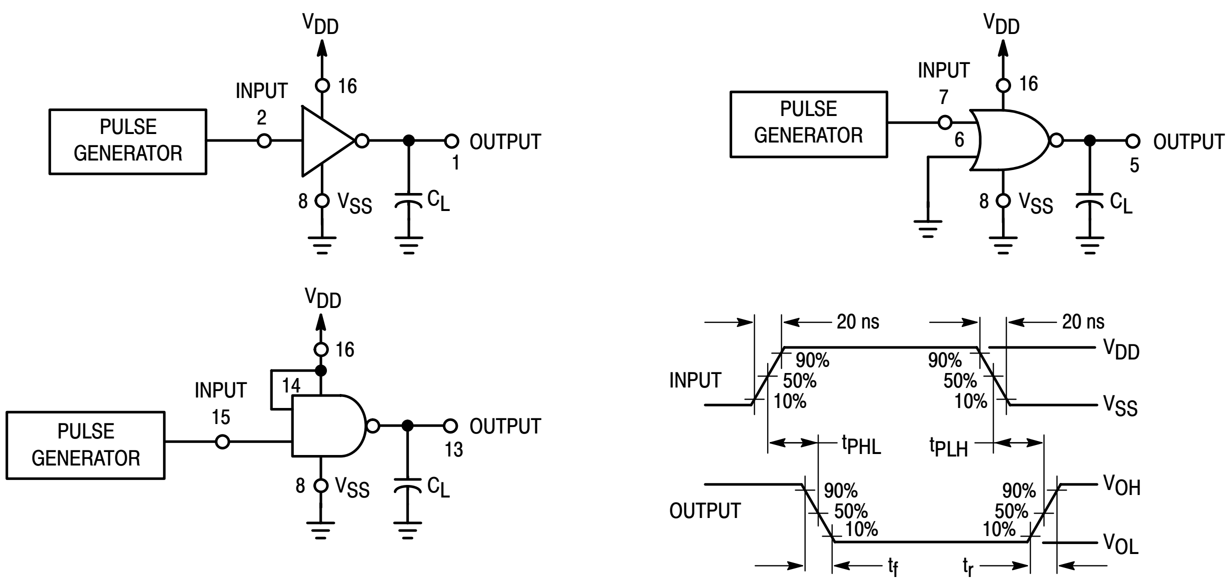


Figure 1. Switching Time Test Circuits and Waveforms

MC14584B

Hex Schmitt Trigger

The MC14584B Hex Schmitt Trigger is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to “square up” slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysteresis, Use MC14106B which is Pin−for−Pin Replacement for CD40106B and MM74Cl4

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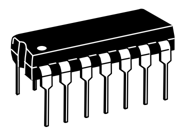
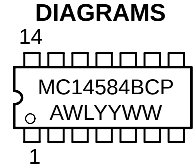
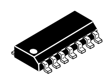
MARKING DIAGRAMS

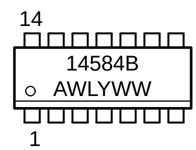


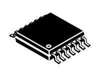
PDIP−14
P SUFFIX
CASE 646



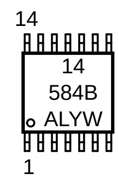


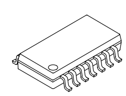
SOIC−14
D SUFFIX
CASE 751A



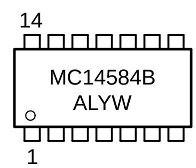


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

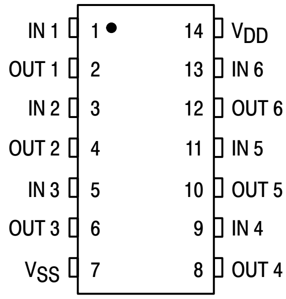
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

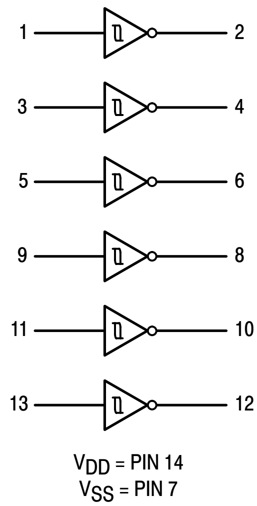
Device	Package	Shipping
MC14584BCP	PDIP−14	2000/Box
MC14584BD	SOIC−14	55/Rail
MC14584BDR2	SOIC−14	2500/Tape & Reel
MC14584BDT	TSSOP−14	96/Rail
MC14584BDTEL	TSSOP−14	2000/Tape & Reel
MC14584BF	SOEIAJ−14	See Note 1.
MC14584BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

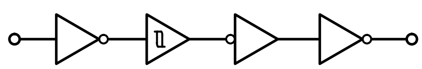
PIN ASSIGNMENT



LOGIC DIAGRAM



EQIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD}	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.8 µA/kHz) f + I_{DD} I_T = (3.6 µA/kHz) f + I_{DD} I_T = (5.4 µA/kHz) f + I_{DD}							µAdc
Hysteresis Voltage	V_H (7.)	5.0 10 15	0.27 0.36 0.77	1.0 1.3 1.7	0.25 0.3 0.6	0.6 0.7 1.1	1.0 1.2 1.5	0.21 0.25 0.50	1.0 1.2 1.4	Vdc
Threshold Voltage Positive−Going	V_{T+}	5.0 10 15	1.9 3.4 5.2	3.5 7.0 10.6	1.8 3.3 5.2	2.7 5.3 8.0	3.4 6.9 10.5	1.7 3.2 5.2	3.4 6.9 10.5	Vdc
Negative−Going	V_{T-}	5.0 10 15	1.6 3.0 4.5	3.3 6.7 9.7	1.6 3.0 4.6	2.1 4.6 6.9	3.2 6.7 9.8	1.5 3.0 4.7	3.2 6.7 9.9	Vdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

7. $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+max} - V_{T-min}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0 10 15	— — —	125 50 40	250 100 80	ns

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

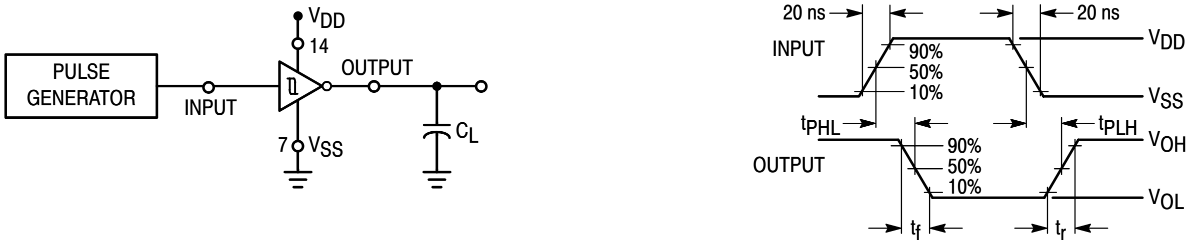
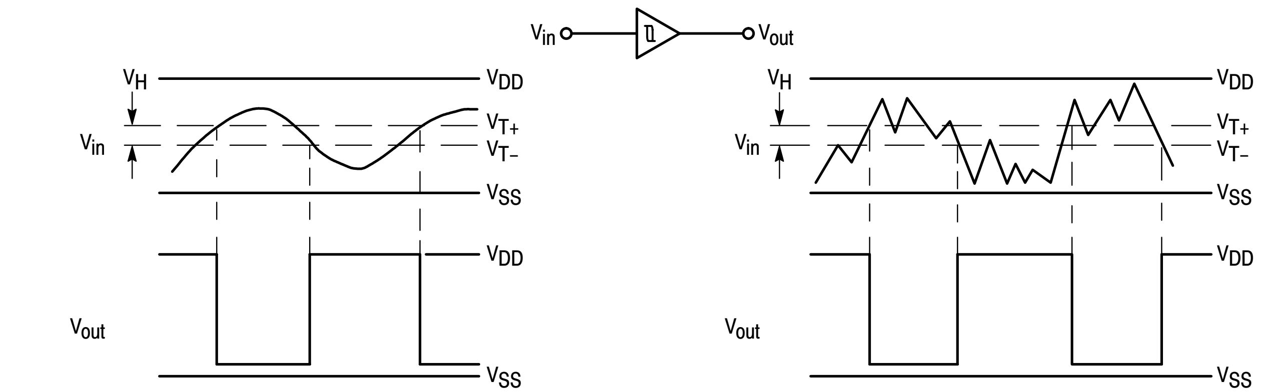


Figure 1. Switching Time Test Circuit and Waveforms



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 2. Typical Schmitt Trigger Applications

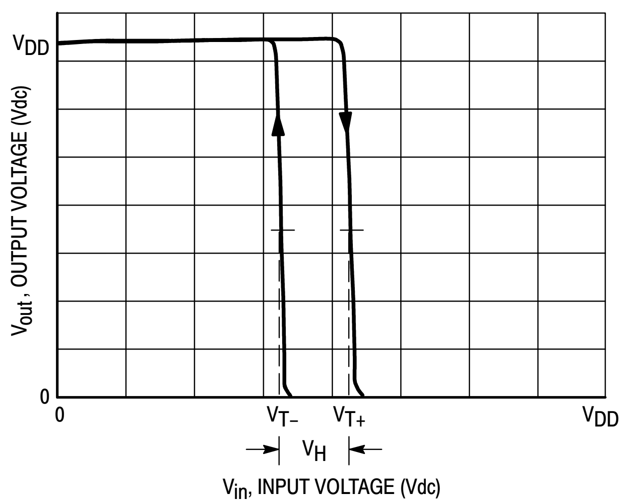


Figure 3. Typical Transfer Characteristics

MC14585B

4-Bit Magnitude Comparator

The MC14585B 4−Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A < B, A = B, and A > B), and three outputs (A < B, A = B, and A > B). This device compares two 4−bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4−bits, units can be cascaded by connecting outputs (A > B), (A < B), and (A = B) to the corresponding inputs of the next significant comparator. Inputs (A < B), (A = B), and (A > B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421−BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded − See Fig. 3

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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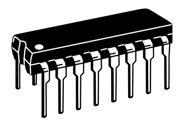
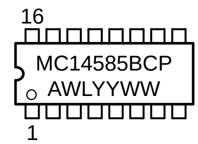
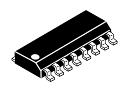
MARKING DIAGRAMS

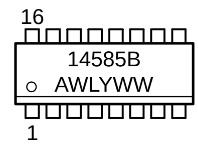


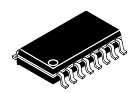
PDIP−16
P SUFFIX
CASE 648



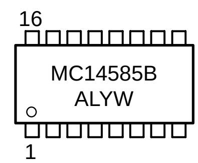


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



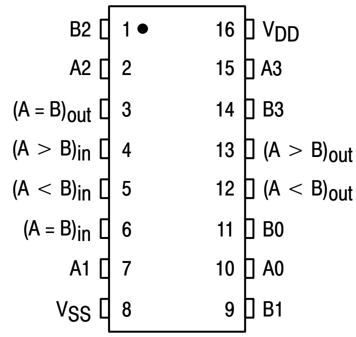
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

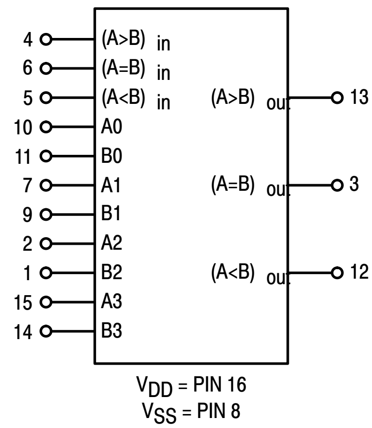
Device	Package	Shipping
MC14585BCP	PDIP−16	2000/Box
MC14585BD	SOIC−16	48/Rail
MC14585BDR2	SOIC−16	2500/Tape & Reel
MC14585BF	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE (x = Don't Care)

Inputs							Outputs		
Comparing				Cascading					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	x	x	x	x	x	x	0	0	1
A3 = B3	A2 > B2	x	x	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 > B1	x	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	x	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	x	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	x	1	1	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	x	x	x	1	0	0
A3 = B3	A2 = B2	A1 < B1	x	x	x	x	1	0	0
A3 = B3	A2 < B2	x	x	x	x	x	1	0	0
A3 < B3	x	x	x	x	x	x	1	0	0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.6 µA/kHz) f + I_{DD} I_T = (1.2 µA/kHz) f + I_{DD} I_T = (1.8 µA/kHz) f + I_{DD}							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

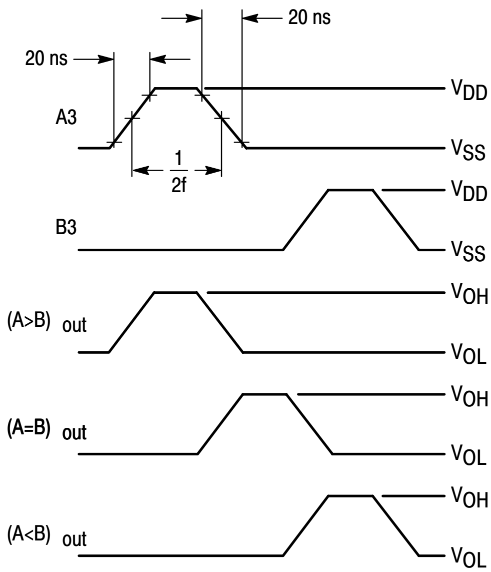
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) (C_L = 50 pF, T_A = 25°C)

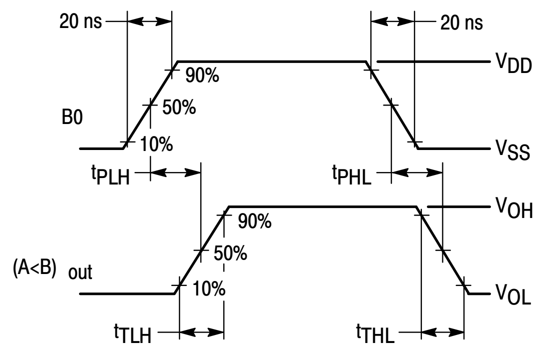
Characteristic	Symbol	V_{DD}	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Turn−On, Turn−Off Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 345 ns		5.0	—	430	860	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	—	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	—	130	260	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low.
f in respect to a system clock.

Figure 1. Dynamic Power Dissipation Signal Waveforms



Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A<B) low.

Figure 2. Dynamic Signal Waveforms

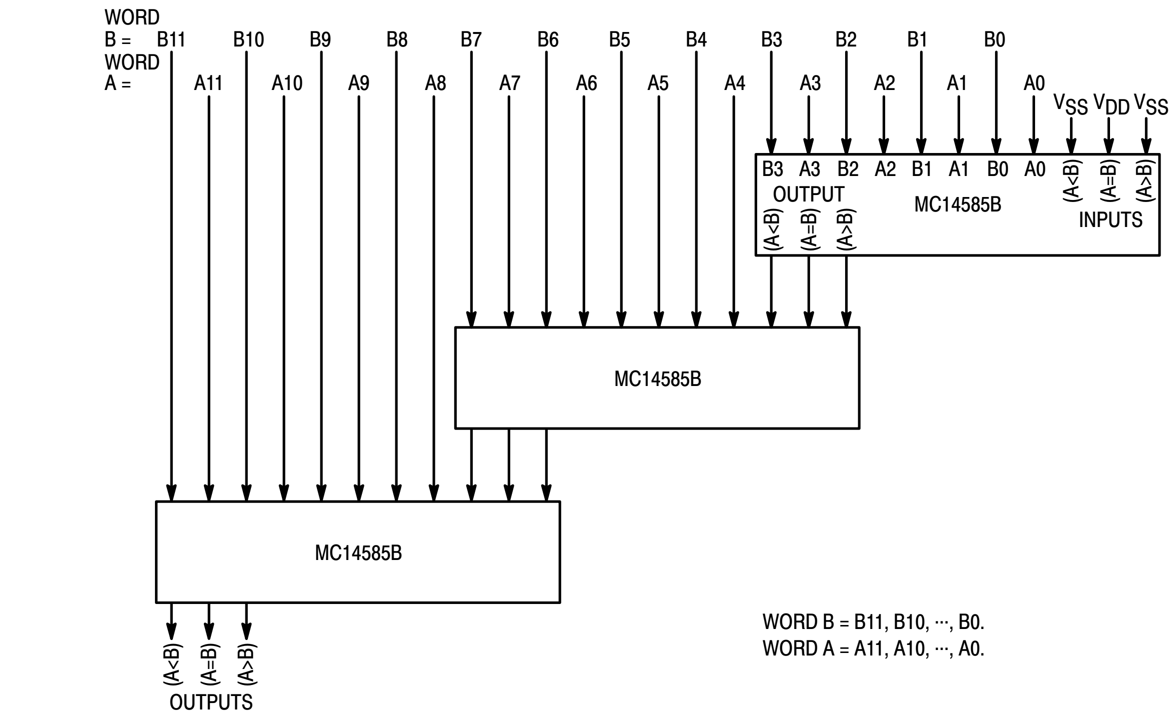
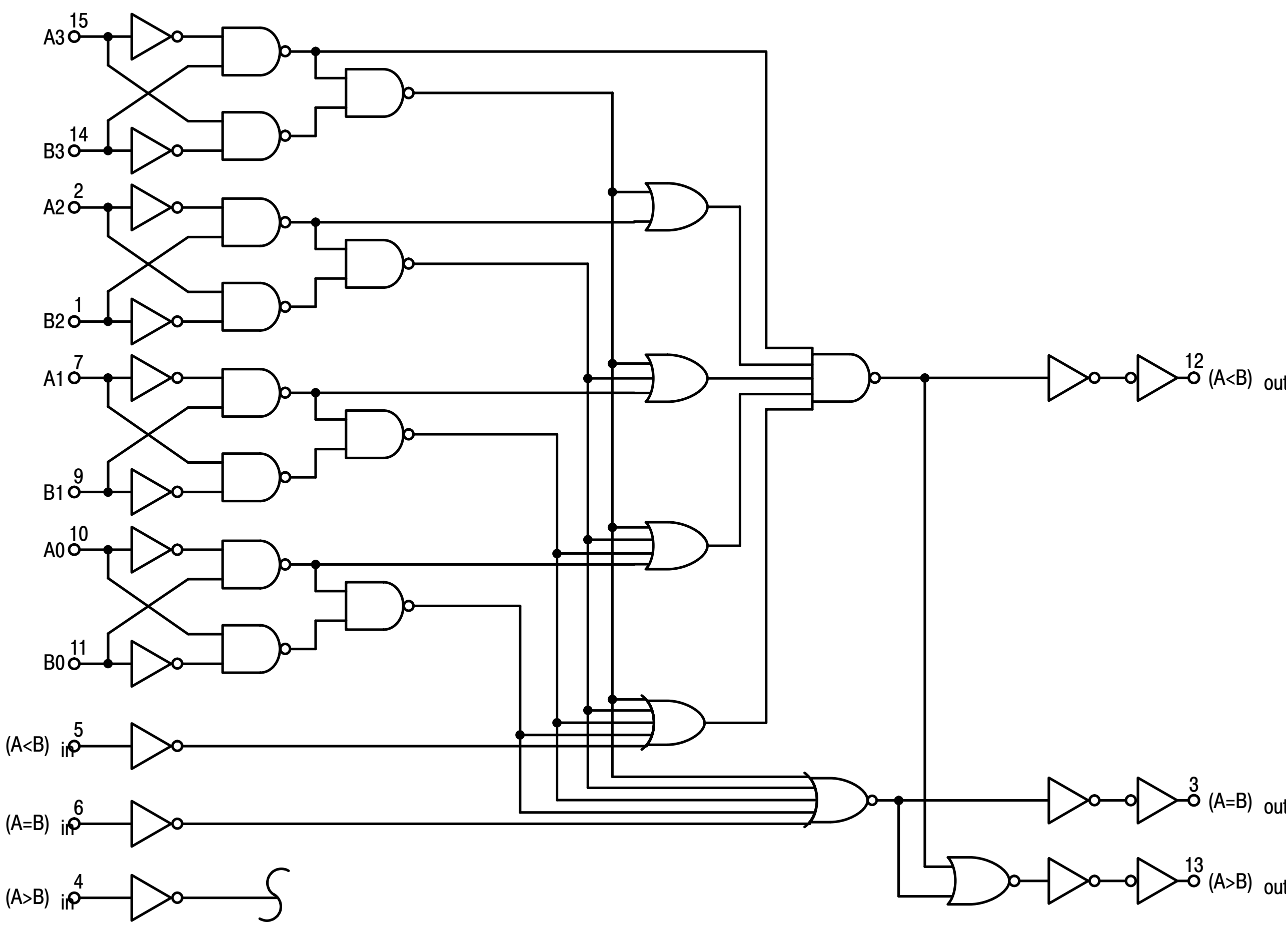


Figure 3. Cascading Comparators

LOGIC DIAGRAM



MC14598B

8-Bit Bus-Compatible Latches

The MC14598B is an 8−bit latch addressed with an external binary address. The 8 latch−outputs are high drive, three−state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2.

All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three−State Bus Compatible Parallel Outputs
- Three−State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire−O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range, Enable (DC or Transient)	−0.5 to V_{DD} + 0.5	V
V_{in}	Input Voltage Range, All Other Inputs (DC or Transient)	−0.5 to V_{DD} + 12	V
V_{out}	Output Voltage Range, (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

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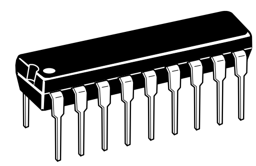


MARKING DIAGRAMS

PDIP−18
P SUFFIX
CASE 707

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

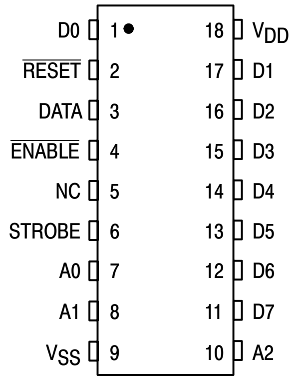
ORDERING INFORMATION

Device	Package	Shipping
MC14598BCP	PDIP−18	20/Rail

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

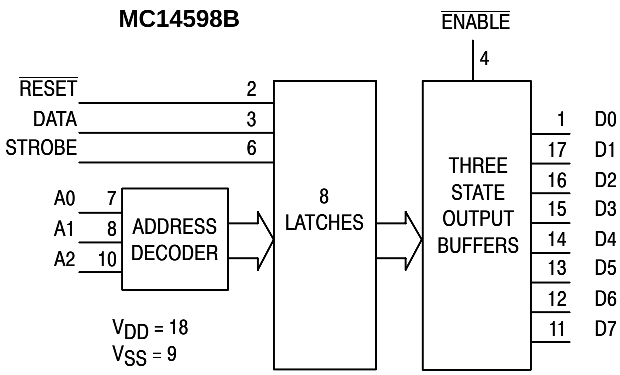
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



BLOCK DIAGRAMS

MC14598B



OUTPUT TRUTH TABLE

$\overline{\text{Enable}}$	Outputs
1	High Impedance
0	D_n

D_n = State of nth latch

NC = NO CONNECTION

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level, V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level, V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (4.) — $\overline{\text{Enable}}$ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	0.8	—	1.1	0.8	—	0.8	
(V_O = 9.0 or 1.0 Vdc)		10	—	1.6	—	2.2	1.6	—	1.6	
(V_O = 13.5 or 1.5 Vdc)		15	—	2.4	—	3.4	2.4	—	2.4	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	2.0	—	2.0	1.9	—	2.0	—	
(V_O = 1.0 or 9.0 Vdc)		10	6.0	—	6.0	3.1	—	6.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	10	—	10	4.3	—	10	—	
Input Voltage "0" Level, Other Inputs	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current Source ($\overline{\text{Full}}$ — Sink Only)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc)		5.0	– 1.0	–	– 1.0	– 2.0	—	– 1.0	—	
(V_{OH} = 9.5 Vdc)		10	—	—	—	– 6.0	—	—	—	
(V_{OH} = 13.5 Vdc)		1 5	—	—	—	– 12	—	—	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.6	—	1.6	3.2	—	1.6	—	mAdc
(V_{OL} = 0.5 Vdc)		10	—	—	—	6.0	—	—	—	
(V_{OL} = 1.5 Vdc)		15	—	—	—	12	—	—	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Three−State Leakage Current	I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current at an External Load Capacitance of 130 pF (4.)	I_T	5.0	I_T = (2.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (4.0 µA/kHz) f + I_{DD}							
			I_T = (6.0 µA/kHz) f + I_{DD}							

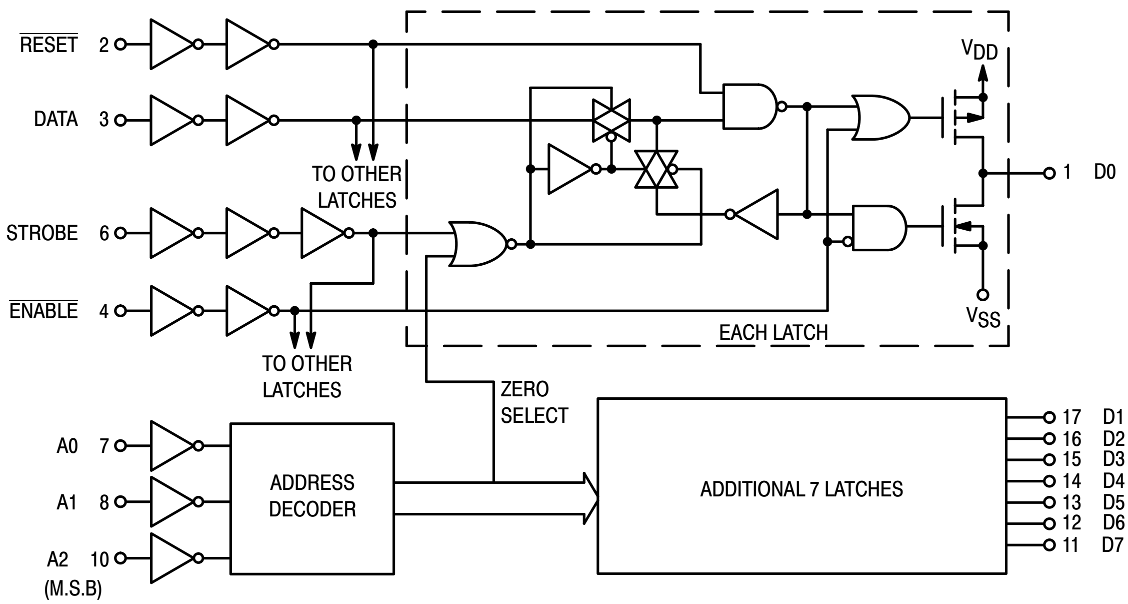
3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (5.) (T_A = 25°C, C_L = 130 pF + 1 TTL Load)

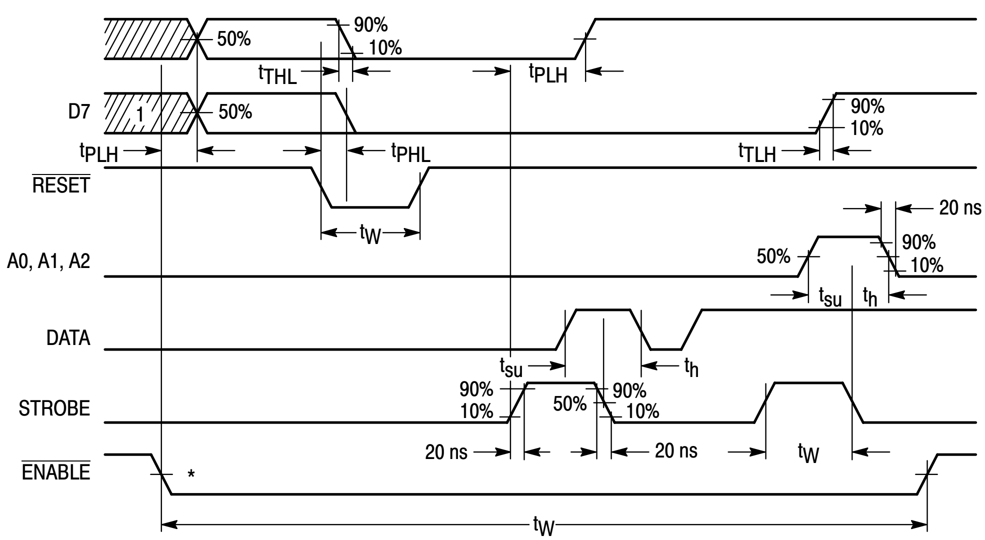
Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ (6.)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (0.5 ns/pF) C_L + 35 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.2 ns/pF) C_L + 25 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.16 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
$\overline{\text{Enable}}$ to Output		5.0	—	160	320	
		10	—	125	250	
		15	—	100	200	
Strobe to Output		5.0	—	200	400	
		10	—	100	200	
		15	—	80	160	
$\overline{\text{Reset}}$ to Output		5.0	—	175	350	
		10	—	90	180	
		15	—	70	140	
Pulse Width	t_{WH}, t_{WL}					ns
$\overline{\text{Enable}}$		5.0	320	160	—	
		10	240	120	—	
		15	160	80	—	
Strobe		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
Increment		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
$\overline{\text{Reset}}$		5.0	300	150	—	
		10	160	80	—	
		15	100	50	—	
Setup Time	t_{su}					ns
Data		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Address		5.0	200	100	—	
		10	100	50	—	
		15	70	35	—	
Hold Time	t_h					ns
Data		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Address		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	20	– 25	—	ns
		10	20	– 15	—	
		15	20	– 10	—	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



*1.4 V with V_{DD} = 5.0 V

NOTES:

1. High−impedance output state (another device controls bus).
2. Output Load as for MC14597B.

LATCH TRUTH TABLE

Strobe	$\overline{\text{Reset}}$	Address Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

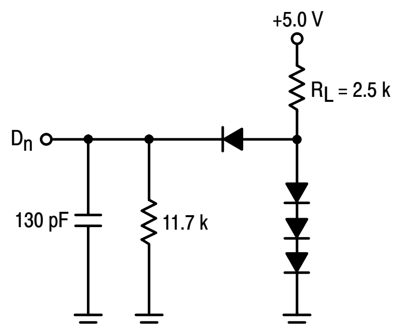
*= No change in state of latch
X = Don’t care

TRUTH TABLE FOR MC14597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
↓	X	1	Count Up	—
↑	X	1	No Change	—
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don’t care

**TEST LOAD
ALL OUTPUTS**



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MC1488

Quad Line EIA-232D Driver

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA−232D.

Features

- Current Limited Output
  ±10 mA typical
- Power−Off Source Impedance
  300 Ω minimum
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All ON Semiconductor MDTL and MTTL Logic Families
- Pb−Free Packages are Available

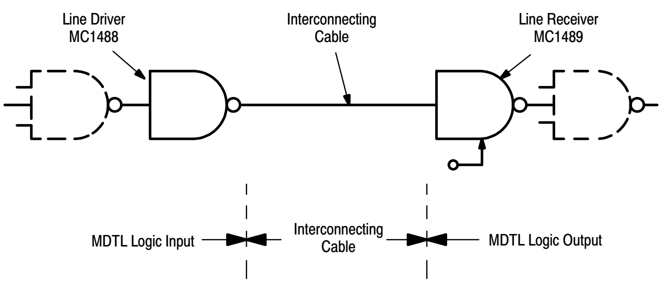

Figure 1. Simplified Application

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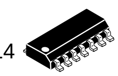
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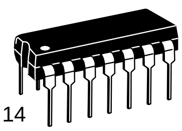
SOIC−14
D SUFFIX
CASE 751A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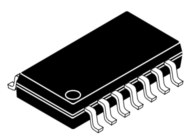
PDIP−14
P SUFFIX
CASE 646

14

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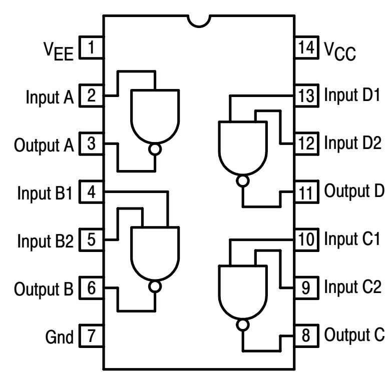
SOEIAJ−14
M SUFFIX
CASE 965

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 445 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 445 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

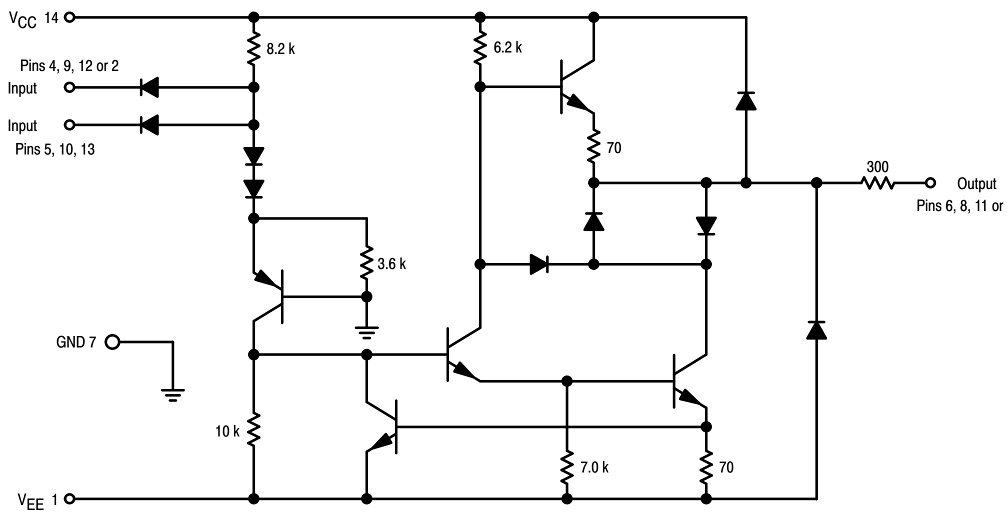


Figure 2. Circuit Schematic
(1/4 of Circuit Shown)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+ 15 − 15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, SO−14 and Plastic Dual−In−Line Package) Derate above T_A = + 25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to + 75	°C
Storage Temperature Range	T_{stg}	− 65 to + 175	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (V_{CC} = + 9.0 ± 1% Vdc, V_{EE} = −9.0 ± 1% Vdc, T_A = 0 to 75°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current − Low Logic State (V_{IL} = 0)	I_{IL}	−	1.0	1.6	mA
Input Current − High Logic State (V_{IH} = 5.0 V)	I_{IH}	−	−	10	µA
Output Voltage − High Logic State (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = + 9.0 Vdc, V_{EE} = − 9.0 Vdc) (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = + 13.2 Vdc, V_{EE} = − 13.2 Vdc)	V_{OH}	 + 6.0 + 9.0	 +7.0 +10.5	 − −	Vdc
Output Voltage − Low Logic State (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = + 9.0 Vdc, V_{EE} = − 9.0 Vdc) (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = + 13.2 Vdc, V_{EE} = − 13.2 Vdc)	V_{OL}	 − 6.0 − 9.0	 − 7.0 − 10.5	 − −	Vdc
Positive Output Short−Circuit Current, Note 1	I_{OS+}	+ 6.0	+ 10	+ 12	mA
Negative Output Short−Circuit Current, Note 1	I_{OS-}	− 6.0	− 10	− 12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\lvert V_O \rvert$ = ± 2.0 V)	r_o	300	−	−	Ohms
Positive Supply Current (R_I = ∞) (V_{IH} = 1.9 Vdc, V_{CC} = + 9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = + 9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = + 12 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = + 12 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = + 15 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = + 15 Vdc)	I_{CC}	 − − − − − −	 + 15 + 4.5 + 19 + 5.5 − −	 + 20 + 6.0 + 25 + 7.0 + 34 + 12	mA
Negative Supply Current (R_L = ∞) (V_{IH} = 1.9 Vdc, V_{EE} = − 9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = − 9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = − 12 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = − 12 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = − 15 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = − 15 Vdc)	I_{EE}	 − − − − − −	 − 13 − − 18 − − −	 − 17 − 500 − 23 − 500 − 34 − 2.5	 mA µA mA µA mA mA
Power Consumption (V_{CC} = 9.0 Vdc, V_{EE} = − 9.0 Vdc) (V_{CC} = 12 Vdc, V_{EE} = − 12 Vdc)	P_C	 − −	 − −	 333 576	mW

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = −9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time (z_I = 3.0 k and 15 pF)	t_{PLH}	−	275	350	ns
Fall Time (z_I = 3.0 k and 15 pF)	t_{THL}	−	45	75	ns
Propagation Delay Time (z_I = 3.0 k and 15 pF)	t_{PHL}	−	110	175	ns
Rise Time (z_I = 3.0 k and 15 pF)	t_{TLH}	−	55	100	ns

6. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

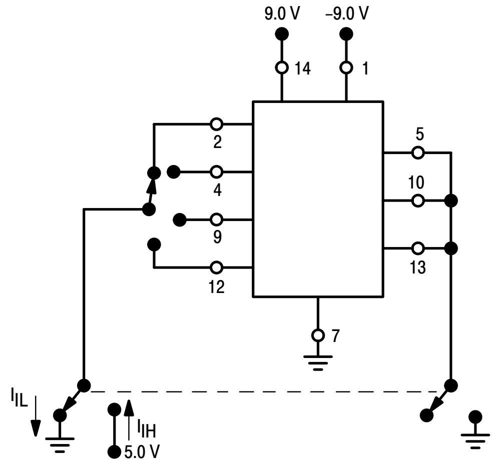


Figure 3. Input Voltage

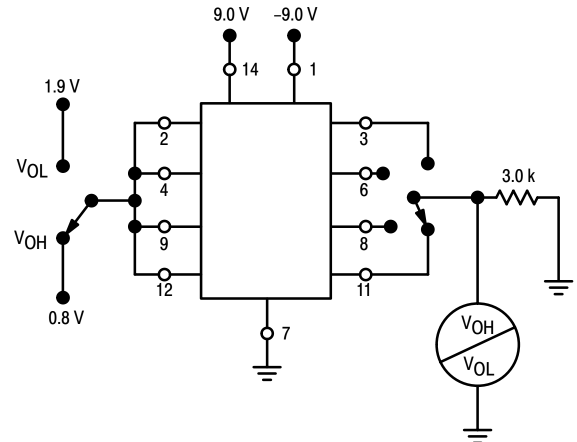


Figure 4. Output Current

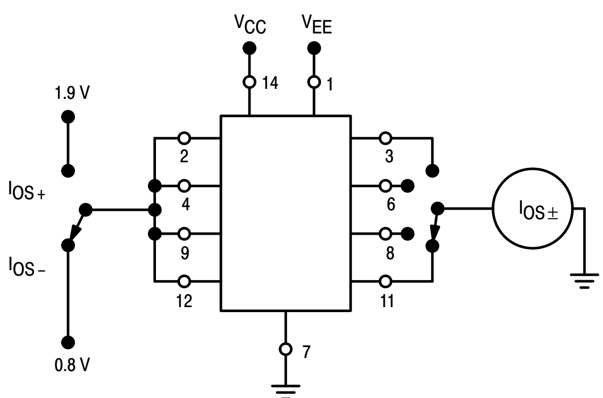


Figure 5. Output Short−Circuit Current

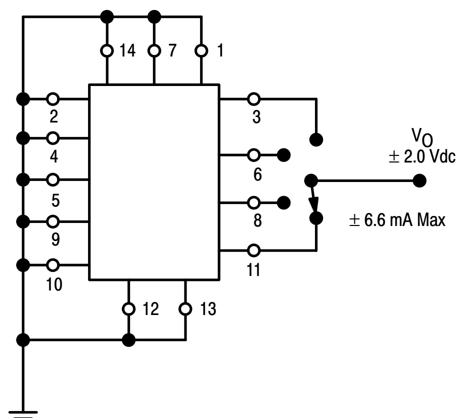


Figure 6. Output Resistance (Power Off)

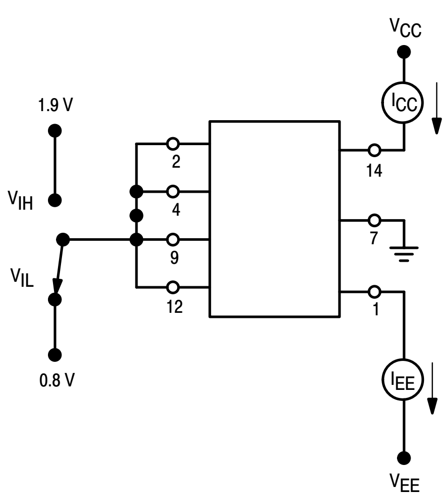


Figure 7. Power Supply Currents

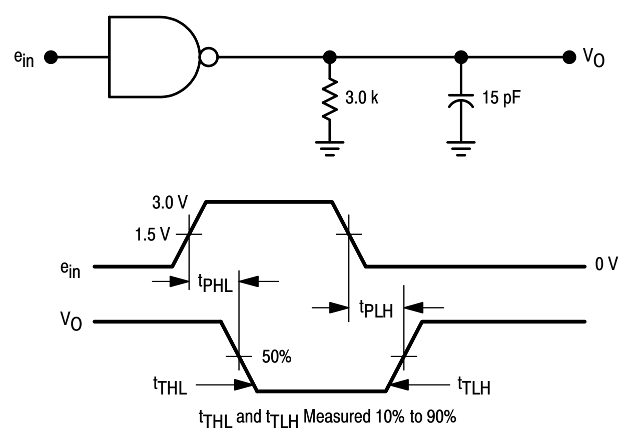


Figure 8. Switching Response

TYPICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

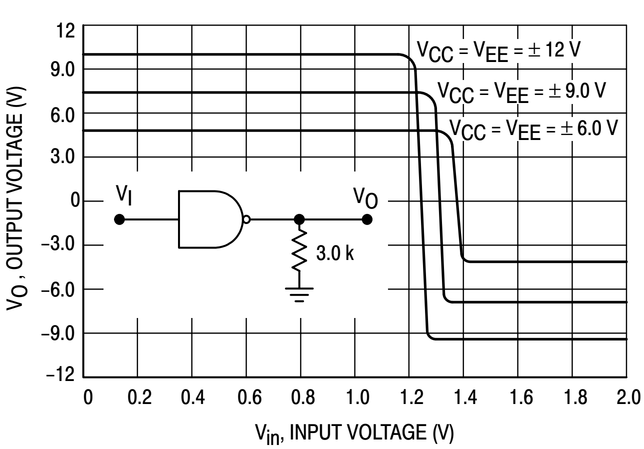


Figure 9. Transfer Characteristics versus Power Supply Voltage

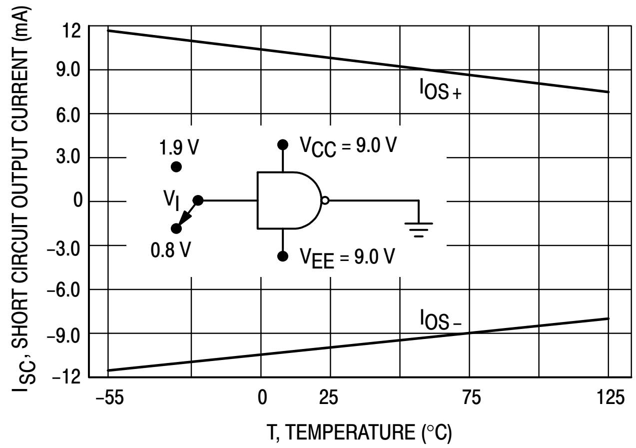


Figure 10. Short Circuit Output Current versus Temperature

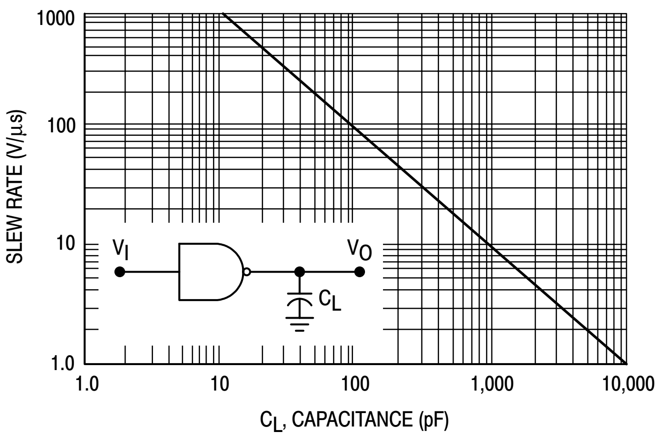


Figure 11. Output Slew Rate versus Load Capacitance

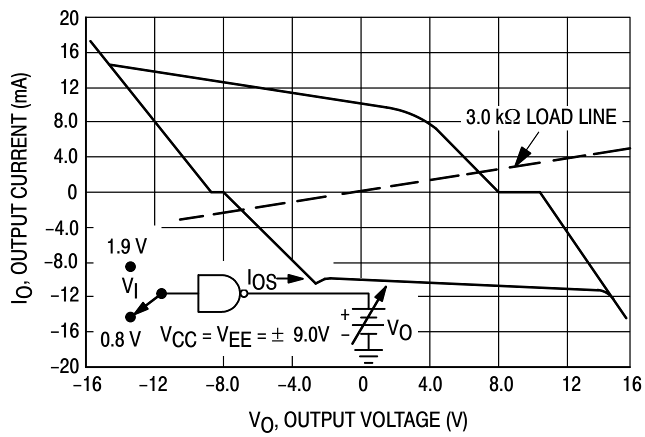


Figure 12. Output Voltage and Current−Limiting Characteristics

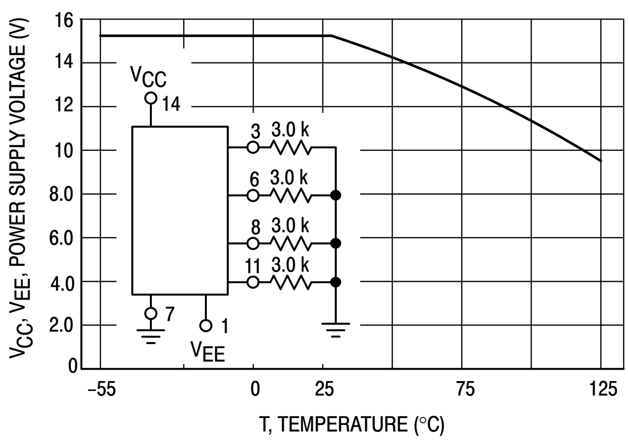


Figure 13. Maximum Operating Temperature versus Power Supply Voltage

APPLICATIONS INFORMATION

The Electronic Industries Association EIA−232D specification details the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA−232D defined levels. The EIA−232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5.0 and 15 V in magnitude and are positive for a Logic “0” and negative for a Logic “1.” These voltages are so defined when the drivers are terminated with a 3000 to 7000 Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA−232D levels with one stage of inversion.

The EIA−232D specification further requires that during transitions, the driver output slew rate must not exceed 30 V per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 14 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per microsecond.

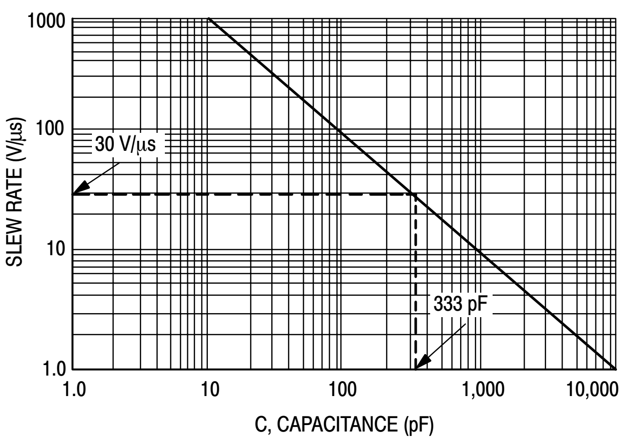


Figure 14. Slew Rate versus Capacitance for I_{SC} = 10 mA

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power supply voltages are greater than 9.0 V (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power supply designs, a loss of system power causes a low impedance on the power supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 Ω output resistors to ground. If all four outputs were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power supplies of the drivers, a diode should be placed in each power supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 15, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25 V limits specified in the earlier Standard EIA−232B.) The addition of the diodes also permits the MC1488 to withstand faults with power supplies of less than the 9.0 V stated above.

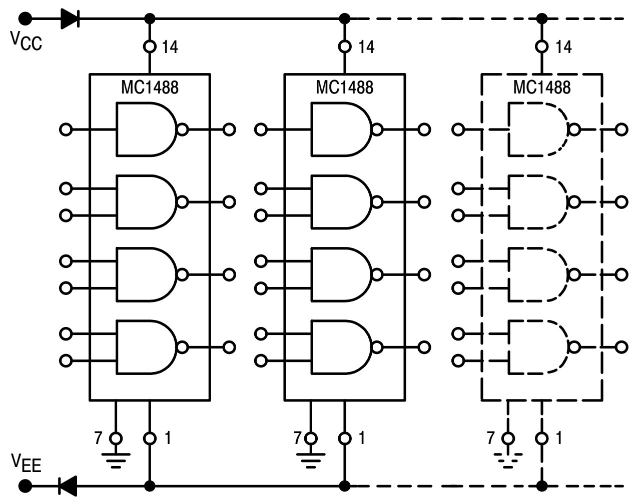


Figure 15. Power Supply Protection to Meet Power Off Fault Conditions

The maximum short circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting − this enables the circuit designer to define the output voltage levels independent of power supplies and can be accomplished by diode clamping of the output pins. Figure 16 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range − as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power supplies. In fact, the positive supply can vary from a minimum 7.0 V (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately − 2.5 V to the minimum specified − 15 V. The MC1488 will drive the output to within 2.0 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current limiting and supply voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA−232D lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 17 shows one such combination.

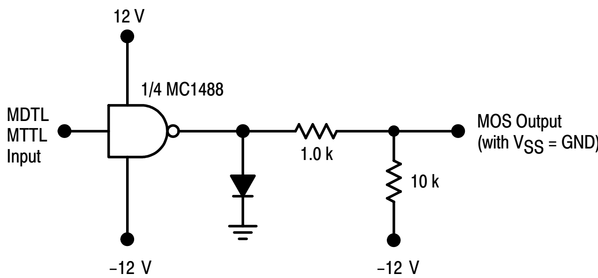


Figure 16. MDTL/MTTL−to−MOS Translator

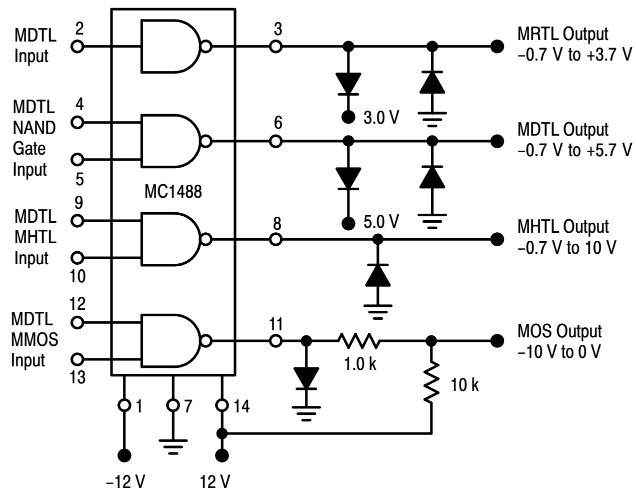


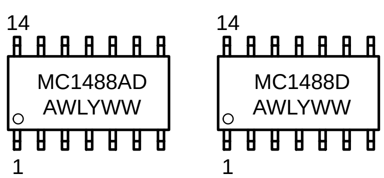
Figure 17. Logic Translator Applications

ORDERING INFORMATION

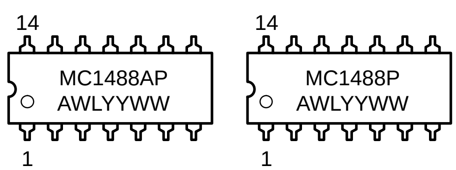
Device	Package	Operating Temperature Range	Shipping
MC1488D	SOIC−14	T_A = 0 to +75°C	55 Units/Rail
MC1488DR2			2500 Tape & Reel
MC1488DR2G	SOIC−14 (Pb−Free)		2500 Tape & Reel
MC1488P	PDIP−14	T_A = 0 to +75°C	500 Units/Rail
MC1488PG	PDIP−14 (Pb−Free)		500 Units/Rail
MC1488M	SOEIAJ−14	T_A = 0 to +75°C	50 Units/Rail
MC1488M	SOEIAJ−14 (Pb−Free)		50 Units/Rail
MC1488MEL	SOEIAJ−14		2000 Tape & Reel
MC1488MEL	SOEIAJ−14 (Pb−Free)		2000 Tape & Reel

MARKING DIAGRAMS

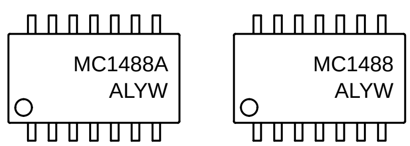
SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646



SOEIAJ−14
M SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

MC1489, MC1489A

Quad Line EIA-232D Receivers

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA−232D.

Features

- Input Resistance − 3.0 k to 7.0 kΩ
- Input Signal Range − ± 30 V
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering
- Pb−Free Packages are Available

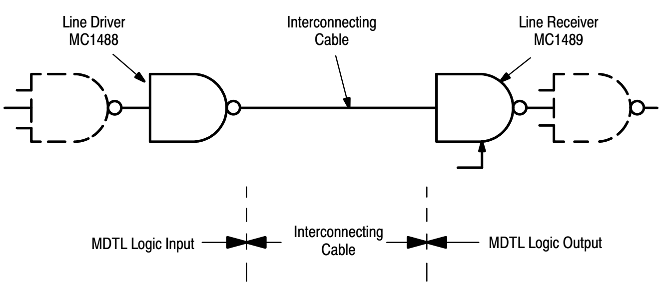


Figure 1. Simplified Application

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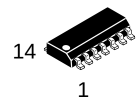
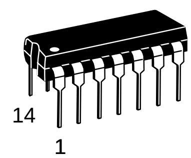
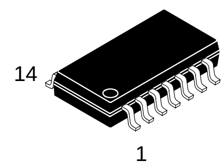


SOIC−14
D SUFFIX
CASE 751A

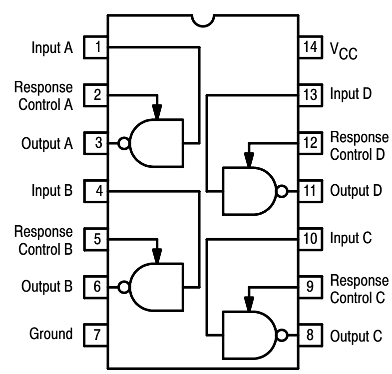


PDIP−14
P SUFFIX
CASE 646



SOEIAJ−14
M SUFFIX
CASE 965

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 453 of this data sheet.

DEVICE MARKING INFORMATION

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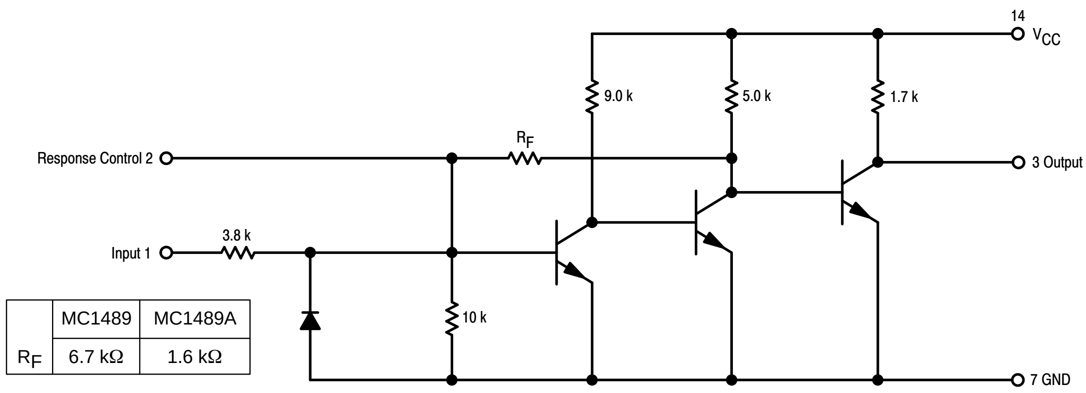
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



	MC1489	MC1489A
R_F	6.7 kΩ	1.6 kΩ

Figure 2. Representative Schematic Diagram
(1/4 of Circuit Shown)

MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	± 30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, SOIC−14 and Plastic Dual In−Line Package) Derate above T_A = + 25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to + 75	°C
Storage Temperature Range	T_{stg}	− 65 to + 175	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

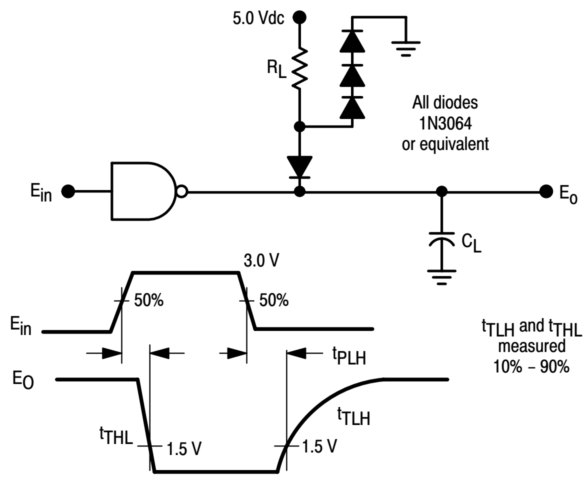
ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = + 5.0 Vdc ± 10%, T_A = 0 to + 75°C, unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = + 25 Vdc) (V_{IH} = + 3.0 Vdc)	I_{IH}	3.6 0.43	− −	8.3 −	mA
Negative Input Current	(V_{IH} = − 25 Vdc) (V_{IH} = − 3.0 Vdc)	I_{IL}	− 3.6 − 0.43	− −	− 8.3 −	mA
Input Turn−On Threshold Voltage (T_A = + 25°C, V_{OL} ⩽ 0.45 V)	 MC1489 MC1489A	V_{IH}	 1.0 1.75	 − 1.95	 1.5 2.25	Vdc
Input Turn−Off Threshold Voltage (T_A = + 25°C, V_{OH} ⩾ 2.5 V, I_L = − 0.5 mA)	 MC1489 MC1489A	V_{IL}	 0.75 0.75	 − 0.8	 1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = − 0.5 mA) (Input Open Circuit, I_L = − 0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	−	0.2	0.45	Vdc
Output Short−Circuit Current		I_{OS}	−	− 3.0	− 4.0	mA
Power Supply Current (All Gates “on,” I_{out} = 0 mA, V_{IH} = + 5.0 Vdc)		I_{CC}	−	16	26	mA
Power Consumption	(V_{IH} = + 5.0 Vdc)	P_C	−	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = + 25°C, See Figure 3.)

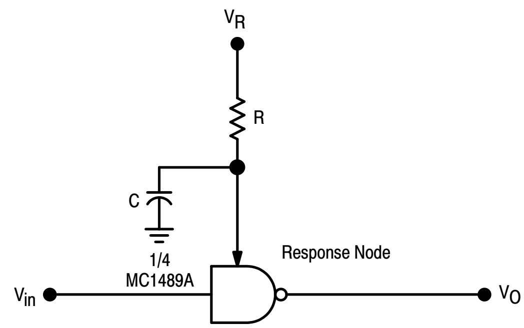
Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	−	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	−	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	−	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	−	10	20	ns

TEST CIRCUITS



C_L = 15 pF = total parasitic capacitance which includes probe and wiring capacitances

Figure 3. Switching Response



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

Figure 4. Response Control Node

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C, unless otherwise noted)

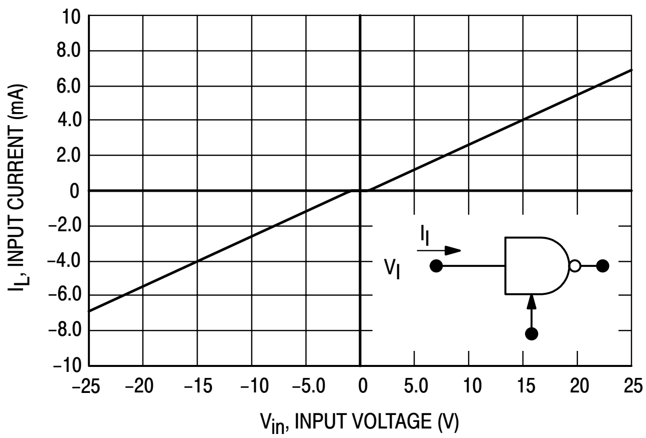


Figure 5. Input Current

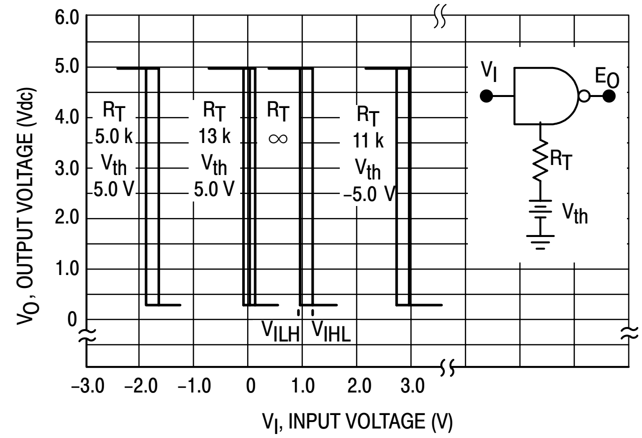


Figure 6. MC1489 Input Threshold Voltage Adjustment

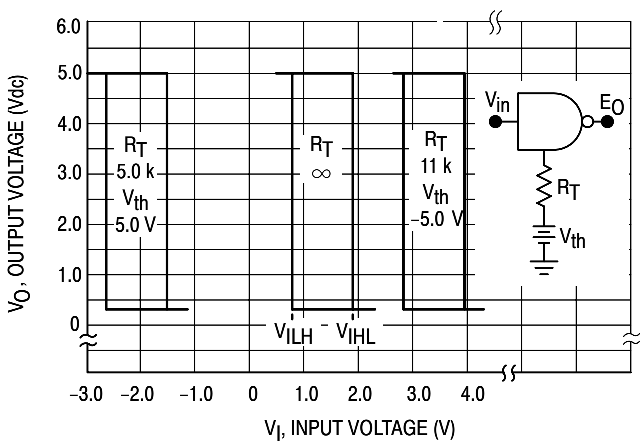


Figure 7. MC1489A Input Threshold Voltage Adjustment

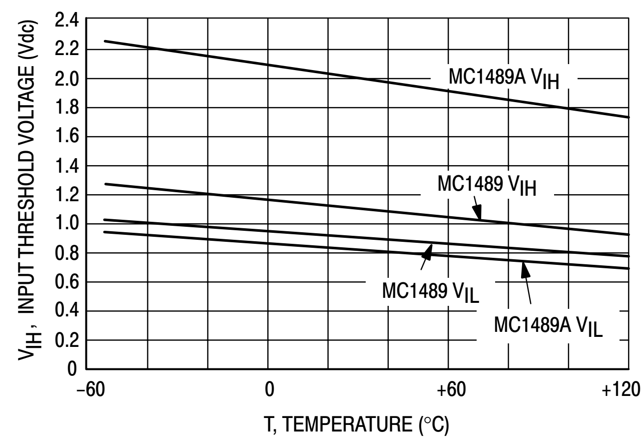


Figure 8. Input Threshold Voltage versus Temperature

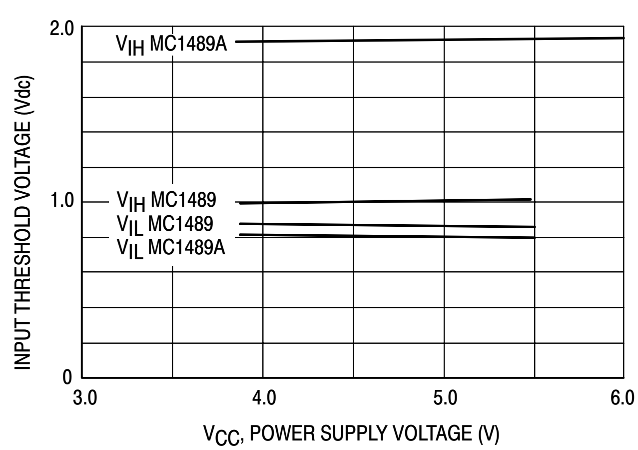


Figure 9. Input Threshold versus Power Supply Voltage

APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA−232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA−232D defined levels. The EIA−232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between − 3.0 and −25 V as a Logic "1" and inputs between 3.0 and 25 V as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn−on voltage of 1.25 V and turn−off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn−on of 1.95 V and turn−off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 4, 6 and 7 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 10 and 11 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 12).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 13 where two receivers are slaved to the same line that must still meet the EIA−232D impedance requirement.

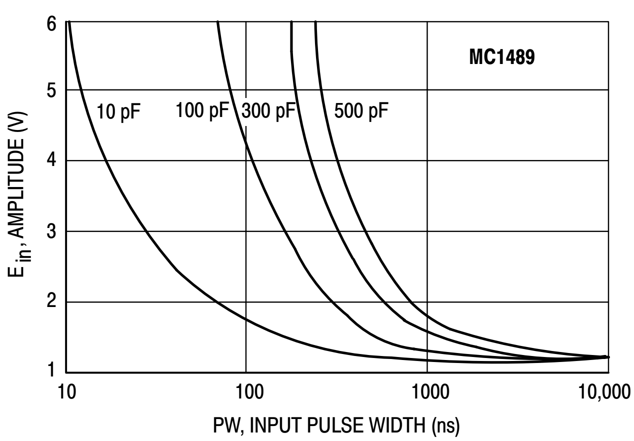


Figure 10. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

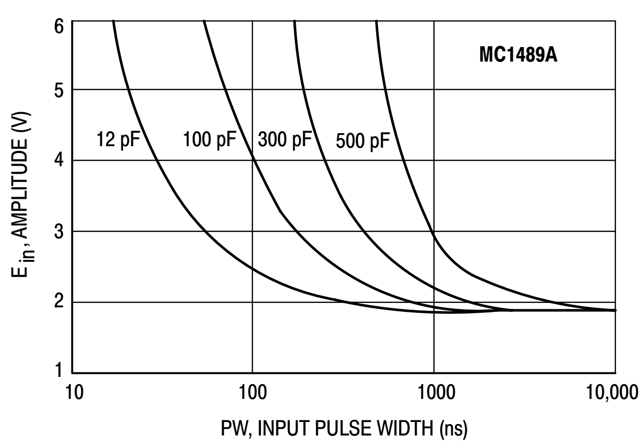


Figure 11. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

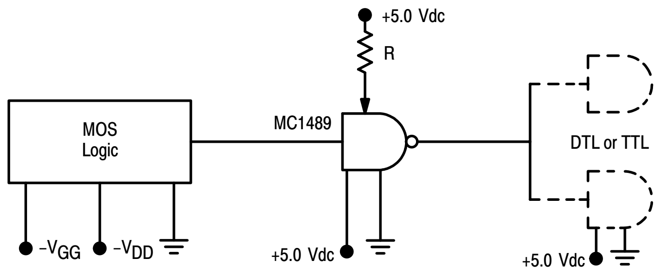


Figure 12. Typical Translator Application − MOS to DTL or TTL

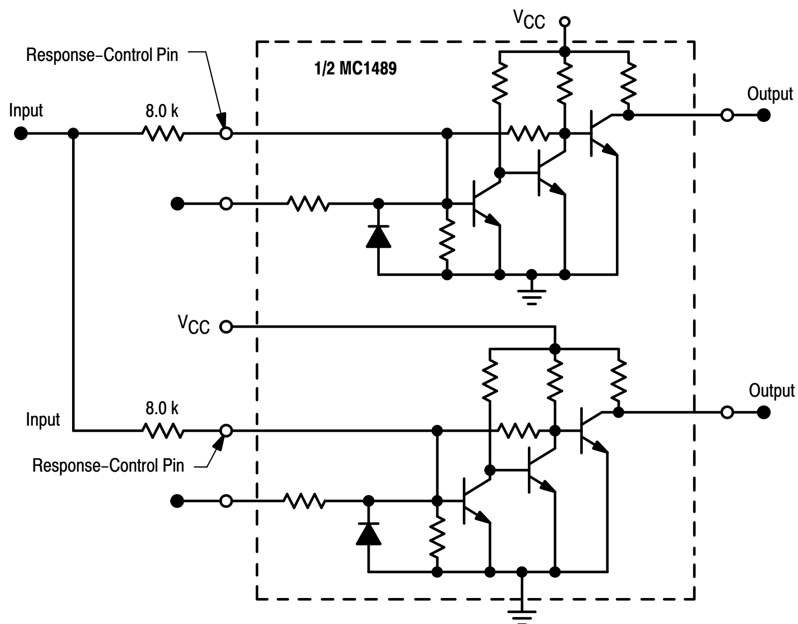


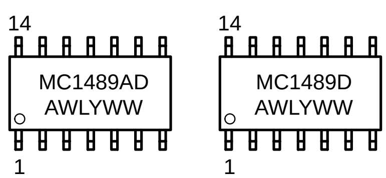
Figure 13. Typical Paralleling of Two MC1489, A Receivers to Meet EIA−232D

ORDERING INFORMATION

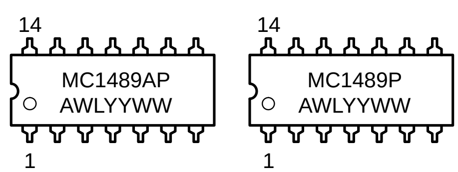
Device	Package	Operating Temperature Range	Shipping
MC1489D	SOIC−14	T_A = 0 to +75°C	55 Units/Rail
MC1489DR2			2500 Tape & Reel
MC1489AD			55 Units/Rail
MC1489ADG	SOIC−14 (Pb−Free)		55 Units/Rail
MC1489ADR2	SOIC−14		2500 Tape & Reel
MC1489ADR2G	SOIC−14 (Pb−Free)		2500 Tape & Reel
MC1489P	PDIP−14	T_A = 0 to +75°C	25 Units/Rail
MC1489PG	PDIP−14 (Pb−Free)		25 Units/Rail
MC1489AP	PDIP−14		25 Units/Rail
MC1489M	SOEIAJ−14	T_A = 0 to +75°C	50 Units/Rail
MC1489MEL			2000 Tape & Reel
MC1489AM			50 Units/Rail
MC1489AM	SOEIAJ−14 (Pb−Free)		50 Units/Rail
MC1489AMEL	SOEIAJ−14		2000 Tape & Reel
MC1489AMEL	SOEIAJ−14 (Pb−Free)		2000 Tape & Reel

MARKING DIAGRAMS

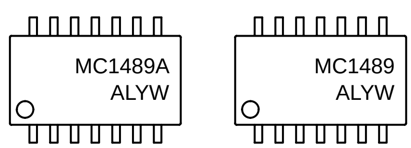
SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646



SOEIAJ−14
M SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

MC1496, MC1496B

Balanced Modulators/ Demodulators

These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See ON Semiconductor Application Note AN531 for additional design information.

Features

- Excellent Carrier Suppression −65 dB typ @ 0.5 MHz
  −50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection −85 dB Typical
- This Device Contains 8 Active Transistors
- Pb−Free Package is Available*

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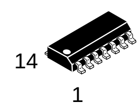
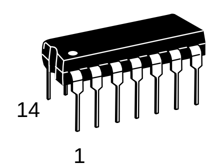
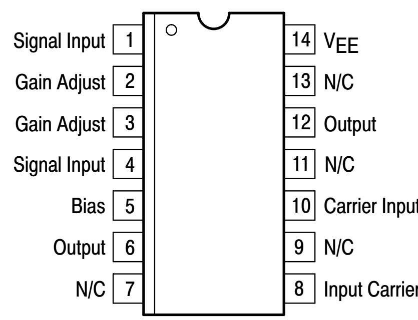


SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 465 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 465 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

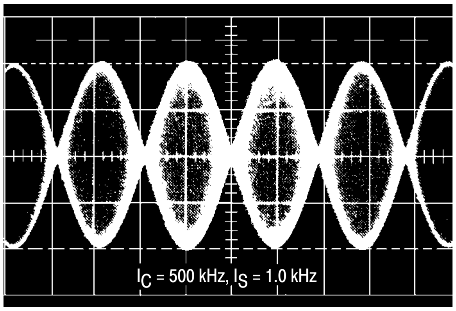


Figure 1. Suppressed Carrier Output Waveform

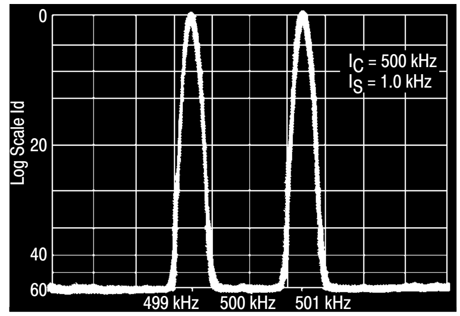


Figure 2. Suppressed Carrier Spectrum

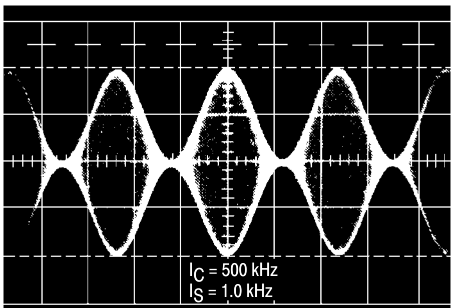


Figure 3. Amplitude Modulation Output Waveform

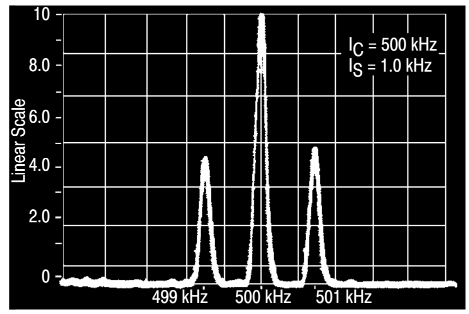


Figure 4. Amplitude−Modulation Spectrum

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V6−V8, V10−V1, V12−V8, V12−V10, V8−V4, V8−V1, V10−V4, V6−V10, V2−V5, V3−V5)	ΔV	30	Vdc
Differential Input Signal	V8 − V10 V4 − V1	+5.0 ±(5 + I5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction−to−Air Plastic Dual In−Line Package	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range MC1496 MC1496B	T_A	0 to +70 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM)	ESD	 2000 400	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{EE} = −8.0 Vdc, I5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, $T_A = T_{low}$ to T_{high}, all input and output characteristics are single−ended, unless otherwise noted.) (Note 1)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Carrier Feedthrough	5	1	V_{CFT}				μVrms
V_C = 60 mVrms sine wave and offset adjusted to zero, f_C = 1.0 kHz				−	40	−	
f_C = 10 MHz				−	140	−	
V_C = 300 mVpp square wave:							mVrms
offset adjusted to zero, f_C = 1.0 kHz				−	0.04	0.4	
offset not adjusted, f_C = 1.0 kHz				−	20	200	
Carrier Suppression	5	2	V_{CS}				dB
f_S = 10 kHz, 300 mVrms							
f_C = 500 kHz, 60 mVrms sine wave				40	65	−	
f_C = 10 MHz, 60 mVrms sine wave				−	50	−	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 Ω)	8	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mVrms sine wave, f_S = 1.0 kHz, 300 mVrms sine wave				−	300	−	
Signal Input Port, V_S = 300 mVrms sine wave, $\|V_C\|$ = 0.5 Vdc				−	80	−	
Signal Gain (V_S = 100 mVrms, f = 1.0 kHz; $\|V_C\|$= 0.5 Vdc)	10	3	A_{VS}	2.5	3.5	−	V/V
Single−Ended Input Impedance, Signal Port, f = 5.0 MHz	6	−					
Parallel Input Resistance			r_{ip}	−	200	−	kΩ
Parallel Input Capacitance			c_{ip}	−	2.0	−	pF
Single−Ended Output Impedance, f = 10 MHz	6	−					
Parallel Output Resistance			r_{op}	−	40	−	kΩ
Parallel Output Capacitance			c_{oo}	−	5.0	−	pF
Input Bias Current $I_{bS} = \frac{I1 + I4}{2}$; $I_{bC} = \frac{I8 + I10}{2}$	7	−					μA
			I_{bS}	−	12	30	
			I_{bC}	−	12	30	
Input Offset Current	7	−					μA
I_{ioS} = I1−I4			$\|I_{ioS}\|$	−	0.7	7.0	
I_{ioC} = I8−I10			$\|I_{ioC}\|$	−	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	7	−	$\|TC_{Iio}\|$	−	2.0	−	nA/°C
Output Offset Current (I6−I9)	7	−	$\|I_{oo}\|$	−	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	7	−	$\|TC_{Ioo}\|$	−	90	−	nA/°C
Common−Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	−	5.0	−	Vpp
Common−Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$= 0.5 Vdc	9	−	ACM	−	−85	−	dB
Common−Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	−	V_{out}	−	8.0	−	Vpp
Differential Output Voltage Swing Capability	10	−	V_{out}	−	8.0	−	Vpp
Power Supply Current	7	6					mAdc
I6 +I12			I_{CC}	−	2.0	4.0	
I14			I_{EE}	−	3.0	5.0	
DC Power Dissipation	7	5	P_D	−	33	−	mW

1. T_{low} = 0°C for MC1496, = −40°C for MC1496B; T_{high} = +70°C for MC1496, = +125°C for MC1496B

GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal−input transistor pair − or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input−signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single−ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I5(\text{mA})}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors “on” and two transistors “off” (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I5.

$$V_S \leqslant I5\ R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common−mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage−current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, P_D = 2 I5 (V6 − V14) + I5)V5 − V14 where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

I5 = I6 = I12,

$I_B << I_C$ for all transistors

then :

$$R5 = \frac{V - -\phi}{I5} - 500\ \Omega$$

where: R5 is the resistor between Pin 5 and ground

ϕ = 0.75 at T_A = +25°C

The MC1496 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common−Mode Quiescent Output Voltage

$$V6 = V12 = V+ - I5\ R_L$$

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector−base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

30 Vdc ≥ [(V6, V12) − (V8, V10)] ≥ 2 Vdc

30 Vdc ≥ [(V8, V10) − (V1, V4)] ≥ 2.7 Vdc

30 Vdc ≥ [(V1, V4) − (V5)] ≥ 2.7 Vdc

The foregoing conditions are based on the following approximations:

V6 = V12, V8 = V10, V1 = V4

Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21C = \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \Bigg|_{V_o = 0}$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21S = \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \Bigg|_{V_c = 0.5 \text{ Vdc},\ V_o = 0}$$

Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

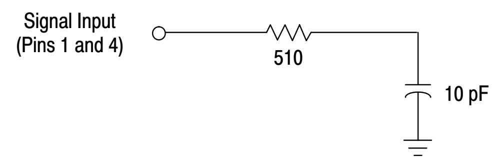
The output signal is taken from Pins 6 and 12 either balanced or single−ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single−ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source−tuned circuits that cause the oscillation.



An alternate method for low−frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

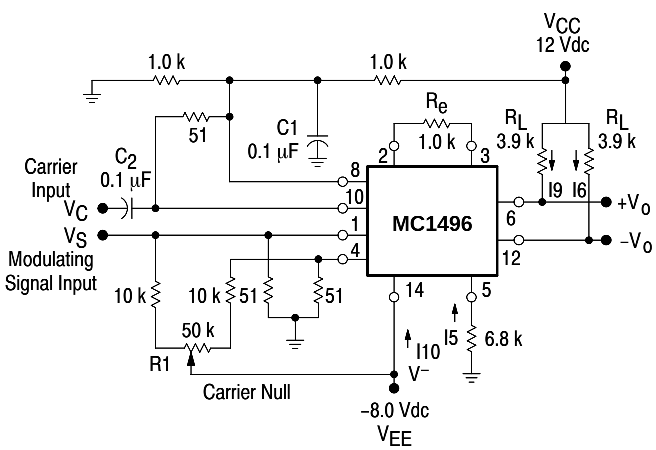
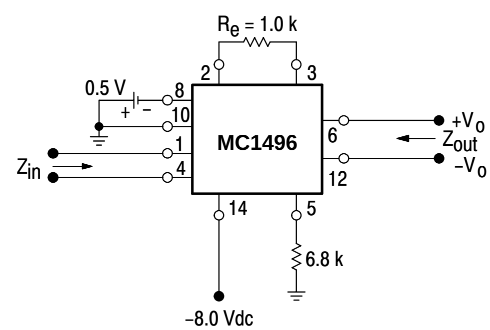


Figure 5. Carrier Rejection and Suppression



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

Figure 6. Input−Output Impedance

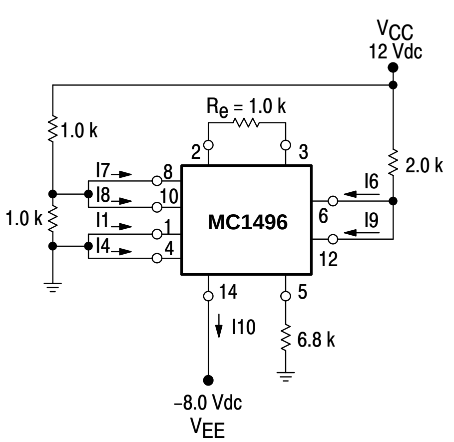


Figure 7. Bias and Offset Currents

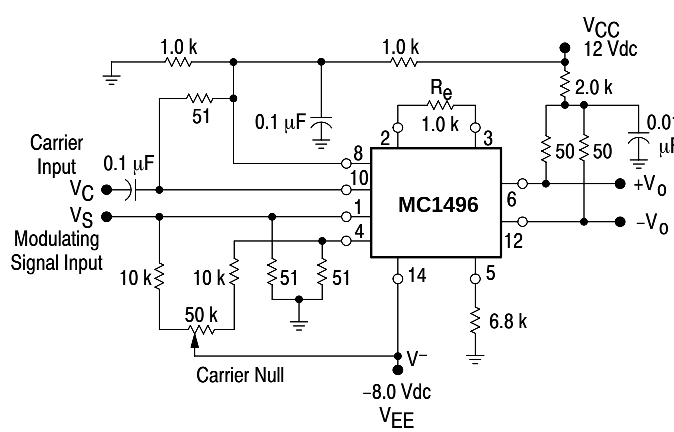


Figure 8. Transconductance Bandwidth

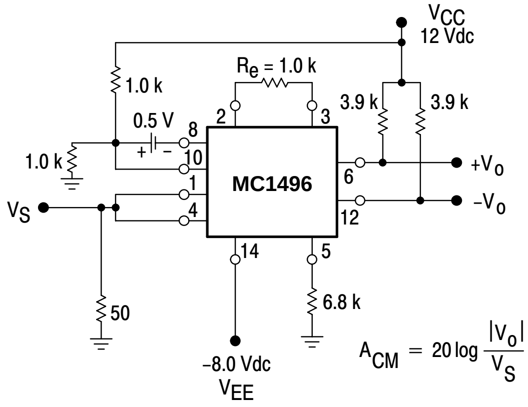


Figure 9. Common Mode Gain

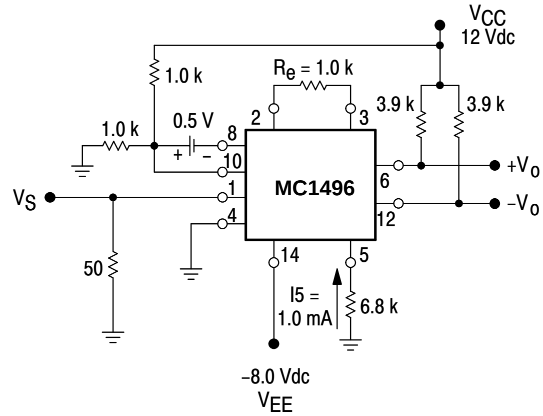


Figure 10. Signal Gain and Output Swing

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

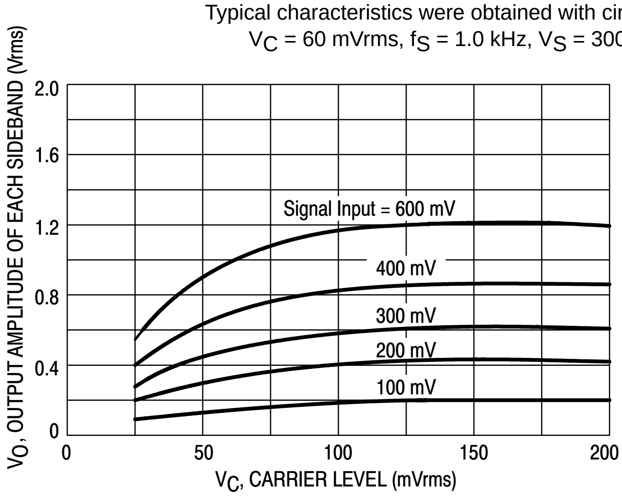


Figure 11. Sideband Output versus Carrier Levels

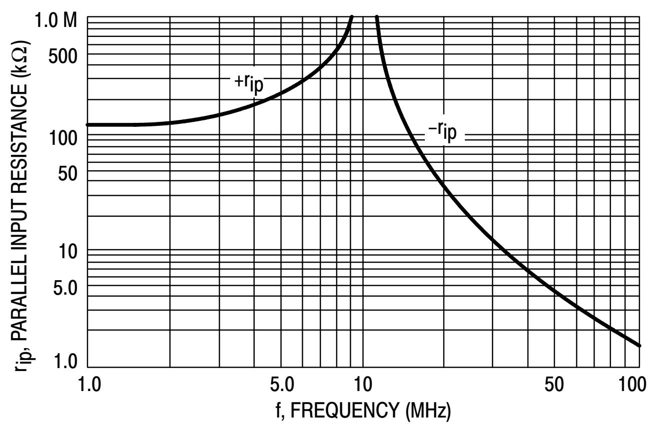


Figure 12. Signal−Port Parallel−Equivalent Input Resistance versus Frequency

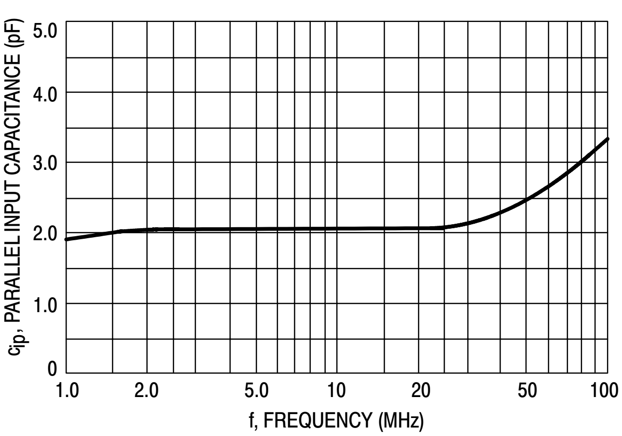


Figure 13. Signal−Port Parallel−Equivalent Input Capacitance versus Frequency

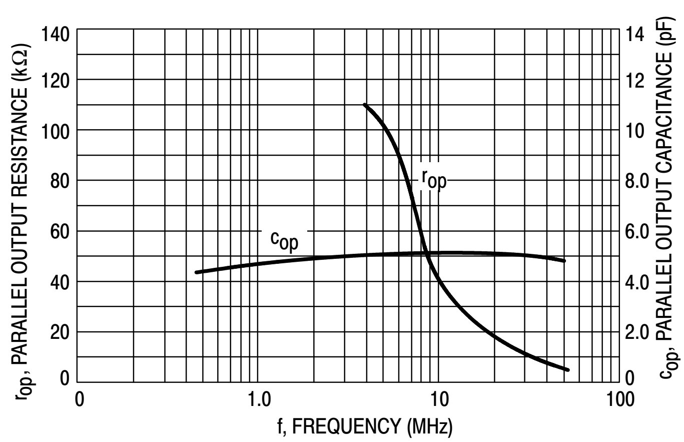


Figure 14. Single−Ended Output Impedance versus Frequency

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

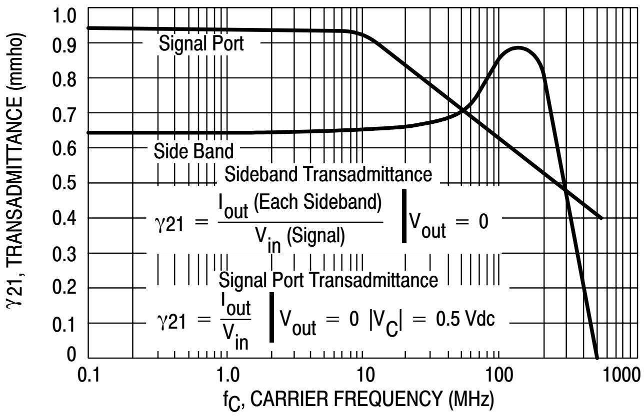


Figure 15. Sideband and Signal Port Transadmittances versus Frequency

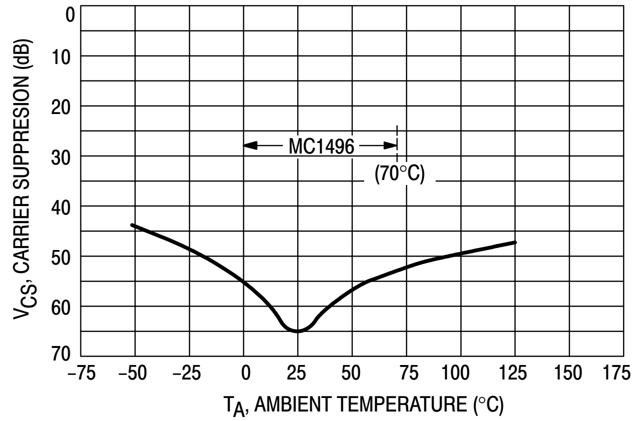


Figure 16. Carrier Suppression versus Temperature

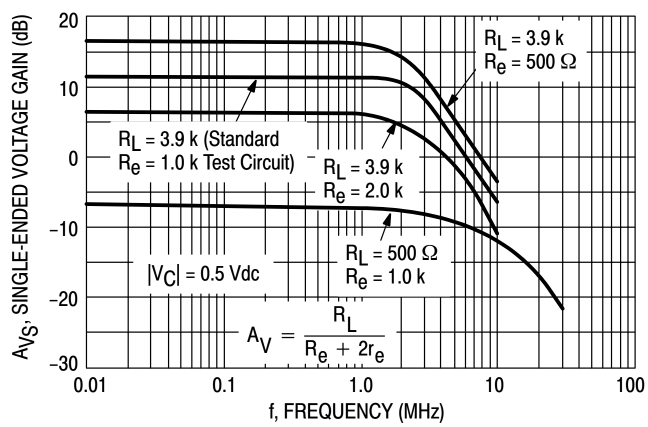


Figure 17. Signal−Port Frequency Response

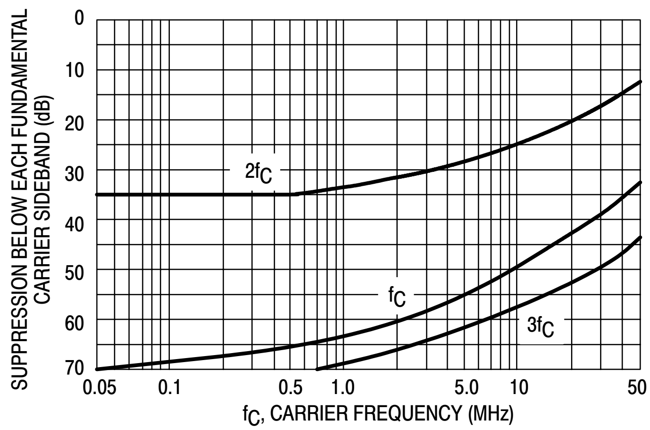


Figure 18. Carrier Suppression versus Frequency

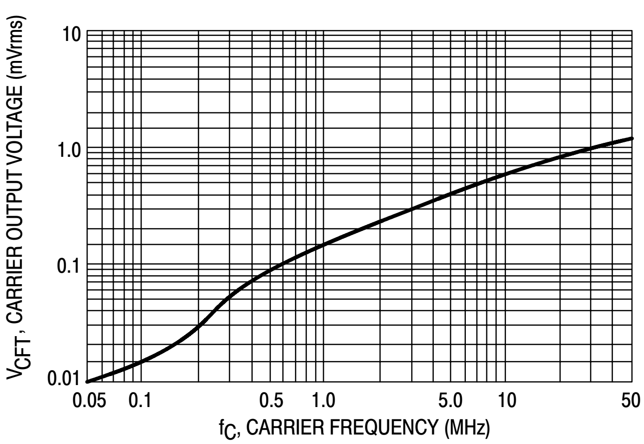


Figure 19. Carrier Feedthrough versus Frequency

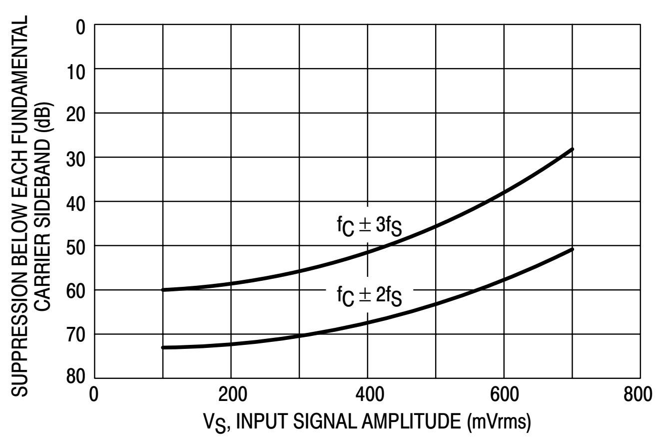


Figure 20. Sideband Harmonic Suppression versus Input Signal Level

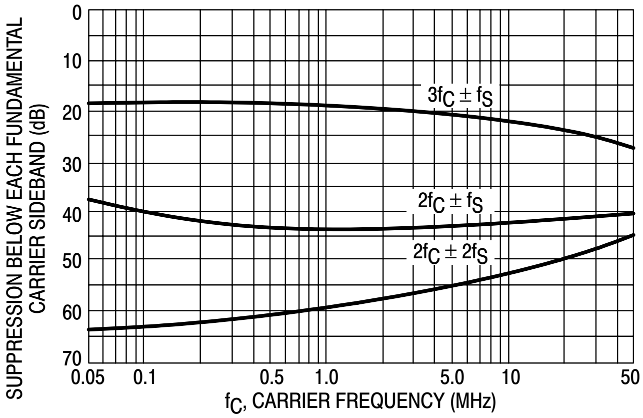


Figure 21. Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

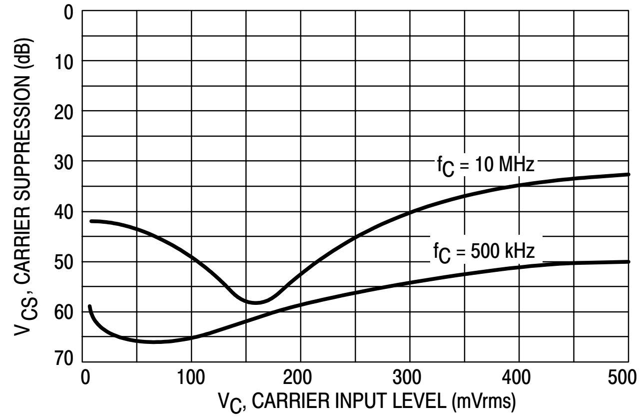


Figure 22. Carrier Suppression versus Carrier Input Level

OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross−coupled so that full−wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low−level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high−level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I5)\,(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

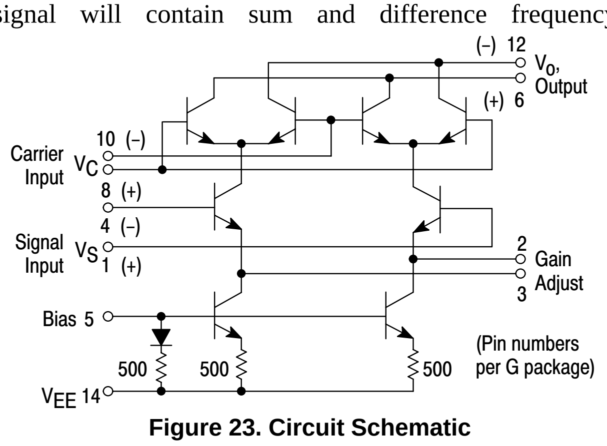


Figure 23. Circuit Schematic

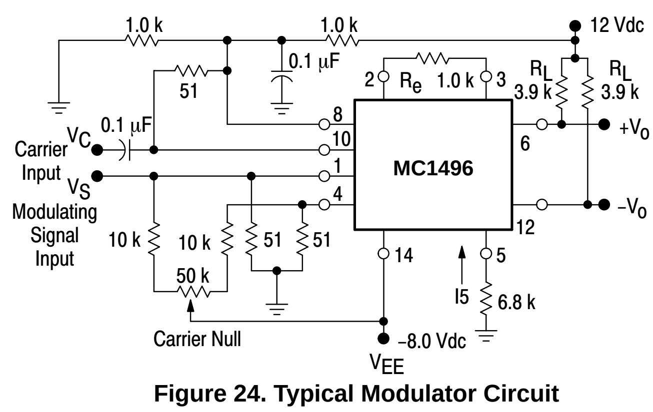


Figure 24. Typical Modulator Circuit

Table 1. Voltage Gain and Output Frequencies

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low−level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High−level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low−level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High−level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

2. Low−level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
3. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude ofeach of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
4. All gain expressions are for a single−ended output. For a differential output connection, multiply each expression by two.
5. R_L = Load resistance.
6. R_E = Emitter resistance between Pins 2 and 3.
7. r_e = Transistor dynamic emitter resistance, at 25°C; $re \approx \frac{26\ mV}{I_5\ (mA)}$
8. K = Boltzmann′s Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low−level modulating signal input and the following carrier input conditions:

1) Low−level dc
2) High−level dc
3) Low−level ac
4) High−level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 25 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 26 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 26 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 27.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 28).

This product detector has a sensitivity of 3.0 μV and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on Pins 8 and 10 should be increased to 1.0 μF. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 29 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 30 and 31 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1496 will function as a phase detector. High−level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

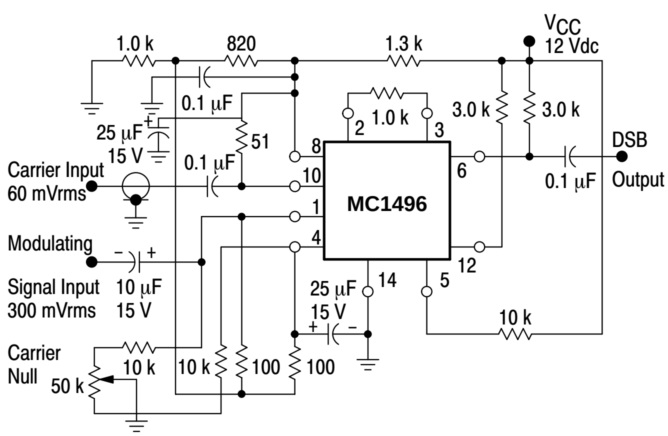


Figure 25. Balanced Modulator
(12 Vdc Single Supply)

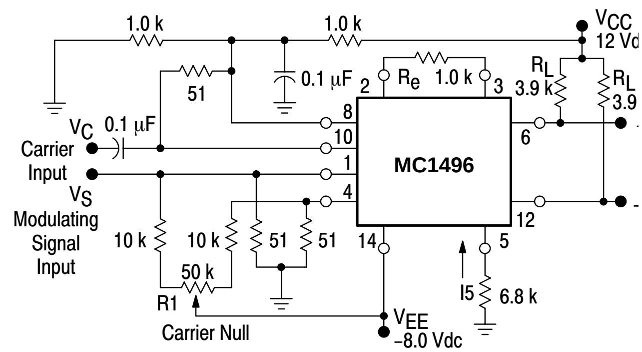


Figure 26. Balanced Modulator−Demodulator

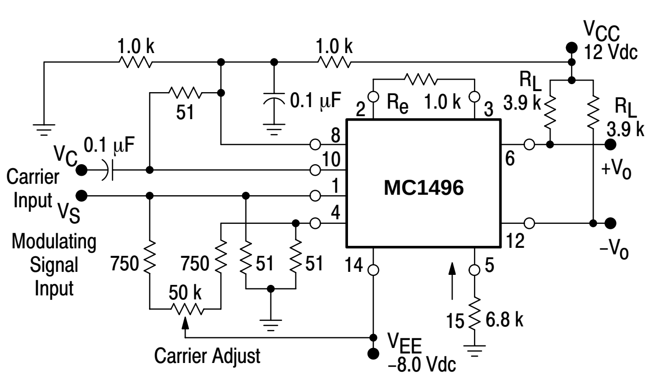


Figure 27. AM Modulator Circuit

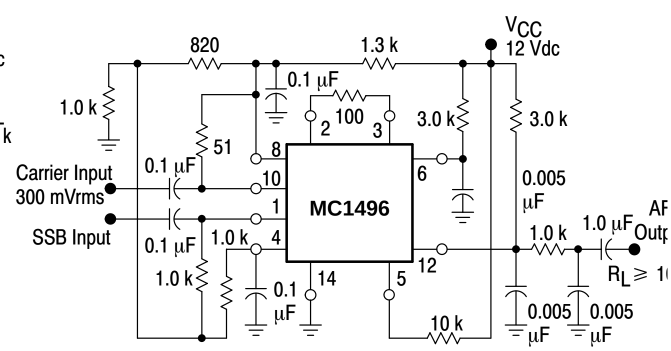
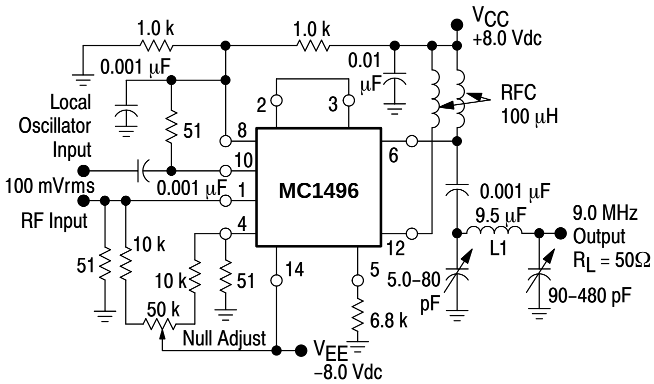


Figure 28. Product Detector
(12 Vdc Single Supply)



L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44−6 Toroid Core.

Figure 29. Doubly Balanced Mixer (Broadband Inputs, 9.0 MHz Tuned Output)

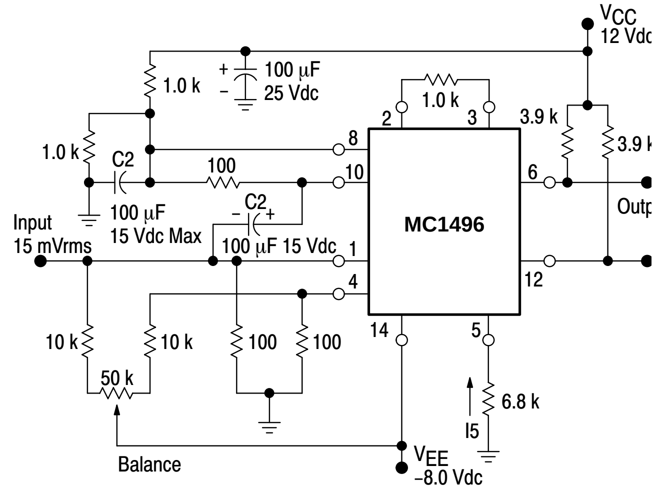


Figure 30. Low−Frequency Doubler

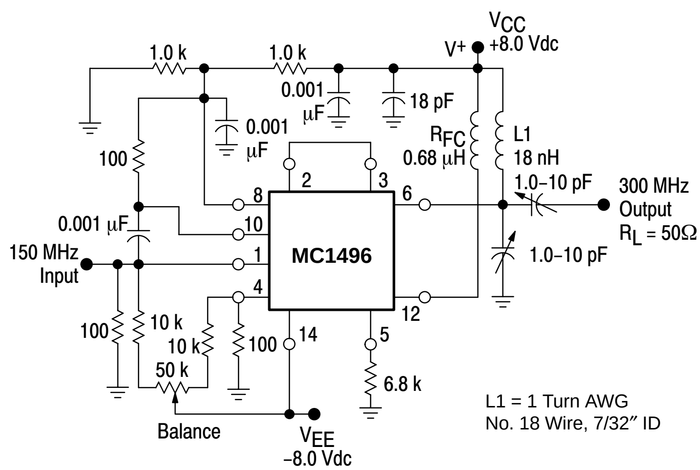
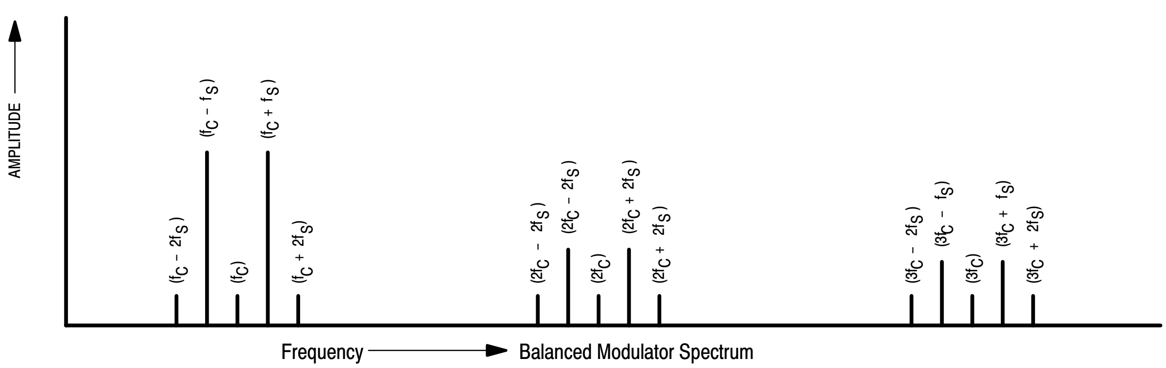


Figure 31. 150 to 300 MHz Doubler



DEFINITIONS

f_C	Carrier Fundamental	$f_C \pm nf_S$	Fundamental Carrier Sideband Harmonics
f_S	Modulating Signal	nf_C	Carrier Harmonics
$f_C \pm f_S$	Fundamental Carrier Sidebands	$nf_C \pm nf_S$	Carrier Harmonic Sidebands

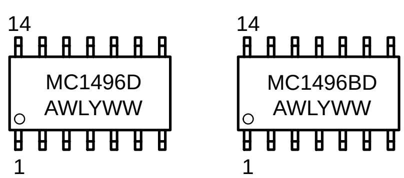
ORDERING INFORMATION

Device	Package	Shipping†
MC1496D	SOIC−14	55 Units/Rail
MC1496DR2	SOIC−14	2500 Tape & Reel
MC1496DR2G	SOIC−14 (Pb−Free)	2500 Tape & Reel
MC1496P	PDIP−14	25 Units/Rail
MC1496PG	PDIP−14 (Pb−Free)	25 Units/Rail
MC1496P1	PDIP−14	25 Units/Rail
MC1496BD	SOIC−14	55 Units/Rail
MC1496BDR2	SOIC−14	2500 Tape & Reel
MC1496BP	PDIP−14	25 Units/Rail

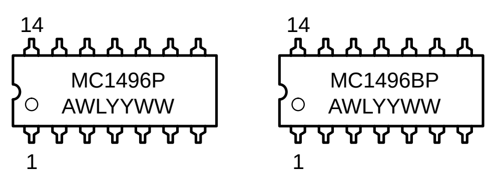
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646

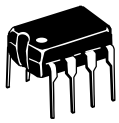


A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week

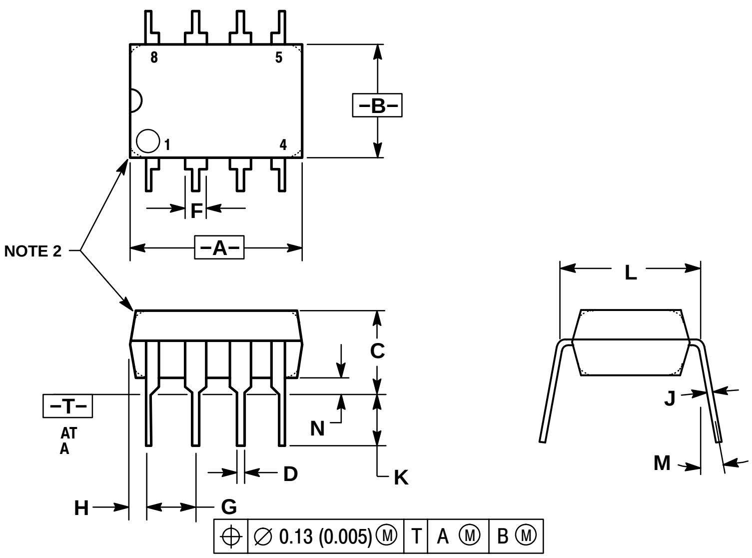
CHAPTER 3
Case Outlines and Package Dimensions

8 LEAD PDIP
CASE 626−05
ISSUE L

DATE 09/29/2000



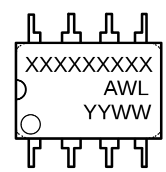
CA 11

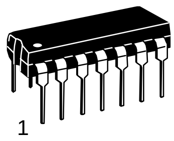


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	M M T		C	
M	M	MA	M	MA
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
	2.54 BSC		0.100 BSC	
	0.76	1.27	0.030	0.050
	0.20	0.30	0.008	0.012
	2.92	3.43	0.115	0.135
	7.62 BSC		0.300 BSC	
M	---	10†	---	10†
	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

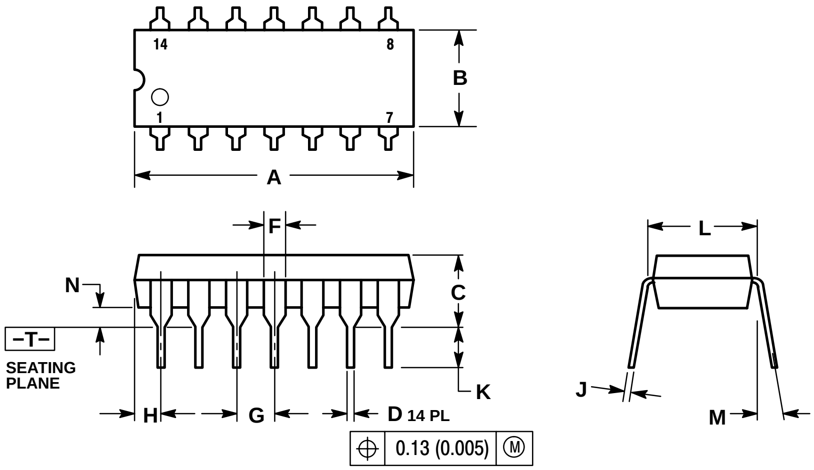




SCALE 1:1

PDIP−14
CASE 646−06
ISSUE N

DATE 04 MAY 2004

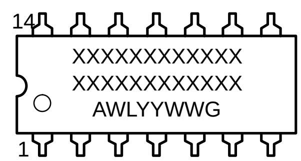


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 †	−−−	10 †
N	0.015	0.039	0.38	1.01

STYLES ON NEXT PAGE

GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ◦”, may or may not be present.

PDIP−14
CASE 646−06
ISSUE N

DATE 04 MAY 2004

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

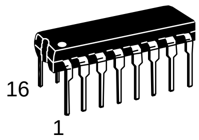
STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

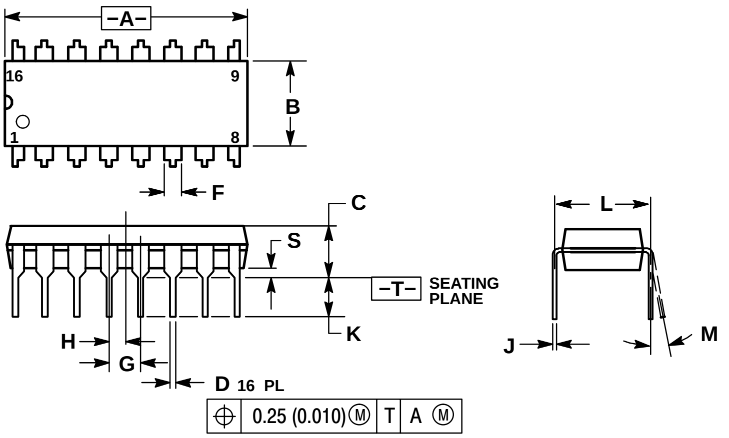
STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE



SCALE 1:1

PDIP−16
CASE 648−08
ISSUE T

DATE 04 MAY 2004



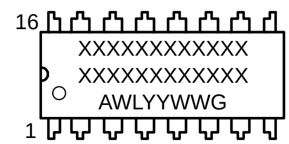
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 †	10 †	0 †	10 †
S	0.020	0.040	0.51	1.01

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*

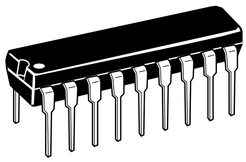


XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

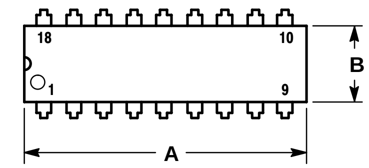
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ◦”, may or may not be present.

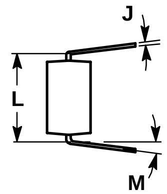
18 LEAD PDIP
CASE 707−02
ISSUE D

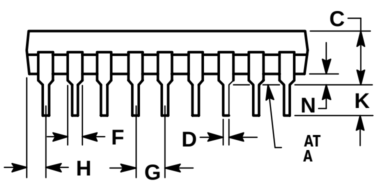
DATE 09/29/2000

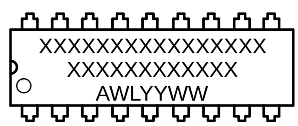


CA 1 1







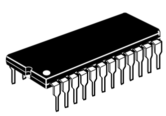


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

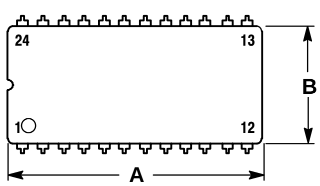
	C		M M T	
M	M	MA	M	MA
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
	0.100 BSC		2.54 BSC	
	0.040	0.060	1.02	1.52
	0.008	0.012	0.20	0.30
	0.115	0.135	2.92	3.43
	0.300 BSC		7.62 BSC	
M	0 †	15 †	0 †	15 †
	0.020	0.040	0.51	1.02

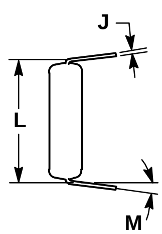
24 LEAD PDIP
CASE 709−02
ISSUE D

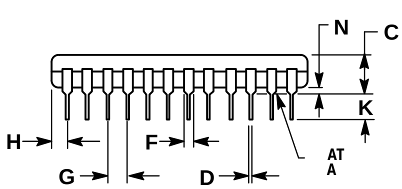
DATE 09/29/2000

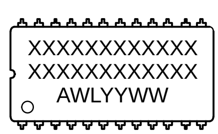


CA 1 2





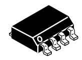




NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	C		M M T	
M	M	MA	M	MA
A	1.235	1.265	31.37	32.13
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
	0.100 BSC		2.54 BSC	
	0.065	0.080	1.65	2.03
	0.008	0.015	0.20	0.38
	0.115	0.135	2.92	3.43
	0.600 BSC		15.24 BSC	
M	0 †	15 †	0 †	15 †
	0.020	0.040	0.51	1.02

8

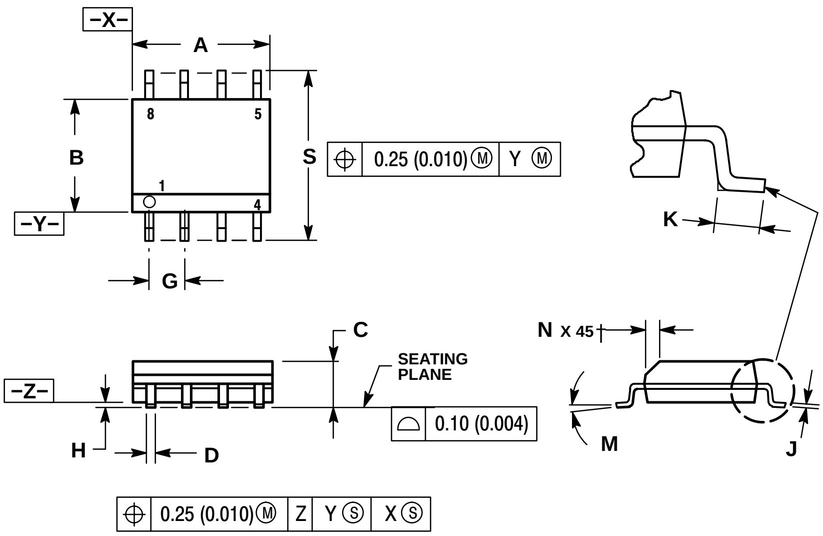


1

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AD

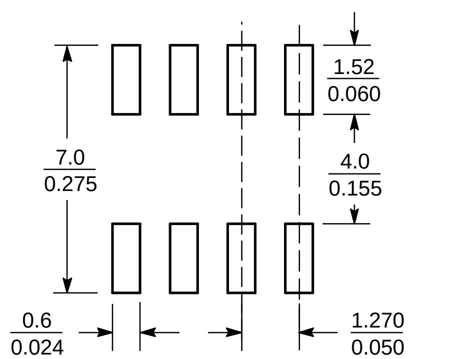
DATE 18 NOV 2004



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

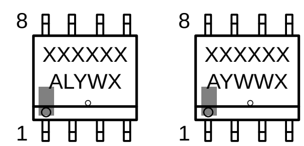
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

RECOMMENDED FOOTPRINT



SCALE 6:1 (mm / inches)

GENERIC MARKING DIAGRAM*



IC   Discrete

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W, WW = Work Week
° = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

STYLES ON NEXT PAGE

SOIC−8 NB
CASE 751−07
ISSUE AD

DATE 18 NOV 2004

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

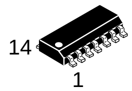
STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

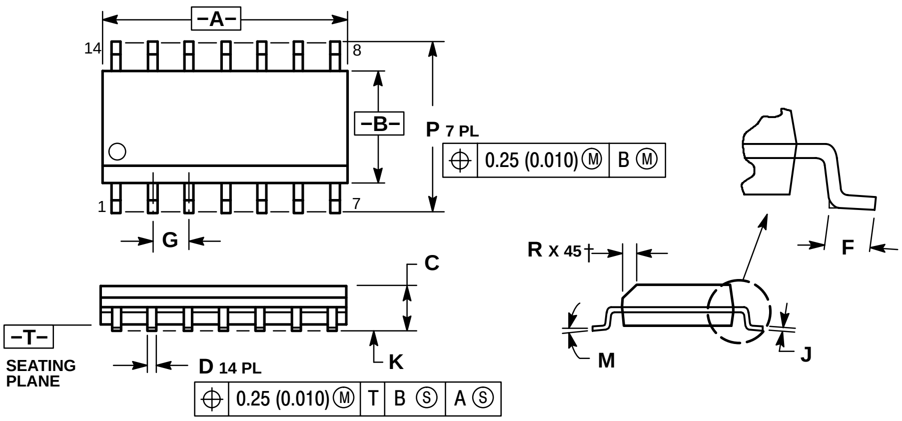
STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

SOIC−14
CASE 751A−03
ISSUE G

DATE 30 APR 2004



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 †	7 †	0 †	7 †
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

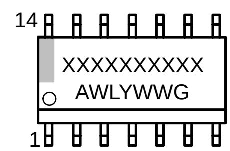
STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

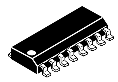
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

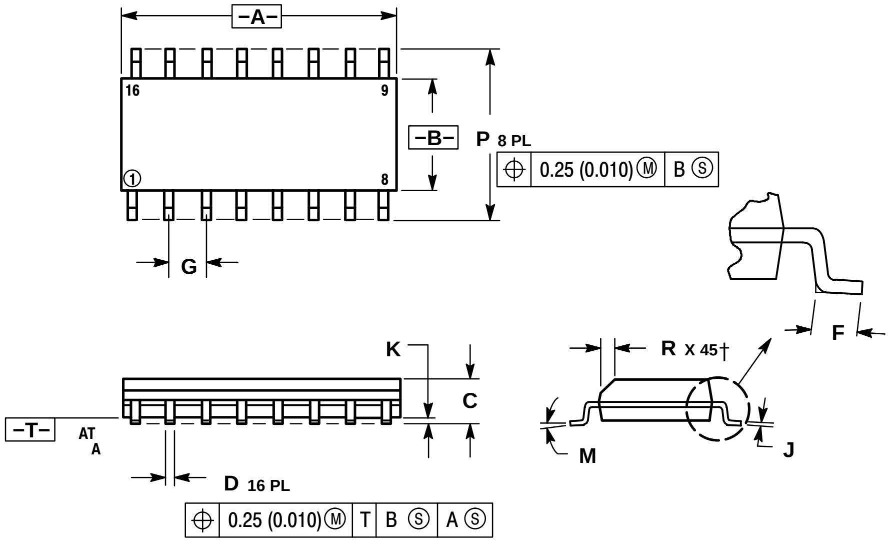
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ °”, may or may not be present.



CA 11

SOIC
CASE 751B−05
ISSUE J

DATE 04/28/1993



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	M M T		C	
M	M	MA	M	MA
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
	1.27 BSC		0.050 BSC	
	0.19	0.25	0.008	0.009
	0.10	0.25	0.004	0.009
M	0†	7†	0†	7†
	5.80	6.20	0.229	0.244
	0.25	0.50	0.010	0.019

STYLES ON NEXT PAGE

SOIC
CASE 751B−05
ISSUE J

DATE 04/28/1993

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

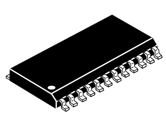
STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

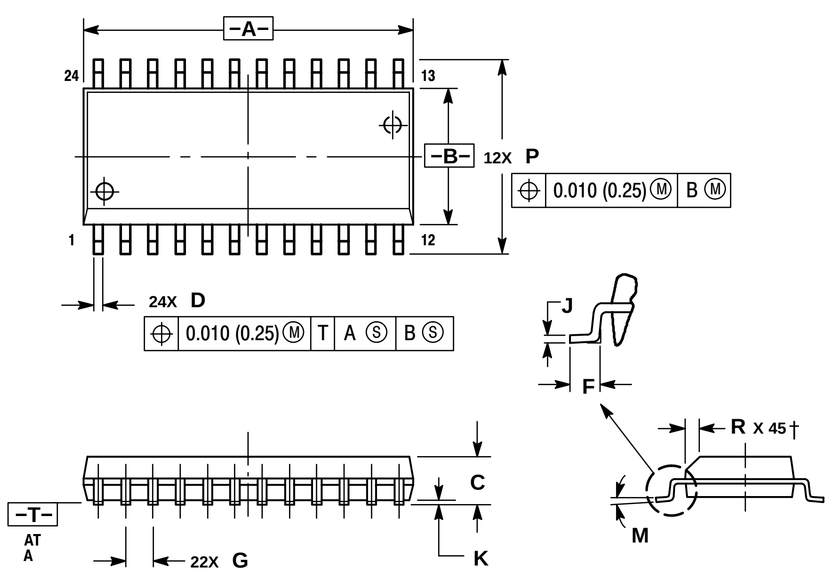
STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOIC
CASE 751E−04
ISSUE E

DATE 06/18/1993

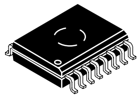


CA 1 1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

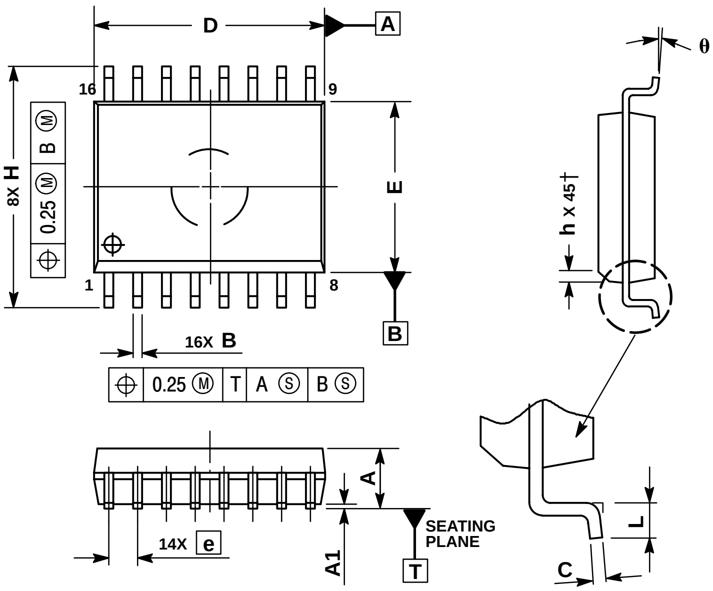
	M M T		C	
M	M	MA	M	MA
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
	1.27 BSC		0.050 BSC	
	0.23	0.32	0.009	0.013
	0.13	0.29	0.005	0.011
M	0†	8†	0†	8†
	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029



SO−16 WB
CASE 751G−03
ISSUE C

DATE 30 APR 2004

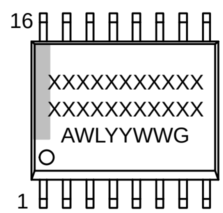
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 †	7 †

GENERIC MARKING DIAGRAM*

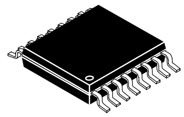


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

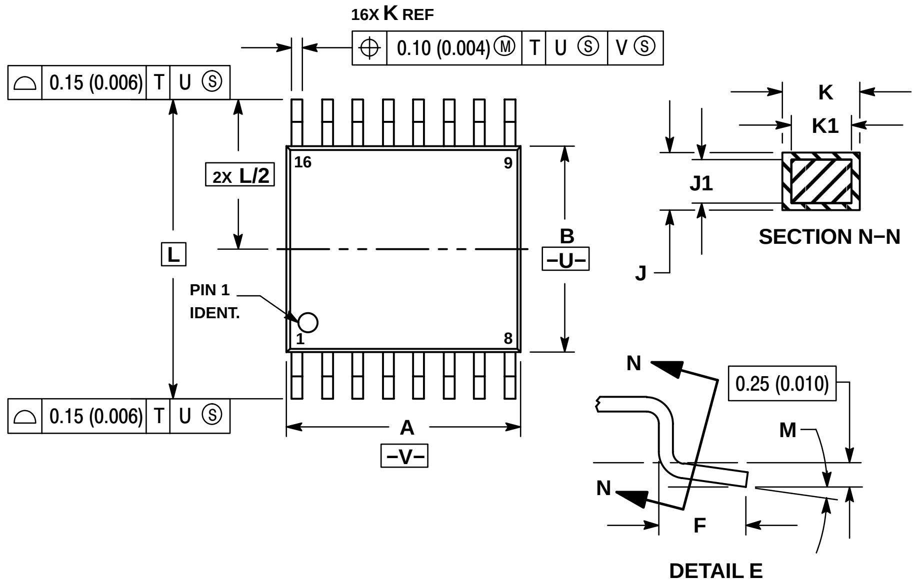
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ◦”, may or may not be present.

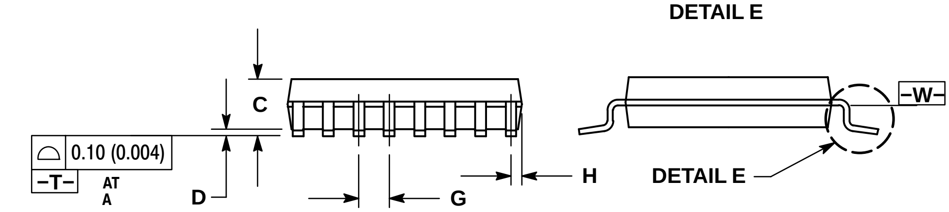
TSSOP
CASE 948F−01
ISSUE O

DATE 12/20/1994



CA 2 1





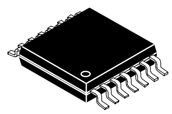
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

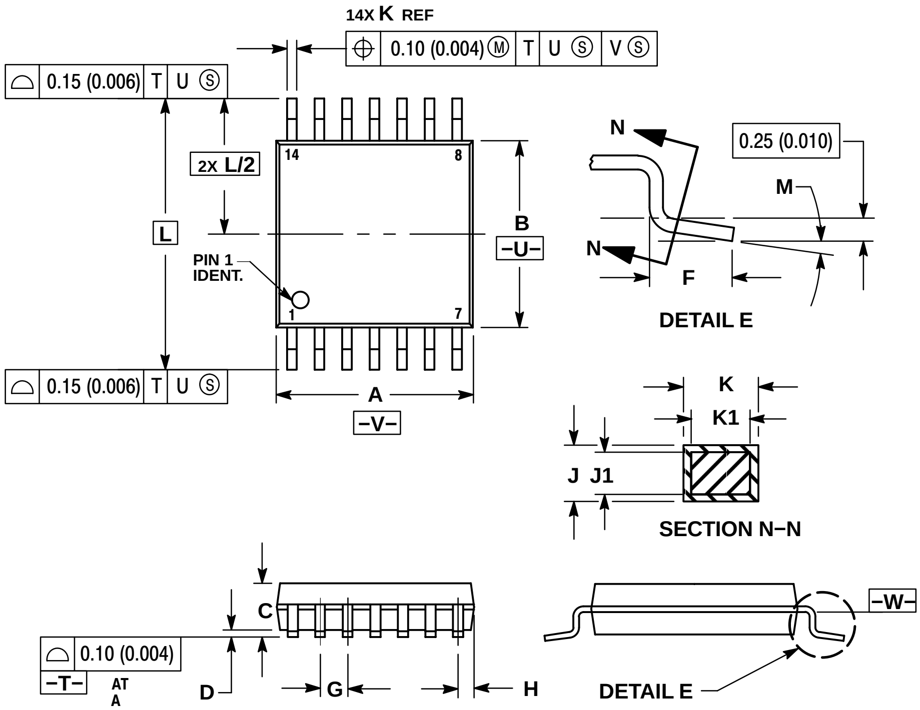
	M M T		C	
M	M	MA	M	MA
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
	0.65 BSC		0.026 BSC	
	0.18	0.28	0.007	0.011
	0.09	0.20	0.004	0.008
1	0.09	0.16	0.004	0.006
	0.19	0.30	0.007	0.012
1	0.19	0.25	0.007	0.010
	6.40 BSC		0.252 BSC	
M	0 †	8 †	0 †	8 †

TSSOP
CASE 948G−01
ISSUE O

DATE 12/07/1994



CA 21



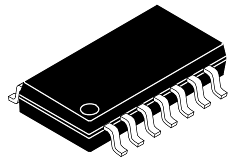
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

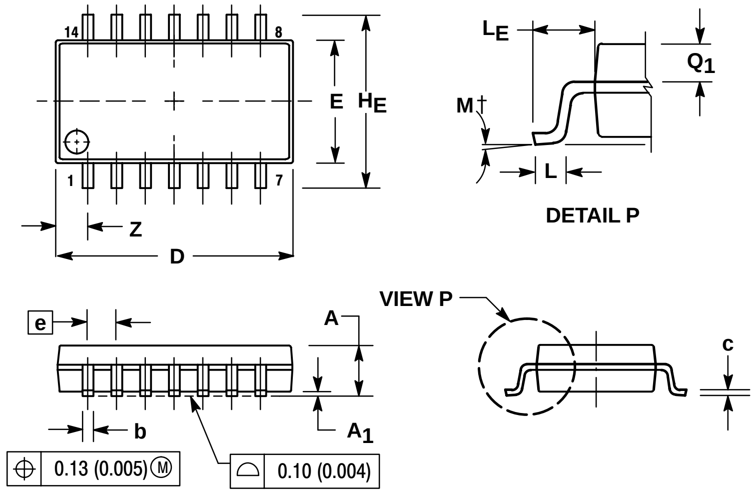
	M M T		C	
M	M	MA	M	MA
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
	0.65 BSC		0.026 BSC	
	0.50	0.60	0.020	0.024
	0.09	0.20	0.004	0.008
1	0.09	0.16	0.004	0.006
	0.19	0.30	0.007	0.012
1	0.19	0.25	0.007	0.010
	6.40 BSC		0.252 BSC	
M	0†	8†	0†	8†

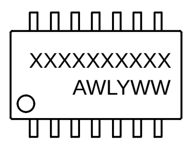
SOEIAJ−14
CASE 965−01
ISSUE O

DATE 01/19/1994



CA 21



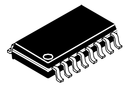


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

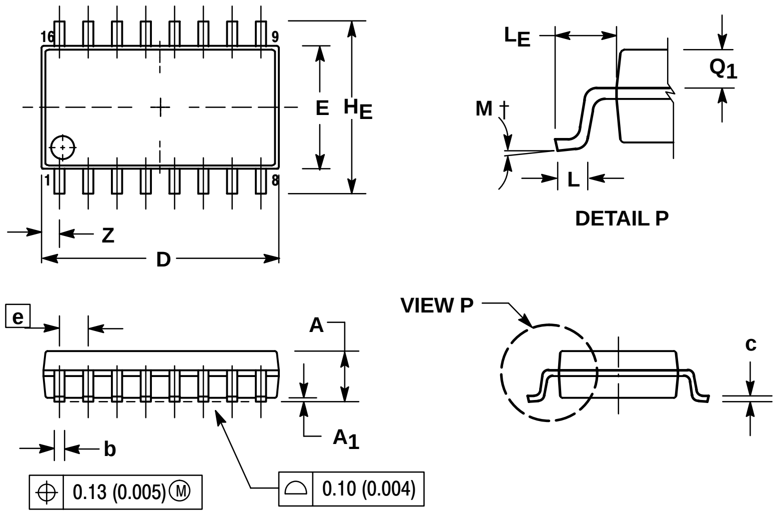
	M M T		C	
M	M	MA	M	MA
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
	0.35	0.50	0.014	0.020
	0.18	0.27	0.007	0.011
	9.90	10.50	0.390	0.413
	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
	7.40	8.20	0.291	0.323
0 50	0.50	0.85	0.020	0.033
	1.10	1.50	0.043	0.059
M	0 †	10 †	0 †	10 †
1	0.70	0.90	0.028	0.035
	---	1.42	---	0.056

SOEIAJ−16
CASE 966−01
ISSUE O

DATE 01/19/1994



CA 1 1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	M M T		C	
M	M	MA	M	MA
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
	0.35	0.50	0.014	0.020
	0.18	0.27	0.007	0.011
	9.90	10.50	0.390	0.413
	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
	7.40	8.20	0.291	0.323
	0.50	0.85	0.020	0.033
	1.10	1.50	0.043	0.059
M	0 †	10 †	0 †	10 †
1	0.70	0.90	0.028	0.035
	---	0.78	---	0.031

CHAPTER 4
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