Practical RTD Interface Solutions

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1.0 Purpose

This application note is intended to review Resistance Temperature Devices and commonly used interfaces for them.

In an industrial environment, longitudinal noise in a wide spectrum may exist requiring good common mode rejection at the circuit interface.

A brief discussion of longitudinal balance and how to improve the interface response to longitudinal noise is presented.

Circuit configurations that provide better longitudinal balance along with design recommendations for optimal performance are presented.

2.0 RTD Review

2.1 RTD DESCRIPTION

An RTD (Resistance Temperature Device) can be fabricated in several ways, but the most common are based on the temperature characteristics of Platinum. It has a predictable temperature characteristic that can be controlled and configured in a number of different ways.

Platinum wire wound around glass or ceramic and platinum thin film chip designs are common.

Many kinds of RTD designs are available to designers but this discussion will be limited to some of the most common.

2.2 RTD STANDARDS

An international standard, EN 60751, defines the detailed electrical characteristics of platinum temperature sensors. The standard contains tables of resistance vs temperature, tolerances, curves and temperature ranges.

2.3 RTD SPECIFICATIONS

Three common RTDs are the PT100, PT500 and the PT1000. The 100, 500 and 1000 represent the resistances of each at 0°C. From −200°C to 0°C their Resistance vs Temperature characteristic is described by a 3rd order polynomial

$$R=R_0(1+At+Bt^2+C(t-100)t^3)$$

From 0°C to 850°C the device is described by a 2nd order polynomial:

$$R=R_0(1+At\_Bt^2)$$

The coefficients are : $A = 3.9083\times10^{-3}$°C^{-1} $B = -5.775\times10^{-7}$°C^{-1} $C = -4.183\times10^{-12}$°C^{-1}

2.4 RECOMMENDATIONS

- For precision applications, remember that these sensors are not exactly linear. The above polynomials can be used in a microcomputer after the information has been digitized to get accurate temperature readings.
- For precision applications, use the higher valued resistance sensors for increased sensitivity and resolution (PT1000).
- Higher resistance sensors may require higher single supply voltage, or even 2 supplies. Allow sufficient headroom for linear performance.
- Choose current drive levels that minimize sensor self heating. Acceptable current levels for each type of sensor and allowable measurement error can be easily calculated.
- When choosing a sampling interval for the data acquisition system, remember that these sensors have response times.

3.0 2, 3 and 4 Wire Configurations

Temperature sensors can be configured in several ways:

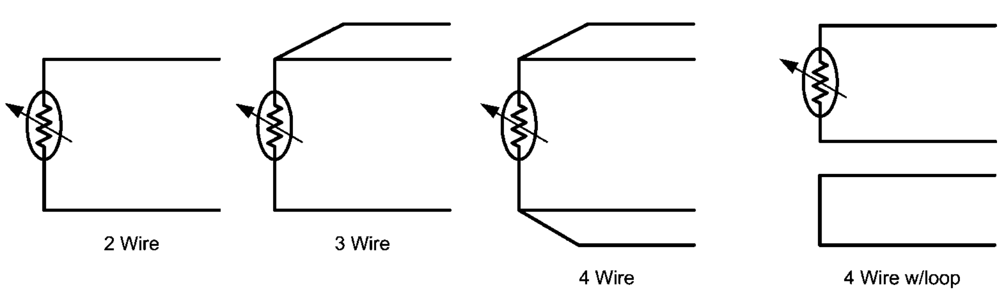

FIGURE 1. Standard Schematic

2 wire – This configuration is used when the parasitic resistance of the connection wires is known and doesn't change. This can be compensated for by a computation later in the signal path.

3 wire – This configuration allows the designer to monitor one side of the current loop with a Kelvin connection. The voltage drop in the resistance of the loop is measured and compensated for. For users with only three wires available.

4 wire – This configuration allows the designer to monitor both sides of the current loop with a Kelvin connection on both sides of the RTD. This yields another measure of precision as well as compensation for wires of differing lengths.

4 wire with loop – This configuration is similar to the 4 wire but here the designer has options about how to measure the loss in the loop. The resistance of the wire can be measured independently of the RTD loop. The designer does not need to rely on good Kelvin connections at the RTD. For that reason, more precision and reliability can be achieved.

3.1 4 WIRE INTERFACE

Figure 1 is a commonly used circuit to excite an RTD.

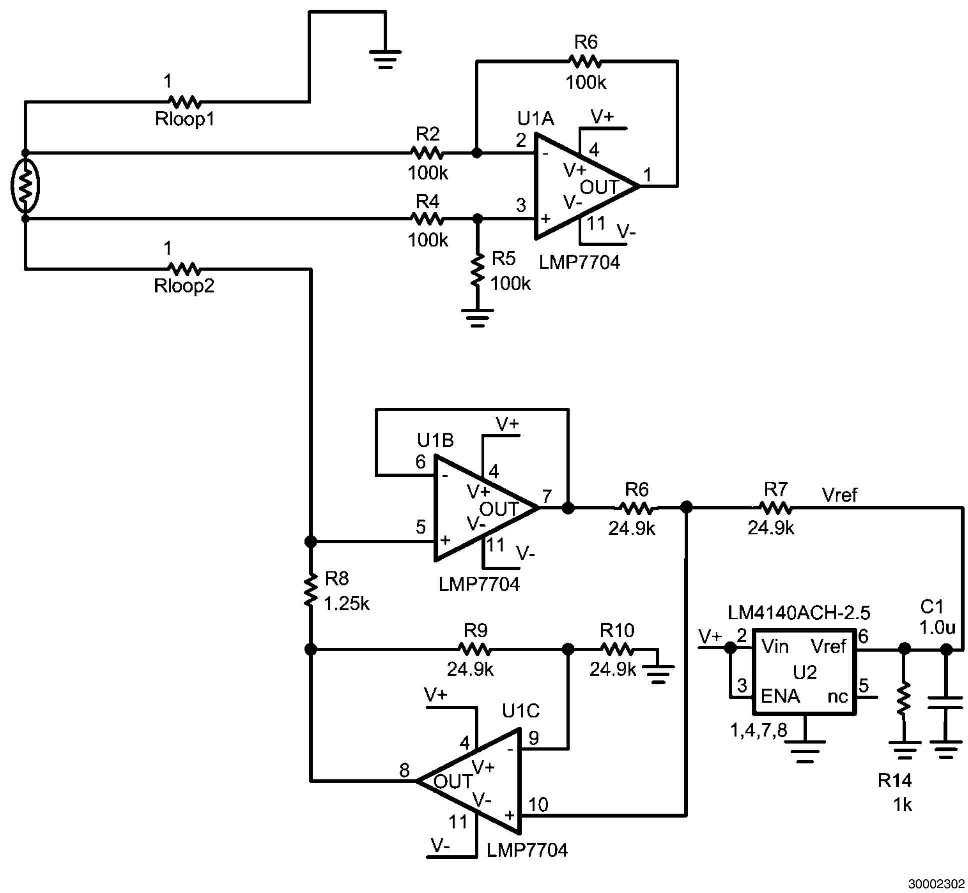

FIGURE 2.

With a constant current driver, the self heating of the RTD is easily controlled. The higher sensitivity RTDs (higher resistance) require lower current drive for good accuracy and minimal self heating.

The LM4140 is a high precision, low noise voltage reference.

The LMP7704 is a quad, precision, CMOS input, RRIO, wide supply range amplifier.

3.1.1 Circuit Theory

3.1.1.1 Current Source

In *Figure 1*, U1B and U1C constitute a boot strapped current source where

$$I = \frac{V_{ref}}{R8}$$

Because the input impedance of U1C pin 5 is so high, the current flowing in R6 is approximately equal to the current flowing in R7.

$$V_{IN}U1C = \frac{V_{ref} - V_{OUT}U1B}{2} + V_{OUT}U1B \;\therefore\; V_{IN}U1C = \frac{V_{ref} + V_{OUT}U1B}{2}$$

$$V_{OUT}U1C = 2\left[\frac{V_{ref} + V_{OUT}U1B}{2}\right] = V_{ref} + V_{OUT}U1B$$

$$V_{OUT}U1B = V_{IN}U1B$$

$$VR8 = V_{OUT}U1C - V_{IN}U1B$$

$$VR8 = V_{ref} + V_{OUT}U1B - V_{IN}U1B$$

$$\therefore$$

$$VR9 = V_{ref} \text{ (No matter what } V_{IN}U1B \text{ is)}$$

3.1.1.2 Differential Receive Amplifier.

U1A is a Kelvin connected differential amplifier, i.e. connected to the pair of wires that does not carry excitation current because of the high input impedance of the differential amplifier. Actually, some small amount of current does flow into these inputs and should be accounted for when setting the current.

This Kelvin connection eliminates any error caused by the wire resistance in the current loop.

3.2 RECOMMENDATIONS

- This circuit will accommodate a resistance sensor that ranges from about 80Ω to 1.1k in a single 5V supply.
- Higher resistance ranges will require higher VCC.
- Any resistances lower than 80Ω or so will require a negative supply to accurately provide outputs close to 0.0 Vdc.
- This circuit will not work well in the presence of significant longitudinal voltages on long wire loops to the RTD. For this kind of environment, use balanced circuits.
- Use Resistor networks to keep like values on opposite pairs closely matched.
- Spice models are available for this OP AMP at www.national.com. By using SPICE simulations, good resistor choices can be made well in advance.

4.0 Longitudinal Balance

Whenever a sensor is separated from the electronic circuit interface by more than a meter or so, and the environment contains common mode noise, it is important to consider balance. If the lines are well balanced, and the receiver is differential, they will reject common mode noise.

4.1 UNDERSTANDING BALANCE

A simple way to look at balance on cable lines is by checking the impedance to ground from each conductor. The DC circuit is a good place to begin.

When determining the balance for a pair of wires, find the equivalent impedance from each wire to ground. In this case, we will just look at the DC circuit, so the equivalent DC resistance from each wire to ground will suffice; R1 to ground on one side, and R2 on the other.

$$BAL_{dB} = 20 * \log\left[\frac{R1 - R2}{R1 + R2}\right]$$

This familiar sum and difference formula is a good way to compare 2 impedances (R1 and R2). The result is a large number in dB for resistors that are close in value. You can put the sum on top and the difference on the bottom if you wish; it only changes the sign of the result. The idea is to get a large number.

If this analysis is applied to *Figure 2* and *Figure 3*, the balance is non existent. It shows a high impedance current source on one side and ground on the other.

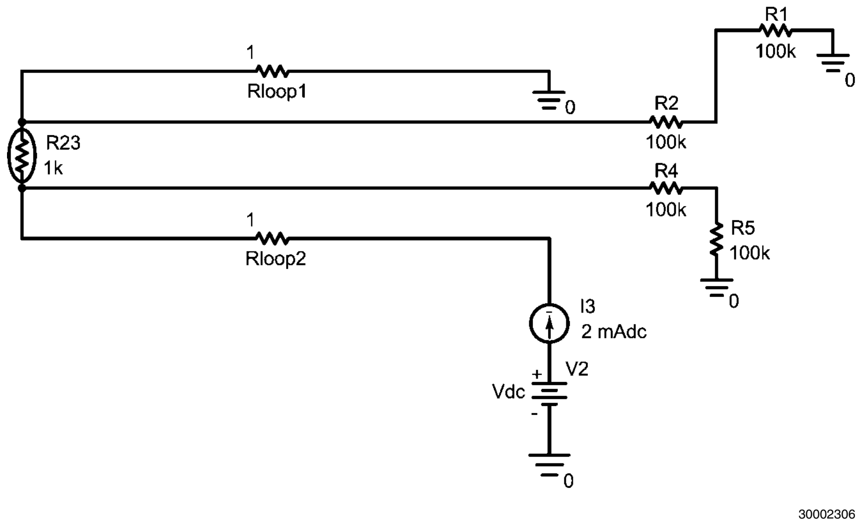

FIGURE 3. Equivalent Balance Circuit for Figure 2

The current carrying loop will convert common mode noise to differential noise in the voltage measuring loop because the resistances to ground are so different. BAL = 0.0

This noise will appear on the differential inputs of the receiver and get into the sampling system. By adding a few components, good balance can be achieved.

5.0 Balanced 2 and 4 Wire Interfaces

In *Figure 4*, a 634Ω resistor (R1) and a low pass filter (U1C, R7, R8, C1 and C2) are added to improve the input balance. The voltage reference is halved and R10 is halved (634Ω) to keep the voltage swings in the loop well within the 10 VDC supply range. The DC circuit is unaffected.

Looking back into the loop current circuit, common mode voltages see a 634 to ground on one side and a 634Ω resistor to the output of U1D on the other. The output of U1D now looks like a good AC ground in the stop band frequencies of the low pass filter of U1C. The Salen Key low pass filter F3 db is chosen to attenuate frequencies of 60 Hz, 120 Hz and 180 Hz. At these frequencies excellent CMR is maintained. These are common longitudinal noise sources in industrial environments.

For higher frequency CMR, higher frequency OP AMPs should be used.

At DC, the circuit is a high impedance current source. See *Figure 5*.

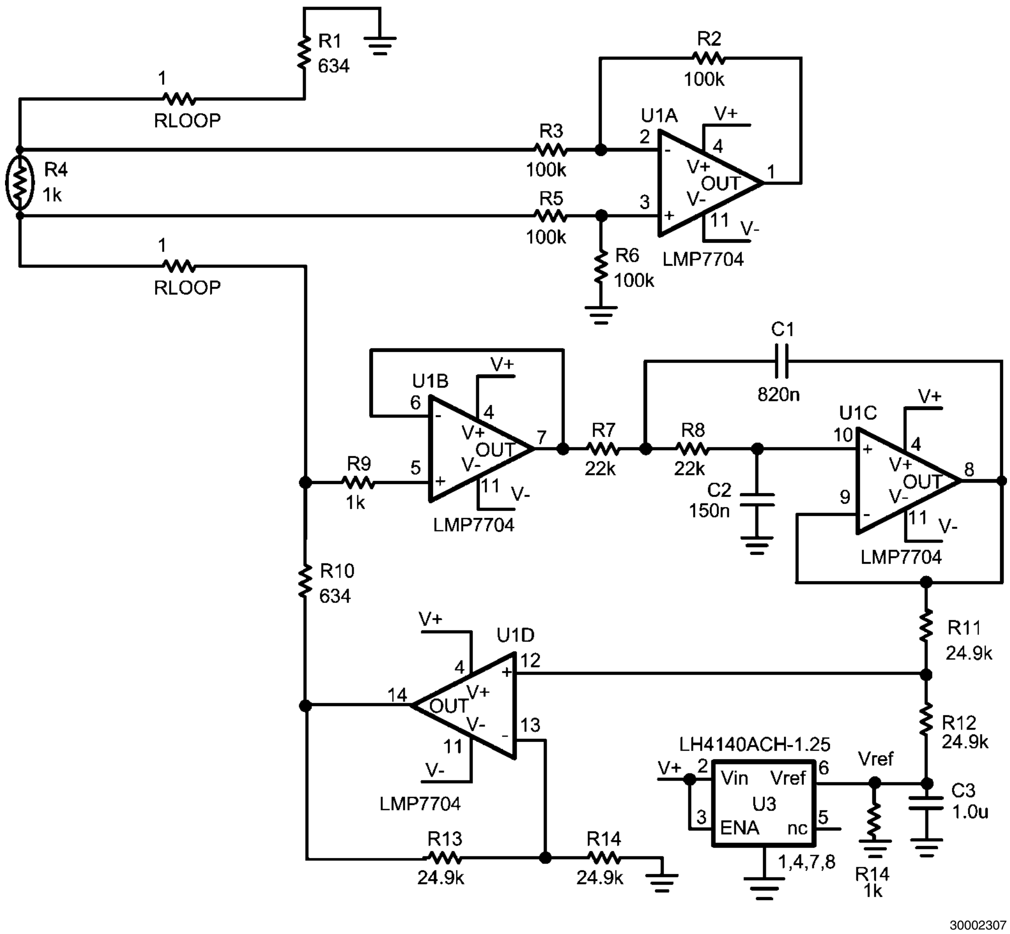

FIGURE 4.

5.1 RECOMMENDATIONS

- Depending on the resistance range of the RTD, the voltage supplies may need to change.
- For this voltage reference, the V+ must be kept to 5 VDC.
- For very low resistance range RTDs, a negative rail of −2 VDC will work nicely with a positive rail of 10.0 VDC to accommodate the higher resistance values.
- A series resistor is added to U1B,IN+ to add isolation from the cable.
- Spice models are available for these OP AMPS at www.national.com. By using SPICE simulations, good resistor choices can be made well in advance.

5.2 BALANCED 4 WIRE

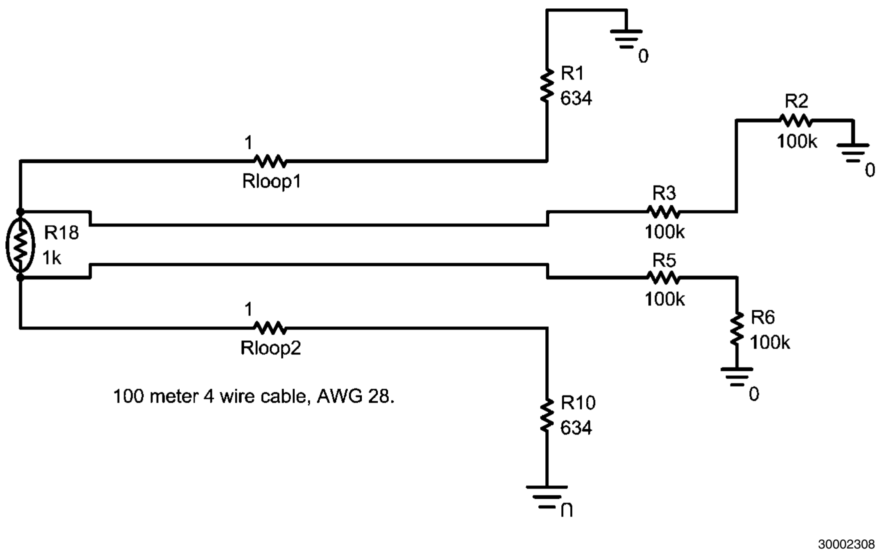

FIGURE 5. Balanced 4 Wire Equivalent Circuit

This balance scheme is much better. The balance number is limited by the resistor tolerances.

6.0 Balanced 3 Wire Interface

Another Balanced interface of interest is a self zeroing 3 wire interface. It is a possibility that the user only has 3 wires available to get to an RTD. This circuit will accommodate that need and cancel the affects of the loop resistance.

A dual version LMP7702 is used for the differential amplifiers. A dual LMP7702 is used for the differential amplifiers.

U1A measures the voltage drop across half of the current loop.

U2B measures the voltage drop across the RTD.

U2A measures the difference between the two providing a corrected output. If the A/D converter has multiple inputs, the differential measurement is reduced to 2 amplifiers and the correction could be implemented in software. This reduces the OP AMP requirement to a single quad.

By monitoring one side of the current loop, multiplying the voltage drop by 2 and subtracting it from the RTD voltage, the effect of the loop resistance is removed.

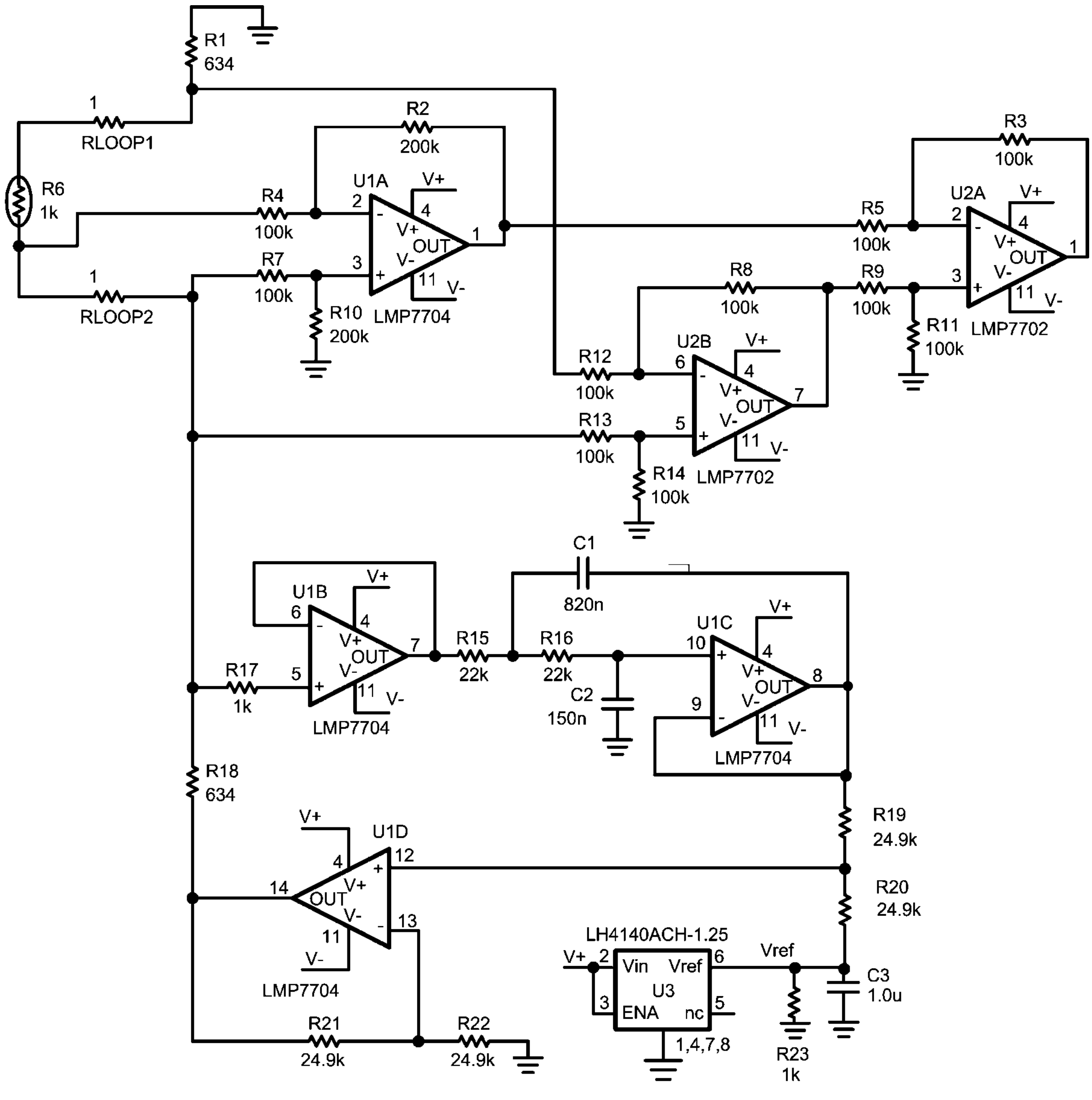

FIGURE 6.

7.0 Recommendations

- Make the interface to the sensor as balanced as possible. This rejects common mode noise and reduces the requirement for low frequency filtering.
- Don't connect high impedance IC connections directly to cables. They are susceptible to high voltages that can be developed in the cables. Use ESD protection circuits for higher reliability designs. R17 provides some protection for the follower of U2A. The input bias current for U2 should be sufficiently low so the input offset caused by the 1k is small.
- Parasitic capacitance can degrade balance. Make the layout as symmetrical and compact as possible
- Spice models are available for this OP AMP at www.national.com. By using SPICE simulations, good resistor choices can be made well in advance.
- The same low pass filter in the current source is used to create a good AC ground at the output of U1D at the power line frequencies. Equal resistances to ground from each side of the RTD in addition to the low pass in the current source will give good CMR at power line frequencies.

8.0 Test Results

A prototype of the above circuit was built and evaluated for accuracy and balance. It was constructed so that 2 wire, 3 wire and 4 wire circuits could be evaluated. The prototype was also equipped with adjustments to remove offset voltage errors that occurred because of resistor mismatching.

To get good results, the following are required:

- Use a V− of 1V or more. This is required because when measuring the voltage drop across the loop resistance, the voltage is too close to GND to actually have GND as the V− rail.

- Use precisely matched resistors (resistor networks) for all of the differential amplifiers to avoid offsets due to resistor mismatch.

8.1 ACCURACY

Figure 7 is a graph of RTD resistance measured and calculated voltage drop.

The lines virtually overlap showing measurement accuracy is basically as good as the resistor matching in the circuit.

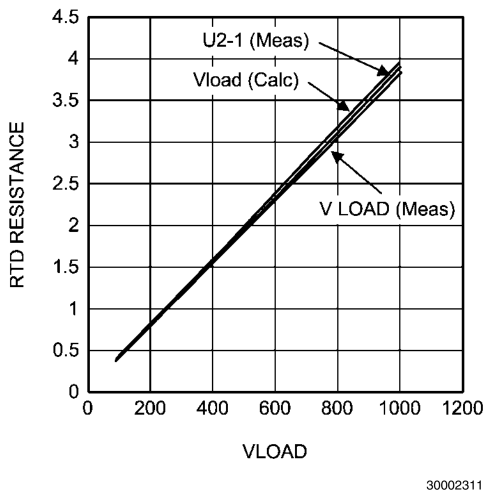

FIGURE 7. Resistance vs Voltage

8.2 BALANCE

The circuit in *Figure 6* was modified to the two wire version to test balance.

Note that in the 3 wire configuration, the balance circuitry is ineffective. Having the third wire in itself creates an imbalance in the cable that is difficult to overcome. The balance circuits do work well in the 2 and 4 wire versions of this circuit.

A common mode signal was applied to both sides of the test resistor R6. A generator Z of 50Ω was used. With a signal that is the same amplitude and phase applied to both sides of the test resistor, the output voltage at U2B pin 7 in the frequency domain was plotted and is shown in *Figure 8*. This plot shows that at as frequency increases, the common mode rejection increases. The filter characteristics can be chosen to reject the common mode frequencies of the system.

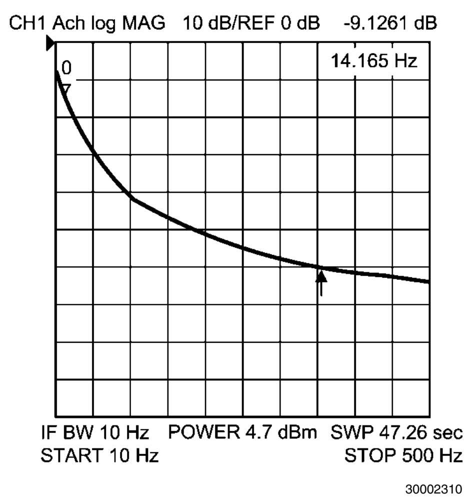

FIGURE 8.

8.3 RAW DATA

R6 (Ω)	V1 (VDC) (Meas)	V2 (VDC) (Meas)	V1–V2 (VDC) (Calc)	I(Load) (ADC) (Calc)	I(Load) (ADC) (Meas)	U1–1 (VDC) (Meas)	U2–7 (VDC) (Meas)	U2–1 (VDC) (Meas)	Vload (VDC) (Calc)	V Load (VDC) (Meas)
100	5.441	2.939	2.502	0.003946372	0.003916	0.07920	0.4712	0.3917	0.394637224	0.3916
200.27	5.831	3.330	2.501	0.003944795	0.003913	0.07950	0.8635	0.7838	0.790024085	0.7834
299.89	6.219	3.717	2.502	0.003946372	0.003908	0.07910	1.2534	1.1732	1.183477571	1.1722
399.99	6.607	4.105	2.502	0.003946372	0.003905	0.07938	1.6430	1.5620	1.578509432	1.5609
500	6.995	4.492	2.503	0.003947950	0.003900	0.07972	2.0320	1.9520	1.973974763	1.9500
600	7.382	4.879	2.503	0.003947950	0.003896	0.07990	2.4200	2.3390	2.368769716	2.3370
700	7.769	5.265	2.504	0.003949527	0.003892	0.07930	2.8090	2.7280	2.764668770	2.7250
800	8.152	5.648	2.504	0.003949527	0.003887	0.07930	3.1940	3.1130	3.159621451	3.1090
900	8.536	6.031	2.505	0.003951104	0.003884	0.07980	3.5800	3.4990	3.555993691	3.4950
1000	8.921	6.416	2.505	0.003951104	0.003879	0.07970	3.9680	3.8860	3.951104101	3.8820

Notes

Notes

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