Tools to Debug “Dead” Boards

Hardware Prototype Bring-up

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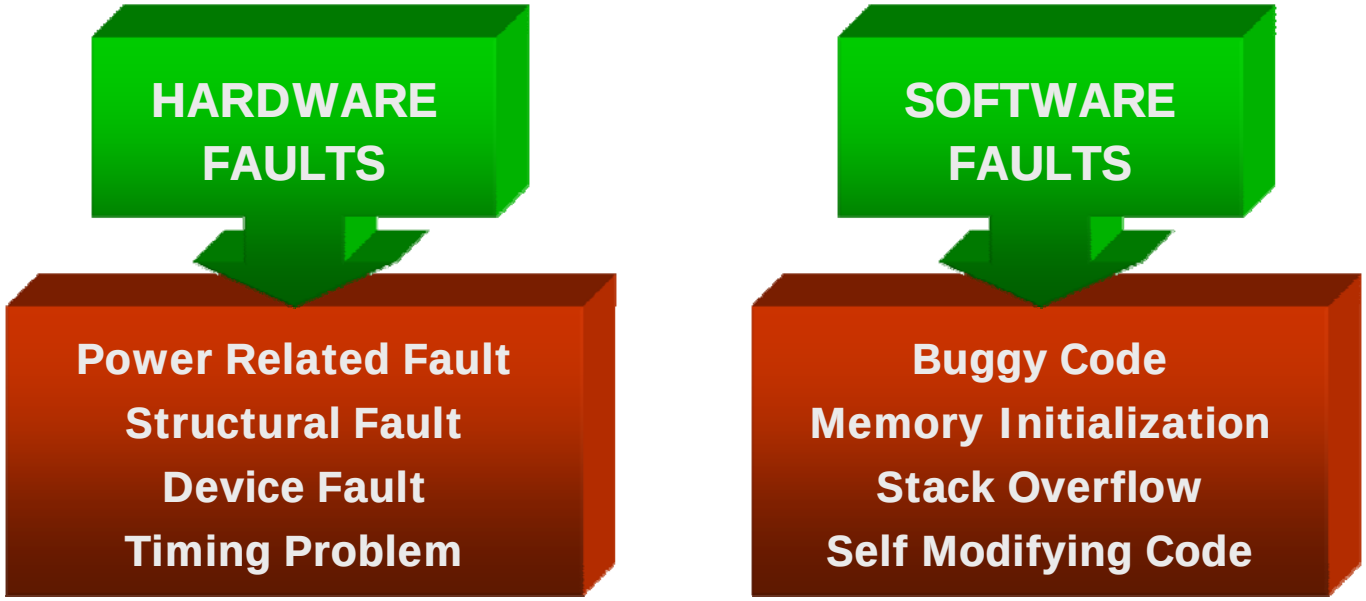
Webinar Outline

- What is a Dead Board?
- Prototype Bring-up & Debug Cycle
- Existing Test Tools
- Corelis Structural & Emulation Test Tools
- Case Study – Complex TI Based Target

What is a “Dead” Board?

“Dead” generally refers to a board that does not respond, initialize or power-up to an expected state. Failure modes can typically be broken down into two categories: hardware and software.



Prototype Bring-Up Cycle

- Visually check correct component installation
- Verify no shorts on power rails to ground
- Apply current-limited power to the board, ensure nothing gets hot, verify voltage levels
- Load basic boot code and functional code to verify CPU and peripheral operation

Engineering Toolbox

- **There are many tools that can assist in the debug process**
- **Having the most efficient tool for the job saves engineering time**
- **Knowing which tool to use at the right time is key**

Multi-Meter
Oscilloscope
Logic Analyzer
Bus Analyzer
Real-Time Trace
Debugger
In-Circuit Emulator

Corelis Toolbox

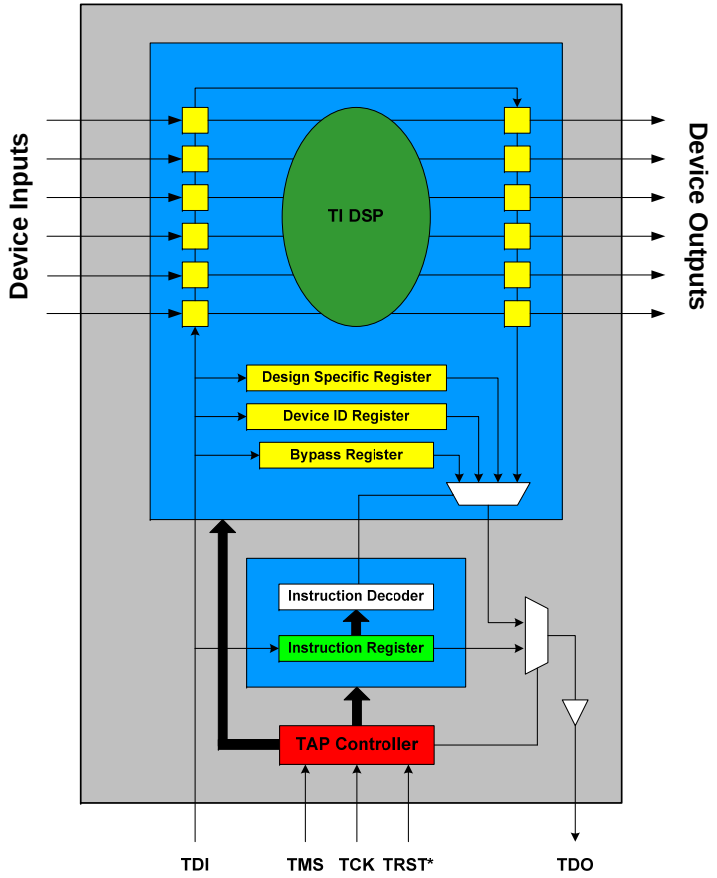
- Corelis directly replaces many traditional debug tools by providing automated test generation and low level diagnostic information saving valuable engineering time and effort
- **Structural testing** identifies physical faults such as broken circuit traces, solder bridges and cold solder joints
- **Emulation testing** verifies DSP operation and exercises peripheral interfaces at intended design speeds

Structural Test

JTAG Architecture

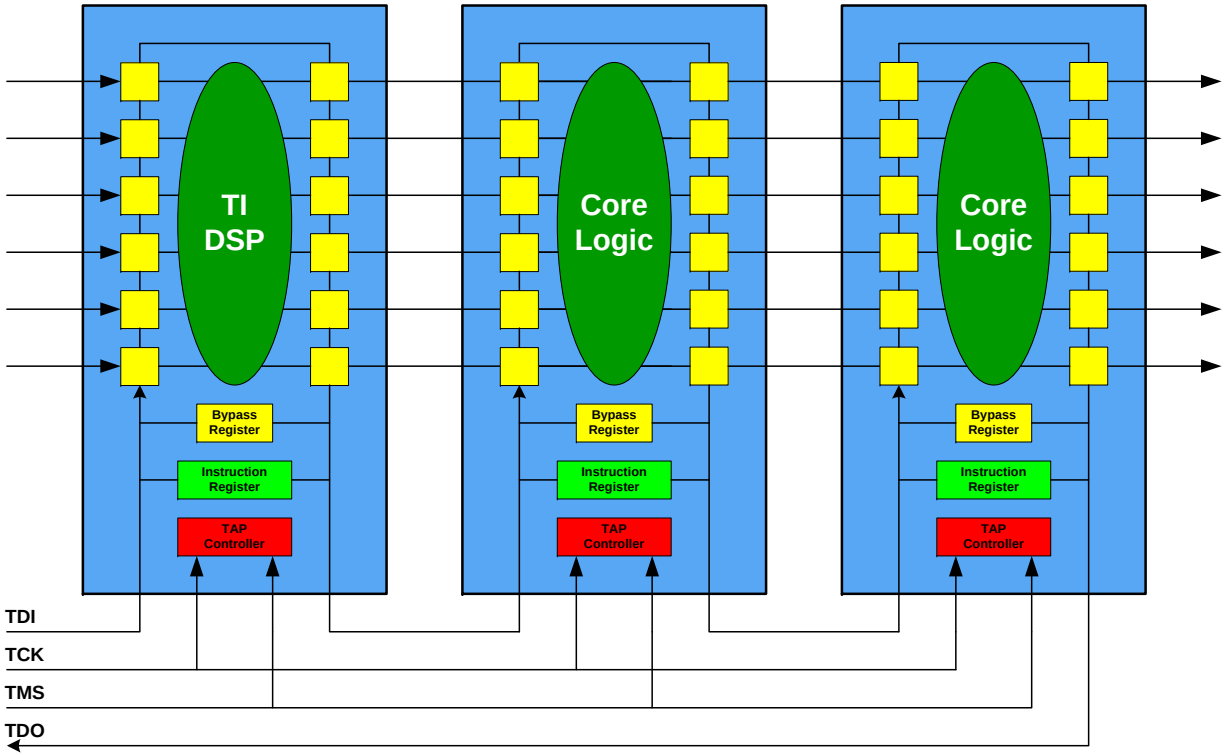
Main Building Blocks of a JTAG Device

- JTAG Interface Pins
- Test Data Registers
- Instruction Register
- TAP Controller



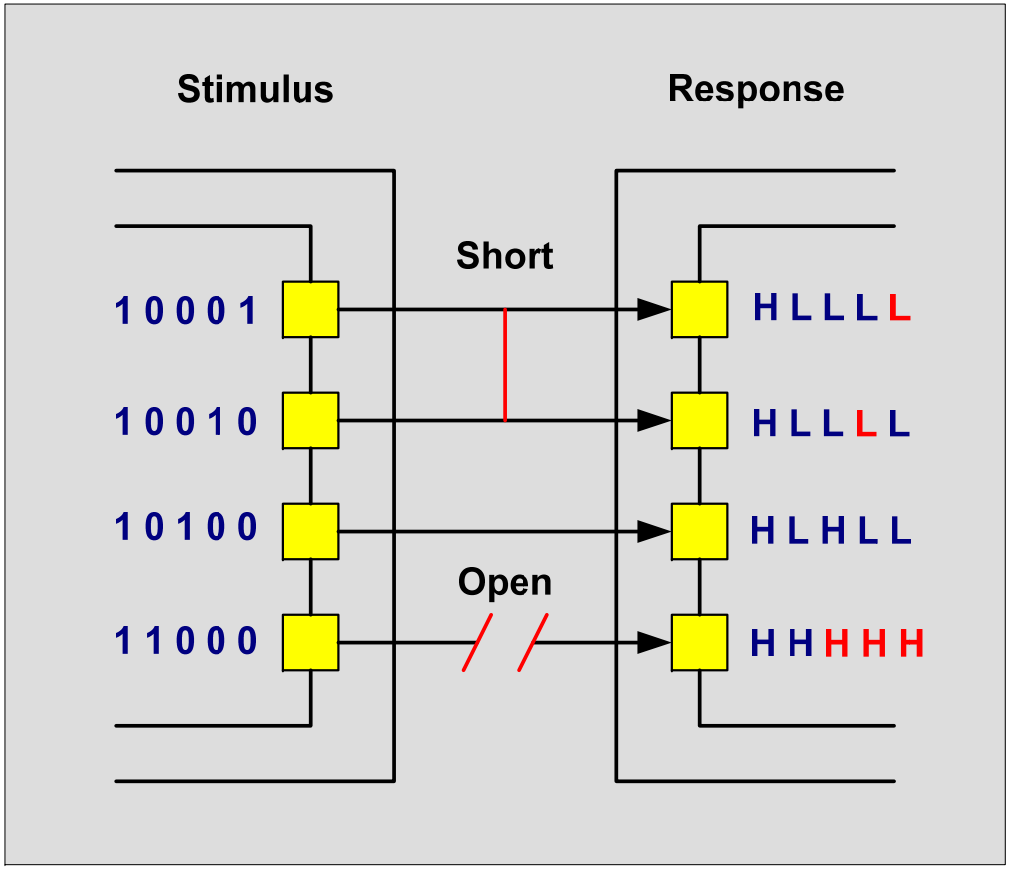
Structural Test

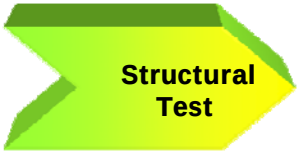
JTAG Scan-Chain



Structural Test

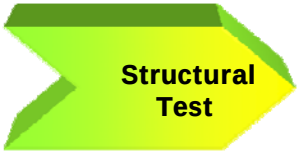
JTAG Test Vectors





JTAG Benefits

- JTAG provides the capability to test interconnects on a PC-board without physical test probes or test fixtures
- Does not require the board to be in a bootable state for fault diagnostics
- JTAG allows In-System Programming of devices such as Flash, CPLDs, FPGAs and Serial EEPROMs



JTAG Advantages

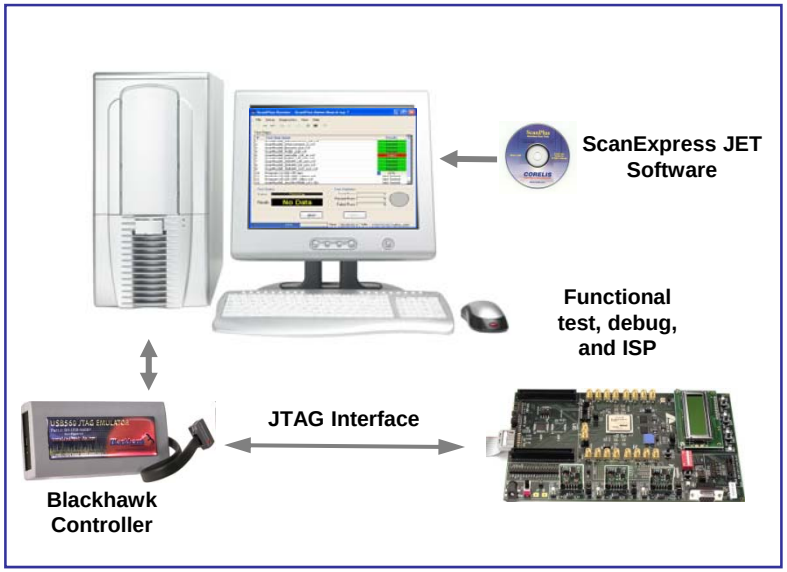
- Automatic test generation removes engineers from having to create elaborate test cases
- Fast test times
- Net/Pin level diagnostics
- JTAG helps identify board problems up front meaning general purpose tools like oscilloscopes and voltage meters are used less
- Test vectors can be reused in production

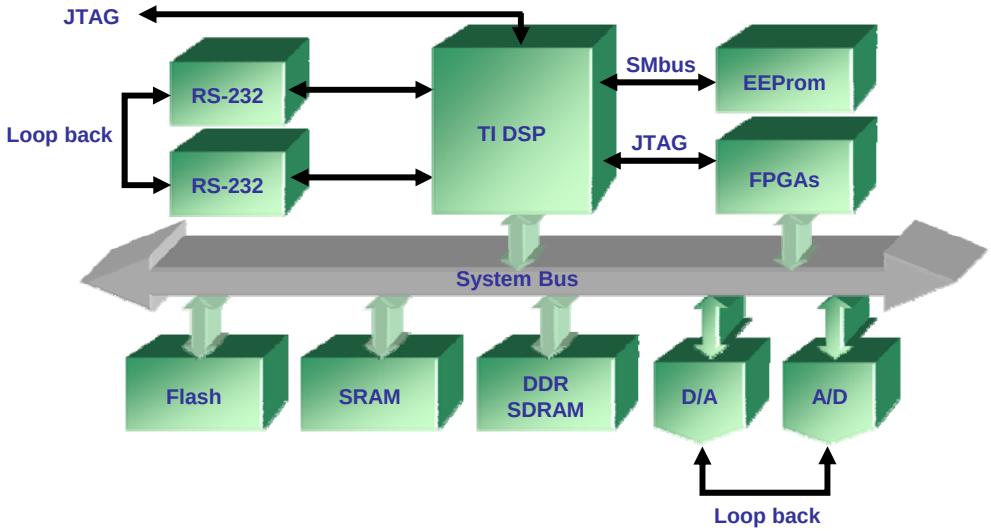
Emulation Test

JTAG Emulation Test

JET uses a DSP's JTAG debug port to perform:

- DSP initialization
- At-speed functional testing of DSP peripherals (memory, I/O)
- In-System-Programming (ISP) of flash devices





JET Benefits

- Does not require the board to be in a bootable state for fault diagnostics
- Embedded tests are downloaded and run from on-chip DSP memory at-speed
- Provides testability on all DSP addressable components by exercising their functionality
- In-system programming at theoretical speeds reduces time waiting for code to download

JET Advantages

- Automated test development for DSP initialization, memory and flash
- Device level diagnostics
- Customized diagnostic messages
- JET rigorously exercises **all** external memory locations before execution of any boot code
- Test vectors can be reused in production

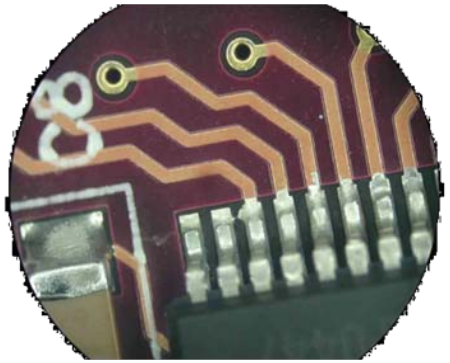
Combining JTAG & JET

Structural Test → Emulation Test → Combined JTAG & JET

Feature	JTAG Test	Emulation Test	Combined Test
Structural coverage	Very good	Good	Excellent
Functional coverage	Low	High	High
Programming (ISP) time	Average	Excellent	Excellent
Test time	Fast	Fast	Fast
Test points required	Very few	Very few	Very few
Test development	Automatic	Semi Auto	Auto/Semi
Diagnostics	Excellent	Average	Excellent

JTAG & JET Fault Coverage

- JTAG Pin Connectivity; Noisy Signals
- Opens, Shorts & Stuck-At Conditions
- DSP Initialization
- Component Discovery and Identification
- Bad Memory Locations
- Flash Communication Problems
- Timing Problems



Case Study — Complex TI Target

- Board includes twenty-six TI DaVinci processors
- Board includes other JTAG and non-JTAG components
- JTAG components include a PowerPC CPU and two FPGAs
- Corelis JTAG tools are able to perform full interconnect and basic memory pin testing
- JET to the rescue…JET emulation testing identified crosstalk and signal integrity issues on SDRAM memories that JTAG scans did not detect