Ver 1.1

TFT LCD Specification

Model NO.: TD028TTEB5

Customer Signature
Date

Table of Contents

Record of Reversion

Rev	Issued Date	Description
0.0	Nov, 10, 2006	New Create
0.1	Nov, 23, 2006	Update RA SPEC
1.0	DEC, 15, 2006	Apply for system Update White Chromaticity Update DVDD/AVDD Supply Current
1.1	Mar, 18, 2007	Update Reliability SPEC, item 10.

1. FEATURES

The 2.8 inch (real 2.83 inch) LCD module is the Transmissive active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and COG design are built on the panel. Highly integrated LCD module includes backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		2.8 inch (real 2.83 inch)	-
Display Type		Transmissive	-
Active Area (HxV)		43.2 X 57.6	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.06 X 0.180	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (18 bits)	-
Outline Dimension (HxVxT)		52.9x73.7x3.4 (TYP; FPC excluded)	mm
Weight		45	g
Power consumption	LCD Panel + System	28	mW
	Backlight	288 (Typ, I_F= 20mA)	

3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

Recommend connector: FH23-39S-0.3SHW(05)/HIROSE

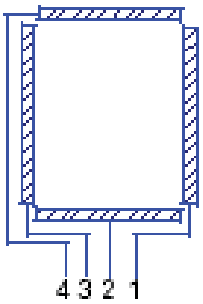
Pin	Symbol	I/O	Description	Remark
1	LED+	-	High Voltage Power Supply for LED	
2	LED-	-	Low Voltage Power Supply for LED	
3	DVDD	-	Power Supply of Digital	
4	AVDD	-	Input to DC/DC	
5	VSS	-	Ground	
6	YU	-	Touch Panel Y(12 Clock Side)	
7	XL	-	Touch Panel X(Left Side)	
8	YL	-	Touch Panel Y(6 Clock Side)	
9	XR	-	Touch Panel X(Right Side)	
10	SPI_CS	I	SPI Chip Select	Reserved for Register Setup
11	SPI_SDA	I/O	SPI Serial Data Input/Output	Reserved for Register Setup
12	VSS	-	Ground	
13	SPI_SCL	-	SPI Clock	Reserved for Register Setup
14	SD	I	Auto power on/of sequence enable input	
15	RST	I	RESET(L: Reset, H: Active)	
16	B0/ID1	I	BLUE data Bit B0(LSB)/ LCM ID Pin 1 (Pull-down 10K to VSS by Resistor)	
17	B1	I	BLUE data Bit B1	
18	B2	I	BLUE data Bit B2	
19	B3	I	BLUE data Bit B3	
20	B4	I	BLUE data Bit B4	
21	B5	I	BLUE data Bit B5(MSB)	
22	G0/ID2	I	GREEN data Bit G0(LSB)/ LCM ID Pin 2 (Pull-high 10K to DVDD by Resistor)	
23	G1	I	GREEN data Bit G1	
24	G2	I	GREEN data Bit G2	
25	G3	I	GREEN data Bit G3	
26	G4	I	GREEN data Bit G4	
27	G5	I	GREEN data Bit G5(MSB)	

28	R0/ID0	I	RED data Bit R0(LSB)/ LCM ID Pin 0 (Pull-down 10K to VSS by Resistor)	
29	R1	I	RED data Bit R1	
30	R2	I	RED data Bit R2	
31	R3	I	RED data Bit R3	
32	R4	I	RED data Bit R4	
33	R5	I	RED data Bit R5(MSB)	
34	VSS	-	Ground	
35	DCK	I	Data Sampling Clock Signal	
36	VSS	-	Ground	
37	VSYNC	I	Vertical sync signal	
38	HSYNC	I	Horizontal sync signal	
39	DENB	I	Data Enable	

3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	9	XR	Touch Panel Right Side	
2	8	YL	Touch Panel Lower Side	
3	7	XL	Touch Panel Left Side	
4	6	YU	Touch Panel Upper Side	

Pin Assignment for Touch panel

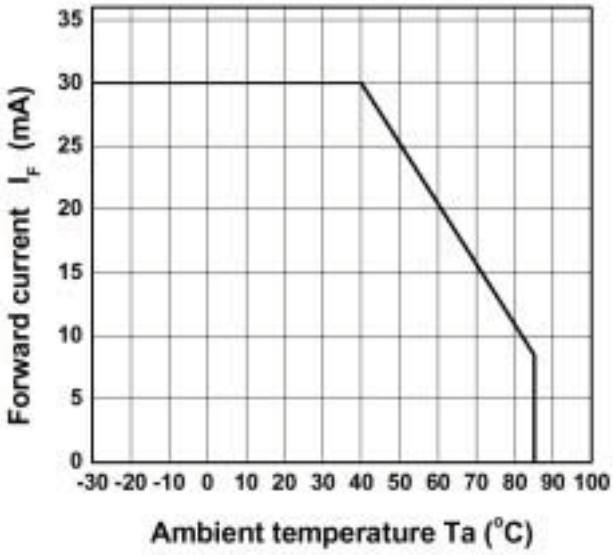


4. ABSOLUTE MAXIMUM RATINGS

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	DVDD	-0.3	3.6	V	
Analog Supply Voltage	AVDD	-0.3	3.6	V	
Touch Panel Operation Voltage	V_{Touch}	-	5	V	
Backlight LED forward Voltage	V_F	-	14.4	V	
Backlight LED reverse Voltage	V_R	-	20	V	
Backlight LED forward current (Ta=25℃)	I_F	-	25	mA	Note
Operating Temperature	Topr	-20	+60	℃	
Storage Temperature	Tstg	-30	+70	℃	

Note: Relation between maximum LED forward current and ambient temperature is showed as bellow.



5.ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		DVDD	1.6	2.8	3.3	V	
Logic Supply Voltage Ripple		—	—	—	100	mV	
Analog Supply Voltage		AVDD	2.5	2.8	3.3	V	
Analog Supply Voltage Ripple		—	—	—	100	mV	
Logic Input Voltage	High	VIH	0.8DVDD	—	DVDD+0.3	V	DCK,HSYNC, VSYNC,DENB ,DATA,SPI
	Low	VIL	VSS-0.3	—	0.2DVDD		
Leakage current		IL	-1	—	1	uA	
DVDD/AVDD Supply Current		I_{VDD}	-	6.0	6.4	mA	

Note 1: Power consumption test condition

a. Input voltage: 2.8V

b. Test pattern:

5.2 Driving backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	25	mA	LED/Part
LED Life Time	-	-	10000	-	Hr	I_F: 20mA
Forward Current Voltage	V_F	-	14.4	16	V	I_F: 20mA ,LED/Part

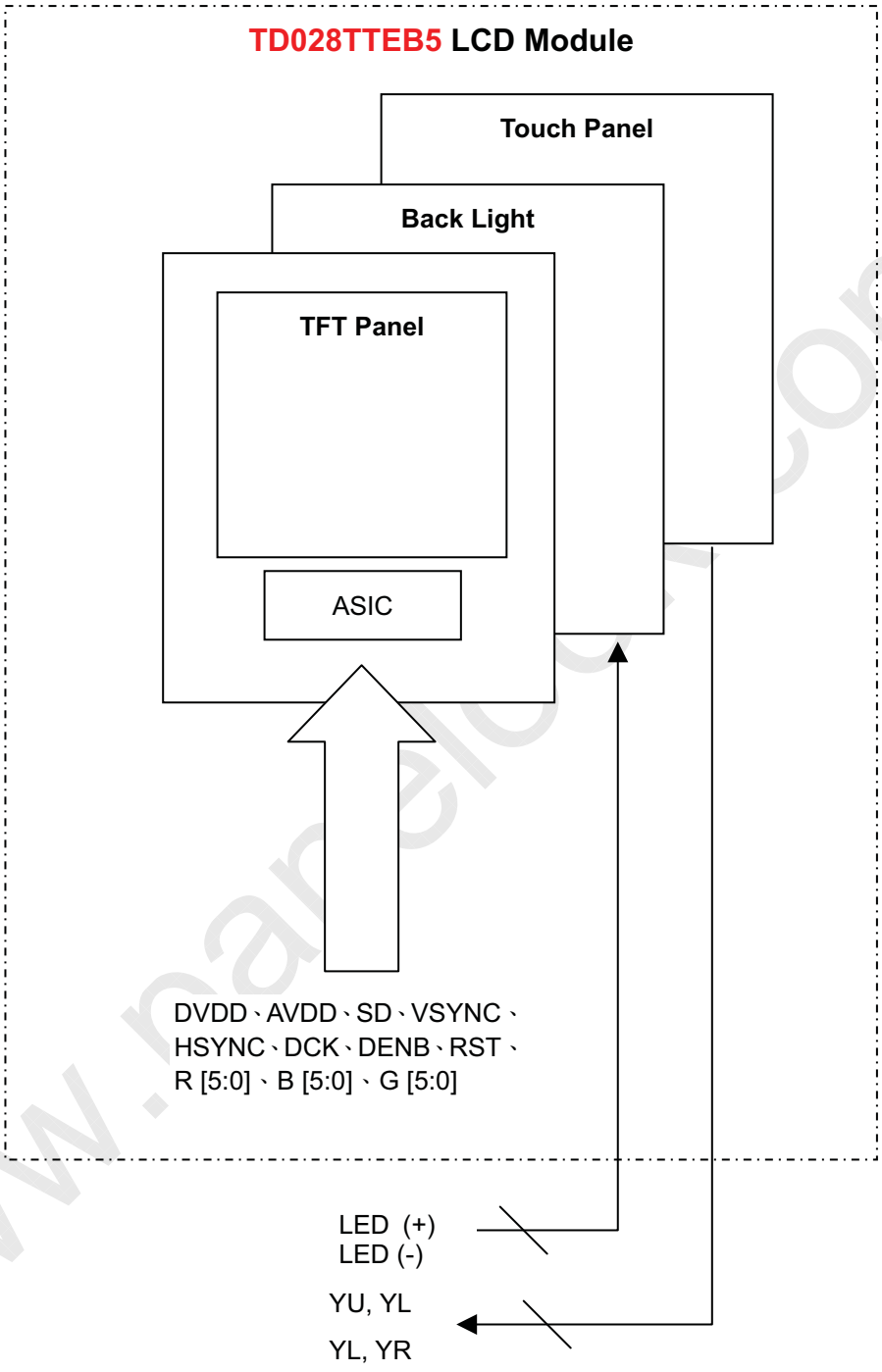
Note: Backtlight driving circuit is recommend as the fix current circuit.

5.3 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	200	-	1300	Ω	
Resistor between terminals (YU-YL)	Ry	200	-	1300	Ω	
Operation Voltage	V_{Touch}	-	5	-	V	DC
Line Linearity (X direction)	-	-1.5	-	+1.5	%	Note
Line Linearity (Y direction)	-	-1.5	-	+1.5	%	
Chattering	-	-	10	-	ms	
Surface Hardness	-	3	-	-	H	JIS K 5600
Minimum tension for detecting	-	-	-	80	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note. The minimum test force is 80 g.

6. BLOCK DIAGRAM



7. TIMING CHART

7.1 Display timing

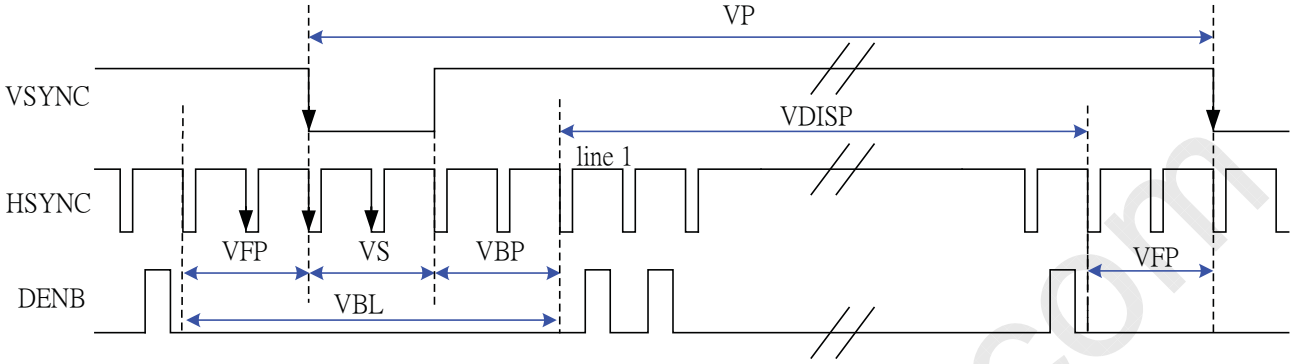
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit	Remark
				MIN	TYP	MAX		
Normal	Vertical Cycle	VP		430	435	450	Line	
	Vertical Pulse Low width	VS		1	2	—		
	Vertical Data Start	VDS	VS+VBP	2	4	15	Line	*Note1
	Vertical Front Porch	VFP		108	111	—	Line	
	Vertical Blanking Period	VBL	VS+VBP+VFP	110	115	—	Line	
	Vertical Active Area	VDISP		—	320	—	Line	
	Horizontal Cycle	HP		260	280	300	dot	
	Horizontal Pulse Low Width	HS		2	10	—	dot	
	Horizontal Data Start	HDS	HS+HBP	10	30	63	dot	*Note2
	Horizontal Front Porch	HFP		—	10	—	dot	
	Horizontal Blanking Period	HBL	VS+VBP+VFP	20	40	—		
	Horizontal Active Area	HDISP		—	240	—	dot	
	Clock Frequency	fDCK		6.7	7.3	8.5	MHz	
		tDCK		149	136	118	nS	

Note1 Please change the register R3 via SPI command to modify the VDS(Min./Max.)

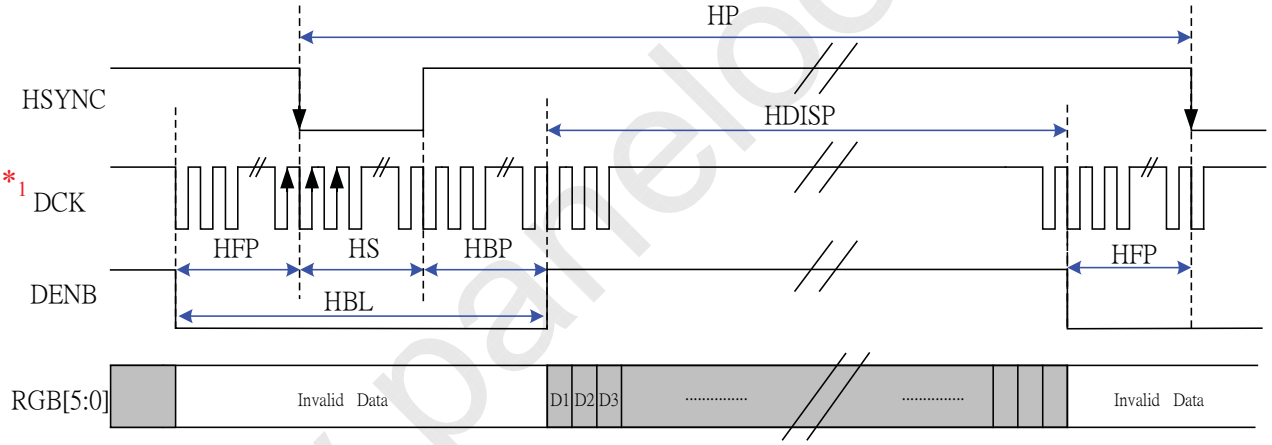
Note2 Please change the register R4 via SPI command to modify the HDS(Min./Max.)

7.2 Input timing chart

＜Vertical Timing chart＞



＜Horizontal Timing chart＞

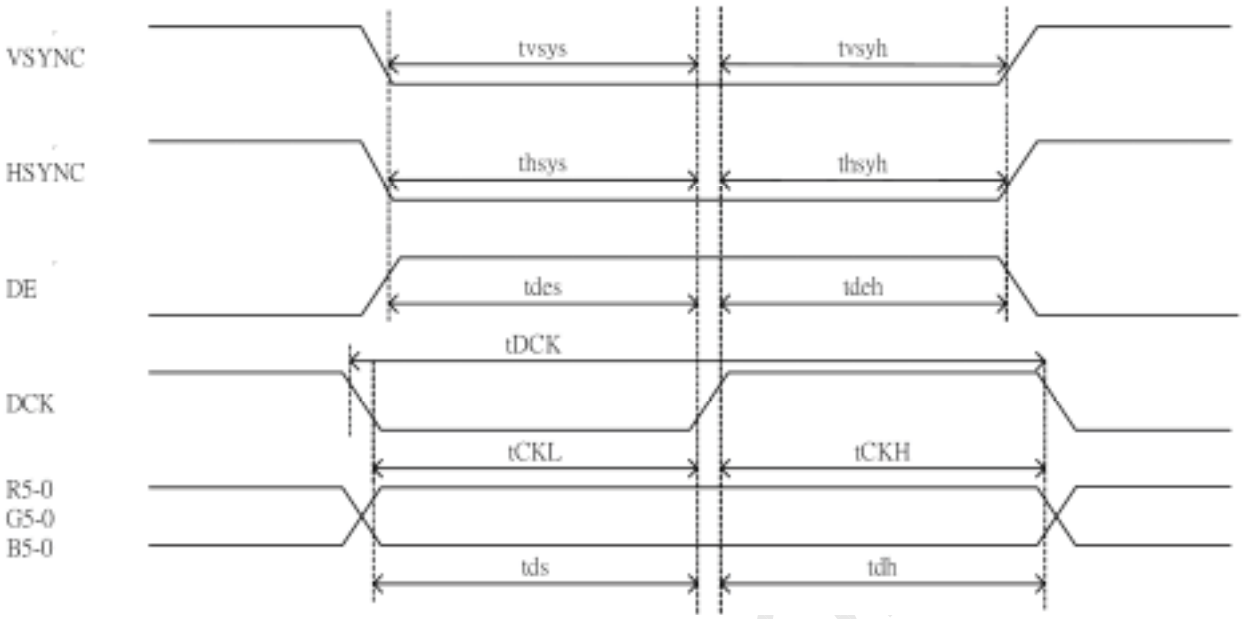


*1 The frequency of DCK should be continued whether in display or blank region to ensure IC operating normally.

Note：

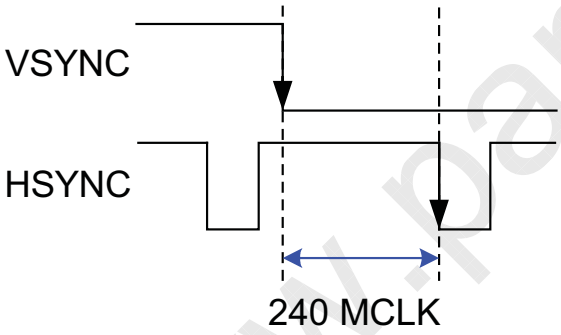
（1） In VS+HS mode，just remove the DE signal，all the other timing is the same 。Please change the register R2 via SPI command to modify the VS+HS mode。

7.3 Setup / Hold Timing chart

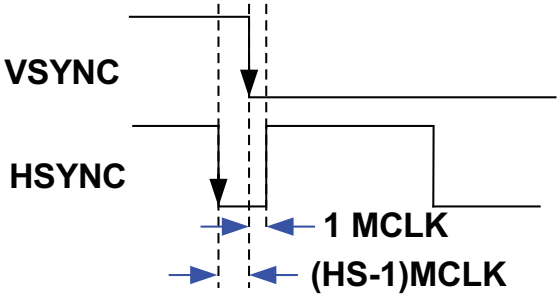


Phase difference of Sync.(thv)：

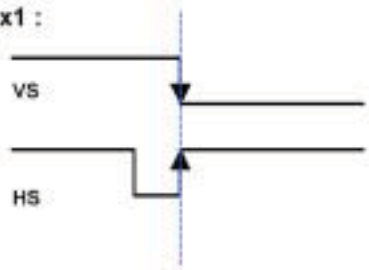
Maximum Timing chart：



Minimum Timing chart：

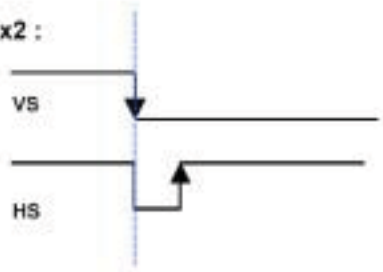


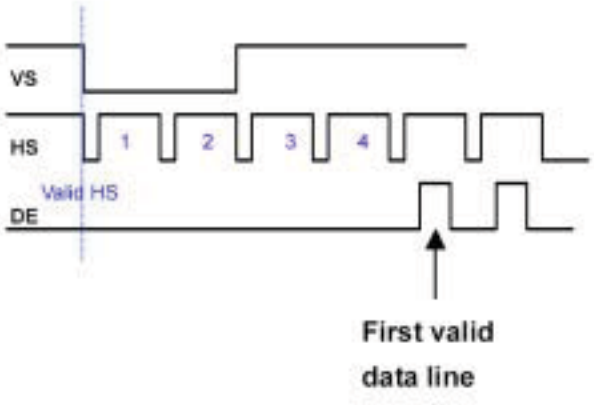
Ex1 :



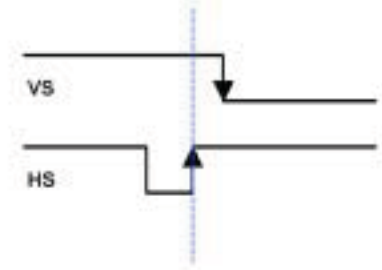
If the VS falling edge and HS rising edge are in the same time, the timing is in the margin and not surely which is the first valid data line.

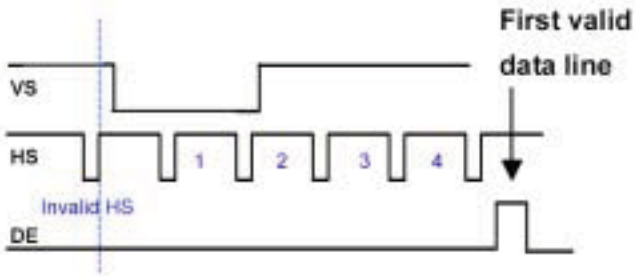
Ex2 :





Ex3 :





If VS falling edge is delay some time after HS rising edge, this timing will cause the first valid data line delay one HS time.

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	—	—	ns
Vertical Sync. Hold time	tvsyh		20	—	—	ns
Horizontal Sync. Setup time	thsys		20	—	—	ns
Horizontal Sync. Hold time	thsyh		20	—	—	ns
Phase difference of Sync. Signal Falling edge	thv		-(HS-1)	—	240	DCK
Clock Low Priod	tCKL		75	—	—	ns
Clock High Priod	tCKH		75	—	—	ns
Data setup time	tds		20	—	—	ns
Data Hold time	tdh		20	—	—	ns
DE setup time	tdes		30	—	—	ns
DE Hold time	tdeh		30	—	—	ns

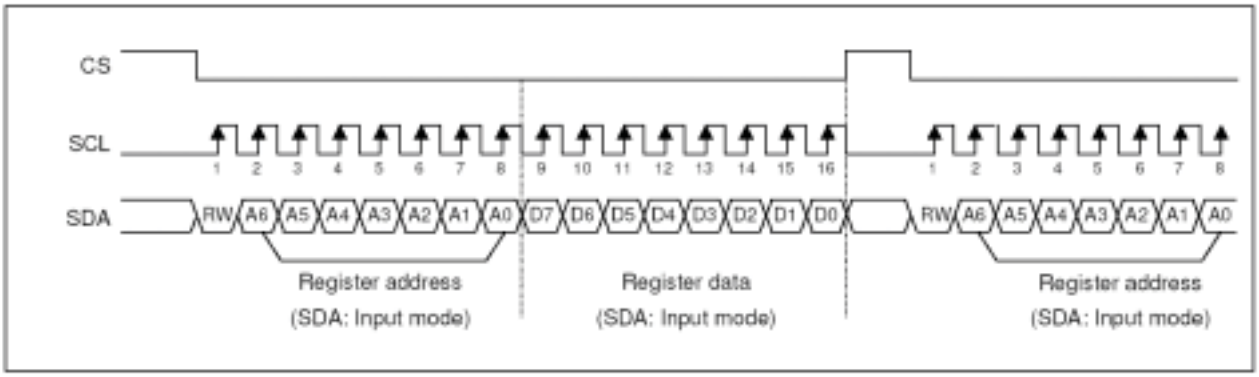
Note: Thv range if it can't meet our spec, just give up first Hsync. It can't impact any side effect.

<SERIAL INTERFACE>

The LCM support the 3-pin serial interface to set internal register. Read/Write bit RW, Serial address A6 to A0 and serial data D7 to D0 are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

Serial interface signal timing chart

Write Mode (RW=L)

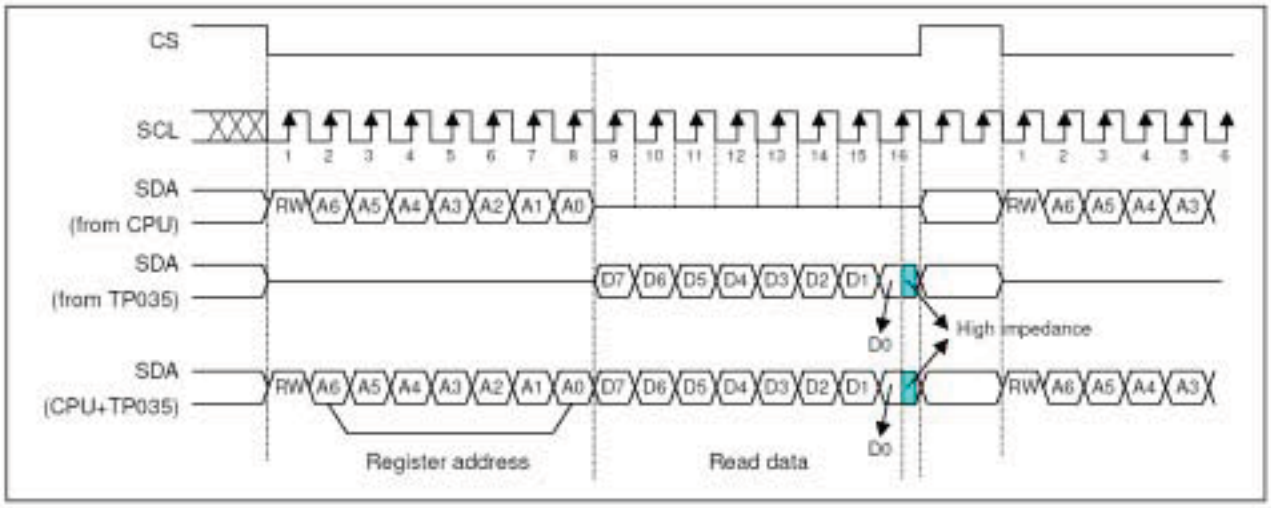


The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit address and 8-bit data set for the command.

When using SCL wiring, the module has to be designed carefully to avoid any noise coming from reflection or from external sources. We recommand checking operation with the actual module.

If there is a break in data transmission by RESETB or CS pulse, while transferring a Command or Parameter, before Bit D0 of the byte has been completed, then LCM will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CS) is activated after RESETB have been High state.

Read Mode (RW=H)



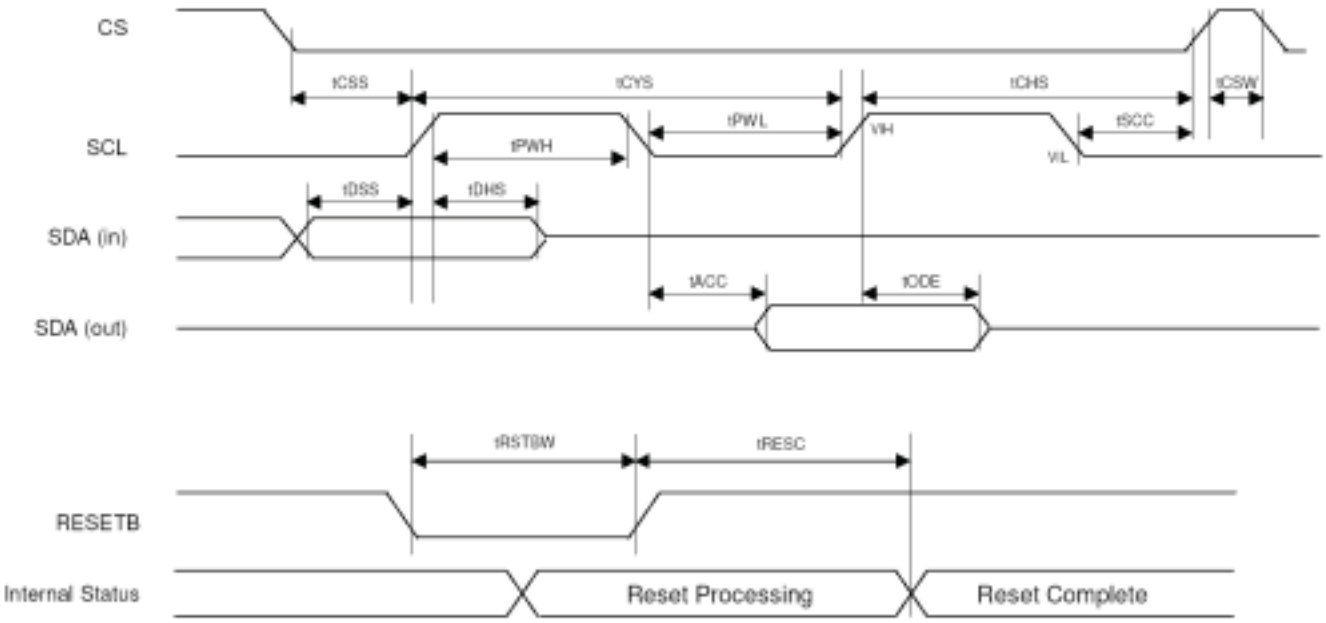
The read mode of the interface means that the micro controller reads data from the LCM.
To do so the micro controller first has to send a command: the read status command.
Then the following byte is transmitted in the opposite direction. After that CS is required to go high.

The LCM samples the SDA data input at rising SCL edges, but shifts SDA data output at falling SCL edges.
Thus the micro controller is supposed to read SDA data at rising SCL edges.

After the read status command has been sent, the SDA line must be set to tristate not later then at the rising SCL edge of the last bit.

The LCM can read data of the Register0 to Register63

Serial interface and reset waveform (VIH=0.8DVDD，VIL=0.2DVDD)



Serial interface and Reset						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Clock cycle	tCYS	-	150	-	-	ns
Clock High Period	tPWH	-	60	-	-	ns
Clock Low Period	tPWL	-	60	-	-	ns
Data Set-up Time	tDSS	-	60	-	-	ns
Data Hold Time	tDHS	-	60	-	-	ns
CS High width	tCSW	-	1	-	-	us
CS Set-up Time	tCSS	-	60	-	-	ns
CS Hold Time	tCHS	-	70	-	-	ns
SCL to CS	tSCC		40	-	-	ns
Output Access Time	tACC		10	-	50	ns
Output Disable Time	tODE		25	-	80	ns
RSTB low width	tRSTBW	-	1000	-	-	ns
RESET complete time	tRESC	-	-	-	1000	ns

Command descriptions：

Reset the internal register by setting low level the RESET pin or software reset command.

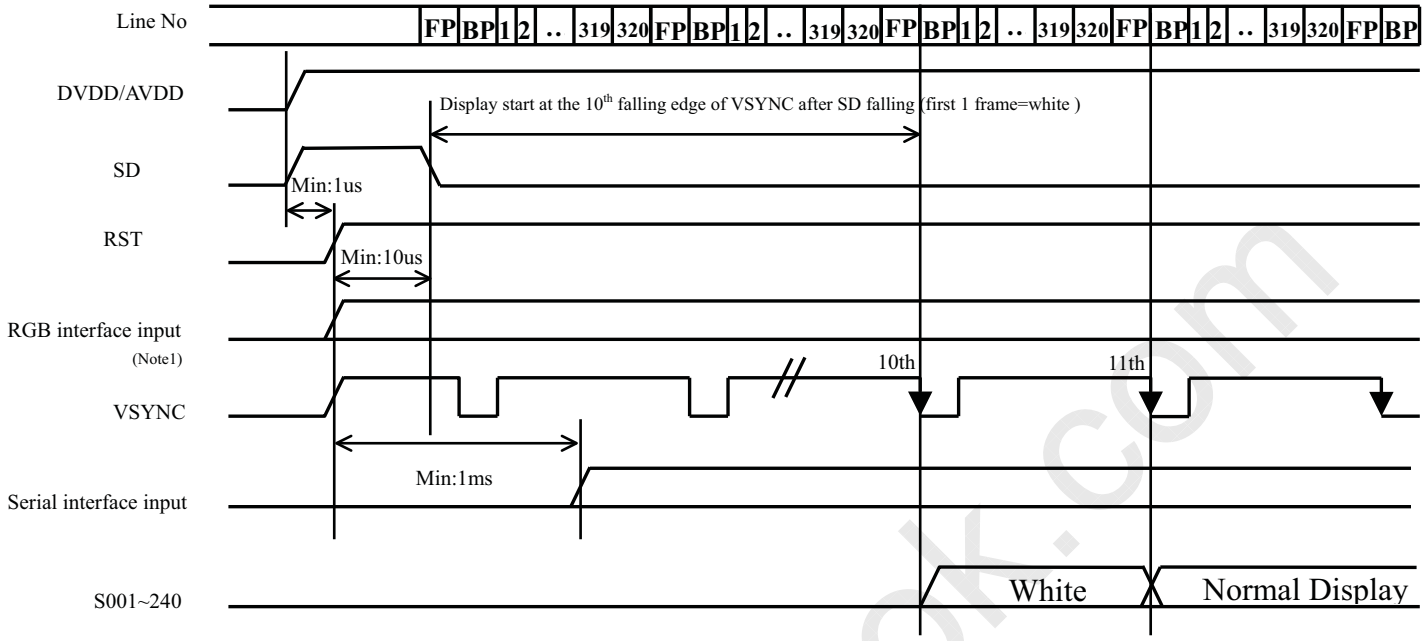
Register [Dec]	Default [Hex]	Bit name	Setting value D7	D6	D5	D4	D3	D2	D1	D0	Description	Remark
R0	85h	CHIPID[2:0]									Chip ID (Read only)	The Chip ID can be changed by MASK Option.
			1								D7=1 for SPFD5413C	
					0	0	0				ID 0	
					0	0	1				ID 1	
					-	-	-				-	
					1	1	1				ID 7	
		REVID[2:0]									Revision ID (Read only)	The Revision ID can be changed by MASK Option.
								0	0	0	REV 0	
								0	0	1	REV 1	
								0	1	0	REV 2	
								0	1	1	REV 3	
								1	0	0	REV 4	
								1	0	1	REV 5	
								1	1	0	REV 6	
								1	1	1	REV 7	
R1	00h	VCM[7:5]									VCOM amplitude adjustment by VCOMH voltage change at full color mode	VCOMH voltage change at full color mode
			0	1	1						150 mV	
			0	1	0						100 mV	
			0	0	1						50 mV	
			0	0	0						0 mV	
			1	0	0						-50 mV	
			1	0	1						-100 mV	
			1	1	0						-150 mV	
			1	1	1						-200 mV	
		VCM[4:0]									VCOM voltage select at full color mode	VCOM_DC value setting at full color mode
						0	1	1	1	1	VCOMH=4.305V, VCOML=0.705V	
						0	1	1	1	0	VCOMH=4.290V, VCOML=0.690V	
						0	1	1	0	1	VCOMH=4.275V, VCOML=0.675V	
						0	1	1	0	0	VCOMH=4.260V, VCOML=0.660V	
						0	-	-	-	-	-	
						0	0	0	0	1	VCOMH=4.095V,VCOML=0.495V	
						0	0	0	0	0	VCOMH=4.080V,VCOML=0.480V	
						1	0	0	0	0	VCOMH=4.065V,VCOML=0.465V	
						1	0	0	0	1	VCOMH=4.050V,VCOML=0.450V	
						1	-	-	-	-	-	
						1	1	1	0	1	VCOMH=3.870V,VCOML=0.270V	
						1	1	1	1	0	VCOMH=3.855V,VCOML=0.255V	
						1	1	1	1	1	VCOMH=3.840V,VCOML=0.240V	
R2	00h	SYNCP									SYNC polarity select	Mode slection
				0							Negative	
				1							Positive	
		DINT									Input data mapping select	
					0						18 bit interface (262k color)	
					1						16 bit interface (65k color, R:G:B=5:6:5)	
		DCKP									Input clock polarity change	
						0					No change	
						1					Change	
		MSEL									Input Timing Model Select	
									0	0	HS+VS+DE	
									0	1	HS+VS	
									-	-	-	

Register [Dec]	Default [Hex]	Bit name	Setting value D7	D6	D5	D4	D3	D2	D1	D0	Description	Remark
R3	04h	VSTS[3:0]									Vertical valid data start time select (VDS)	
							0	0	0	0	2 HSYNC	
							0	0	0	1	2 HSYNC	
							0	0	1	0	2 HSYNC	
							0	0	1	1	3 HSYNC	
							0	1	0	0	4 HSYNC	
							0	1	0	1	5 HSYNC	
							-	-	-	-	-	
							1	1	1	1	15 HSYNC	
R4	1Eh	HSTS[5:0]									Horizontal valid data start time select (HDS)	
					0	0	0	0	0	0	10 DCK	
					0	0	0	0	0	1	10 DCK	
					0	0	0	0	1	0	10 DCK	
					0	0	0	0	1	1	10 DCK	
					0	0	0	1	0	0	10 DCK	
					0	0	0	1	0	1	10 DCK	
					0	0	0	1	1	0	10 DCK	
					0	0	0	1	1	1	10 DCK	
					0	0	1	0	0	0	10 DCK	
					0	0	1	0	0	1	10 DCK	
					0	0	1	0	1	0	10 DCK	
					0	0	1	0	1	1	11 DCK	
					0	0	1	1	0	0	12 DCK	
					-	-	-	-	-	-	-	
					0	1	1	1	1	0	30 DCK	
					-	-	-	-	-	-	-	
					1	1	1	1	1	1	63 DCK	
R5	01h	PARS[7:0]									Partial start line select	When VSYNC+HSYNC+DE mode, DE=H: Normal display line DE=L: Non-display line (White) When VSYNC+HSYNC mode, Normal display line can be selected by R5,6,7 and 8.
			0	0	0	0	0	0	0	0	Do not setting when PARS[8]=0, Gate256 is selected when PARS[8]=1	
			0	0	0	0	0	0	0	1	Gate1 is selected when PARS[8]=0, Gate257 is selected when PARS[8]=1	
			0	0	0	0	0	0	1	0	Gate2 is selected when PARS[8]=0, Gate258 is selected when PARS[8]=1	
			0	0	0	0	0	0	1	1	Gate3 is selected when PARS[8]=0, Gate259 is selected when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	1	1	1	1	1	1	Gate63 is selected when PARS[8]=0, Gate319 is selected when PARS[8]=1	
			0	1	0	0	0	0	0	0	Gate64 is selected when PARS[8]=0, Gate320 is selected when PARS[8]=1	
			0	1	0	0	0	0	0	1	Gate65 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			0	1	0	0	0	0	1	0	Gate66 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
R6	00h	PARS[8]									Partial start line select	
										0	Gate1 – Gate255 is selected	
										1	Gate256 – Gate320 is selected	

Register [Dec]	Default [Hex]	Bit name	Setting value D7	D6	D5	D4	D3	D2	D1	D0	Description	Remark
R7	20h	PARE[7:0]									Partial end line select	When VSYNC+HSYNC+DE mode, DE=H: Normal display line DE=L: Non-display line (White) When VSYNC+HSYNC mode, Normal display line can be selected by R5,6,7 and 8.
			0	0	0	0	0	0	0	0	Do not setting when PARE[8]=0, Gate256 is selected when PARE[8]=1	
			0	0	0	0	0	0	0	1	Gate1 is selected when PARE[8]=0, Gate257 is selected when PARE[8]=1	
			0	0	0	0	0	0	1	0	Gate2 is selected when PARE[8]=0, Gate258 is selected when PARE[8]=1	
			0	0	0	0	0	0	1	1	Gate3 is selected when PARE[8]=0, Gate259 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-		
			0	0	0	1	1	1	1	1	Gate31 is selected when PARE[8]=0, Gate286 is selected when PARE[8]=1	
			0	0	1	0	0	0	0	0	Gate32 is selected when PARE[8]=0, Gate287 is selected when PARE[8]=1	
			0	0	1	0	0	0	0	1	Gate33 is selected when PARE[8]=0, Gate288 is selected when PARE[8]=1	
			0	0	1	0	0	0	1	0	Gate34 is selected when PARE[8]=0, Gate289 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	1	1	1	1	1	1	Gate63 is selected when PARE[8]=0, Gate319 is selected when PARE[8]=1	
			0	1	0	0	0	0	0	0	Gate64 is selected when PARE[8]=0, Gate320 is selected when PARE[8]=1	
			0	1	0	0	0	0	0	1	Gate65 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			0	1	0	0	0	0	1	0	Gate66 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
R8	00h	PARE[8]									Partial end line select	
										0	Gate1 – Gate255 is selected	
										1	Gate256 – Gate320 is selected	
R9	C1h	RL									Shift direction (right / left)	
			0								D240 to D1	
			1								D1 t0 D240	
		TB									Shift direction (top / bottom)	
				0							Bottom to top	
				1							Top to bottom	
		CM									Full color or partial color setup	
					0						Normal (262K color)	
					1						Partial(8 color)	
		RESOL[1:0]									Resolution mode select	
						0	0				240 x RGB x 320	
						1	1				240 x RGB x 240	
		INVSEL									Invert mode eclect	
								0			Line inversion	
								1			Frame inversion	
		STV1									STV1(single / main panel) signal control	
									0		STV1 signal output	
									1		STV1 signal not output	
		STV2									STV2(dual / sub panel) signal control	
										0	STV2 signal output	
										1	STV2 signal not output	
R10	00h	CMDR									Software reset	
										0	Normal	
										1	Software reset	

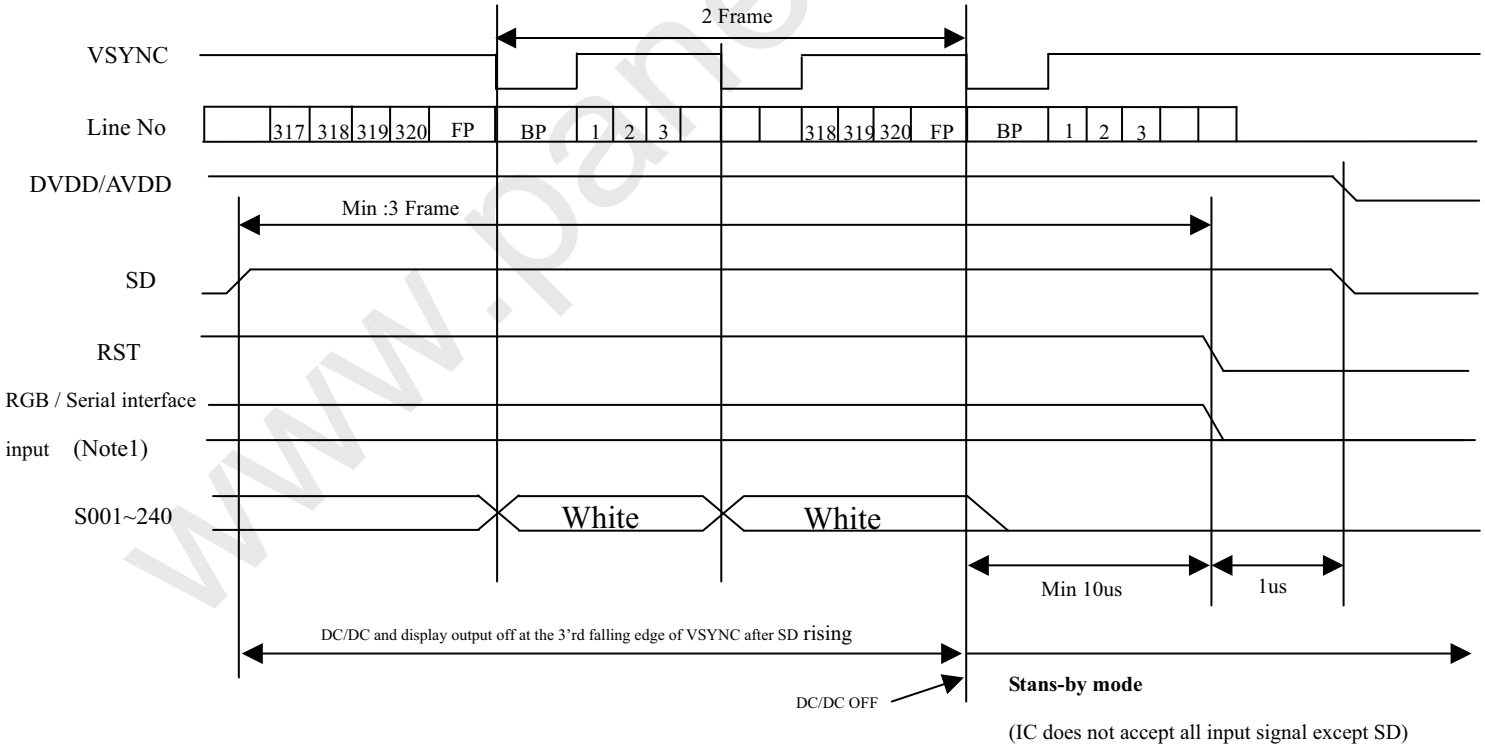
8. Power On/Off Sequence

Power on sequence



(Note 1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DENB

Power off sequence



(Note 1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DENB

9. Optical Characteristics

9.1 Optical Specification

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11(R)		CR ≥ 10	45	55	-	Degree	Note 9-1
	Θ12(L)			45	55	-		
	Θ21(U)			50	60	-		
	Θ22(D)			40	45	-		
Response Time	Tr+Tf		Θ=0°	-	35	50	ms	Note 9-2
Contrast Ratio	CR		Θ=0°	200:1	300:1	-	-	Note 9-3
Luminance	L		Θ=0° I_F=20mA	240	280	-	cd/m^2	Note 9-4
NTSC	-		-	45	50	-	%	Note 9-4
Uniformity	-		-	75	80	-	%	Note 9-5
Chromaticity	Red	x	Θ=0°	0.565	0.615	0.665	-	Note 9-6
		y		0.300	0.350	0.400		
	Green	x		0.290	0.34	0.390		
		y		0.509	0.559	0.609		
	Blue	x		0.096	0.146	0.196		
		y		0.062	0.112	0.162		
	White	x		0.275	0.310	0.345		
		y		0.290	0.330	0.370		

9.2 Basic measure condition

9.2.1 Driving voltage

VDD= 12.0V, VEE=-6.5V

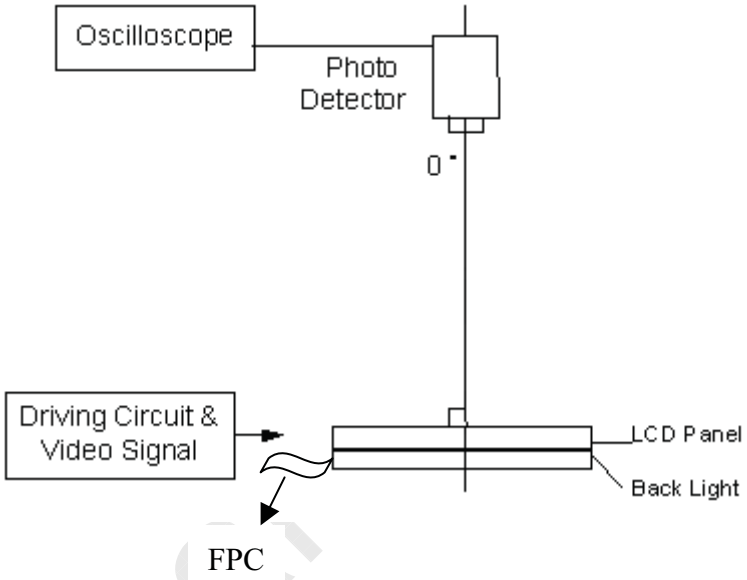
9.2.2 Ambient temperature: Ta=25℃

9.2.3 Testing point: measure in the display center point and the test angle Θ=0°

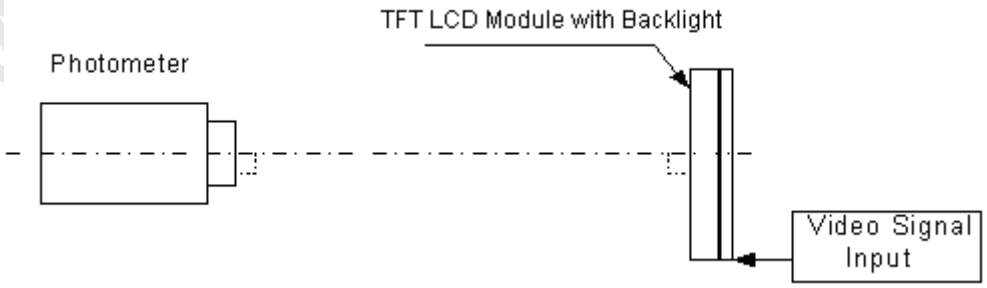
9.2.4 Testing Facility

Environmental illumination: ≤ 1 Lux

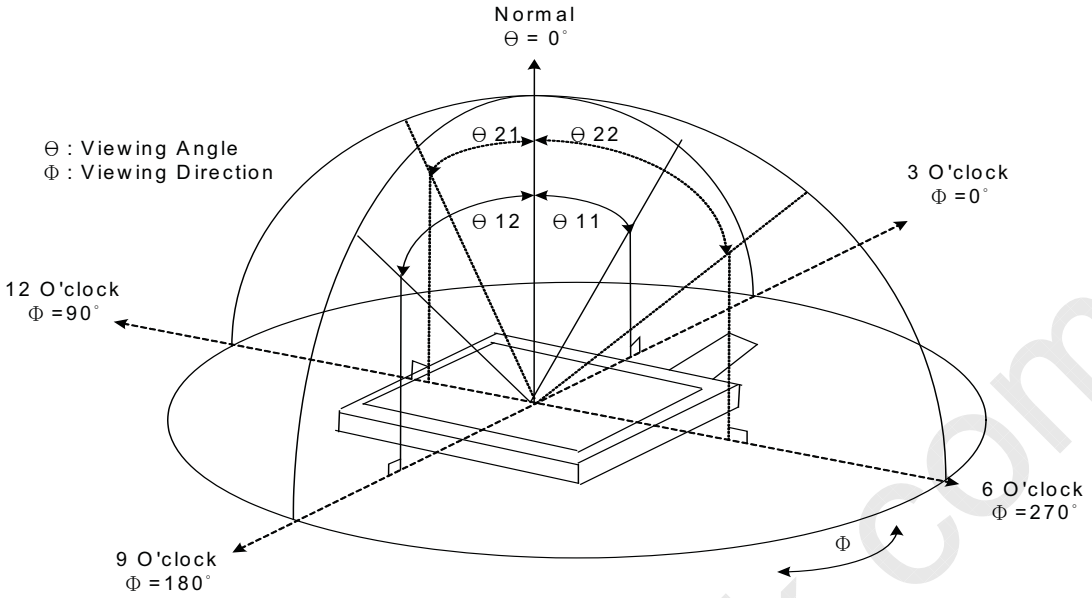
A. System A (DMS 900 series)



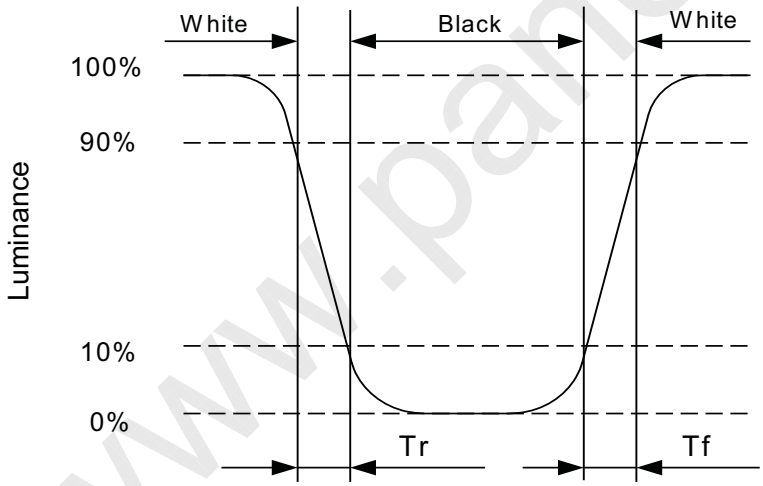
B. System B (BM5A)



Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Definition of response time: (Measure System C)



Note 9-3: **Contrast Ratio** in back light on (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 9-4: **Luminance** : (Measure System A_ Spectrum meter)

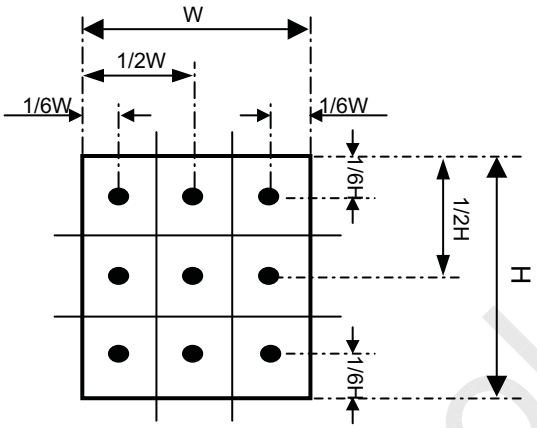
Test Point: Display Center

(The minimum transmission ratio of touch panel is 80%)

Note 9-5: **Uniformity** (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

Note 9-6: White chromaticity as back light on and NTSC(Measure System A_Spectrum)

10. Reliability

No	Test Item	Condition
1	High Temperature Operation,HTO IEC 68-2-2	Ta=60℃, 240Hrs
2	High Temperature Storage,HTS IEC 68-2-2	Ta=70℃, 240Hrs
3	Low Temperature Operation,LTO IEC 68-2-1	Ta=-20℃, 240Hrs
4	Low Temperature Storage,LTS IEC 68-2-1	Ta=-30℃, 240Hrs
5	High Temperature & High Humidity Operation,HHO IEC 68-2-3	Ta=40℃, RH=95%, 240Hrs
6	High Temperature & High Humidity Storage,HHS IEC 68-2-3	Ta=60℃, RH=90%, 240Hrs
7	Thermal Shock,TS IEC 68-2-14	-30℃(0.5hrs)⟷70℃(0.5hrs), 50Cycles
8	Low Pressure test - Operation	Operation, 15,000ft(0.52atm) /48hours.

9	Low Pressure test - Non Operation	Non-Operation, 40,000ft(0.186atm) /48hours
10	Storage	1.60℃(16Hrs) 2.25℃, 60%RH, 2Hrs 3.90%RH, 25℃→55℃ within 3 Hrs, stay 9Hrs at 55℃,55℃→25℃ within 3Hrs ,stay 9Hrs at 25℃ 4.25℃, 60%RH, 2Hrs 5.-20℃, 24Hrs 6.25℃, 60%RH, 2Hrs 7.90%RH, 25℃→55℃ within 3 Hrs,stay 9Hrs at 55℃,55℃→25℃ within 3Hrs ,stay 9Hrs at 25℃ . repeat 2 times
11	Sine Vibration Test - Operation	Sweep rate 0.5 octave/ min. 3 axes, 3 sweep per axis. 5~9 Hz, 6.6mm(P-P), 9~200Hz, 1.0G, 200~500Hz,1.5G
12	Sine Vibration Test - Non Operation IEC 68-2-6	5g Zero to peak, Sweep rate 0.5 octave/ min. one sweep, 10~500Hz, all 3 axes(X,Y,Z)
13	Random Vibration Test - Operation	3 axes, 30 min per axis, 1.67 grms, 10~200Hz, 0.01G^2/Hz, 200~500Hz, 0.003G^2/Hz
14	Random Vibration Test - Non Operation	0.025G^2/Hz, 10~500Hz, Normal 3.5Grms in each axis

15	Shock Test- Non Operation IEC 68-2-27	Acceleration: 400G; Time: 2.0ms;Directions: ±X, ±Y, ±Z; Cycles: one
16	Dust Test IEC 68-2-68	Condition 1: Temperature Range: 15℃ to 35℃ Relative Humidity: 25 % to 75 % Air Pressure: 86 kPa to 106 kPa Particle size: 50 micrometer Duration time: 8 hours BS EN 60529: IP5X degree of protection Condition2: The box fills with enough talcum powder to cover up UUT and the box only contain 1 unit. Test shall be continued for a period of 1 minute.
17	FPC Bending Test IEC 68-2-21	Connector side : bending angle will be decided per different project . LCD side : bending angle will be decided per different project . Minimum 15 cycles for each side.
18	FPC connection Insert/Remove test	Insert/Remove LCM FPC for 15 cycles.
19	Image Retention Test	Black/white block interleave pattern in +40℃ for 12 hours, residual image should not be found on R,G,B and Black/white block interleave pattern after 120 minutes at room temp.
20	Touch Panel Writing Friction Resistance Test	After 100,000 cycles (forward – back two way defined as 1 cycle) with a stylus of R0.8 polyacetal (load: 250g) in center of active area and measure it.

21	Touch Panel Pin Activation Test	Hit it 1,000,000 times with a silicon rubber of R8 Hs40 and measure it. The hitting force shall be 250g and hitting speed 3 times per second.

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

11.1.1 In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

11.1.2 The machine and working table for the panel should have ESD protection strategy.

11.1.3 In handling the panel, ionized airflow decreases the charge in the environment is necessary.

11.1.4 In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

11.2.1 Working environment of the panel should be in the clean room.

11.2.2 Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

11.3 Touch panel

11.3.1 The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

11.3.2 When any dust or stain is observed on a film surface, clean it using a glass lens cleaner for something similar.

11.4 Others

11.4.1 Turn off the power supply before connecting and disconnecting signal input cable.

11.4.2 Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

11.4.3 Water drop on the surface or condensation as panel power on will corrode panel electrode.

11.4.4 As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

11.4.5 In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.

11.5 Design notes on touch panel

11.5.1 Explanation of each boundary of touch panel

A .Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

B .Viewing area

a. Cosmetic inspection to be done for this area.

This area is set as inside of boundary of double-sided adhesive with tolerance.

C .Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

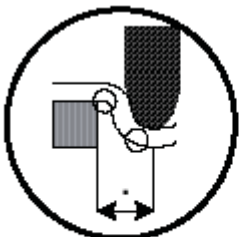
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

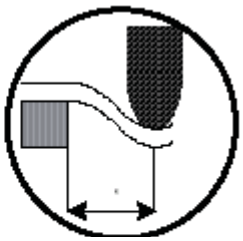
D .Active area

a. This area is where the performance is guaranteed.

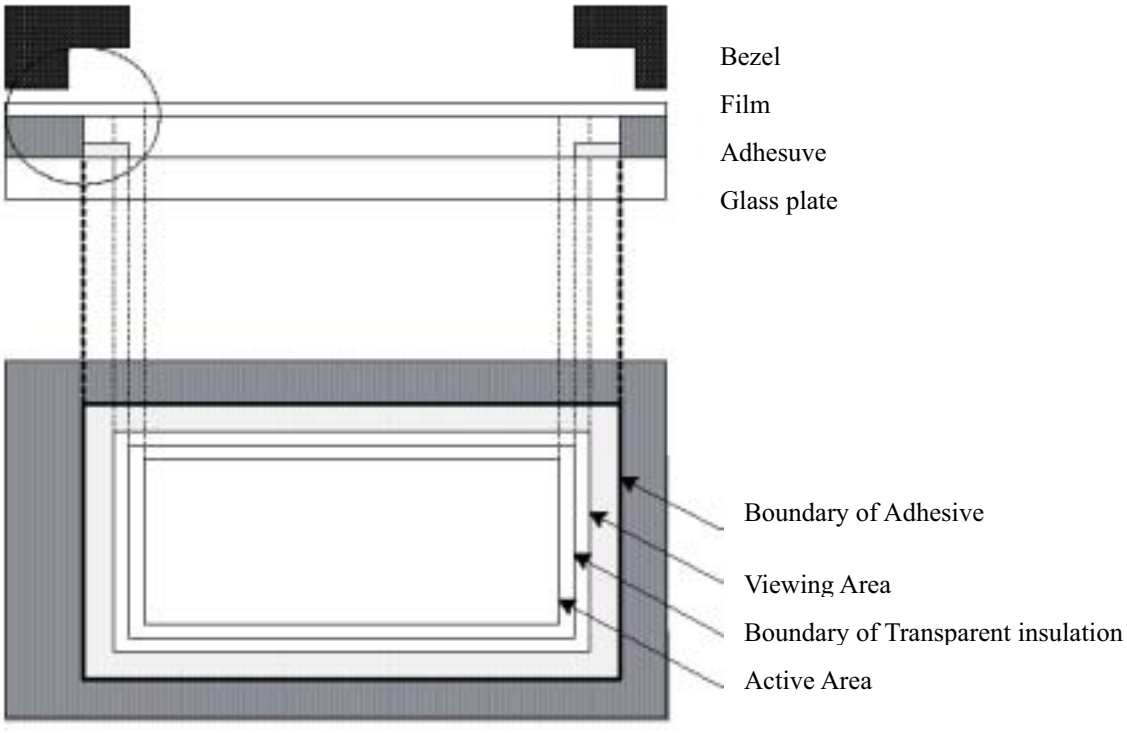
This area set as 2.3mm inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.



There is some possibility to damage ITO



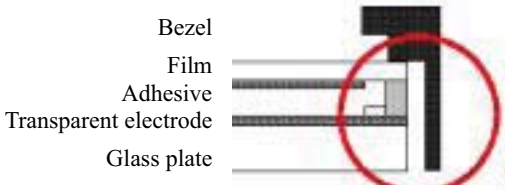
No Damage to ITO



11.5.2 Housing and touch panel

A. Please have clearance between the side of touch panel and any conductive material such as metal frame (Drawing.1). Transparent electrode exists on glass of touch panel from end to end.

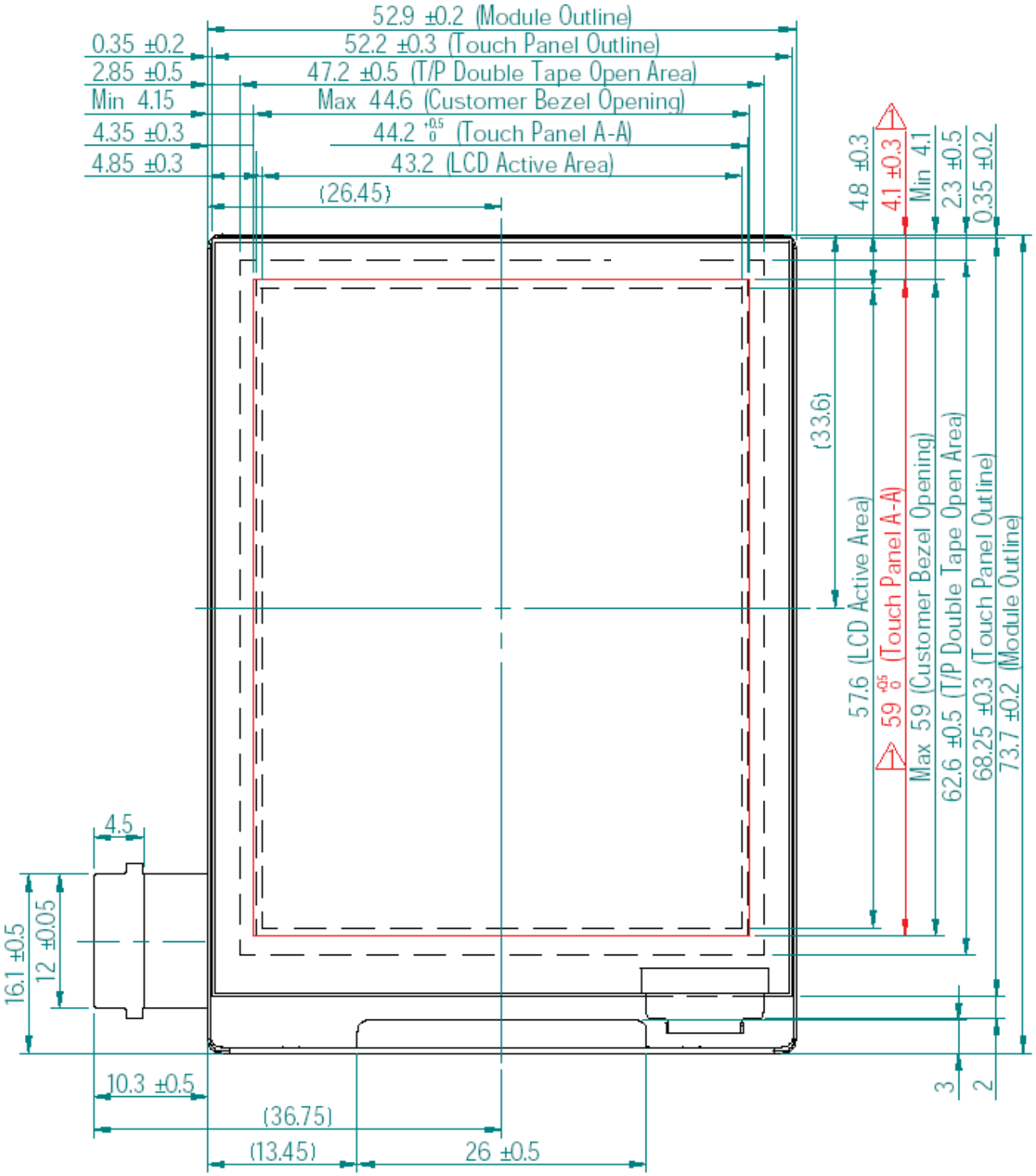
B. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause the malfunction.

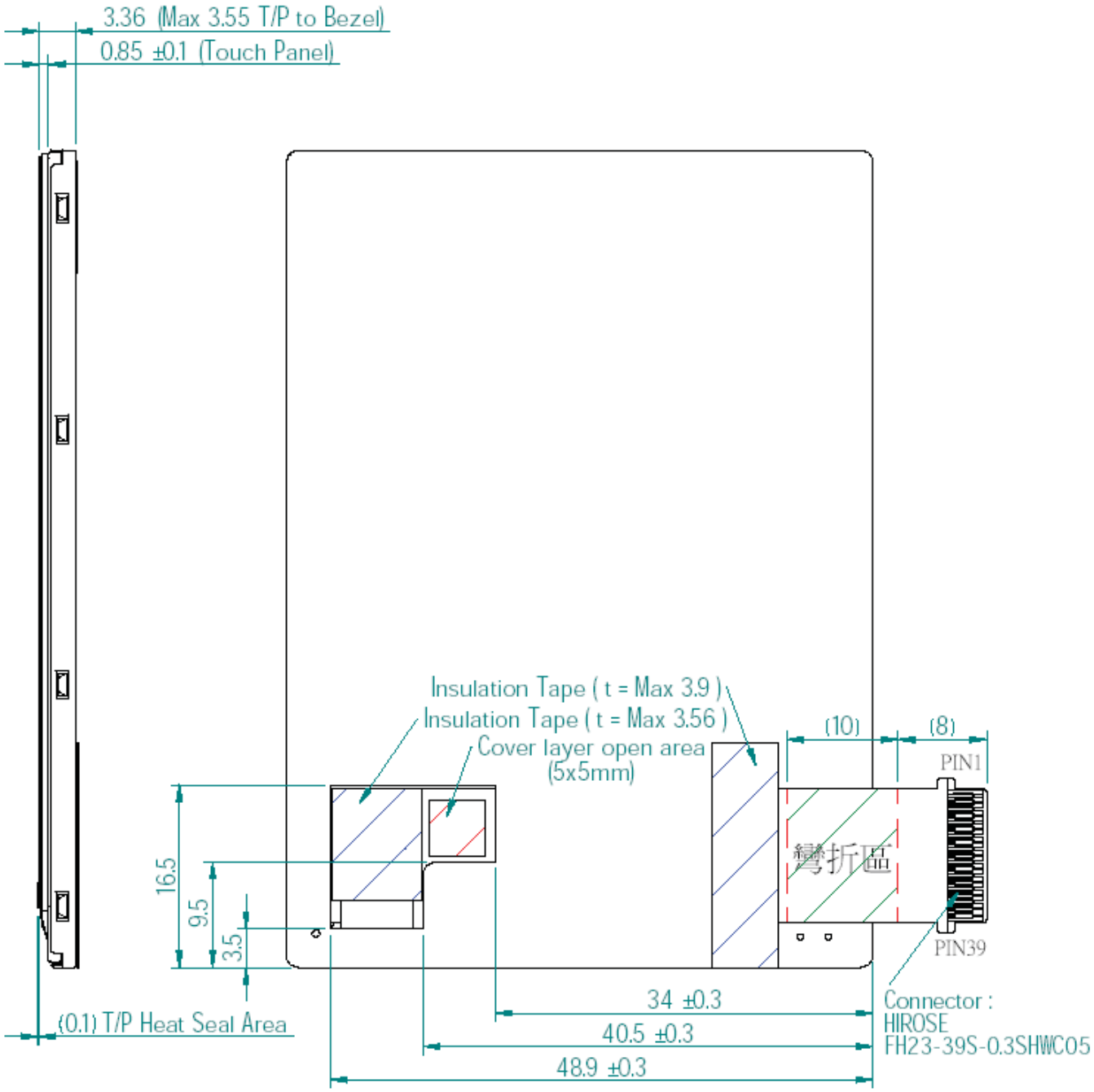


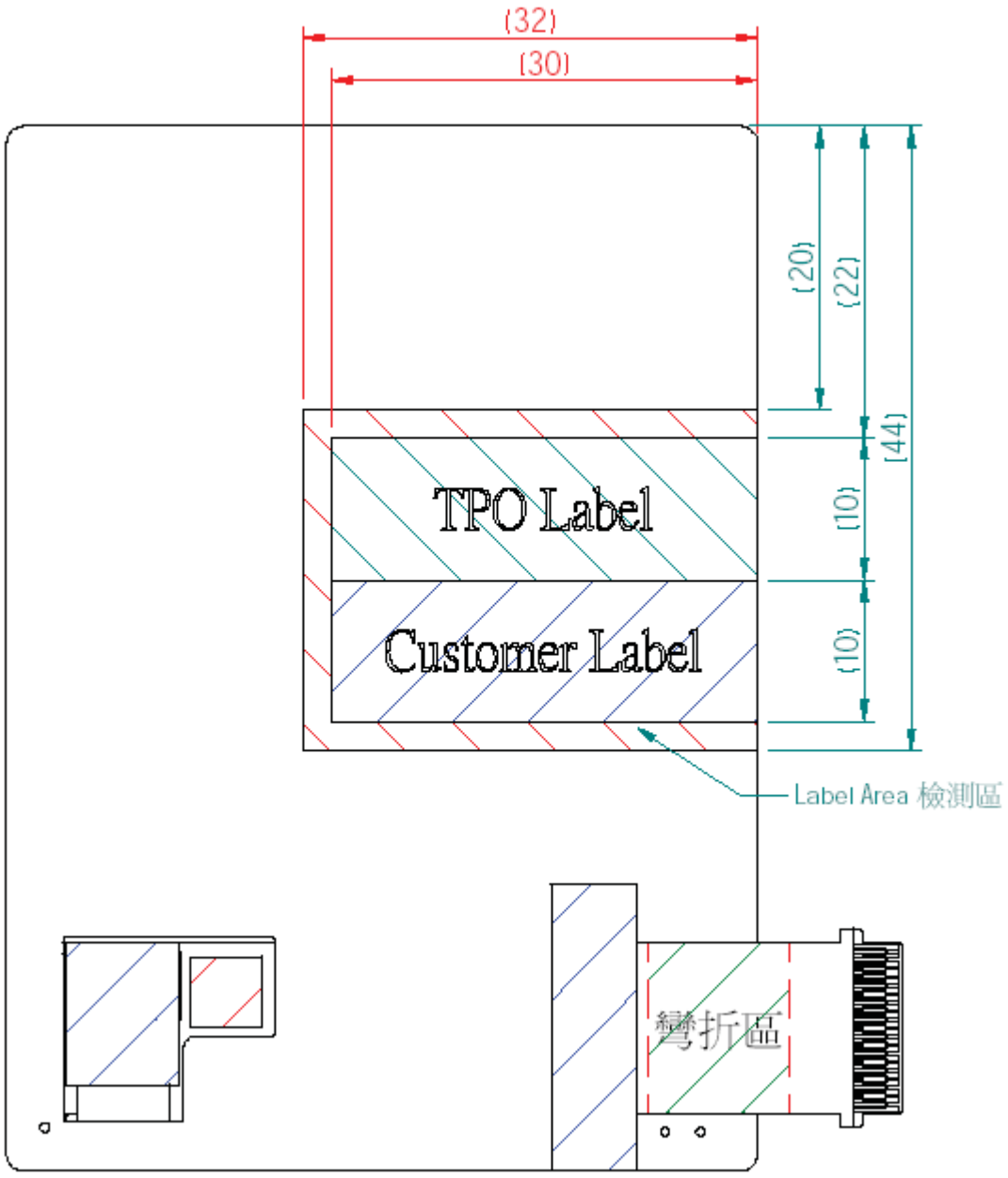
Drawing 1

Drawing 2

12. Mechanical Drawing



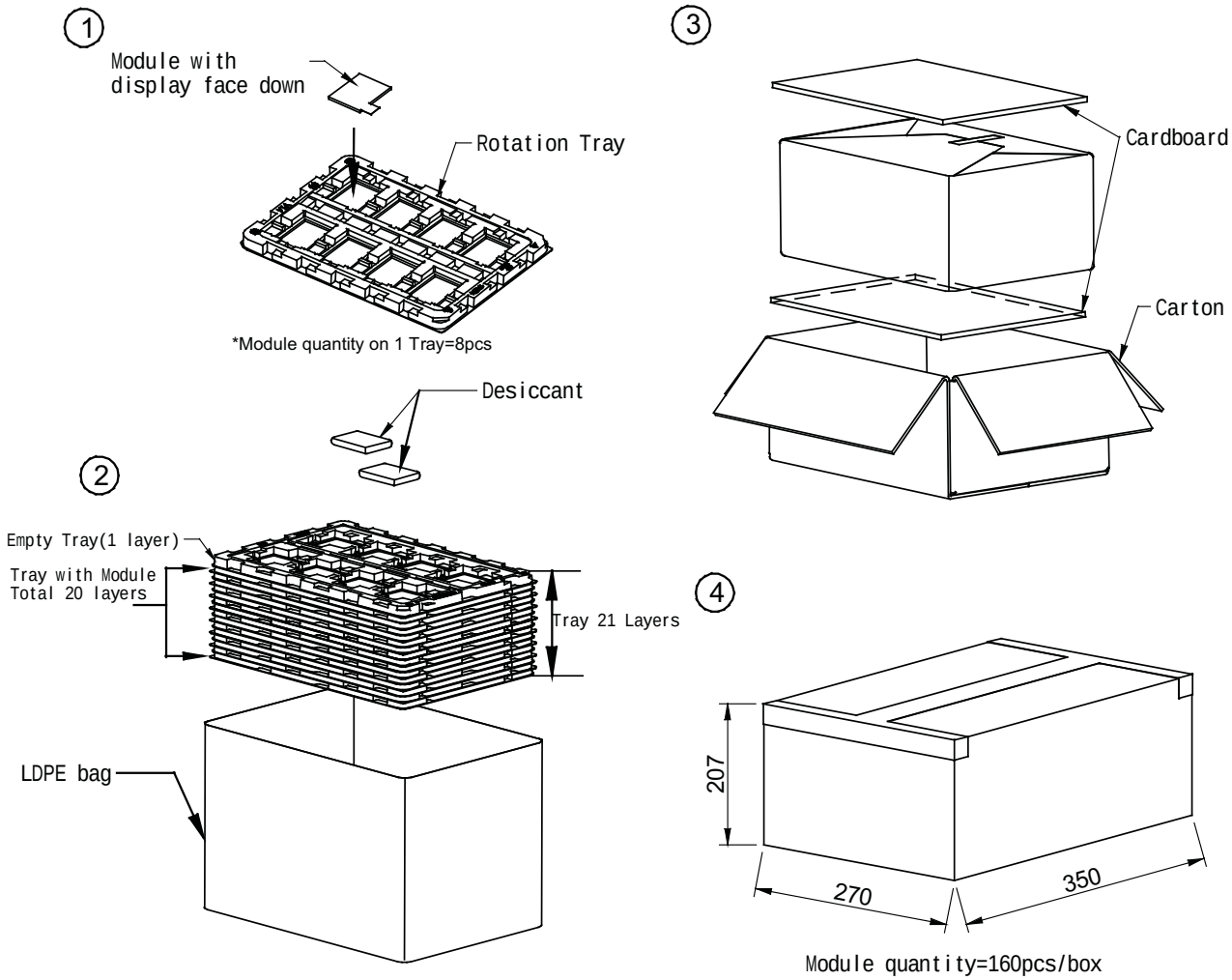




Note:

1.Please design the bezel not to contact with the T/P upper electrode film. Otherwise, T/P may input incorrectly by giving the force to the bezel, and we recommend using the bezel material which is hard to bend.
2.The tolerance of module height is excluded warp of the shield case and the FPC.
3.Please design the bezel cushion within the T/P double tape area.
4.The dimension without tolerance is for reference only.

13. Packing Drawing



TD028TTEB5 Module delivery packing method:

13.1 Packed the module into tray cavity(with display face down) .

13.2 Stacking the tray with 15 layers and with 1 empty tray above the stacking tray unit. Place 2pcs desiccants above the empty tray and pack the stacking tray unit into LDPE bag.

13.3 Place 1 pc cardboard inside the carton bottom, and place the package unit into the carton, then cover 1pc cardboard at top of the package unit.

13.4 Sealing the carton with adhesive tape.