LINEAR TECHNOLOGY

IN THIS ISSUE…

LT LINEAR TECHNOLOGY

LTC1406: 8-Bit, 20MHz ADC Offers 250MHz Input Bandwidth and Tiny Footprint

by Jeff Huehn

LTC Goes High Speed

Everyone knows about Linear Technology's linear and switching regulators, but over the last several years Linear has built an impressive family of data conversion products. With the recent introduction of fast 12-bit and 14-bit ADCs, and, most recently, a 16-bit part, the family continues to expand. Now, the newest member of the LTC converter family, the LTC1406, takes LTC in a new direction: high speed for communications and video conversion.

LTC1406 Features

❑ 20Msps sample rate, 8-bit parallel output
❑ 250MHz internal sample-and-hold
❑ 48.5dB S/(N + D) and 62dB THD
❑ 7.0 effective bits at 70MHz
❑ ±1LSB DNL and INL Max
❑ Low power with power-down mode
❑ Small footprint: 24-pin narrow SSOP package

Why Use Linear Technology?

There are other 8-bit, 20Msps converters on the market, so why use the LTC1406? The LTC1406 has several significant advantages over its seemingly similar competitors.

Wide Input Bandwidth for Communications

One very useful advantage is the extremely wideband sample-and-hold. The 250MHz input bandwidth of the LTC1406 allows for undersampling of very high frequency signals. Coupled with its excellent distortion, the LTC1406 has better high frequency undersampling performance than any other 8-bit, 20MHz part on the market. The signal-to-(noise + distortion) ratio is a nearly ideal 48.5dB for low frequencies; it stays flat all the way out to 10MHz. Even at 70MHz, well beyond the Nyquist frequency of 10MHz, the signal-to-(noise + distortion) ratio is still close to 44dB, which is equivalent to 7.0 ENOBs (effective number of bits). Figure 1 illustrates this outstanding performance along with the spurious free dynamic range (SFDR). For applications in communications, or any application that depends on high dynamic range and a high number of effective bits at very high input frequencies, the LTC1406 outperforms the competition.
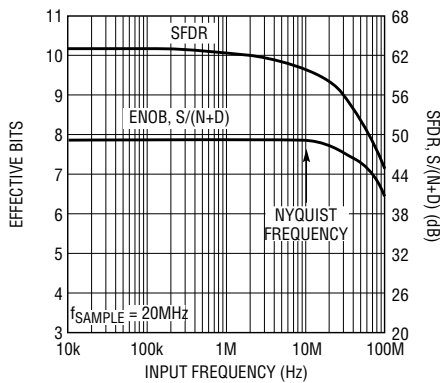
Small Footprint

Is board space a problem? The LTC1406 is also the smallest 8-bit, 20MHz part available. It comes in the tiny GN-24 package that occupies only 52mm² (only 1.75 times the size of an

Figure 1. LTC1406 SINAD and SFDR plot shows 7 effective bits at 70MHz input frequency.

LTC1406, continued from page 1

SO-8 package). It also requires only three surface mount bypass capacitors, one for the analog, digital, and output logic supplies, one for the reference input (V_{REF}) and one for the V_{BIAS} pin, resulting in a small layout footprint in addition to a small package.

Low Power Shutdown Mode

The low power consumption of the LTC1406 can be reduced even further by taking advantage of the Shutdown mode. Taking the $\overline{SHDN}$ pin low powers down the converter and bias circuitry so that the part draws only a tiny leakage current from the supply. This can reduce power consumption in portable and battery-powered equipment whenever the converter is idle.

Overrange/ Underrange Detection

Another feature unique to the LTC1406 is the ability to detect an overrange or underrange condition using the Overflow/Underflow bit. The OF/UF output will transition from 0 to 1 at 1LSB below the 0000 0000 to 0000 0001 transition and 1LSB above the 1111 1110 to 1111 1111 transition, providing a clear indicator that the input signal is outside the full-scale conversion range of the converter. This can be used as a flag when trimming the input span to maximize the signal-to-noise ratio. For imaging applications where the output of a CCD varies from pixel to pixel, for communications applications where the magnitude of the input signal is constantly changing or for any application where the input span varies, the LTC1406 makes it easy to optimize performance.

Ease of Use with Flexibility

Trying to make a high speed data converter perform used to be somewhere near the magic end of the "science–magic scale." It was also generally true that the more flexibility (the more options the user had for connecting the part), the more difficult it was to get the part to work properly. The LTC1406 changes that: it was designed to make it easy to get good performance and to be very easy to use without sacrificing flexibility. It starts with very simple, straightforward connections. A power supply, a reference, a clock and an input are all you need to start converting high speed signals into ones and zeros.

Connecting the supply voltage is a good example of the simplicity and flexibility built into the LTC1406. In the simplest configuration, connect the analog, digital and output logic supplies together to a single 5V supply and bypass capacitor and you're done. If you need to interface with 3V logic, the LTC1406 is ready for that too. The logic inputs are set up to work equally well with 3V or 5V signals and the output logic supply (O_{VDD}) can be connected to a separate 3V supply to provide 3V data out. This eliminates the need for circuitry to level shift a 3V clock up to 5V and/or level shift the entire 5V data bus back down to 3V.

The reference is also easier to provide. Rather than the conventional half-flash architecture that requires two reference voltages, two bypass capacitors and two buffer amplifiers for the top and bottom of the reference ladder, the LTC1406 requires only one 2.5V reference and bypass capacitor. This is really an advantage when changing or trimming the input span. Instead of moving both the top and bottom voltages to obtain the correct span, the single 2.5V reference functions as a gain control. It also requires less current, and therefore less power, from the reference, since there is no resistive ladder to drive. The typical reference current required is about 1mA (5mW) compared to about 7mA (35mW) for most of the half-flash architectures.

Flexible Analog Inputs

Easy to Drive

One of the strongest features of the LTC1406 is the structure of the inputs. The inputs are very easy to drive. Following the rising clock edge, the LTC1406 goes into track mode and, like other converters, the inputs draw a small current spike to charge the input sampling capacitors. However, the input capacitance is typically one-fourth that of competitive parts, so the current spike necessary to charge them is much smaller. While the clock is high, the voltage across the sampling capacitors will track the voltage on the inputs. Again, this small input capacitance makes the inputs much easier to drive, particularly for high input frequencies. Reducing the capacitive load by 70%–80% greatly reduces the input-buffer-amplifier requirement and may eliminate the need for a buffer amplifier altogether.
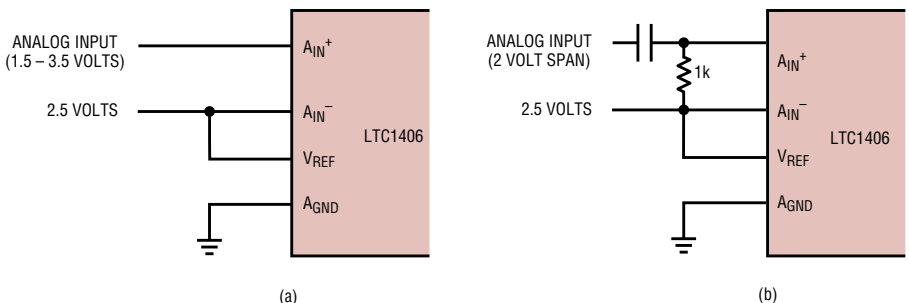
Figure 2. (a) Using $A_{IN}+$ as the input and connecting $A_{IN}–$ to V_{REF} yields an input span of 1.5V– 3.5V. (b) AC coupling the input yields a 2V AC-coupled span.
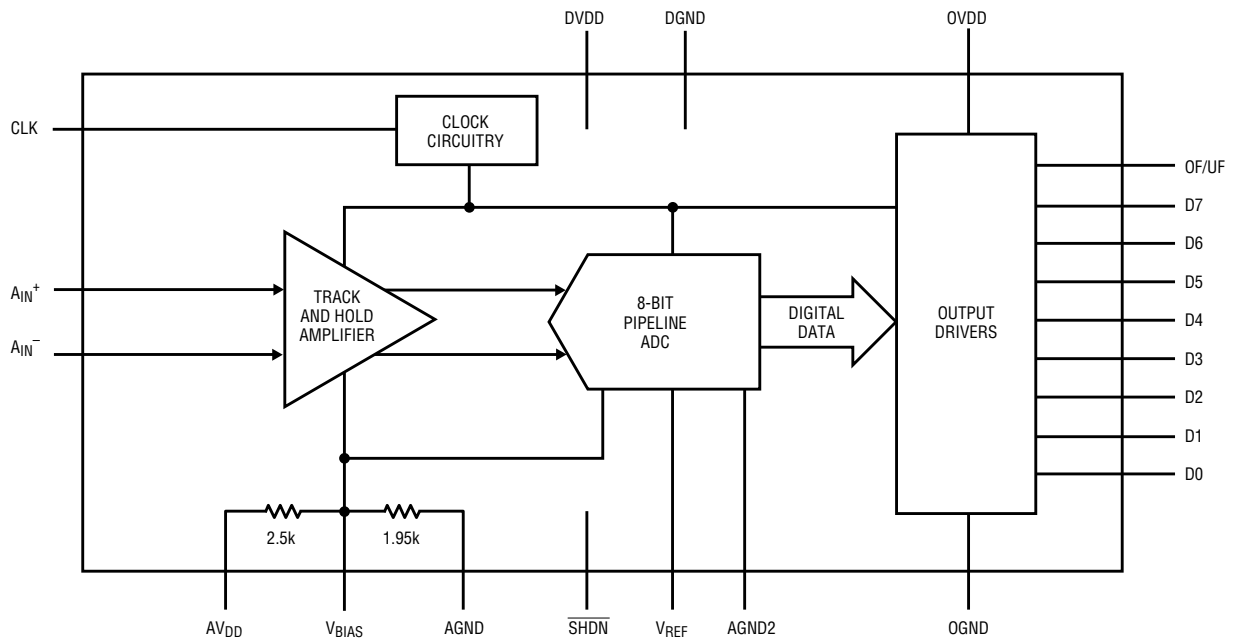
Figure 3. The LTC1406 has a wideband differential track-and-hold that can capture input signals of up to 230MHz. The separate output supply and grounding pins allow for easy interface to 3V logic.

On the falling clock edge, the part samples the input voltage; the inputs draw only a small leakage current while the clock is low.

Differential or Single-Ended

The LTC1406's inputs are truly differential; they will always convert the difference between $A_{IN}+$ and $A_{IN}-$. The maximum output code (1111 1111) occurs when $A_{IN}+ - (A_{IN}-) = 1V$ and the minimum output code (0000 0000) occurs when $A_{IN}+ - (A_{IN}-) = -1V$. These differential inputs also have outstanding common mode rejection, so that any noise or unwanted signal that is common to both inputs will be rejected. However, the inputs need not be driven differentially to achieve good performance. If a differential signal is present, the differential inputs can be connected directly. If the input signal is single ended, there is no need for a complicated transformer to create a differential signal; the LTC1406 will handle a single-ended signal as easily as a differential signal. The $A_{IN}-$ input can be tied to a common mode voltage and $A_{IN}+$ becomes the signal input, with a $\pm1V$ span centered around $A_{IN}-$. Again, to simplify the hookup $A_{IN}-$ can be connected to V_{REF} resulting in an input span of 1.5V–3.5V as shown in Figure 2a.

Rail-to-Rail Common Mode

Another nice feature of the LTC1406 input structure is that the inputs have a common mode range that extends to either rail. In single-ended mode, the 2V input span can extend from 0V–2V to 3V–5V. The $\pm1V$ differential-input span can also extend between the rails. This allows for direct coupling to a wide range of inputs without any additional circuitry. In addition, the input can be AC coupled to allow for a 2V input span centered around virtually any common mode voltage (see Figure 2b).
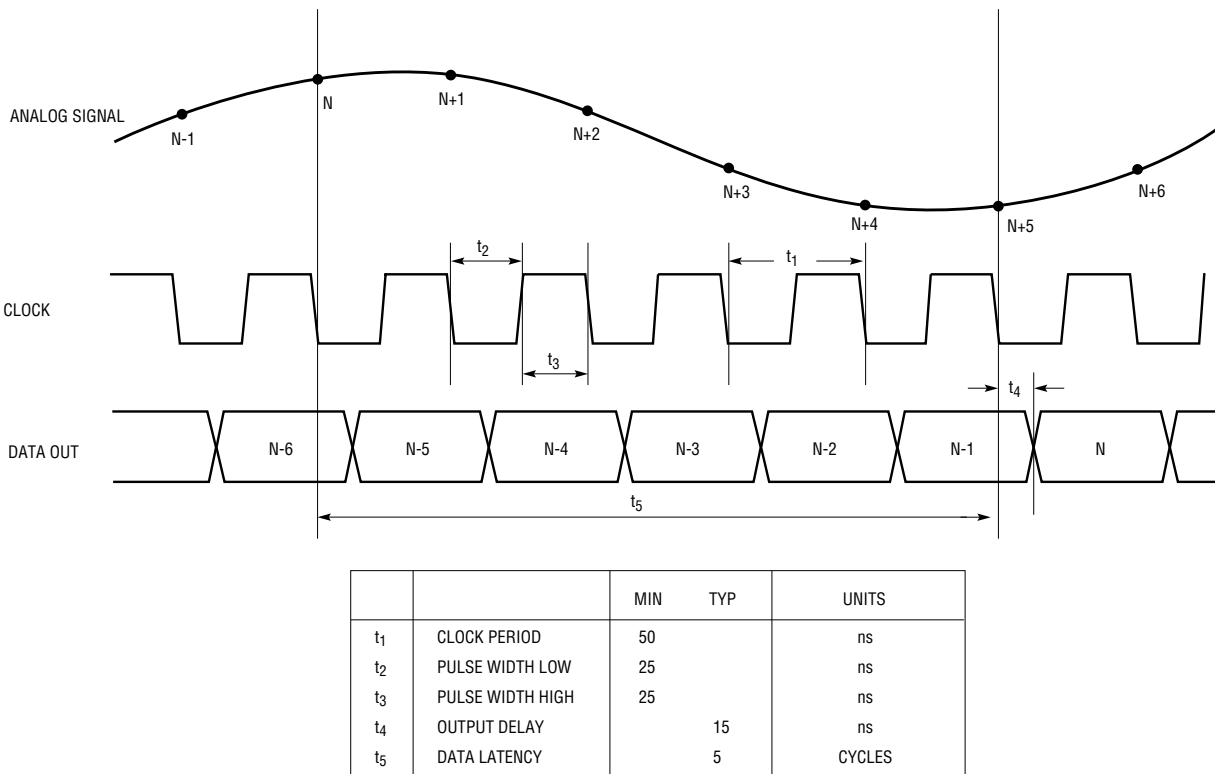
Keys to Using High Speed ADCs

The LTC1406 uses an internal sample-and-hold and a pipeline quantizing architecture to convert an analog signal to an 8-bit parallel output. The input is sampled on the falling clock edge, converted into an internal differential voltage and fed into a comparator to determine the most significant bit. The result of that decision is subtracted from the sample and the residue is multiplied by two and then passed on to the next stage via a similar sample-and-hold. This continues down the eight pipeline stages. The comparator outputs are then combined in a digital error-correction circuit into an 8-bit parallel word. Figure 3 is a block diagram of the LTC1406.

The one-bit-per-stage pipeline architecture of the LTC1406 is very similar to the half-flash or subranging architecture (sometimes also referred to as pipeline, the difference being the number of bits determined in each comparator cycle) used in other 8-bit, 20MHz converters. However, if you are more familiar with the successive approximation register (SAR) architecture used in many lower speed, higher resolution converters (including most of Linear Technology's converters), there are some things you need to know about high speed ADCs.

Almost all high speed converters have latency in the output data. This is defined as the delay, usually expressed as a number of clock cycles, from the sampling of the analog input to the appearance of the conversion data on the digital outputs. The most common architecture for 8-bit, 20MHz converters, the half-flash, typically has a delay of 2.5 clock cycles. The

		MIN	TYP	UNITS
t_1	CLOCK PERIOD	50		ns
t_2	PULSE WIDTH LOW	25		ns
t_3	PULSE WIDTH HIGH	25		ns
t_4	OUTPUT DELAY		15	ns
t_5	DATA LATENCY		5	CYCLES

Figure 4. As with all pipeline ADCs, there is latency in the output data. Output data is available from the LTC1406 5 cycles after the input is sampled and the conversion starts.

data latency of the LTC1406, as well as other 8-bit, one-bit-per-stage, pipeline converters, is five clock cycles. Each falling clock edge samples the input and starts a conversion. The digital representation of that sample will be available as an 8-bit parallel word following the fifth falling edge after the start of conversion. So although each conversion takes five clock cycles, a new conversion result is available on each falling edge. Figure 4 clearly illustrates the relationship between the sampled analog input and when the output data is available.

Another important consideration when using a high speed converter is the sampling clock. Most high speed converters use both phases of the clock, so it is critical to maintain a 50% duty cycle. During each clock phase, half of the stages of the ADC are sampling and half are amplifying. At conversion speeds below the maximum conversion rate, the duty cycle can deviate from 50% with no degradation in performance. At the maximum conversion rate it is important to maintain a 50% duty

cycle clock. It is also important to provide a clock that has low jitter and fast rise and fall times (<2ns).

Finally, much of the internal circuitry operates dynamically, resulting in two important consequences. First, as with most high speed ADCs, there is a lower limit on the conversion speed. The minimum conversion speed of the LTC1406 is 10kHz. Second, some high speed ADCs, including the LTC1406, are dynamically biased and the bias must be periodically refreshed. Under normal, free-running conversion conditions, the bias is refreshed during each clock cycle. However, when power is first applied or the clock stops for longer than 100µs (for example, in Shutdown mode), the part must typically be clocked for 20 clock cycles at a sample rate of greater than 10kHz before the output data will be valid.

Easy, Clean, Small Layout

One of the reasons that high speed converters can de difficult to use is that the board layout becomes extremely critical for high input fre-

quencies. The layout in Figure 5 shows how easy it is to get a clean, tight layout using the LTC1406 even when connecting the output logic to the digital supply and ground—it's almost automatic. It also illustrates the advantage of the tiny GN-24 package relative to the standard SO-24. The pinout is designed for a smooth flow from analog input signal to digital output. All of the supplies, reference, and analog inputs are located on one side of the part and the clock input and digital data outputs are on the other. This allows for easy separation of the analog and digital ground planes and helps to prevent digital noise from coupling into the analog inputs. As mentioned earlier, the LTC1406 requires very few external components and the pinout is designed to allow the bypass capacitors to be located very close to the package. This close bypassing minimizes lead inductance and sensitivity to currents flowing in the ground plane, which can be critical when the whole system is clocking at 20MHz.
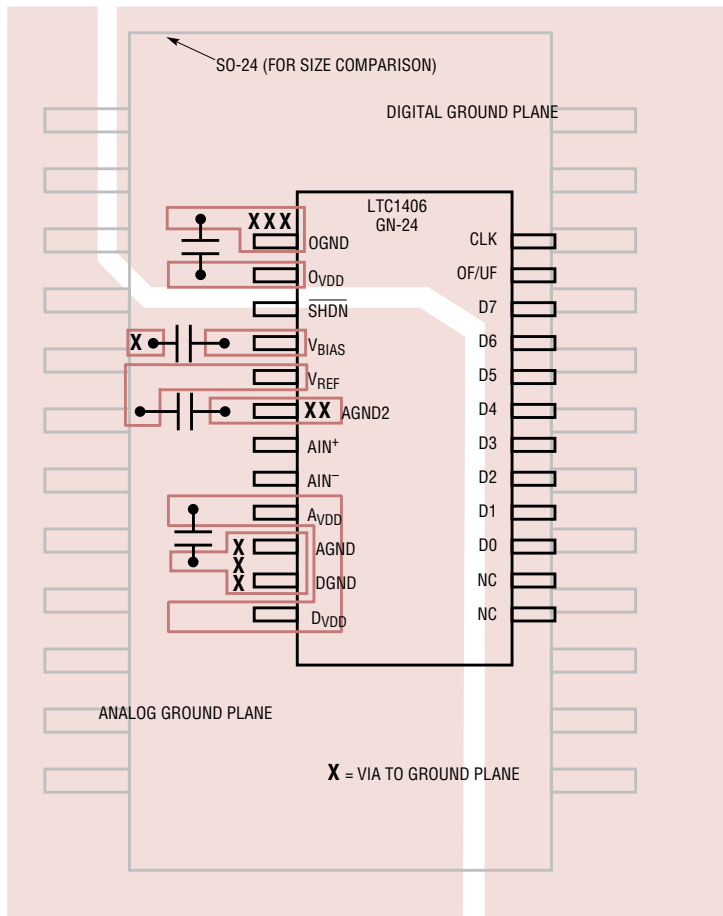
Clean, Wideband Undersampling Performance

All of the features and advantages of the LTC1406 wouldn't mean a thing without outstanding performance. Fortunately, the LTC1406 has it. Extremely low noise combined with low distortion and wide input bandwidth make the LTC1406 a great performer over an extremely wide range of input frequencies. As shown in Figure 1, the signal-to-(noise + distortion) ratio stays nearly flat out to 10MHz. Figure 6 shows a FFT plot for an input frequency of 30MHz and provides an even clearer picture of the low distortion and high spurious free dynamic range for frequencies beyond the Nyquist frequency of 10MHz.

Conclusion

The LTC1406 has everything high speed designers need: wide input bandwidth, great high frequency and undersampling performance, the smallest package of any 8-bit, 20MHz converter available and a host of features that make it easy to use and easy to get maximum performance. Linear Technology and the LTC1406 will be welcome additions to high speed data conversion.

Figure 5. The tiny footprint of the LTC1406 saves board spacecompared to an SO-24. A clean layout includes short bypass loops and separation of analog and digital signals
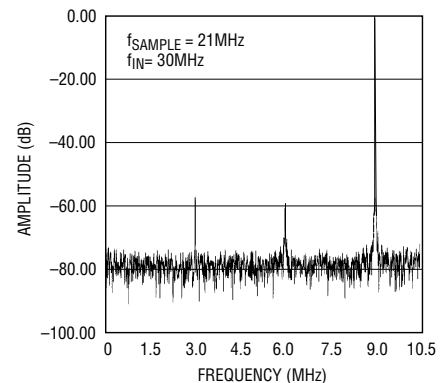
Figure 6. An FFT plot of the LTC1406 shows outstanding performance for high input frequencies: the S/(N + D) si 47dB and the SFDR is 56dB for an input frequency of 30MHz.