

# DATA SHEET

## **BST84**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical  
D-MOS transistor

BST84

DESCRIPTION

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

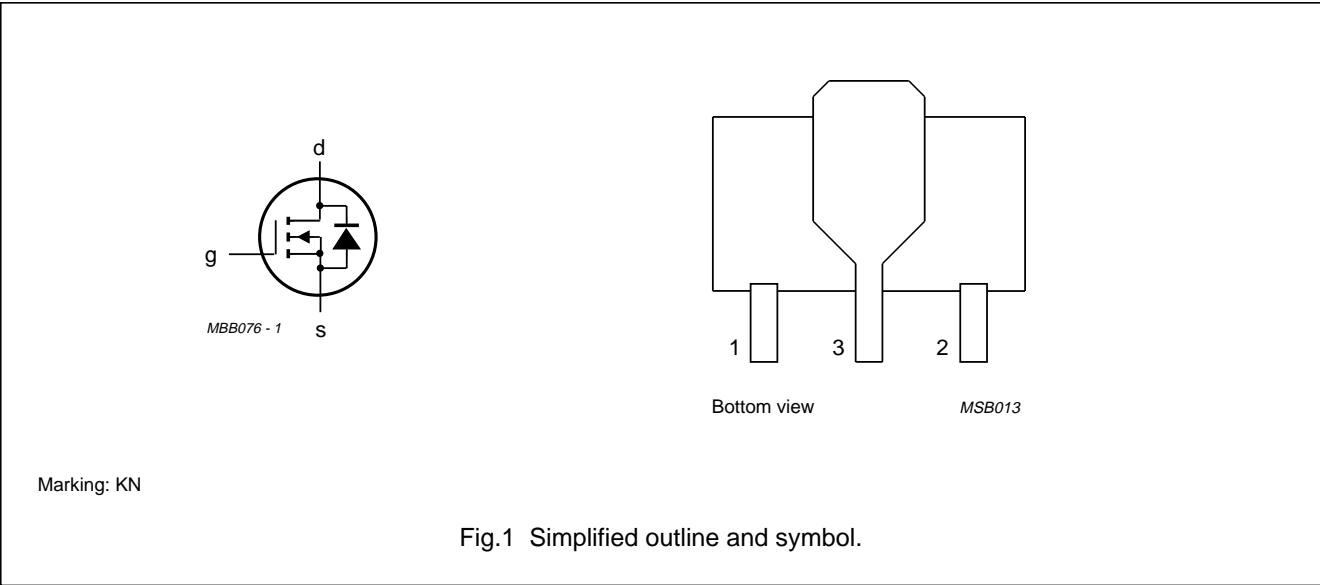
QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$I_D$	max.	250	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	1	W
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	6 12	$\Omega$
Transfer admittance $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	250	mS

PINNING - SOT89

- 1 = source
- 2 = gate
- 3 = drain

PIN CONFIGURATION



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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Drain current (peak)	$I_{DM}$	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ (note 1)	$P_{tot}$	max.	1 W
Storage temperature range	$T_{stg}$		$-65$ to $+150\text{ }^{\circ}\text{C}$
Junction temperature	$T_j$	max.	$150\text{ }^{\circ}\text{C}$

### THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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### Note

1. Transistor mounted on a ceramic substrate with area of  $2.5\text{ cm}^2$  and thickness of 0.7 mm.

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**CHARACTERISTICS**
 $T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Drain-source breakdown voltage

 $I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$ 
 $V_{(BR)DSS}$  min. 200 V

Drain-source leakage current

 $V_{DS} = 160\text{ V}; V_{GS} = 0$ 
 $I_{DSS}$  max. 10  $\mu\text{A}$ 

Gate-source leakage current

 $V_{GS} = 20\text{ V}; V_{DS} = 0$ 
 $I_{GSS}$  max. 100 nA

Gate threshold voltage

 $I_D = 1\text{ mA}; V_{DS} = V_{GS}$ 
 $V_{GS(th)}$  min. 0.8 V  
max. 2.8 V

Drain-source ON-resistance

 $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$ 
 $R_{DS(on)}$  typ. 6  $\Omega$   
max. 12  $\Omega$ 

Transfer admittance

 $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$ 
 $|Y_{fs}|$  typ. 250 mS

 Input capacitance at  $f = 1\text{ MHz}$ 
 $V_{DS} = 10\text{ V}; V_{GS} = 0$ 
 $C_{iss}$  typ. 70 pF  
max. 90 pF

 Output capacitance at  $f = 1\text{ MHz}$ 
 $V_{DS} = 10\text{ V}; V_{GS} = 0$ 
 $C_{oss}$  typ. 20 pF  
max. 30 pF

 Feedback capacitance at  $f = 1\text{ MHz}$ 
 $V_{DS} = 10\text{ V}; V_{GS} = 0$ 
 $C_{rss}$  typ. 5 pF  
max. 10 pF

Switching times (see Figs 2 and 3)

 $I_D = 250\text{ mA}; V_{DD} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$ 
 $t_{on}$  typ. 4 ns  
max. 10 ns

 $t_{off}$  typ. 15 ns  
max. 25 ns

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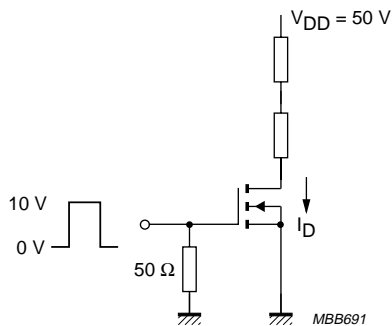


Fig.2 Switching times test circuit.

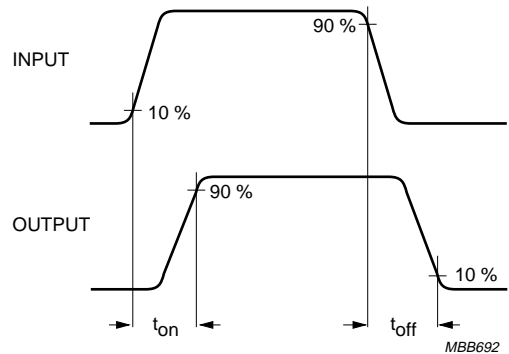


Fig.3 Input and output waveforms.

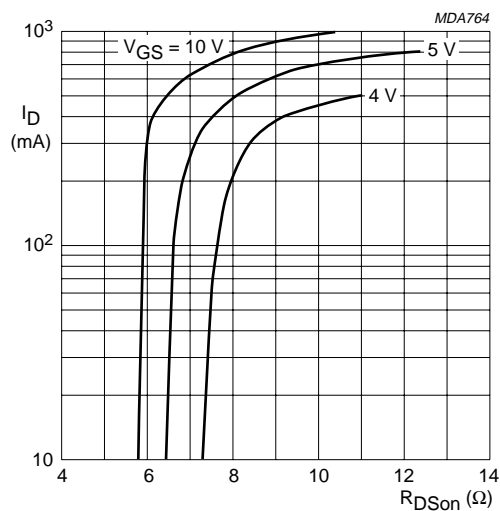


Fig.4  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

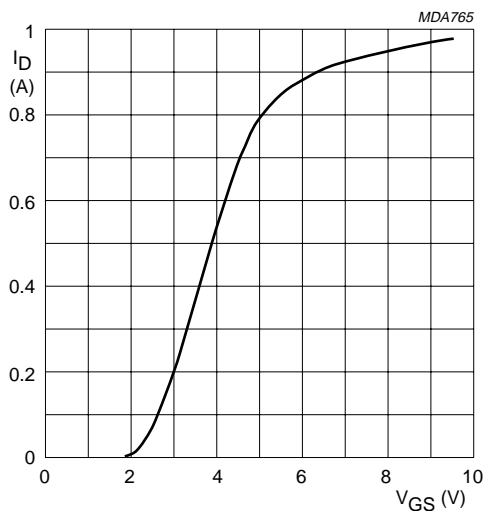
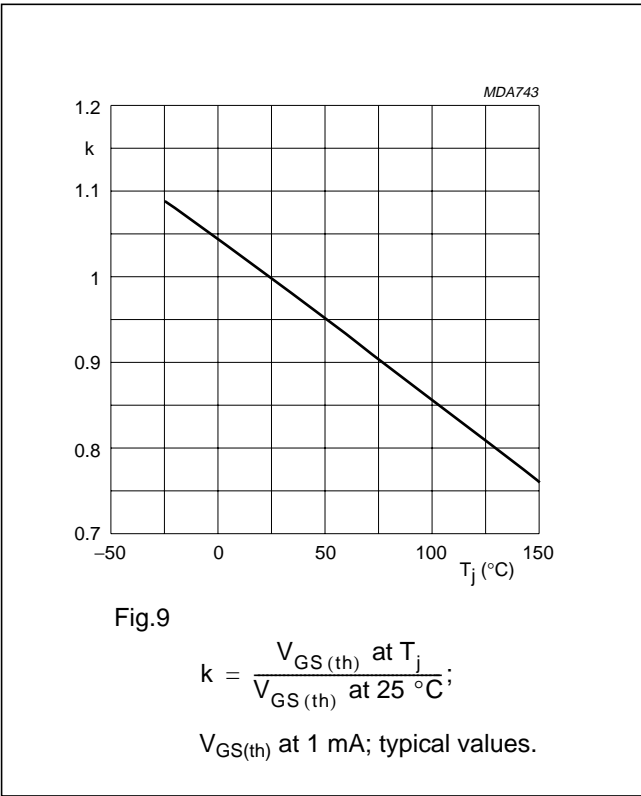
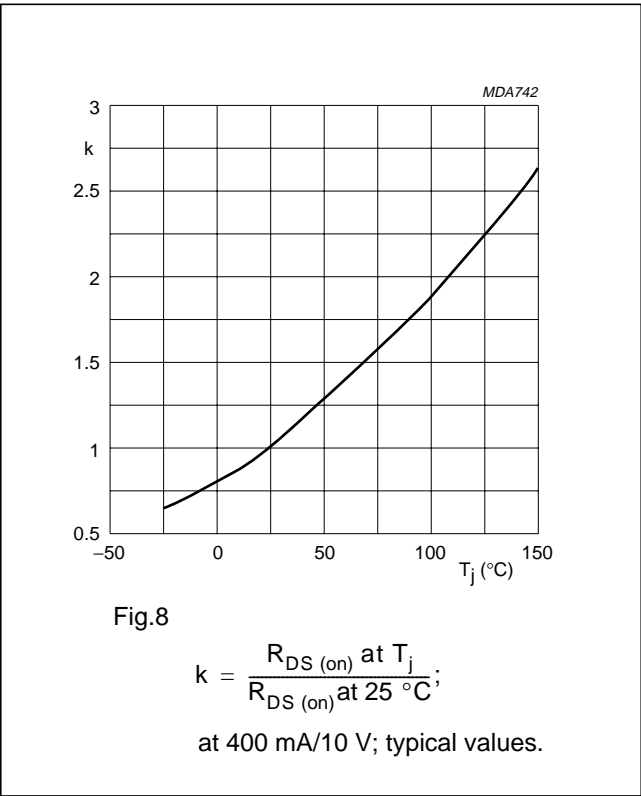
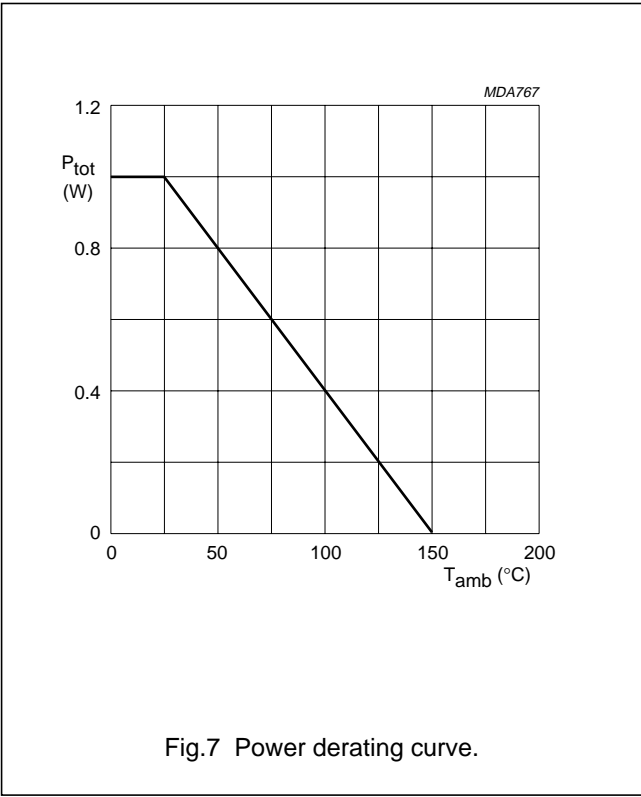
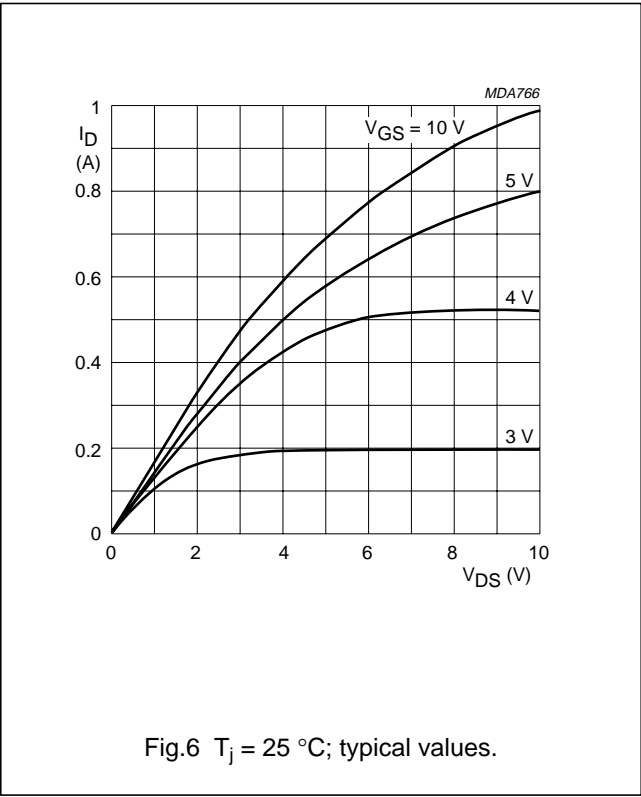


Fig.5  $T_j = 25\text{ }^\circ\text{C}$ ;  $V_{DS} = 10$  V; typical values.

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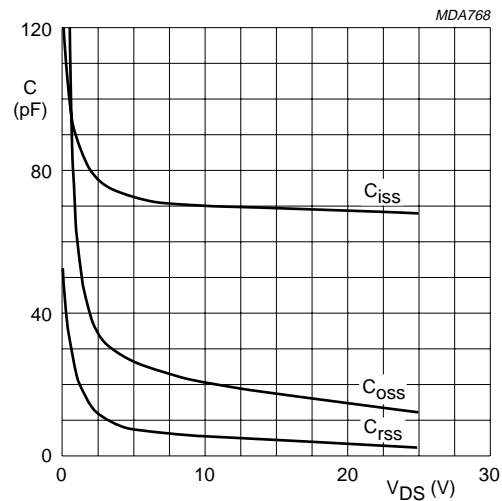


Fig.10  $T_j = 25\text{ }^{\circ}\text{C}$ ;  $V_{GS} = 0$ ;  $f = 1\text{ MHz}$ ; typical values.

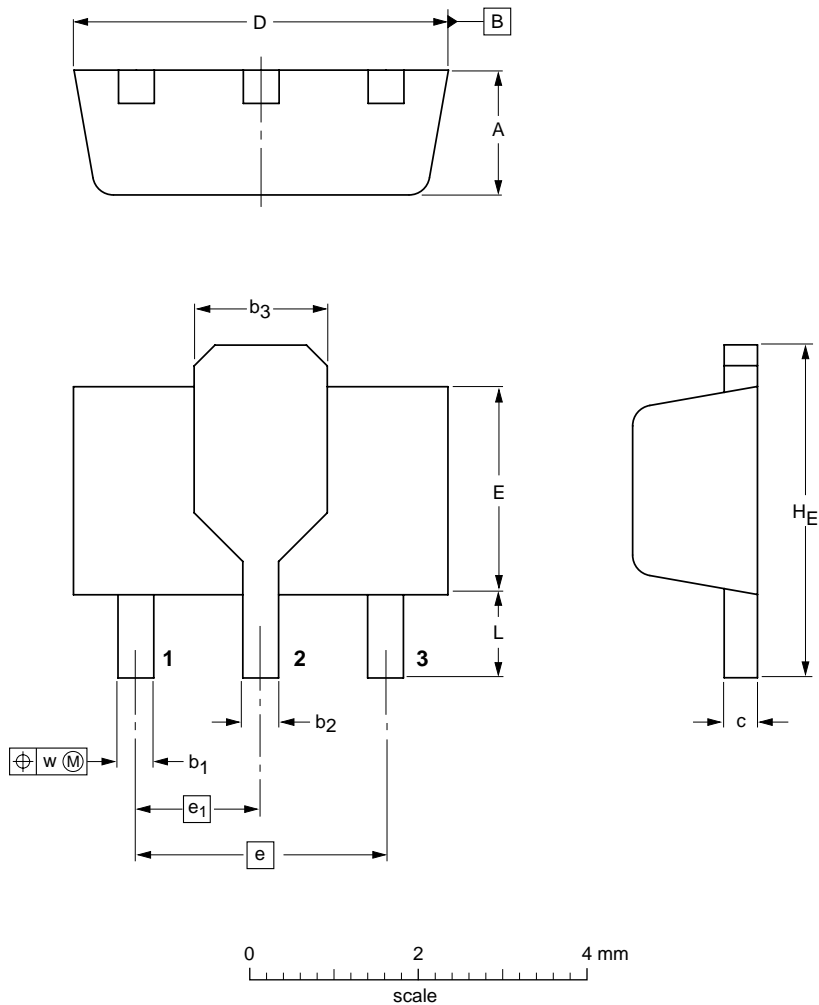
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PACKAGE OUTLINES


Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28



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**BST84****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**BST84****NOTES**

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**NOTES**

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