

ADVANCED DC/DC CONVERTERS

Fang Lin Luo
Hong Ye



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Dedicated to
Our respected great lady Mme. Liao Jing
Ms. Luo Yuan Zhi and her family

Preface

The purpose of this book is to provide up-to-date information on advanced DC/DC converters that is both concise and useful for engineering students and practicing professionals. It is well organized in 748 pages with 320 diagrams to introduce more than 100 topologies of the advanced DC/DC converters originally developed by the authors. EMI/EMC reduction and various DC voltage sources are also illustrated in this book. All prototypes represent novel approaches and great contributions to modern power engineering.

Power engineering is the method used to supply electrical energy from a source to its users. It is of vital importance to industry. It is likely that the air we breathe and water we drink are taken for granted until they are not there. Energy conversion technique is the main focus of power engineering. The corresponding equipment can be divided into four groups:

- AC/AC transformers
- AC/DC rectifiers
- DC/DC converters
- DC/AC inverters

From recent reports, the production of DC/DC converters occupies the largest percentage of the total turnover of all conversion equipment production. DC/DC conversion technology is progressing rapidly. According to incomplete statistics, there are more than 500 topologies of DC/DC converters existing, with new topologies created every year. It is a lofty undertaking to treat the large number of DC/DC converters. The authors have sorted these converters into six generations since 2001. This systematical work is very helpful for DC/DC converter's evolution and development. The converters are listed below:

1. First generation (classical/traditional) converters
2. Second generation (multiple-quadrant) converters
3. Third generation (switched component) converters
4. Fourth generation (soft-switching) converters
5. Fifth generation (synchronous rectifier) converters
6. Sixth generation (multiple-element resonant power) converters

A review of the DC/DC conversion technique development reveals that the idea was induced from other equipment. Transformers successfully convert an AC source voltage to other AC output voltage(s) with very high efficiency. Rectifier devices such as diode, transistor, and thyristor effectively rectify an AC source voltage to DC output voltage. Nearly eight decades ago, people sought to invent equipment to convert a DC source voltage to another DC output voltage(s) with high efficiency. Unfortunately, no such simple apparatus such as a transformer and/or rectifier was found for DC/DC conversion purpose.

High frequency switch-on and -off semiconductor devices paved the way for chopper circuits. This invention inspired the idea for DC/DC conversion. Therefore, the fundamental DC/DC converters were derived from the corresponding choppers. At present, the fundamental converters — Buck converter, Boost converter, and Buck-Boost converter — are still the basic circuits for DC/DC conversion technique in research and development.

The voltage-lift technique is a popular method that is widely applied in electronic circuit design. Applying this technique effectively overcomes the effects of parasitic elements and greatly increases the output voltage. Therefore, these DC/DC converters can convert the source voltage into a higher output voltage with high power efficiency, high power density, and simple structure. It is applied in the periodical switching circuit. Usually, a capacitor is charged during switch-on by a certain voltage. This charged capacitor voltage can be arranged on top-up to output voltage during switch-off. Therefore, the output voltage can be lifted. A typical example is the sawtooth-wave generator with voltage-lift circuit.

The voltage-lift technique has been successfully employed in the design of DC/DC converters. However, its output voltage increases in arithmetic progression, stage by stage. The super-lift technique is a great achievement in DC/DC conversion technology. It is more powerful than the voltage-lift technique; the output voltage transfer gain of super-lift converters can be very high, which increases in geometric progression, stage by stage. It effectively enhances the voltage transfer gain in power series. Four series of super-lift converters created by the authors are introduced in this book. Some industrial applications verified their versatile and powerful characteristics.

Multiple-quadrant operation is often required in industrial applications. Most publications in the literature concentrate on the single-quadrant operation. This fact is reasonable since most novel approaches were derived from its simple structure. To compensate for these losses, the authors have spent much time and spirit to develop multiple-quadrant converters, positive-negative converters in various generations.

This book is organized in 18 chapters. The DC/DC conversion technique is introduced in [Chapter 1](#) and the voltage lift converters in [Chapter 2](#). Chapters 3 to 6 introduce the four series super-lift converters. [Chapter 7](#) introduces the second generation converters; and [Chapter 8](#), the third generation converters. Chapters 9 and 10 introduce the two-series multiple-lift push-pull switched-capacitor converters. [Chapter 11](#) introduces the fourth

generation converters and [Chapter 12](#) the fifth generation converters. Chapters 13 to 16 introduce the sixth generation converters. [Chapter 17](#) introduces various DC voltage sources; and [Chapter 18](#) introduces the gating-signal generator, EMI/EMC, and some applications.

The authors are pioneers in DC/DC conversion technology. They have devoted many years to this research area and created a large number of outstanding converters, including world-renowned series DC/DC converters, namely, Luo-Converters, which cover all six generation converters. Super-lift converters are our favorite achievement in our 20-years' research fruits. Our biographies and information are provided on the following page.

Our acknowledgment goes to the executive editor for this book.

Dr. Fang Lin Luo and Dr. Hong Ye

*Nanyang Technological University
Singapore*

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Introduction

Conversion technique is a major research area in the field of power electronics. The equipment for conversion techniques have applications in industry, research and development, government organizations, and daily life. The equipment can be divided in four technologies:

- AC/AC transformers
- AC/DC rectifiers
- DC/DC converters
- DC/AC inverters

According to incomplete statistics, there have been more than 500 prototypes of DC/DC converters developed in the past six decades. All existing DC/DC converters were designed to meet the requirements of certain applications. They are usually called by their function, for example, Buck converter, Boost converter and Buck-Boost converter, and zero current switching (ZCS) and zero voltage switching (ZVS) converters. The large number of DC/DC converters had not been evolutionarily classified until 2001. The authors have systematically classified the types of converters into six generations according to their characteristics and development sequence. This classification grades all DC/DC converters and categorizes new prototypes. Since 2001, the DC/DC converter family tree has been built and this classification has been recognized worldwide. Following this principle, it is now easy to sort and allocate DC/DC converters and assess their technical features.

1.1 Historical Review

DC/DC conversion technology is a major subject area in the field of power engineering and drives, and has been under development for six decades. DC/DC converters are widely used in industrial applications and computer hardware circuits. DC/DC conversion techniques have developed very

quickly. Statistics show that the DC/DC converter worldwide market will grow from U.S. \$3336 million in 1995 to U.S. \$5128 million in the year 2004 with a compound annual growth rate (CAGR) of 9%.* This compares to the AC/DC power supply market, which will have a CAGR of only about 7.5% during the same period. In addition to its higher growth rate, the DC/DC converter market is undergoing dramatic changes as a result of two major trends in the electronics industry: low voltage and high power density. From this investigation it can be seen that the production of DC/DC converters in the world market is much higher than that of AC/DC converters.

The DC/DC conversion technique was established in the 1920s. A simple voltage conversion, the simplest DC/DC converter is a voltage divider (such as rheostat, potential-meter, and so on), but it only transfers output voltage lower than input voltage with poor efficiency. The multiple-quadrant chopper is the second step in DC/DC conversion. Much time has been spent trying to find equipment to convert the DC energy source of one voltage to another DC actuator with another voltage, as does a transformer employed in AC/AC conversion.

Some preliminary types of DC/DC converters were used in industrial applications before the Second World War. Research was blocked during the war, but applications of DC/DC converters were recognized. After the war, communication technology developed very rapidly and required low voltage DC power supplies. This resulted in the rapid development of DC/DC conversion techniques. Preliminary prototypes can be derived from choppers.

1.2 Multiple-Quadrant Choppers

Choppers are the circuits that convert fixed DC voltage to variable DC voltage or pulse-width-modulated (PWM) AC voltage. In this book, we concentrate on its first function.

1.2.1 Multiple-Quadrant Operation

A DC motor can run in forward running or reverse running. During the forward starting process its armature voltage and armature current are both positive. We usually call this forward motoring operation or *quadrant I* operation. During the forward braking process its armature voltage is still positive and its armature current is negative. This state is called the forward regenerating operation or *quadrant II* operation. Analogously, during the reverse starting process the DC motor armature voltage and current are both negative. This reverse motoring operation is called the *quadrant III* operation.

* Figures are taken from the Darnell Group News report on *DC-DC Converters: Global Market Forecasts, Demand Characteristics and Competitive Environment* published in February 2000.

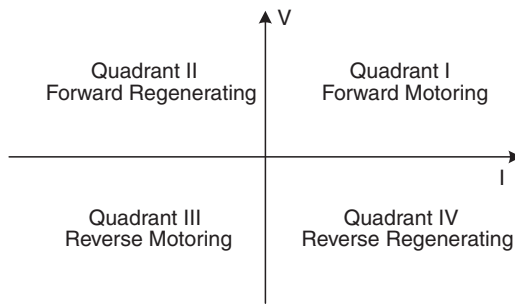


FIGURE 1.1
Four-quadrant operation.

During reverse braking process its armature voltage is still negative and its armature current is positive. This state is called the reverse regenerating operation *quadrant IV* operation.

Referring to the DC motor operation states; we can define the multiple-quadrant operation as below:

Quadrant I operation: forward motoring, voltage is positive, current is positive

Quadrant II operation: forward regenerating, voltage is positive, current is negative

Quadrant III operation: reverse motoring, voltage is negative, current is negative

Quadrant IV operation: reverse regenerating, voltage is negative, current is positive

The operation status is shown in the Figure 1.1. Choppers can convert a fixed DC voltage into various other voltages. The corresponding chopper is usually named according to its quadrant operation chopper, e.g., the first-quadrant chopper or “A”-type chopper. In the following description we use the symbols V_{in} as the fixed voltage, V_p the chopped voltage, and V_O the output voltage.

1.2.2 The First-Quadrant Chopper

The first-quadrant chopper is also called “A”-type chopper and its circuit diagram is shown in [Figure 1.2a](#) and corresponding waveforms are shown in [Figure 1.2b](#). The switch S can be some semiconductor devices such as BJT, IGBT, and MOSFET. Assuming all parts are ideal components, the output voltage is calculated by the formula,

$$V_O = \frac{t_{on}}{T} V_{in} = kV_{in} \quad (1.1)$$

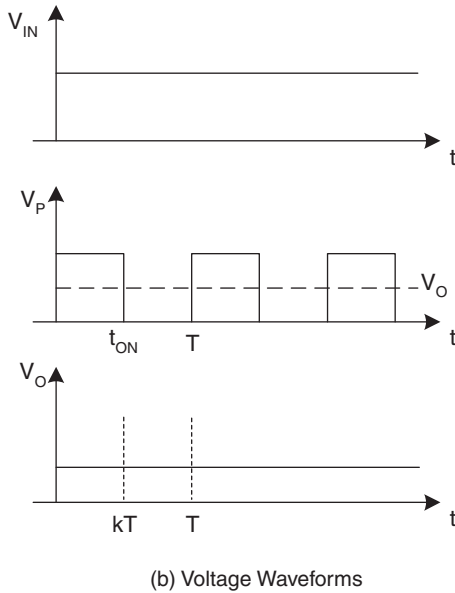
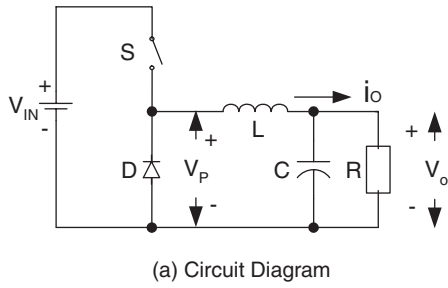


FIGURE 1.2

The first-quadrant chopper.

where T is the repeating period $T = 1/f$, f is the chopping frequency, t_{on} is the switch-on time, k is the conduction duty cycle $k = t_{on}/T$.

1.2.3 The Second-Quadrant Chopper

The second-quadrant chopper is the called “B”-type chopper and the circuit diagram and corresponding waveforms are shown in [Figure 1.3a and b](#). The output voltage can be calculated by the formula,

$$V_O = \frac{t_{off}}{T} V_{in} = (1 - k) V_{in} \quad (1.2)$$

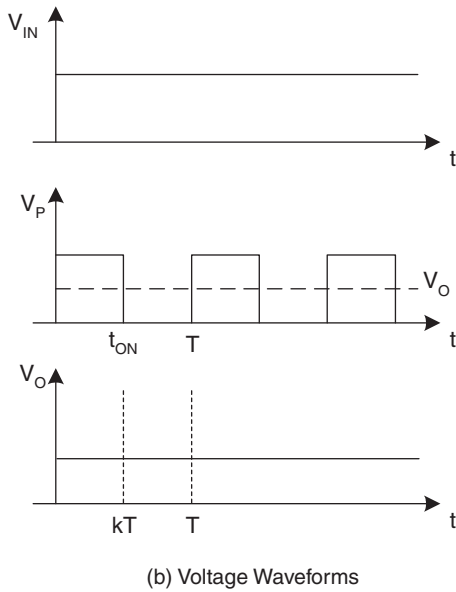
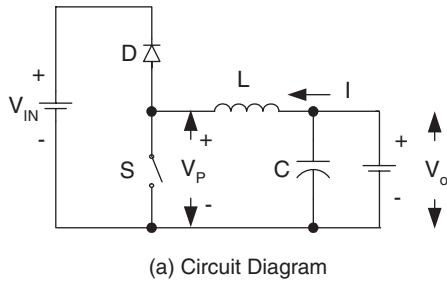


FIGURE 1.3

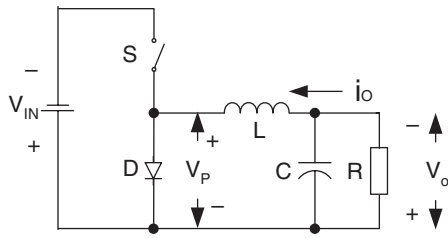
The second-quadrant chopper.

where T is the repeating period $T = 1/f$, f is the chopping frequency, t_{off} is the switch-off time $t_{off} = T - t_{on}$, and k is the conduction duty cycle $k = t_{on}/T$.

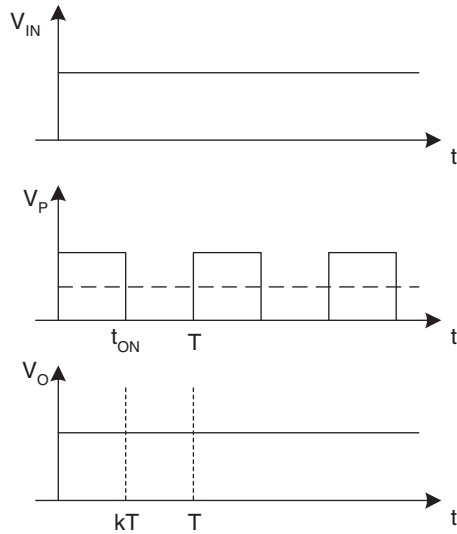
1.2.4 The Third-Quadrant Chopper

The third-quadrant chopper and corresponding waveforms are shown in [Figure 1.4a and b](#). All voltage polarity is defined in the figure. The output voltage (absolute value) can be calculated by the formula,

$$V_O = \frac{t_{on}}{T} V_{in} = kV_{in} \quad (1.3)$$



(a) Circuit Diagram



(b) Voltage Waveforms

FIGURE 1.4

The third-quadrant chopper.

where t_{on} is the switch-on time, and k is the conduction duty cycle $k = t_{on}/T$.

1.2.5 The Fourth-Quadrant Chopper

The fourth-quadrant chopper and corresponding waveforms are shown in [Figure 1.5a and b](#). All voltage polarity is defined in the figure. The output voltage (absolute value) can be calculated by the formula,

$$V_O = \frac{t_{off}}{T} V_{in} = (1 - k) V_{in} \quad (1.4)$$

where t_{off} is the switch-off time $t_{off} = T - t_{on}$, time, and k is the conduction duty cycle $k = t_{on}/T$.

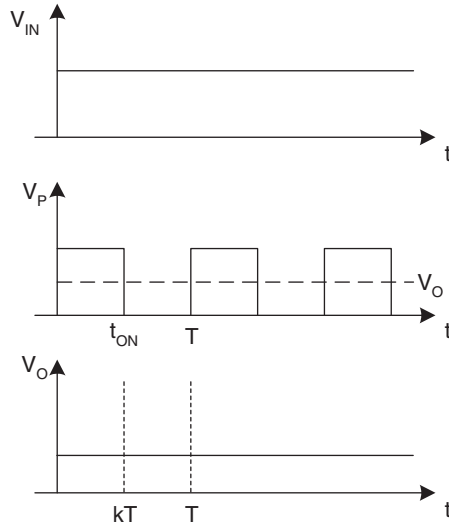
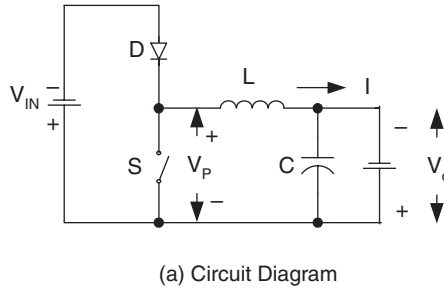


FIGURE 1.5
The fourth-quadrant chopper.

1.2.6 The First and Second Quadrant Chopper

The first and second quadrant chopper is shown in [Figure 1.6](#). Dual quadrant operation is usually requested in the system with two voltage sources V_1 and V_2 . Assume that the condition $V_1 > V_2$, and the inductor L is an ideal component. During quadrant I operation, S_1 and D_2 work, and S_2 and D_1 are idle. Vice versa, during quadrant II operation, S_2 and D_1 work, and S_1 and D_2 are idle. The relation between the two voltage sources can be calculated by the formula,

$$V_2 = \begin{cases} kV_1 & \text{QI_operation} \\ (1-k)V_1 & \text{QII_operation} \end{cases} \quad (1.5)$$

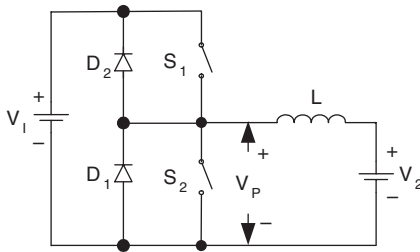


FIGURE 1.6
The first-second quadrant chopper.

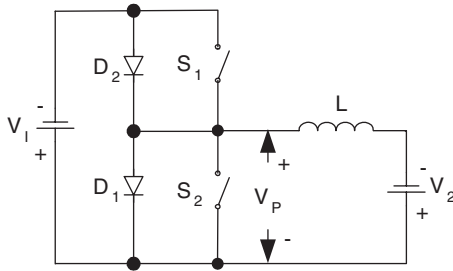


FIGURE 1.7
The third-fourth quadrant chopper.

where k is the conduction duty cycle $k = t_{on}/T$.

1.2.7 The Third and Fourth Quadrant Chopper

The third and fourth quadrant chopper is shown in Figure 1.7. Dual quadrant operation is usually requested in the system with two voltage sources V_1 and V_2 . Both voltage polarity is defined in the figure, we just concentrate their absolute values in analysis and calculation. Assume that the condition $V_1 > V_2$, the inductor L is ideal component. During quadrant I operation, S_1 and D_2 work, and S_2 and D_1 are idle. Vice versa, during quadrant II operation, S_2 and D_1 work, and S_1 and D_2 are idle. The relation between the two voltage sources can be calculated by the formula,

$$V_2 = \begin{cases} kV_1 & \text{QIII_operation} \\ (1-k)V_1 & \text{QIV_operation} \end{cases} \quad (1.6)$$

where k is the conduction duty cycle $k = t_{on}/T$.

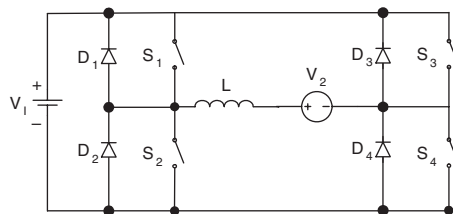


FIGURE 1.8
The four-quadrant chopper.

TABLE 1.1

The Switches and Diode's Status for Four-Quadrant Operation

Switch or Diode	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
S_1	Works	Idle	Idle	Works
D_1	Idle	Works	Works	Idle
S_2	Idle	Works	Works	Idle
D_2	Works	Idle	Idle	Works
S_3	Idle	Idle	On	Idle
D_3	Idle	Idle	Idle	On
S_4	On	Idle	Idle	Idle
D_4	Idle	On	Idle	Idle
Output	$V_2 +, I_2 +$	$V_2 +, I_2 -$	$V_2 -, I_2 -$	$V_2 -, I_2 +$

1.2.8 The Four-Quadrant Chopper

The four-quadrant chopper is shown in Figure 1.8. The input voltage is positive, output voltage can be either positive or negative. The switches and diode status for the operation are shown in Table 1.1. The output voltage can be calculated by the formula,

$$V_2 = \begin{cases} kV_1 & QI_operation \\ (1-k)V_1 & QII_operation \\ -kV_1 & QIII_operation \\ -(1-k)V_1 & QIV_operation \end{cases} \quad (1.7)$$

1.3 Pump Circuits

The electronic pump is a major component of all DC/DC converters. Historically, they can be sorted into four groups:

- Fundamental pumps
- Developed pumps
- Transformer-type pumps
- Super-lift pumps

1.3.1 Fundamental Pumps

Fundamental pumps are developed from fundamental DC/DC converters just like their name:

- Buck pump
- Boost pump
- Buck-boost pump

All fundamental pumps consist of three components: a switch S , a diode D , and an inductor L .

1.3.1.1 Buck Pump

The circuit diagram of the buck pump, and some current waveforms are shown in [Figure 1.9](#). Switch S and diode D are alternately on and off. Usually, the buck pump works in continuous operation mode, inductor current is continuous in this case.

1.3.1.2 Boost Pump

The circuit diagram of the boost pump, and some current waveforms are shown in [Figure 1.10](#). Switch S and diode D are alternately on and off. The inductor current is usually continuous.

1.3.1.3 Buck-Boost Pump

The circuit diagram of the buck-boost pump and some current waveforms are shown in [Figure 1.11](#). Switch S and diode D are alternately on and off. Usually, the buck-boost pump works in continuous operation mode, inductor current is continuous in this case.

1.3.2 Developed Pumps

Developed pumps are created from the developed DC/DC converters just like their name:

- Positive Luo-pump
- Negative Luo-pump
- Cúk-pump

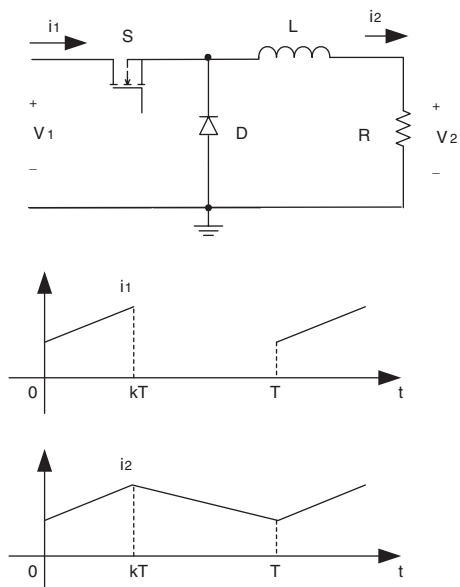


FIGURE 1.9
Buck pump.

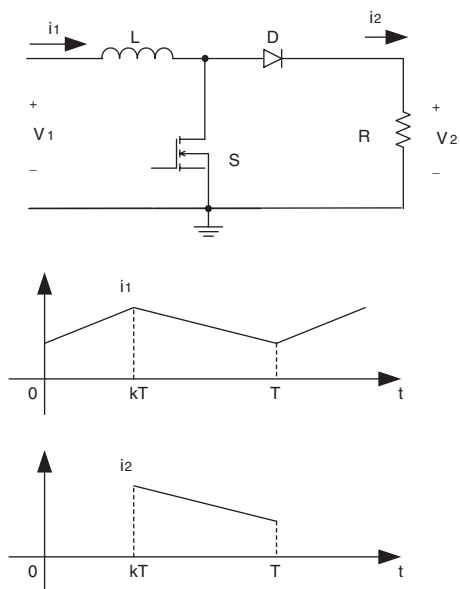


FIGURE 1.10
Boost pump.

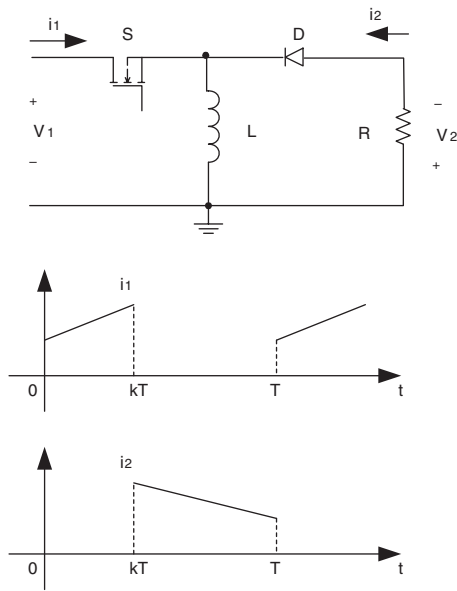


FIGURE 1.11
Buck-boost pump.

All developed pumps consist of four components: a switch S , a diode D , a capacitor C , and an inductor L .

1.3.2.1 Positive Luo-Pump

The circuit diagram of the positive Luo-pump and some current and voltage waveforms are shown in Figure 1.12. Switch S and diode D are alternately on and off. Usually, this pump works in continuous operation mode, inductor current is continuous in this case. The output terminal voltage and current is usually positive.

1.3.2.2 Negative Luo-Pump

The circuit diagram of the negative Luo-pump and some current and voltage waveforms are shown in Figure 1.13. Switch S and diode D are alternately on and off. Usually, this pump works in continuous operation mode, inductor current is continuous in this case. The output terminal voltage and current is usually negative.

1.3.2.3 Cúk-Pump

The circuit diagram of the Cúk pump and some current and voltage waveforms are shown in Figure 1.14. Switch S and diode D are alternately on and off. Usually, the Cúk pump works in continuous operation mode, inductor current is continuous in this case. The output terminal voltage and current is usually negative.

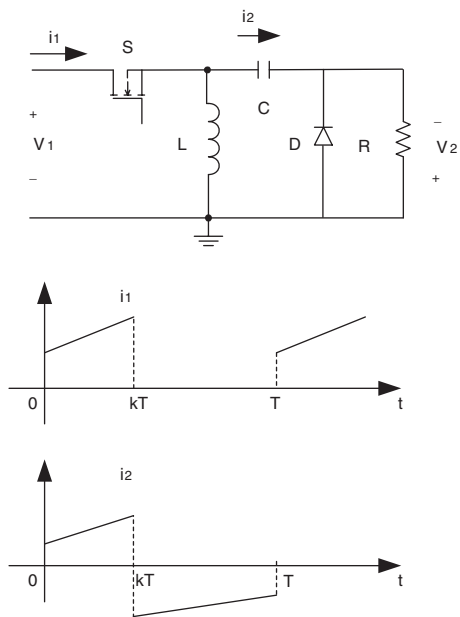


FIGURE 1.12
Positive Luo-pump.

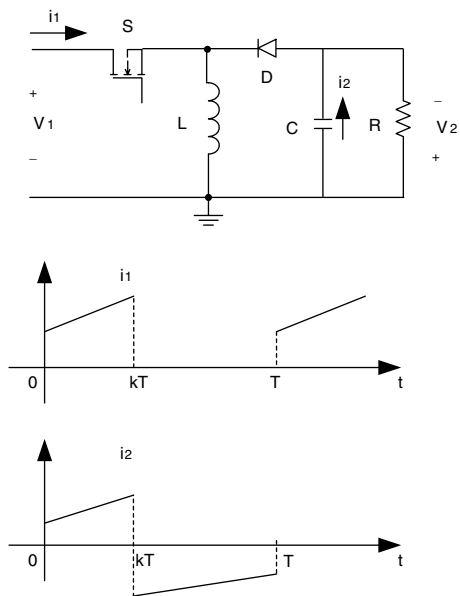


FIGURE 1.13
Negative Luo-pump.

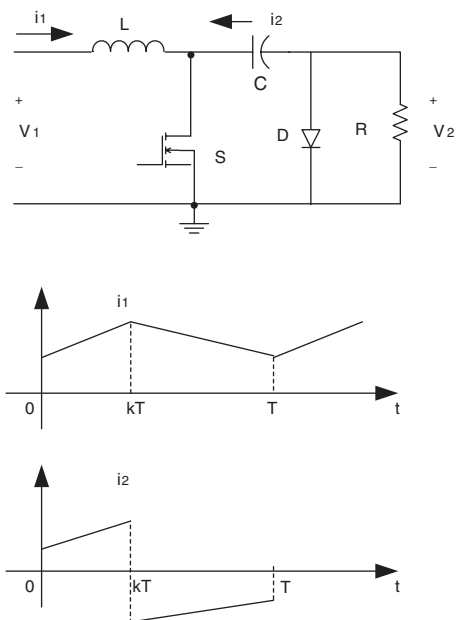


FIGURE 1.14
Cúk-pump.

1.3.3 Transformer-Type Pumps

Transformer-type pumps are developed from transformer-type DC/DC converters just like their name:

- Forward pump
- Fly-Back pump
- ZETA pump

All transformer-type pumps consist of a switch S , a transformer with the turn ratio N and other components such as diode D (one or more) and capacitor C .

1.3.3.1 Forward Pump

The circuit diagram of the forward pump and some current waveforms are shown in [Figure 1.15](#). Switch S and diode D_1 are synchronously on and off, and diode D_2 is alternately off and on. Usually, the forward pump works in discontinuous operation mode, input current is discontinuous in this case.

1.3.3.2 Fly-Back Pump

The circuit diagram of the fly-back pump and some current waveforms are in [Figure 1.16](#). Since the primary and secondary windings of the transformer

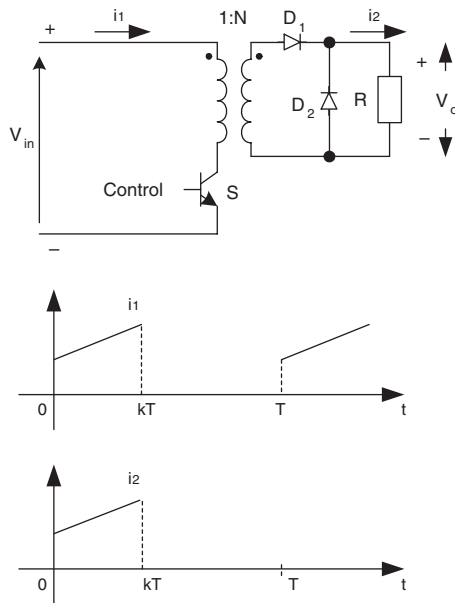


FIGURE 1.15
Forward pump.

are purposely arranged in inverse polarities, switch S and diode D are alternately on and off. Usually, the fly-back pump works in discontinuous operation mode, input current is discontinuous in this case.

1.3.3.3 ZETA Pump

The circuit diagram of the ZETA pump and some current waveforms are shown in [Figure 1.17](#). Switch S and diode D are alternately on and off. Usually, the ZETA pump works in discontinuous operation mode, input current is discontinuous in this case.

1.3.4 Super-Lift Pumps

Super-lift pumps are developed from super-lift DC/DC converters:

- Positive super Luo-pump
- Negative super Luo-pump
- Positive push-pull pump
- Negative push-pull pump
- Double/Enhanced circuit (DEC)

All super-lift pumps consist of switches, diodes, capacitors, and sometimes an inductor.

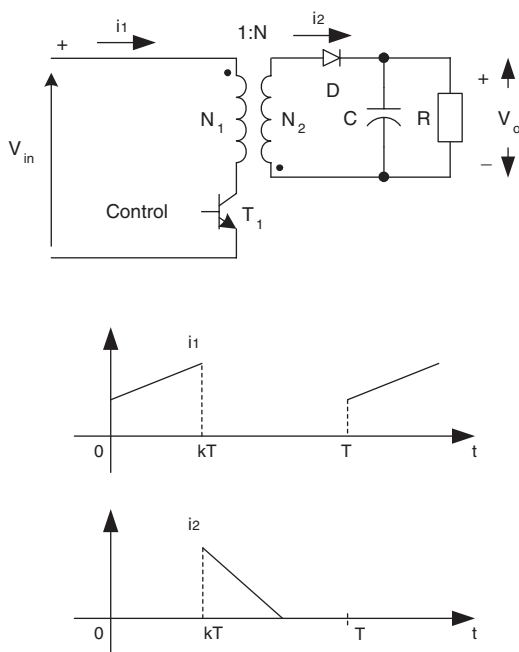


FIGURE 1.16
Fly-back pump.

1.3.4.1 Positive Super Luo-Pump

The circuit diagram of the positive super-lift pump and some current waveforms are shown in Figure 1.18. Switch S and diode D_1 are synchronously on and off, but diode D_2 is alternately off and on. Usually, the positive super-lift pump works in continuous conduction mode (CCM), inductor current is continuous in this case.

1.3.4.2 Negative Super Luo-Pump

The circuit diagram of the negative super-lift pump and some current waveforms are shown in Figure 1.19. Switch S and diode D_1 are synchronously on and off, but diode D_2 is alternately off and on. Usually, the negative super-lift pump works in CCM, but input current is discontinuous in this case.

1.3.4.3 Positive Push-Pull Pump

All push-pull pumps consist of two switches without any inductor. They can be employed in multiple-lift switched capacitor converters. The circuit diagram of positive push-pull pump and some current waveforms are shown in Figure 1.20. Since there is no inductor in the pump, it is applied in

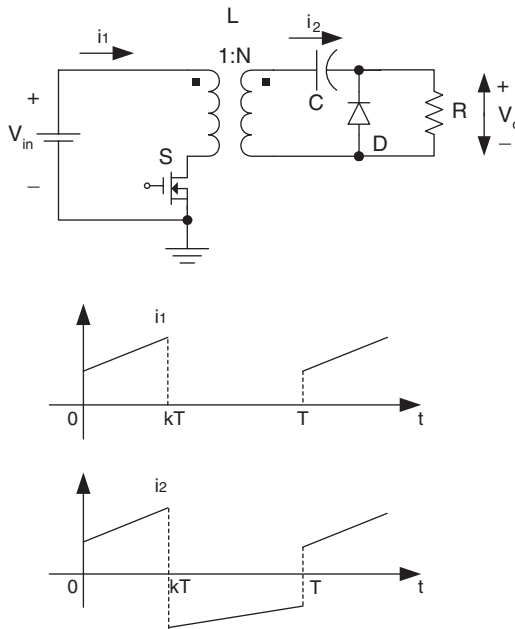


FIGURE 1.17
ZETA pump.

switched-capacitor converters. The main switch S and diode D_1 are synchronously on and off, but the slave switch S_1 and diode D_2 are alternately off and on. Usually, the positive push-pull pump works in push-pull state continuous operation mode.

1.3.4.4 Negative Push-Pull Pump

The circuit diagram of this push-pull pump and some current waveforms are shown in [Figure 1.21](#). Since there is no inductor in the pump, it is often used in switched-capacitor converters. The main switch S and diode D are synchronously on and off, but the slave switch S_1 is alternately off and on. Usually, the super-lift pump works in push-pull state continuous operation mode, inductor current is continuous in this case.

1.3.4.5 Double/Enhanced Circuit (DEC)

The circuit diagram of the double/enhanced circuit and some current waveforms are in [Figure 1.22](#). The switch is the only other existing circuit part. This circuit is usually applied in lift, super-lift, and push-pull converters. These two diodes are alternately on and off, so that two capacitors are alternately charging and discharging. Usually, this circuit can enhance the voltage doubly or at certain times.

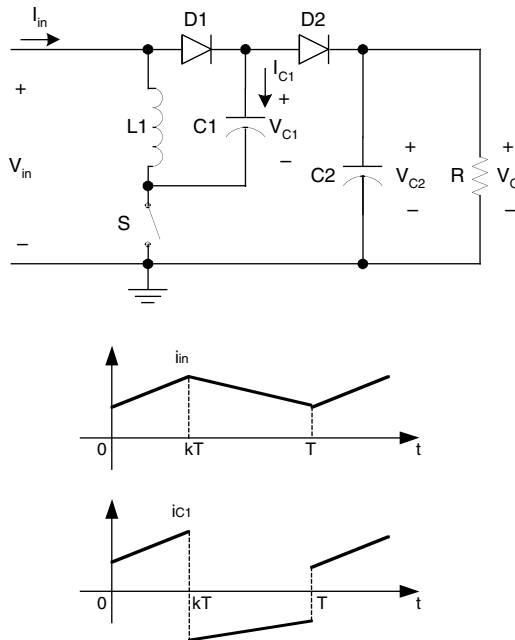


FIGURE 1.18
Positive super Luo-pump.

1.4 Development of DC/DC Conversion Technique

According to incomplete statistics, there are more than 500 existing prototypes of DC/DC converters. The main purpose of this book is to categorize all existing prototypes of DC/DC converters. This job is of vital importance for future development of DC/DC conversion techniques. The authors have devoted 20 years to this subject area, their work has been recognized and assessed by experts worldwide. The authors classify all existing prototypes of DC/DC converters into six generations. They are

- First generation (classical/traditional) converters
- Second generation (multi-quadrant) converters
- Third generation (switched-component **SI/SC**) converters
- Fourth generation (soft-switching: **ZCS/ZVS/ZT**) converters
- Fifth generation (synchronous rectifier **SR**) converters
- Sixth generation (multiple energy-storage elements resonant **MER**) converters

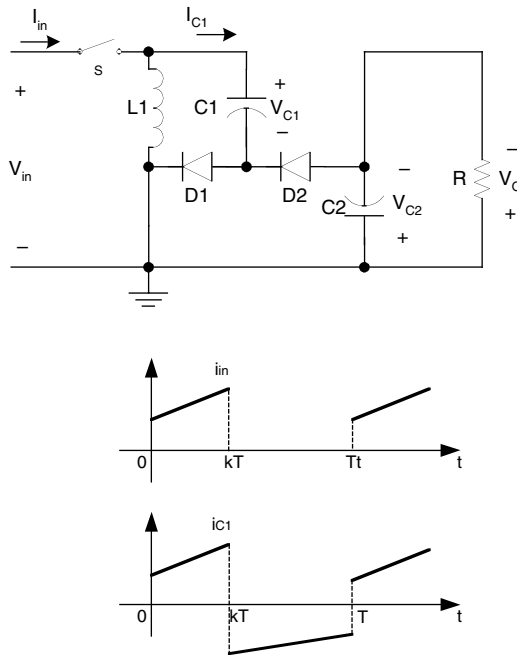


FIGURE 1.19
Negative super Luo-pump.

1.4.1 The First Generation Converters

The first-generation converters perform in a single quadrant mode and in low power range (up to around 100 W). Since its development lasts a long time, it has, briefly, five categories:

- Fundamental converters
- Transformer-type converters
- Developed converters
- Voltage-lift converters
- Super-lift converters

1.4.1.1 Fundamental Converters

Three types of fundamental DC/DC classifications were constructed, these are **buck** converter, **boost** converter, and **buck-boost** converter. They can be derived from single quadrant operation choppers. For example, the buck converter was derived from an A-type chopper. These converters have two main problems: linkage between input and output and very large output voltage ripple.

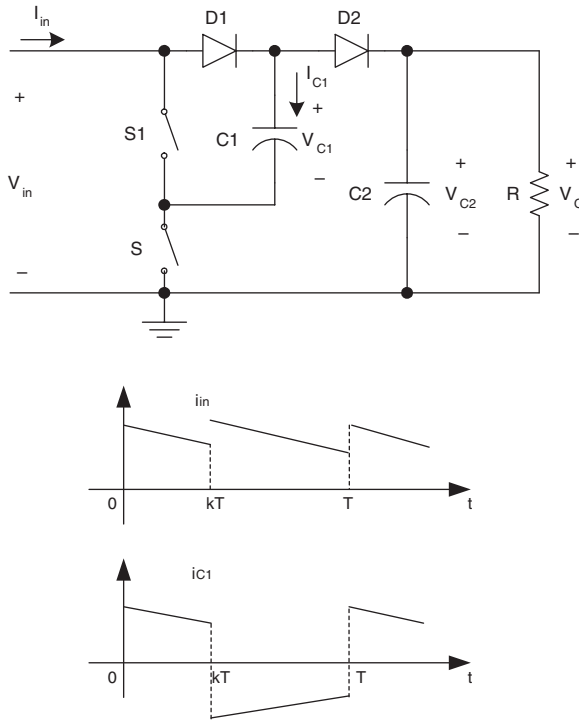


FIGURE 1.20
Positive push-pull pump.

1.4.1.1.1 Buck Converter

The buck converter is a step-down DC/DC converter. It works in first-quadrant operation. It can be derived from a quadrant I chopper. Its circuit diagram, and switch-on and -off equivalent circuit are shown in [Figure 1.23](#). The output voltage is calculated by the formula,

$$V_O = \frac{t_{on}}{T} V_{in} = k V_{in} \quad (1.8)$$

where T is the repeating period $T = 1/f$, f is the chopping frequency, t_{on} is the switch-on time, and k is the conduction duty cycle $k = t_{on}/T$.

1.4.1.1.2 Boost Converter

The boost converter is a step-up DC/DC converter. It works in second-quadrant operation. It can be derived from quadrant II chopper. Its circuit diagram, and switch-on and -off equivalent circuit are shown in [Figure 1.24](#). The output voltage is calculated by the formula,

$$V_O = \frac{T}{T - t_{on}} V_{in} = \frac{1}{1 - k} V_{in} \quad (1.9)$$

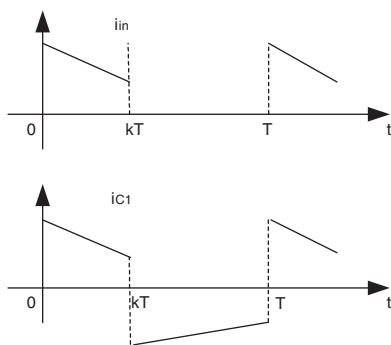
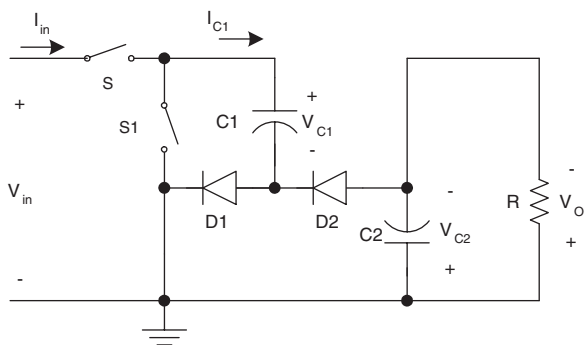


FIGURE 1.21
Negative push-pull pump.

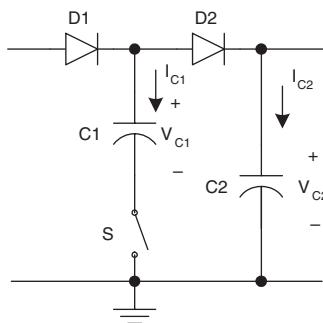
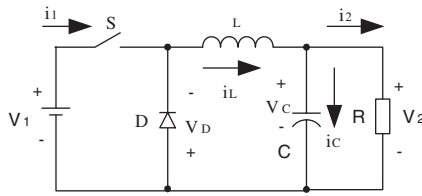
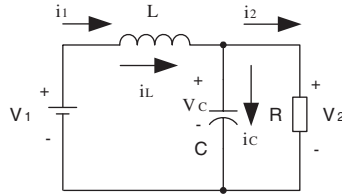


FIGURE 1.22
Double/enhanced circuit (DEC).

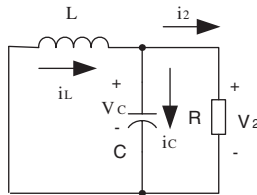
where T is the repeating period $T = 1/f$, f is the chopping frequency, t_{on} is the switch-on time, k is the conduction duty cycle $k = t_{on}/T$.



(a) Circuit diagram



(b) Switch-on



(c) Switch-off

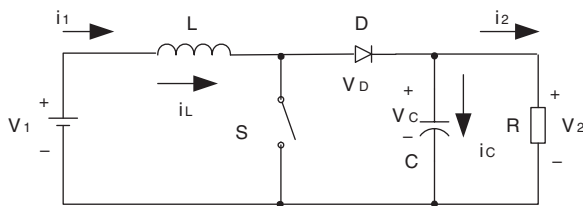
FIGURE 1.23
Buck converter.

1.4.1.1.3 Buck-Boost Converter

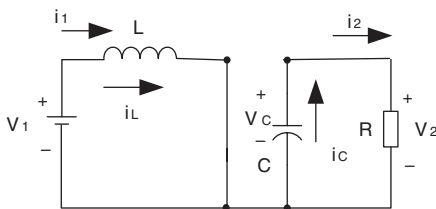
The buck-boost converter is a step down/up DC/DC converter. It works in third-quadrant operation. Its circuit diagram, switch-on and -off equivalent circuit, and waveforms are shown in [Figure 1.25](#). The output voltage is calculated by the formula,

$$V_O = \frac{t_{on}}{T - t_{on}} V_{in} = \frac{k}{1 - k} V_{in} \quad (1.10)$$

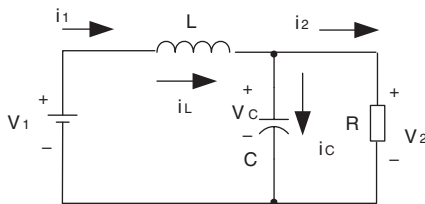
where T is the repeating period $T = 1/f$, f is the chopping frequency, t_{on} is the switch-on time, and k is the conduction duty cycle $k = t_{on}/T$. By using this converter it is easy to obtain the random output voltage, which can be higher or lower than the input voltage. It provides great convenience for industrial applications.



(a) Circuit diagram



(b) Switch on



(c) Switch off

FIGURE 1.24
Boost converter.

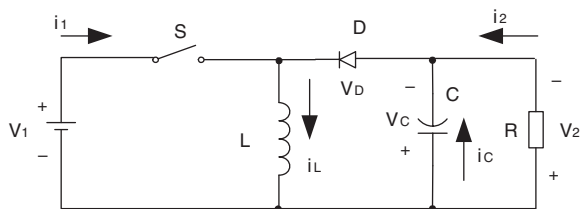
1.4.1.2 Transformer-Type Converters

Since all fundamental DC/DC converters keep the linkage from input side to output side and the voltage transfer gain is comparably low, transformer-type converters were developed in the 1960s to 1980s. There are a large group of converters such as the **forward** converter, **push-pull** converter, **fly-back** converter, **half-bridge** converter, **bridge** converter, and **Zeta** (or **ZETA**) converter. Usually, these converters have high transfer voltage gain and high insulation between both sides. Their gain usually depends on the transformer's turn ratio N , which can be thousands times.

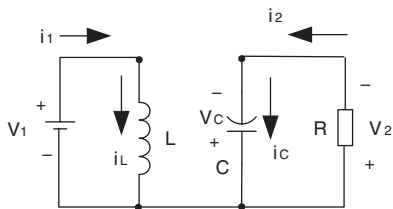
1.4.1.2.1 Forward Converter

A forward converter is a transformer-type buck converter with a turn ratio N . It works in first quadrant operation. Its circuit diagram is shown in [Figure 1.26](#). The output voltage is calculated by the formula,

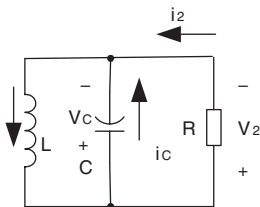
$$V_O = kNV_{in} \quad (1.12)$$



(a) Circuit diagram



(b) Switch on



(c) Switch off

FIGURE 1.25

Buck-boost converter.

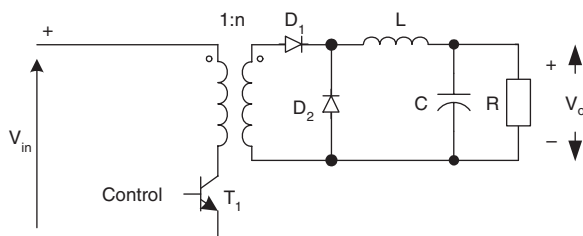


FIGURE 1.26

Forward converter.

where N is the transformer turn ratio, and k is the conduction duty cycle $k = t_{on}/T$.

In order to exploit the magnetic ability of the transformer iron core, a tertiary winding can be employed in the transformer. Its corresponding circuit diagram is shown in [Figure 1.27](#).

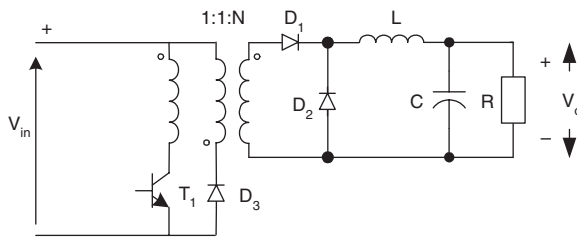


FIGURE 1.27
Forward converter with tertiary winding.

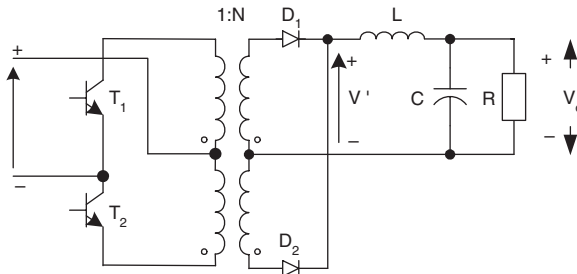


FIGURE 1.28
Push-pull converter.

1.4.1.2.2 Push-Pull Converter

The boost converter works in push-pull state, which effectively avoids the iron core saturation. Its circuit diagram is shown in Figure 1.28. Since there are two switches, which work alternately, the output voltage is doubled. The output voltage is calculated by the formula,

$$V_O = 2kNV_{in} \quad (1.13)$$

where N is the transformer turn ratio, and k is the conduction duty cycle $k = t_{on}/T$.

1.4.1.2.3 Fly-Back Converter

The fly-back converter is a transformer type converter using the demagnetizing effect. Its circuit diagram is shown in Figure 1.29. The output voltage is calculated by the formula,

$$V_O = \frac{k}{1-k} NV_{in} \quad (1.14)$$

where N is the transformer turn ratio, and k is the conduction duty cycle $k = t_{on}/T$.

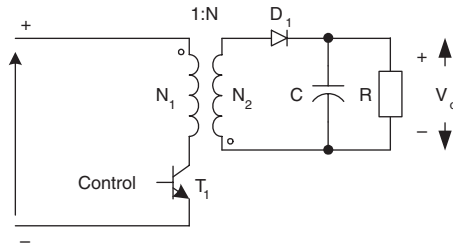


FIGURE 1.29
Fly-back converter.

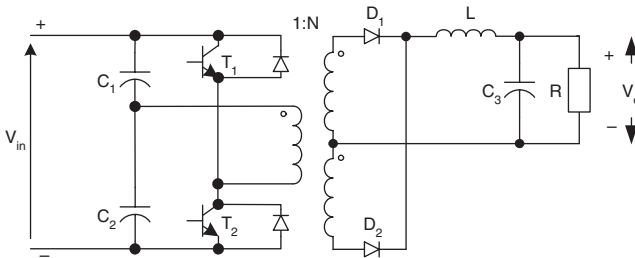


FIGURE 1.30
Half-bridge converter.

1.4.1.2.4 Half-Bridge Converter

In order to reduce the primary side in one winding, the half-bridge converter was constructed. Its circuit diagram is shown in Figure 1.30. The output voltage is calculated by the formula,

$$V_O = kNV_{in} \quad (1.15)$$

where N is the transformer turn ratio, and k is the conduction duty cycle $k = t_{on}/T$.

1.4.1.2.5 Bridge Converter

The bridge converter employs more switches and therefore gains double output voltage. Its circuit diagram is shown in Figure 1.31. The output voltage is calculated by the formula,

$$V_O = 2kNV_{in} \quad (1.16)$$

where N is the transformer turn ratio, and k is the conduction duty cycle $k = t_{on}/T$.

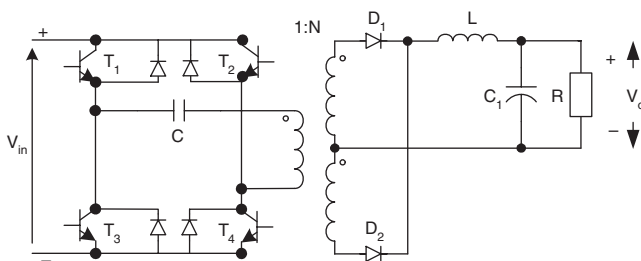


FIGURE 1.31
Bridge converter.

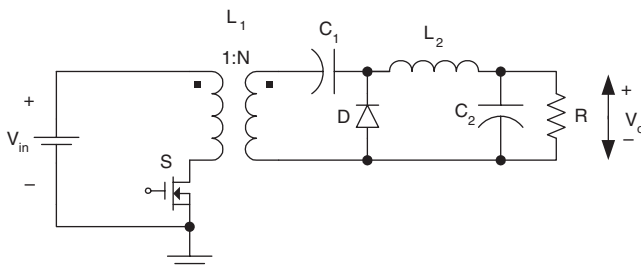


FIGURE 1.32
Zeta converter.

1.4.1.2.6 ZETA Converter

The ZETA converter is a transformer type converter with a low-pass filter. Its output voltage ripple is small. Its circuit diagram is shown in Figure 1.32. The output voltage is calculated by the formula,

$$V_O = \frac{k}{1-k} NV_{in} \quad (1.17)$$

where N is the transformer turn ratio, and k is the conduction duty cycle $k = t_{on}/T$.

1.4.1.2.7 Forward Converter with Tertiary Winding and Multiple Outputs

Some industrial applications require multiple outputs. This requirement is easily realized by constructing multiple secondary windings and the corresponding conversion circuit. For example, a forward converter with tertiary winding and three outputs is shown in Figure 1.33. The output voltage is calculated by the formula,

$$V_O = kN_i V_{in} \quad (1.18)$$

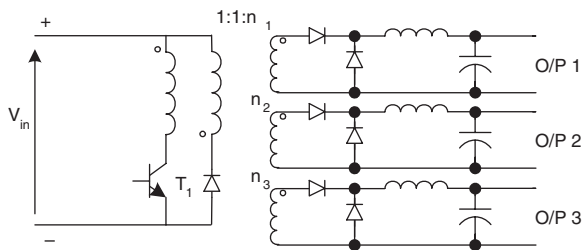


FIGURE 1.33

Forward converter with tertiary winding and three outputs.

where N_i is the transformer turn ratio to the secondary winding, $i = 1, 2$, and 3 respectively, and k is the conduction duty cycle $k = t_{on}/T$. In principle, this structure is available for all transformer-type DC/DC converters for multiple outputs applications.

1.4.1.3 Developed Converters

Developed-type converters overcome the second fault of the fundamental DC/DC converters. They are derived from fundamental converters by the addition of a low-pass filter. The preliminary design was published in a conference in 1977 (Massey and Snyder, 1977). The author designed three types of converters that derived from fundamental DC/DC converters plus a low-pass filter. This conversion technique was very popular between 1970 and 1990. Typical prototype converters are positive output (P/O) **Luo**-converter, negative output (N/O) **Luo**-converter, double output (D/O) **Luo**-converter, **Cúk**-converter, **SEPIC** (single-ended primary inductance converter) and Watkins-Johnson converters. The output voltage ripple of all developed-type converters is usually small and can be lower than 2%.

In order to obtain the random output voltage, which can be higher or lower input voltage. All developed converters provide ease of application for industry. Therefore, the output voltage gain of all developed converters is

$$V_o = \frac{k}{1-k} V_{in} \quad (1.19)$$

1.4.1.3.1 Positive Output (P/O) Luo-Converter

The positive output **Luo**-converter is the elementary circuit of the series *positive output Luo-converters*. It can be derived from the buck-boost converter. Its circuit diagram is shown in [Figure 1.34](#). The output voltage is calculated by the Equation (1.19).

1.4.1.3.2 Negative Output (N/O) Luo-Converter

The negative output **Luo**-converter is the elementary circuit of the series *negative output Luo-converters*. It can also be derived from buck-boost converters. Its

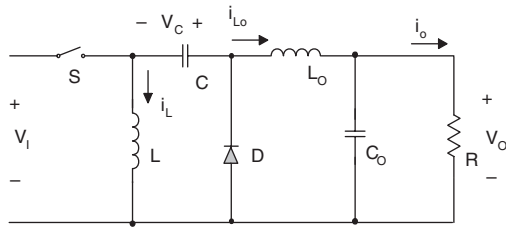


FIGURE 1.34
Positive output Luo-converter.

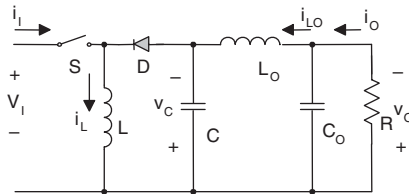


FIGURE 1.35
Negative output Luo-converter.

circuit diagram is shown in Figure 1.35. The output voltage is calculated by the Equation (1.19).

1.4.1.3.3 Double Output (D/O) Luo-Converter

In order to obtain mirror symmetrical positive plus negative output voltage double output (D/O) Luo-converters were constructed. The double output Luo-converter is the elementary circuit of the series *double output Luo-converters*. It can also be derived from the buck-boost converter. Its circuit diagram is shown in Figure 1.36. The output voltage is calculated by Equation (1.19).

1.4.1.3.4 Cúk-Converter

The Cúk-converter is derived from boost converter. Its circuit diagram is shown in Figure 1.37. The output voltage is calculated by Equation (1.19).

1.4.1.3.5 Single-Ended Primary Inductance Converter

The single-ended primary inductance converter (**SEPIC**) is derived from the boost converter. Its circuit diagram is shown in Figure 1.38. The output voltage is calculated by Equation (1.19).

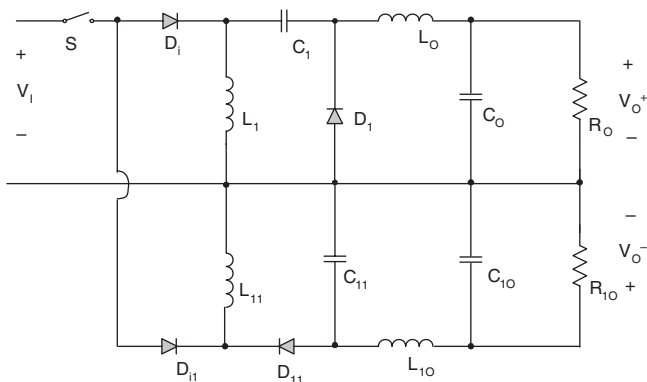


FIGURE 1.36
Double output Luo-converter.

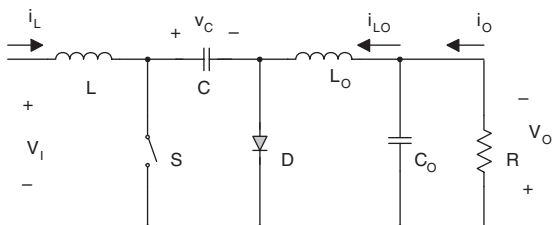


FIGURE 1.37
Cúk-converter.

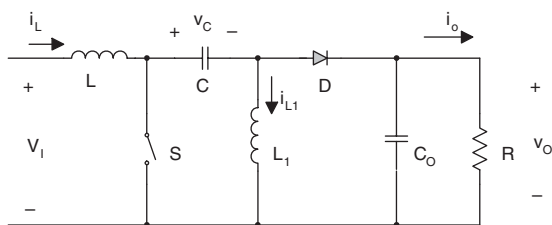


FIGURE 1.38
SEPIC.

1.4.1.3.6 Tapped Inductor Converter

These converters are derived from fundamental converters. The circuit diagrams are shown in [Table 1.2](#). The voltage transfer gains are shown in [Table 1.3](#). Here the tapped inductor ratio is $n = n1/(n1 + n2)$.

TABLE 1.2
The Circuit Diagrams of the Tapped Inductor Fundamental Converters

	Standard Converter	Switch Tap	Diode to Tap	Rail to Tap
Buck				
Boost				
Buck-Boost				

TABLE 1.3
The Voltage Transfer Gains of the Tapped Inductor Fundamental Converters

Converter	No tap	Switched to tap	Diode to tap	Rail to tap
Buck	k	$\frac{k}{n+k(1-n)}$	$\frac{nk}{1+k(n-1)}$	$\frac{k-n}{k(1-n)}$
Boost	$\frac{1}{1-k}$	$\frac{n+k(1-n)}{n(1-k)}$	$\frac{1+k(n-1)}{1-k}$	$\frac{n-k}{n(1-k)}$
Buck-Boost	$\frac{k}{1-k}$	$\frac{k}{n(1-k)}$	$\frac{nk}{1-k}$	$\frac{k}{1-k}$

1.4.1.4 Voltage Lift Converters

Voltage lift technique is a good method to lift the output voltage, and is widely applied in electronic circuit design. After long-term industrial application and research this method has been successfully used in DC/DC conversion technique. Using this method the output voltage can be easily lifted by tens to hundreds of times. Voltage lift converters can be classed into **self-lift**, **re-lift**, **triple-lift**, **quadruple-lift**, and **high-stage** lift converters. The main contributors in this area are Dr. Fang Lin Luo and Dr. Hong Ye. These circuits will be introduced in [Chapter 2](#) in detail.

1.4.1.5 Super Lift Converters

Voltage lift (VL) technique is a popular method that is widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent years, and has opened a way to design high voltage gain converters. Three series Luo-converters are examples of voltage lift technique implementations. However, the output voltage increases in stage by stage just along the arithmetic progression. A novel approach — super lift (SL) technique — has been developed, which implements the output voltage increasing stage by stage along in geometric progression. It effectively enhances the voltage transfer gain in power-law. The typical circuits are sorted into four series: positive output super-lift Luo-converters, negative output super-lift Luo-converters, positive output cascade boost converters, and negative output cascade boost converters. These circuits will be introduced in the [Chapter 3](#) to [Chapter 6](#) in detail.

1.4.2 The Second Generation Converters

The second generation converters are called multiple quadrant operation converters. These converters perform in two-quadrant operation and four-quadrant operation with medium output power range (hundreds of Watts or higher). The topologies can be sorted into two main categories: first are

the converters derived from the multiple-quadrant choppers and/or from the first generation converters. Second are constructed with transformers. Usually, one quadrant operation requires at least one switch. Therefore, a two-quadrant operation converter has at least two switches, and a four-quadrant operation converter has at least four switches. Multiple-quadrant choppers were employed in industrial applications for a long time. They can be used to implement the DC motor multiple-quadrant operation. As the chopper titles indicate, there are class-A converters (one-quadrant operation), class-B converters (two-quadrant operation), class-C converters, class-D converters, and class-E (four-quadrant operation) converters. These converters are derived from multi-quadrant choppers, for example, class B converters are derived from B-type choppers and class E converters are derived from E-type choppers. The class-A converter works in quadrant I, which corresponds to the forward-motoring operation of a DC motor drive. The class-B converter works in quadrant I and II operation, which corresponds to the forward-running motoring and regenerative braking operation of a DC motor drive. The class-C converter works in quadrant I and VI operation. The class-D converter works in quadrant III and VI operation, which corresponds to the reverse-running motoring and regenerative braking operation of a DC motor drive. The class-E converter works in four-quadrant operation, which corresponds to the four-quadrant operation of a DC motor drive. In recent years many papers have investigated the class-E converters for industrial applications. Multi-quadrant operation converters can be derived from the first generation converters. For example, multi-quadrant Luo-converters are derived from positive-output Luo-converters and negative-output Luo-converters. These circuits will be introduced in [Chapter 7](#) in detail. The transformer-type multi-quadrant converters easily change the current direction by transformer polarity and diode rectifier. The main types of such converters can be derived from the **forward** converter, **half-bridge** converter, and **bridge** converter.

1.4.3 The Third Generation Converters

The third generation converters are called switched component converters, and are made of either inductors or capacitors, so-called switched-inductor and switched-capacitors. They can perform in two- or four-quadrant operation with high output power range (thousands of Watts). Since they are made of only inductor or capacitors, they are small. Consequently, the power density and efficiency are high.

1.4.3.1 Switched Capacitor Converters

Switched-capacitor DC/DC converters consist of only capacitors. Because there is no inductor in the circuit, their size is small. They have outstanding advantages such as low power losses and low electromagnetic interference

(EMI). Since its electromagnetic radiation is low, switched-capacitor DC/DC converters are required in certain equipment. The switched-capacitor can be integrated into an integrated-chip (IC). Hence, its size is largely reduced. Much attention has been drawn to the switched-capacitor converter since its development. Many papers have been published discussing its characteristics and advantages. However, most of the converters in the literature perform a single-quadrant operation. Some of them work in the push-pull status. In addition, their control circuit and topologies are very complex, especially, for the large difference between input and output voltages. These circuits will be introduced in the [Chapter 8](#) in detail.

1.4.3.2 Multiple-Quadrant Switched Capacitor Luo-Converters

Switched-capacitor DC/DC converters consist of only capacitors. Since its power density is very high it is widely applied in industrial applications. Some industrial applications require multiple quadrant operation, so that, multiple-quadrant switched-capacitor Luo-converters have been developed. There are two-quadrant operation type and four-quadrant operation type, which will be discussed in detail.

1.4.3.3 Multiple-Lift Push-Pull Switched Capacitor Converters

Voltage lift (VL) technique is a popular method widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent years, and has opened a way to design high voltage gain converters. Three series Luo-converters are examples of voltage lift technique implementation. However, the output voltage increases stage-by-stage just along the arithmetic progression. A novel approach — multiple-lift push-pull (ml-pp) technique — has been developed that implements the output voltage, which increases stage by stage along the arithmetic progression. It effectively enhances the voltage transfer gain. The typical circuits are sorted into two series: *positive output multiple-lift push-pull switched capacitor Luo-converters* and *negative output multiple-lift push-pull switched capacitor Luo-converters*. These circuits will be introduced in the [Chapter 9](#) and [Chapter 10](#) in detail.

1.4.3.4 Multiple-Quadrant Switched Inductor Converters

The switched-capacitors have many advantages, but their circuits are not simple. If the difference of input and output voltages is large, many capacitors must be required. The switched-inductor has the outstanding advantage that only one inductor is required for one switched inductor converter no matter how large the difference between input and output voltages is. This characteristic is very important for large power conversion. At the present time, large power conversion equipment is close to using switched-inductor converters. For example, the MIT DC/DC converter designed by Prof. John G. Kassakian for his new system in the 2005 automobiles is a two-quadrant

switched-inductor DC/DC converter. These circuits will be introduced in [Chapter 8](#).

1.4.4 The Fourth Generation Converters

The fourth generation DC/DC converters are called soft-switching converters. There are four types of soft-switching methods:

1. Resonant-switch converters
2. Load-resonant converters
3. Resonant-dc-link converters
4. High-frequency-link integral-half-cycle converters

Until now attention has been paid only to the resonant-switch conversion method. This resonance method is available for working independently to load. There are three main categories: zero-current-switching (ZCS), zero-voltage-switching (ZVS), and zero-transition (ZT) converters. Most topologies usually perform in single quadrant operation in the literature. Actually, these converters can perform in two- and four-quadrant operation with high output power range (thousands of Watts). According to the transferred power becomes large, the power losses increase largely. Main power losses are produced during the switch-on and switch-off period. How to reduce the power losses across the switch is the clue to increasing the power transfer efficiency. Soft-switching technique successfully solved this problem. Professor Fred Lee is the pioneer of the soft-switching technique. He established a research center and manufacturing base to realize the zero-current-switching (ZCS) and zero-voltage-switching (ZVS) DC/DC converters. His first paper introduced his research in 1984. ZCS and ZVS converters have three resonant states: over resonance (completed resonance), optimum resonance (critical resonance) and quasi resonance (subresonance). Only the quasi-resonance state has two clear cross-zero points in a repeating period. Many papers after 1984 have been published that develop the ZCS quasi-resonant-converters (QRCs) and ZVS-QRCs.

1.4.4.1 Zero-Current-Switching Quasi-Resonant Converters

ZCS-QRC equips the resonant circuit on the switch side to keep the switch-on and switch-off at zero-current condition. There are two states: full-wave state and half wave state. Most engineers use the half-wave state. This technique has half-wave current resonance waveform with two zero-cross points.

1.4.4.2 Zero-Voltage-Switching Quasi-Resonant Converters

ZVS-QRC equips the resonant circuit on the switch side to keep the switch-on and switch-off at zero-current condition. There are two states: full-wave state

and half wave state. Most engineers use the half-wave state. This technique has half-wave current resonance waveform with two zero-cross points.

1.4.4.3 Zero-Transition Converters

Using ZCS-QRC and ZVS-QRC largely reduces the power losses across the switches. Consequently, the switch device power rates become lower and converter power efficiency is increased. However, ZCS-QRC and ZVS-QRC have large current and voltage stresses. Therefore the device's current and voltage peak rates usually are 3 to 5 times higher than the working current and voltage. It is not only costly, but also ineffective. Zero-Transition (ZT) technique overcomes this fault. It implements zero-voltage plus zero-current-switching (ZV-ZCS) technique without significant current and voltage stresses. These circuits will be introduced in [Chapter 11](#) in detail.

1.4.5 The Fifth Generation Converters

The fifth generation converters are called synchronous rectifier (SR) DC/DC converters. This type of converter was required by development of computing technology. Corresponding to the development of the micro-power consumption technique and high-density IC manufacture, the power supplies with low output voltage and strong current are widely used in communications, computer equipment, and other industrial applications. Intel, which developed the Zelog-type computers, governed the world market for a long time. Inter-80 computers used the 5 V power supply. In order to increase the memory size and operation speed, large-scale integrated chip (LSIC) technique has been quickly developed. As the amount of IC manufacturing increased, the gaps between the layers became narrower. At the same time, the micro-power-consumption technique was completed. Therefore new computers such as those using Pentium I, II, III, and IV, use a 3.3 V power supply. Future computers will have larger memory and will require lower power supply voltages, e.g. 2.5, 1.8, 1.5, even if 1.1 V. Such low power supply voltage cannot be obtained by the traditional diode rectifier bridge because the diode voltage drop is too large. Because of this requirement, new types of MOSFET were developed. They have very low conduction resistance (6 to 8 m Ω .) and forward voltage drop (0.05 to 0.2 V). Many papers have been published since 1990 and many prototypes have been developed. The fundamental topology is derived from the forward converter. Active-clamped circuit, flat-transformers, double current circuit, soft-switching methods, and multiple current methods can be used in SR DC/DC converters. These circuits will be introduced in [Chapter 12](#) in detail.

1.4.6 The Sixth Generation Converters

The sixth generation converters are called multiple energy-storage elements resonant (MER) converters. Current source resonant inverters are the heart

of many systems and equipment, e.g., uninterruptible power supply (UPS) and high-frequency annealing (HFA) apparatus. Many topologies shown in the literature are the series resonant converters (SRC) and parallel resonant converters (PRC) that consist of two or three or four energy storage elements. However, they have limitations. These limitations of two-, three-, and/or four-element resonant topologies can be overcome by special design. These converters have been categorized into three main types:

- Two energy-storage elements resonant DC/AC and DC/AC/DC converters
- Three energy-storage elements resonant DC/AC and DC/AC/DC converters
- Four energy-storage elements (2L-2C) resonant DC/AC and DC/AC/DC converters

By mathematical calculation there are eight prototypes of two-element converters, 38 prototypes of three-element converters, and 98 prototypes of four-element (2L-2C) converters. By careful analysis of these prototypes we find that few circuits can be realized. If we keep the output in low-pass bandwidth, the series components must be inductors and shunt components must be capacitors. Through further analysis, the first component of the resonant-filter network can be an inductor in series, or a capacitor in shunt. In the first case, only alternate (square wave) voltage sources can be applied to the network. In the second case, only alternate (square wave) current sources can be applied to the network. These circuits will be introduced in [Chapter 13](#) to [Chapter 16](#) in detail.

1.5 Categorize Prototypes and DC/DC Converter Family Tree

There are more than 500 topologies of DC/DC converters. It is urgently necessary to categorize all prototypes. From all accumulated knowledge we can build a DC/DC converter family tree, which is shown in [Figure 1.39](#). In each generation we introduce some circuits to readers to promote understanding of the characteristics.

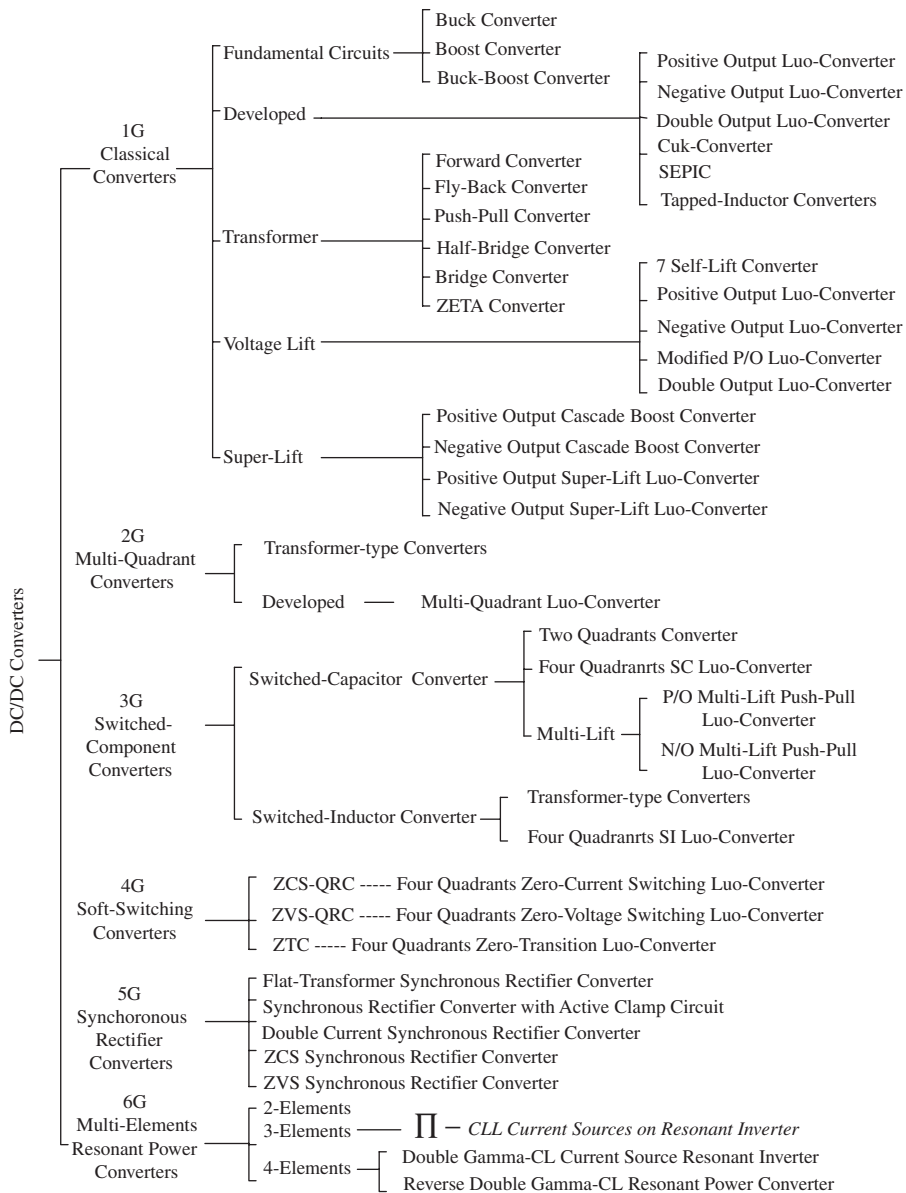


FIGURE 1.39
DC/DC converter family.

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Voltage-Lift Converters

The voltage-lift (VL) technique is a popular method that is widely applied in electronic circuit design. Applying this technique effectively overcomes the effects of parasitic elements and greatly increases the output voltage. Therefore, these DC/DC converters can convert the source voltage into a higher output voltage with high power efficiency, high power density, and a simple structure.

2.1 Introduction

VL technique is applied in the periodical switching circuit. Usually, a capacitor is charged during switch-on by certain voltages, e.g., source voltage. This charged capacitor voltage can be arranged on top-up to some parameter, e.g., output voltage during switch-off. Therefore, the output voltage can be lifted higher. Consequently, this circuit is called a self-lift circuit. A typical example is the saw-tooth-wave generator with a self-lift circuit.

Repeating this operation, another capacitor can be charged by a certain voltage, which may possibly be the input voltage or other equivalent voltage. The second capacitor charged voltage is also possibly arranged on top-up to some parameter, especially output voltage. Therefore, the output voltage can be higher than that of the self-lift circuit. As usual, this circuit is called re-lift circuit.

Analogously, this operation can be repeated many times. Consequently, the series circuits are called triple-lift circuits, quadruple-lift circuits, and so on.

Because of the effect of parasitic elements the output voltage and power transfer efficiency of DC-DC converters are limited. Voltage lift technique opens a way to improve circuit characteristics. After long-term research, this technique has been successfully applied to DC-DC converters. Three series Luo-converters are the DC-DC converters, which were developed from prototypes using VL technique. These converters perform DC-DC voltage increasing conversion with high power density, high efficiency, and cheap topology in simple structure. They are different from any other DC-DC step-up converters and possess many advantages including a high output voltage

with small ripples. Therefore, these converters are widely used in computer peripheral equipment and industrial applications, especially for high output voltage projects. This chapter's contents are arranged thusly:

1. Seven types of self-lift converters
2. Positive output Luo-converters
3. Negative output Luo-converters
4. Modified positive output Luo-converters
5. Double output Luo-converters

2.2 Seven Self-Lift Converters

All self-lift converters introduced here are derived from developed converters such as Luo-converters, Cúk-converters, and single-ended primary inductance converters (SEPICs) discussed in Section 1.3. Since all circuits are simple, usually only one more capacitor and diode required that the output voltage be higher by an input voltage. The output voltage is calculated by the formula

$$V_O = \left(\frac{k}{1-k} + 1\right)V_{in} = \frac{1}{1-k} V_{in} \quad (2.1)$$

There are seven circuits:

- Self-lift Cúk converter
- Self-lift P/O Luo-converter
- Reverse self-lift P/O Luo-converter
- Self-lift N/O Luo-converter
- Reverse self-lift Luo-converter
- Self-lift SEPIC
- Enhanced self-lift P/O Luo-converter

These converters perform DC-DC voltage increasing conversion in simple structures. In these circuits the switch S is a semiconductor device (MOSFET, BJT, IGBT and so on). It is driven by a pulse-width-modulated (PWM) switching signal with variable frequency f and conduction duty k . For all circuits, the load is usually resistive, i.e.,

$$R = V_O / I_O$$

The normalized load is

$$z_N = \frac{R}{fL_{eq}} \quad (2.2)$$

where L_{eq} is the equivalent inductance.

We concentrate on the absolute values rather than polarity in the following description and calculations. The directions of all voltages and currents are defined and shown in the corresponding figures. We also assume that the semiconductor switch and the passive components are all ideal. All capacitors are assumed to be large enough that the ripple voltage across the capacitors can be negligible in one switching cycle for the average value discussions.

For any component X (e.g., C , L and so on): its instantaneous current and voltage are expressed as i_X and v_X . Its average current and voltage values are expressed as I_X and V_X . The input voltage and current are V_O and I_O ; the output voltage and current are V_I and I_I . T and f are the switching period and frequency.

The voltage transfer gain for the continuous conduction mode (CCM) is

$$M = \frac{V_o}{V_I} = \frac{I_I}{I_o} \quad (2.3)$$

$$\text{Variation of current } i_L: \quad \zeta_1 = \frac{\Delta i_L / 2}{I_L} \quad (2.4)$$

$$\text{Variation of current } i_{Lo}: \quad \zeta_2 = \frac{\Delta i_{Lo} / 2}{I_{Lo}} \quad (2.5)$$

$$\text{Variation of current } i_D: \quad \xi = \frac{\Delta i_D / 2}{I_D} \quad (2.6)$$

$$\text{Variation of voltage } v_C: \quad \rho = \frac{\Delta v_C / 2}{V_C} \quad (2.7)$$

$$\text{Variation of voltage } v_{C1}: \quad \sigma_1 = \frac{\Delta v_{C1} / 2}{v_{C1}} \quad (2.8)$$

$$\text{Variation of voltage } v_{C2}: \quad \sigma_2 = \frac{\Delta v_{C2} / 2}{v_{C2}} \quad (2.9)$$

Variation of output voltage v_o :
$$\varepsilon = \frac{\Delta V_o / 2}{V_o} \quad (2.10)$$

Here I_D refers to the average current i_D which flows through the diode D during the switch-off period, not its average current over the whole period.

Detailed analysis of the seven self-lift DC-DC converters will be given in the following sections. Due to the length limit of this book, only the simulation and experimental results of the self-lift Cúk converter are given. However, the results and conclusions of other self-lift converters should be quite similar to those of the self-lift Cúk-converter.

2.2.1 Self-Lift Cúk Converter

Self-lift Cúk converters and their equivalent circuits during switch-on and switch-off period are shown in [Figure 2.1](#). It is derived from the Cúk converter. During switch-on period, S and D_1 are on, D is off. During switch-off period, D is on, S and D_1 are off.

2.2.1.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero. Thus

$$V_{C1} = V_{CO} = V_O \quad (2.11)$$

During switch-on period, the voltage across capacitors C and C_1 are equal. Since we assume that C and C_1 are sufficiently large, so

$$V_C = V_{C1} = V_O \quad (2.12)$$

The inductor current i_L increases during switch-on and decreases during switch-off. The corresponding voltages across L are V_I and $-(V_C - V_I)$.

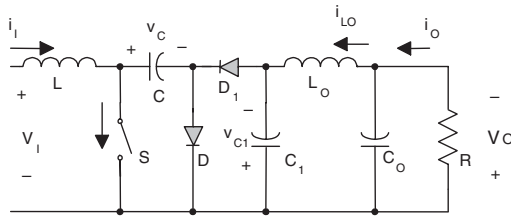
Therefore,

$$kTV_I = (1 - k)T(V_C - V_I)$$

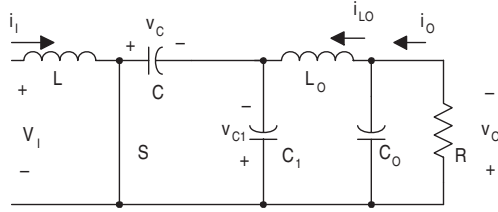
Hence,

$$V_O = V_C = V_{C1} = V_{CO} = \frac{1}{1 - k} V \quad (2.13)$$

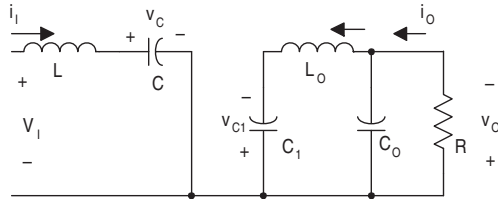
The voltage transfer gain in the CCM is



(a) Circuit diagram



(b) Switch on



(c) Switch off

FIGURE 2.1

Self-lift Cúk converter and equivalent circuits. (a) The self-lift Cúk converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k} \quad (2.14)$$

The characteristics of M vs. conduction duty cycle k are shown in [Figure 2.2](#).

Since all the components are considered ideal, the power loss associated with all the circuit elements are neglected. Therefore the output power P_O is considered to be equal to the input power P_{IN} :

$$V_O I_O = V_I I_I$$

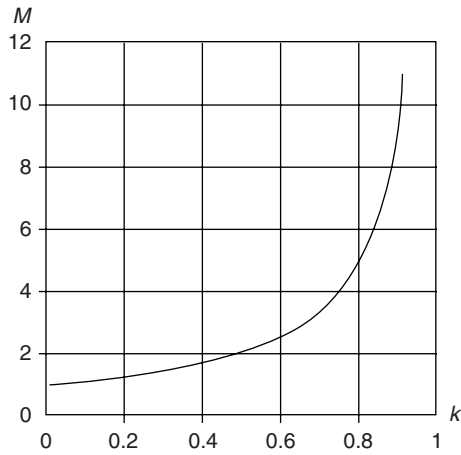


FIGURE 2.2
Voltage transfer gain M vs. k .

Thus,

$$I_L = I_I = \frac{1}{1-k} I_O$$

During switch-off,

$$i_D = i_L \quad I_D = \frac{1}{1-k} I_O \quad (2.15)$$

The capacitor C_O acts as a low pass filter so that

$$I_{LO} = I_O$$

The current i_L increases during switch-on. The voltage across it during switch-on is V_I , therefore its peak-to-peak current variation is

$$\Delta i_L = \frac{kTV_I}{L}$$

The variation ratio of the current i_L is

$$\zeta_1 = \frac{\Delta i_L / 2}{I_L} = \frac{kTV_I}{2I_L} = \frac{k(1-k)^2 R}{2fL} = \frac{kR}{2M^2 fL} \quad (2.16)$$

The variation of current i_D is

$$\xi = \zeta_1 = \frac{kR}{2M^2 fL} \quad (2.17)$$

The peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{I_L(1-k)T}{C} = \frac{I_O}{fC} \quad (2.18)$$

The variation ratio of the voltage v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{I_O}{2fCV_O} = \frac{1}{2fRC} \quad (2.19)$$

The peak-to-peak variation of the voltage v_{C1} is

$$\Delta v_{C1} = \frac{I_{LO}(1-k)T}{C_1} = \frac{I_O(1-k)}{fC_1} \quad (2.20)$$

The variation ratio of the voltage v_{C1} is

$$\sigma_1 = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{I_O(1-k)}{2fC_1V_O} = \frac{1}{2MfRC_1} \quad (2.21)$$

The peak-to-peak variation of the current i_{LO} is approximately:

$$\Delta i_{LO} = \frac{\frac{1}{2} \frac{\Delta v_{C1}}{2} \frac{T}{2}}{L_O} = \frac{I_O(1-k)}{8f^2L_OC_1} \quad (2.22)$$

The variation ratio of the current i_{LO} is approximately:

$$\zeta_2 = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{I_O(1-k)}{16f^2L_OC_1I_O} = \frac{1}{16Mf^2L_OC_1} \quad (2.24)$$

The peak-to-peak variation of voltage v_O and v_{CO} is

$$\Delta v_O = \Delta v_{CO} = \frac{\frac{1}{2} \frac{\Delta i_{LO}}{2} \frac{T}{2}}{C_O} = \frac{I_O(1-k)}{64f^3L_OC_1C_O} \quad (2.25)$$

The variation ratio of the output voltage is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{I_o(1-k)}{128f^3L_oC_1C_oV_o} = \frac{1}{128Mf^3L_oC_1C_oR} \quad (2.26)$$

The voltage transfer gain of the self-lift Cúk converter is the same as the original boost converter. However, the output current of the self-lift Cúk converter is continuous with small ripple.

The output voltage of the self-lift Cúk converter is higher than the corresponding Cúk converter by an input voltage. It retains one of the merits of the Cúk converter. They both have continuous input and output current in CCM. As for component stress, it can be seen that the self-lift converter has a smaller voltage and current stresses than the original Cúk converter.

2.2.1.2 Discontinuous Conduction Mode

Self-lift Cúk converters operate in the discontinuous conduction mode (DCM) if the current i_D reduces to zero during switch-off. As a special case, when i_D decreases to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM. The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2} \frac{R}{M^2 f L} = 1 \quad (2.27)$$

Therefore the boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL}} = \sqrt{\frac{kz_N}{2}} \quad (2.28)$$

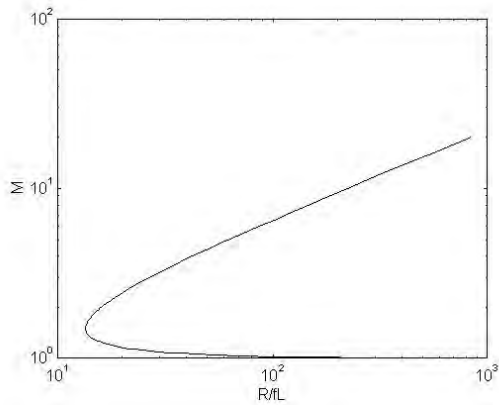
where z_N is the normalized load $R/(fL)$.

The boundary between CCM and DCM is shown in [Figure 2.3a](#). The curve that describes the relationship between M_B and z_N has the minimum value $M_B = 1.5$ and $k = 1/3$ when the normalized load z_N is 13.5.

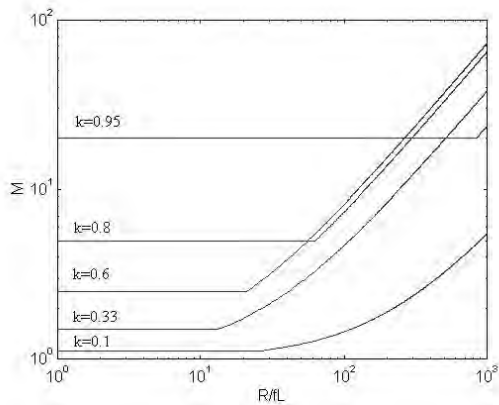
When $M > M_B$, the circuit operates in the DCM. In this case the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$ where $kT < t_1 < T$ and $0 < m < 1$.

Define m as the current filling factor (FF). After mathematical manipulation:

$$m = \frac{1}{\xi} = \frac{M^2}{k \frac{R}{2fL}} \quad (2.29)$$



a) Boundary between CCM and DCM



b) The voltage transfer gain M vs. the normalized load at various k

FIGURE 2.3

Boundary between CCM and DCM and DC voltage transfer gain M vs. the normalized load at various k . (a) Boundary between CCM and DCM. (b) The voltage transfer gain M vs. the normalized load at various k .

From the above equation we can see that the discontinuous conduction mode is caused by the following factors:

- Switch frequency f is too low
- Duty cycle k is too small
- Inductance L is too small
- Load resistor R is too big

In the discontinuous conduction mode, current i_L increases during switch-on and decreases in the period from kT to $(1-k)mT$. The corresponding voltages across L are V_I and $-(V_C - V_I)$. Therefore, $kTV_I = (1-k)mT(V_C - V_I)$. Hence,

$$V_C = [1 + \frac{k}{(1-k)m}]V_I \quad (2.30)$$

Since we assume that C , C_1 , and C_O are large enough,

$$V_O = V_C = V_{CO} = [1 + \frac{k}{(1-k)m}]V_I \quad (2.31)$$

or

$$V_O = [1 + k^2(1-k)\frac{R}{2fL}]V_I \quad (2.32)$$

The voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL} \quad (2.33)$$

The relation between DC voltage transfer gain M and the normalized load at various k in the DCM is also shown [Figure 2.3b](#). It can be seen that in DCM, the output voltage increases as the load resistance R is increasing.

2.2.2 Self-Lift P/O Luo-Converter

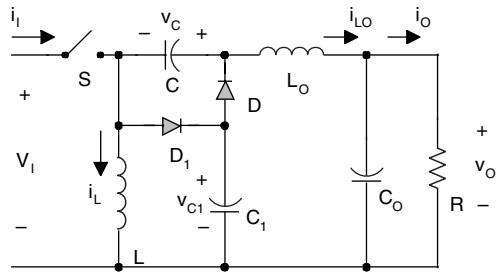
Self-lift positive output Luo-converters and the equivalent circuits during switch-on and switch-off period are shown in [Figure 2.4](#). It is the self-lift circuit of the positive output Luo-converter. It is derived from the elementary circuit of positive output Luo-converter. During switch-on period, S and D_1 are switch-on, D is switch-off. During switch-off period, D is on, S and D_1 are off.

2.2.2.1 Continuous Conduction Mode

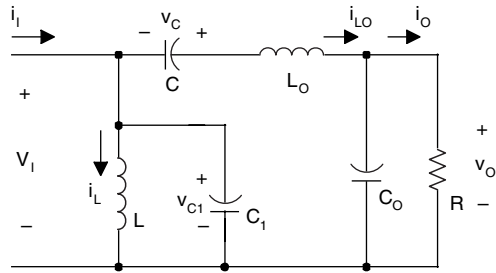
In steady state, the average inductor voltages over a period are zero. Thus

$$V_C = V_{CO} = V_O$$

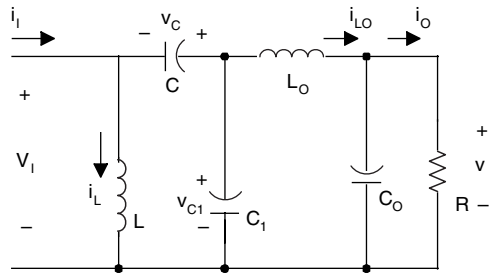
During switch-on period, the voltage across capacitor C_1 is equal to the source voltage. Since we assume that C and C_1 are sufficiently large,



a) Self-Lift Positive Output Luo-Converter



b) The equivalent circuit during switch-on



c) The equivalent circuit during switch-off

FIGURE 2.4

Self-lift positive output Luo-converter and its equivalent circuits. (a) Self-lift positive output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

$$V_{C1} = V_I$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_I and $-(V_C - V_{C1})$.

Therefore

$$kTV_I = (1-k)T(V_C - V_{C1})$$

Hence,

$$V_O = \frac{1}{1-k} V_I$$

The voltage transfer gain in the CCM is

$$M = \frac{V_O}{V_I} = \frac{1}{1-k} \quad (2.34)$$

Since all the components are considered ideal, the power loss associated with all the circuit elements are neglected. Therefore the output power P_O is considered to be equal to the input power P_{IN} , $V_O I_O = V_I I_I$
Thus,

$$I_I = \frac{1}{1-k} I_O$$

The capacitor C_O acts as a low pass filter so that

$$I_{LO} = I_O$$

The charge of capacitor C increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C-ON} kT = I_O kT \quad Q_- = I_{C-OFF} (1-k)T = I_L (1-k)T$$

In a switch period,

$$Q_+ = Q_- \quad I_L = \frac{k}{1-k} I_O$$

during switch-off period,

$$i_D = i_L + i_{LO}$$

Therefore,

$$I_D = I_L + I_{LO} = \frac{1}{1-k} I_O$$

For the current and voltage variations and boundary condition, we can get the following equations using a similar method that was used in the analysis of self-lift Cúk converter.

Current variations:

$$\zeta_1 = \frac{1}{2M^2} \frac{R}{fL} \quad \zeta_2 = \frac{k}{2M} \frac{R}{fL_O} \quad \xi = \frac{k}{2M^2} \frac{R}{fL_{eq}}$$

where L_{eq} refers to

$$L_{eq} = \frac{LL_O}{L + L_O}$$

Voltage variations:

$$\rho = \frac{k}{2} \frac{1}{fCR} \quad \sigma_1 = \frac{M}{2} \frac{1}{fC_1R} \quad \varepsilon = \frac{k}{8M} \frac{1}{f^2L_OC_O}$$

2.2.2.2 Discontinuous Conduction Mode

Self-lift positive output Luo-converters operate in the DCM if the current i_D reduces to zero during switch-off. As the critical case, when i_D decreases to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM.

The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2M^2} \frac{R}{fL_{eq}} = 1$$

Therefore the boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \quad (2.35)$$

where z_N is the normalized load $R / (fL_{eq})$ and L_{eq} refers to $L_{eq} = LL_O / (L + L_O)$.

When $M > M_B$, the circuit operates at the DCM. In this case the circuit operates in the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$, where $KT < t_1 < T$ and $0 < m < 1$, with m as the current filling factor. We define m as:

$$m = \frac{1}{\xi} = \frac{M^2}{k \frac{R}{2fL_{eq}}} \quad (2.36)$$

In the discontinuous conduction mode, current i_L increases in the switch-on period kT and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_I and $-(V_C - V_{C1})$. Therefore,

$$kTV_I = (1 - k)mT(V_C - V_{C1})$$

and

$$V_C = V_{CO} = V_O \quad V_{C1} = V_I$$

Hence,

$$V_O = [1 + \frac{k}{(1 - k)m}]V_I$$

or

$$V_O = [1 + k^2(1 - k)\frac{R}{2fL_{eq}}]V_I \quad (2.37)$$

So the real DC voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1 - k)\frac{R}{2fL_{eq}} \quad (2.38)$$

In DCM, the output voltage increases as the load resistance R is increasing.

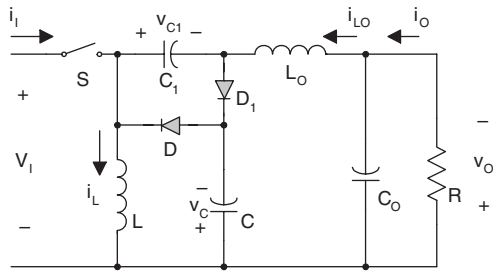
2.2.3 Reverse Self-Lift P/O Luo-Converter

Reverse self-lift positive output Luo-converters and their equivalent circuits during switch-on and switch-off period are shown in [Figure 2.5](#). It is derived from the elementary circuit of positive output Luo-converters. During switch-on period, S and D_1 are on, D is off. During switch-off period, D is on, S and D_1 are off.

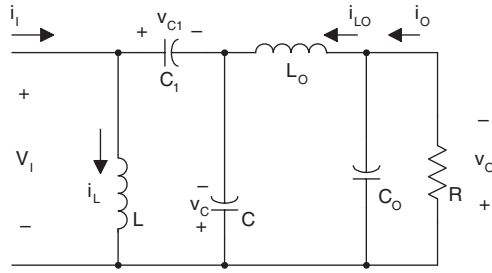
2.2.3.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero. Thus

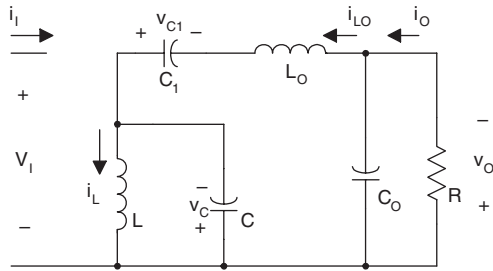
$$V_{C1} = V_{CO} = V_O$$



a) Reverse Self-Lift Positive Output Luo-Converter



b) The equivalent circuit during switch-on



c) The equivalent circuit during switch-off

FIGURE 2.5

Reverse self-lift positive output Luo-converter and its equivalent circuits. (a) Reverse self-lift positive output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

During switch-on period, the voltage across capacitor C is equal to the source voltage plus the voltage across C_1 . Since we assume that C and C_1 are sufficiently large,

$$V_{C1} = V_I + V_C$$

Therefore,

$$V_{C1} = V_I + \frac{k}{1-k} V_I = \frac{1}{1-k} V_I \quad V_O = V_{CO} = V_{C1} = \frac{1}{1-k} V_I \quad (2.39)$$

The voltage transfer gain in the CCM is

$$M = \frac{V_O}{V_I} = \frac{1}{1-k} \quad (2.40)$$

Since all the components are considered ideal, the power losses on all the circuit elements are neglected. Therefore the output power P_O is considered to be equal to the input power P_{IN} ,

$$V_O I_O = V_I I_I$$

Thus,

$$I_I = \frac{1}{1-k} I_O$$

The capacitor C_O acts as a low pass filter so that

$$I_{LO} = I_O$$

The charge of capacitor C_1 increases during switch-on and decreases during switch-off

$$Q_+ = I_{C1-ON} kT$$

$$Q_- = I_{LO} (1-k)T = I_O (1-k)T$$

In a switch period,

$$Q_+ = Q_- \quad I_{C1-ON} = \frac{1-k}{k} I_O$$

$$I_{C-ON} = I_{LO} + I_{C1-ON} = I_O + \frac{1-k}{k} I_O = \frac{1}{k} I_O \quad (2.41)$$

The charge of capacitor C increases during switch-off and decreases during switch-on.

$$Q_+ = I_{C-OFF}(1-k)T \quad Q_- = I_{C-ON}kT = \frac{1}{k}I_OkT$$

In a switch period,

$$Q_+ = Q_- \quad I_{C-OFF} = \frac{1-k}{k}I_{C-ON} = \frac{1}{1-k}I_O \quad (2.42)$$

Therefore,

$$I_L = I_{LO} + I_{C-OFF} = I_O + \frac{1}{1-k}I_O = \frac{2-k}{1-k}I_O = I_O + I_I$$

During switch-off,

$$i_D = i_L - i_{LO}$$

Therefore,

$$I_D = I_L - I_{LO} = I_O$$

The following equations are used for current and voltage variations and boundary conditions.

Current variations:

$$\zeta_1 = \frac{k}{(2-k)M^2} \frac{R}{fL}, \quad \zeta_2 = \frac{k}{2M} \frac{R}{fL_O}, \quad \xi = \frac{1}{2M^2} \frac{R}{fL_{eq}}$$

where L_{eq} refers to

$$L_{eq} = \frac{LL_O}{L + L_O}$$

Voltage variations:

$$\rho = \frac{1}{2k} \frac{1}{fCR}, \quad \sigma_1 = \frac{1}{2M} \frac{1}{fC_1R}, \quad \epsilon = \frac{k}{16M} \frac{1}{f^2C_O L_O}$$

2.2.3.2 Discontinuous Conduction Mode

Reverse self-lift positive output Luo-converter operates in the DCM if the current i_D reduces to zero during switch-off at $t = T$, then the circuit operates at the boundary of CCM and DCM. The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2M^2} \frac{R}{fL_{eq}} = 1$$

Therefore the boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \quad (2.43)$$

where z_N is the normalized load $R / (fL_{eq})$ and L_{eq} refers to $L_{eq} = LL_O / L + L_O$.

When $M > M_B$, the circuit operates in the DCM. In this case the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m] T$, where $kT < t_1 < T$ and $0 < m < 1$. m is the current filling factor.

$$m = \frac{1}{\xi} = \frac{M^2}{k \frac{R}{2fL_{eq}}} \quad (2.44)$$

In the discontinuous conduction mode, current i_L increases during switch-on and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_I and $-V_C$.

Therefore,

$$kTV_I = (1 - k)mTV_C$$

and

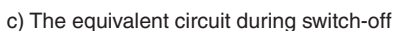
$$V_{C1} = V_{CO} = V_O \quad V_{C1} = V_I + V_C$$

Hence,

$$V_O = [1 + \frac{k}{(1 - k)m}] V_I$$

or

$$V_O = \left[1 + k^2(1 - k) \frac{R}{2fL_{eq}} \right] V_I \quad (2.45)$$



Self-lift negative output Luo-converter and its equivalent circuits. (a) Self-lift negative output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

$$M_{DCM} = 1 + k^2(1 - k) \frac{R}{2fL} \quad (2.46)$$

Self-lift negative output Luo-converters and their equivalent circuits during switch-on and switch-off period are shown in Figure 2.6. It is the self-lift circuit of the negative output Luo-converter. The function of capacitor C_1 is to lift the voltage V_C by a source voltage V_I . S and D_1 are on, and D is off during switch-on period. D is on, and S and D_1 are off during switch-off period.

2.2.4.1 Continuous Conduction Mode

In the steady state, the average inductor voltages over a period are zero. Thus

$$V_C = V_{CO} = V_O$$

During switch-on period, the voltage across capacitor C_1 is equal to the source voltage. Since we assume that C and C_1 are sufficiently large, $V_{C1} = V_I$.

Inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_I and $-(V_C - V_{C1})$.

Therefore,

$$kTV_I = (1-k)T(V_C - V_{C1})$$

Hence,

$$V_O = V_C = V_{CO} = \frac{1}{1-k} V_I \quad (2.47)$$

The voltage transfer gain in the CCM is

$$M = \frac{V_O}{V_I} = \frac{1}{1-k} \quad (2.48)$$

Since all the components are considered ideal, the power loss associated with all the circuit elements are neglected. Therefore the output power P_O is considered to be equal to the input power P_{IN} , $V_O I_O = V_I I_I$.

Thus,

$$I_I = \frac{1}{1-k} I_O$$

The capacitor C_O acts as a low pass filter so that $I_{LO} = I_O$.

For the current and voltage variations and boundary condition, the following equations can be obtained by using a similar method that was used in the analysis of self-lift Cúk converter.

Current variations:

$$\zeta_1 = \frac{k}{2M^2} \frac{R}{fL}, \quad \zeta_2 = \frac{k}{16} \frac{1}{f^2 L_O C} \quad \xi = \frac{k}{2M^2} \frac{R}{fL}$$

Voltage variations:

$$\rho = \frac{k}{2} \frac{1}{fCR} \quad \sigma_1 = \frac{M}{2} \frac{1}{fC_1R} \quad \varepsilon = \frac{k}{128} \frac{1}{f^3 L_O C C_O R}$$

2.2.4.2 Discontinuous Conduction Mode

Self-lift negative output Luo-converters operate in the DCM if the current i_D reduces to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM. The variation ratio of the current i_D is 1 when the circuit works at the boundary state.

$$\xi = \frac{k}{2M^2} \frac{R}{fL} = 1$$

Therefore the boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \quad (2.49)$$

where L_{eq} refers to $L_{eq} = L$ and z_N is the normalized load $R / (fL_{eq})$.

When $M > M_B$, the circuit operates in the DCM. In this case the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$, where $KT < t_1 < T$ and $0 < m < 1$. m is the current filling factor and is defined as:

$$m = \frac{1}{\xi} = \frac{M^2}{k \frac{R}{2fL}} \quad (2.50)$$

In the discontinuous conduction mode, current i_L increases during switch-on and decreases during period from kT to $(1 - k)mT$. The voltages across L are V_I and $-(V_C - V_{C1})$.

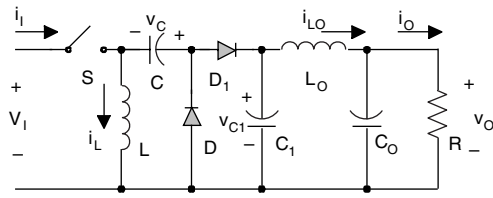
$$kTV_I = (1 - k)mT(V_C - V_{C1})$$

and

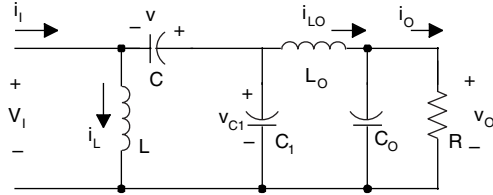
$$V_{C1} = V_I \quad V_C = V_{CO} = V_O$$

Hence,

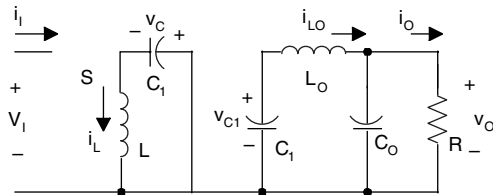
$$V_O = [1 + \frac{k}{(1 - k)m}]V_I \quad \text{or} \quad V_O = [1 + k^2(1 - k)\frac{R}{2fL}]V_I$$



a) Reverse Self-Lift Negative Output Luo-Converter



b) The equivalent circuit during switch-on



c) The equivalent circuit during switch-off

FIGURE 2.7

Reverse self-lift negative output Luo-converter and its equivalent circuits. (a) Reverse self-lift negative output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

So the real DC voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1 - k) \frac{R}{2fL} \quad (2.51)$$

We can see that in DCM, the output voltage increases as the load resistance R is increasing.

2.2.5 Reverse Self-Lift N/O Luo-Converter

Reverse self-lift negative output Luo-converters and their equivalent circuits during switch-on and switch-off period are shown in [Figure 2.7](#). It is derived from the Zeta converter. During switch-on period, S and D_1 are on, D is off. During switch-off period, D is on, S and D_1 are off.

2.2.5.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero. Thus

$$V_{C1} = V_{CO} = V_O$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_I and $-V_C$. Therefore

$$kTV_I = (1-k)TV_C$$

Hence,

$$V_C = \frac{k}{1-k} V_I \quad (2.52)$$

voltage across C . Since we assume that C and C_1 are sufficiently large,

$$V_{C1} = V_I + V_C$$

Therefore,

$$V_{C1} = V_I + \frac{k}{1-k} V_I = \frac{1}{1-k} V_I \quad V_O = V_{CO} = V_{C1} = \frac{1}{1-k} V_I$$

The voltage transfer gain in the CCM is

$$M = \frac{V_O}{V_I} = \frac{1}{1-k} \quad (2.53)$$

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore the output power P_O is considered to be equal to the input power P_{IN} , $V_O I_O = V_I I_I$.

Thus,

$$I_I = \frac{1}{1-k} I_O$$

The capacitor C_O acts as a low pass filter so that $I_{LO} = I_O$.

The charge of capacitor C_1 increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C1-ON} kT \quad Q_- = I_{C1-OFF} (1-k)T = I_O (1-k)T$$

In a switch period,

$$Q_+ = Q_- \quad I_{C1-ON} = \frac{1-k}{k} I_{C-OFF} = \frac{1-k}{k} I_O$$

The charge of capacitor C increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C-ON} kT \quad Q_- = I_{C-OFF} (1-k)T$$

In a switch period,

$$Q_+ = Q_-$$

$$I_{C-ON} = I_{C1-ON} + I_{LO} = \frac{1-k}{k} I_O + I_O = \frac{1}{k} I_O$$

$$I_{C-OFF} = \frac{k}{1-k} I_{C-ON} = \frac{k}{1-k} \frac{1}{k} I_O = \frac{1}{1-k} I_O$$

Therefore,

$$I_L = I_{C-OFF} = \frac{1}{1-k} I_O$$

During switch-off period,

$$i_D = i_L \quad I_D = I_L = \frac{1}{1-k} I_O$$

For the current and voltage variations and the boundary condition, we can get the following equations using a similar method that was used in the analysis of self-lift Cúk converter.

Current variations:

$$\zeta_1 = \frac{k}{2M^2} \frac{R}{fL} \quad \zeta_2 = \frac{1}{16M} \frac{R}{f^2 L_O C_1} \quad \xi = \frac{k}{2M^2} \frac{R}{fL}$$

Voltage variations:

$$\rho = \frac{1}{2k} \frac{1}{fC_1 R} \quad \sigma_1 = \frac{1}{2M} \frac{1}{fC_1 R} \quad \varepsilon = \frac{1}{128M} \frac{1}{f^3 L_O C_1 C_O R}$$

2.2.5.2 Discontinuous Conduction Mode

Reverse self-lift negative output Luo-converters operate in the DCM if the current i_D reduces to zero during switch-off. As a special case, when i_D decreases to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM.

The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2M^2} \frac{R}{fL_{eq}} = 1$$

The boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}}$$

where z_N is the normalized load $R / (fL_{eq})$ and L_{eq} refers to $L_{eq} = L$.

When $M > M_B$, the circuit operates at the DCM. In this case, diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$ where $KT < t_1 < T$ and $0 < m < 1$ with m as the current filling factor.

$$m = \frac{1}{\xi} = \frac{M^2}{k \frac{R}{2fL_{eq}}} \quad (2.54)$$

In the discontinuous conduction mode, current i_L increases in the switch-on period kT and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_I and $-V_C$.

Therefore,

$$kTV_I = (1 - k)mTV_C$$

and

$$V_{C1} = V_{CO} = V_O \quad V_{C1} = V_I + V_C$$

Hence,

$$V_O = [1 + \frac{k}{(1 - k)m}]V_I$$

or

$$V_O = \left[1 + k^2(1-k) \frac{R}{2fL} \right] V_I \quad (2.55)$$

The voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k) \frac{R}{2fL} \quad (2.56)$$

It can be seen that in DCM, the output voltage increases as the load resistance R is increasing.

2.2.6 Self-Lift SEPIC

Self-lift SEPIC and the equivalent circuits during switch-on and switch-off period are shown in [Figure 2.8](#). It is derived from SEPIC (with output filter). S and D_1 are on, and D is off during switch-on period. D is on, and S and D_1 are off during switch-off period.

2.2.6.1 Continuous Conduction Mode

In steady state, the average voltage across inductor L over a period is zero. Thus $V_C = V_I$.

During switch-on period, the voltage across capacitor C_1 is equal to the voltage across C . Since we assume that C and C_1 are sufficiently large,

$$V_{C1} = V_C = V_I$$

In steady state, the average voltage across inductor L_O over a period is also zero.

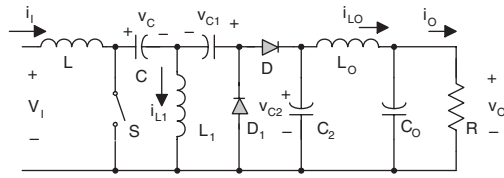
Thus
$$V_{C2} = V_{CO} = V_O$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_I and $-(V_C - V_{C1} + V_{C2} - V_I)$.

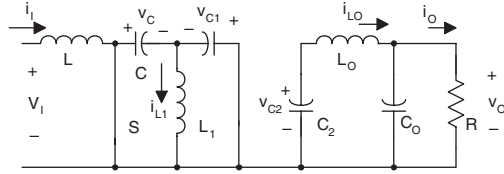
Therefore

$$kTV_I = (1-k)T(V_C - V_{C1} + V_{C2} - V_I)$$

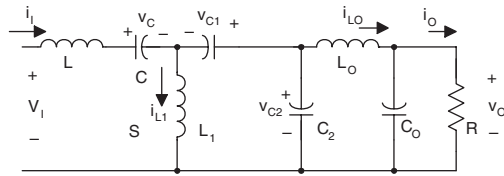
or



a) Self-Lift Sepic Converter



b) The equivalent circuit during switch-on



c) The equivalent circuit during switch-off

FIGURE 2.8

Self-lift sepic converter and its equivalent circuits. (a) Self-lift sepic converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

$$kTV_I = (1-k)T(V_O - V_I)$$

Hence,

$$V_O = \frac{1}{1-k} V_I = V_{CO} = V_{C2} \quad (2.57)$$

The voltage transfer gain in the CCM is

$$M = \frac{V_O}{V_I} = \frac{1}{1-k} \quad (2.58)$$

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore the output power P_O is considered to be equal to the input power P_{IN} , $V_O I_O = V_I I_I$.

Thus,

$$I_I = \frac{1}{1-k} I_O = I_L$$

The capacitor C_O acts as a low pass filter so that

$$I_{LO} = I_O$$

The charge of capacitor C increases during switch-off and decreases during switch-on.

$$Q_- = I_{C-ON} kT \quad Q_+ = I_{C-OFF} (1-k)T = I_I (1-k)T$$

In a switch period,

$$Q_+ = Q_- \quad I_{C-ON} = \frac{1-k}{k} I_{C-OFF} = \frac{1-k}{k} I_I$$

The charge of capacitor C_2 increases during switch-off and decreases during switch-on.

$$Q_- = I_{C2-ON} kT = I_O kT \quad Q_+ = I_{C2-OFF} (1-k)T$$

In a switch period,

$$Q_+ = Q_- \quad I_{C2-OFF} = \frac{k}{1-k} I_{C-ON} = \frac{k}{1-k} I_O$$

The charge of capacitor C_1 increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C1-ON} kT \quad Q_- = I_{C1-OFF} (1-k)T$$

In a switch period,

$$Q_+ = Q_- \quad I_{C1-OFF} = I_{C2-OFF} + I_{LO} = \frac{k}{1-k} I_O + I_O = \frac{1}{1-k} I_O$$

Therefore

$$I_{C1-ON} = \frac{1-k}{k} I_{C1-OFF} = \frac{1}{k} I_O \quad I_{L1} = I_{C1-ON} - I_{C-ON} = 0$$

During switch-off,

$$i_D = i_L - i_{L1}$$

Therefore,

$$I_D = I_I = \frac{1}{1-k} I_O$$

For the current and voltage variations and the boundary condition, we can get the following equations using a similar method that is used in the analysis of self-lift Cúk converter.

Current variations:

$$\zeta_1 = \frac{k}{2M^2} \frac{R}{fL} \quad \zeta_2 = \frac{k}{16} \frac{R}{f^2 L_O C_2} \quad \xi = \frac{k}{2M^2} \frac{R}{fL_{eq}}$$

where L_{eq} refers to

$$L_{eq} = \frac{LL_O}{L + L_O}$$

Voltage variations:

$$\rho = \frac{M}{2} \frac{1}{fCR} \quad \sigma_1 = \frac{M}{2} \frac{1}{fC_1 R} \quad \sigma_2 = \frac{k}{2} \frac{1}{fC_2 R} \quad \epsilon = \frac{k}{128} \frac{1}{f^3 L_O C_2 C_O R}$$

2.2.6.2 Discontinuous Conduction Mode

Self-lift Sepic converters operate in the DCM if the current i_D reduces to zero during switch-off. As a special case, when i_D decreases to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM.

The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2M^2} \frac{R}{fL_{eq}} = 1$$

Therefore the boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \quad (2.59)$$

where z_N is the normalized load $R / (fL_{eq})$ and L_{eq} refers to $L_{eq} = \frac{LL_O}{L + L_O}$.

When $M > M_B$, the circuit operates in the DCM. In this case the current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$ where $KT < t_1 < T$ and $0 < m < 1$. m is defined as:

$$m = \frac{1}{\xi} = \frac{M^2}{k \frac{R}{2fL_{eq}}} \quad (2.60)$$

In the discontinuous conduction mode, current i_L increases during switch-on and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_I and $-(V_C - V_{C1} + V_{C2} - V_I)$.

Thus,

$$kTV_I = (1 - k)T(V_C - V_{C1} + V_{C2} - V_I)$$

and

$$V_C = V_I \quad V_{C1} = V_C = V_I \quad V_{C2} = V_{CO} = V_O$$

Hence,

$$V_O = [1 + \frac{k}{(1 - k)m}]V_I$$

or

$$V_O = \left[1 + k^2(1 - k) \frac{R}{2fL_{eq}} \right] V_I$$

So the real DC voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1 - k) \frac{R}{2fL_{eq}} \quad (2.61)$$

In DCM, the output voltage increases as the load resistance R is increasing.

2.2.7 Enhanced Self-Lift P/O Luo-Converter

Enhanced self-lift positive output Luo-converter circuits and the equivalent circuits during switch-on and switch-off periods are shown in [Figure 2.9](#). They are derived from the self-lift positive output Luo-converter in [Figure 2.4](#) with swapping the positions of switch S and inductor L .

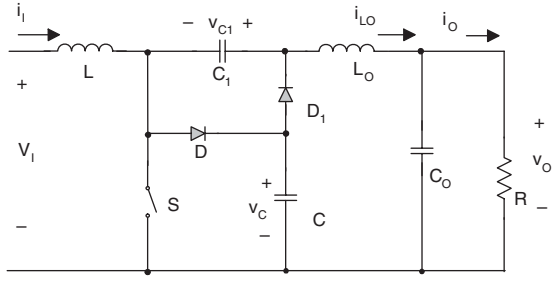


FIGURE 2.9
Enhanced self-lift P/O Luo-converter.

During switch-on period, S and D_1 are on, and D is off. Obtain:

$$V_C = V_{C1}$$

and

$$\Delta i_L = \frac{V_I}{L} kT$$

During switch-off period, D is on, and S and D_1 are off.

$$\Delta i_L = \frac{V_C - V_I}{L} (1-k)T$$

So that

$$V_C = \frac{1}{1-k} V_I$$

The output voltage and current and the voltage transfer gain are

$$V_O = V_I + V_{C1} = \left(1 + \frac{1}{1-k}\right) V_I \quad (2.62)$$

$$I_O = \frac{1-k}{2-k} I_I \quad (2.64)$$

$$M = 1 + \frac{1}{1-k} = \frac{2-k}{1-k} \quad (2.65)$$

Average voltages:

$$V_C = \frac{1}{1-k} V_I \quad (2.66)$$

$$V_{C1} = \frac{1}{1-k} V_I \quad (2.67)$$

Average currents:

$$I_{LO} = I_O \quad (2.68)$$

$$I_L = \frac{2-k}{1-k} I_O = I_I \quad (2.69)$$

Therefore,

$$\frac{V_O}{V_I} = \frac{1}{1-k} + 1 = \frac{2-k}{1-k} \quad (2.70)$$

2.3 Positive Output Luo-Converters

Positive output Luo-converters perform the voltage conversion from positive to positive voltages using VL technique. They work in the first quadrant with large voltage amplification. Five circuits have been introduced in the literature:

- Elementary circuit
- Self-lift circuit
- Re-lift circuit
- Triple-lift circuit
- Quadruple-lift circuit

The elementary circuit can perform step-down and step-up DC-DC conversion, which was introduced in previous section. Other positive output Luo-converters are derived from this elementary circuit, they are the self-lift circuit, re-lift circuit, and multiple-lift circuits (e.g., triple-lift and quadruple-lift circuits) shown in the corresponding figures. Switch S in these diagrams is a P-channel power MOSFET device (PMOS), and S_1 is an N-channel power MOSFET device (NMOS). They are driven by a PWM switch signal with

repeating frequency f and conduction duty k . The switch repeating period is $T = 1/f$, so that the switch-on period is kT and switch-off period is $(1 - k)T$. For all circuits, the load is usually resistive, $R = V_O/I_O$; the combined inductor $L = L_1L_2/(L_1 + L_2)$; the normalized load is $z_N = R/fL$. Each converter consists of a positive Luo-pump and a low-pass filter L_2 - C_O , and lift circuit (introduced in the following sections). The pump inductor L_1 transfers the energy from source to capacitor C during switch-off, and then the stored energy on capacitor C is delivered to load R during switch-on. Therefore, if the voltage V_C is higher the output voltage V_O should be higher.

When the switch S is turned off, the current i_D flows through the free-wheeling diode D . This current descends in whole switch-off period $(1 - k)T$. If current i_D does not become zero before switch S turned on again, this working state is defined as the continuous conduction mode (CCM). If current i_D becomes zero before switch S turned on again, this working state is defined as the discontinuous conduction mode (DCM).

Assuming that the output power is equal to the input power,

$$P_O = P_{IN} \quad \text{or} \quad V_O I_O = V_I I_I$$

The voltage transfer gain in continuous mode is

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O}$$

Variation ratio of current i_{L1} :

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}}$$

Variation ratio of current i_{L2} :

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}}$$

Variation ratio of current i_D :

$$\zeta = \frac{\Delta i_D / 2}{I_{L1} + I_{L2}}$$

Variation ratio of current i_{L2+j} is

$$\chi_j = \frac{\Delta i_{L2+j} / 2}{I_{L2+j}} \quad j = 1, 2, 3, \dots$$

Variation ratio of voltage v_C :

$$\rho = \frac{\Delta v_C / 2}{V_C}$$

Variation ratio of voltage v_{Cj} :

$$\sigma_j = \frac{\Delta v_{Cj} / 2}{V_{Cj}} \quad j = 1, 2, 3, 4, \dots$$

Variation ratio of output voltage v_{CO} :

$$\varepsilon = \frac{\Delta v_O / 2}{V_O}$$

2.3.1 Elementary Circuit

Elementary circuit and its switch-on and -off equivalent circuits are shown in [Figure 2.10](#). Capacitor C acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductor L_1 . Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, i.e., $v_C(t) \approx V_C$, even though it stores and transfers energy from the input to the output.

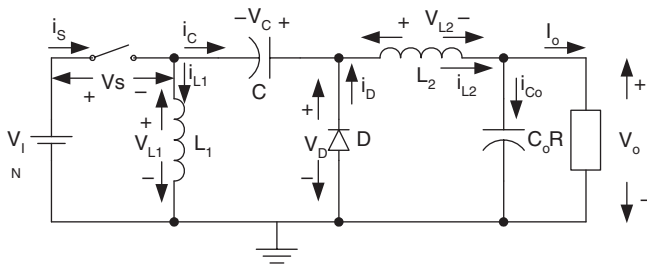
2.3.1.1 Circuit Description

When switch S is on, the source current $i_l = i_{L1} + i_{L2}$. Inductor L_1 absorbs energy from the source. In the mean time inductor L_2 absorbs energy from source and capacitor C , both currents i_{L1} and i_{L2} increase. When switch S is off, source current $i_l = 0$. Current i_{L1} flows through the free-wheeling diode D to charge capacitor C . Inductor L_1 transfers its stored energy to capacitor C . In the mean time current i_{L2} flows through the $(C_O - R)$ circuit and free-wheeling diode D to keep itself continuous. Both currents i_{L1} and i_{L2} decrease. In order to analyze the circuit working procession, the equivalent circuits in switch-on and -off states are shown in [Figures 2.10b, c, and d](#).

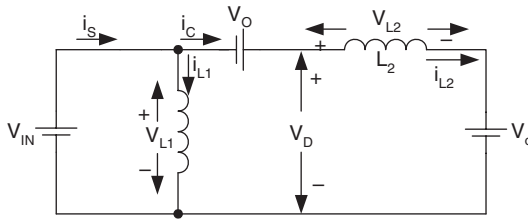
Actually, the variations of currents i_{L1} and i_{L2} are small so that $i_{L1} \approx I_{L1}$ and $i_{L2} \approx I_{L2}$.

The charge on capacitor C increases during switch off:

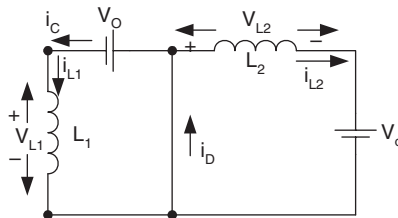
$$Q+ = (1 - k)T I_{L1}.$$



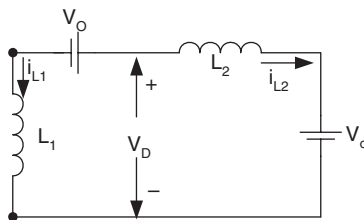
a) Circuit Diagram



b) Switch-on



c) Switch-off



d) Discontinuous mode

FIGURE 2.10

Elementary circuit of positive output Luo-converter(a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

It decreases during switch-on:

$$Q = kTI_{L2}$$

In a whole period investigation, $Q_+ = Q_-$. Thus,

$$I_{L2} = \frac{1-k}{k} I_{L1} \quad (2.71)$$

Since capacitor C_O performs as a low-pass filter, the output current

$$I_{L2} = I_O \quad (2.72)$$

These two Equations (2.71) and (2.72) are available for all positive output Luo-Converters.

The source current is $i_l = i_{L1} + i_{L2}$ during switch-on period, and $i_l = 0$ during switch-off. Thus, the average source current I_l is

$$I_l = k \times i_l = k(i_{L1} + i_{L2}) = k(1 + \frac{1-k}{k})I_{L1} = I_{L1} \quad (2.73)$$

Therefore, the output current is

$$I_O = \frac{1-k}{k} I_l \quad (2.74)$$

Hence, output voltage is

$$V_O = \frac{k}{1-k} V_I \quad (2.75)$$

The voltage transfer gain in continuous mode is

$$M_E = \frac{V_O}{V_I} = \frac{k}{1-k} \quad (2.76)$$

The curve of M_E vs. k is shown in [Figure 2.11](#).

Current i_{L1} increases and is supplied by V_I during switch-on. It decreases and is inversely biased by $-V_C$ during switch-off. Therefore,

$$kTV_I = (1-k)TV_C$$

The average voltage across capacitor C is

$$V_C = \frac{k}{1-k} V_I = V_O \quad (2.77)$$

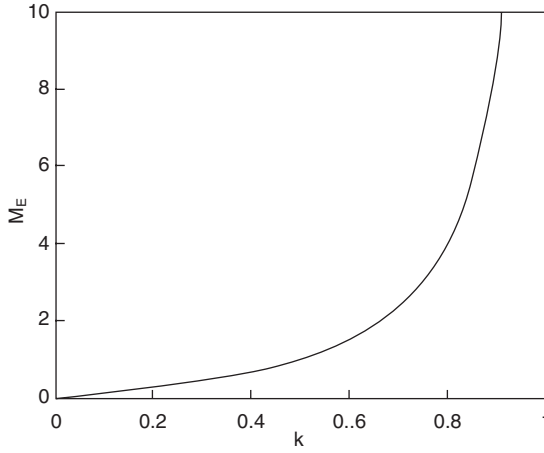


FIGURE 2.11

Voltage transfer gain M_E vs. k

2.3.1.2 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in [Figure 2.12](#).

Current i_{L1} increases and is supplied by V_I during switch-on. It decreases and is inversely biased by $-V_C$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L1} = \frac{kTV_I}{L_1}$$

Considering Equation (2.73), the variation ratio of the current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_I}{2L_1 I_I} = \frac{1-k}{2M_E} \frac{R}{fL_1} \quad (2.78)$$

Current i_{L2} increases and is supplied by the voltage $(V_I + V_C - V_O) = V_I$ during switch-on. It decreases and is inversely biased by $-V_O$ during switch-off. Therefore its peak-to-peak variation is

$$\Delta i_{L2} = \frac{kTV_I}{L_2} \quad (2.79)$$

Considering Equation (2.72), the variation ratio of current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{kTV_I}{2L_2 I_O} = \frac{k}{2M_E} \frac{R}{fL_2} \quad (2.80)$$

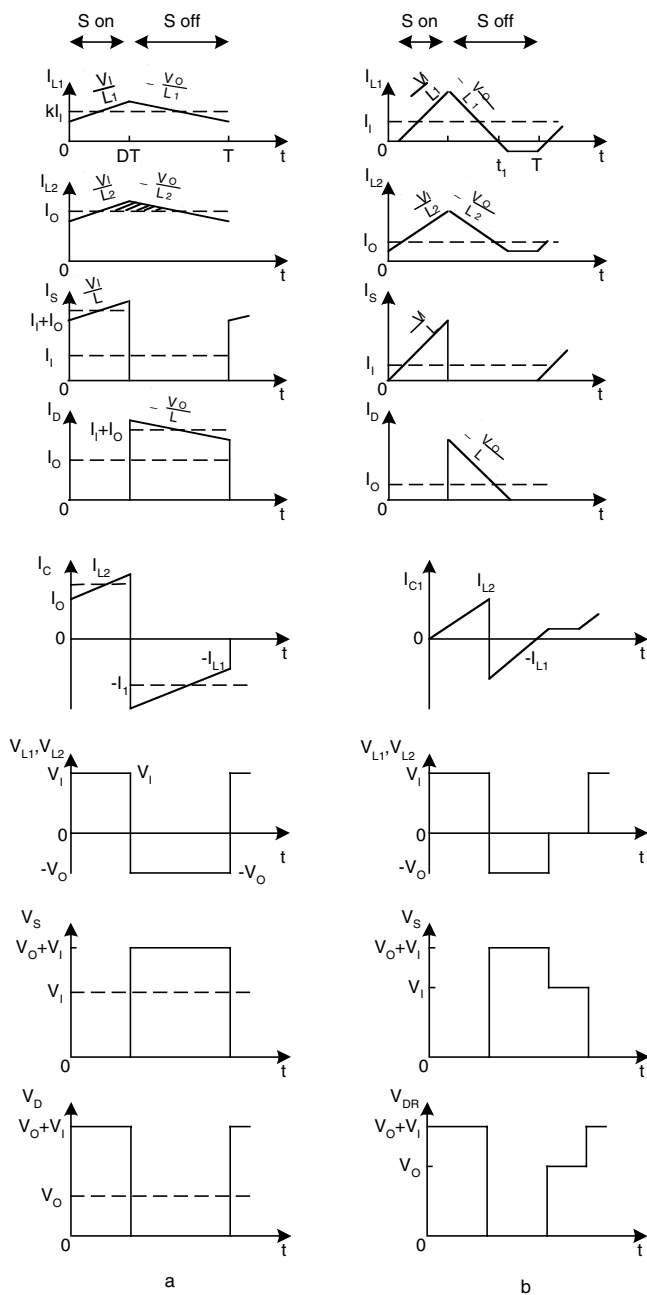


FIGURE 2.12

Some voltage and current waveforms of elementary circuit.

When switch is off, the free-wheeling diode current is $i_D = i_{L1} + i_{L2}$ and

$$\Delta i_D = \Delta i_{L1} + \Delta i_{L2} = \frac{kTV_L}{L_1} + \frac{kTV_L}{L_2} = \frac{kTV_L}{L} = \frac{(1-k)TV_O}{L} \quad (2.81)$$

Considering Equation (2.71) and Equation (2.72), the average current in switch-off period is

$$I_D = I_{L1} + I_{L2} = \frac{I_O}{1-k}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D / 2}{I_D} = \frac{(1-k)^2 TV_O}{2LI_O} = \frac{k(1-k)R}{2M_E fL} = \frac{k^2}{M_E^2} \frac{R}{2fL} \quad (2.82)$$

The peak-to-peak variation of v_C is

$$\Delta v_C = \frac{Q}{C} = \frac{1-k}{C} TI_I$$

Considering Equation (2.77), the variation ratio of v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{(1-k)TI_I}{2CV_O} = \frac{k}{2} \frac{1}{fCR} \quad (2.83)$$

If $L_1 = L_2 = 1 \text{ mH}$, $C = C_O = 20 \text{ } \mu\text{F}$, $R = 10 \text{ } \Omega$, $f = 50 \text{ kHz}$ and $k = 0.5$, we get $\xi_1 = \xi_2 = 0.05$, $\zeta = 0.025$ and $\rho = 0.025$. Therefore, the variations of i_{L1} , i_{L2} , and v_C are small.

In order to investigate the variation of output voltage v_O , we have to calculate the charge variation on the output capacitor C_O , because

$$Q = C_O V_O$$

and

$$\Delta Q = C_O \Delta v_O$$

ΔQ is caused by Δi_{L2} and corresponds to the **area** of the triangle with the **height** of half of Δi_{L2} and the **width** of half of the repeating period $T/2$, which is shown in [Figure 2.12](#). Considering Equation (2.79),

$$\Delta Q = \frac{1}{2} \frac{\Delta i_{L2}}{2} \frac{T}{2} = \frac{T}{8} \frac{kTV_L}{L_2}$$

Thus, the half peak-to-peak variation of output voltage v_o and v_{co} is

$$\frac{\Delta v_o}{2} = \frac{\Delta Q}{C_o} = \frac{kT^2 V_I}{8C_o L_2}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{kT^2}{8C_o L_2} \frac{V_I}{V_o} = \frac{k}{8M_E} \frac{1}{f^2 C_o L_2} \quad (2.84)$$

If $L_2 = 1 \text{ mH}$, $C_o = 20 \text{ }\mu\text{F}$, $f = 50 \text{ kHz}$ and $k = 0.5$, we obtain that $\varepsilon = 0.00125$. Therefore, the output voltage V_o is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and $I_o = V_o/R$.

2.3.1.3 Instantaneous Values of Currents and Voltages

Referring to [Figure 2.12](#), the instantaneous values of the currents and voltages are listed below:

$$v_s = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_o + V_I & \text{for } kT < t \leq T \end{cases} \quad (2.85)$$

$$v_D = \begin{cases} V_I + V_o & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.86)$$

$$v_{L1} = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -V_o & \text{for } kT < t \leq T \end{cases} \quad (2.87)$$

$$v_{L2} = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -V_o & \text{for } kT < t \leq T \end{cases} \quad (2.88)$$

$$i_l = i_s = \begin{cases} i_{L1}(0) + i_{L2}(0) + \frac{V_I}{L} t & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.89)$$

$$i_{L1} = \begin{cases} i_{L1}(0) + \frac{V_I}{L_1} t & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{V_o}{L_1} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.90)$$

$$i_{L2} = \begin{cases} i_{L2}(0) + \frac{V_L}{L_2} t & \text{for } 0 < t \leq kT \\ i_{L2}(kT) - \frac{V_O}{L_2} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.91)$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ i_{L1}(kT) + i_{L2}(kT) - \frac{V_O}{L} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.92)$$

$$i_C \approx \begin{cases} i_{L2}(0) + \frac{V_L}{L_2} t & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) + \frac{V_O}{L_1} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.93)$$

$$i_{CO} \approx \begin{cases} i_{L2}(0) + \frac{V_L}{L_2} t - I_O & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) + \frac{V_O}{L_1} (t - kT) - I_O & \text{for } kT < t \leq T \end{cases} \quad (2.94)$$

where

$$i_{L1}(0) = \frac{kI_O}{1-k} - \frac{(1-k)V_O}{2fL_1}$$

$$i_{L1}(kT) = \frac{kI_O}{1-k} + \frac{(1-k)V_O}{2fL_1}$$

$$i_{L2}(0) = I_O - \frac{(1-k)V_O}{2fL_2}$$

$$i_{L2}(kT) = I_O + \frac{(1-k)V_O}{2fL_2}$$

2.3.1.4 Discontinuous Mode

Referring to [Figure 2.10d](#), we can see that the diode current i_D becomes zero during switch off before next period switch on. The condition for discontinuous mode is

$$\zeta \geq 1$$

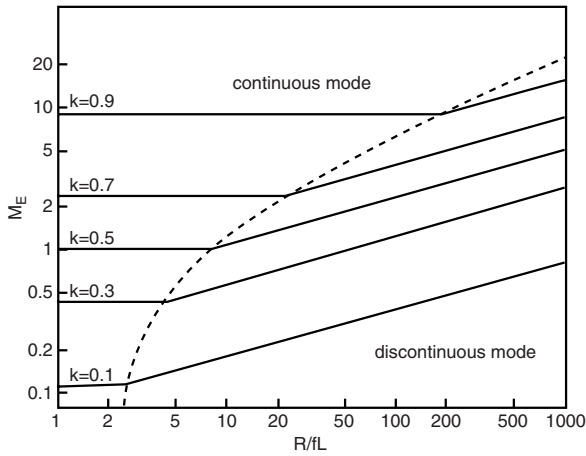


FIGURE 2.13

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$.

i.e.,

$$\frac{k^2}{M_E^2} \frac{R}{2fL} \geq 1$$

or

$$M_E \leq k \sqrt{\frac{R}{2fL}} = k \sqrt{\frac{z_N}{2}} \quad (2.95)$$

The graph of the boundary curve vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.13](#). It can be seen that the boundary curve is a monorising function of the parameter k .

In this case the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_E]T$, where m_E is the **filling efficiency** and it is defined as:

$$m_E = \frac{1}{\zeta} = \frac{M_E^2}{k^2 \frac{R}{2fL}} \quad (2.96)$$

Considering Equation (2.95), therefore $0 < m_E < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_ET$, for the current i_L , then

$$kTV_I = (1 - k)m_ETV_C$$

or

$$V_C = \frac{k}{(1 - k)m_E} V_I = k(1 - k) \frac{R}{2fL} V_I$$

with

$$\sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

and for the current i_{LO}

$$kT(V_I + V_C - V_O) = (1-k)m_ETV_O$$

Therefore, output voltage in discontinuous mode is

$$V_O = \frac{k}{(1-k)m_E} V_I = k(1-k) \frac{R}{2fL} V_I$$

with

$$\sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \quad (2.97)$$

i.e., the output voltage will linearly increase during load resistance R increasing. The output voltage vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.13](#). It can be seen that larger load resistance R may cause higher output voltage in discontinuous conduction mode.

2.3.1.5 Stability Analysis

Stability analysis is of vital importance for any converter circuit. Considering the various methods including the Bode plot, the root-locus method in s -plane is used for this analysis. According to the circuit network and control system theory, the transfer function in s -domain for switch-on and -off are obtained:

$$G_{on} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{on} = \frac{sCR}{s^3 CC_O L_2 R + s^2 CL_2 + s(C + C_O)R + 1} \quad (2.98)$$

$$G_{off} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{off} = \frac{sCR}{s^3 CC_O L_2 R + s^2 CL_2 + s(C + C_O)R + 1} \quad (2.99)$$

where s is the Laplace operator. From Equation (2.98) and Equation (2.99) in Laplace transform it can be seen that the elementary converter is a third order control circuit. The zero is determined by the equations where the numerator is equal to zero, and the poles are determined by the equation where the denominator is equal to zero. There is a zero at original point (0,

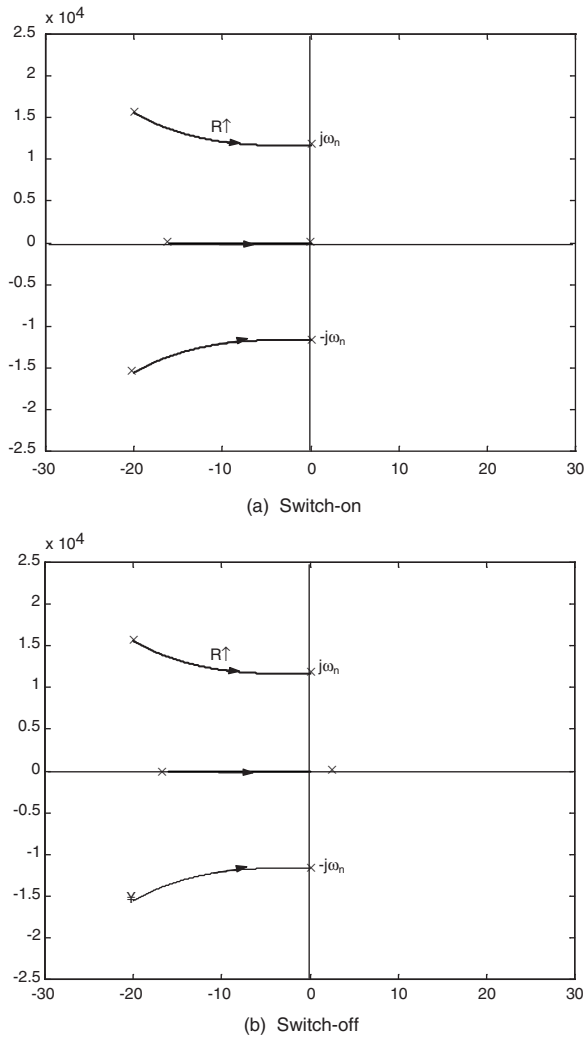


FIGURE 2.14

Stability analysis of elementary circuit. (a) Switch-on. (b) Switch-off.

0) and three poles located in the left-hand half plane in Figure 2.14, so that this converter is stable. Since the equations to determine the poles are the equations with all positive real coefficients, according to the **Gauss theorem**, the three poles are one negative real pole and a pair of conjugate complex poles with negative real part. When the load resistance R increases and tends toward infinity, the three poles move. The real pole goes to the original point and eliminates with the zero. The pair of conjugate complex poles becomes a pair of imaginary poles located on the image axis. Assuming $C = C_O$ and $L_1 = L_2$ [$L = L_1 L_2 / (L_1 + L_2)$ or $L_2 = 2L$], the pair of imaginary poles are

$$s = \pm j \sqrt{\frac{C + C_0}{CC_0 L_2}} = \pm j \sqrt{\frac{1}{CL}} = \pm j \omega_n \quad \text{for switch on} \quad (2.100)$$

$$s = \pm j \sqrt{\frac{C + C_0}{CC_0 L_2}} = \pm j \sqrt{\frac{1}{CL}} = \pm j \omega_n \quad \text{for switch off} \quad (2.101)$$

where $\omega_n = \sqrt{1/CL}$ is the converter normal angular frequency. They are locating on the stability boundary. Therefore, the circuit works in the critical state. This fact is verified by experiment and computer simulation. When $R = \infty$, the output voltage v_o intends to be very high value. The output voltage V_o cannot be infinity because of the leakage current penetrating the capacitor C_o .

2.3.2 Self-Lift Circuit

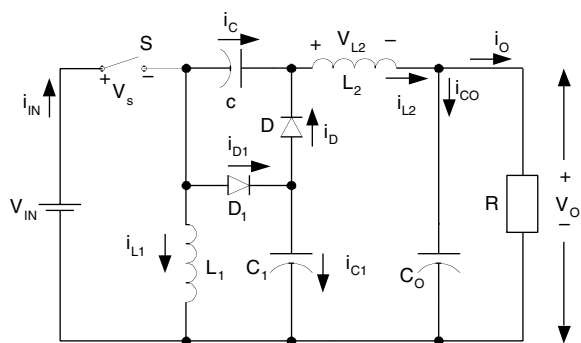
Self-lift circuit and its switch-on and -off equivalent circuits are shown in Figure 2.15, which is derived from the elementary circuit. Comparing to Figure 2.10 and Figure 2.15, it can be seen that the pump circuit and filter are retained and there is only one capacitor C_1 and one diode D_1 more, as a lift circuit is added into the circuit. Capacitor C_1 functions to lift the capacitor voltage V_c by a source voltage V_{in} . Current $i_{c1}(t) = \delta(t)$ is an exponential function. It has a large value at the power on moment, but it is small in the steady state because $V_{c1} = V_{in}$.

2.3.2.1 Circuit Description

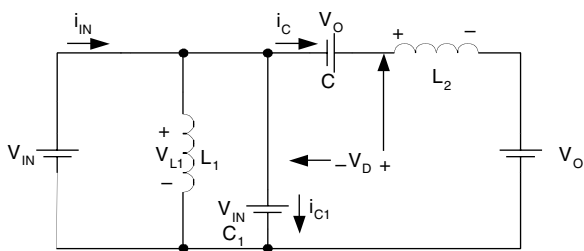
When switch S is on, the instantaneous source current is $i_l = i_{L1} + i_{L2} + i_{C1}$. Inductor L_1 absorbs energy from the source. In the mean time inductor L_2 absorbs energy from source and capacitor C . Both currents i_{L1} and i_{L2} increase, and C_1 is charged to $v_{c1} = V_l$. When switch S is off, the instantaneous source current is $i_l = 0$. Current i_{L1} flows through capacitor C_1 and diode D to charge capacitor C . Inductor L_1 transfers its stored energy to capacitor C . In the mean time, current i_{L2} flows through the $(C_o - R)$ circuit, capacitor C_1 and diode D , to keep itself continuous. Both currents i_{L1} and i_{L2} decrease. In order to analyze the circuit working procession, the equivalent circuits in switch-on and -off states are shown in Figures 2.15b, c and d. Assuming that capacitor C_1 is sufficiently large, voltage V_{c1} is equal to V_l in steady state.

Current i_{L1} increases in switch-on period kT , and decreases in switch-off period $(1 - k)T$. The corresponding voltages applied across L_1 are V_l and $-(V_c - V_l)$ respectively. Therefore,

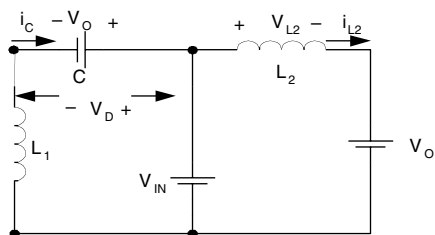
$$kTV_l = (1 - k)T(V_c - V_l)$$



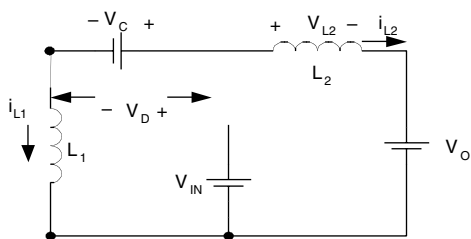
(a) circuit diagram



(b) switch on



(c) switch off



(d) discontinuous mode

FIGURE 2.15

Self-lift circuit. (a) Circuit diagram. (b) Switch on. (c) Switch off. (d) Discontinuous mode.

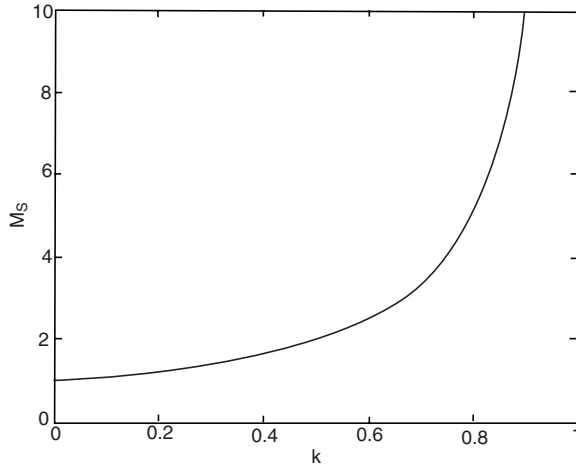


FIGURE 2.16
Voltage transfer gain M_s vs. k .

Hence,

$$V_C = \frac{1}{1-k} V_I \quad (2.102)$$

Current i_{L2} increases in switch-on period kT , and decreases in switch-off period $(1-k)T$. The corresponding voltages applied across L_2 are $(V_I + V_C - V_O)$ and $-(V_O - V_I)$. Therefore,

$$kT(V_C + V_I - V_O) = (1-k)T(V_O - V_I)$$

Hence,

$$V_O = \frac{1}{1-k} V_I \quad (2.103)$$

and the output current is

$$I_O = (1-k)I_I \quad (2.104)$$

Therefore, the voltage transfer gain in continuous mode is

$$M_s = \frac{V_O}{V_I} = \frac{1}{1-k} \quad (2.105)$$

The curve of M_s vs. k is shown in [Figure 2.16](#).

2.3.2.2 Average Current I_{C1} and Source Current I_s

During switch-off period $(1-k)T$, current i_{C1} is equal to $(i_{L1} + i_{L2})$, and the charge on capacitor C_1 decreases. During switch-on period kT , the charge increases, so its average current in switch-on period is

$$I_{C1} = \frac{1-k}{k}(i_{L1} + i_{L2}) = \frac{1-k}{k}(I_{L1} + I_{L2}) = \frac{I_O}{k} \quad (2.106)$$

During switch-off period $(1-k)T$ the source current i_I is 0, and in the switch-on period kT ,

$$i_I = i_{L1} + i_{L2} + i_{C1}$$

Hence, $I_I = k(i_{L1} + i_{L2} + i_{C1}) = k(I_{L1} + I_{L2} + I_{C1})$

$$= k(I_{L1} + I_{L2})(1 + \frac{1-k}{k}) = k \frac{I_{L2}}{1-k} \frac{1}{k} = \frac{I_O}{1-k} \quad (2.107)$$

2.3.2.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in [Figure 2.17](#). Current i_{L1} increases and is supplied by V_I during switch-on period kT . It decreases and is reversely biased by $-(V_C - V_I)$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L1} = \frac{kTV_I}{L_1}$$

Hence, the variation ratio of current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kV_I T}{2kL_1 I_I} = \frac{1-k}{2M_S} \frac{R}{fL_1} \quad (2.108)$$

Current i_{L2} increases and is supplied by the voltage $(V_I + V_C - V_O) = V_I$ in switch-on period kT . It decreases and is inversely biased by $-(V_C - V_I)$ during switch-off. Therefore its peak-to-peak variation is

$$\Delta i_{L2} = \frac{kTV_I}{L_2}$$

Thus, the variation ratio of current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{kV_I T}{2L_2 I_O} = \frac{k}{2M_S} \frac{R}{fL_2} \quad (2.109)$$

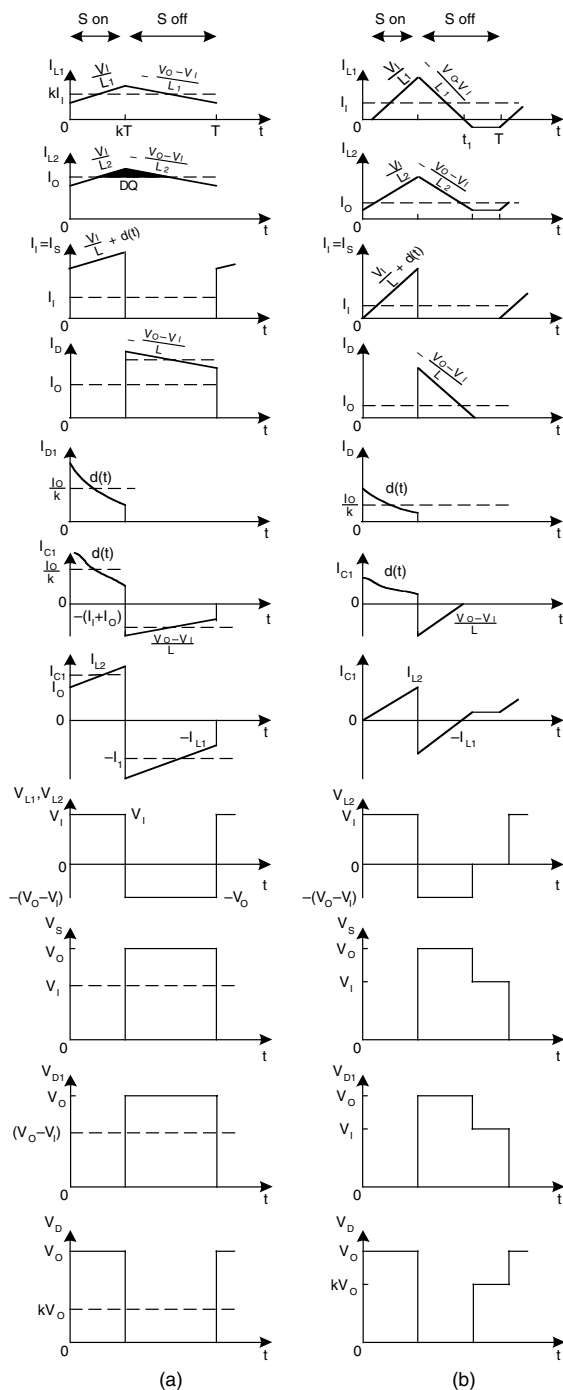


FIGURE 2.17

Some voltage and current waveforms of self-lift circuit.

When switch is off, the free-wheeling diode current is $i_D = i_{L1} + i_{L2}$ and

$$\Delta i_D = \Delta i_{L1} + \Delta i_{L2} = \frac{kTV_L}{L} = \frac{k(1-k)V_O}{L} T \quad (2.110)$$

Considering Equation (2.71) and Equation (2.72),

$$I_D = I_{L1} + I_{L2} = \frac{I_O}{1-k}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D / 2}{I_D} = \frac{k(1-k)^2 TV_O}{2LI_O} = \frac{k}{M_S^2} \frac{R}{2fL} \quad (2.111)$$

The peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q}{C} = \frac{(1-k)TI_{L1}}{C} = \frac{1-k}{C} kTI_L$$

Hence, its variation ratio is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{(1-k)^2 kI_L T}{2CV_L} = \frac{k}{2fCR} \quad (2.112)$$

The charge on capacitor C_1 increases during switch-on, and decreases during switch-off period $(1-k)T$ by the current $(I_{L1} + I_{L2})$. Therefore, its peak-to-peak variation is

$$\Delta v_{C1} = \frac{(1-k)T(I_{L1} + I_{L2})}{C_1} = \frac{I_O}{fC_1}$$

Considering $V_{C1} = V_L$, the variation ratio of voltage v_{C1} is

$$\sigma = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{I_O}{2fC_1 V_L} = \frac{M_S}{2fC_1 R} \quad (2.113)$$

If $L_1 = L_2 = 1\text{mH}$, $C = C_1 = C_O = 20\text{ }\mu\text{F}$, $R = 40\text{ }\Omega$, $f = 50\text{ kHz}$ and $k = 0.5$, we obtained that $\xi_1 = 0.1$, $\xi_2 = 0.1$, $\zeta = 0.1$, $\rho = 0.006$ and $\sigma = 0.025$. Therefore, the variations of i_{L1} , i_{L2} , v_{C1} and v_C are small.

Considering Equation (2.84) and Equation (2.105), the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{kT^2}{8C_o L_2} \frac{V_I}{V_o} = \frac{k}{8M_s} \frac{1}{f^2 C_o L_2} \quad (2.114)$$

If $L_2 = 1 \text{ mH}$, $C_o = 20 \text{ }\mu\text{F}$, $f = 50 \text{ kHz}$ and $k = 0.5$, $\varepsilon = 0.0006$. Therefore, the output voltage V_o is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and $I_o = V_o/R$.

2.3.2.4 Instantaneous Value of the Currents and Voltages

Referring to [Figure 2.17](#), the instantaneous values of the currents and voltages are listed below:

$$v_s = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_o & \text{for } kT < t \leq T \end{cases} \quad (2.115)$$

$$v_D = \begin{cases} V_o & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.116)$$

$$v_{D1} = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_o & \text{for } kT < t \leq T \end{cases} \quad (2.117)$$

$$v_{L1} = v_{L2} = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -(V_o - V_I) & \text{for } kT < t \leq T \end{cases} \quad (2.118)$$

$$i_l = i_s = \begin{cases} i_{L1}(0) + i_{L2}(0) + \delta(t) + \frac{V_I}{L} t & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.119)$$

$$i_{L1} = \begin{cases} i_{L1}(0) + \frac{V_I}{L_1} t & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{V_o - V_I}{L_1} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.120)$$

$$i_{L2} = \begin{cases} i_{L2}(0) + \frac{V_I}{L_2} t & \text{for } 0 < t \leq kT \\ i_{L2}(kT) - \frac{V_o - V_I}{L_2} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.121)$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ i_{L1}(kT) + i_{L2}(kT) - \frac{V_O - V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.122)$$

$$i_{D1} = \begin{cases} \delta(t) & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.123)$$

$$i_C = \begin{cases} i_{L2}(0) + \frac{V_I}{L_2}t & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{V_O - V_I}{L_1}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.124)$$

$$i_{C1} = \begin{cases} \delta(t) & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) - i_{L2}(kT) + \frac{V_O - V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.125)$$

$$i_{CO} = \begin{cases} i_{L2}(0) + \frac{V_I}{L_2}t - I_O & \text{for } 0 < t \leq kT \\ i_{L2}(kT) - \frac{V_O - V_I}{L_2}(t - kT) - I_O & \text{for } kT < t \leq T \end{cases} \quad (2.126)$$

where

$$i_{L1}(0) = k I_I - k V_I / 2 f L_1$$

$$i_{L1}(kT) = k I_I + k V_I / 2 f L_1$$

and

$$i_{L2}(0) = I_O - k V_O / 2 f M L_2$$

$$i_{L2}(kT) = I_O + k V_O / 2 f M L_2$$

2.3.2.5 Discontinuous Mode

Referring to [Figure 2.15d](#), we can see that the diode current i_D becomes zero during switch off before next period switch on. The condition for discontinuous mode is $\zeta \geq 1$,

$$\text{i.e.,} \quad \frac{k}{M_s^2} \frac{R}{2fL} \geq 1$$

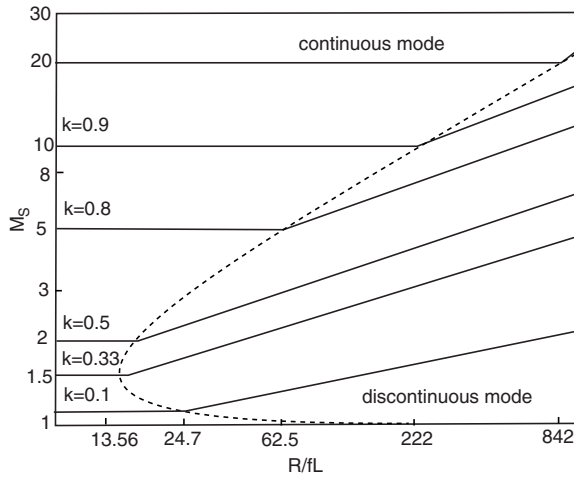


FIGURE 2.18

The boundary between CCM and DCM and the output voltage vs. the normalized load $z_N = R/fL$.

or

$$M_s \leq \sqrt{k} \sqrt{\frac{R}{2fL}} = \sqrt{k} \sqrt{\frac{z_N}{2}} \quad (2.127)$$

The graph of the boundary curve vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.18](#). It can be seen that the boundary curve has a minimum value of 1.5 at $k = 1/3$.

In this case the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_s]T$, where m_s is the **filling efficiency** and it is defined as:

$$m_s = \frac{1}{\zeta} = \frac{M_s^2}{k \frac{R}{2fL}} \quad (2.128)$$

Considering Equation (2.127), therefore $0 < m_s < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_sT$, for the current i_L

$$kTV_I = (1 - k)m_sT(V_C - V_I)$$

or

$$V_C = \left[1 + \frac{k}{(1 - k)m_s}\right]V_I = \left[1 + k^2(1 - k)\frac{R}{2fL}\right]V_I$$

with

$$\sqrt{k} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

and for the current i_{LO}

$$kT(V_I + V_C - V_O) = (1-k)m_s T(V_O - V_I)$$

Therefore, output voltage in discontinuous mode is

$$V_O = [1 + \frac{k}{(1-k)m_s}]V_I = [1 + k^2(1-k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \quad (2.129)$$

i.e., the output voltage will linearly increase while load resistance R increases. The output voltage V_O vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.18](#). Larger load resistance R causes higher output voltage in discontinuous conduction mode.

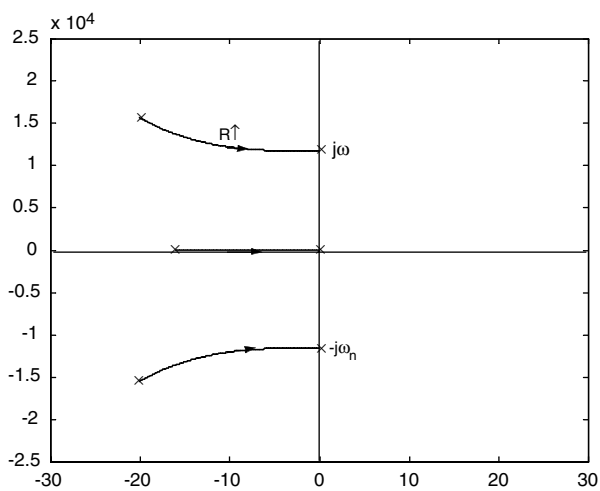
2.3.2.6 Stability Analysis

Taking the root-locus method in s-plane for stability analysis the transfer functions in s-domain for switch-on and -off are obtained:

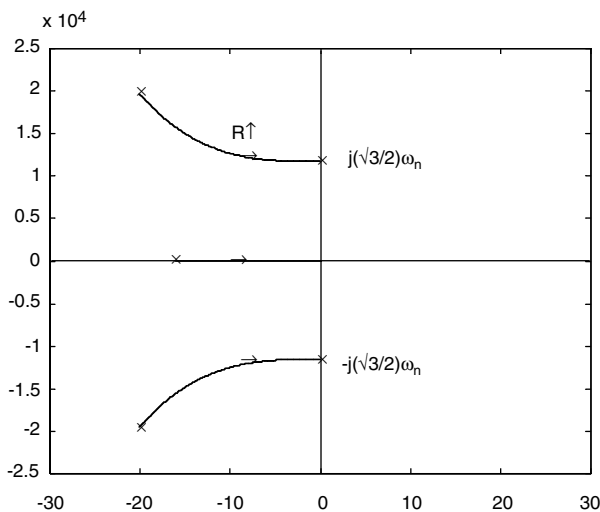
$$G_{on} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{on} = \frac{sCR}{s^3 CC_O L_2 R + s^2 CL_2 + s(C + C_O)R + 1} \quad (2.130)$$

$$G_{off} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{off} = \frac{sCR}{s^3 (C + C_1)C_O L_2 R + s^2 (C + C_1)L_2 + s(C + C_1 + C_O)R + 1} \quad (2.131)$$

where s is the Laplace operator. From Equations (2.130) and (2.131) in Laplace transform it can be seen that the self-lift converter is a third order control circuit. The zero is determined by the equation when the numerator is equal to zero, and the poles are determined by the equation when the denominator is equal to zero. There is a zero at origin point (0, 0) and three poles located in the left-hand half plane in [Figure 2.19](#), so that the self-lift converter is stable. Since the equations to determine the poles are the equations with all positive real coefficients, according to the **Gauss theorem**, the three poles are one negative real pole and a pair of conjugate complex poles with negative real part. When the load resistance R increases and tends towards infinity, the three poles move. The real pole goes to the origin point and eliminates with the zero. The pair of conjugate complex poles becomes a pair of imaginary poles locating on the image axis. Assuming $C = C_1 = C_O$ and $L_1 = L_2$ ($L = L_1 L_2 / (L_1 + L_2)$ or $L_2 = 2L$), the pair of imaginary poles are



(a) Switch on



(b) Switch off

FIGURE 2.19

Stability analysis of self-lift circuit. (a) Switch-on. (b) Switch-off.

$$s = \pm j \sqrt{\frac{C + C_0}{CC_0L_2}} = \pm j \sqrt{\frac{1}{CL}} = \pm j \omega_n \quad \text{for switch on} \quad (2.132)$$

$$s = \pm j \sqrt{\frac{C + C_1 + C_0}{(C + C_1)C_0L_2}} = \pm j \sqrt{\frac{3}{4CL}} = \pm j \frac{\sqrt{3}}{2} \omega_n \quad \text{for switch off} \quad (2.133)$$

where $\omega_n = \sqrt{1/CL}$ is the self-lift converter normal angular frequency. They are locating on the stability boundary. Therefore, the circuit works in the critical state. This fact is verified by experiment and computer simulation. When $R = 8$, the output voltage v_o intends to be a very high value. The output voltage V_o cannot be infinity because of the leakage current penetrating the capacitor C_o .

2.3.3 Re-Lift Circuit

Re-lift circuit, and its switch-on and -off equivalent circuits are shown in Figure 2.20, which is derived from the self-lift circuit. It consists of two static switches S and S_1 ; three diodes D , D_1 , and D_2 ; three inductors L_1 , L_2 and L_3 ; four capacitors C , C_1 , C_2 , and C_o . From Figure 2.10, Figure 2.15, and Figure 2.20, it can be seen that the pump circuit and filter are retained and there are one capacitor C_2 , one inductor L_3 and one diode D_2 added into the re-lift circuit. The lift circuit consists of D_1 - C_1 - L_3 - D_2 - S_1 - C_2 . Capacitors C_1 and C_2 perform characteristics to lift the capacitor voltage V_C by twice the source voltage V_I . L_3 performs the function as a ladder joint to link the two capacitors C_1 and C_2 and lift the capacitor voltage V_C up. Current $i_{C1}(t) = \delta_1(t)$ and $i_{C2}(t) = \delta_2(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C1} = v_{C2} = V_I$ in steady state.

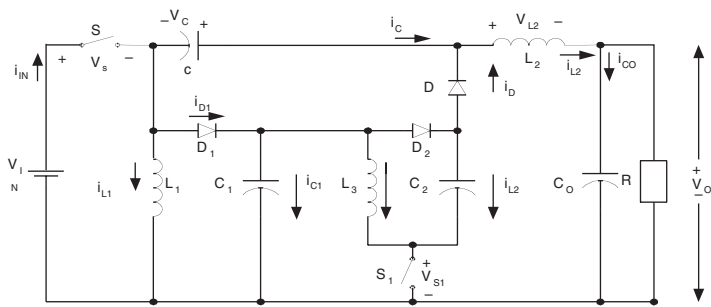
2.3.3.1 Circuit Description

When switches S and S_1 turn on, the source instantaneous current $i_i = i_{L1} + i_{L2} + i_{C1} + i_{L3} + i_{C2}$. Inductors L_1 and L_3 absorb energy from the source. In the mean time inductor L_2 absorbs energy from source and capacitor C . Three currents i_{L1} , i_{L3} and i_{L2} increase. When switches S and S_1 turn off, source current $i_i = 0$. Current i_{L1} flows through capacitor C_1 , inductor L_3 , capacitor C_2 and diode D to charge capacitor C . Inductor L_1 transfers its stored energy to capacitor C . In the mean time, current i_{L2} flows through the $(C_o - R)$ circuit, capacitor C_1 , inductor L_3 , capacitor C_2 and diode D to keep itself continuous. Both currents i_{L1} and i_{L2} decrease. In order to analyze the circuit working procession, the equivalent circuits in switch-on and -off states are shown in Figure 2.20b, c, and d. Assuming capacitor C_1 and C_2 are sufficiently large, and the voltages V_{C1} and V_{C2} across them are equal to V_I in steady state.

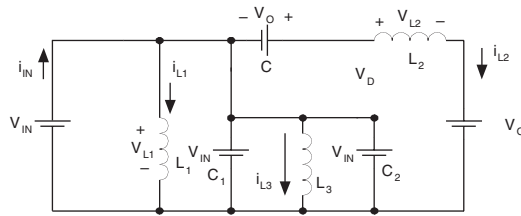
Voltage v_{L3} is equal to V_I during switch-on. The peak-to-peak variation of current i_{L3} is

$$\Delta i_{L3} = \frac{V_I k T}{L_3} \quad (2.134)$$

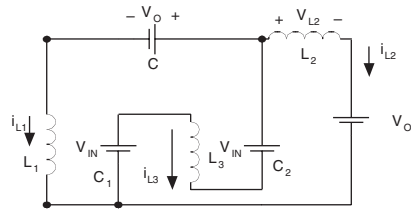
This variation is equal to the current reduction when it is switch-off. Suppose its voltage is $-V_{L3-off}$, so



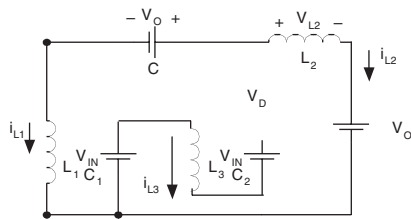
(a) circuit diagram



(b) switch on



(c) switch off



(d) discontinuous mode

FIGURE 2.20

Re-lift circuit: (a) circuit diagram; (b) switch on; (c) switch off; (d) discontinuous mode.

$$\Delta i_{L3} = \frac{V_{L3-off}(1-k)T}{L_3}$$

Thus, during switch-off the voltage drop across inductor L_3 is

$$V_{L3-off} = \frac{k}{1-k} V_I \quad (2.135)$$

Current i_{L1} increases in switch-on period kT , and decreases in switch-off period $(1-k)T$. The corresponding voltages applied across L_1 are V_I and $-(V_C - 2V_I - V_{L3-off})$. Therefore,

$$kTV_I = (1-k)T(V_C - 2V_I - V_{L3-off})$$

Hence,
$$V_C = \frac{2}{1-k} V_I \quad (2.136)$$

Current i_{L2} increases in switch-on period kT , and it decreases in switch-off period $(1-k)T$. The corresponding voltages applied across L_2 are $(V_I + V_C - V_O)$ and $-(V_O - 2V_I - V_{L3-off})$. Therefore,

$$kT(V_C + V_I - V_O) = (1-k)T(V_O - 2V_I - V_{L3-off})$$

Hence,
$$V_O = \frac{2}{1-k} V_I \quad (2.137)$$

and the output current is

$$I_O = \frac{1-k}{2} I_I \quad (2.138)$$

The voltage transfer gain in continuous mode is

$$M_R = \frac{V_O}{V_I} = \frac{2}{1-k} \quad (2.139)$$

The curve of M_R vs. k is shown in [Figure 2.21](#).

2.3.3.2 Other Average Currents

Considering Equation (2.71),

$$I_{L1} = \frac{k}{1-k} I_O = \frac{k}{2} I_I \quad (2.140)$$

and
$$I_{L3} = I_{L1} + I_{L2} = \frac{1}{1-k} I_O \quad (2.141)$$

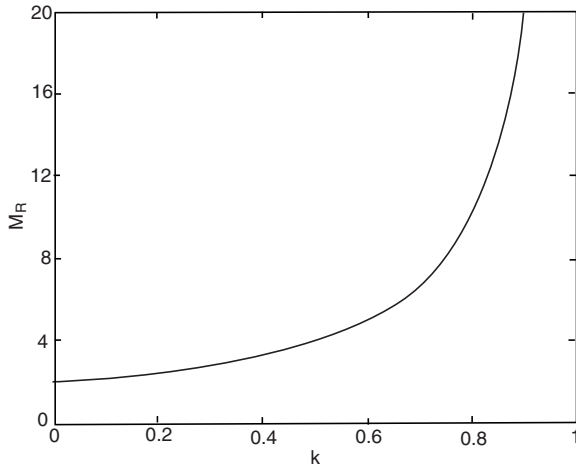


FIGURE 2.21

Voltage transfer gain M_R vs. k .

Currents i_{C1} and i_{C2} equal to $(i_{L1} + i_{L2})$ during **switch-off** period $(1 - k)T$, and the charges on capacitors C_1 and C_2 decrease, i.e.,

$$i_{C1} = i_{C2} = (i_{L1} + i_{L2}) = \frac{1}{1-k} I_O$$

The charges increase during **switch-on** period kT , so their average currents are

$$I_{C1} = I_{C2} = \frac{1-k}{k} (I_{L1} + I_{L2}) = \frac{1-k}{k} \left(\frac{k}{1-k} + 1 \right) I_O = \frac{I_O}{k} \quad (2.142)$$

During switch-off the source current i_l is 0, and in the switch-on period kT , it is

$$i_l = i_{L1} + i_{L2} + i_{C1} + i_{L3} + i_{C2}$$

Hence,

$$\begin{aligned} I_l &= k i_l = k(I_{L1} + I_{L2} + I_{C1} + I_{L3} + I_{C2}) = k[2(I_{L1} + I_{L2}) + 2I_{C1}] \\ &= 2k(I_{L1} + I_{L2}) \left(1 + \frac{1-k}{k} \right) = 2k \frac{I_{L2}}{1-k} \frac{1}{k} = \frac{2}{1-k} I_O \end{aligned} \quad (2.143)$$

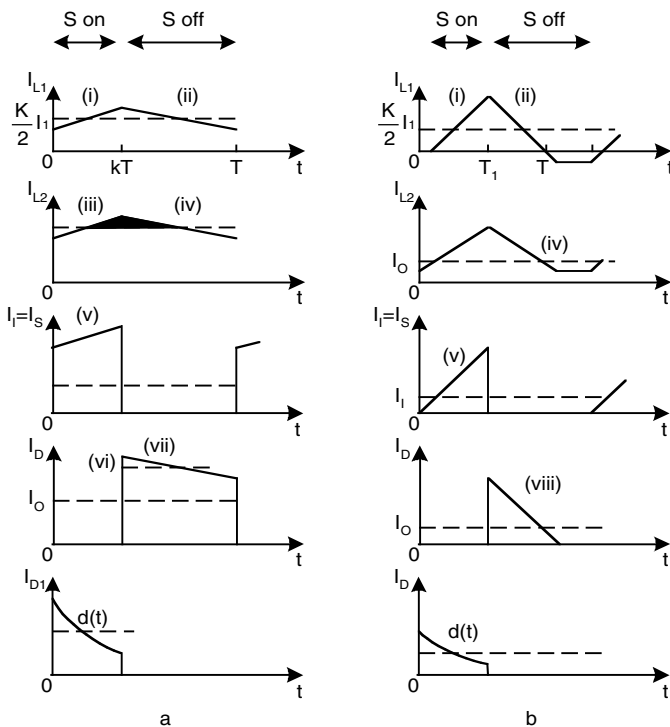


FIGURE 2.22

Some voltage and current waveforms of re-lift circuit.

2.3.3.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.22. Current i_{L1} increases and is supplied by V_I during switch-on period kT . It decreases and is reversely biased by $-(V_C - 2V_I - V_{L3})$ during switch-off period $(1 - k)T$. Therefore, its peak-to-peak variation is

$$\Delta i_{L1} = \frac{kTV_I}{L_1}$$

Considering Equation (2.140), the variation ratio of current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kV_I T}{kL_1 I_I} = \frac{1 - k}{2M_R} \frac{R}{fL_1} \quad (2.144)$$

Current i_{L2} increases and is supplied by the voltage $(V_I + V_C - V_O) = V_I$ during switch-on period kT . It decreases and is reversely biased by $-(V_O - 2V_I - V_{L3})$ during switch-off. Therefore, its peak-to-peak variation is

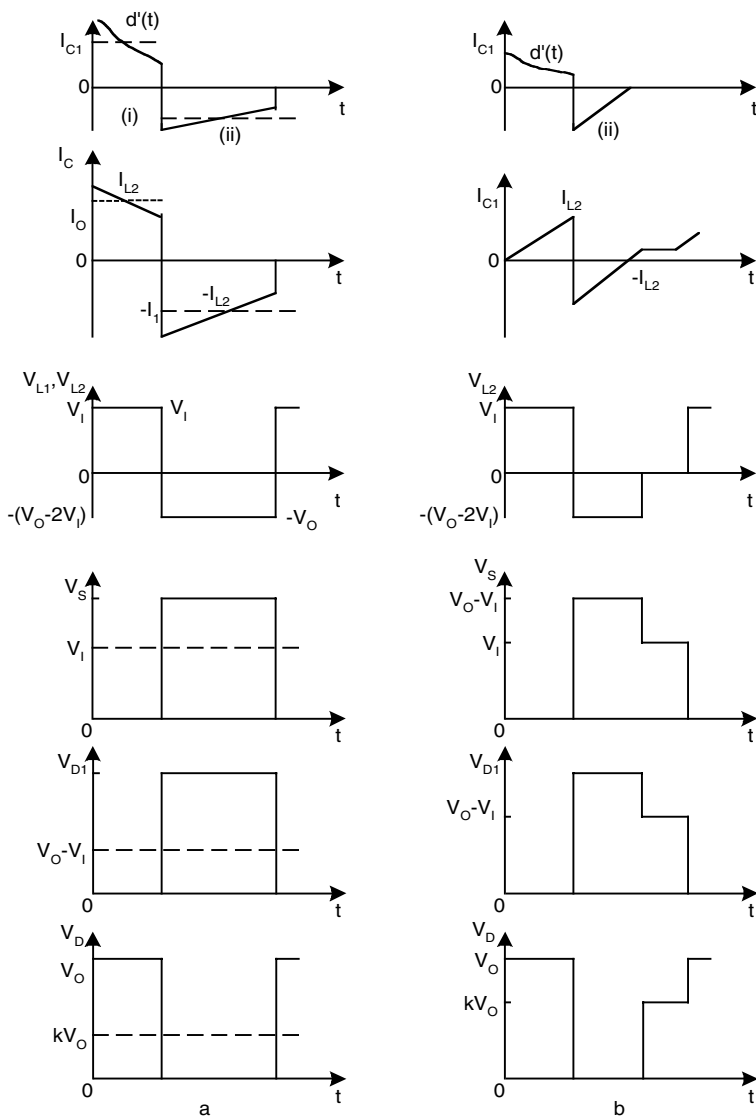


FIGURE 2.22 (continued)

$$\Delta i_{L2} = \frac{kTV_I}{L_2}$$

Considering Equation (2.72), the variation ratio of current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{kTV_I}{2L_2 I_O} = \frac{k}{2M_R} \frac{R}{fL_2} \quad (2.145)$$

When switch is off, the free-wheeling diode current is $i_D = i_{L1} + i_{L2}$ and

$$\Delta i_D = \Delta i_{L1} + \Delta i_{L2} = \frac{kTV_L}{L} = \frac{k(1-k)V_O}{2L} T \quad (2.146)$$

Considering Equation (2.71) and Equation (2.72),

$$I_D = I_{L1} + I_{L2} = \frac{I_O}{1-k}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D / 2}{I_D} = \frac{k(1-k)^2 TV_O}{4LI_O} = \frac{k(1-k)R}{2M_R fL} = \frac{k}{M_R^2} \frac{R}{fL} \quad (2.147)$$

Considering Equation (2.134) and Equation (2.141), the variation ratio of current i_{L3} is

$$\chi_1 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{kV_L T}{2L_3 \frac{1}{1-k} I_O} = \frac{k}{M_R^2} \frac{R}{fL_3} \quad (2.148)$$

If $L_1 = L_2 = 1 \text{ mH}$, $L_3 = 0.5 \text{ mH}$, $R = 160 \Omega$, $f = 50 \text{ kHz}$ and $k = 0.5$, we obtained that $\xi_1 = 0.2$, $\xi_2 = 0.2$, $\zeta = 0.1$ and $\chi_1 = 0.2$. Therefore, the variations of i_{L1} , i_{L2} and i_{L3} are small.

The peak-to-peak variation of v_C is

$$\Delta v_C = \frac{Q+}{C} = \frac{1-k}{C} TI_{L1} = \frac{k(1-k)}{2C} TI_L$$

Considering Equation (2.136), the variation ratio is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{k(1-k)TI_L}{4CV_O} = \frac{k}{2fCR} \quad (2.149)$$

The charges on capacitors C_1 and C_2 increase during switch-on period kT , and decrease during switch-off period $(1-k)T$ by the current $(I_{L1} + I_{L2})$. Therefore their peak-to-peak variations are

$$\Delta v_{C1} = \frac{(1-k)T(I_{L1} + I_{L2})}{C_1} = \frac{(1-k)I_L}{2C_1 f}$$

$$\Delta v_{C2} = \frac{(1-k)T(I_{L1} + I_{L2})}{C_2} = \frac{(1-k)I_L}{2C_2 f}$$

Considering $V_{C1} = V_{C2} = V_I$, the variation ratios of voltages v_{C1} and v_{C2} are

$$\sigma_1 = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{(1-k)I_I}{4fC_1V_I} = \frac{M_R}{2fC_1R} \quad (2.150)$$

$$\sigma_2 = \frac{\Delta v_{C2} / 2}{V_{C2}} = \frac{(1-k)I_I}{4V_I C_2 f} = \frac{M_R}{2fC_2R} \quad (2.151)$$

Considering Equation (2.84), the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{kT^2}{8C_O L_2} \frac{V_I}{V_O} = \frac{k}{8M_R} \frac{1}{f^2 C_O L_2} \quad (2.152)$$

If $C = C_1 = C_2 = C_O = 20 \mu\text{F}$, $L_2 = 1 \text{ mH}$, $R = 160 \Omega$, $f = 50 \text{ kHz}$ and $k = 0.5$, we obtained that $\rho = 0.0016$, $\sigma_1 = \sigma_2 = 0.0125$, and $\varepsilon = 0.0003$. The ripples of v_C , v_{C1} , v_{C2} and v_{CO} are small. Therefore, the output voltage v_O is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_O(t)$ is almost a real DC waveform with very small ripple as well, and $I_O = V_O/R$.

2.3.3.4 Instantaneous Value of the Currents and Voltages

Referring to [Figure 2.22](#), the instantaneous current and voltage values are listed below:

$$v_s = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O & \text{for } kT < t \leq T \end{cases} \quad (2.153)$$

$$v_D = \begin{cases} V_O & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.154)$$

$$v_{D1} + v_{D2} = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O & \text{for } kT < t \leq T \end{cases} \quad (2.155)$$

$$v_{L3} = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -\frac{k}{1-k} V_I & \text{for } kT < t \leq T \end{cases} \quad (2.156)$$

$$v_{L1} = v_{L2} = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -[V_O - (2 - \frac{k}{1-k})V_I] & \text{for } kT < t \leq T \end{cases} \quad (2.157)$$

$$i_l = i_s = \begin{cases} i_{L1}(0) + i_{L2}(0) + i_{L3}(0) + \delta_1(t) + \delta_2(t) + \frac{V_l}{L}t + \frac{V_l}{L_3}t & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.158)$$

$$i_{L1} = \begin{cases} i_{L1}(0) + \frac{V_l}{L_1}t & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{V_o - (2 - \frac{k}{1-k})V_l}{L_1}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.159)$$

$$i_{L2} = \begin{cases} i_{L2}(0) + \frac{V_l}{L_2}t & \text{for } 0 < t \leq kT \\ i_{L2}(kT) - \frac{V_o - (2 - \frac{k}{1-k})V_l}{L_2}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.160)$$

$$i_{L3} = \begin{cases} i_{L3}(0) + \frac{V_l}{L_3}t & \text{for } 0 < t \leq kT \\ i_{L3}(kT) - \frac{\frac{k}{1-k}V_l}{L_3}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.161)$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ i_{L1}(kT) + i_{L2}(kT) - \frac{V_o - (2 - \frac{k}{1-k})V_l}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.162)$$

$$i_{D1} = \begin{cases} \delta_1(t) + \delta_2(t) & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.163)$$

$$i_{D2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.164)$$

$$i_c = \begin{cases} i_{L2}(0) + \frac{V_l}{L_2}t & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{V_o - V_l}{L_1}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.165)$$

$$i_{C1} = \begin{cases} \delta_1(t) & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) - i_{L2}(kT) + \frac{V_O - (2 + \frac{k}{1-k})V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.166)$$

$$i_{C2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) - i_{L2}(kT) + \frac{V_O - (2 + \frac{k}{1-k})V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.167)$$

$$i_{CO} = \begin{cases} i_{L2}(0) + \frac{V_I}{L_2}t - I_O & \text{for } 0 < t \leq kT \\ i_{L2}(kT) - \frac{V_O - (2 + \frac{k}{1-k})V_I}{L_2}(t - kT) - I_O & \text{for } kT < t \leq T \end{cases} \quad (2.168)$$

where $i_{L1}(0) = k I_I/2 - k V_I/2 f L_1$, $i_{L1}(kT) = k I_I/2 + k V_I/2 f L_1$, and $i_{L2}(0) = I_O - k V_I/2 f L_2$, $i_{L2}(kT) = I_O + k V_I/2 f L_2$, and $i_{L3}(0) = I_O + k I_I/2 - k V_I/2 f L_3$, $i_{L3}(kT) = I_O + k I_I/2 + k V_I/2 f L_3$.

2.3.3.5 Discontinuous Mode

Referring to Figure 2.20d, we can see that the diode current i_D becomes zero during switch off before next period switch on. The condition for discontinuous mode is

$$\zeta \geq 1$$

i.e.,

$$\frac{k}{M_R^2} \frac{R}{fL} \geq 1$$

$$\text{or} \quad M_R \leq \sqrt{k} \sqrt{\frac{R}{fL}} = \sqrt{k} \sqrt{z_N} \quad (2.169)$$

The graph of the boundary curve vs. the normalized load $z_N = R/fL$ is shown in Figure 2.23. It can be seen that the boundary curve has a minimum value of 3.0 at $k = 1/3$.

In this case the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_R]T$, where m_R is the **filling efficiency** and it is defined as:

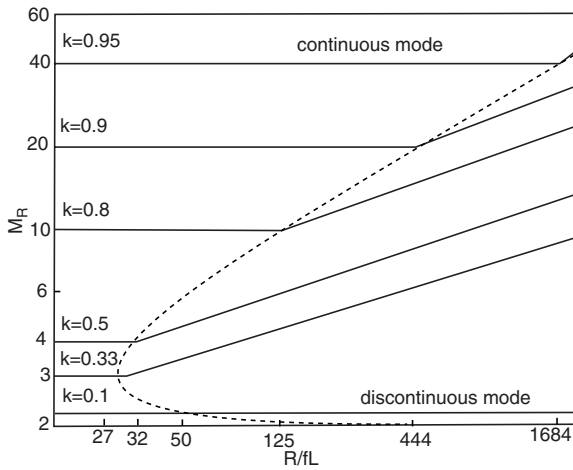


FIGURE 2.23

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$.

$$m_R = \frac{1}{\zeta} = \frac{M_R^2}{k \frac{R}{fL}} \quad (2.170)$$

Considering Equation (2.169), therefore $0 < m_R < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_RT$, for the current i_L

$$kTV_I = (1 - k)m_RT(V_C - 2V_I - V_{L3-off})$$

or

$$V_C = [2 + \frac{k}{1-k} + \frac{k}{(1-k)m_R}]V_I = [2 + \frac{k}{1-k} + k^2(1-k)\frac{R}{4fL}]V_I$$

with

$$\sqrt{k} \sqrt{\frac{R}{fL}} \geq \frac{2}{1-k}$$

and for the current i_{LO} $kT(V_I + V_C - V_O) = (1 - k)m_RT(V_O - 2V_I - V_{L3-off})$

Therefore, output voltage in discontinuous mode is

$$V_O = [2 + \frac{k}{1-k} + \frac{k}{(1-k)m_R}]V_I = [2 + \frac{k}{1-k} + k^2(1-k)\frac{R}{4fL}]V_I$$

with

$$\sqrt{k} \sqrt{\frac{R}{fL}} \geq \frac{2}{1-k} \quad (2.171)$$

i.e., the output voltage will linearly increase during load resistance R increasing. The output voltage vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.23](#). Larger load resistance R may cause higher output voltage in discontinuous mode.

2.3.3.6 Stability Analysis

Stability analysis is of vital importance for any converter circuit. According to the circuit network and control systems theory, the transfer functions in s -domain for switch-on and -off states are obtained:

$$G_{on} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{on} = \frac{sCR}{s^3 L_2 C C_O R + s^2 L_2 C + s(C + C_O)R + 1} \quad (2.172)$$

$$\begin{aligned} G_{off} &= \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{off} \\ &= \frac{\frac{R}{1+sC_O R} sC \frac{s(C_1 + C_2) + s^3 L_3 C_1 C_2}{s^2 C_1 C_2}}{\left(sC \frac{s(C_1 + C_2) + s^3 L_3 C_1 C_2}{s^2 C_1 C_2} \frac{R + sL_2 + s^2 L_2 C_O R}{1 + sC_O R} \right.} \\ &\quad \left. + \frac{s(C_1 + C_2) + s^3 L_3 C_1 C_2}{s^2 C_1 C_2} + \frac{R + sL_2 + s^2 L_2 C_O R}{1 + sC_O R} \right) \\ &= \frac{sCR[(C_1 + C_2) + s^2 L_3 C_1 C_2]}{\left(sC[(C_1 + C_2) + s^2 L_3 C_1 C_2][R + sL_2 + s^2 L_2 C_O R] + (1 + sC_O R)[(C_1 + C_2) \right.} \\ &\quad \left. + s^2 L_3 C_1 C_2] + sC_1 C_2[R + sL_2 + s^2 L_2 C_O R] \right)} \quad (2.173) \end{aligned}$$

where s is the Laplace operator. From Equation (2.172) and Equation (2.173) in Laplace transform we can see that the re-lift converter is a third order control circuit for switch-on state and a fifth order control circuit for switch-off state.

For the switch-on state, the zeros are determined by the equation when the numerator of Equation (2.172) is equal to zero, and the poles are determined by the equation when the denominator of Equation (2.172) is equal to zero. There is a zero at the origin point (0, 0). Since the equation to determine the poles is the equation with all positive real coefficients, according to the **Gauss theorem**, the three poles are: one negative real pole (p_3)

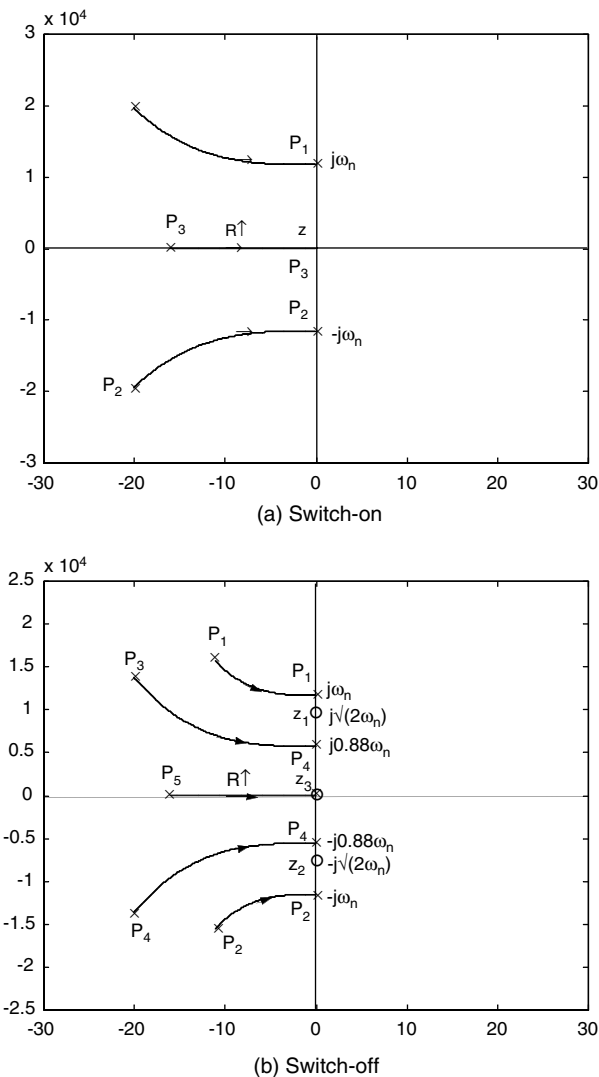


FIGURE 2.24

Stability analysis of re-lift circuit. (a) Switch-on. (b) Switch-off.

and a pair of conjugate complex poles with negative real part ($p_{1,2}$). The three poles are located in the left half plane in Figure 2.24, so that the re-lift converter is stable. When the load resistance R increases and intends towards infinity, the three poles move. The real pole goes to the origin point and eliminates with the zero. The pair of conjugate complex poles becomes a pair of imaginary poles locating on the imaginary axis. Assuming that all capacitors have same capacitance C , and $L_1 = L_2$ $\{L = L_1 L_2 / (L_1 + L_2)$ or $L_2 = 2L\}$ and $L_3 = L$, Equation (2.172) becomes:

$$G_{on} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{on} = \frac{1}{s^2 L_2 C_O + \frac{C + C_O}{C}} = \frac{1}{2s^2 LC + 2} \quad (2.174)$$

and the pair of imaginary poles is

$$p_{1,2} = \pm j \sqrt{\frac{C + C_O}{L_2 C C_O}} = \pm j \sqrt{\frac{1}{LC}} = \pm j \omega_n \quad \text{poles for switch on} \quad (2.175)$$

where $\omega_n = (LC)^{-1/2}$ is the re-lift converter normal angular frequency.

For the switch-off state, the zeros are determined by the equation when the numerator of Equation (2.173) is equal to zero, and the poles are determined by the equation when the denominator of Equation (2.173) is equal to zero. There are three zeros: one (z_3) at the original point (0, 0) and two zeros ($z_{1,2}$) on the imaginary axis which are

$$z_{1,2} = \pm j \sqrt{\frac{C_1 + C_2}{L_3 C_1 C_2}} = \pm j \sqrt{\frac{2}{LC}} = \pm j \sqrt{2} \omega_n \quad \text{zeros for switch off} \quad (2.176)$$

Since the equation to determine the poles is the equation with all positive real coefficients, according to the **Gauss theorem**, the five poles are one negative real pole (p_5) and two pairs of conjugate complex poles with negative real parts ($p_{1,2}$ and $p_{3,4}$). There are five poles located in the left-hand half plane in [Figure 2.24](#), so that the re-lift converter is stable. When the load resistance R increases and intends towards infinity, the five poles move. The real pole goes to the origin point and eliminates with the zero. The two pairs of conjugate complex poles become two pairs of imaginary poles locating on the imaginary axis. Assuming that all capacitors have same capacitance C , and $L_1 = L_2$ ($L = L_1 L_2 / (L_1 + L_2)$ or $L_2 = 2L$) and $L_3 = L$, Equation (2.173) becomes:

$$\begin{aligned} G_{off} = \left\{ \frac{\delta V_O(s)}{\delta V_I(s)} \right\}_{off} &= \frac{C(C_1 + C_2) + s^2 L_3 C C_1 C_2}{\left((C C_1 + C C_2 + C_1 C_2 + s^2 L_3 C C_1 C_2)(1 + s^2 L_2 C_O) \right.} \\ &\quad \left. + (C_O C_1 + C_O C_2 + s^2 L_3 C_O C_1 C_2) \right) \\ &= \frac{2C^2 + s^2 LC^3}{(3C^2 + s^2 LC^3)(1 + 2s^2 LC) + (2C^2 + s^2 LC^3)} = \frac{2 + s^2 LC}{2s^4 L^2 C^2 + 8s^2 LC + 5} \quad (2.177) \end{aligned}$$

and the two pairs of imaginary poles are

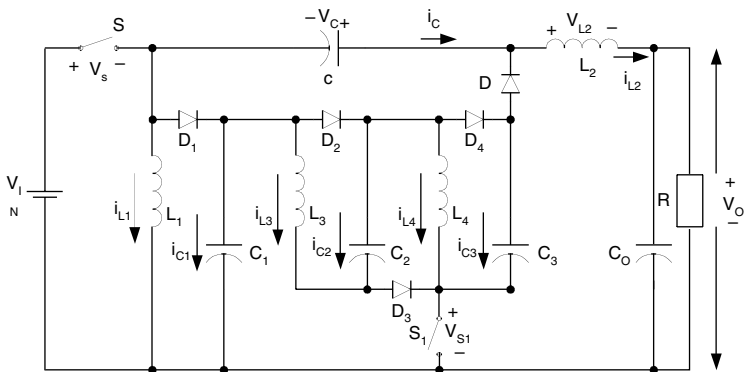


FIGURE 2.25
Triple-lift circuit.

$$s^2 LC = \frac{-8 \pm \sqrt{64 - 40}}{4} = -2 \pm \frac{\sqrt{6}}{2} = \begin{cases} -3.225 \\ -0.775 \end{cases}$$

poles for switch off, so that

$$p_{1,2} = \pm j 1.8 \omega_n$$

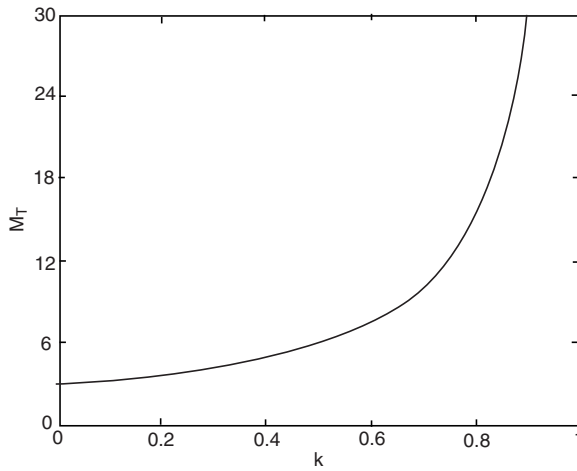
and

$$p_{3,4} = \pm j 0.88 \omega_n \quad (2.178)$$

For both states when R tends to infinity all poles are locating on the stability boundary. Therefore, the circuit works in the critical state. From Equation (2.171) the output voltage will be infinity. This fact is verified by the experimental results and computer simulation results. When $R = \infty$, the output voltage v_o tends to be a very high value. In this particular circuit since there is some leakage current across the capacitor C_o , the output voltage v_o can not be infinity.

2.3.4 Multiple-Lift Circuits

Referring to [Figure 2.20a](#), it is possible to build multiple-lift circuits using the parts (L_3 - C_2 - S_1 - D_2) multiple times. For example in [Figure 2.25](#) the parts (L_4 - C_3 - D_3 - D_4) were added in the triple-lift circuit. Because the voltage at the point of the joint (L_4 - C_3) is positive value and higher than that at the point of the joint (L_3 - C_2), so that we can use a diode D_3 to replace the switch (S_2). For multiple-lift circuits all further switches can be replaced by diodes. According to this principle, triple-lift circuits and quadruple-lift circuits were built as shown in [Figure 2.25](#) and [Figure 2.28](#). In this book it is not necessary to introduce the particular analysis and calculations one by one to readers. However, their formulas are shown in this section.

**FIGURE 2.26**

Voltage transfer gain M_T vs. k .

2.3.4.1 Triple-Lift Circuit

A triple-lift circuit is shown in [Figure 2.25](#), and it consists of two static switches S and S_1 ; four inductors L_1 , L_2 , L_3 , and L_4 ; and five capacitors C , C_1 , C_2 , C_3 , and C_O ; and five diodes. Capacitors C_1 , C_2 , and C_3 perform characteristics to lift the capacitor voltage V_C by three times the source voltage V_I . L_3 and L_4 perform the function as ladder joints to link the three capacitors C_1 , C_2 , and C_3 and lift the capacitor voltage V_C up. Current $i_{C1}(t)$, $i_{C2}(t)$, and $i_{C3}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C1} = v_{C2} = v_{C3} = V_I$ in steady state.

The output voltage and current are

$$V_O = \frac{3}{1-k} V_I \quad (2.179)$$

and

$$I_O = \frac{1-k}{3} I_I \quad (2.180)$$

The voltage transfer gain in continuous mode is

$$M_T = \frac{V_O}{V_I} = \frac{3}{1-k} \quad (2.181)$$

The curve of M_T vs. k is shown in [Figure 2.26](#).

Other average voltages:

$$V_C = V_O \quad V_{C1} = V_{C2} = V_{C3} = V_I$$

Other average currents:

$$I_{L2} = I_O \quad I_{L1} = \frac{k}{1-k} I_O$$

$$I_{L3} = I_{L4} = I_{L1} + I_{L2} = \frac{1}{1-k} I_O$$

Current variations:

$$\xi_1 = \frac{1-k}{2M_T} \frac{R}{fL_1} \quad \xi_2 = \frac{k}{2M_T} \frac{R}{fL_2} \quad \zeta = \frac{k(1-k)R}{2M_T fL} = \frac{k}{M_T^2} \frac{3R}{2fL}$$

$$\chi_1 = \frac{k}{M_T^2} \frac{R}{fL_3} \quad \chi_2 = \frac{k}{M_T^2} \frac{R}{fL_4}$$

Voltage variations:

$$\rho = \frac{k}{2fCR} \quad \sigma_1 = \frac{M_T}{2fC_1R}$$

$$\sigma_2 = \frac{M_T}{2fC_2R} \quad \sigma_3 = \frac{M_T}{2fC_3R}$$

The variation ratio of output voltage v_c is

$$\varepsilon = \frac{k}{8M_T} \frac{1}{f^2 C_O L_2} \quad (2.182)$$

The output voltage ripple is very small. The boundary between continuous and discontinuous conduction modes is

$$M_T \leq \sqrt{k} \sqrt{\frac{3R}{2fL}} = \sqrt{\frac{3kz_N}{2}} \quad (2.183)$$

This boundary curve is shown in [Figure 2.27](#). Comparing with Equations (2.95), (2.165) (2.169), and (2.183), it can be seen that the boundary curve has a minimum value of M_T that is equal to 4.5, corresponding to $k = 1/3$.

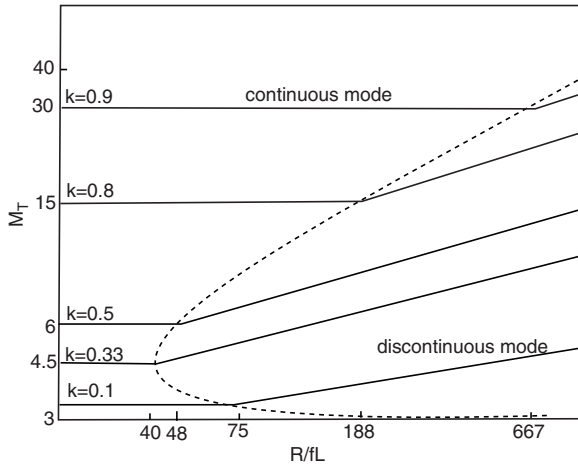


FIGURE 2.27

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$.

In discontinuous mode the current i_D exists in the period between kT and $[k + (1 - k)m_T]T$, where m_T is the filling efficiency that is

$$m_T = \frac{1}{\zeta} = \frac{M_T^2}{k \frac{3R}{2fL}} \quad (2.184)$$

Considering Equation (2.183), therefore, $0 < m_T < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_T T$, for the current i_{L1}

$$kTV_I = (1 - k)m_T T(V_C - 3V_I - V_{L3-off} - V_{L4-off})$$

or

$$V_C = \left[3 + \frac{2k}{1 - k} + \frac{k}{(1 - k)m_T}\right]V_I = \left[3 + \frac{2k}{1 - k} + k^2(1 - k)\frac{R}{6fL}\right]V_I$$

with $\sqrt{k} \sqrt{\frac{3R}{2fL}} \geq \frac{3}{1 - k}$

and for the current i_{L2} $kT(V_I + V_C - V_O) = (1 - k)m_T T(V_O - 2V_I - V_{L3-off} - V_{L4-off})$

Therefore, output voltage in discontinuous mode is

$$V_O = \left[3 + \frac{2k}{1 - k} + \frac{k}{(1 - k)m_T}\right]V_I = \left[3 + \frac{2k}{1 - k} + k^2(1 - k)\frac{R}{6fL}\right]V_I$$

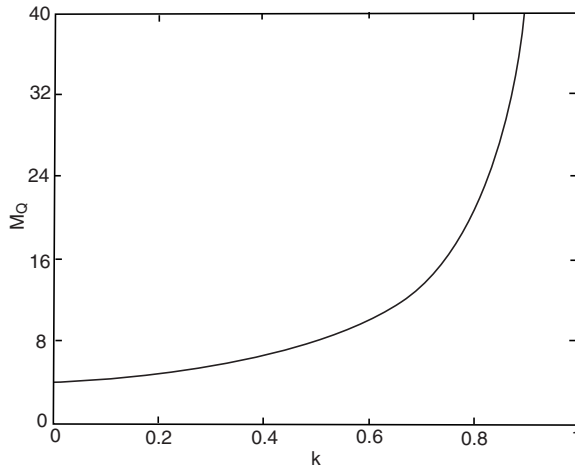


FIGURE 2.29
Voltage transfer gain M_Q vs. k .

$$M_Q = \frac{V_O}{V_I} = \frac{4}{1-k} \quad (2.188)$$

The curve of M_Q vs. k is shown in [Figure 2.29](#). Other average voltages:

$$V_C = V_O; \quad V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_I$$

Other average currents:

$$I_{L2} = I_O; \quad I_{L1} = \frac{k}{1-k} I_O$$

$$I_{L3} = I_{L4} = I_{L5} = I_{L1} + I_{L2} = \frac{1}{1-k} I_O$$

Current variations:

$$\xi_1 = \frac{1-k}{2M_Q} \frac{R}{fL_1} \quad \xi_2 = \frac{k}{2M_Q} \frac{R}{fL_2} \quad \xi = \frac{k(1-k)R}{2M_Q fL} = \frac{k}{M_Q^2} \frac{2R}{fL}$$

$$\chi_1 = \frac{k}{M_Q^2} \frac{R}{fL_3} \quad \chi_2 = \frac{k}{M_Q^2} \frac{R}{fL_4} \quad \chi_3 = \frac{k}{M_Q^2} \frac{R}{fL_5}$$

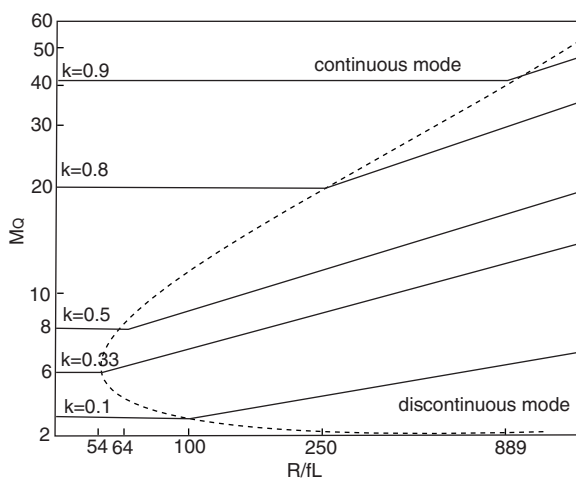


FIGURE 2.30

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$.

Voltage variations:

$$\rho = \frac{k}{2fCR} \quad \sigma_1 = \frac{M_Q}{2fC_1R}$$

$$\sigma_2 = \frac{M_Q}{2fC_2R} \quad \sigma_3 = \frac{M_Q}{2fC_3R} \quad \sigma_4 = \frac{M_Q}{2fC_4R}$$

The variation ratio of output voltage V_c is

$$\varepsilon = \frac{k}{8M_Q} \frac{1}{f^2 C_0 L_2} \quad (2.189)$$

The output voltage ripple is very small.

The boundary between continuous and discontinuous modes is

$$M_Q \leq \sqrt{k} \sqrt{\frac{2R}{fL}} = \sqrt{2kz_N} \quad (2.190)$$

This boundary curve is shown in [Figure 2.30](#). Comparing with Equations (2.95), (2.127), (2.169), (2.183), and (2.190), it can be seen that this boundary curve has a minimum value of M_Q that is equal to 6.0, corresponding to $k = 1/3$.

In discontinuous mode the current i_D exists in the period between kT and $[k + (1 - k)m_Q]T$, where m_Q is the filling efficiency that is

$$m_Q = \frac{1}{\zeta} = \frac{M_Q^2}{k \frac{2R}{fL}} \quad (2.191)$$

Considering Equation (2.190), therefore $0 < m_Q < 1$. Since the current i_D becomes zero at $t = kT + (1 - k)m_QT$, for the current i_{L1} we have

$$kTV_I = (1 - k)m_QT(V_C - 4V_I - V_{L3-off} - V_{L4-off} - V_{L5-off})$$

or

$$V_C = [4 + \frac{3k}{1-k} + \frac{k}{(1-k)m_Q}]V_I = [4 + \frac{3k}{1-k} + k^2(1-k)\frac{R}{8fL}]V_I$$

with

$$\sqrt{k} \sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k}$$

and for current i_{L2} we have

$$kT(V_I + V_C - V_O) = (1 - k)m_QT(V_O - 2V_I - V_{L3-off} - V_{L4-off} - V_{L5-off})$$

Therefore, output voltage in discontinuous mode is

$$V_O = [4 + \frac{3k}{1-k} + \frac{k}{(1-k)m_Q}]V_I = [4 + \frac{3k}{1-k} + k^2(1-k)\frac{R}{8fL}]V_I$$

with

$$\sqrt{k} \sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k} \quad (2.192)$$

i.e., the output voltage will linearly increase during load resistance R increasing, as shown in [Figure 2.30](#).

2.3.5 Summary

From the analysis and calculation in previous sections, the common formulas for all circuits can be obtained:

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O} \quad L = \frac{L_1 L_2}{L_1 + L_2} \quad z_N = \frac{R}{fL} \quad R = \frac{V_O}{I_O}$$

Current variations:

$$\xi_1 = \frac{1-k}{2M} \frac{R}{fL_1} \quad \xi_2 = \frac{k}{2M} \frac{R}{fL_2} \quad \chi_j = \frac{k}{M^2} \frac{R}{fL_{j+2}} \quad (j = 1, 2, 3, \dots)$$

Voltage variations:

$$\rho = \frac{k}{2fCR} \quad \varepsilon = \frac{k}{8M} \frac{1}{f^2 C_O L_2} \quad \sigma_j = \frac{M}{2fC_j R} \quad (j = 1, 2, 3, 4, \dots)$$

In order to write common formulas for the boundaries between continuous and discontinuous modes and output voltage for all circuits, the circuits can be numbered. The definition is that subscript 0 means the elementary circuit, subscript 1 means the self-lift circuit, subscript 2 means the re-lift circuit, subscript 3 means the triple-lift circuit, subscript 4 means the quadruple-lift circuit, and so on.

The voltage transfer gain is

$$M_j = \frac{k^{h(j)}[j+h(j)]}{1-k} \quad j = 0, 1, 2, 3, 4, \dots \quad (2.193)$$

The free-wheeling diode current i_D 's variation is

$$\zeta_j = \frac{k^{[1+h(j)]}}{M_j^2} \frac{j+h(j)}{2} z_N \quad (2.194)$$

The boundaries are determined by the condition:

$$\zeta_j \geq 1$$

or

$$\frac{k^{[1+h(j)]}}{M_j^2} \frac{j+h(j)}{2} z_N \geq 1 \quad j = 0, 1, 2, 3, 4, \dots \quad (2.195)$$

Therefore, the boundaries between continuous and discontinuous modes for all circuits are

$$M_j = k^{\frac{1+h(j)}{2}} \sqrt{\frac{j+h(j)}{2} z_N} \quad j = 0, 1, 2, 3, 4, \dots \quad (2.196)$$

The filling efficiency is

$$m_j = \frac{1}{\zeta_j} = \frac{M_j^2}{k^{[1+h(j)]}} \frac{2}{j+h(j)} \frac{1}{z_N} \quad (2.197)$$

The output voltage in discontinuous mode for all circuits is

$$V_{O-j} = \left[j + \frac{j+h(j)-1}{1-k} + k^{[2-u(j)]} \frac{1-k}{2[j+h(j)]} z_N \right] V_I \quad j = 0, 1, 2, 3, 4, \dots \quad (2.198)$$

where

$$h(j) = \begin{cases} 0 & \text{if } j \geq 1 \\ 1 & \text{if } j = 0 \end{cases} \quad \text{is the **Hong Function**} \quad (2.199)$$

Assuming that $f = 50$ kHz, $L_1 = L_2 = 1$ mH, $L_2 = L_3 = L_4 = L_5 = 0.5$ mH, $C = C_1 = C_2 = C_3 = C_4 = C_O = 20$ μ F and the source voltage $V_I = 10$ V, the value of the output voltage V_O with various conduction duty k in continuous mode are shown in [Figure 2.31](#). Typically, some values of the output voltage V_O and its ripples in conduction duty $k = 0.33, 0.5, 0.75$ and 0.9 are listed in [Table 2.1](#). From these data it states the fact that the output voltage of all Luo-Converters is almost a real DC voltage with very small ripple.

The boundaries between continuous and discontinuous modes of all circuits are shown in [Figure 2.32](#). The curves of all M vs. z_N state that the continuous mode area increases from M_E via M_S, M_R, M_T to M_Q . The boundary of the elementary circuit is a monorising curve, but other curves are not monorising. There are minimum values of the boundaries of other circuits, which of M_S, M_R, M_T and M_Q correspond at $k = 1/3$.

2.3.6 Discussion

Some important points are vital for particular circuit design. They are discussed in the following sections.

2.3.6.1 Discontinuous-Conduction Mode

Usually, the industrial applications require the DC-DC converters to work in continuous mode. However, it is irresistible that DC-DC converter works

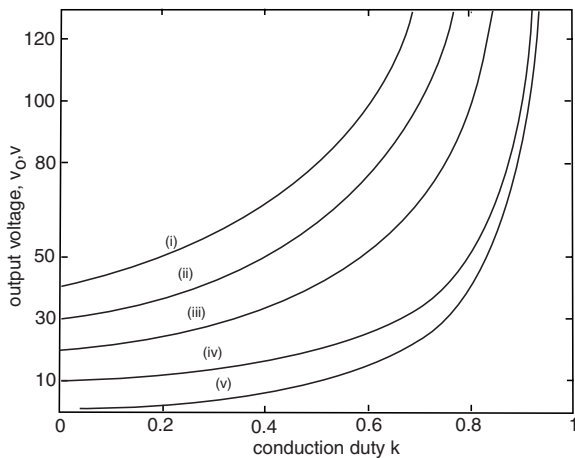


FIGURE 2.31

Output voltages of all positive output Luo-converters ($V_I = 10$ V).

TABLE 2.1

Comparison among Five Positive Output Luo-Converters

Positive Output Luo-Converters	I_O	V_O	V_O ($V_I = 10$ V)			
			$k = 0.33$	$k = 0.5$	$k = 0.75$	$k = 0.9$
Elementary Circuit	$I_O = \frac{1-k}{k} I_I$	$V_O = \frac{k}{1-k} V_I$	5 V	10 V	30 V	90 V
Self-Lift Circuit	$I_O = (1-k) I_I$	$V_O = \frac{1}{1-k} V_I$	15 V	20 V	40 V	100 V
Re-Lift Circuit	$I_O = \frac{1-k}{2} I_I$	$V_O = \frac{2}{1-k} V_I$	30 V	40 V	80 V	200 V
Triple-Lift Circuit	$I_O = \frac{1-k}{3} I_I$	$V_O = \frac{3}{1-k} V_I$	45 V	60 V	120 V	300 V
Quadruple-Lift Circuit	$I_O = \frac{1-k}{4} I_I$	$V_O = \frac{4}{1-k} V_I$	60 V	80 V	160 V	400 V

in discontinuous mode sometimes. The analysis in Section 2.3.2 through Section 2.3.5 shows that during switch-off if current i_D becomes zero before next period switch-on, the state is called discontinuous mode. The following factors affect the diode current i_D to become discontinuous:

1. Switch frequency f is too low
2. Conduction duty cycle k is too small
3. Combined inductor L is too small
4. Load resistance R is too big

Discontinuous mode means i_D is discontinuous during switch-off. The output current $i_O(t)$ is still continuous if L_2 and C_O are large enough.

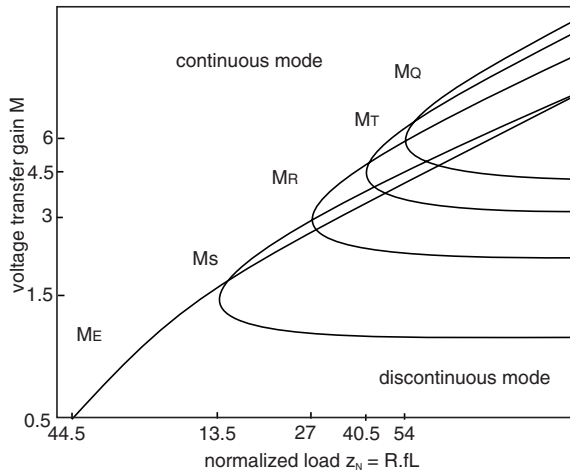


FIGURE 2.32

Boundaries between continuous and discontinuous modes of all positive output Luo-converters.

2.3.6.2 Output Voltage V_O vs. Conduction Duty k

Output voltage V_O is a positive value and is usually greater than the source voltage V_I when the conduction duty ratio is $k > 0.5$ for the elementary circuit, and any value in the range of $0 < k < 1$ for self-lift, re-lift, and multiple-lift circuits. Although small k results that the output voltage V_O of self-lift and re-lift circuits is greater than V_I and $2V_I$ and so on, when $k = 0$ it results in $V_O = 0$ because switch S is never turned on.

If k is close to the value of 1, the ideal output voltage V_O should be a very big value. Unfortunately, because of the effect of parasitic elements, output voltage V_O falls down very quickly. Finally, $k = 1$ results in $V_O = 0$, not infinity for all circuits. In this case the accident of i_{L1} toward infinity will happen. The recommended value range of the conduction duty k is

$$0 < k < 0.9$$

2.3.6.3 Switch Frequency f

In this paper the repeating frequency $f = 50$ kHz was selected. Actually, switch frequency f can be selected in the range between 10 kHz and 500 kHz. Usually, the higher the frequency, the lower the ripples.

2.4 Negative Output Luo-Converters

Negative output Luo-converters perform the voltage conversion from positive to negative voltages using VL technique. They work in the third quadrant with large voltage amplification. Five circuits have been introduced. They are

- Elementary circuit
- Self-lift circuit
- Re-lift circuit
- Triple-lift circuit
- Quadruple-lift circuit

As the positive output Luo-converters, the **negative output Luo-converters** are another series of DC-DC step-up converters, which were developed from prototypes using voltage lift technique. These converters perform positive to negative DC-DC voltage increasing conversion with high power density, high efficiency, and cheap topology in simple structure.

The elementary circuit can perform step-down and step-up DC-DC conversion. The other negative output Luo-converters are derived from this elementary circuit, they are the self-lift circuit, re-lift circuit, and multiple-lift circuits (e.g., triple-lift and quadruple-lift circuits) shown in the corresponding figures and introduced in the next sections respectively. Switch S in these diagrams is a P-channel power MOSFET device (PMOS). It is driven by a PWM switch signal with repeating frequency f and conduction duty k . In this book the switch repeating period is $T = 1/f$, so that the switch-on period is kT and switch-off period is $(1 - k)T$. For all circuits, the load is usually resistive, i. e., $R = V_O/I_O$; the normalized load is $z_N = R/fL$. Each converter consists of a negative Luo-pump and a “Π”-type filter C - L_O - C_O , and a lift circuit (except elementary circuit). The pump inductor L absorbs the energy from source during switch-on and transfers the stored energy to capacitor C during switch-off. The energy on capacitor C is then delivered to load during switch-on. Therefore, if the voltage V_C is high the output voltage V_O is correspondingly high.

When the switch S is turned off the current i_D flows through the free-wheeling diode D . This current descends in whole switch-off period $(1 - k)T$. If current i_D does not become zero before switch S is turned on again, we define this working state to be continuous mode. If current i_D becomes zero before switch S is turned on again, we define this working state to be discontinuous mode.

The directions of all voltages and currents are indicated in the figures. All descriptions and calculations in the text are concentrated to the absolute values. In this paper for any component X , its instantaneous current and voltage values are expressed as i_X and v_X , or $i_X(t)$ and $v_X(t)$, and its average current and voltage values are expressed as I_X and V_X . For general description, the output voltage and current are V_O and I_O ; the input voltage and current are V_I and I_I . Assuming the output power equals the input power,

$$P_O = P_{IN} \quad \text{or} \quad V_O I_O = V_I I_I$$

The following symbols are used in the text of this paper.

The voltage transfer gain is in **CCM**:

$$M = \frac{V_O}{V_I} = \frac{I_L}{I_O}$$

Variation ratio of current i_L :

$$\zeta = \frac{\Delta i_L / 2}{I_L}$$

Variation ratio of current i_{LO} :

$$\xi = \frac{\Delta i_{LO} / 2}{I_{LO}}$$

Variation ratio of current i_D :

$$\zeta = \frac{\Delta i_D / 2}{I_L} \quad \text{during switch-off, } i_D = i_L$$

Variation ratio of current i_{Lj} is

$$\chi_j = \frac{\Delta i_{Lj} / 2}{I_{Lj}} \quad j = 1, 2, 3, \dots$$

Variation ratio of voltage v_C :

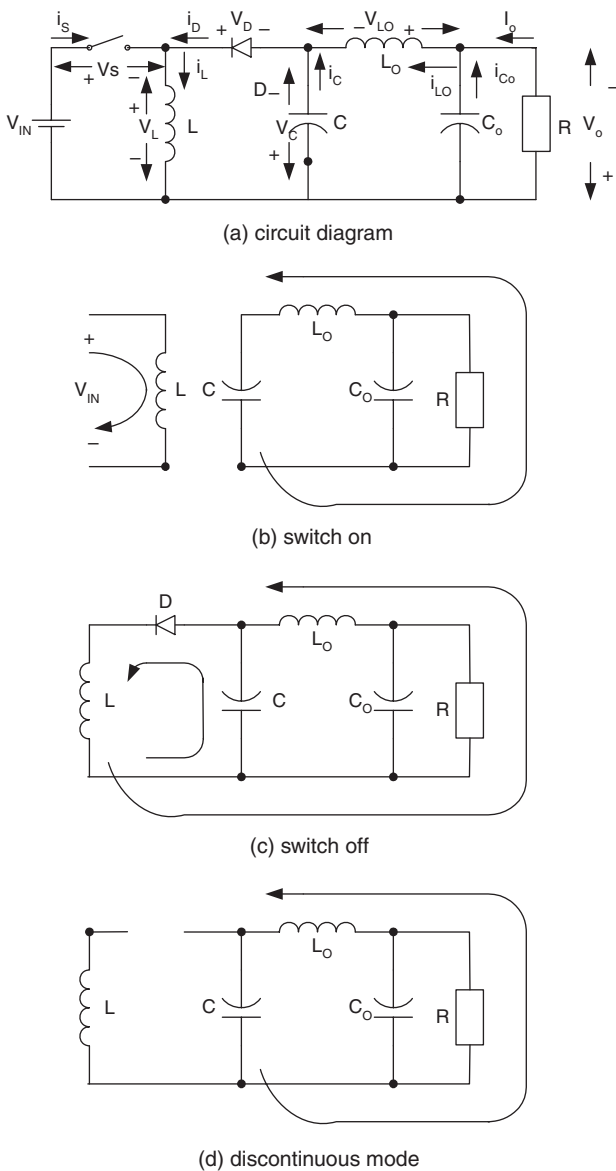
$$\rho = \frac{\Delta v_C / 2}{V_C}$$

Variation ratio of voltage v_{Cj} :

$$\sigma_j = \frac{\Delta v_{Cj} / 2}{V_{Cj}} \quad j = 1, 2, 3, 4, \dots$$

Variation ratio of output voltage $v_O = v_{CO}$:

$$\varepsilon = \frac{\Delta v_O / 2}{V_O}$$

**FIGURE 2.33**

Elementary circuit: (a) circuit diagram; (b) switch-on; (c) switch-off; (d) discontinuous mode.

2.4.1 Elementary Circuit

The elementary circuit, and its switch-on and -off equivalent circuits are shown in Figure 2.33. This circuit can be considered as a combination of an electronic pump S - L - D - C and a “ Π ”-type low-pass filter C - L_O - C_O . The electronic

pump injects certain energy to the low-pass filter every cycle. Capacitor C in Figure 2.33 acts as the primary means of storing and transferring energy from the input source to the output load. Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, i.e., $v_C(t) \approx V_C$, even though it stores and transfers energy from the input to the output.

2.4.1.1 Circuit Description

When switch S is on, the equivalent circuit is shown in Figure 2.33b. In this case the source current $i_l = i_L$. Inductor L absorbs energy from the source, and current i_L linearly increases with slope V_l/L . In the mean time the diode D is blocked since it is inversely biased. Inductor L_O keeps the output current I_O continuous and transfers energy from capacitor C to the load R , i.e., $i_{C-on} = i_{L_O}$. When switch S is off, the equivalent circuit is shown in Figure 2.33c. In this case the source current $i_l = 0$. Current i_L flows through the free-wheeling diode D to charge capacitor C and enhances current i_{L_O} . Inductor L transfers its stored energy to capacitor C and load R via inductor L_O , i.e., $i_L = i_{C-off} + i_{L_O}$. Thus, currents i_L decrease.

2.4.1.2 Average Voltages and Currents

The output current $I_O = I_{L_O}$ because the capacitor C_O does not consume any energy in the steady state. The average output current is

$$I_O = I_{L_O} = I_{C-on} \quad (2.200)$$

The charge on the capacitor C increases during switch-off:

$$Q+ = (1 - k) T I_{C-off}$$

And it decreases during switch-on:

$$Q- = k T I_{C-on} \quad (2.201)$$

In a whole repeating period T ,

$$Q+ = Q-, \quad I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k} I_O$$

Therefore, the inductor current I_L is

$$I_L = I_{C-off} + I_O = \frac{I_O}{1-k} \quad (2.202)$$

Equation (2.200) and Equation (2.202) are available for all circuit of negative output Luo-converters. The source current is $i_I = i_L$ during switch-on period. Therefore, its average source current I_I is

$$I_I = k \times i_I = ki_L = kI_L = \frac{k}{1-k} I_O$$

or

$$I_O = \frac{1-k}{k} I_I \quad (2.203)$$

and the output voltage is

$$V_O = \frac{k}{1-k} V_I \quad (2.204)$$

The voltage transfer gain in continuous mode is

$$M_E = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{k}{1-k} \quad (2.205)$$

The curve of M_E vs. k is shown in [Figure 2.34](#). Current i_L increases and is supplied by V_I during switch-on. It decreases and is inversely biased by $-V_C$ during switch-off,

$$kTV_I = (1-k)TV_C \quad (2.206)$$

Therefore,

$$V_C = V_O = \frac{k}{1-k} V_I \quad (2.207)$$

2.4.1.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in [Figure 2.35](#). Current i_L increases and is supplied by V_I during switch-on. Thus, its peak-to-peak variation is

$$\Delta i_L = \frac{kTV_I}{L}$$

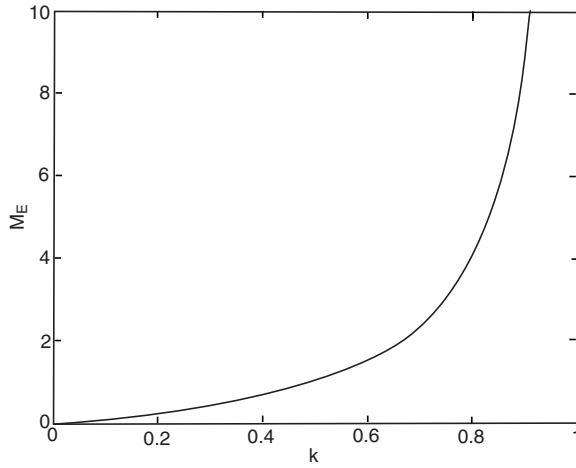


FIGURE 2.34
Voltage transfer gain M_E vs. k .

Considering Equation (2.202) and Equation (2.205), and $R = V_O/I_O$, the variation ratio of the current i_L is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_I T}{2LI_O} = \frac{k(1-k)R}{2M_E fL} = \frac{k^2}{M_E^2} \frac{R}{2fL} \quad (2.208)$$

Considering Equation (2.201), the peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q_-}{C} = \frac{k}{C} TI_O \quad (2.209)$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{kI_O T}{2CV_O} = \frac{k}{2} \frac{1}{fCR} \quad (2.210)$$

Since voltage V_O variation is very small, the peak-to-peak variation of current i_{LO} is calculated by the area (B) of the triangle with the width of $T/2$ and height $\Delta v_C/2$.

$$\Delta i_{LO} = \frac{B}{L_O} = \frac{1}{2} \frac{T}{2} \frac{k}{2CL_O} TI_O = \frac{k}{8f^2 CL_O} I_O \quad (2.211)$$

Considering Equation (2.200), the variation ratio of current i_{LO} is

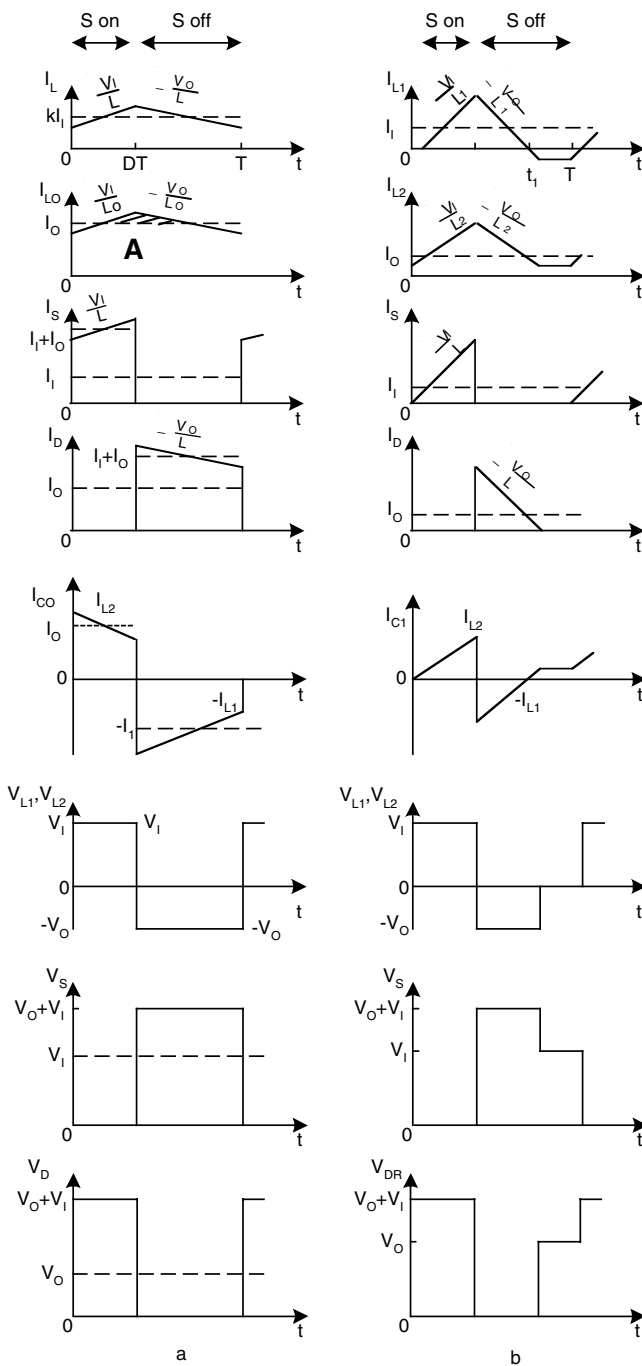


FIGURE 2.35

Some voltage and current waveforms of elementary circuit.

$$\xi = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{k}{16} \frac{1}{f^2 C L_O} \quad (2.212)$$

Since the voltage v_c is a triangle waveform, the difference between v_c and output voltage V_O causes the ripple of current i_{LO} , and the difference between i_{LO} and output current I_O causes the ripple of output voltage v_o . The ripple waveform of current i_{LO} should be a partial parabola in [Figure 2.35](#) because of the triangle waveform of Δv_c . To simplify the calculation we can treat the ripple waveform of current i_{LO} as a triangle waveform in [Figure 2.35](#) because the ripple of the current i_{LO} is very small. Therefore, the peak-to-peak variation of voltage v_{CO} is calculated by the area (A) of the triangle with the width of $T/2$ and height $\Delta i_{LO}/2$:

$$\Delta v_{CO} = \frac{A}{C_O} = \frac{1}{2} \frac{T}{2} \frac{k}{16 f^2 C C_O L_O} I_O = \frac{k}{64 f^3 C C_O L_O} I_O \quad (2.213)$$

The variation ratio of current v_{CO} is

$$\varepsilon = \frac{\Delta v_{CO} / 2}{V_{CO}} = \frac{k}{128 f^3 C C_O L_O} \frac{I_O}{V_O} = \frac{k}{128 f^3 C C_O L_O} R \quad (2.214)$$

Assuming that $f = 50$ kHz, $L = L_O = 100$ μ H, $C = C_O = 5$ μ F, $R = 10$ Ω and $k = 0.6$, we obtain

$$M_E = 1.5 \quad \zeta = 0.16 \quad \zeta = 0.03 \quad \rho = 0.12 \quad \text{and} \quad \varepsilon = 0.0015$$

The output voltage V_O is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_O = V_O/R$.

2.4.1.4 Instantaneous Values of Currents and Voltages

Referring to [Figure 2.35](#), the instantaneous current and voltage values are listed below:

$$v_s = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O & \text{for } kT < t \leq T \end{cases} \quad (2.215)$$

$$v_D = \begin{cases} V_I + V_O & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.216)$$

$$v_L = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -V_O & \text{for } kT < t \leq T \end{cases} \quad (2.217)$$

$$i_l = i_s = \begin{cases} i_L(0) + \frac{V_L}{L} t & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.218)$$

$$i_L = \begin{cases} i_L(0) + \frac{V_L}{L} t & \text{for } 0 < t \leq kT \\ i_L(kT) - \frac{V_O}{L} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.219)$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ i_L(kT) - \frac{V_O}{L} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.220)$$

$$i_C \approx \begin{cases} -I_{C-on} & \text{for } 0 < t \leq kT \\ I_{C-off} & \text{for } kT < t \leq T \end{cases} \quad (2.221)$$

where

$$i_L(0) = k I_l - k V_L / 2 f L$$

$$i_L(kT) = k I_l + k V_L / 2 f L$$

Since the instantaneous current i_{LO} and voltage v_{CO} are partial parabolas with very small ripples, they can be treated as a DC current and voltage.

2.4.1.5 Discontinuous Mode

Referring to [Figure 2.33d](#), we can see that the diode current i_D becomes zero during switch off before next period switch on. The condition for discontinuous mode is

$$\zeta \geq 1$$

i.e.,

$$\frac{k^2}{M_E^2} \frac{R}{2fL} \geq 1$$

or

$$M_E \leq k \sqrt{\frac{R}{2fL}} = k \sqrt{\frac{z_N}{2}} \quad (2.222)$$

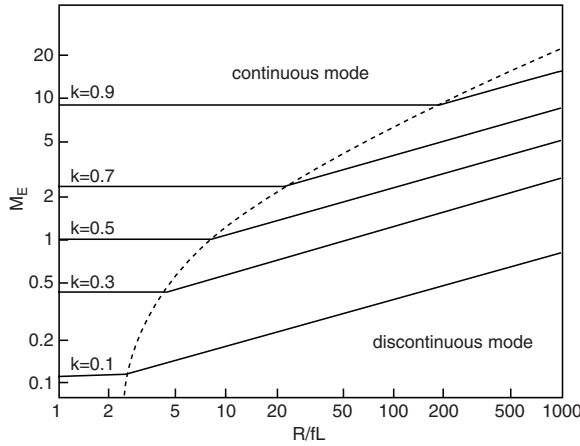


FIGURE 2.36

The boundary between continuous and discontinuous modes and output voltage vs. the normalized load $z_N = \sqrt{R/fL}$ (elementary circuit).

The graph of the boundary curve vs. the normalized load $z_N = R/fL$ is shown in Figure 2.36. It can be seen that the boundary curve is a monorising function of the parameter k .

In this case the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_E]T$, where m_E is the **filling efficiency** and it is defined as:

$$m_E = \frac{1}{\zeta} = \frac{M_E^2}{k^2 \frac{R}{2fL}} \quad (2.223)$$

Considering Equation (2.222), therefore $0 < m_E < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_ET$, for the current i_L

$$kTV_I = (1 - k)m_ETV_C$$

or

$$V_C = \frac{k}{(1 - k)m_E} V_I = k(1 - k) \frac{R}{2fL} V_I$$

$$\text{with } \sqrt{\frac{R}{2fL}} \geq \frac{1}{1 - k}$$

and for the current i_{LO}

$$kT(V_I + V_C - V_O) = (1 - k)m_ETV_O$$

Therefore, output voltage in discontinuous mode is

$$V_O = \frac{k}{(1-k)m_E} V_I = k(1-k) \frac{R}{2fL} V_I \quad \text{with} \quad \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \quad (2.224)$$

i.e., the output voltage will linearly increase during load resistance R increasing. The output voltage vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.36](#). Larger load resistance R may cause higher output voltage in discontinuous mode.

2.4.2 Self-Lift Circuit

Self-lift circuit, and its switch-on and -off equivalent circuits are shown in [Figure 2.37](#), which is derived from the elementary circuit. It consists of eight passive components. They are one static switch S ; two inductors L , L_O ; three capacitors C , C_1 , and C_O ; and two diodes D , D_1 . Comparing with [Figure 2.33](#) and [Figure 2.37](#), it can be seen that there are only one more capacitor C_1 and one more diode D_1 added into the self-lift circuit. Circuit C_1 - D_1 is the lift circuit. Capacitor C_1 functions to lift the capacitor voltage V_C by a source voltage V_I . Current $i_{C_1}(t)$ is an exponential function $\delta(t)$. It has a large value at the moment of power on, but it is small in the steady state because $V_{C_1} = V_I$.

2.4.2.1 Circuit Description

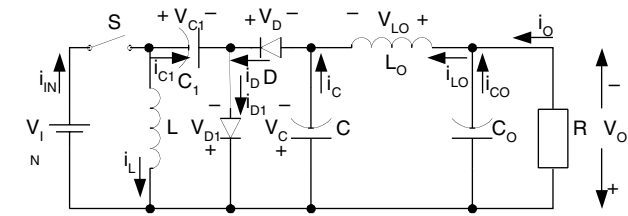
When switch S is on, the equivalent circuit is shown in [Figure 2.37b](#). In this case the source current $i_l = i_L + i_{C_1}$. Inductor L absorbs energy from the source, and current i_l linearly increases with slope V_I/L . In the mean time the diode D_1 is conducted and capacitor C_1 is charged by the current i_{C_1} . Inductor L_O keeps the output current I_O continuous and transfers energy from capacitor C to the load R , i.e., $i_{C-on} = i_{L_O}$. When switch S is off, the equivalent circuit is shown in [Figure 2.37c](#). In this case the source current $i_l = 0$. Current i_L flows through the free-wheeling diode D to charge capacitor C and enhances current i_{L_O} . Inductor L transfers its stored energy via capacitor C_1 to capacitor C and load R (via inductor L_O), i.e., $i_L = i_{C_1-off} = i_{C-off} + i_{L_O}$. Thus, current i_L decreases.

2.4.2.2 Average Voltages and Currents

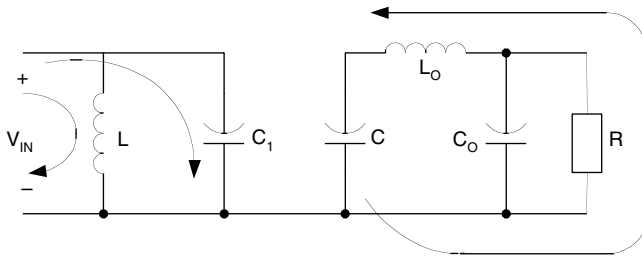
The output current $I_O = I_{L_O}$ because the capacitor C_O does not consume any energy in the steady state. The average output current:

$$I_O = I_{L_O} = I_{C-on} \quad (2.225)$$

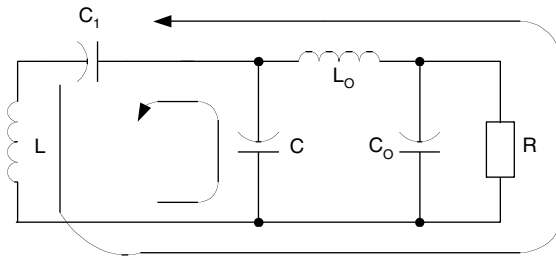
The charge of the capacitor C increases during switch-off:



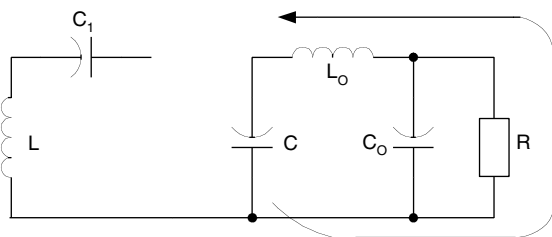
(a) circuit diagram



(b) switch on



(c) switch off



(d) discontinuous mode

FIGURE 2.37

Self-lift circuit: (a) circuit diagram; (b) switch on; (c) switch off; (d) discontinuous mode.

$$Q_+ = (1 - k) T I_{C-off}$$

And it decreases during switch-on:

$$Q_- = k T I_{C-on} \quad (2.226)$$

In a whole repeating period T , $Q_+ = Q_-$.

Thus,

$$I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k} I_O$$

Therefore, the inductor current I_L is

$$I_L = I_{C-off} + I_O = \frac{I_O}{1-k} \quad (2.227)$$

From [Figure 2.37](#),

$$I_{C1-off} = I_L = \frac{1}{1-k} I_O \quad (2.228)$$

and

$$I_{C1-on} = \frac{1-k}{k} I_{C1-off} = \frac{1}{k} I_O \quad (2.229)$$

In steady state we can use

$$V_{C1} = V_I$$

Investigate current i_L , it increases during switch-on with slope V_I/L and decreases during switch-off with slope $-(V_O - V_{C1})/L = -(V_O - V_I)/L$.

Therefore,

$$kV_I = (1-k)(V_O - V_I)$$

or

$$V_O = \frac{1}{1-k} V_I \quad (2.230)$$

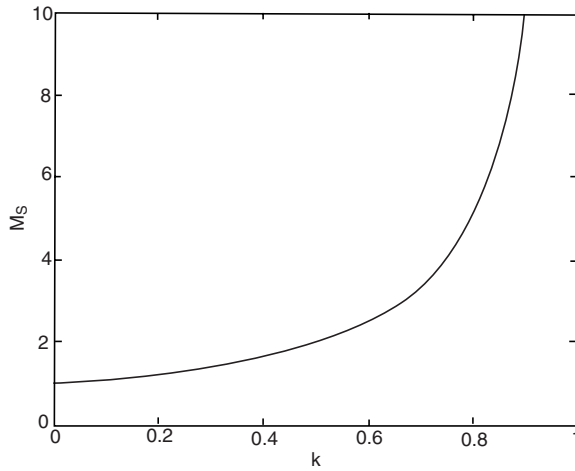


FIGURE 2.38

Voltage transfer gain M_s vs. k .

and

$$I_O = (1 - k)I_I \quad (2.231)$$

The voltage transfer gain in continuous mode is

$$M_s = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1 - k} \quad (2.232)$$

The curve of M_s vs. k is shown in [Figure 2.38](#).

Circuit (C- L_O - C_O) is a “ Π ” type low-pass filter. Therefore,

$$V_C = V_O = \frac{k}{1 - k} V_I \quad (2.233)$$

2.4.2.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in [Figure 2.39](#).

Current i_L increases and is supplied by V_I during switch-on. Thus, its peak-to-peak variation is

$$\Delta i_L = \frac{kTV_I}{L}$$

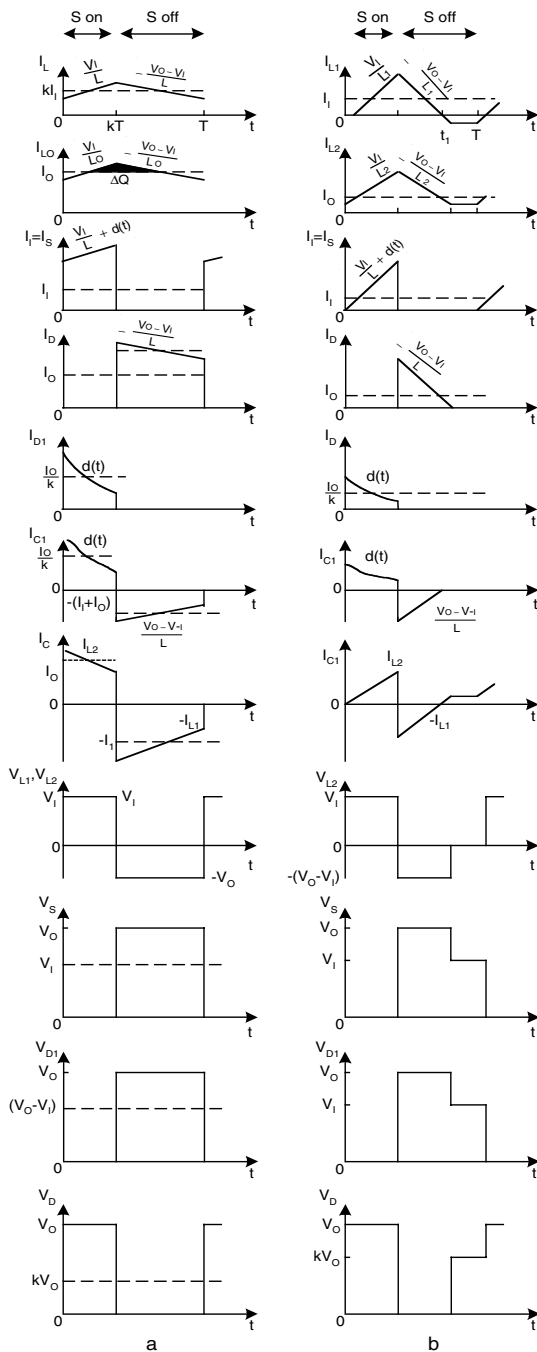


FIGURE 2.39

Some voltage and current waveforms of self-lift circuit.

Considering Equation (2.227) and $R = V_O/I_O$, the variation ratio of the current i_L is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_I T}{2LI_O} = \frac{k(1-k)R}{2M_S fL} = \frac{k}{M_S^2} \frac{R}{2fL} \quad (2.234)$$

Considering Equation (2.226), the peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q_-}{C} = \frac{k}{C} TI_O$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{kI_O T}{2CV_O} = \frac{k}{2} \frac{1}{fCR} \quad (2.235)$$

The peak-to-peak variation of voltage v_{C1} is

$$\Delta v_{C1} = \frac{kT}{C_1} I_{C1-on} = \frac{1}{fC} I_O$$

The variation ratio of voltage v_{C1} is

$$\sigma_1 = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{I_O}{2fC_1 V_I} = \frac{M_S}{2} \frac{1}{fC_1 R} \quad (2.236)$$

Considering the Equation (2.211):

$$\Delta i_{LO} = \frac{1}{2} \frac{T}{2} \frac{k}{2CL_O} TI_O = \frac{k}{8f^2 CL_O} I_O$$

The variation ratio of current i_{LO} is

$$\xi = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{k}{16} \frac{1}{f^2 CL_O} \quad (2.237)$$

Considering Equation (2.213):

$$\Delta v_{CO} = \frac{B}{C_O} = \frac{1}{2} \frac{T}{2} \frac{k}{16f^2 CC_O L_O} I_O = \frac{k}{64f^3 CC_O L_O} I_O$$

The variation ratio of current v_{CO} is

$$\varepsilon = \frac{\Delta v_{CO} / 2}{V_{CO}} = \frac{k}{128 f^3 C C_O L_O} \frac{I_O}{V_O} = \frac{k}{128 f^3 C C_O L_O R} \quad (2.238)$$

Assuming that $f = 50$ kHz, $L = L_O = 100$ μ H, $C = C_O = 5$ μ F, $R = 10$ Ω and $k = 0.6$, we obtain

$$M_S = 2.5 \quad \zeta = 0.096 \quad \xi = 0.03 \quad \rho = 0.12 \quad \text{and} \quad \varepsilon = 0.0015$$

The output voltage V_O is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_O(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_O = V_O/R$.

2.4.2.4 Instantaneous Value of the Currents and Voltages

Referring to [Figure 2.39](#), the instantaneous values of the currents and voltages are listed below:

$$v_s = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O - V_I & \text{for } kT < t \leq T \end{cases} \quad (2.239)$$

$$v_D = \begin{cases} V_O & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.240)$$

$$v_{D1} = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O & \text{for } kT < t \leq T \end{cases} \quad (2.241)$$

$$v_L = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -(V_O - V_I) & \text{for } kT < t \leq T \end{cases} \quad (2.242)$$

$$i_I = i_S = \begin{cases} i_{L1}(0) + \delta(t) + \frac{V_I}{L} t & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.243)$$

$$i_L = \begin{cases} i_L(0) + \frac{V_I}{L} t & \text{for } 0 < t \leq kT \\ i_L(kT) - \frac{V_O - V_I}{L} (t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.244)$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{V_O - V_L}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.245)$$

$$i_{D1} = \begin{cases} \delta(t) & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.246)$$

$$i_{C1} = \begin{cases} \delta(t) & \text{for } 0 < t \leq kT \\ -i_L(kT) + \frac{V_O - V_L}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.247)$$

$$i_C \approx \begin{cases} -I_{C-on} & \text{for } 0 < t \leq kT \\ I_{C-off} & \text{for } kT < t \leq T \end{cases} \quad (2.248)$$

where

$$i_L(0) = k I_L - k V_L / 2 f L$$

$$i_L(kT) = k I_L + k V_L / 2 f L$$

Since the instantaneous current i_{LO} and voltage v_{CO} are partial parabolas with very small ripples, they can be treated as a DC current and voltage.

2.4.2.5 Discontinuous Mode

Referring to [Figure 2.37d](#), we can see that the diode current i_D becomes zero during switch off before next period switch on. The condition for discontinuous mode is

$$\zeta \geq 1$$

i.e.,

$$\frac{k}{M_s^2} \frac{R}{2fL} \geq 1$$

or

$$M_s \leq \sqrt{k} \sqrt{\frac{R}{2fL}} = \sqrt{k} \sqrt{\frac{z_N}{2}} \quad (2.249)$$

The graph of the boundary curve vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.40](#). It can be seen that the boundary curve has a minimum value of 1.5 at $k = 1/3$.

In this case the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_s]T$, where m_s is the **filling efficiency** and it is defined as:

$$m_s = \frac{1}{\zeta} = \frac{M_s^2}{k \frac{R}{2fL}} \quad (2.250)$$

Considering Equation (2.249), therefore $0 < m_s < 1$. Since the diode current i_D becomes 0 at $t = kT + (1 - k)m_sT$, for the current i_L

$$kTV_I = (1 - k)m_sT(V_C - V_I)$$

or

$$V_C = [1 + \frac{k}{(1 - k)m_s}]V_I = [1 + k^2(1 - k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1 - k}$$

and for the current i_{LO}

$$kT(V_I + V_C - V_O) = (1 - k)m_sT(V_O - V_I)$$

Therefore, output voltage in discontinuous mode is

$$V_O = [1 + \frac{k}{(1 - k)m_s}]V_I = [1 + k^2(1 - k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1 - k} \quad (2.251)$$

i.e., the output voltage will linearly increase during load resistance R increasing. The output voltage V_O vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.40](#). Larger load resistance R causes higher output voltage in discontinuous mode.

2.4.3 Re-Lift Circuit

Re-lift circuit, and its switch-on and -off equivalent circuits are shown in [Figure 2.41](#), which is derived from the self-lift circuit. It consists of one static switch S ; three inductors L , L_1 , and L_O ; four capacitors C , C_1 , C_2 , and C_O ; and diodes. From [Figure 2.33](#), [Figure 2.37](#), and [Figure 2.41](#), it can be seen that there are one capacitor C_2 , one inductor L_1 and two diodes D_2 , D_{11} added into the re-lift circuit. Circuit C_1 - D_1 - D_{11} - L_1 - C D_2 is the lift circuit. Capacitors C_1 and C_2 perform characteristics to lift the capacitor voltage V_C by twice

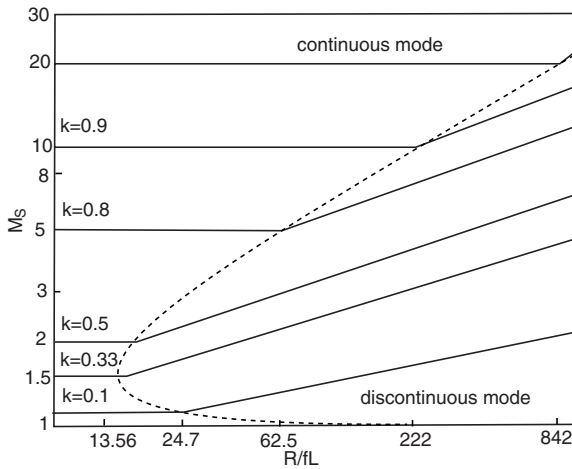


FIGURE 2.40

The boundary between continuous and discontinuous modes and output voltage vs. the normalized load $z_N = R/fL$ (self-lift circuit).

that of source voltage $2V_I$. Inductor L_1 performs the function as a ladder joint to link the two capacitors C_1 and C_2 and lift the capacitor voltage V_C up. Currents $i_{C1}(t)$ and $i_{C2}(t)$ are exponential functions $\delta_1(t)$ and $\delta_2(t)$. They have large values at the moment of power on, but they are small because $v_{C1} = v_{C2} \equiv V_I$ is in steady state.

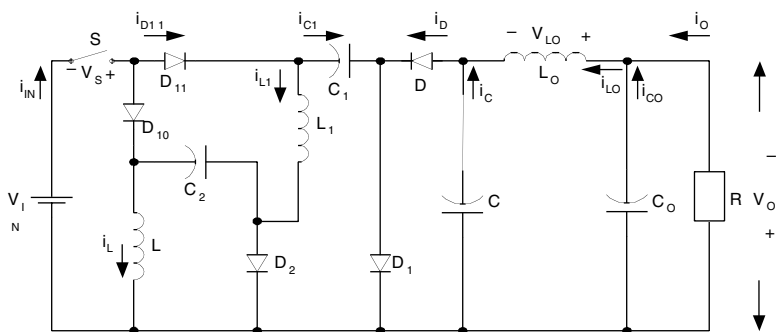
2.4.3.1 Circuit Description

When switch S is on, the equivalent circuit is shown in Figure 2.41b. In this case the source current $i_I = i_L + i_{C1} + i_{C2}$. Inductor L absorbs energy from the source, and current i_L linearly increases with slope V_I/L . In the mean time the diodes D_1, D_2 are conducted so that capacitors C_1 and C_2 are charged by the current i_{C1} and i_{C2} . Inductor L_O keeps the output current I_O continuous and transfers energy from capacitors C to the load R , i.e., $i_{C-on} = i_{LO}$. When switch S is off, the equivalent circuit is shown in Figure 2.41c. In this case the source current $i_I = 0$. Current i_L flows through the free-wheeling diode D , capacitors C_1 and C_2 , inductor L_1 to charge capacitor C and enhances current i_{LO} . Inductor L transfers its stored energy to capacitor C and load R via inductor L_O , i.e., $i_L = i_{C1-off} = i_{C2-off} = i_{L1-off} = i_{C-off} + i_{LO}$. Thus, current i_L decreases.

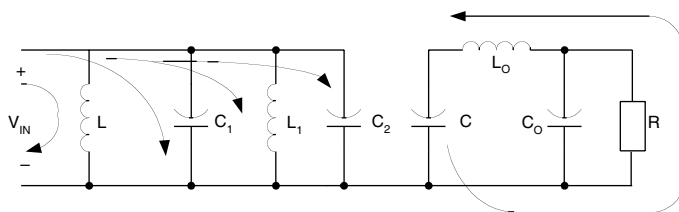
2.4.3.2 Average Voltages and Currents

The output current $I_O = I_{LO}$ because the capacitor C_O does not consume any energy in the steady state. The average output current:

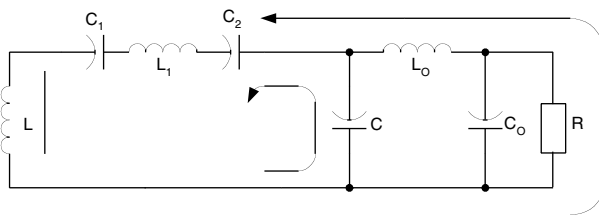
$$I_O = I_{LO} = I_{C-on} \quad (2.252)$$



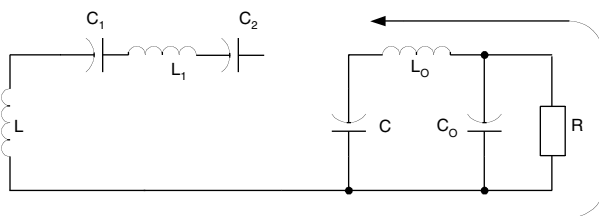
(a) circuit diagram



(b) switch on



(c) switch off



(d) discontinuous mode

FIGURE 2.41

Re-lift circuit: (a) circuit diagram; (b) switch on; (c) switch off; (d) discontinuous mode.

The charge of the capacitor C increases during switch-off:

$$Q_+ = (1 - k) T I_{C-off}$$

And it decreases during switch-on:

$$Q_- = k T I_{C-on}$$

In a whole repeating period T , $Q_+ = Q_-$. Thus,

$$I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k} I_O$$

Therefore, the inductor current I_L is

$$I_L = I_{C-off} + I_O = \frac{I_O}{1-k} \quad (2.253)$$

We know from [Figure 2.48b](#) that

$$I_{C1-off} = I_{C2-off} = I_{L1} = I_L = \frac{1}{1-k} I_O \quad (2.254)$$

and

$$I_{C1-on} = \frac{1-k}{k} I_{C1-off} = \frac{1}{k} I_O \quad (2.255)$$

and

$$I_{C2-on} = \frac{1-k}{k} I_{C2-off} = \frac{1}{k} I_O \quad (2.256)$$

In steady state we can use

$$V_{C1} = V_{C2} = V_I$$

and

$$V_{L1-on} = V_I \quad V_{L1-off} = \frac{k}{1-k} V_I$$

Investigate current i_L , it increases during switch-on with slope V_I/L and decreases during switch-off with slope $-(V_O - V_{C1} - V_{C2} - V_{L1-off})/L = -[V_O - 2V_I - k V_I/(1-k)]/L$. Therefore,

$$kTV_I = (1-k)T(V_O - 2V_I - \frac{k}{1-k} V_I)$$

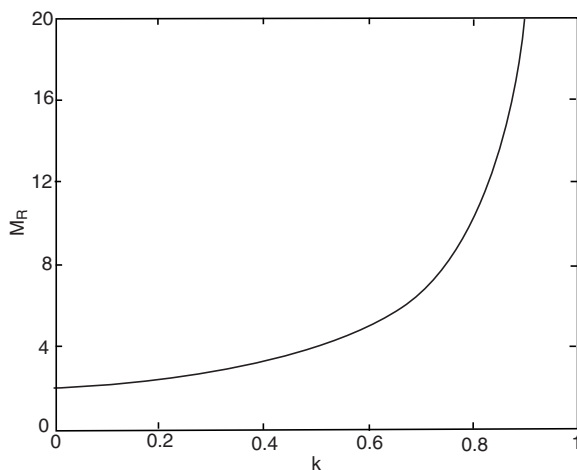


FIGURE 2.42

Voltage transfer gain M_R vs. k .

or

$$V_O = \frac{2}{1-k} V_I \quad (2.257)$$

and

$$I_O = \frac{1-k}{2} I_I \quad (2.258)$$

The voltage transfer gain in continuous mode is

$$M_R = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2}{1-k} \quad (2.259)$$

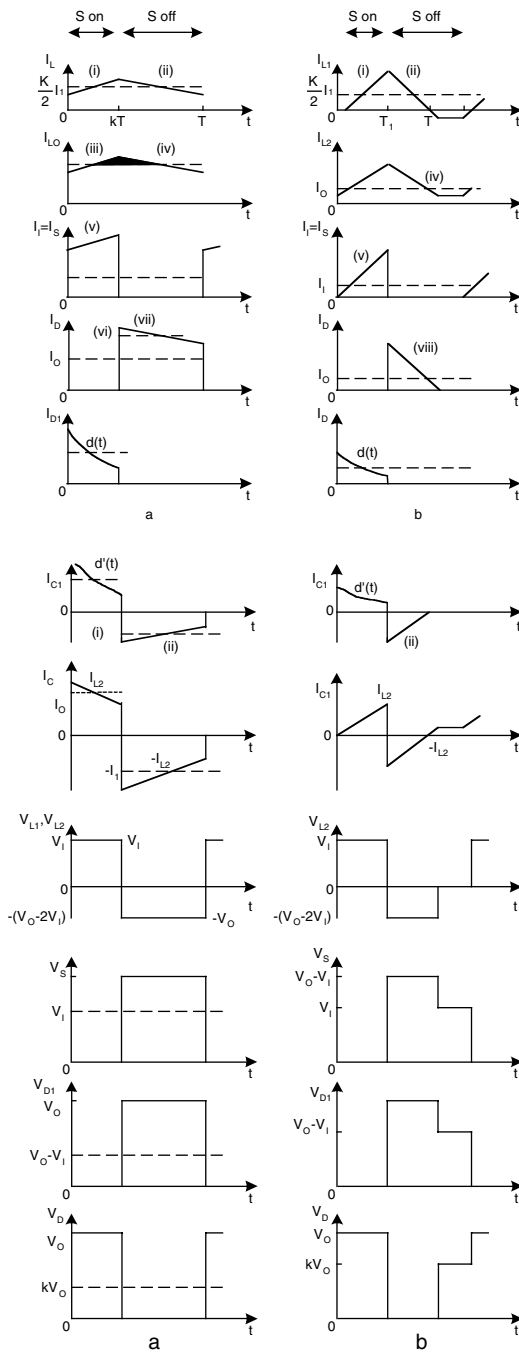
The curve of M_s vs. k is shown in [Figure 2.42](#).

Circuit (C - L_O - C_O) is a “Π” type low-pass filter. Therefore,

$$V_C = V_O = \frac{2}{1-k} V_I \quad (2.260)$$

2.4.3.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in [Figure 2.43](#).

**FIGURE 2.43**

Some voltage and current waveforms of re-lift circuit.

Current i_L increases and is supplied by V_I during switch-on. Thus, its peak-to-peak variation is

$$\Delta i_L = \frac{kTV_I}{L}$$

Considering Equation (2.253) and $R = V_O/I_O$, the variation ratio of the current i_L is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_IT}{2LI_O} = \frac{k(1-k)R}{2M_R fL} = \frac{k}{M_R^2} \frac{R}{fL} \quad (2.261)$$

The peak-to-peak variation of current i_{L1} is

$$\Delta i_{L1} = \frac{k}{L_1} TV_I$$

The variation ratio of current i_{L1} is

$$\chi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_I}{2L_1 I_O} (1-k) = \frac{k(1-k)}{2M_R} \frac{R}{fL_1} \quad (2.262)$$

The peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q-}{C} = \frac{k}{C} TI_O$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{kI_OT}{2CV_O} = \frac{k}{2} \frac{1}{fCR} \quad (2.263)$$

The peak-to-peak variation of voltage v_{C1} is

$$\Delta v_{C1} = \frac{kT}{C_1} I_{C1-on} = \frac{1}{fC} I_O$$

The variation ratio of voltage v_{C1} is

$$\sigma_1 = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{I_O}{2fC_1 V_I} = \frac{M_R}{2} \frac{1}{fC_1 R} \quad (2.264)$$

Take the same operation, variation ratio of voltage v_{C2} is

$$\sigma_2 = \frac{\Delta v_{C2} / 2}{V_{C2}} = \frac{I_O}{2fC_2V_I} = \frac{M_R}{2} \frac{1}{fC_2R} \quad (2.265)$$

Considering the Equation (2.211):

$$\Delta i_{LO} = \frac{1}{2} \frac{T}{2} \frac{k}{2CL_O} TI_O = \frac{k}{8f^2CL_O} I_O$$

The variation ratio of current i_{LO} is

$$\xi = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{k}{16} \frac{1}{f^2CL_O} \quad (2.266)$$

Considering the Equation (2.213):

$$\Delta v_{CO} = \frac{B}{C_O} = \frac{1}{2} \frac{T}{2} \frac{k}{16f^2CC_O L_O} I_O = \frac{k}{64f^3CC_O L_O} I_O$$

The variation ratio of current v_{CO} is

$$\varepsilon = \frac{\Delta v_{CO} / 2}{V_{CO}} = \frac{k}{128f^3CC_O L_O} \frac{I_O}{V_O} = \frac{k}{128} \frac{1}{f^3CC_O L_O R} \quad (2.267)$$

Assuming that $f = 50$ kHz, $L = L_O = 100$ μ H, $C = C_O = 5$ μ F, $R = 10$ Ω and $k = 0.6$, we obtain

$$M_R = 5 \quad \zeta = 0.048 \quad \xi = 0.03 \quad \rho = 0.12 \quad \text{and} \quad \varepsilon = 0.0015$$

The output voltage V_O is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_O(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_O = V_O/R$.

2.4.3.4 Instantaneous Value of the Currents and Voltages

Referring to [Figure 2.43](#), the instantaneous current and voltage values are listed below:

$$v_s = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O - (2 - \frac{k}{1-k})V_I & \text{for } kT < t \leq T \end{cases} \quad (2.268)$$

$$v_D = \begin{cases} V_O & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.269)$$

$$v_{D1} = v_{D2} = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ V_O & \text{for } kT < t \leq T \end{cases} \quad (2.270)$$

$$v_{L1} = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -\frac{k}{1-k} V_I & \text{for } kT < t \leq T \end{cases} \quad (2.271)$$

$$v_L = \begin{cases} V_I & \text{for } 0 < t \leq kT \\ -[V_O - (2 - \frac{k}{1-k})V_I] & \text{for } kT < t \leq T \end{cases} \quad (2.272)$$

$$i_l = i_s = \begin{cases} i_L(0) + \frac{V_I}{L}t + \delta_1(t) + \delta_2(t) + i_{L1}(0) + \frac{V_I}{L_1}t & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.273)$$

$$i_L = \begin{cases} i_L(0) + \frac{V_I}{L}t & \text{for } 0 < t \leq kT \\ i_L(kT) - \frac{V_O - (2 - \frac{k}{1-k})V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.274)$$

$$i_{L1} = \begin{cases} i_{L1}(0) + \frac{V_I}{L_1}t & \text{for } 0 < t \leq kT \\ i_{L1}(kT) - \frac{\frac{k}{1-k}V_I}{L_1}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.275)$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \leq kT \\ i_L(kT) - \frac{V_O - (2 - \frac{k}{1-k})V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.276)$$

$$i_{D1} = \begin{cases} \delta_1(t) & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.277)$$

$$i_{D2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \leq kT \\ 0 & \text{for } kT < t \leq T \end{cases} \quad (2.278)$$

$$i_{C1} = \begin{cases} \delta_1(t) & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) + \frac{V_O - (2 - \frac{k}{1-k})V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.279)$$

$$i_{C2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \leq kT \\ -i_{L1}(kT) + \frac{V_O - (2 - \frac{k}{1-k})V_I}{L}(t - kT) & \text{for } kT < t \leq T \end{cases} \quad (2.280)$$

$$i_C = \begin{cases} -I_{C-on} & \text{for } 0 < t \leq kT \\ I_{C-off} & \text{for } kT < t \leq T \end{cases} \quad (2.281)$$

where

$$i_L(0) = k I_I - k V_I / 2 f L$$

$$i_L(kT) = k I_I + k V_I / 2 f L$$

and

$$i_{L1}(0) = k I_I - k V_I / 2 f L_1$$

$$i_{L1}(kT) = k I_I + k V_I / 2 f L_1$$

Since the instantaneous currents i_{LO} and i_{CO} are partial parabolas with very small ripples. They are very nearly DC current.

2.4.3.5 Discontinuous Mode

Referring to [Figure 2.41d](#), we can see that the diode current i_D becomes zero during switch off before next period switch on. The condition for discontinuous mode is

$$\zeta \geq 1$$

i.e.,

$$\frac{k}{M_R^2} \frac{R}{fL} \geq 1$$

or

$$M_R \leq \sqrt{k} \sqrt{\frac{R}{fL}} = \sqrt{k} \sqrt{z_N} \quad (2.282)$$

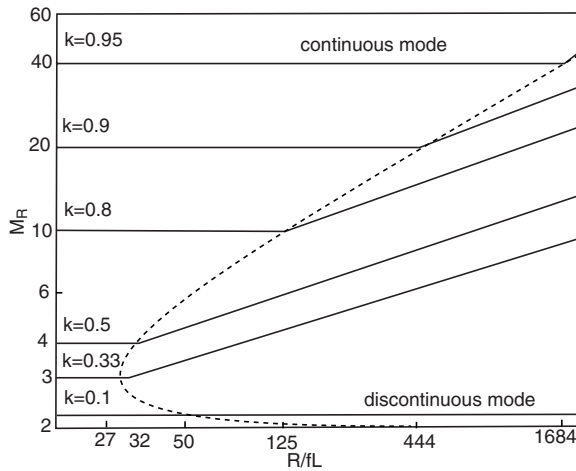


FIGURE 2.44

The boundary between continuous and discontinuous modes and output voltage vs. the normalized load $z_N = R/fL$ (re-lift circuit).

The graph of the boundary curve vs. the normalized load $z_N = R/fL$ is shown in Figure 2.44. It can be seen that the boundary curve has a minimum value of 3.0 at $k = 1/3$.

In this case the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_R]T$, where m_R is the **filling efficiency** and it is defined as:

$$m_R = \frac{1}{\zeta} = \frac{M_R^2}{k \frac{R}{fL}} \quad (2.283)$$

Considering Equation (2.282), therefore $0 < m_R < 1$. Because inductor current $i_{L1} = 0$ at $t = t_1$, so that

$$V_{L1-off} = \frac{k}{(1 - k)m_R} V_I$$

Since the current i_D becomes zero at $t = t_1 = [k + (1 - k)m_R]T$, for the current i_L

$$kTV_I = (1 - k)m_RT(V_C - 2V_I - V_{L1-off})$$

or

$$V_C = [2 + \frac{2k}{(1 - k)m_R}]V_I = [2 + k^2(1 - k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{fL}} \geq \frac{2}{1 - k}$$

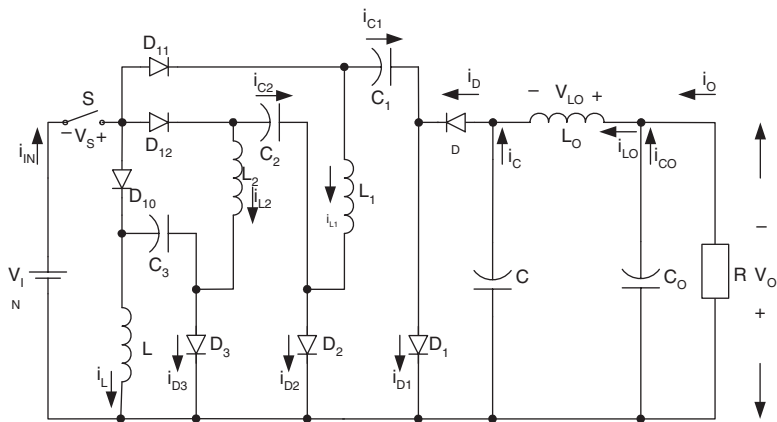


FIGURE 2.45
Triple-lift circuit.

and for the current i_{LO}

$$kT(V_I + V_C - V_O) = (1 - k)m_R T(V_O - 2V_I - V_{L1-off})$$

Therefore, output voltage in discontinuous mode is

$$V_O = [2 + \frac{2k}{(1-k)m_R}]V_I = [2 + k^2(1-k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{R}{fL}} \geq \frac{2}{1-k} \quad (2.284)$$

i.e., the output voltage will linearly increase during load resistance R increasing. The output voltage vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.44](#). Larger load resistance R may cause higher output voltage in discontinuous mode.

2.4.4 Multiple-Lift Circuits

Referring to [Figure 2.45](#), it is possible to build a multiple-lift circuit just only using the parts (L_1 - C_2 - D_2 - D_{11}) multiple times. For example, in [Figure 2.16](#) the parts (L_2 - C_3 - D_3 - D_{12}) were added in the triple-lift circuit. According to this principle, the triple-lift circuit and quadruple-lift circuit were built as shown in [Figure 2.45](#) and [Figure 2.48](#). In this book it is not necessary to introduce the particular analysis and calculations one by one to readers. However, their formulas are shown in this section.

2.4.4.1 Triple-Lift Circuit

Triple-lift circuit is shown in [Figure 2.45](#). It consists of one static switch S ; four inductors L , L_1 , L_2 , and L_O ; and five capacitors C , C_1 , C_2 , C_3 , and C_O ; and

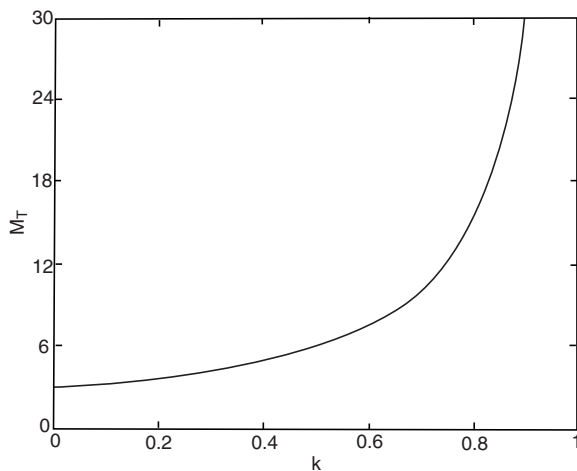


FIGURE 2.46

Voltage transfer gain of triple-lift circuit.

diodes. Circuit C_1 - D_1 - L_1 - C_2 - D_2 - D_{11} - L_2 - C_3 - D_3 - D_{12} is the lift circuit. Capacitors C_1 , C_2 , and C_3 perform characteristics to lift the capacitor voltage V_C by three times that of the source voltage V_I . L_1 and L_2 perform the function as ladder joints to link the three capacitors C_1 , C_2 , and C_3 and lift the capacitor voltage V_C up. Current $i_{C1}(t)$, $i_{C2}(t)$, and $i_{C3}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C1} = v_{C2} = v_{C3} \cong V_I$ in steady state.

The output voltage and current are

$$V_O = \frac{3}{1-k} V_I \quad (2.285)$$

and

$$I_O = \frac{1-k}{3} I_I \quad (2.286)$$

The voltage transfer gain in continuous mode is

$$M_T = V_O / V_I = \frac{3}{1-k} \quad (2.287)$$

The curve of M_T vs. k is shown in [Figure 2.46](#).

Other average voltages:

$$V_C = V_O \quad V_{C1} = V_{C2} = V_{C3} = V_I$$

Other average currents:

$$I_{LO} = I_O \quad I_L = I_{L1} = I_{L2} = \frac{1}{1-k} I_O$$

Current variation ratios:

$$\zeta = \frac{k}{M_T^2} \frac{3R}{2fL} \quad \xi = \frac{k}{16} \frac{1}{f^2 CL_O}$$

$$\chi_1 = \frac{k(1-k)}{2M_T} \frac{R}{fL_1} \quad \chi_2 = \frac{k(1-k)}{2M_T} \frac{R}{fL_2}$$

Voltage variation ratios:

$$\rho = \frac{k}{2} \frac{1}{fCR} \quad \sigma_1 = \frac{M_T}{2} \frac{1}{fC_1R}$$

$$\sigma_2 = \frac{M_T}{2} \frac{1}{fC_2R} \quad \sigma_3 = \frac{M_T}{2} \frac{1}{fC_3R}$$

The variation ratio of output voltage V_C is

$$\varepsilon = \frac{k}{128} \frac{1}{f^3 CC_O L_O R} \quad (2.288)$$

The output voltage ripple is very small. The boundary between continuous and discontinuous modes is

$$M_T \leq \sqrt{k} \sqrt{\frac{3R}{2fL}} = \sqrt{\frac{3kz_N}{2}} \quad (2.289)$$

It can be seen that the boundary curve has a minimum value of M_T that is equal to 4.5, corresponding to $k = 1/3$. The boundary curve vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.47](#).

In discontinuous mode the current i_D exists in the period between kT and $[k + (1-k)m_T]T$, where m_T is the filling efficiency that is

$$m_T = \frac{1}{\zeta} = \frac{M_T^2}{k \frac{3R}{2fL}} \quad (2.290)$$

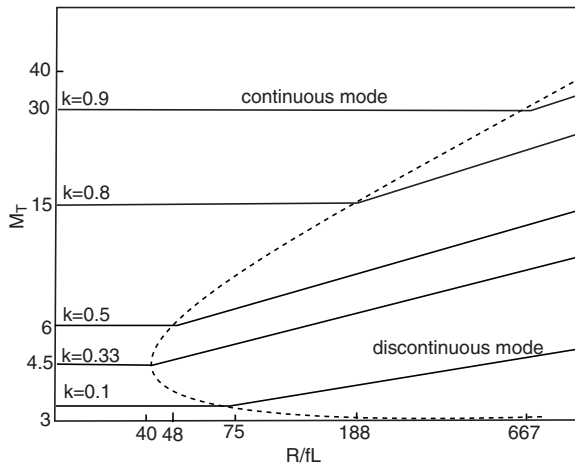


FIGURE 2.47

The boundary between continuous and discontinuous modes and output voltage vs. the normalized load $z_N = R/fL$ (triple-lift circuit).

Considering Equation (2.289), therefore $0 < m_T < 1$. Because inductor current $i_{L1} = i_{L2} = 0$ at $t = t_1$, so that

$$V_{L1-off} = V_{L2-off} = \frac{k}{(1-k)m_T} V_I$$

Since the current i_D becomes zero at $t = t_1 = [k + (1-k)m_T]T$, for the current i_L we have

$$kTV_I = (1-k)m_T T(V_C - 3V_I - V_{L1-off} - V_{L2-off})$$

or

$$V_C = \left[3 + \frac{3k}{(1-k)m_T}\right]V_I = \left[3 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k}$$

and for the current i_{LO} we have

$$kT(V_I + V_C - V_O) = (1-k)m_T T(V_O - 2V_I - V_{L1-off} - V_{L2-off})$$

Therefore, output voltage in discontinuous mode is

$$V_O = \left[3 + \frac{3k}{(1-k)m_T}\right]V_I = \left[3 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k} \quad (2.291)$$

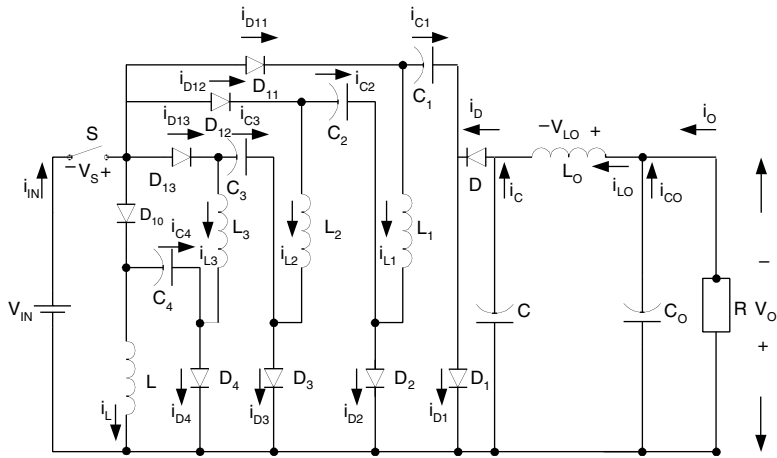


FIGURE 2.48
Quadruple-lift circuit.

i.e., the output voltage will linearly increase during load resistance R increasing. The output voltage vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.47](#). We can see that the output voltage will increase when the load resistance R increases.

2.4.4.2 Quadruple-Lift Circuit

Quadruple-lift circuit is shown in [Figure 2.48](#). It consists of one static switch S ; five inductors L , L_1 , L_2 , L_3 , and L_O ; and six capacitors C , C_1 , C_2 , C_3 , C_4 , and C_O . Capacitors C_1 , C_2 , C_3 , and C_4 perform characteristics to lift the capacitor voltage V_C by four times of source voltage V_I . L_1 , L_2 , and L_3 perform the function as ladder joints to link the four capacitors C_1 , C_2 , C_3 , and C_4 and lift the output capacitor voltage V_C up. Current $i_{C1}(t)$, $i_{C2}(t)$, $i_{C3}(t)$, and $i_{C4}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C1} = v_{C2} = v_{C3} = v_{C4} \cong V_I$ in steady state.

The output voltage and current are

$$V_O = \frac{4}{1-k} V_I \quad (2.292)$$

and

$$I_O = \frac{1-k}{4} I_I \quad (2.293)$$

The voltage transfer gain in continuous mode is

$$M_Q = V_O / V_I = \frac{4}{1-k} \quad (2.294)$$

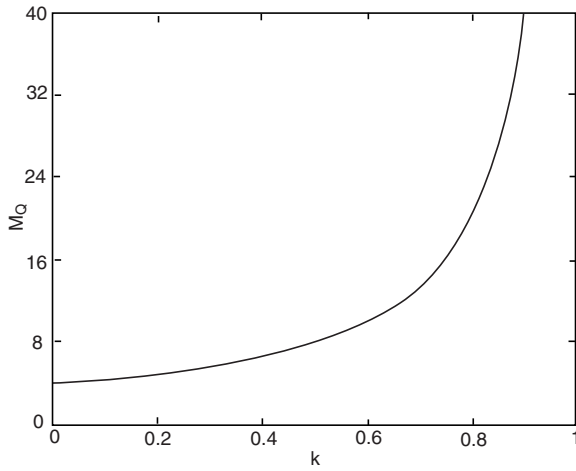


FIGURE 2.49

Voltage transfer gain of quadruple-lift circuit.

The curve of M_Q vs. k is shown in [Figure 2.49](#). Other average voltages:

$$V_C = V_O \quad V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_I$$

Other average currents:

$$I_{LO} = I_O \quad I_L = I_{L1} = I_{L2} = I_{L3} = \frac{1}{1-k} I_O$$

Current variation ratios:

$$\zeta = \frac{k}{M_Q^2} \frac{2R}{fL} \quad \xi = \frac{k}{16} \frac{1}{f^2 CL_O}$$

$$\chi_1 = \frac{k(1-k)}{2M_Q} \frac{R}{fL_1} \quad \chi_2 = \frac{k(1-k)}{2M_Q} \frac{R}{fL_2} \quad \chi_3 = \frac{k(1-k)}{2M_Q} \frac{R}{fL_3}$$

Voltage variation ratios:

$$\rho = \frac{k}{2} \frac{1}{fCR} \quad \sigma_1 = \frac{M_Q}{2} \frac{1}{fC_1R}$$

$$\sigma_2 = \frac{M_Q}{2} \frac{1}{fC_2R} \quad \sigma_3 = \frac{M_Q}{2} \frac{1}{fC_3R} \quad \sigma_4 = \frac{M_Q}{2} \frac{1}{fC_4R}$$

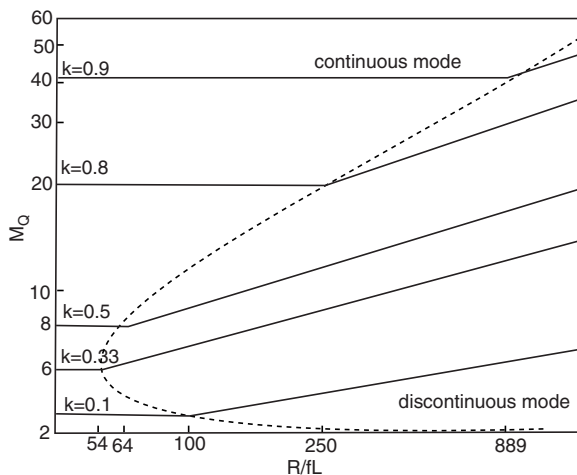


FIGURE 2.50

The boundary between continuous and discontinuous modes and output voltage vs. the normalized load $z_N = R/fL$ (quadruple-lift circuit).

The variation ratio of output voltage V_C is

$$\varepsilon = \frac{k}{128} \frac{1}{f^3 C C_O L_O R} \quad (2.295)$$

The output voltage ripple is very small. The boundary between continuous and discontinuous conduction modes is

$$M_Q \leq \sqrt{k} \sqrt{\frac{2R}{fL}} = \sqrt{2kz_N} \quad (2.296)$$

It can be seen that the boundary curve has a minimum value of M_Q that is equal to 6.0, corresponding to $k = 1/3$. The boundary curve is shown in [Figure 2.50](#).

In discontinuous mode the current i_d exists in the period between kT and $[k + (1 - k)m_Q]T$, where m_Q is the filling efficiency that is

$$m_Q = \frac{1}{\zeta} = \frac{M_Q^2}{k \frac{2R}{fL}} \quad (2.297)$$

Considering Equation (2.296), therefore $0 < m_Q < 1$. Because inductor current $i_{L1} = i_{L2} = i_{L3} = 0$ at $t = t_1$, so that

$$V_{L1-off} = V_{L2-off} = V_{L3-off} = \frac{k}{(1-k)m_Q} V_I$$

Since the current i_D becomes zero at $t = t_1 = kT + (1-k)m_Q T$, for the current i_L we have

$$kTV_I = (1-k)m_Q T(V_C - 4V_I - V_{L1-off} - V_{L2-off} - V_{L3-off})$$

or

$$V_C = [4 + \frac{4k}{(1-k)m_Q}]V_I = [4 + k^2(1-k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k}$$

and for current i_{LO} we have

$$kT(V_I + V_C - V_O) = (1-k)m_Q T(V_O - 2V_I - V_{L1-off} - V_{L2-off} - V_{L3-off})$$

Therefore, output voltage in discontinuous mode is

$$V_O = [4 + \frac{4k}{(1-k)m_Q}]V_I = [4 + k^2(1-k)\frac{R}{2fL}]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k} \quad (2.298)$$

i.e., the output voltage will linearly increase while load resistance R increases. The output voltage vs. the normalized load $z_N = R/fL$ is shown in [Figure 2.50](#). We can see that the output voltage will increase during load resistance while the load R increases.

2.4.5 Summary

From the analysis and calculation in previous sections, the common formulae can be obtained for all circuits:

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O} \quad z_N = \frac{R}{fL} \quad R = \frac{V_O}{I_O}$$

Current variation ratios:

$$\zeta = \frac{k(1-k)R}{2MfL} \quad \xi = \frac{k}{16f^2CL_O}$$

$$\chi_j = \frac{k(1-k)R}{2MfL_j} \quad (j = 1, 2, 3, \dots)$$

Voltage variation ratios:

$$\rho = \frac{k}{2fCR} \quad \varepsilon = \frac{k}{128f^3CC_O L_O R} \quad \sigma_j = \frac{M}{2fC_j R} \quad (j = 1, 2, 3, 4, \dots)$$

In order to write common formulas for the boundaries between continuous and discontinuous modes and output voltage for all circuits, the circuits can be numbered. The definition is that subscript 0 means the elementary circuit, subscript 1 means the self-lift circuit, subscript 2 means the re-lift circuit, subscript 3 means the triple-lift circuit, subscript 4 means the quadruple-lift circuit, and so on. Therefore, the voltage transfer gain in continuous mode for all circuits is

$$M_j = \frac{k^{h(j)}[j + h(j)]}{1 - k} \quad j = 0, 1, 2, 3, 4, \dots \quad (2.299)$$

The variation of the free-wheeling diode current i_D is

$$\zeta_j = \frac{k^{[1+h(j)]}}{M_j^2} \frac{j + h(j)}{2} z_N \quad (2.300)$$

The boundaries are determined by the condition:

$$\zeta_j \geq 1$$

or

$$\frac{k^{[1+h(j)]}}{M_j^2} \frac{j + h(j)}{2} z_N \geq 1 \quad j = 0, 1, 2, 3, 4, \dots \quad (2.301)$$

Therefore, the boundaries between continuous and discontinuous modes for all circuits are

$$M_j = k^{\frac{1+h(j)}{2}} \sqrt{\frac{j + h(j)}{2} z_N} \quad j = 0, 1, 2, 3, 4, \dots \quad (2.302)$$

The filling efficiency is

$$m_j = \frac{1}{\zeta_j} = \frac{M_j^2}{k^{[1+h(j)]}} \frac{2}{j + h(j)} \frac{1}{z_N} \quad (2.303)$$

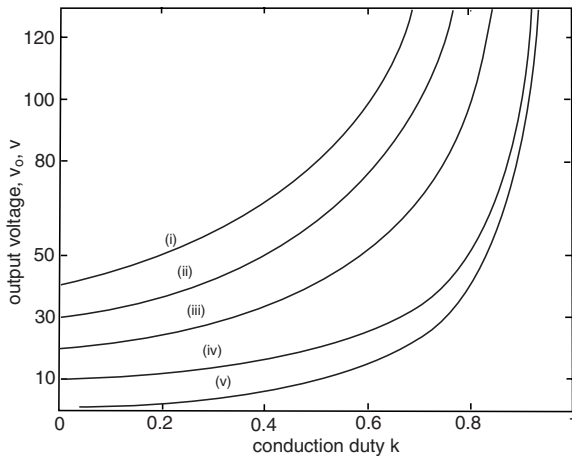


FIGURE 2.51

Output voltages of all negative output Luo-converters ($V_I = 10$ V).

The voltage across the capacitor C in discontinuous mode for all circuits

$$V_{C-j} = [j + k^{[2-h(j)]} \frac{1-k}{2} z_N] V_I \quad j = 0, 1, 2, 3, 4, \dots \quad (2.304)$$

The output voltage in discontinuous mode for all circuits

$$V_{O-j} = [j + k^{[2-h(j)]} \frac{1-k}{2} z_N] V_I \quad j = 0, 1, 2, 3, 4, \dots \quad (2.305)$$

where

$$h(j) = \begin{cases} 0 & \text{if } j \geq 1 \\ 1 & \text{if } j = 0 \end{cases} \quad \text{is the Hong Function}$$

The voltage transfer gains in continuous mode for all circuits are shown in [Figure 2.51](#). The boundaries between continuous and discontinuous modes of all circuits are shown in [Figure 2.52](#). The curves of all M vs. z_N state that the continuous mode area increases from M_E via M_S , M_R , M_T to M_Q . The boundary of elementary circuit is a monorising curve, but other curves are not monorising. There are minimum values of the boundaries of other curves, which of M_S , M_R , M_T and M_Q correspond at $k = 1/3$.

Assuming that $f = 50$ kHz, $L = L_O = L_1 = L_2 = L_3 = L_4 = 100$ μ H, $C = C_1 = C_2 = C_3 = C_4 = C_O = 5$ μ F and the source voltage $V_I = 10$ V, the value of the output voltage V_O in various conduction duty k are shown in [Figure 2.22](#). Typically, some values of the output voltage V_O in conduction duty $k = 0.33$,

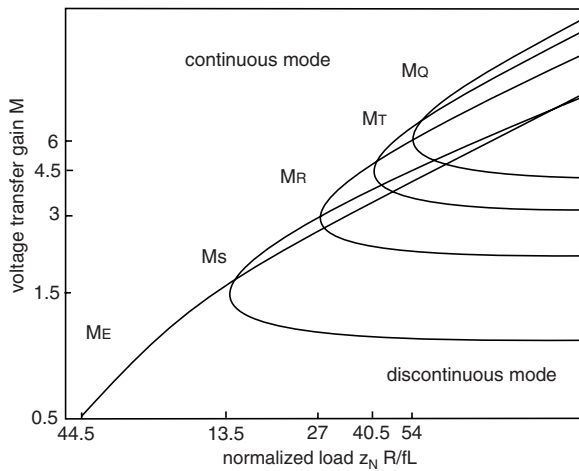


FIGURE 2.52

Boundaries between continuous and discontinuous modes of all negative output Luo-converters.

TABLE 2.2

Comparison among Five Negative Output Luo-Converters

Negative Output Luo-Converters	I_O	V_O	V_O ($V_I = 10$ V)			
			$k = 0.33$	$k = 0.5$	$k = 0.75$	$k = 0.9$
Elementary Circuit	$I_O = \frac{1-k}{k} I_I$	$V_O = \frac{k}{1-k} V_I$	5 V	10 V	30 V	90 V
Self-Lift Circuit	$I_O = (1-k) I_I$	$V_O = \frac{1}{1-k} V_I$	15 V	20 V	40 V	100 V
Re-Lift Circuit	$I_O = \frac{1-k}{2} I_I$	$V_O = \frac{2}{1-k} V_I$	30 V	40 V	80 V	200 V
Triple-Lift Circuit	$I_O = \frac{1-k}{3} I_I$	$V_O = \frac{3}{1-k} V_I$	45 V	60 V	120 V	300 V
Quadruple-Lift Circuit	$I_O = \frac{1-k}{4} I_I$	$V_O = \frac{4}{1-k} V_I$	60 V	80 V	160 V	400 V

0.5, 0.75, and 0.9 are listed in Table 2.2. The ripple of the output voltage is very small, say smaller than 1%. For example, using the above data and $R = 10 \Omega$, the variation ratio of the output voltage is $\epsilon = 0.0025 \times k = 0.0008$, 0.0012, 0.0019, and 0.0023 respectively. From these data the fact we find is that the output voltage of all negative output Luo-converters is almost a real DC voltage with very small ripple.

2.5 Modified Positive Output Luo-Converters

Negative output Luo-converters perform the voltage conversion from positive to negative voltages using VL technique with only one switch S . This section introduces the technique to modify positive output Luo-converters that can employ only **one** switch for all circuits. Five circuits have been introduced in the literature. They are

- Elementary circuit
- Self-lift circuit
- Re-lift circuit
- Triple-lift circuit
- Quadruple-lift circuit

There are five circuits introduced in this section, namely the elementary circuit, self-lift circuit, re-lift circuit, and multiple-lift circuit (triple-lift and quadruple-lift circuits). In all circuits the switch S is a PMOS. It is driven by a PWM switch signal with variable frequency f and conduction duty k . For all circuits, the load is usually resistive, $R = V_O/I_O$. We concentrate the absolute values rather than polarity in the following descriptions and calculations. The directions of all voltages and currents are defined and shown in the figures. We will assume that all the components are ideal and the capacitors are large enough. We also assume that the circuits operate in continuous conduction mode. The output voltage and current are V_O and I_O ; the input voltage and current are V_I and I_I .

2.5.1 Elementary Circuit

Elementary circuit is shown in [Figure 2.10](#). It is the elementary circuit of positive output Luo-converters. The output voltage and current and the voltage transfer gain are

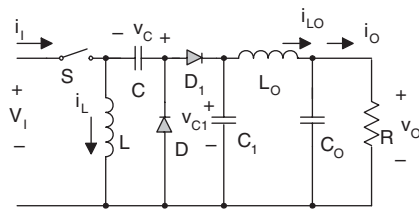
$$V_O = \frac{k}{1-k} V_I$$

$$I_O = \frac{1-k}{k} I_I$$

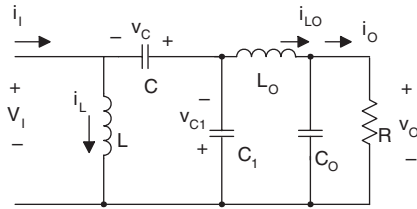
$$M_E = \frac{k}{1-k}$$

Average voltage:

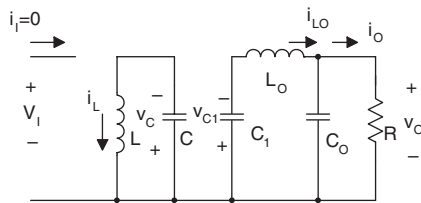
$$V_C = V_O$$



(a) Self-lift circuit



(b) Switch-on equivalent circuit



(c) Switch-off equivalent circuit

FIGURE 2.53

Modified self-lift circuit and its equivalent circuit. (a) Self-lift circuit. (b) Switch-on equivalent circuit. (c) Switch-off equivalent circuit.

Average currents:

$$I_{L0} = I_O \quad I_L = \frac{k}{1-k} I_O$$

2.5.2 Self-Lift Circuit

Self-lift circuit is shown in [Figure 2.53](#). It is derived from the elementary circuit. In steady state, the average inductor voltages over a period are zero. Thus

$$V_{C1} = V_{C0} = V_O \quad (2.306)$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_I and $-V_C$.

Therefore

$$kTV_I = (1-k)TV_C$$

Hence,

$$V_C = \frac{k}{1-k} V_I \quad (2.307)$$

During switch-on period, the voltage across capacitor C_1 are equal to the source voltage plus the voltage across C . Since we assume that C and C_1 are sufficiently large,

$$V_{C1} = V_I + V_C$$

Therefore,

$$V_{C1} = V_I + \frac{k}{1-k} V_I = \frac{1}{1-k} V_I$$

$$V_O = V_{CO} = V_{C1} = \frac{1}{1-k} V_I$$

The voltage transfer gain of continuous conduction mode (CCM) is

$$M = \frac{V_O}{V_I} = \frac{1}{1-k}$$

The output voltage and current and the voltage transfer gain are

$$V_O = \frac{1}{1-k} V_I$$

$$I_O = (1-k)I_I$$

$$M_S = \frac{1}{1-k} \quad (2.308)$$

Average voltages:

$$V_C = kV_O$$

$$V_{C1} = V_O$$

Average currents:

$$I_{LO} = I_O$$

$$I_L = \frac{1}{1-k} I_O$$

We also implement the breadboard prototype of the proposed self-lift circuit. NMOS IRFP460 is used as the semiconductor switch. The diode is MR824. The other parameters are

$$V_I = 0 \sim 30 \text{ V}, R = 30 \sim 340 \text{ } \Omega, k = 0.1 \sim 0.9$$

$$C = C_O = 100 \text{ } \mu\text{F} \text{ and } L = 470 \text{ } \mu\text{H}$$

2.5.3 Re-Lift Circuit

Re-lift circuit and its equivalent circuits are shown in [Figure 2.54](#). It is derived from the self-lift circuit. The function of capacitors C_2 is to lift the voltage v_C by source voltage V_I , the function of inductor L_1 acts like a hinge of the foldable ladder (capacitor C_2) to lift the voltage v_C during switch off.

In steady state, the average inductor voltages over a period are zero. Thus

$$V_{C1} = V_{CO} = V_O$$

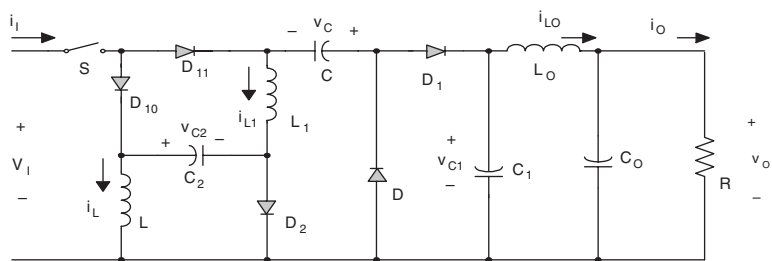
Since we assume C_2 is large enough and C_2 is biased by the source voltage V_I during switch-on period, thus $V_{C2} = V_I$

From the switch-on equivalent circuit, another capacitor voltage equation can also be derived since we assume all the capacitors to be large enough,

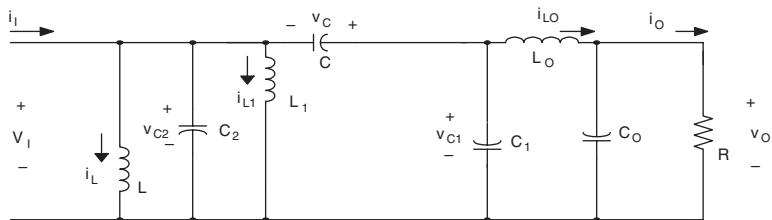
$$V_O = V_{C1} = V_C + V_I$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_I and $-V_{L-OFF}$. Therefore

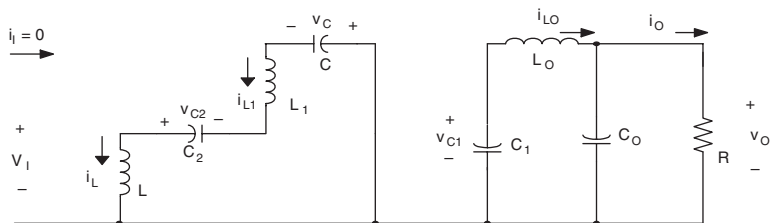
$$kTV_I = (1-k)TV_{L-OFF}$$



(a) Re-lift circuit



(b) Switch-on equivalent circuit



(c) Switch-off equivalent circuit

FIGURE 2.54

Modified re-lift circuit. (a) Re-lift circuit. (b) Switch-on equivalent circuit. (c) Switch-off equivalent circuit.

Hence,

$$V_{L-OFF} = \frac{k}{1-k} V_I$$

The inductor current i_{L1} increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L_1 are V_I and $-V_{L1-OFF}$.

Therefore

$$kTV_I = (1-k)TV_{L1-OFF}$$

Hence,

$$V_{L1-OFF} = \frac{k}{1-k} V_I$$

From the switch-off period equivalent circuit,

$$V_C = V_{C-OFF} = V_{L-OFF} + V_{L1-OFF} + V_{C2}$$

Therefore,

$$V_C = \frac{k}{1-k} V_I + \frac{k}{1-k} V_I + V_I = \frac{1+k}{1-k} V_I \quad (2.309)$$

$$V_O = \frac{1+k}{1-k} V_I + V_I = \frac{2}{1-k} V_I$$

Then we get the voltage transfer ratio in CCM,

$$M = M_R = \frac{2}{1-k} \quad (2.310)$$

The following is a brief summary of the main equations for the re-lift circuit. The output voltage and current and gain are

$$V_O = \frac{2}{1-k} V_I$$

$$I_O = \frac{1-k}{2} I_I$$

$$M_R = \frac{2}{1-k}$$

Average voltages:

$$V_C = \frac{1+k}{1-k} V_I$$

$$V_{C1} = V_{C0} = V_O$$

$$V_{C2} = V_I$$

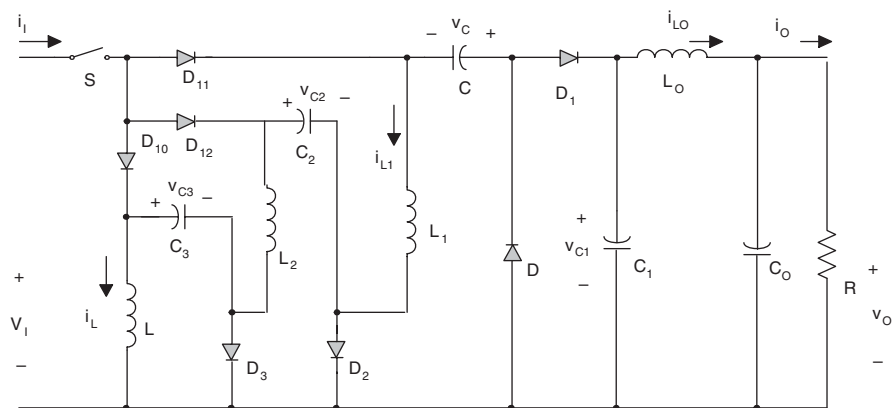


FIGURE 2.55

Modified triple-lift circuit.

Average currents:

$$I_{LO} = I_O$$

$$I_L = I_{L1} = \frac{1}{1-k} I_O$$

2.5.4 Multi-Lift Circuit

Multiple-lift circuits are derived from re-lift circuits by repeating the section of L_1 - C_1 - D_1 multiple times. For example, triple-list circuit is shown in Figure 2.55. The function of capacitors C_2 and C_3 is to lift the voltage v_C across capacitor C by twice the source voltage $2V_I$, the function of inductors L_1 and L_2 acts like hinges of the foldable ladder (capacitors C_2 and C_3) to lift the voltage v_C during switch off.

The output voltage and current and voltage transfer gain are

$$V_O = \frac{3}{1-k} V_I$$

and

$$I_O = \frac{1-k}{3} I_I$$

$$M_T = \frac{3}{1-k} \quad (2.311)$$

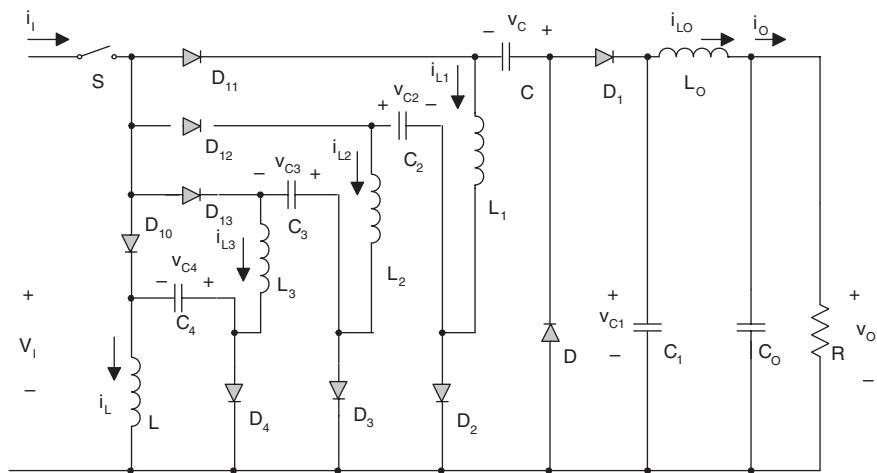


FIGURE 2.56
Modified quadruple-lift circuit.

Other average voltages:

$$V_C = \frac{2+k}{1-k} V_I$$

and

$$V_{C1} = V_O \quad V_{C2} = V_{C3} = V_I$$

Other average currents:

$$I_{L_O} = I_O$$

$$I_{L1} = I_{L2} = I_L = \frac{1}{1-k} I_O$$

The quadruple-lift circuit is shown in [Figure 2.56](#). The function of capacitors C_2 , C_3 , and C_4 is to lift the voltage v_C across capacitor C by three times the source voltage $3V_I$. The function of inductors L_1 , L_2 , and L_3 acts like hinges of the foldable ladder (capacitors C_2 , C_3 , and C_4) to lift the voltage v_C during switch off. The output voltage and current and voltage transfer gain are

$$V_O = \frac{4}{1-k} V_I$$

and

$$I_O = \frac{1-k}{4} I_I$$

$$M_Q = \frac{4}{1-k} \quad (2.312)$$

Average voltages:

$$V_C = \frac{3+k}{1-k} V_I$$

and

$$V_{C1} = V_O$$

$$V_{C2} = V_{C3} = V_{C4} = V_I$$

Average currents:

$$I_{LO} = I_O$$

and

$$I_L = \frac{k}{1-k} I_O$$

$$I_{L1} = I_{L2} = I_{L3} + I_L + I_{LO} = \frac{1}{1-k} I_O$$

2.5.5 Application

A high-efficiency, widely adjustable high voltage regulated power supply (HVRPS) is designed to use these Luo-converters in a high voltage test rig. The proposed HVRPS is shown in [Figure 2.57](#). The HVRPS was constructed by using a PWM IC TL494 to implement closed-loop control together with the modified positive output Luo-converters. Its output voltage is basically a DC value with small ripple and can be widely adjustable. The source voltage is 24 V DC and the output voltage can vary from 36 V to 1000 V DC. The measured experimental results show that the efficiency can be as high as 95% and the source effect ratio is about 0.001 and load effect ratio is about 0.005.

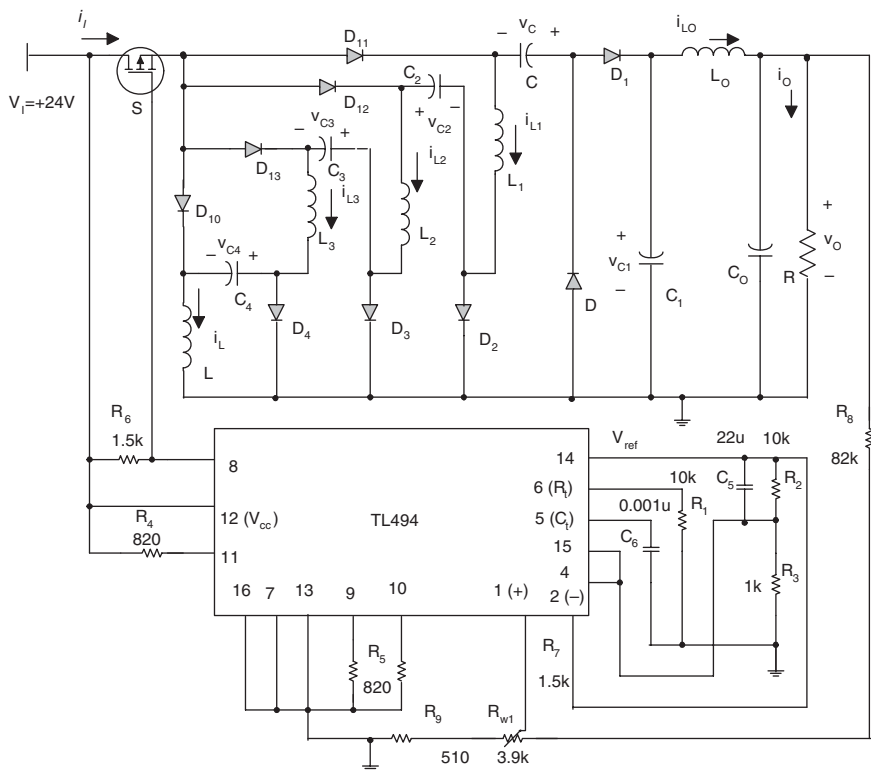


FIGURE 2.57

A high voltage testing power supply.

2.6 Double Output Luo-Converters

Mirror-symmetrical double output voltages are specially required in industrial applications and computer periphery circuits. Double output DC-DC Luo-converters can convert the positive input source voltage to positive and negative output voltages. It consists of two conversion paths. Double output Luo-converters perform from positive to positive and negative DC-DC voltage increasing conversion with high power density, high efficiency, and cheap topology in simple structure.

Double output DC-DC Luo-converters consist of two conversion paths. Usually, mirror-symmetrical double output voltages are required in industrial applications and computer periphery circuits such as operational amplifiers, computer periphery power supplies, differential servo-motor drives, and some symmetrical voltage medical equipment. In recent years the DC-DC conversion technique has been greatly developed. The main objective is

to reach a high efficiency, high power density and cheap topology in simple structure.

The elementary circuit can perform step-down and step-up DC-DC conversion. The other double output Luo-converters are derived from this elementary circuit, they are the self-lift circuit, re-lift circuit, and multiple-lift circuits (e.g., triple-lift and quadruple-lift circuits). Switch S in these circuits is a PMOS. It is driven by a PWM switch signal with repeating frequency f and conduction duty k . In this paper the switch repeating period is $T = 1/f$, so that the switch-on period is kT and switch-off period is $(1 - k)T$. For all circuits, the loads are usually resistive, i.e., $R = V_{O+}/I_{O+}$ and $R_1 = V_{O-}/I_{O-}$; the normalized loads are $z_{N+} = R/fL$ (where $L = L_1$ and $L = L_1L_2/L_1 + L_2$ for elementary circuits) and $z_{N-} = R_1/fL_{11}$. In order to keep the positive and negative output voltages to be symmetrically equal to each other, usually, we purposely select that $L = L_{11}$ and $z_{N+} = z_{N-}$.

Each converter has two conversion paths. The positive path consists of a positive pump circuit S - L_1 - D_0 - C_1 and a “ Π ”-type filter (C_2)- L_2 - C_O , and a lift circuit (except elementary circuits). The pump inductor L_1 absorbs energy from source during switch-on and transfers the stored energy to capacitor C_1 during switch-off. The energy on capacitor C_1 is then delivered to load R during switch-on. Therefore, a high voltage V_{C1} will correspondingly cause a high output voltage V_{O+} .

The negative path consists of a negative pump circuit S - L_{11} - D_{10} -(C_{11}) and a “ Π ”-type filter C_{11} - L_{12} - C_{10} , and a lift circuit (except elementary circuits). The pump inductor L_{11} absorbs the energy from source during switch-on and transfers the stored energy to capacitor C_{11} during switch-off. The energy on capacitor C_{11} is then delivered to load R_1 during switch-on. Hence, a high voltage V_{C11} will correspondingly cause a high output voltage V_{O-} .

When switch S is turned off, the currents flowing though the freewheeling diodes D_0 and D_{10} are existing. If the currents i_{D0} and i_{D10} do not fall to zero before switch S is turned on again, we define this working state to be continuous conduction mode. If the currents i_{D0} and i_{D10} become zero before switch S is turned on again, we define that working state to be discontinuous conduction mode.

The output voltages and currents are V_{O+} , V_{O-} and I_{O+} , I_{O-} ; the input voltage and current are V_I and $I_I = I_{I+} + I_{I-}$. Assuming that the power loss can be ignored, $P_I = P_O$, or $V_I I_I = V_{O+} I_{O+} + V_{O-} I_{O-}$. For general description, we have the following definitions in continuous mode: The voltage transfer gain in the continuous mode:

$$M_+ = \frac{V_{O+}}{V_I} \quad \text{and} \quad M_- = \frac{V_{O-}}{V_I}$$

Variation ratio of the diode's currents:

$$\zeta_+ = \frac{\Delta i_{D0} / 2}{I_{D0}} \quad \text{and} \quad \zeta_- = \frac{\Delta i_{D10} / 2}{I_{L11}}$$

Variation ratio of pump inductor's currents:

$$\xi_{1+} = \frac{\Delta i_{L1} / 2}{I_{L1}} \quad \text{and} \quad \xi_- = \frac{\Delta i_{L11} / 2}{I_{L11}}$$

Variation ratio of filter inductor's currents:

$$\xi_{2+} = \frac{\Delta i_{L2} / 2}{I_{L2}} \quad \text{and} \quad \xi_- = \frac{\Delta i_{L12} / 2}{I_{L12}}$$

Variation ratio of lift inductor's currents:

$$\chi_{j+} = \frac{\Delta i_{L2+j} / 2}{I_{L2+j}} \quad \text{and} \quad \chi_{j-} = \frac{\Delta i_{L12+j} / 2}{I_{L12+j}} \quad j = 1, 2, 3, \dots$$

Variation ratio of pump capacitor's voltages:

$$\rho_+ = \frac{\Delta v_{C1} / 2}{V_{C1}} \quad \text{and} \quad \rho_- = \frac{\Delta v_{C11} / 2}{V_{C11}}$$

Variation ratio of lift capacitor's voltages:

$$\sigma_{j+} = \frac{\Delta v_{C1+j} / 2}{V_{C1+j}} \quad \text{and} \quad \sigma_{j-} = \frac{\Delta v_{C11+j} / 2}{V_{C11+j}} \quad j = 1, 2, 3, 4, \dots$$

Variation ratio of output voltages:

$$\varepsilon_+ = \frac{\Delta v_{O+} / 2}{V_{O+}} \quad \text{and} \quad \varepsilon_- = \frac{\Delta v_{O-} / 2}{V_{O-}}$$

2.6.1 Elementary Circuit

The elementary circuit is shown in [Figure 2.58](#). Since the positive Luo-converters and negative Luo-converters have been published, this section can be simplified.

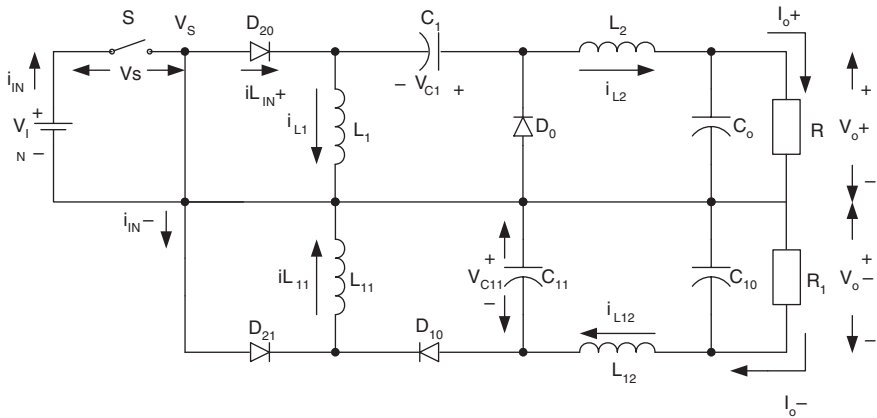


FIGURE 2.58
Elementary circuit.

2.6.1.1 Positive Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.59a, and the equivalent circuit during switch-off in Figure 2.59b. The relations of the average currents and voltages are

$$I_{L2} = \frac{1-k}{k} I_{L1} \quad \text{and} \quad I_{L2} = I_{O+}$$

Positive path input current is

$$I_{I+} = k \times i_{I+} = k(i_{L1} + i_{L2}) = k\left(1 + \frac{1-k}{k}\right) I_{L1} = I_{L1} \quad (2.313)$$

The output current and voltage are

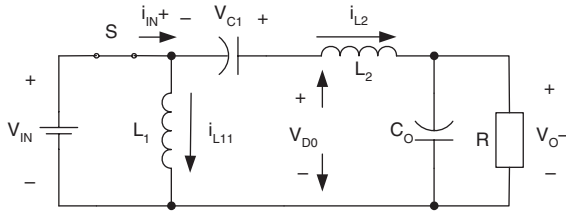
$$I_{O+} = \frac{1-k}{k} I_{I+} \quad \text{and} \quad V_{O+} = \frac{k}{1-k} V_I$$

The voltage transfer gain in continuous mode is

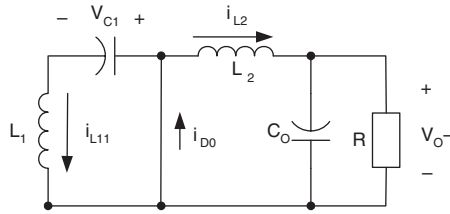
$$M_{E+} = \frac{V_{O+}}{V_I} = \frac{k}{1-k} \quad (2.314)$$

The average voltage across capacitor C_1 is

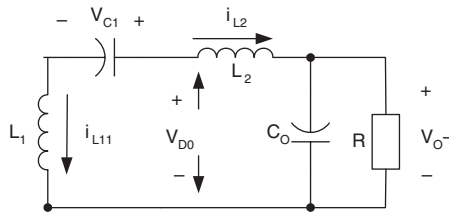
$$V_{C1} = \frac{k}{1-k} V_I = V_{O+}$$



(a) switch on



(b) switch off



(c) discontinuous mode

FIGURE 2.59

Equivalent circuits of elementary circuit positive path: (a) switch on; (b) switch off; (c) discontinuous conduction mode.

The variation ratios of the parameters are

$$\xi_{1+} = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_L}{2L_1 I_{L1}} = \frac{1-k}{2M_E} \frac{R}{fL_1} \quad \text{and} \quad \xi_{2+} = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{kTV_L}{2L_2 I_{L2}} = \frac{k}{2M_E} \frac{R}{fL_2}$$

The variation ratio of current i_{D0} is

$$\zeta_+ = \frac{\Delta i_{D0} / 2}{I_{D0}} = \frac{(1-k)^2 TV_{O+}}{2LI_{O+}} = \frac{k(1-k)R}{2M_E fL} = \frac{k^2}{M_E^2} \frac{R}{2fL} \quad (2.315)$$

The variation ratio of v_{C1} is

$$\rho_+ = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{(1-k)TI_{I+}}{2C_1V_{O+}} = \frac{k}{2} \frac{1}{fC_1R}$$

The variation ratio of output voltage v_{O+} is

$$\varepsilon_+ = \frac{\Delta v_{O+} / 2}{V_{O+}} = \frac{kT^2}{8C_OL_2} \frac{V_I}{V_{O+}} = \frac{k}{8M_E} \frac{1}{f^2C_OL_2} \quad (2.316)$$

If $L_1 = L_2 = 1$ mH, $C_1 = C_0 = 20$ μ F, $R = 10$ Ω , $f = 50$ kHz and $k = 0.5$, we get $\xi_{1+} = 0.05$, $\xi_{2+} = 0.05$, $\zeta_+ = 0.05$, $\rho_+ = 0.025$, and $\varepsilon = 0.00125$. Therefore, the variations of i_{L1} , i_{L2} and v_{C1} are small. The output voltage V_{O+} is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_{O+}(t)$ is almost a real DC waveform with very small ripple as well, and is equal to $I_{O+} = V_{O+}/R$.

2.6.1.2 Negative Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.60(a) the equivalent circuit during switch-off is shown in Figure 2.60(b). The relations of the average currents and voltages are

$$I_{O-} = I_{L12} \quad \text{and} \quad I_{O-} = I_{L12} = I_{C11-on}$$

Since

$$I_{C11-off} = \frac{k}{1-k} I_{C11-on} = \frac{k}{1-k} I_{O-}$$

the inductor current I_{L11} is

$$I_{L11} = I_{C11-off} + I_{O-} = \frac{I_{O-}}{1-k} \quad (2.317)$$

So that

$$I_{I-} = k \times i_{I-} = ki_{L11} = kI_{L11} = \frac{k}{1-k} I_{O-}$$

The output current and voltage are

$$I_{O-} = \frac{1-k}{k} I_{I-} \quad \text{and} \quad V_{O-} = \frac{k}{1-k} V_I$$

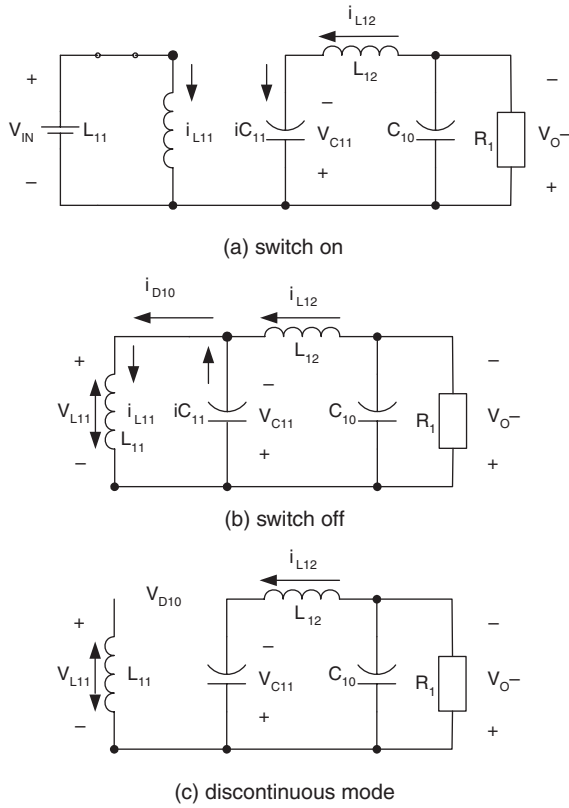


FIGURE 2.60

Equivalent circuits of elementary circuit negative path: (a) switch on; (b) switch off; (c) discontinuous conduction mode.

The voltage transfer gain in continuous mode is

$$M_{E-} = \frac{V_{O-}}{V_I} = \frac{k}{1-k} \quad (2.318)$$

and

$$V_{C11} = V_{O-} = \frac{k}{1-k} V_I$$

From Equations (2.314) and (2.318), we can define that $M_E = M_{E+} = M_{E-}$. The curve of M_E vs. k is shown in [Figure 2.61](#).

The variation ratios of the parameters are

$$\xi_- = \frac{\Delta i_{L12} / 2}{I_{L12}} = \frac{k}{16 f^2 C_{10} L_{12}} \quad \text{and} \quad \rho_- = \frac{\Delta v_{C11} / 2}{V_{C11}} = \frac{k I_{O-} T}{2 C_{11} V_{O-}} = \frac{k}{2 f C_{11} R_1}$$

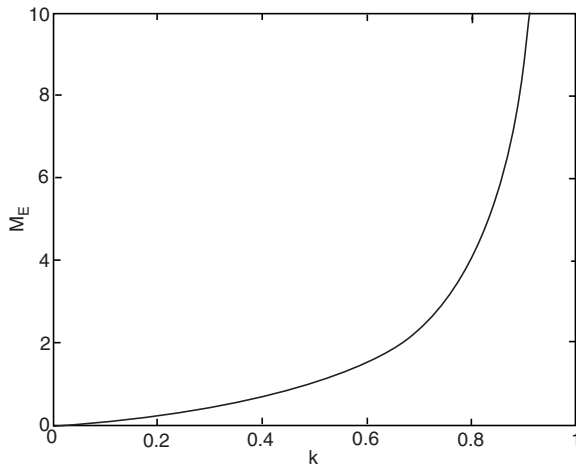


FIGURE 2.61

Voltage transfer gain M_E vs. k .

The variation ratio of current i_{L11} and i_{D10} is

$$\zeta_- = \frac{\Delta i_{L11} / 2}{I_{L11}} = \frac{k(1-k)V_I T}{2L_{11}I_{O-}} = \frac{k(1-k)R_1}{2M_E f L_{11}} = \frac{k^2}{M_E^2} \frac{R_1}{2f L_{11}} \quad (2.319)$$

The variation ratio of current v_{C10} is

$$\varepsilon_- = \frac{\Delta v_{C10} / 2}{V_{C10}} = \frac{k}{128 f^3 C_{11} C_{10} L_{12}} \frac{I_{O-}}{V_{O-}} = \frac{k}{128 f^3 C_{11} C_{10} L_{12} R_1} \quad (2.320)$$

Assuming that $f = 50$ kHz, $L_{11} = L_{12} = 0.5$ mH, $C = C_O = 20$ μ F, $R_1 = 10$ Ω and $k = 0.5$, obtained $M_E = 1$, $\zeta = 0.05$, $\rho = 0.025$, $\xi = 0.00125$ and $\varepsilon = 0.0000156$. The output voltage V_{O-} is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_{O-}(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_{O-} = V_{O-}/R_1$.

2.6.1.3 Discontinuous Mode

The equivalent circuits of the discontinuous mode's operation are shown in [Figure 2.59c](#) and [Figure 2.60c](#). In order to obtain the mirror-symmetrical double output voltages, select:

$$L = \frac{L_1 L_2}{L_1 + L_2} = L_{11}$$

and $R = R_1$. Thus, we define

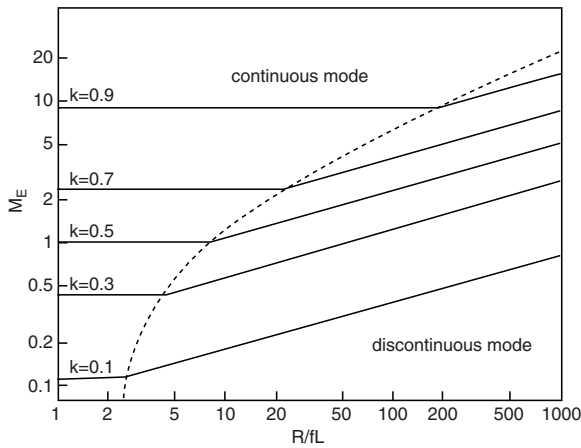


FIGURE 2.62

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$ (elementary circuit).

$$V_O = V_{O+} = |V_{O-}| \quad M_E = M_{E+} = M_{E-} = \frac{V_O}{V_I} = \frac{k}{1-k}$$

$$z_N = z_{N+} = z_{N-} \quad \text{and} \quad \zeta = \zeta_+ = \zeta_-$$

The free-wheeling diode currents i_{D0} and i_{D10} become zero during switch off before next period switch on. The boundary between continuous and discontinuous modes is

$$\zeta \geq 1$$

i.e.,

$$\frac{k^2}{M_E^2} \frac{z_N}{2} \geq 1$$

or

$$M_E \leq k \sqrt{\frac{z_N}{2}} \quad (2.321)$$

The boundary curve is shown in [Figure 2.62](#).

In this case the free-wheeling diode's diode current exists in the period between kT and $[k + (1 - k)m_E]T$, where m_E is the **filling efficiency** and it is defined as:

$$m_E = \frac{1}{\zeta} = \frac{2M_E^2}{k^2 z_N} \quad (2.322)$$

Considering the Equation (2.321), therefore, $0 < m_E < 1$. Since the diode current i_{D0} becomes zero at $t = kT + (1-k)m_ET$, for the current i_{L1} $kTV_I = (1-k)m_ETV_C$ or

$$V_{C1} = \frac{k}{(1-k)m_E} V_I = k(1-k) \frac{z_N}{2} V_I \quad \text{with} \quad \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \quad (2.323)$$

and for the current i_{L2}

$$kT(V_I + V_{C1} - V_{O+}) = (1-k)m_ETV_{O+}$$

Therefore, the positive output voltage in discontinuous mode is

$$V_{O+} = \frac{k}{(1-k)m_E} V_I = k(1-k) \frac{z_N}{2} V_I \quad \text{with} \quad \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \quad (2.324)$$

For the current i_{L11} we have

$$kTV_I = (1-k)m_ETV_{C11}$$

or

$$V_{C11} = \frac{k}{(1-k)m_E} V_I = k(1-k) \frac{z_N}{2} V_I \quad \text{with} \quad \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \quad (2.325)$$

and for the current i_{L12} we have

$$kT(V_I + V_{C11} - V_{O-}) = (1-k)m_ETV_{O-}$$

Therefore, the negative output voltage in discontinuous mode is

$$V_{O-} = \frac{k}{(1-k)m_E} V_I = k(1-k) \frac{z_N}{2} V_I \quad \text{with} \quad \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \quad (2.326)$$

We then have

$$V_O = V_{O+} = V_{O-} = k(1-k) \frac{z_N}{2} V_I$$

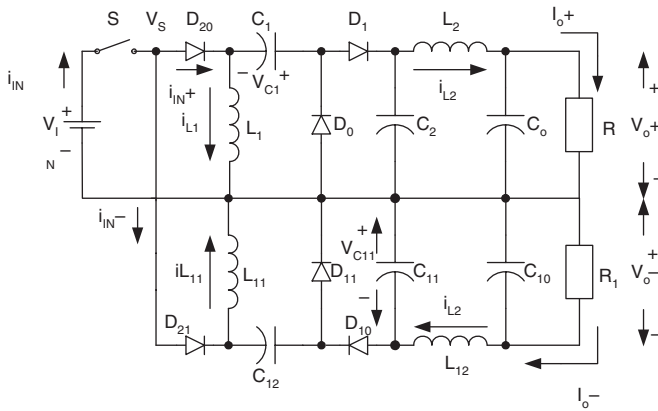


FIGURE 2.63
Self-lift circuit.

i.e., the output voltage will linearly increase while load resistance increases. It can be seen that larger load resistance may cause higher output voltage in discontinuous mode as shown in [Figure 2.62](#).

2.6.2 Self-Lift Circuit

Self-lift circuit shown in [Figure 2.63](#) is derived from the elementary circuit. The positive conversion path consists of a pump circuit S - L_1 - D_0 - C_1 , a filter (C_2)- L_2 - C_o , and a lift circuit D_1 - C_2 . The negative conversion path consists of a pump circuit S - L_{11} - D_{10} -(C_{11}), a “ Π ”-type filter C_{11} - L_{12} - C_{10} , and a lift circuit D_{11} - C_{11} .

2.6.2.1 Positive Conversion Path

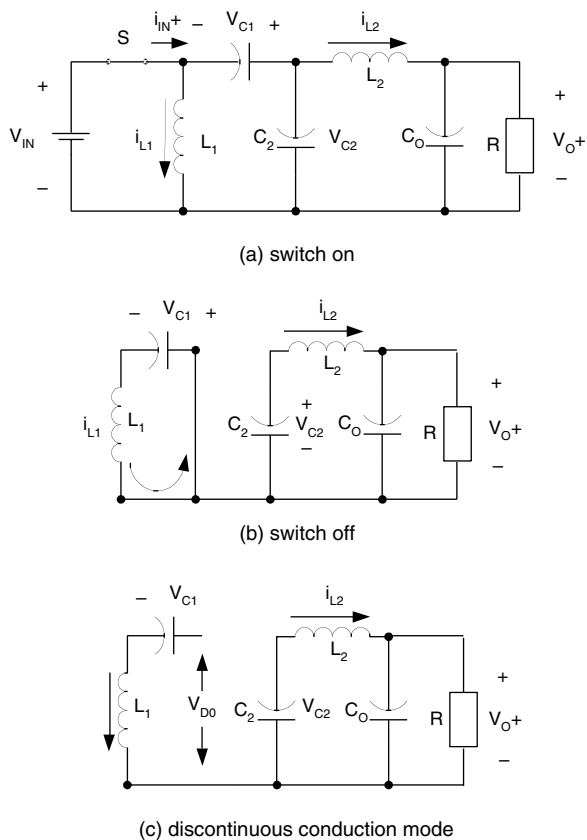
The equivalent circuit during switch-on is shown in [Figure 2.64a](#), and the equivalent circuit during switch-off in [Figure 2.64b](#). The voltage across inductor L_1 is equal to V_I during switch-on, and $-V_{C1}$ during switch-off. We have the relations:

$$V_{C1} = \frac{k}{1-k} V_I$$

Hence,

$$V_O = V_{CO} = V_{C2} = V_I + V_{C1} = \frac{1}{1-k} V_I$$

and

**FIGURE 2.64**

Equivalent circuits of self-lift circuit positive path: (a) switch on; (b) switch off; (c) discontinuous conduction mode.

$$V_{O+} = \frac{1}{1-k} V_I$$

The output current is

$$I_{O+} = (1-k)I_{I+}$$

Other relations are

$$I_{I+} = k i_{I+} \quad i_{I+} = I_{L1} + i_{C1-on} \quad i_{C1-off} = \frac{k}{1-k} i_{C1-on}$$

and

$$I_{L1} = i_{C1-off} = ki_{I+} = I_{I+} \quad (2.327)$$

Therefore, the voltage transfer gain in continuous mode is

$$M_{S+} = \frac{V_{O+}}{V_I} = \frac{1}{1-k} \quad (2.328)$$

The variation ratios of the parameters are

$$\xi_{2+} = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k}{16} \frac{1}{f^2 C_2 L_2} \quad \rho_+ = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{(1-k)I_{I+}}{2fC_1 \frac{k}{1-k} V_I} = \frac{1}{2kfC_1 R}$$

and

$$\sigma_{1+} = \frac{\Delta v_{C2} / 2}{V_{C2}} = \frac{k}{2fC_2 R}$$

The variation ratio of the currents i_{D0} and i_{L1} is

$$\zeta_+ = \xi_{1+} = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kV_I T}{2L_1 I_{I+}} = \frac{k}{M_S^2} \frac{R}{2fL_1} \quad (2.329)$$

The variation ratio of output voltage v_{O+} is

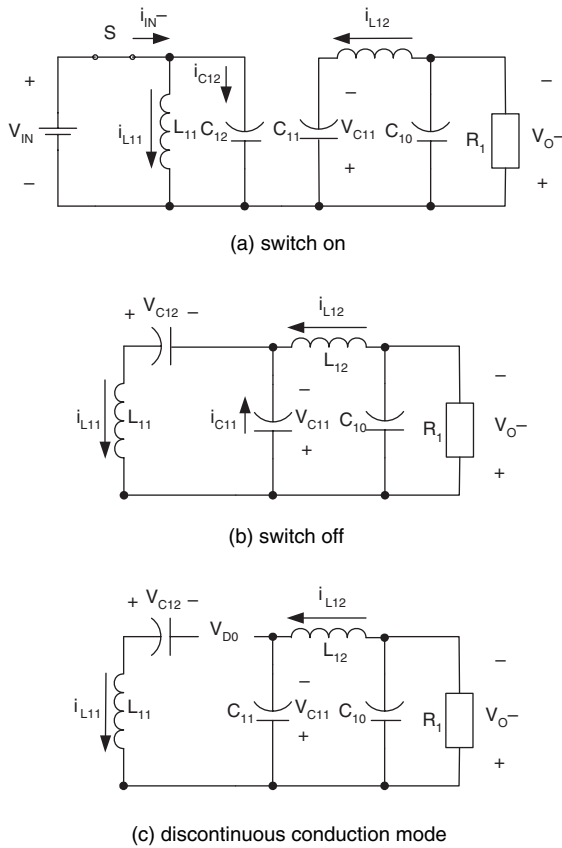
$$\epsilon_+ = \frac{\Delta v_{O+} / 2}{V_{O+}} = \frac{k}{128} \frac{1}{f^3 C_2 C_O L_2 R} \quad (2.330)$$

If $L_1 = L_2 = 0.5$ mH, $C_1 = C_2 = C_O = 20$ μ F, $R = 40$ Ω , $f = 50$ kHz, and $k = 0.5$, obtained that $\xi_{1+} = \zeta = 0.1$, $\rho_+ = 0.00625$; and $\sigma_{1+} = 0.00625$, $\xi_{2+} = 0.00125$ and $\epsilon = 0.000004$. Therefore, the variations of i_{L1} , v_{C1} , i_{L2} and v_{C2} are small. The output voltage V_{O+} is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_{O+}(t)$ is almost a real DC waveform with very small ripple as well, and $I_{O+} = V_{O+}/R$.

2.6.2.2 Negative Conversion Path

The equivalent circuit during switch-on is shown in [Figure 2.65a](#), and the equivalent circuit during switch-off in [Figure 2.65b](#). The relations of the average currents and voltages are

$$I_{O-} = I_{L12} = I_{C11-on} \quad I_{C11-off} = \frac{k}{1-k} \quad I_{C11-on} = \frac{k}{1-k} I_{O-}$$

**FIGURE 2.65**

Equivalent circuits of self-lift circuit negative path: (a) switch on; (b) switch off; (c) discontinuous conduction mode.

and

$$I_{L11} = I_{C11-off} + I_{O-} = \frac{I_{O-}}{1-k} \quad (2.331)$$

We know that

$$I_{C12-off} = I_{L11} = \frac{1}{1-k} I_{O-} \quad \text{and} \quad I_{C12-on} = \frac{1-k}{k} I_{C12-off} = \frac{1}{k} I_{O-}$$

So that

$$V_{O-} = \frac{1}{1-k} V_I \quad \text{and} \quad I_{O-} = (1-k) I_I$$

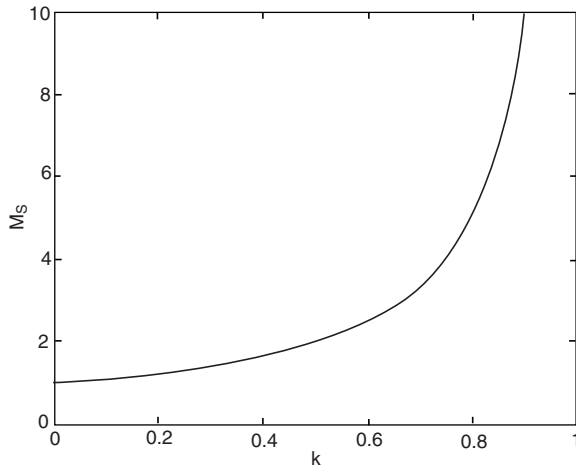


FIGURE 2.66

Voltage transfer gain M_S vs. k .

The voltage transfer gain in continuous mode:

$$M_{S-} = \frac{V_{O-}}{V_I} = \frac{1}{1-k} \quad (2.332)$$

Circuit (C_{11} - L_{12} - C_{10}) is a “ Π ” type low-pass filter. Therefore,

$$V_{C11} = V_{O-} = \frac{k}{1-k} V_I$$

From Equation (2.328) and Equation (2.332), we define $M_S = M_{S+} = M_{S-}$. The curve of M_S vs. k is shown in [Figure 2.66](#).

The variation ratios of the parameters are

$$\xi_- = \frac{\Delta i_{L12} / 2}{I_{L12}} = \frac{k}{16} \frac{1}{f^2 C_{10} L_{12}}$$

$$\rho_- = \frac{\Delta v_{C11} / 2}{V_{C11}} = \frac{k I_{O-} T}{2 C_{11} V_{O-}} = \frac{k}{2} \frac{1}{f C_{11} R_1}$$

$$\sigma_{1-} = \frac{\Delta v_{C12} / 2}{V_{C12}} = \frac{I_{O-}}{2 f C_{12} V_I} = \frac{M_S}{2} \frac{1}{f C_{12} R_1}$$

The variation ratio of currents i_{D10} and i_{L11} is

$$\zeta_- = \frac{\Delta i_{L11} / 2}{I_{L11}} = \frac{k(1-k)V_I T}{2L_{11}I_{O-}} = \frac{k(1-k)R_1}{2M_s f L_{11}} = \frac{k}{M_s^2} \frac{R_1}{2fL_{11}} \quad (2.333)$$

the variation ratio of current v_{C10} is

$$\varepsilon_- = \frac{\Delta v_{C10} / 2}{V_{C10}} = \frac{k}{128f^3 C_{11} C_{10} L_{12}} \frac{I_{O-}}{V_{O-}} = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1} \quad (2.334)$$

Assuming that $f = 50$ kHz, $L_{11} = L_{12} = 0.5$ μ H, $C_{11} = C_{10} = 20$ μ F, $R_1 = 40$ Ω and $k = 0.5$, we obtain $M_s = 2$, $\zeta_- = 0.2$, $\rho_- = 0.006$, $\sigma_{1-} = 0.025$, $\xi_- = 0.0006$ and $\varepsilon_- = 0.000004$. The output voltage V_{O-} is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_{O-}(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_{O-} = V_{O-}/R_1$.

2.6.2.3 Discontinuous Conduction Mode

The equivalent circuits of the discontinuous conduction mode's operation are shown in Figure 2.64 and Figure 2.65. Since we select $z_N = z_{N+} = z_{N-}$, $M_s = M_{s+} = M_{s-}$ and $\zeta = \zeta_+ = \zeta_-$. The boundary between continuous and discontinuous conduction modes is

$$\zeta \geq 1$$

or

$$\frac{k}{M_s^2} \frac{z_N}{2} \geq 1$$

Hence,

$$M_s \leq \sqrt{k} \sqrt{\frac{z}{2}} = \sqrt{\frac{kz_N}{2}} \quad (2.335)$$

This boundary curve is shown in Figure 2.67. Compared with Equation (2.321) and Equation (2.335), this boundary curve has a minimum value of M_s that is equal to 1.5 at $k = 1/3$.

The filling efficiency is defined as:

$$m_s = \frac{1}{\zeta} = \frac{2M_s^2}{kz_N} \quad (2.336)$$

For the current i_{L1} we have

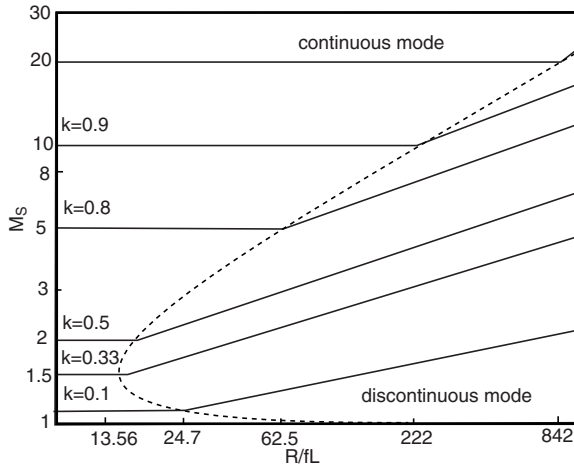


FIGURE 2.67

The boundary between continuous and discontinuous conduction modes and the output voltage vs. the normalized load $z_N = R/fL$ (self-lift circuit).

$$kTV_I = (1 - k)m_{s+}TV_{C1}$$

or

$$V_{C1} = \frac{k}{(1 - k)m_s} V_I = k^2(1 - k) \frac{z_N}{2} V_I \quad \text{with} \quad \sqrt{\frac{kz_N}{2}} \geq \frac{1}{1 - k} \quad (2.337)$$

Therefore, the positive output voltage in discontinuous mode is

$$V_{O+} = V_{C1} + V_I = \left[1 + \frac{k}{(1 - k)m_s}\right] V_I = \left[1 + k^2(1 - k) \frac{z_N}{2}\right] V_I$$

with
$$\sqrt{\frac{kz_N}{2}} \geq \frac{1}{1 - k} \quad (2.338)$$

For the current i_{L11} we have

$$kTV_I = (1 - k)m_s T(V_{C11} - V_I)$$

or

$$V_{C11} = \left[1 + \frac{k}{(1 - k)m_s}\right] V_I = \left[1 + k^2(1 - k) \frac{z_N}{2}\right] V_I$$

with

$$\sqrt{\frac{kz_N}{2}} \geq \frac{1}{1-k} \quad (2.339)$$

and for the current i_{L12} we have

$$kT(V_I + V_{C11} - V_{O-}) = (1-k)m_s T(V_{O-} - V_I)$$

Therefore, the negative output voltage in discontinuous conduction mode is

$$V_{O-} = [1 + \frac{k}{(1-k)m_s}]V_I = [1 + k^2(1-k)\frac{z_N}{2}]V_I$$

with

$$\sqrt{\frac{kz_N}{2}} \geq \frac{1}{1-k} \quad (2.340)$$

We then have

$$V_O = V_{O+} = V_{O-} = [1 + k^2(1-k)\frac{z_N}{2}]V_I$$

i.e., the output voltage will linearly increase during load resistance increasing. Larger load resistance causes higher output voltage in discontinuous conduction mode as shown in [Figure 2.67](#).

2.6.3 Re-Lift Circuit

Re-lift circuit shown in [Figure 2.68](#) is derived from self-lift circuit. The positive conversion path consists of a pump circuit $S-L_1-D_0-C_1$ and a filter $(C_2)-L_2-C_{O'}$, and a lift circuit $D_1-C_2-D_3-L_3-D_2-C_3$. The negative conversion path consists of a pump circuit $S-L_{11}-D_{10}-(C_{11})$ and a “Π”-type filter $C_{11}-L_{12}-C_{10'}$, and a lift circuit $D_{11}-C_{12}-L_{13}-D_{22}-C_{13}-D_{12}$.

2.6.3.1 Positive Conversion Path

The equivalent circuit during switch-on is shown in [Figure 2.69a](#), and the equivalent circuit during switch-off in [Figure 2.69b](#). The voltage across inductors L_1 and L_3 is equal to V_I during switch-on, and $-(V_{C1} - V_I)$ during switch-off. We have the relations:

$$V_{C1} = \frac{1+k}{1-k} V_I \quad \text{and} \quad V_O = V_{CO} = V_{C2} = V_I + V_{C1} = \frac{2}{1-k} V_I$$

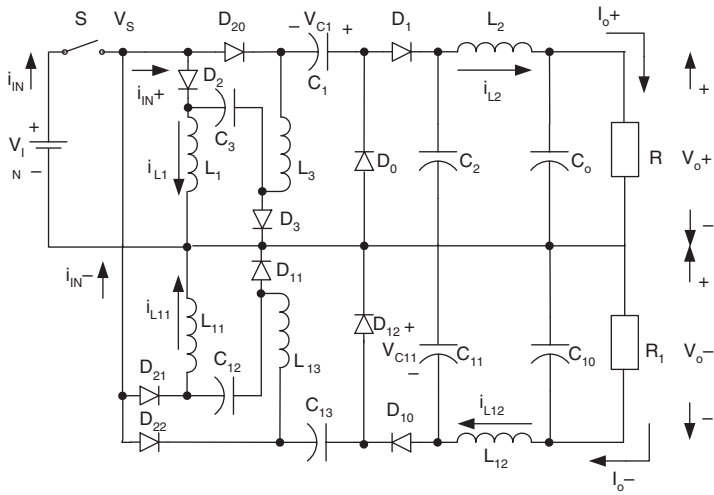


FIGURE 2.68
Re-lift circuit.

Thus,

$$V_{O+} = \frac{2}{1-k} V_I$$

and

$$I_{O+} = \frac{1-k}{2} I_{I+}$$

The other relations are

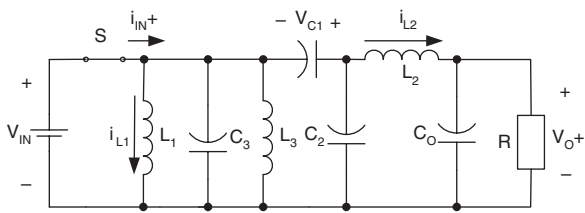
$$I_{I+} = k i_{I+} \quad i_{I+} = I_{L1} + I_{L3} + i_{C3-on} + i_{C1-on} \quad i_{C1-off} = \frac{k}{1-k} i_{C1-on}$$

and

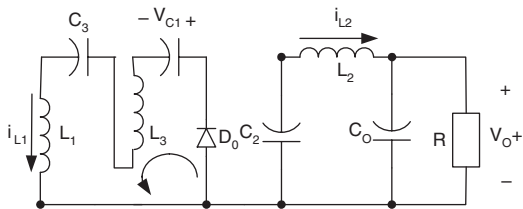
$$I_{L1} = I_{L3} = i_{C1-off} = i_{C3-off} = \frac{k}{2} i_{I+} = \frac{1}{2} I_{I+} \quad (2.341)$$

The voltage transfer gain in continuous mode is

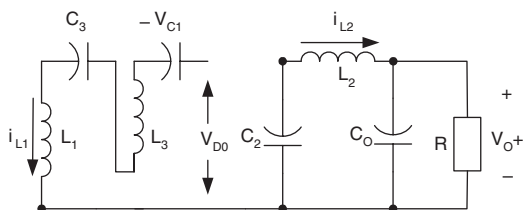
$$M_{R+} = \frac{V_{O+}}{V_I} = \frac{2}{1-k} \quad (2.342)$$



(a) switch on



(b) switch off



(c) discontinuous mode

FIGURE 2.69

Equivalent circuits of re-lift circuit positive path: (a) switch on; (b) switch off; (c) discontinuous mode.

The variation ratios of the parameters are

$$\xi_{2+} = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k}{16} \frac{1}{f^2 C_2 L_2} \quad \text{and} \quad \chi_{1+} = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k V_I T}{2 L_3 \frac{1}{2} I_{I+}} = \frac{k}{M_R^2} \frac{R}{f L_3}$$

$$\rho_+ = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{(1-k) T I_L}{4 C_1 \frac{1+k}{1-k} V_I} = \frac{1}{(1+k) f C_1 R}$$

$$\sigma_{1+} = \frac{\Delta v_{C2} / 2}{V_{C2}} = \frac{k}{2 f C_2 R} \quad \sigma_{2+} = \frac{\Delta v_{C3} / 2}{V_{C3}} = \frac{1-k}{4 f C_3} \frac{I_{I+}}{V_I} = \frac{M_R}{2 f C_3 R}$$

The variation ratio of currents i_{D0} and i_{L1} is

$$\zeta_+ = \xi_{1+} = \frac{\Delta i_{D0} / 2}{I_{D0}} = \frac{k V_I T}{L_1 I_{1+}} = \frac{k}{M_R^2} \frac{R}{f L_1} \quad (2.343)$$

and the variation ratio of output voltage v_{O+} is

$$\varepsilon_+ = \frac{\Delta v_{O+} / 2}{V_{O+}} = \frac{k}{128} \frac{1}{f^3 C_2 C_O L_2 R} \quad (2.344)$$

If $L_1 = L_2 = L_3 = 0.5$ mH, $C_1 = C_2 = C_3 = C_O = 20$ μ F, $R = 160$ Ω , $f = 50$ kHz, and $k = 0.5$, we obtained that $\xi_1 = \zeta_+ = 0.2$, $\chi_1 = 0.2$, $\sigma_\square = 0.0125$, $\rho = 0.004$; and $\sigma_1 = 0.00156$, $\xi_2 = 0.0125$ and $\varepsilon = 0.000001$. Therefore, the variations of i_{L1} , i_{L2} and i_{L3} are small, and the ripples of v_{C1} , v_{C3} and v_{C2} are small. The output voltage v_{O+} (and v_{CO}) is almost a real DC voltage with very small ripple. Because of the resistive load, the output current i_{O+} is almost a real DC waveform with very small ripple as well, and $I_{O+} = V_{O+}/R$.

2.6.3.2 Negative Conversion Path

The equivalent circuit during switch-on is shown in [Figure 2.70a](#), and the equivalent circuit during switch-off is shown in [Figure 2.70b](#). The relations of the average currents and voltages are

$$I_{O-} = I_{L12} = I_{C11-on} \quad I_{C11-off} = \frac{k}{1-k} I_{C11-on} = \frac{k}{1-k} I_{O-}$$

and

$$I_{L11} = I_{C11-off} + I_{O-} = \frac{I_{O-}}{1-k} \quad (2.345)$$

$$I_{C12-off} = I_{C13-off} = I_{L11} = \frac{1}{1-k} I_{O-} \quad I_{C12-on} = \frac{1-k}{k} I_{C12-off} = \frac{1}{k} I_{O-}$$

$$I_{C13-on} = \frac{1-k}{k} I_{C13-off} = \frac{1}{k} I_{O-}$$

In steady state we have:

$$V_{C12} = V_{C13} = V_I \quad V_{L13-on} = V_I \quad \text{and} \quad V_{L13-off} = \frac{k}{1-k} V_I$$

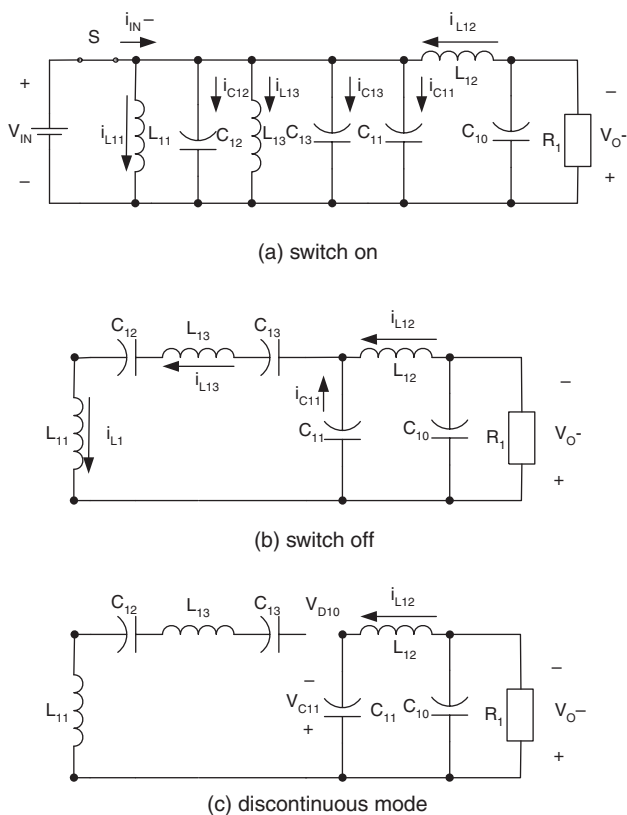


FIGURE 2.70

Equivalent circuits of re-lift circuit negative path: (a) switch on; (b) switch off; (c) discontinuous mode.

$$V_{O-} = \frac{2}{1-k} V_I \quad \text{and} \quad I_{O-} = \frac{1-k}{2} I_{I-}$$

The voltage transfer gain in continuous mode is

$$M_{R-} = \frac{V_{O-}}{V_I} = \frac{I_{I-}}{I_{O-}} = \frac{2}{1-k} \quad (2.346)$$

Circuit $(C_{11}-L_{12}-C_{10})$ is a “ Π ” type low-pass filter.

Therefore,

$$V_{C11} = V_{O-} = \frac{2}{1-k} V_I$$

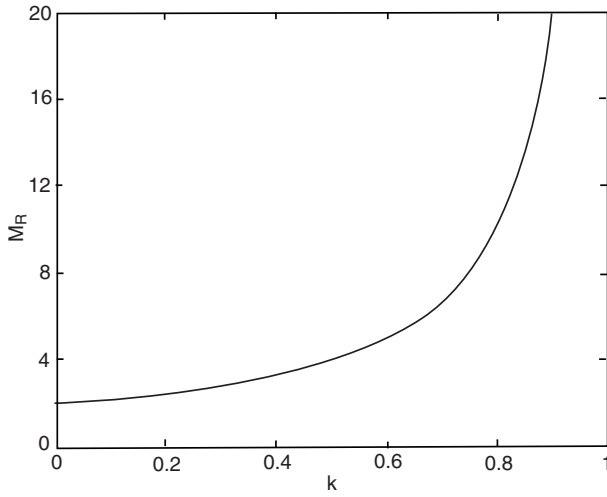


FIGURE 2.71

Voltage transfer gain M_R vs. k .

From Equation (2.342) and Equation (2.346) we define $M_R = M_{R+} = M_{R-}$. The curve of M_R vs. k is shown in [Figure 2.71](#).

The variation ratios of the parameters are

$$\xi_- = \frac{\Delta i_{L12} / 2}{I_{L12}} = \frac{k}{16} \frac{1}{f^2 C_{10} L_{12}}$$

and

$$\chi_{1-} = \frac{\Delta i_{L13} / 2}{I_{L13}} = \frac{kTV_I}{2L_{13}I_{O-}}(1-k) = \frac{k(1-k)}{2M_R} \frac{R_1}{fL_{13}}$$

$$\rho_- = \frac{\Delta v_{C11} / 2}{V_{C11}} = \frac{kI_{O-}T}{2C_{11}V_{O-}} = \frac{k}{2} \frac{1}{fC_{11}R_1}$$

$$\sigma_{1-} = \frac{\Delta v_{C12} / 2}{V_{C12}} = \frac{I_{O-}}{2fC_{12}V_I} = \frac{M_R}{2} \frac{1}{fC_{12}R_1}$$

$$\sigma_{2-} = \frac{\Delta v_{C13} / 2}{V_{C13}} = \frac{I_{O-}}{2fC_{13}V_I} = \frac{M_R}{2} \frac{1}{fC_{13}R_1}$$

The variation ratio of the current i_{D10} and i_{L11} is

$$\zeta_- = \frac{\Delta i_{L11} / 2}{I_{L11}} = \frac{k(1-k)V_I T}{2L_{11}I_{O-}} = \frac{k(1-k)R_1}{2M_R fL_{11}} = \frac{k}{M_R^2} \frac{R_1}{fL_{11}} \quad (2.347)$$

The variation ratio of current v_{C10} is

$$\varepsilon_- = \frac{\Delta v_{C10} / 2}{V_{C10}} = \frac{k}{128 f^3 C_{11} C_{10} L_{12}} \frac{I_{O-}}{V_{O-}} = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1} \quad (2.348)$$

Assuming that $f = 50$ kHz, $L_{11} = L_{12} = 0.5$ mH, $C = C_O = 20$ μ F, $R_1 = 160$ Ω and $k = 0.5$, we obtain $M_R = 4$, $\zeta_- = 0.2$, $\rho_- = 0.0016$, $\sigma_{1-} = \sigma_{2-} = 0.0125$, $\xi_- = 0.00125$ and $\varepsilon_- = 10^{-6}$. The output voltage V_{O-} is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_{O-}(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_{O-} = V_{O-}/R_1$.

2.6.3.3 Discontinuous Conduction Mode

The equivalent circuits of the discontinuous conduction mode are shown in [Figure 2.69](#) and [Figure 2.70](#). In order to obtain the mirror-symmetrical double output voltages, we purposely select $z_N = z_{N+} = z_{N-}$ and $\zeta = \zeta_+ = \zeta_-$. The free-wheeling diode currents i_{D0} and i_{D10} become zero during switch off before next period switch on. The boundary between continuous and discontinuous conduction modes is

$$\zeta \geq 1$$

or

$$\frac{k}{M_R^2} z_N \geq 1$$

Hence,

$$M_R \leq \sqrt{k z_N} \quad (2.349)$$

This boundary curve is shown in [Figure 2.71](#). Comparing with Equations (2.321), (2.335), and (2.349), it can be seen that the boundary curve has a minimum value of M_R that is equal to 3.0, corresponding to $k = 1/3$. The filling efficiency m_R is

$$m_R = \frac{1}{\zeta} = \frac{M_R^2}{k z_N} \quad (2.350)$$

So

$$V_{C1} = [1 + \frac{2k}{(1-k)m_R}] V_I = [1 + k^2(1-k) \frac{z_N}{2}] V_I$$

with

$$\sqrt{kz_N} \geq \frac{2}{1-k} \quad (2.351)$$

Therefore, the positive output voltage in discontinuous conduction mode is

$$V_{O+} = V_{C1} + V_I = [2 + \frac{2k}{(1-k)m_R}]V_I = [2 + k^2(1-k)\frac{z_N}{2}]V_I$$

with

$$\sqrt{kz_N} \geq \frac{2}{1-k} \quad (2.352)$$

For the current i_{L11} because inductor current $i_{L13} = 0$ at $t = t_1$, so that

$$V_{L13-off} = \frac{k}{(1-k)m_R} V_I$$

for the current i_{L11} we have

$$kTV_I = (1-k)m_RT(V_{C11} - 2V_I - V_{L13-off})$$

or

$$V_{C11} = [2 + \frac{2k}{(1-k)m_R}]V_I = [2 + k^2(1-k)\frac{z_N}{2}]V_I \quad \text{with} \quad \sqrt{kz_N} \geq \frac{2}{1-k} \quad (2.353)$$

and for the current i_{L12}

$$kT(V_I + V_{C11} - V_{O-}) = (1-k)m_RT(V_{O-} - 2V_I - V_{L13-off})$$

Therefore, the negative output voltage in discontinuous conduction mode is

$$V_{O-} = [2 + \frac{2k}{(1-k)m_R}]V_I = [2 + k^2(1-k)\frac{z_N}{2}]V_I \quad \text{with} \quad \sqrt{kz_N} \geq \frac{2}{1-k} \quad (2.354)$$

So

$$V_O = V_{O+} = V_{O-} = [2 + k^2(1-k)\frac{z_N}{2}]V_I$$

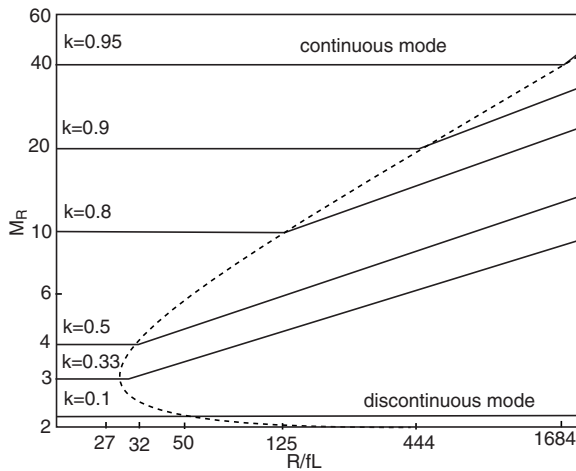


FIGURE 2.72

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$ (re-lift circuit).

i.e., the output voltage will linearly increase during load resistance increasing. Larger load resistance may cause higher output voltage in discontinuous mode as shown in Figure 2.72.

2.6.4 Multiple-Lift Circuit

Referring to Figure 2.68, it is possible to build a multiple-lifts circuit only using the parts $(L_3-D_{20}-C_3-D_3)$ multiple times in the positive conversion path, and using the parts $(D_{22}-L_{13}-C_{13}-D_{12})$ multiple times in the negative conversion path. For example, in Figure 2.73 the parts $(L_4-D_4-C_4-D_5)$ and parts $(D_{23}-L_{14}-C_{14}-D_{13})$ were added in the triple-lift circuit. According to this principle, triple-lift circuits and quadruple-lift circuits have been built as shown in Figure 2.73 and Figure 2.76. In this book it is not necessary to introduce the particular analysis and calculations one by one to readers. However, their calculation formulas are shown in this section.

2.6.4.1 Triple-Lift Circuit

Triple-lift circuit is shown in Figure 2.73. The positive conversion path consists of a pump circuit $S-L_1-D_0-C_1$ and a filter $(C_2)-L_2-C_O$, and a lift circuit $D_1-C_2-D_2-C_3-D_3-L_3-D_4-C_4-D_5-L_4$. The negative conversion path consists of a pump circuit $S-L_{11}-D_{10}-(C_{11})$ and a “Π”-type filter $C_{11}-L_{12}-C_{10}$, and a lift circuit $D_{11}-C_{12}-D_{22}-C_{13}-L_{13}-D_{12}-D_{23}-L_{14}-C_{14}-D_{13}$.

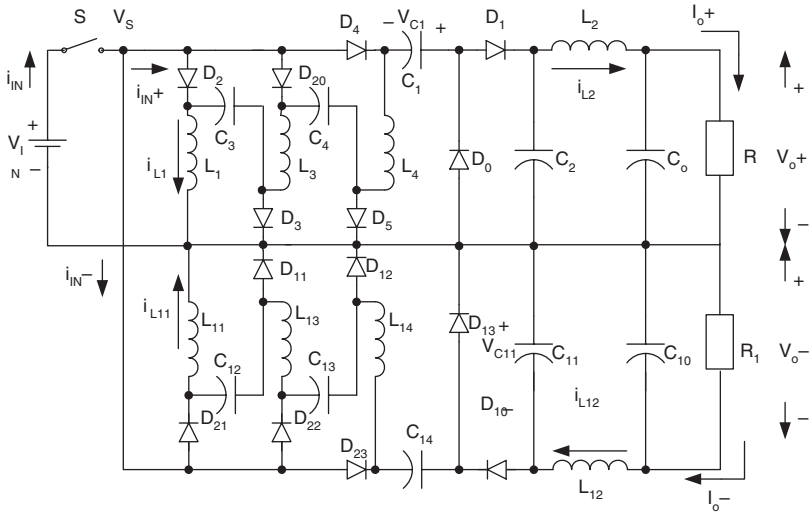


FIGURE 2.73
Triple-lift circuit.

2.6.4.1.1 Positive Conversion Path

The lift circuit is D_1 - C_2 - D_2 - C_3 - D_3 - L_3 - D_4 - C_4 - D_5 - L_4 . Capacitors C_2 , C_3 , and C_4 perform characteristics to lift the capacitor voltage V_{C1} by three times of source voltage V_I . L_3 and L_4 perform the function as ladder joints to link the three capacitors C_3 and C_4 and lift the capacitor voltage V_{C1} up. Current $i_{C2}(t)$, $i_{C3}(t)$, and $i_{C4}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C3} = v_{C4} = V_I$ and $v_{C2} = V_{O+}$ in steady state.

The output voltage and current are

$$V_{O+} = \frac{3}{1-k} V_I \quad \text{and} \quad I_{O+} = \frac{1-k}{3} I_{I+}$$

The voltage transfer gain in continuous mode is

$$M_{T+} = \frac{V_{O+}}{V_I} = \frac{3}{1-k} \quad (2.355)$$

Other average voltages:

$$V_{C1} = \frac{2+k}{1-k} V_I \quad V_{C3} = V_{C4} = V_I \quad V_{CO} = V_{C2} = V_{O+}$$

Other average currents:

$$I_{L2} = I_{O+} \quad I_{L1} = I_{L3} = I_{L4} = \frac{1}{3} I_{I+} = \frac{1}{1-k} I_{O+}$$

Current variations:

$$\xi_{1+} = \zeta_{+} = \frac{k(1-k)R}{2M_T fL} = \frac{k}{M_T^2} \frac{3R}{2fL} \quad \xi_{2+} = \frac{k}{16} \frac{1}{f^2 C_2 L_2}$$

$$\chi_{1+} = \frac{k}{M_T^2} \frac{3R}{2fL_3} \quad \chi_{2+} = \frac{k}{M_T^2} \frac{3R}{2fL_4}$$

Voltage variations:

$$\rho_{+} = \frac{3}{2(2+k)fC_1 R} \quad \sigma_{1+} = \frac{k}{2fC_2 R}$$

$$\sigma_{2+} = \frac{M_T}{2fC_3 R} \quad \sigma_{3+} = \frac{M_T}{2fC_4 R}$$

The variation ratio of output voltage V_{C0} is

$$\varepsilon_{+} = \frac{k}{128} \frac{1}{f^3 C_2 C_O L_2 R} \quad (2.356)$$

2.6.4.1.2 Negative Conversion Path

Circuit C_{12} - D_{11} - L_{13} - D_{22} - C_{13} - D_{12} - L_{14} - D_{23} - C_{14} - D_{13} is the lift circuit. Capacitors C_{12} , C_{13} , and C_{14} perform characteristics to lift the capacitor voltage V_{C11} by three times the source voltage V_I . L_{13} and L_{14} perform the function as ladder joints to link the three capacitors C_{12} , C_{13} , and C_{14} and lift the capacitor voltage V_{C11} up. Current $i_{C12}(t)$, $i_{C13}(t)$ and $i_{C14}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C12} = v_{C13} = v_{C14} \cong V_I$ in steady state.

The output voltage and current are

$$V_{O-} = \frac{3}{1-k} V_I \quad \text{and} \quad I_{O-} = \frac{1-k}{3} I_{I-}$$

The voltage transfer gain in continuous mode is

$$M_{T-} = V_{O-} / V_I = \frac{3}{1-k} \quad (2.357)$$

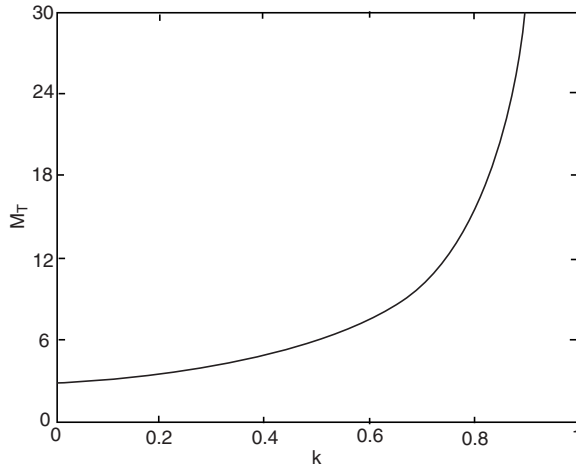


FIGURE 2.74

Voltage transfer gain M_T vs. k .

From Equation (2.355) and Equation (2.357) we define $M_T = M_{T+} = M_{T-}$. The curve of M_T vs. k is shown in [Figure 2.74](#).

Other average voltages:

$$V_{C11} = V_{O-} \quad V_{C12} = V_{C13} = V_{C14} = V_I$$

Other average currents:

$$I_{L12} = I_{O-} \quad I_{L11} = I_{L13} = I_{L14} = \frac{1}{1-k} I_{O-}$$

Current variation ratios:

$$\begin{aligned} \zeta_- &= \frac{k}{M_T^2} \frac{3R_1}{2fL_{11}} & \xi_{2-} &= \frac{k}{16} \frac{1}{f^2 C_{10} L_{12}} \\ \chi_{1-} &= \frac{k(1-k)}{2M_T} \frac{R_1}{fL_{13}} & \chi_{2-} &= \frac{k(1-k)}{2M_T} \frac{R_1}{fL_{14}} \end{aligned}$$

Voltage variation ratios:

$$\begin{aligned} \rho_- &= \frac{k}{2} \frac{1}{fC_{11}R_1} & \sigma_{1-} &= \frac{M_T}{2} \frac{1}{fC_{12}R_1} \\ \sigma_{2-} &= \frac{M_T}{2} \frac{1}{fC_{13}R_1} & \sigma_{3-} &= \frac{M_T}{2} \frac{1}{fC_{14}R_1} \end{aligned}$$

The variation ratio of output voltage V_{C10} is

$$\varepsilon_- = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1} \quad (2.358)$$

2.6.4.1.3 Discontinuous Mode

To obtain the mirror-symmetrical double output voltages, we purposely select: $L_1 = L_{11}$ and $R = R_1$.

Define:

$$V_O = V_{O+} = V_{O-} \quad M_T = M_{T+} = M_{T-} = \frac{V_O}{V_I} = \frac{3}{1-k} \quad z_N = z_{N+} = z_{N-}$$

and

$$\zeta = \zeta_+ = \zeta_-$$

The free-wheeling diode currents i_{D0} and i_{D10} become zero during switch off before next period switch on. The boundary between continuous and discontinuous conduction modes is

$$\zeta \geq 1$$

Then

$$M_T \leq \sqrt{\frac{3kz_N}{2}} \quad (2.359)$$

This boundary curve is shown in [Figure 2.75](#). Comparing Equation (2.321), Equation (2.335), Equation (2.349), and Equation (2.359), it can be seen that the boundary curve has a minimum value of M_T that is equal to 4.5, corresponding to $k = 1/3$.

In discontinuous mode the currents i_{D0} and i_{D10} exist in the period between kT and $[k + (1 - k)m_T]T$, where m_T is the filling efficiency that is

$$m_T = \frac{1}{\zeta} = \frac{2M_T^2}{3kz_N} \quad (2.360)$$

Considering Equation (2.359), therefore $0 < m_T < 1$. Since the current i_{D0} becomes zero at $t = t_1 = [k + (1 - k)m_T]T$, for the current i_{L1} , i_{L3} and i_{L4}

$$3kTV_I = (1 - k)m_T T(V_{C1} - 2V_I)$$

or

$$V_{C1} = [2 + \frac{3k}{(1 - k)m_T}]V_I = [2 + k^2(1 - k)\frac{z_N}{2}]V_I$$

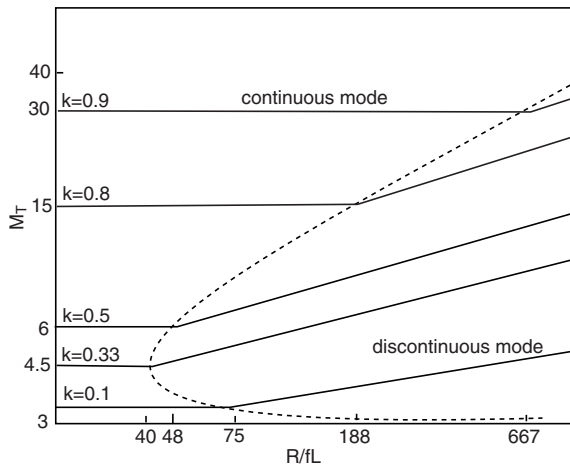


FIGURE 2.75

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fl$ (triple-lift circuit).

with

$$\sqrt{\frac{3kz_N}{2}} \geq \frac{3}{1-k} \quad (2.361)$$

Therefore, the positive output voltage in discontinuous mode is

$$V_{O+} = V_{C1} + V_I = \left[3 + \frac{3k}{(1-k)m_T}\right]V_I = \left[3 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{\frac{3kz_N}{2}} \geq \frac{3}{1-k} \quad (2.362)$$

Because inductor current $i_{L11} = 0$ at $t = t_1$, so that

$$V_{L13-off} = V_{L14-off} = \frac{k}{(1-k)m_T}V_I$$

Since i_{D10} becomes 0 at $t_1 = [k + (1-k)m_T]T$, for the current i_{L11} ,

$$kTV_I = (1-k)m_T T(V_{C11} - 3V_I - V_{L13-off} - V_{L14-off})$$

$$V_{C11} = \left[3 + \frac{3k}{(1-k)m_T}\right]V_I = \left[3 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{\frac{3kz_N}{2}} \geq \frac{3}{1-k} \quad (2.363)$$

for the current i_{L12}

$$kT(V_I + V_{C14} - V_{O-}) = (1-k)m_T T(V_{O-} - 2V_I - V_{L13-off} - V_{L14-off})$$

Therefore, the negative output voltage in discontinuous mode is

$$V_{O-} = [3 + \frac{3k}{(1-k)m_T}]V_I = [3 + k^2(1-k)\frac{z_N}{2}]V_I$$

with

$$\sqrt{\frac{3kz_N}{2}} \geq \frac{3}{1-k} \quad (2.364)$$

So

$$V_O = V_{O+} = V_{O-} = [3 + k^2(1-k)\frac{z_N}{2}]V_I$$

i.e., the output voltage will linearly increase during load resistance increasing, as shown in [Figure 2.75](#).

2.6.4.2 Quadruple-Lift Circuit

Quadruple-lift circuit is shown in [Figure 2.76](#). The positive conversion path consists of a pump circuit $S-L_1-D_0-C_1$ and a filter $(C_2)-L_2-C_O$, and a lift circuit $D_1-C_2-L_3-D_2-C_3-D_3-L_4-D_4-C_4-D_5-L_5-D_6-C_5-S_1$. The negative conversion path consists of a pump circuit $S-L_{11}-D_{10}-(C_{11})$ and a “ Π ”-type filter $C_{11}-L_{12}-C_{10}$, and a lift circuit $D_{11}-C_{12}-D_{22}-L_{13}-C_{13}-D_{12}-D_{23}-L_{14}-C_{14}-D_{13}-D_{24}-L_{15}-C_{15}-D_{14}$.

2.6.4.2.1 Positive Conversion Path

Capacitors C_2 , C_3 , C_4 , and C_5 perform characteristics to lift the capacitor voltage V_{C1} by four times the source voltage V_I . L_3 , L_4 , and L_5 perform the function as ladder joints to link the four capacitors C_2 , C_3 , C_4 , and C_5 , and lift the output capacitor voltage V_{C1} up. Current $i_{C2}(t)$, $i_{C3}(t)$, $i_{C4}(t)$ and $i_{C5}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C3} = v_{C4} = v_{C5} = V_I$ and $v_{C2} = V_{O+}$ in steady state.

The output voltage and current are

$$V_{O+} = \frac{4}{1-k} V_I \quad \text{and} \quad I_{O+} = \frac{1-k}{4} I_{I+}$$

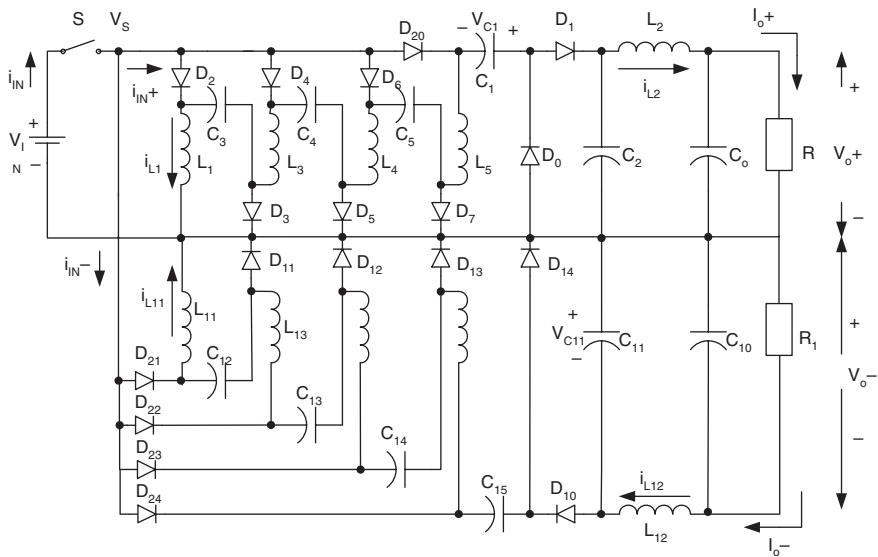


FIGURE 2.76
Quadruple-lift circuit.

The voltage transfer gain in continuous mode is

$$M_{Q+} = \frac{V_{O+}}{V_I} = \frac{4}{1-k} \quad (2.365)$$

Other average voltages:

$$V_{C1} = \frac{3+k}{1-k} V_I \quad V_{C3} = V_{C4} = V_{C5} = V_I \quad V_{CO} = V_{C2} = V_O$$

Other average currents:

$$I_{L2} = I_{O+} \quad I_{L1} = I_{L3} = I_{L4} = I_{L5} = \frac{1}{4} I_{I+} = \frac{1}{1-k} I_{O+}$$

Current variations:

$$\xi_{1+} = \zeta_+ = \frac{k(1-k)R}{2M_Q fL} = \frac{k}{M_Q^2} \frac{2R}{fL} \quad \xi_{2+} = \frac{k}{16} \frac{1}{f^2 C_2 L_2}$$

$$\chi_{1+} = \frac{k}{M_Q^2} \frac{2R}{fL_3} \quad \chi_{2+} = \frac{k}{M_Q^2} \frac{2R}{fL_4} \quad \chi_{3+} = \frac{k}{M_Q^2} \frac{2R}{fL_5}$$

Voltage variations:

$$\rho_+ = \frac{2}{(3+2k)fC_1R} \quad \sigma_{1+} = \frac{M_Q}{2fC_2R}$$

$$\sigma_{2+} = \frac{M_Q}{2fC_3R} \quad \sigma_{3+} = \frac{M_Q}{2fC_4R} \quad \sigma_{4+} = \frac{M_Q}{2fC_5R}$$

The variation ratio of output voltage V_{C0} is

$$\epsilon_+ = \frac{k}{128} \frac{1}{f^3 C_2 C_0 L_2 R} \quad (2.366)$$

2.6.4.2.2 Negative Conversion Path

Capacitors C_{12} , C_{13} , C_{14} , and C_{15} perform characteristics to lift the capacitor voltage V_{C11} by four times the source voltage V_I . L_{13} , L_{14} , and L_{15} perform the function as ladder joints to link the four capacitors C_{12} , C_{13} , C_{14} , and C_{15} and lift the output capacitor voltage V_{C11} up. Current $i_{C12}(t)$, $i_{C13}(t)$, $i_{C14}(t)$, and $i_{C15}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C12} = v_{C13} = v_{C14} = v_{C15} \cong V_I$ in steady state.

The output voltage and current are

$$V_{O-} = \frac{4}{1-k} V_I \quad \text{and} \quad I_{O-} = \frac{1-k}{4} I_{I-}$$

The voltage transfer gain in continuous mode is

$$M_{Q-} = V_{O-} / V_I = \frac{4}{1-k} \quad (2.367)$$

From Equation (2.365) and Equation (2.367) we define $M_Q = M_{Q+} = M_{Q-}$. The curve of M_Q vs. k is shown in [Figure 2.77](#).

Other average voltages:

$$V_{C10} = V_{O-} \quad V_{C12} = V_{C13} = V_{C14} = V_{C15} = V_I$$

Other average currents:

$$I_{L12} = I_{O-} \quad I_{L11} = I_{L13} = I_{L14} = I_{L15} = \frac{1}{1-k} I_{O-}$$

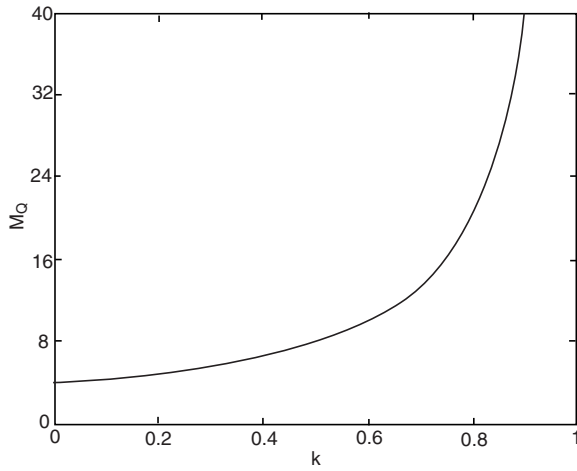


FIGURE 2.77

Voltage transfer gain M_Q vs. k .

Current variation ratios:

$$\zeta_- = \frac{k}{M_Q^2} \frac{2R_1}{fL_{11}} \quad \xi_- = \frac{k}{16} \frac{1}{f^2 CL_{12}}$$

$$\chi_{1-} = \frac{k(1-k)}{2M_Q} \frac{R_1}{fL_{13}} \quad \chi_{2-} = \frac{k(1-k)}{2M_Q} \frac{R_1}{fL_{14}} \quad \chi_{3-} = \frac{k(1-k)}{2M_Q} \frac{R_1}{fL_{15}}$$

Voltage variation ratios:

$$\rho_- = \frac{k}{2} \frac{1}{fC_{11}R_1} \quad \sigma_{1-} = \frac{M_Q}{2} \frac{1}{fC_{12}R_1}$$

$$\sigma_{2-} = \frac{M_Q}{2} \frac{1}{fC_{13}R_1} \quad \sigma_{3-} = \frac{M_Q}{2} \frac{1}{fC_{14}R_1} \quad \sigma_{4-} = \frac{M_Q}{2} \frac{1}{fC_{15}R_1}$$

The variation ratio of output voltage V_{C10} is

$$\varepsilon_- = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1} \quad (2.368)$$

The output voltage ripple is very small.

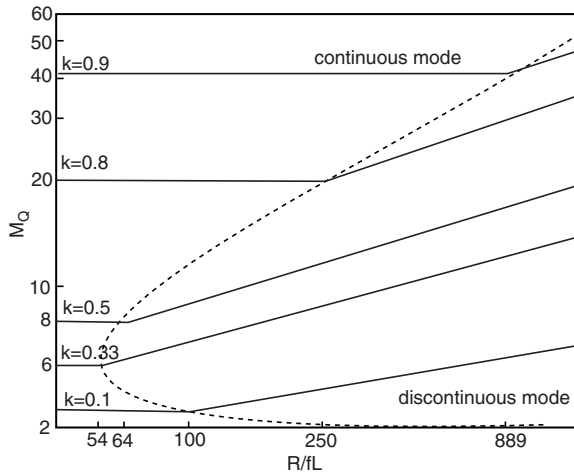


FIGURE 2.78

The boundary between continuous and discontinuous modes and the output voltage vs. the normalized load $z_N = R/fL$ (quadruple-lift circuit).

2.6.4.2.3 Discontinuous Conduction Mode

In order to obtain the mirror-symmetrical double output voltages, we purposely select: $L_1 = L_{11}$ and $R = R_1$. Therefore, we may define

$$V_O = V_{O+} = V_{O-} \quad M_Q = M_{Q+} = M_{Q-} = \frac{V_O}{V_I} = \frac{4}{1-k} \quad z_N = z_{N+} = z_{N-}$$

and
$$\zeta = \zeta_+ = \zeta_-$$

The free-wheeling diode currents i_{D0} and i_{D10} become zero during switch off before next period switch on. The boundary between continuous and discontinuous conduction modes is

$$\zeta \geq 1$$

or

$$M_Q \leq \sqrt{2kz_N} \quad (2.369)$$

This boundary curve is shown in [Figure 2.78](#). Comparing Equations (2.321), (2.335), (2.349), (2.359), and (2.369), it can be seen that this boundary curve has a minimum value of M_Q that is equal to 6.0, corresponding to $k = 1/3$.

In discontinuous mode the currents i_{D0} and i_{D10} exist in the period between kT and $[k + (1 - k)m_Q]T$, where m_Q is the filling efficiency that is

$$m_Q = \frac{1}{\zeta} = \frac{M_Q^2}{2kz_N} \quad (2.370)$$

Considering Equation (2.369), therefore $0 < m_Q < 1$. Since the current i_{D0} becomes zero at $t = t_1 = kT + (1 - k)m_Q T$, for the current i_{L1} , i_{L3} , i_{L4} and i_{L5}

$$4kTV_I = (1 - k)m_Q T(V_{C1} - 3V_I)$$

$$V_{C1} = [3 + \frac{4k}{(1 - k)m_Q}]V_I = [3 + k^2(1 - k)\frac{z_N}{2}]V_I$$

with
$$\sqrt{2kz_N} \geq \frac{4}{1 - k} \quad (2.371)$$

Therefore, the positive output voltage in discontinuous conduction mode is

$$V_{O+} = V_{C1} + V_I = [4 + \frac{4k}{(1 - k)m_Q}]V_I = [4 + k^2(1 - k)\frac{z_N}{2}]V_I$$

with
$$\sqrt{2kz_N} \geq \frac{4}{1 - k} \quad (2.372)$$

Because inductor current $i_{L11} = 0$ at $t = t_1$, so that

$$V_{L13-off} = V_{L14-off} = V_{L15-off} = \frac{k}{(1 - k)m_Q} V_I$$

Since the current i_{D10} becomes zero at $t = t_1 = kT + (1 - k)m_Q T$, for the current i_{L11} we have

$$kTV_I = (1 - k)m_Q T(V_{C11} - 4V_I - V_{L13-off} - V_{L14-off} - V_{L15-off})$$

So

$$V_{C11} = [4 + \frac{4k}{(1 - k)m_Q}]V_I = [4 + k^2(1 - k)\frac{z_N}{2}]V_I$$

with
$$\sqrt{2kz_N} \geq \frac{4}{1 - k} \quad (2.373)$$

TABLE 2.3

Comparison among Five Circuits of Double Output Luo-Converters

Double Output Luo-Converters	I_O	V_O	$k = 0.33$	$V_O(V_s = 10 \text{ V})$		
				$k = 0.5$	$k = 0.75$	$k = 0.9$
Elementary Circuit	$I_O = \frac{1-k}{k} I_s$	$V_O = \frac{k}{1-k} V_s$	5 V	10 V	30 V	90 V
Self-Lift Circuit	$I_O = (1-k) I_s$	$V_O = \frac{1}{1-k} V_s$	15 V	20 V	40 V	100 V
Re-Lift Circuit	$I_O = \frac{1-k}{2} I_s$	$V_O = \frac{2}{1-k} V_s$	30 V	40 V	80 V	200 V
Triple-Lift Circuit	$I_O = \frac{1-k}{3} I_s$	$V_O = \frac{3}{1-k} V_s$	45 V	60 V	120 V	300 V
Quadruple-Lift Circuit	$I_O = \frac{1-k}{4} I_s$	$V_O = \frac{4}{1-k} V_s$	60 V	80 V	160 V	400 V

For the current i_{L12}

$$kT(V_I + V_{C15} - V_{O-}) = (1-k)m_Q T(V_{O-} - 2V_I - V_{L13-off} - V_{L14-off} - V_{L15-off})$$

Therefore, the negative output voltage in discontinuous conduction mode is

$$V_{O-} = [4 + \frac{4k}{(1-k)m_Q}]V_I = [4 + k^2(1-k)\frac{z_N}{2}]V_I$$

with
$$\sqrt{2kz_N} \geq \frac{4}{1-k} \quad (2.374)$$

So

$$V_O = V_{O+} = V_{O-} = [4 + k^2(1-k)\frac{z_N}{2}]V_I$$

i.e., the output voltage will linearly increase during load resistance increasing, as shown in [Figure 2.78](#).

2.6.5 Summary

2.6.5.1 Positive Conversion Path

From the analysis and calculation in previous sections, the common formulae can be obtained for all circuits:

$$M = \frac{V_{O+}}{V_I} = \frac{I_{I+}}{I_{O+}} \quad z_N = \frac{R}{fL} \quad R = \frac{V_{O+}}{I_{O+}}$$

$$L = \frac{L_1 L_2}{L_1 + L_2}$$

for elementary circuits only;

$$L = L_1$$

for other lift circuit's current variations:

$$\xi_{1+} = \frac{1-k}{2M_E} \frac{R}{fL_1} \quad \text{and} \quad \xi_{2+} = \frac{k}{2M_E} \frac{R}{fL_2}$$

for elementary circuit only;

$$\xi_{1+} = \zeta_+ = \frac{k(1-k)R}{2MfL} \quad \text{and} \quad \xi_{2+} = \frac{k}{16} \frac{1}{f^2 C_2 L_2}$$

for other lift circuits

$$\zeta_+ = \frac{k(1-k)R}{2MfL} \quad \chi_{j+} = \frac{k}{M^2} \frac{R}{fL_{j+2}} \quad (j = 1, 2, 3, \dots)$$

Voltage variations are

$$\rho_+ = \frac{k}{2fC_1 R} \quad \varepsilon_+ = \frac{k}{8M_E} \frac{1}{f^2 C_0 L_2}$$

for elementary circuit only;

$$\rho_+ = \frac{M}{M-1} \frac{1}{2fC_1 R} \quad \varepsilon_+ = \frac{k}{128} \frac{1}{f^3 C_2 C_0 L_2 R}$$

for other lift circuits

$$\sigma_{1+} = \frac{k}{2fC_2 R} \quad \sigma_{j+} = \frac{M}{2fC_{j+1} R} \quad (j = 2, 3, 4, \dots)$$

2.6.5.2 Negative Conversion Path

From the analysis and calculation in previous sections, the common formulae can be obtained for all circuits:

$$M = \frac{V_{O-}}{V_I} = \frac{I_{I-}}{I_{O-}} \quad z_{N-} = \frac{R_1}{fL_{11}} \quad R_1 = \frac{V_{O-}}{I_{O-}}$$

Current variation ratios:

$$\zeta_- = \frac{k(1-k)R_1}{2MfL_{11}} \quad \xi_- = \frac{k}{16f^2C_{11}L_{12}} \quad \chi_{j-} = \frac{k(1-k)R_1}{2MfL_{j+2}} \quad (j = 1, 2, 3, \dots)$$

Voltage variation ratios:

$$\rho_- = \frac{k}{2fC_{11}R_1} \quad \varepsilon_- = \frac{k}{128f^3C_{11}C_{10}L_{12}R_1} \quad \sigma_{j-} = \frac{M}{2fC_{j+11}R_1} \quad (j = 1, 2, 3, 4, \dots)$$

2.6.5.3 Common Parameters

Usually, we select the loads $R = R_1$, $L = L_{11}$, so that we have got $z_N = z_{N+} = z_{N-}$. In order to write common formulas for the boundaries between continuous and discontinuous modes and output voltage for all circuits, the circuits can be numbered. The definition is that subscript 0 means the elementary circuit, subscript 1 means the self-lift circuit, subscript 2 means the re-lift circuit, subscript 3 means the triple-lift circuit, subscript 4 means the quadruple-lift circuit, and so on. The voltage transfer gain is

$$M_j = \frac{k^{h(j)}[j + h(j)]}{1 - k} \quad j = 0, 1, 2, 3, 4, \dots$$

The characteristics of output voltage of all circuits are shown in [Figure 2.79](#).

The free-wheeling diode current's variation is

$$\zeta_j = \frac{k^{[1+h(j)]}}{M_j^2} \frac{j + h(j)}{2} z_N$$

The boundaries are determined by the condition:

$$\zeta_j \geq 1$$

or

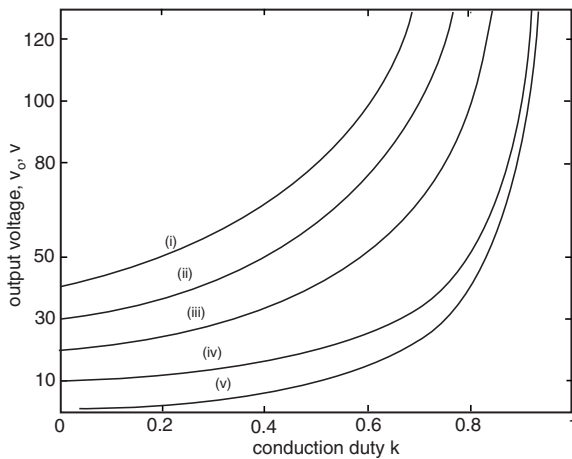


FIGURE 2.79

Output voltages of all double output Luo-converters ($V_i = 10$ V).

$$\frac{k^{[1+h(j)]}}{M_j^2} \frac{j+h(j)}{2} z_N \geq 1 \quad j = 0, 1, 2, 3, 4, \dots$$

Therefore, the boundaries between continuous and discontinuous modes for all circuits are

$$M_j = k^{\frac{1+h(j)}{2}} \sqrt{\frac{j+h(j)}{2} z_N} \quad j = 0, 1, 2, 3, 4, \dots$$

The filling efficiency is

$$m_j = \frac{1}{\zeta_j} = \frac{M_j^2}{k^{[1+h(j)]}} \frac{2}{j+h(j)} \frac{1}{z_N} \quad j = 0, 1, 2, 3, 4, \dots$$

The output voltage in discontinuous mode for all circuits

$$V_{O-j} = [j + k^{[2-h(j)]} \frac{1-k}{2} z_N] V_i$$

where

$$h(j) = \begin{cases} 0 & \text{if } j \geq 1 \\ 1 & \text{if } j = 0 \end{cases} \quad j = 0, 1, 2, 3, 4, \dots \quad h(j) \text{ is the Hong Function}$$

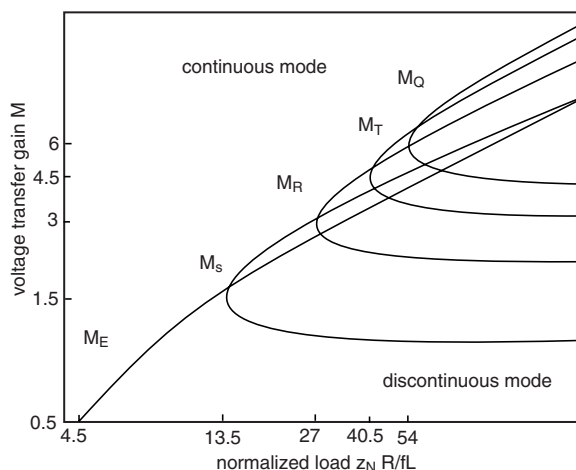


FIGURE 2.80

Boundaries between continuous and discontinuous modes of all double output Luo-Converters.

The boundaries between continuous and discontinuous modes of all circuits are shown in Figure 2.80. The curves of all M vs. z_N state that the continuous mode area increases from M_E via M_S , M_R , M_T to M_Q . The boundary of elementary circuit is a monorising curve, but other curves are not monorising. There are minimum values of the boundaries of other curves, which of M_S , M_R , M_T , and M_Q correspond at $k = 1/3$.

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Positive Output Super-Lift Luo-Converters

Voltage lift (VL) technique has been successfully employed in design of DC/DC converters, e.g., three series Luo-converters. However, the output voltage increases in arithmetic progression. Super-Lift (SL) technique is more powerful than VL technique, its voltage transfer gain can be a very large number. SL technique implements the output voltage increasing in geometric progression. It effectively enhances the voltage transfer gain in power series.

3.1 Introduction

This chapter introduces positive output super lift Luo-converters. In order to differentiate these converters from existing VL converters, these converters are called *positive output super-lift Luo-converters*. There are several sub-series:

- Main series — Each circuit of the main series has only one switch S , n inductors for n^{th} stage circuit, $2n$ capacitors, and $(3n - 1)$ diodes.
- Additional series — Each circuit of the additional series has one switch S , n inductors for n^{th} stage circuit, $2(n + 1)$ capacitors, and $(3n + 1)$ diodes.
- Enhanced series — Each circuit of the enhanced series has one switch S , n inductors for n^{th} stage circuit, $4n$ capacitors, and $(5n - 1)$ diodes.
- Re-enhanced series — Each circuit of the re-enhanced series has one switch S , n inductors for n^{th} stage circuit, $6n$ capacitors, and $(7n - 1)$ diodes.
- Multiple (j)-enhanced series — Each circuit of the multiple (j times)-enhanced series has one switch S , n inductors for n^{th} stage circuit, $2(1 + j)n$ capacitors and $[(3 + 2j)n - 1]$ diodes.

In order to concentrate the voltage enlargement, assume the converters are working in steady state with continuous conduction mode (CCM). The conduction duty ratio is k , switch frequency is f , switch period is $T = 1/f$,

the load is resistive load R . The input voltage and current are V_{in} and I_{in} , out voltage and current are V_O and I_O . Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_O \times I_O$. The voltage transfer gain is G :

$$G = \frac{V_O}{V_{in}}$$

3.2 Main Series

The first three stages of positive output super-lift Luo-converters — main series — are shown in [Figure 3.1](#) through [Figure 3.3](#). For convenience, they are called elementary circuits, re-lift circuit, and triple-lift circuit respectively, and are numbered as $n = 1, 2$, and 3 .

3.2.1 Elementary Circuit

The elementary circuit and its equivalent circuits during switch-on and -off are shown in [Figure 3.1](#). The voltage across capacitor C_1 is charged to V_{in} . The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_O - 2V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L1} is

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_O - 2V_{in}}{L_1} (1 - k)T \quad (3.1)$$

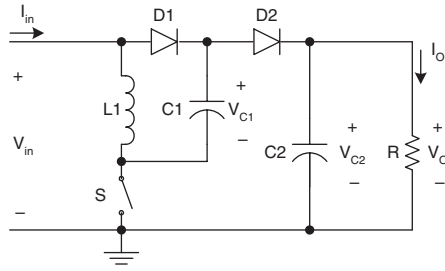
$$V_O = \frac{2 - k}{1 - k} V_{in} \quad (3.2)$$

The voltage transfer gain is

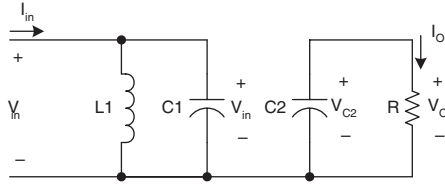
$$G = \frac{V_O}{V_{in}} = \frac{2 - k}{1 - k} \quad (3.3)$$

The input current i_{in} is equal to $(i_{L1} + i_{C1})$ during switch-on, and only equal to i_{L1} during switch-off. Capacitor current i_{C1} is equal to i_{L1} during switch-off. In steady-state, the average charge across capacitor C_1 should not change. The following relations are obtained:

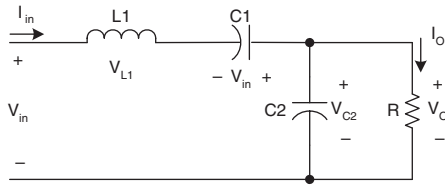
$$i_{in-off} = i_{L1-off} = i_{C1-off} \quad i_{in-on} = i_{L1-on} + i_{C1-on} \quad kTi_{C1-on} = (1 - k)Ti_{C1-off}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.1

Elementary circuit.

If inductance L_1 is large enough, i_{L1} is nearly equal to its average current I_{L1} . Therefore,

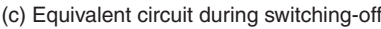
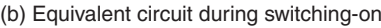
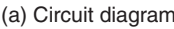
$$i_{in-off} = i_{C1-off} = I_{L1} \quad i_{in-on} = I_{L1} + \frac{1-k}{k} I_{L1} = \frac{I_{L1}}{k} \quad i_{C1-on} = \frac{1-k}{k} I_{L1}$$

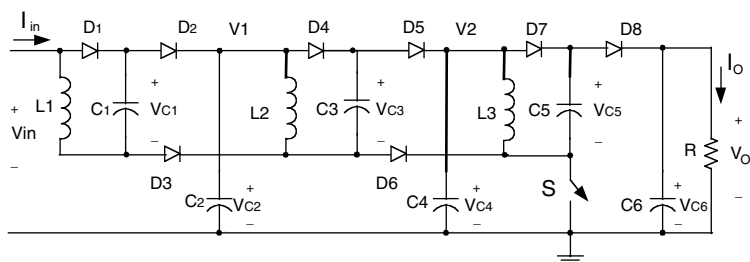
and average input current

$$I_{in} = k i_{in-on} + (1-k) i_{in-off} = I_{L1} + (1-k) I_{L1} = (2-k) I_{L1} \quad (3.4)$$

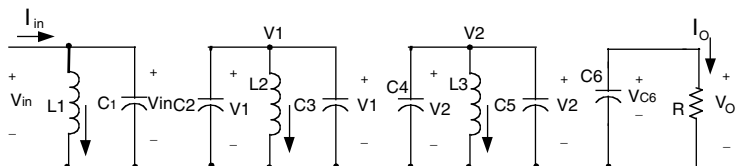
Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k} \right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k} \right)^2 R$$

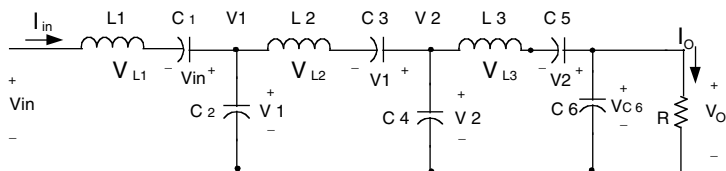




(a) Circuit diagram



(b) Equivalent circuit during switch-on



(c) Equivalent circuit during switch-off

FIGURE 3.3

Triple-lift circuit.

Usually R is in $k\Omega$, f in 10 kHz, and C_2 in μF , this ripple is smaller than 1%.

3.2.2 Re-Lift Circuit

The re-lift circuit is derived from elementary circuit by adding the parts (L_2 - D_3 - D_4 - D_5 - C_3 - C_4). Its circuit diagram and equivalent circuits during switch-on and -off are shown in Figure 3.2. The voltage across capacitor C_1 is charged to V_{in} . As described in previous section the voltage V_1 across capacitor C_2 is

$$V_1 = \frac{2-k}{1-k} V_{in}$$

The voltage across capacitor C_3 is charged to V_1 . The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_O - 2V_1)$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_1}{L_2} kT = \frac{V_O - 2V_1}{L_2} (1-k)T \quad (3.7)$$

$$V_O = \frac{2-k}{1-k} V_1 = \left(\frac{2-k}{1-k}\right)^2 V_{in} \quad (3.8)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2-k}{1-k}\right)^2 \quad (3.9)$$

Similarly, the following relations are obtained:

$$\begin{aligned} \Delta i_{L1} &= \frac{V_{in}}{L_1} kT & I_{L1} &= \frac{I_{in}}{2-k} \\ \Delta i_{L2} &= \frac{V_1}{L_2} kT & I_{L2} &= \left(\frac{2-k}{1-k} - 1\right) I_O = \frac{I_O}{1-k} \end{aligned}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \frac{k(1-k)^4}{2(2-k)^3} \frac{R}{fL_1} \quad (3.10)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{2L_2 I_O} = \frac{k(1-k)^2 TV_O}{2(2-k)L_2 I_O} = \frac{k(1-k)^2}{2(2-k)} \frac{R}{fL_2} \quad (3.11)$$

and the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_4} \quad (3.12)$$

3.2.3 Triple-Lift Circuit

Triple-lift circuit is derived from re-lift circuit by double adding the parts (L_2 - D_3 - D_4 - D_5 - C_3 - C_4). Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 3.3](#). The voltage across capacitor C_1 is charged to V_{in} . As described before the voltage V_1 across capacitor C_2 is $V_1 = (2-k/1-k)V_{in}$, and voltage V_2 across capacitor C_4 is $V_2 = (2-k/1-k)^2 V_{in}$.

The voltage across capacitor C_5 is charged to V_2 . The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_O - 2V_2)$ during switch-off $(1 - k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L3} = \frac{V_2}{L_3} kT = \frac{V_O - 2V_2}{L_3} (1 - k)T \quad (3.13)$$

$$V_O = \frac{2 - k}{1 - k} V_2 = \left(\frac{2 - k}{1 - k}\right)^2 V_1 = \left(\frac{2 - k}{1 - k}\right)^3 V_{in} \quad (3.14)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2 - k}{1 - k}\right)^3 \quad (3.15)$$

Analogously,

$$\begin{aligned} \Delta i_{L1} &= \frac{V_{in}}{L_1} kT & I_{L1} &= \frac{I_{in}}{2 - k} \\ \Delta i_{L2} &= \frac{V_1}{L_2} kT & I_{L2} &= \frac{2 - k}{(1 - k)^2} I_O \\ \Delta i_{L3} &= \frac{V_2}{L_3} kT & I_{L3} &= \frac{I_O}{1 - k} \end{aligned}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(2 - k)TV_{in}}{2L_1 I_{in}} = \frac{k(1 - k)^6}{2(2 - k)^5} \frac{R}{fL_1} \quad (3.16)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1 - k)^2 TV_1}{2(2 - k)L_2 I_O} = \frac{kT(2 - k)^4 V_O}{2(1 - k)^3 L_2 I_O} = \frac{k(2 - k)^4}{2(1 - k)^3} \frac{R}{fL_2} \quad (3.17)$$

The variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1 - k)TV_2}{2L_3 I_O} = \frac{k(1 - k)^2 TV_O}{2(2 - k)L_2 I_O} = \frac{k(1 - k)^2}{2(2 - k)} \frac{R}{fL_3} \quad (3.18)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_6} \quad (3.19)$$

3.2.4 Higher Order Lift Circuit

Higher order lift circuit can be designed by just multiple repeating the parts (L_2 - D_3 - D_4 - D_5 - C_3 - C_4). For n th order lift circuit, the final output voltage across capacitor C_{2n} is

$$V_o = \left(\frac{2-k}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^n \quad (3.20)$$

The variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{2(2-k)^{2(n-i)+1}} \frac{R}{fL_i} \quad (3.21)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{2n}} \quad (3.22)$$

3.3 Additional Series

Using two diodes and two capacitors (D_{11} - D_{12} - C_{11} - C_{12}), a circuit called *double/enhance circuit* (DEC) can be constructed, which is shown in [Figure 3.4](#), which is same as the [Figure 1.22](#) but with components renumbered. If the input voltage is V_{in} , the output voltage V_o can be $2V_{in}$, or other value that is higher than V_{in} . The DEC is very versatile to enhance DC/DC converter's voltage transfer gain.

All circuits of positive output super-lift Luo-converters-additional series are derived from the corresponding circuits of the main series by adding a DEC. The first three stages of this series are shown in [Figure 3.5](#) to [Figure 3.7](#).

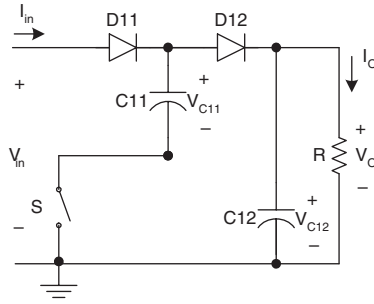


FIGURE 3.4
Double/enhanced circuit (DEC).

For convenience they are called elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit respectively, and numbered as $n = 1, 2$, and 3 .

3.3.1 Elementary Additional Circuit

This circuit is derived from elementary circuit by adding a DEC. Its circuit and switch-on and -off equivalent circuits are shown in [Figure 3.5](#). The voltage across capacitor C_1 is charged to V_{in} and voltage across capacitor C_2 and C_{11} is charged to V_1 . The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_O - 2V_{in})$ during switch-off $(1 - k)T$. Therefore,

$$V_1 = \frac{2-k}{1-k} V_{in} \quad (3.23)$$

and

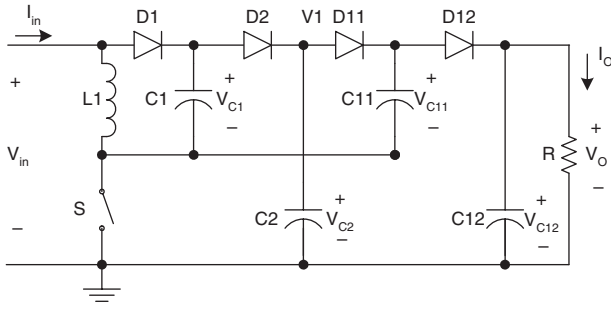
$$V_{L1} = \frac{k}{1-k} V_{in} \quad (3.24)$$

The output voltage is

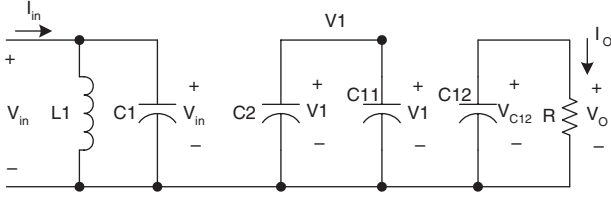
$$V_O = V_{in} + V_{L1} + V_1 = \frac{3-k}{1-k} V_{in} \quad (3.25)$$

The voltage transfer gain is

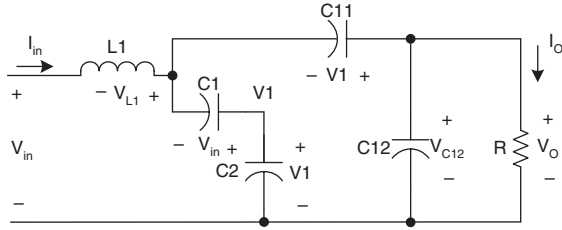
$$G = \frac{V_O}{V_{in}} = \frac{3-k}{1-k} \quad (3.26)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.5

Elementary additional (enhanced) circuit.

The following relations are derived:

$$i_{in-off} = I_{L1} = i_{C11-off} + i_{C1-off} = \frac{2I_O}{1-k}$$

$$i_{in-on} = i_{L1-on} + i_{C1-on} = I_{L1} + \frac{I_O}{k}$$

$$i_{C1-on} = \frac{1-k}{k} i_{C1-off} = \frac{I_O}{k}$$

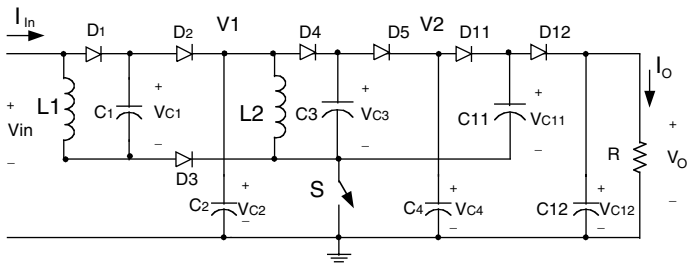
$$i_{C1-off} = i_{C2-off} = \frac{I_O}{1-k}$$

$$i_{C2-off} = \frac{k}{1-k} i_{C2-on} = \frac{k}{1-k} i_{C11-on} = \frac{I_O}{1-k}$$

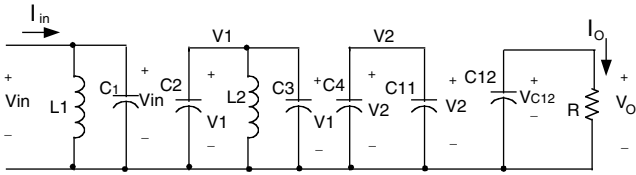
$$i_{C11-on} = \frac{1-k}{k} i_{C11-off} = \frac{I_O}{k}$$

$$i_{C11-off} = I_O + i_{C12-off} = I_O + \frac{k}{1-k} i_{C12-on} = \frac{I_O}{1-k}$$

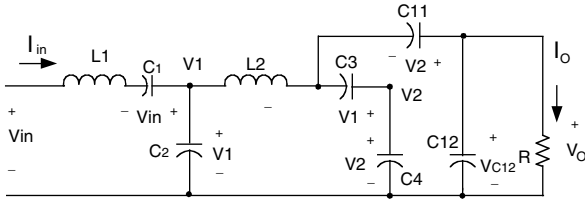
$$i_{C12-off} = \frac{k}{1-k} i_{C12-on} = \frac{kI_O}{1-k}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.6

Re-lift additional circuit.

If inductance L_1 is large enough, i_{L1} is nearly equal to its average current I_{L1} . Therefore,

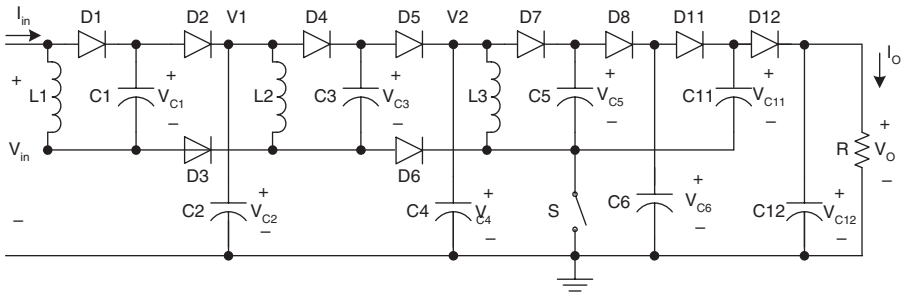
$$i_{in-off} = I_{L1} = \frac{2I_O}{1-k} \quad i_{in-on} = I_{L1} + \frac{I_O}{k} = \left(\frac{2}{1-k} + \frac{1}{k}\right)I_O = \frac{1+k}{k(1-k)}I_O$$

Verification:

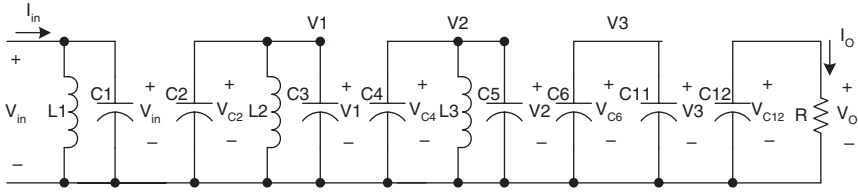
$$I_{in} = ki_{in-on} + (1-k)i_{in-off} = \left(\frac{1+k}{1-k} + 2\right)I_O = \frac{3-k}{1-k}I_O$$

Considering

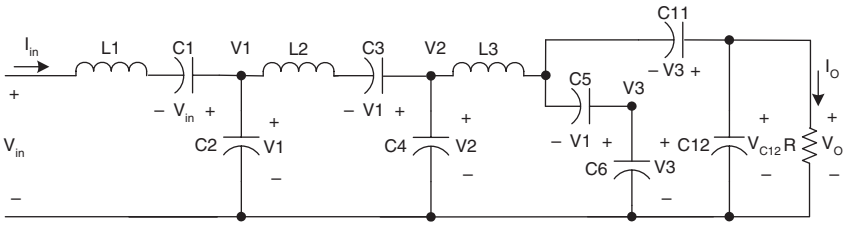
$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.7

Triple-lift additional circuit.

The variation of current i_{L1} is

$$\Delta i_{L1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_1} \quad (3.27)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2R_f C_{12}} \quad (3.28)$$

3.3.2 Re-Lift Additional Circuit

This circuit is derived from the re-lift circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 3.6](#). The voltage across capacitor C_1 is charged to V_{in} . As described in previous section the voltage across C_2 is

$$V_1 = \frac{2-k}{1-k} V_{in}$$

The voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_4 and C_{11} is charged to V_2 . The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_o - 2V_1)$ during switch-off $(1-k)T$. Therefore,

$$V_2 = \frac{2-k}{1-k} V_1 = \left(\frac{2-k}{1-k}\right)^2 V_{in} \quad (3.29)$$

and

$$V_{L2} = \frac{k}{1-k} V_1 \quad (3.30)$$

The output voltage is

$$V_o = V_1 + V_{L2} + V_2 = \frac{2-k}{1-k} \frac{3-k}{1-k} V_{in} \quad (3.31)$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k} \frac{3-k}{1-k} \quad (3.32)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_O} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \quad (3.33)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \quad (3.34)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (3.35)$$

3.3.3 Triple-Lift Additional Circuit

This circuit is derived from the triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 3.7](#). The voltage across capacitor C_1 is charged to V_{in} . As described in previous section the voltage across C_2 is

$$V_1 = \frac{2-k}{1-k} V_{in}$$

and voltage across C_4 is

$$V_2 = \frac{2-k}{1-k} V_1 = \left(\frac{2-k}{1-k}\right)^2 V_{in}$$

The voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_6 and C_{11} is charged to V_3 . The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_O - 2V_2)$ during switch-off $(1-k)T$. Therefore,

$$V_3 = \frac{2-k}{1-k} V_2 = \left(\frac{2-k}{1-k}\right)^2 V_1 = \left(\frac{2-k}{1-k}\right)^3 V_{in} \quad (3.36)$$

and

$$V_{L3} = \frac{k}{1-k} V_2 \quad (3.37)$$

The output voltage is

$$V_O = V_2 + V_{L3} + V_3 = \left(\frac{2-k}{1-k}\right)^2 \frac{3-k}{1-k} V_{in} \quad (3.38)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2-k}{1-k}\right)^2 \frac{3-k}{1-k} \quad (3.39)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{(2-k)(3-k)}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L1} through inductor L_1 is

$$\begin{aligned} \xi_1 &= \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 T V_{in}}{2(2-k)(3-k) L_1 I_O} \\ &= \frac{k(1-k)^3 T}{2(2-k)(3-k) L_1 I_O} \frac{(1-k)^3}{(2-k)^2 (3-k)} V_O = \frac{k(1-k)^6}{2(2-k)^3 (3-k)^2} \frac{R}{f L_1} \end{aligned} \quad (3.40)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\begin{aligned}\xi_2 &= \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_O} \\ &= \frac{k(1-k)^2 T}{2(3-k)L_2 I_O} \frac{(1-k)^2}{(2-k)(3-k)} V_O = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2}\end{aligned}\quad (3.41)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k)TV_2}{4L_3 I_O} = \frac{k(1-k)T}{4L_3 I_O} \frac{1-k}{3-k} V_O = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \quad (3.42)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (3.43)$$

3.3.4 Higher Order Lift Additional Circuit

The higher order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. For n^{th} order lift additional circuit, the final output voltage is

$$V_O = \left(\frac{2-k}{1-k}\right)^{n-1} \frac{3-k}{1-k} V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2-k}{1-k}\right)^{n-1} \frac{3-k}{1-k} \quad (3.44)$$

Analogously, the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \quad (3.45)$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \leq 0 \end{cases} \text{ is the **Hong function**}$$

and

$$u(x) = \begin{cases} 1 & x \geq 0 \\ 0 & x < 0 \end{cases} \text{ is the **unit-step function**}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12}} \quad (3.46)$$

3.4 Enhanced Series

All circuits of positive output super-lift Luo-converters-enhanced series — are derived from the corresponding circuits of the main series by adding a DEC in each stage circuit. The first three stages of this series are shown in [Figures 3.5, 3.8, and 3.9](#). For convenience they are called elementary enhanced circuit, re-lift enhanced circuit, and triple-lift enhanced circuit respectively, and numbered as $n = 1, 2$ and 3 .

3.4.1 Elementary Enhanced Circuit

This circuit is same as the elementary additional circuit shown in [Figure 3.5](#).

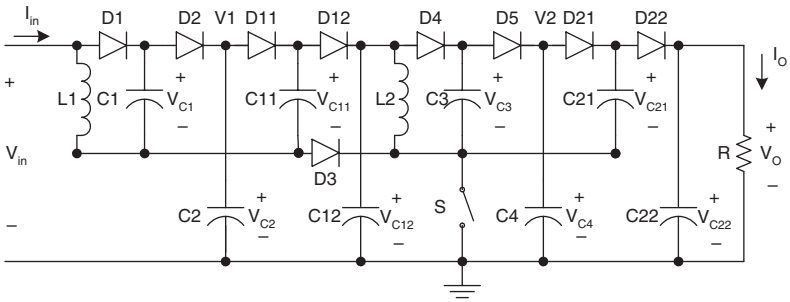
The output voltage is

$$V_o = V_{in} + V_{L1} + V_1 = \frac{3-k}{1-k} V_{in} \quad (3.25)$$

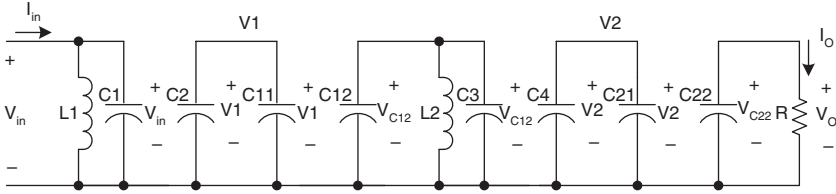
The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{3-k}{1-k} \quad (3.26)$$

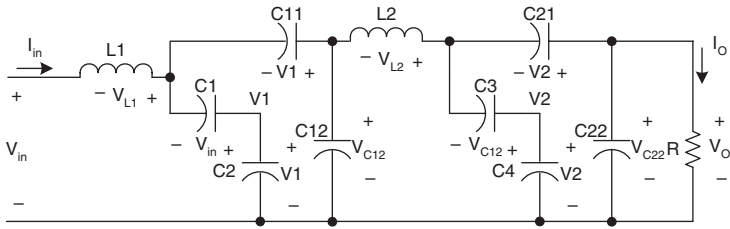
The variation of current i_{L1} is



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.8

Re-lift enhanced circuit.

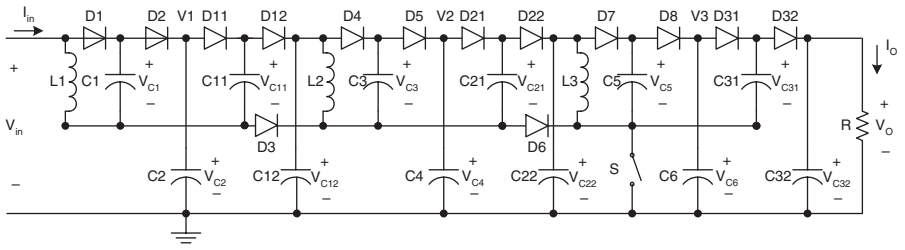
$$\Delta i_{L1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

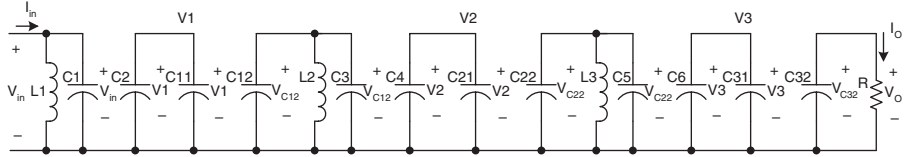
$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_1} \quad (3.27)$$

The ripple voltage of output voltage v_o is

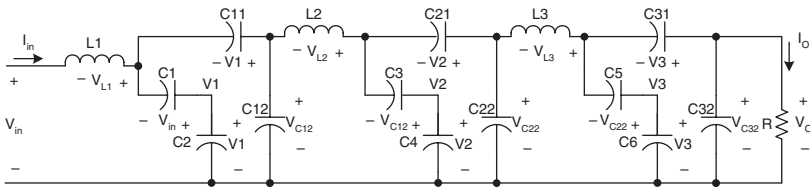
$$\Delta v_o = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.9

Triple-lift enhanced circuit.

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12}} \quad (3.28)$$

3.4.2 Re-Lift Enhanced Circuit

This circuit is derived from the re-lift circuit of the main series by adding the DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 3.8. As described in the previous section the voltage across capacitor C_{12} is charged to

$$V_{C12} = \frac{3-k}{1-k} V_{in}$$

The voltage across capacitor C_3 is charged to V_{C12} and voltage across capacitor C_4 and C_{21} is charged to V_{C4} ,

$$V_{C4} = \frac{2-k}{1-k} V_{C12} = \frac{2-k}{1-k} \frac{3-k}{1-k} V_{in} \quad (3.47)$$

The current flowing through inductor L_2 increases with voltage V_{C12} during switch-on period kT and decreases with voltage $-(V_O - V_{C4} - V_{C12})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L2} = \frac{k}{L_2} V_{C12} = \frac{1-k}{L_2} (V_O - V_{C4} - V_{C12}) \quad (3.48)$$

$$V_O = \frac{3-k}{1-k} V_{C12} = \left(\frac{3-k}{1-k}\right)^2 V_{in} \quad (3.49)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{3-k}{1-k}\right)^2 \quad (3.50)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_O} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \quad (3.51)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \quad (3.52)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{22}} = \frac{I_O(1-k)T}{C_{22}} = \frac{1-k}{fC_{22}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2R_f C_{22}} \quad (3.53)$$

3.4.3 Triple-Lift Enhanced Circuit

This circuit is derived from triple-lift circuit of the main series by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 3.9](#). As described in the previous section the voltage across capacitor C_{12} is charged to $V_{C12} = (3-k/1-k)V_{in}$, and the voltage across capacitor C_{22} is charged to $V_{C22} = (3-k/1-k)^2 V_{in}$.

The voltage across capacitor C_5 is charged to V_{C22} and voltage across capacitor C_6 and C_{31} is charged to V_{C6} .

$$V_{C6} = \frac{2-k}{1-k} V_{C22} = \frac{2-k}{1-k} \left(\frac{3-k}{1-k} \right)^2 V_{in} \quad (3.54)$$

The current flowing through inductor L_3 increases with voltage V_{C22} during switch-on period kT and decreases with voltage $-(V_o - V_{C6} - V_{C22})$ during switch-off $(1-k)T$.

Therefore,
$$\Delta i_{L3} = \frac{k}{L_3} V_{C22} = \frac{1-k}{L_3} (V_o - V_{C6} - V_{C22}) \quad (3.55)$$

$$V_o = \frac{3-k}{1-k} V_{C22} = \left(\frac{3-k}{1-k} \right)^3 V_{in} \quad (3.56)$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k} \right)^3 \quad (3.57)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{(2-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L1} through inductor L_1 is

$$\begin{aligned} \xi_1 &= \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_O} \\ &= \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_O} \frac{(1-k)^3}{(2-k)^2(3-k)} V_O = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \end{aligned} \quad (3.58)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\begin{aligned} \xi_2 &= \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_O} \\ &= \frac{k(1-k)^2 T}{2(3-k)L_2 I_O} \frac{(1-k)^2}{(2-k)(3-k)} V_O = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \end{aligned} \quad (3.59)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\begin{aligned} \xi_3 &= \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k)TV_2}{4L_3 I_O} \\ &= \frac{k(1-k)T}{4L_3 I_O} \frac{1-k}{3-k} V_O = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \end{aligned} \quad (3.60)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32}} = \frac{I_O(1-k)T}{C_{32}} = \frac{1-k}{fC_{32}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{32}} \quad (3.61)$$

3.4.4 Higher Order Lift Enhanced Circuit

The higher order lift enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC in each stage circuit. For the n^{th} order lift enhanced circuit, the final output voltage is $V_O = (3 - k/1 - k)^n V_{in}$. The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{3 - k}{1 - k} \right)^n \quad (3.62)$$

Analogously, the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1 - k)^{2(n-i+1)}}{2[2(2 - k)]^{h(n-i)} (2 - k)^{2(n-i)+1} (3 - k)^{2u(n-i-1)}} \frac{R}{fL_i} \quad (3.63)$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \leq 0 \end{cases} \quad \text{is the \textbf{Hong function}}$$

and

$$u(x) = \begin{cases} 1 & x \geq 0 \\ 0 & x < 0 \end{cases} \quad \text{is the \textbf{unit-step function}}$$

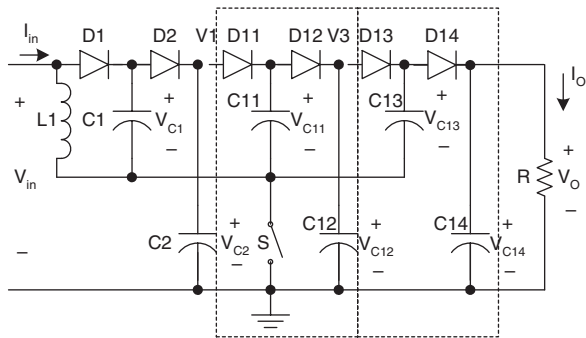
and the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1 - k}{2RfC_{n2}} \quad (3.64)$$

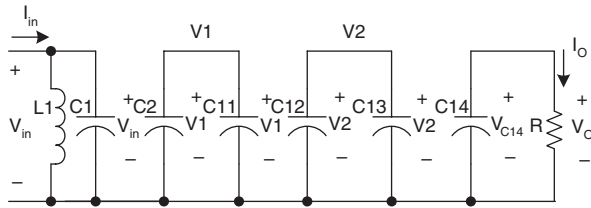
3.5 Re-Enhanced Series

All circuits of positive output super-lift Luo-converters-re-enhanced series — are derived from the corresponding circuits of the main series by adding the DEC twice in each stage circuit.

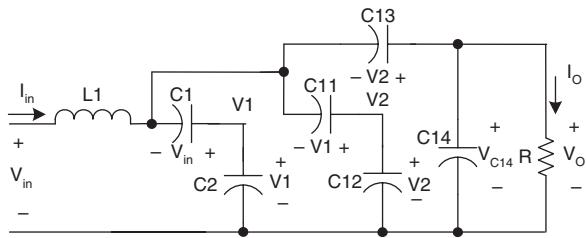
The first three stages of this series are shown in [Figure 3.10](#) to [Figure 3.12](#). For convenience they are named elementary re-enhanced circuits, re-lift re-enhanced circuits, and triple-lift re-enhanced circuits respectively, and numbered as $n = 1, 2$ and 3 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.10

Elementary re-enhanced circuit.

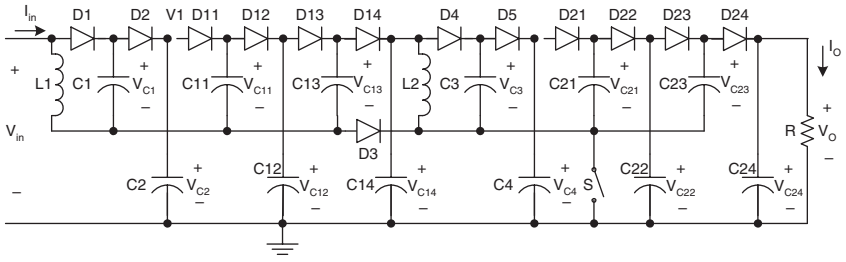
3.5.1 Elementary Re-Enhanced Circuit

This circuit is derived from the elementary circuit by adding the DEC twice. Its circuit and switch-on and -off equivalent circuits are shown in Figure 3.10.

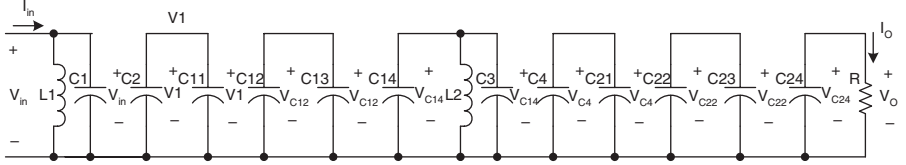
The output voltage is

$$V_O = V_{in} + V_{L1} + V_{C12} = \frac{4-k}{1-k} V_{in} \quad (3.65)$$

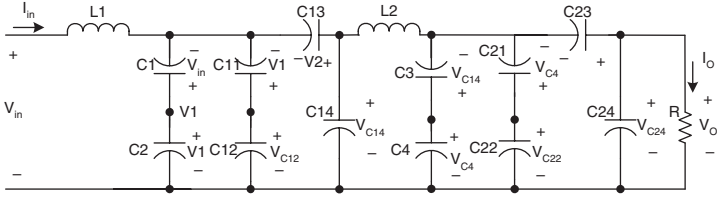
The voltage transfer gain is



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.11

Re-lift re-enhanced circuit.

$$G = \frac{V_o}{V_{in}} = \frac{4-k}{1-k} \quad (3.66)$$

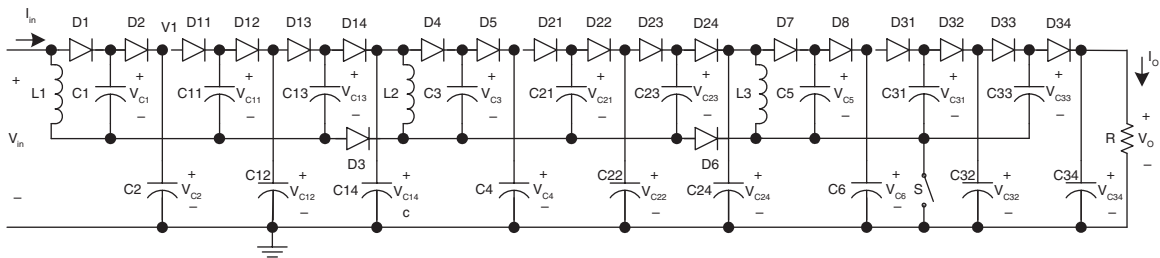
where

$$V_{C2} = \frac{2-k}{1-k} V_{in} \quad (3.67)$$

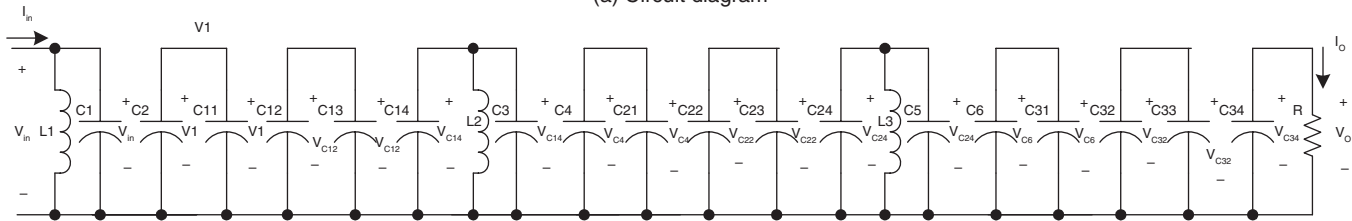
$$V_{C12} = \frac{3-k}{1-k} V_{in} \quad (3.68)$$

and

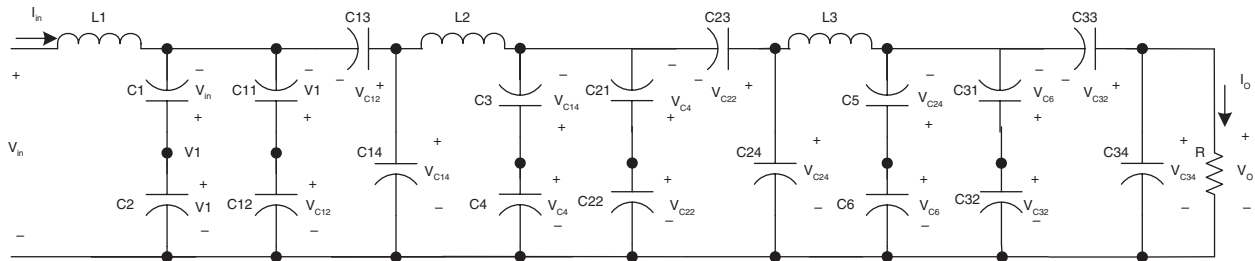
$$V_{L1} = \frac{k}{1-k} V_{in} \quad (3.69)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.12

Triple-lift re-enhanced circuit.

The following relations are obtained:

$$i_{in-off} = I_{L1} = i_{C11-off} + i_{C1-off} = \frac{2I_O}{1-k}$$

$$i_{in-on} = i_{L1-on} + i_{C1-on} = I_{L1} + \frac{I_O}{k}$$

$$i_{C1-on} = \frac{1-k}{k} i_{C1-off} = \frac{I_O}{k}$$

$$i_{C1-off} = i_{C2-off} = \frac{I_O}{1-k}$$

$$i_{C2-off} = \frac{k}{1-k} i_{C2-on} = \frac{k}{1-k} i_{C11-on} = \frac{I_O}{1-k}$$

$$i_{C11-on} = \frac{1-k}{k} i_{C11-off} = \frac{I_O}{k}$$

$$i_{C11-off} = I_O + i_{C12-off} = I_O + \frac{k}{1-k} i_{C12-on} = \frac{I_O}{1-k}$$

$$i_{C12-off} = \frac{k}{1-k} i_{C12-on} = \frac{kI_O}{1-k}$$

If inductance L_1 is large enough, i_{L1} is nearly equal to its average current I_{L1} . Therefore,

$$i_{in-off} = I_{L1} = \frac{2I_O}{1-k} \quad i_{in-on} = I_{L1} + \frac{I_O}{k} = \left(\frac{2}{1-k} + \frac{1}{k}\right)I_O = \frac{1+k}{k(1-k)}I_O$$

Verification:

$$I_{in} = ki_{in-on} + (1-k)i_{in-off} = \left(\frac{1+k}{1-k} + 2\right)I_O = \frac{3-k}{1-k}I_O$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation of current i_{L1} is

$$\Delta i_{L1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_1} \quad (3.70)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{14}} = \frac{I_o(1-k)T}{C_{14}} = \frac{1-k}{fC_{14}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{14}} \quad (3.71)$$

3.5.2 Re-Lift Re-Enhanced Circuit

This circuit is derived from the re-lift circuit of the main series by adding the DEC twice in each stage circuit. Its circuit and switch-on and -off equivalent circuits are shown in [Figure 3.11](#). The voltage across capacitor C_{14} is

$$V_{C14} = \frac{4-k}{1-k} V_{in} \quad (3.72)$$

By the same analysis

$$V_o = \frac{4-k}{1-k} V_{C14} = \left(\frac{4-k}{1-k}\right)^2 V_{in} \quad (3.73)$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^2 \quad (3.74)$$

Analogously,

$$\begin{aligned} \Delta i_{L1} &= \frac{V_{in}}{L_1} kT & I_{L1} &= \frac{3-k}{(1-k)^2} I_o \\ \Delta i_{L2} &= \frac{V_1}{L_2} kT & I_{L2} &= \frac{2I_o}{1-k} \end{aligned}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_o} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \quad (3.75)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \quad (3.76)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{24}} = \frac{I_O(1-k)T}{C_{24}} = \frac{1-k}{fC_{24}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{24}} \quad (3.77)$$

3.5.3 Triple-Lift Re-Enhanced Circuit

This circuit is derived from triple-lift circuit of the main series by adding the DEC twice in each stage circuit. Its circuit and switch-on and -off equivalent circuits are shown in [Figure 3.12](#). The voltage across capacitor C_{14} is

$$V_{C14} = \frac{4-k}{1-k} V_{in} \quad (3.78)$$

The voltage across capacitor C_{24} is

$$V_{C24} = \left(\frac{4-k}{1-k}\right)^2 V_{in} \quad (3.79)$$

By the same analysis

$$V_O = \frac{4-k}{1-k} V_{C24} = \left(\frac{4-k}{1-k}\right)^3 V_{in} \quad (3.80)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{4-k}{1-k}\right)^3 \quad (3.81)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{(2-k)(3-k)}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L1} through inductor L_1 is

$$\begin{aligned} \xi_1 &= \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_O} \\ &= \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_O} \frac{(1-k)^3}{(2-k)^2(3-k)} V_O = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \end{aligned} \quad (3.82)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\begin{aligned} \xi_2 &= \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_O} \\ &= \frac{k(1-k)^2 T}{2(3-k)L_2 I_O} \frac{(1-k)^2}{(2-k)(3-k)} V_O = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \end{aligned} \quad (3.83)$$

The variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k)TV_2}{4L_3 I_O} = \frac{k(1-k)T}{4L_3 I_O} \frac{1-k}{3-k} V_O = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \quad (3.84)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{34}} = \frac{I_O(1-k)T}{C_{34}} = \frac{1-k}{fC_{34}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{34}} \quad (3.85)$$

3.5.4 Higher Order Lift Re-Enhanced Circuit

Higher order lift additional circuits are derived from the corresponding circuit of the main series by adding DEC twice in each stage circuit. For the n^{th} order lift additional circuit, the final output voltage is

$$V_o = \left(\frac{4-k}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^n \quad (3.86)$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{L_i} / 2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \quad (3.87)$$

where

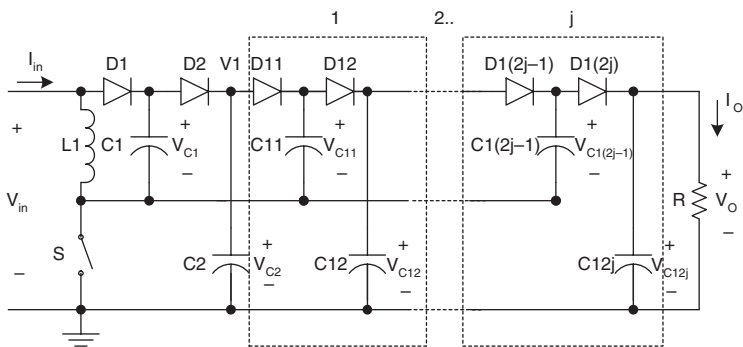
$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \leq 0 \end{cases} \quad \text{is the **Hong function**}$$

and

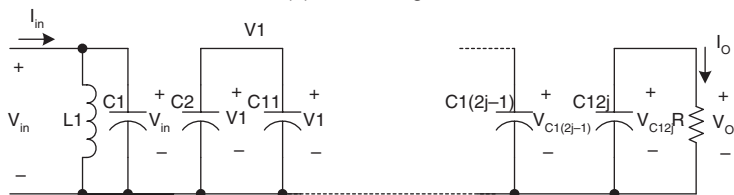
$$u(x) = \begin{cases} 1 & x \geq 0 \\ 0 & x < 0 \end{cases} \quad \text{is the **unit-step function**}$$

and the variation ratio of output voltage v_o is

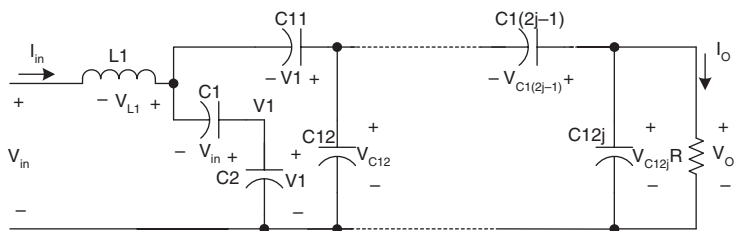
$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{n4}} \quad (3.88)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



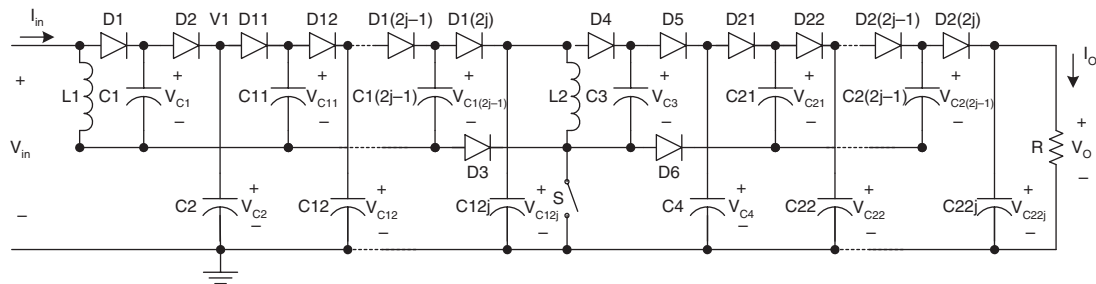
(c) Equivalent circuit during switching-off

FIGURE 3.13

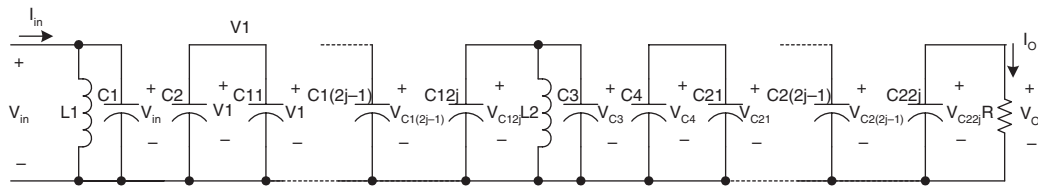
Elementary multiple-enhanced circuit.

3.6 Multiple-Enhanced Series

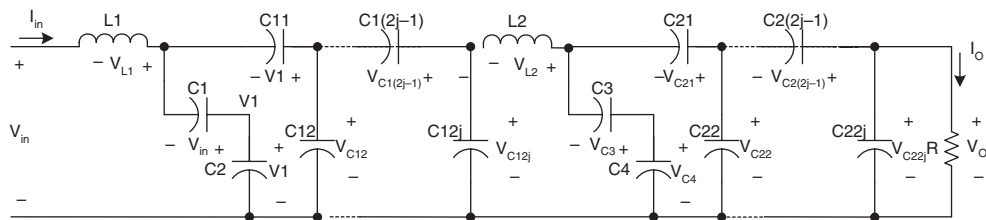
All circuits of positive output super-lift Luo-converters — multiple-enhanced series — are derived from the corresponding circuits of the main series by adding the DEC multiple (j) times in each stage circuit. The first three stages of this series are shown in Figure 3.13 through Figure 3.15. For convenience they are called elementary multiple-enhanced circuits, re-lift multiple-enhanced circuits, and triple-lift multiple-enhanced circuits respectively, and numbered as $n = 1, 2$, and 3.



(a) Circuit diagram



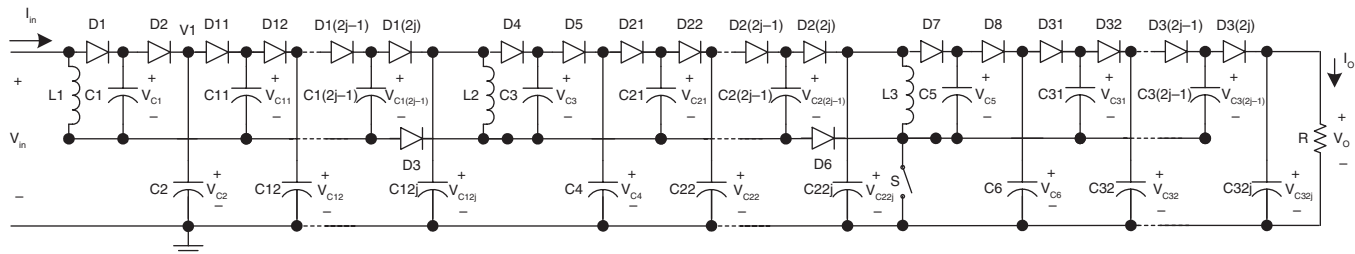
(b) Equivalent circuit during switching-on



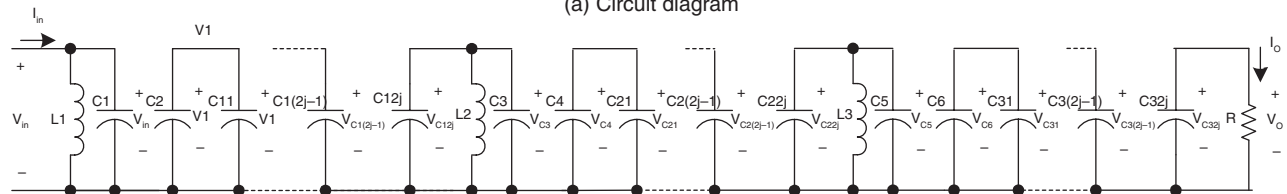
(c) Equivalent circuit during switching-off

FIGURE 3.14

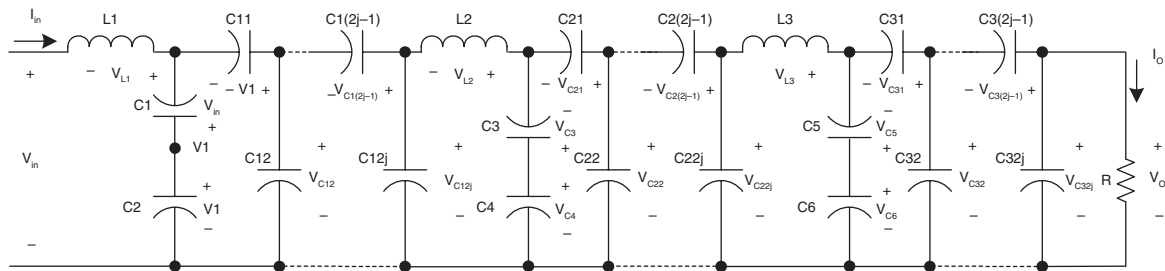
Re-lift multiple-enhanced circuit.



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 3.15

Triple-lift multiple-enhanced circuit.

3.6.1 Elementary Multiple-Enhanced Circuit

This circuit is derived from the elementary circuit of the main series by adding the DEC multiple (j) times. Its circuit and switch-on and -off equivalent circuits are shown in Figure 3.13. The output voltage is

$$V_O = \frac{j+2-k}{1-k} V_{in} \quad (3.89)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{j+2-k}{1-k} \quad (3.90)$$

Following relations are obtained:

$$i_{in-off} = I_{L1} = i_{C11-off} + i_{C1-off} = \frac{2I_O}{1-k} \quad i_{in-on} = i_{L1-on} + i_{C1-on} = I_{L1} + \frac{I_O}{k}$$

$$i_{C1-on} = \frac{1-k}{k} i_{C1-off} = \frac{I_O}{k} \quad i_{C1-off} = i_{C2-off} = \frac{I_O}{1-k}$$

$$i_{C2-off} = \frac{k}{1-k} i_{C2-on} = \frac{k}{1-k} i_{C11-on} = \frac{I_O}{1-k} \quad i_{C11-on} = \frac{1-k}{k} i_{C11-off} = \frac{I_O}{k}$$

$$i_{C11-off} = I_O + i_{C12-off} = I_O + \frac{k}{1-k} i_{C12-on} = \frac{I_O}{1-k} \quad i_{C12-off} = \frac{k}{1-k} i_{C12-on} = \frac{kI_O}{1-k}$$

If inductance L_1 is large enough, i_{L1} is nearly equal to its average current I_{L1} . Therefore,

$$i_{in-off} = I_{L1} = \frac{2I_O}{1-k} \quad i_{in-on} = I_{L1} + \frac{I_O}{k} = \left(\frac{2}{1-k} + \frac{1}{k}\right)I_O = \frac{1+k}{k(1-k)}I_O$$

Verification:

$$I_{in} = ki_{in-on} + (1-k)i_{in-off} = \left(\frac{1+k}{1-k} + 2\right)I_O = \frac{3-k}{1-k}I_O$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation of current i_{L1} is

$$\Delta i_{L1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1 I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_1} \quad (3.91)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12j}} = \frac{I_O(1-k)T}{C_{12j}} = \frac{1-k}{fC_{12j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{12j}} \quad (3.92)$$

3.6.2 Re-Lift Multiple-Enhanced Circuit

This circuit is derived from the re-lift circuit of the main series by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 3.14](#). The voltage across capacitor C_{12j} is

$$V_{C12j} = \frac{j+2-k}{1-k} V_{in} \quad (3.93)$$

The output voltage across capacitor C_{22j} is

$$V_O = V_{C22j} = \left(\frac{j+2-k}{1-k}\right)^2 V_{in} \quad (3.94)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^2 \quad (3.95)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_O} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \quad (3.96)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \quad (3.97)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22j}} = \frac{I_O(1-k)T}{C_{22j}} = \frac{1-k}{fC_{22j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{22j}} \quad (3.98)$$

3.6.3 Triple-Lift Multiple-Enhanced Circuit

This circuit is derived from the triple-lift circuit of the main series by adding the DEC multiple (j) times in each stage circuit. Its circuit and switch-on and -off equivalent circuits are shown in [Figure 3.15](#). The voltage across capacitor C_{12j} is

$$V_{C12j} = \frac{j+2-k}{1-k} V_{in} \quad (3.99)$$

The voltage across capacitor C_{22j} is

$$V_{C22j} = \left(\frac{j+2-k}{1-k} \right)^2 V_{in} \quad (3.100)$$

Same analysis,

$$V_O = \frac{j+2-k}{1-k} V_{C22j} = \left(\frac{j+2-k}{1-k}\right)^3 V_{in} \quad (3.101)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^3 \quad (3.102)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{(2-k)(3-k)}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_O}{I_O} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L1} through inductor L_1 is

$$\begin{aligned} \xi_1 &= \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_O} \\ &= \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_O} \frac{(1-k)^3}{(2-k)^2(3-k)} V_O = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \end{aligned} \quad (3.103)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\begin{aligned} \xi_2 &= \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_O} \\ &= \frac{k(1-k)^2 T}{2(3-k)L_2 I_O} \frac{(1-k)^2}{(2-k)(3-k)} V_O = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \end{aligned} \quad (3.104)$$

The variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3} / 2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3I_O} = \frac{k(1-k)T}{4L_3I_O} \frac{1-k}{3-k} V_O = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \quad (3.105)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32j}} = \frac{I_O(1-k)T}{C_{32j}} = \frac{1-k}{fC_{32j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{32j}} \quad (3.106)$$

3.6.4 Higher Order Lift Multiple-Enhanced Circuit

Higher order lift multiple-enhanced circuits can be derived from the corresponding circuit of the main series converters by adding the DEC multiple (j) times in each stage circuit. For the n^{th} order lift additional circuit, the final output voltage is

$$V_O = \left(\frac{j+2-k}{1-k} \right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{j+2-k}{1-k} \right)^n \quad (3.107)$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{L_i} / 2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \quad (3.108)$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \leq 0 \end{cases} \quad \text{is the Hong function}$$

and

$$u(x) = \begin{cases} 1 & x \geq 0 \\ 0 & x < 0 \end{cases} \quad \text{is the **unit-step function**}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{n2j}} \quad (3.109)$$

3.7 Summary of Positive Output Super-Lift Luo-Converters

All circuits of positive output super-lift Luo-converters can be shown in [Figure 3.16](#) as the family tree. From the analysis in previous sections, the common formula to calculate the output voltage is presented:

$$V_o = \begin{cases} \left(\frac{2-k}{1-k}\right)^n V_{in} & \text{main_series} \\ \left(\frac{2-k}{1-k}\right)^{n-1} \left(\frac{3-k}{1-k}\right) V_{in} & \text{additional_series} \\ \left(\frac{3-k}{1-k}\right)^n V_{in} & \text{enhanced_series} \\ \left(\frac{4-k}{1-k}\right)^n V_{in} & \text{re-enhanced_series} \\ \left(\frac{j+2-k}{1-k}\right)^n V_{in} & \text{multiple-enhanced_series} \end{cases} \quad (3.110)$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \begin{cases} \left(\frac{2-k}{1-k}\right)^n & \text{main_series} \\ \left(\frac{2-k}{1-k}\right)^{n-1} \left(\frac{3-k}{1-k}\right) & \text{additional_series} \\ \left(\frac{3-k}{1-k}\right)^n & \text{enhanced_series} \\ \left(\frac{4-k}{1-k}\right)^n & \text{re-enhanced_series} \\ \left(\frac{j+2-k}{1-k}\right)^n & \text{multiple-enhanced_series} \end{cases} \quad (3.111)$$

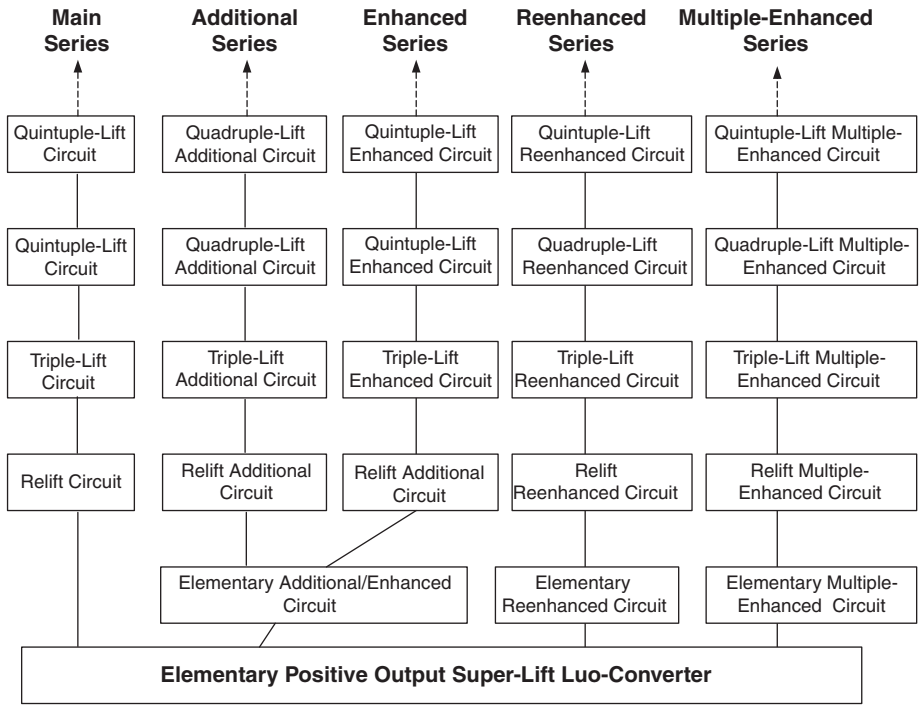


FIGURE 3.16
The family of positive output super-lift Luo-converters.

In order to show the advantages of super-lift Luo-converters, their voltage transfer gains can be compared to that of a buck converter,

$$G = \frac{V_O}{V_{in}} = k$$

forward converter,

$$G = \frac{V_O}{V_{in}} = kN \quad N \text{ is the transformer turns ratio}$$

Cúk-converter,

$$G = \frac{V_O}{V_{in}} = \frac{k}{1-k}$$

fly-back converter,

TABLE 3.1Voltage Transfer Gains of Converters in the Condition $k = 0.2$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.2		
Forward converter		0.2 N (N is the transformer turns ratio)				
Cúk-converter			0.25			
Fly-back converter		0.25 N (N is the transformer turns ratio)				
Boost converter				1.25		
Positive output Luo-converters	1.25	2.5	3.75	5	6.25	$1.25n$
Positive output super-lift Luo-converters — main series	2.25	5.06	11.39	25.63	57.67	2.25^n
Positive output super-lift Luo-converters — additional series	3.5	7.88	17.72	39.87	89.7	$3.5 \cdot 2.25^{(n-1)}$
Positive output super-lift Luo-converters — enhanced series	3.5	12.25	42.88	150	525	3.5^n
Positive output super-lift Luo-converters — re-enhanced series	4.75	22.56	107.2	509	2418	4.75^n
Positive output super-lift Luo-converters — multiple ($j = 4$)- enhanced series	7.25	52.56	381	2762	20,030	7.25^n

$$G = \frac{V_O}{V_{in}} = \frac{k}{1-k} N \quad N \text{ is the transformer turn ratio}$$

boost converter,

$$G = \frac{V_O}{V_{in}} = \frac{1}{1-k}$$

and positive output Luo-converters.

$$G = \frac{V_O}{V_{in}} = \frac{n}{1-k} \quad (3.112)$$

If we assume that the conduction duty k is 0.2, the output voltage transfer gains are listed in [Table 3.1](#).

If the conduction duty k is 0.5, the output voltage transfer gains are listed in [Table 3.2](#).

If the conduction duty k is 0.8, the output voltage transfer gains are listed in [Table 3.3](#).

TABLE 3.2

Voltage Transfer Gains of Converters in the Condition $k = 0.5$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.5		
Forward converter		0.5 N (N is the transformer turns ratio)				
Cúk-converter				1		
Fly-back converter		N (N is the transformer turns ratio)				
Boost converter				2		
Positive output Luo-converters	2	4	6	8	10	$2n$
Positive output super-lift Luo-converters — main series	3	9	27	81	243	3^n
Positive output super-lift Luo-converters — additional series	5	15	45	135	405	$5 \cdot 3^{(n-1)}$
Positive output super-lift Luo-converters — enhanced series	5	25	125	625	3125	5^n
Positive output super-lift Luo-converters — re-enhanced series	7	49	343	2401	16,807	7^n
Positive output super-lift Luo-converters — multiple ($j = 4$)- enhanced series	11	121	1331	14,641	$16 \cdot 10^4$	11^n

TABLE 3.3

Voltage Transfer Gains of Converters in the Condition $k = 0.8$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.8		
Forward converter		0.8 N (N is the transformer turns ratio)				
Cúk-converter				4		
Fly-back converter		$4 N$ (N is the transformer turns ratio)				
Boost converter				5		
Positive output Luo-converters	5	10	15	20	25	$5n$
Positive output super-lift Luo-converters — main series	6	36	216	1296	7776	6^n
Positive output super-lift Luo-converters — additional series	11	66	396	2376	14,256	$11 \cdot 6^{(n-1)}$
Positive output super-lift Luo-converters — enhanced series	11	121	1331	14,641	$16 \cdot 10^4$	11^n
Positive output super-lift Luo-converters — re-enhanced series	16	256	4096	65,536	$104 \cdot 10^4$	16^n
Positive output super-lift Luo-converters — multiple ($j = 4$)- enhanced series	26	676	17,576	$46 \cdot 10^4$	$12 \cdot 10^6$	26^n

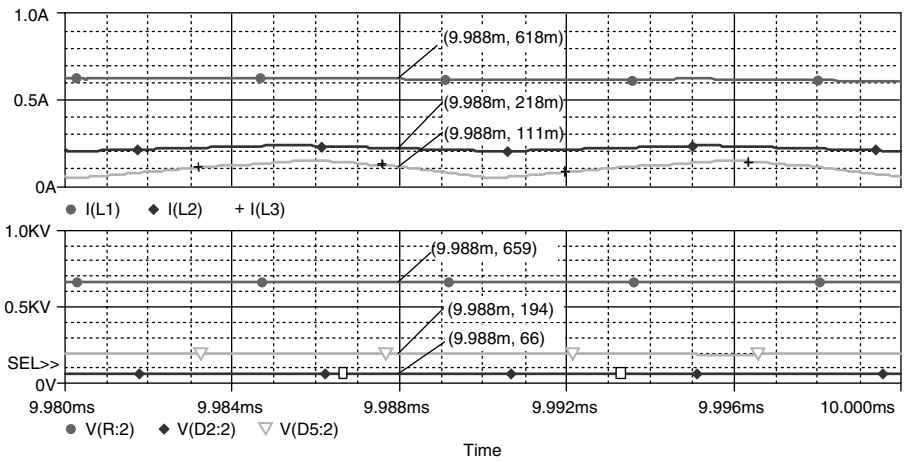


FIGURE 3.17

The simulation results of triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

3.8 Simulation Results

To verify the design and calculation results, the PSpice simulation package was applied to these converters. Choosing $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F, and $R = 30$ k Ω , and using $k = 0.5$ and $f = 100$ kHz.

3.8.1 Simulation Results of a Triple-Lift Circuit

The voltage values V_1 , V_2 and V_O of a triple-lift circuit are 66 V, 194 V, and 659 V respectively and inductor current waveforms are i_{L1} (its average value $I_{L1} = 618$ mA), i_{L2} , and i_{L3} . The simulation results are shown in Figure 3.17. The voltage values are matched to the calculated results.

3.8.2 Simulation Results of a Triple-Lift Additional Circuit

The voltage values V_1 , V_2 , V_3 , and V_O of the triple-lift additional circuit are 57 V, 165 V, 538 V, and 910 V respectively and current waveforms are i_{L1} (its average value $I_{L1} = 1.8$ A), i_{L2} , and i_{L3} . The simulation results are shown in Figure 3.18. The voltage values are matched to the calculated results.

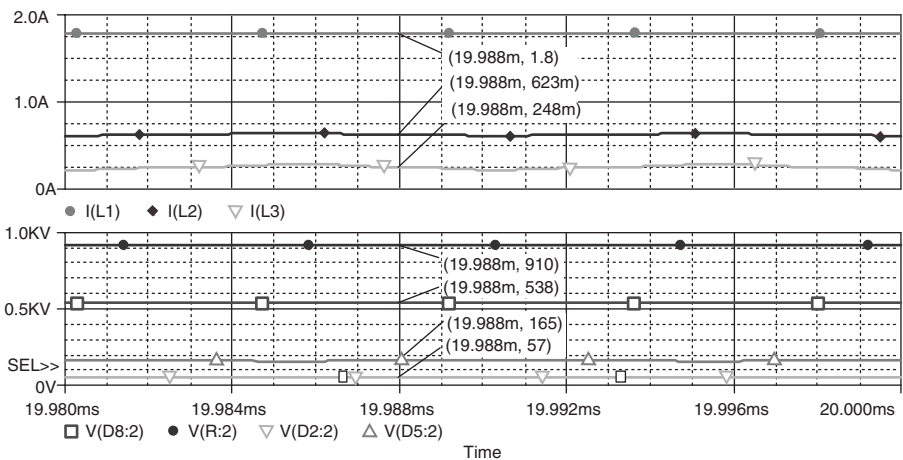


FIGURE 3.18 Simulation results of triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

3.9 Experimental Results

A test rig was constructed to verify the design and calculation results, and compare with PSpice simulation results. The testing conditions were the same: $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F and $R = 30$ k Ω , and using $k = 0.5$ and $f = 100$ kHz. The component of the switch is a MOSFET device IRF950 with the rates 950 V/5 A/2 MHz. The values of the output voltage and first inductor current are measured in the following converters.

3.9.1 Experimental Results of a Triple-Lift Circuit

After careful measurement, the current value of $I_{L1} = 0.62$ A (shown in channel 1 with 1 A/Div) and voltage value of $V_O = 660$ V (shown in channel 2 with 200 V/Div). The experimental results (current and voltage values) are shown in Figure 3.19, that are identically matched to the calculated and simulation results, which are $I_{L1} = 0.618$ A and $V_O = 659$ V shown in Figure 3.17.

3.9.2 Experimental Results of a Triple-Lift Additional Circuit

The experimental results of the current value of $I_{L1} = 1.8$ A (shown in channel 1 with 1 A/Div) and voltage value of $V_O = 910$ V (shown in channel 2 with

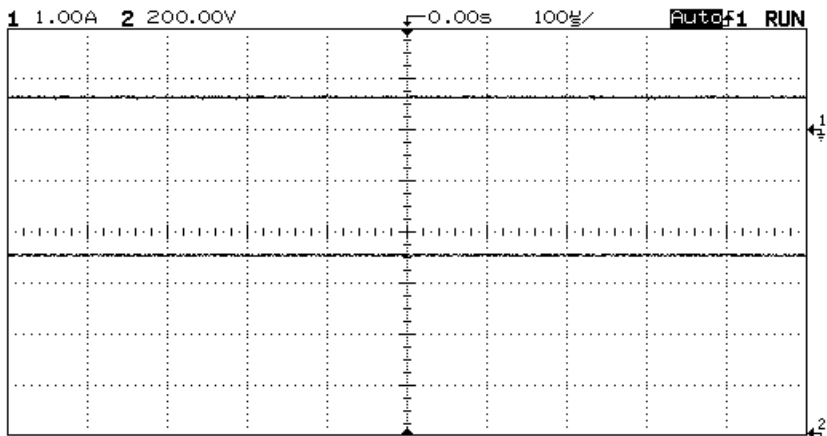


FIGURE 3.19

The experimental results of triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

TABLE 3.4

Comparison of Simulation and Experimental Results of a Triple-Lift Circuit

Stage No. (n)	I_{L1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_O (V)	P_O (W)	η (%)
Simulation results	0.618	0.927	20	18.54	659	14.47	78
Experimental results	0.62	0.93	20	18.6	660	14.52	78

TABLE 3.5

Comparison of Simulation and Experimental Results of a Triple-Lift Additional Circuit

Stage No. (n)	I_{L1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_O (V)	P_O (W)	η (%)
Simulation results	1.8	2.7	20	54	910	27.6	51
Experimental results	1.8	2.7	20	54	910	27.6	51

200 V/Div) are shown in [Figure 3.20](#) that are identically matched to the calculated and simulation results, which are $I_{L1} = 1.8$ A and $V_O = 910$ V shown in [Figure 3.18](#).

3.9.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully, but efficiency, particularly, the efficiencies of the tested circuits is 51 to 78%, which is good for high voltage output equipment. Comparison of the simulation and experimental results, which are listed in the Tables 3.4 and 3.5, demonstrates that all results are well identified each other.

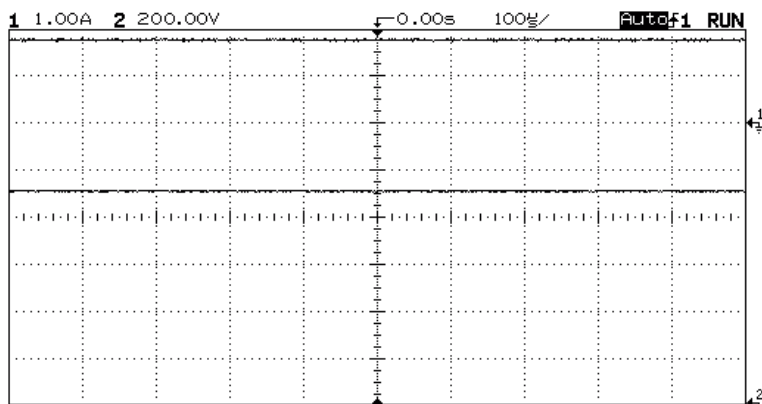


FIGURE 3.20

Experimental results of triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

Usually, there is high inrush current during the initial power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick in only few milliseconds.

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Negative Output Super-Lift Luo-Converters

Along with the positive output super-lift Luo-converters, negative output (N/O) super-lift Luo-converters have also been developed. They perform super-lift technique as well.

4.1 Introduction

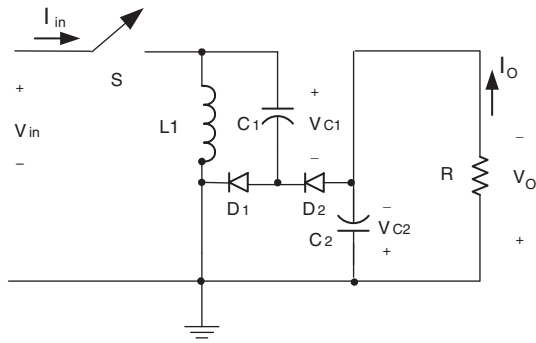
Negative output super-lift Luo-converters are sorted into several sub-series:

- Main series — Each circuit of the main series has one switch S , n inductors, $2n$ capacitors and $(3n - 1)$ diodes.
- Additional series — Each circuit of the additional series has one switch S , n inductors, $2(n + 1)$ capacitors and $(3n + 1)$ diodes.
- Enhanced series — Each circuit of the enhanced series has one switch S , n inductors, $4n$ capacitors and $(5n + 1)$ diodes.
- Re-enhanced series — Each circuit of the re-enhanced series has one switch S , n inductors, $6n$ capacitors and $(7n + 1)$ diodes.
- Multiple-enhanced series — Each circuit of the multiple-enhanced series has one switch S , n inductors, $2(n + j + 1)$ capacitors and $(3n + 2j + 1)$ diodes.

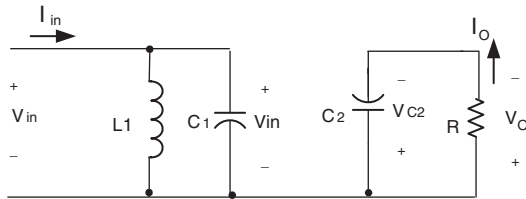
All analyses in this section are based on the condition of steady state operation with continuous conduction mode (CCM).

The conduction duty ratio is k , switch period $T = 1/f$ (f is the switch frequency), the load is resistive load R . The input voltage and current are V_{in} and I_{in} , output voltage and current are V_O and I_O . Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_O \times I_O$. The voltage transfer gain is G :

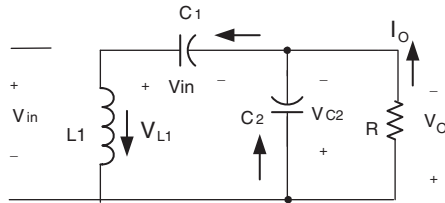
$$G = \frac{V_O}{V_{in}}$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

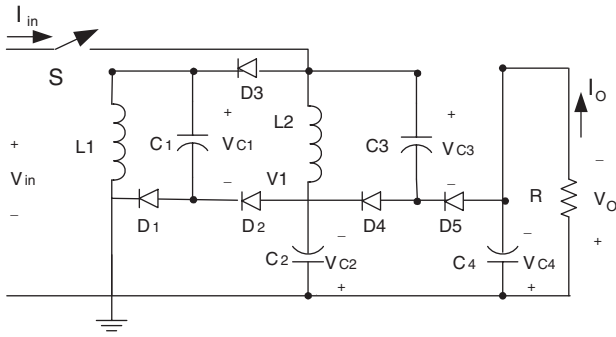
FIGURE 4.1
N/O elementary circuit.

4.2 Main Series

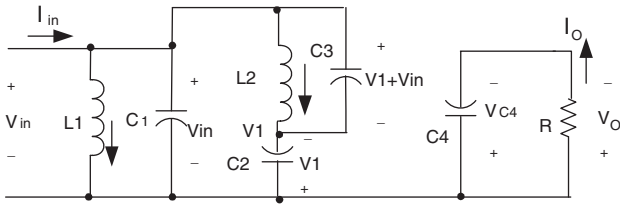
The first three stages of negative output super-lift Luo-converters — main series — are shown in Figure 4.1 to Figure 4.3. For convenience they are called elementary circuits, re-lift circuits, and triple-lift circuits respectively, and numbered as $n = 1, 2$ and 3 .

4.2.1 Elementary Circuit

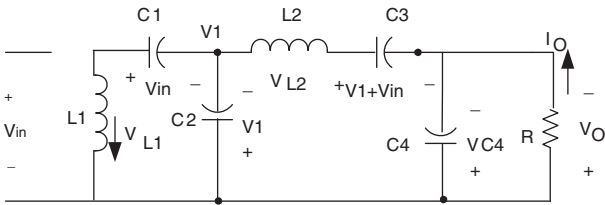
N/O elementary circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 4.1. The voltage across capacitor C_1 is charged



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

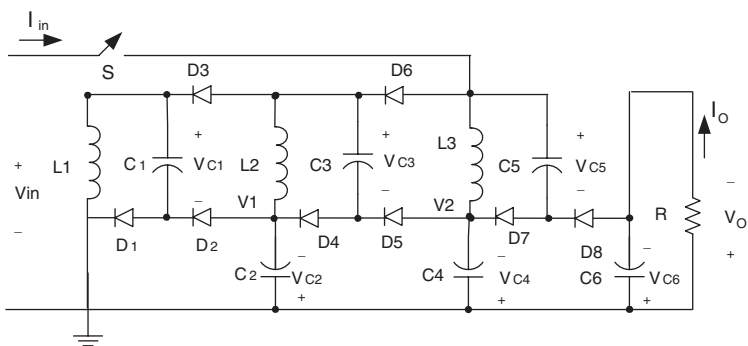
FIGURE 4.2

N/O re-lift circuit.

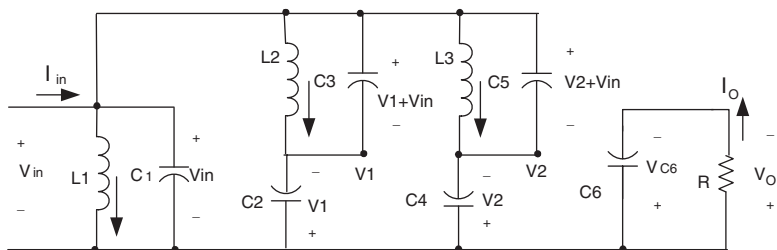
to V_{in} . The current flowing through inductor L_1 increases with slop V_{in}/L_1 during switch-on period kT and decreases with slop $-(V_O - V_{in})/L_1$ during switch-off $(1 - k)T$. Therefore, the variation of current i_{L1} is

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_O - V_{in}}{L_1} (1 - k)T \quad (4.1)$$

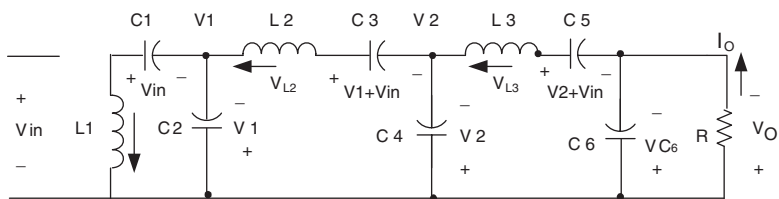
$$V_O = \frac{1}{1 - k} V_{in} = \left(\frac{2 - k}{1 - k} - 1 \right) V_{in} \quad (4.2)$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.3
N/O triple-lift circuit.

The voltage transfer gain is

$$G_1 = \frac{V_O}{V_{in}} = \frac{2-k}{1-k} - 1 \quad (4.3)$$

In steady-state, the average charge across capacitor C_1 in a period should be zero. The relations are available:

$$kTi_{C1-on} = (1-k)Ti_{C1-off} \quad \text{and} \quad i_{C1-on} = \frac{1-k}{k}i_{C1-off}$$

This relation is available for all capacitor's current in switch-on and switch-off periods. The input current i_{in} is equal to $(i_{L1} + i_{C1})$ during switch-on, and zero during switch-off. Capacitor current i_{C1} is equal to i_{L1} during switch-off.

$$i_{in-on} = i_{L1-on} + i_{C1-on} \quad i_{L1-off} = i_{C1-off} = I_{L1}$$

If inductance L_1 is large enough, i_{L1} is nearly equal to its average current I_{L1} . Therefore,

$$i_{in-on} = i_{L1-on} + i_{C1-on} = i_{L1-on} + \frac{1-k}{k} i_{C1-off} = (1 + \frac{1-k}{k}) I_{L1} = \frac{1}{k} I_{L1}$$

and

$$I_{in} = k i_{in-on} = I_{L1} \quad (4.4)$$

Further

$$i_{C2-on} = I_O \quad i_{C2-off} = \frac{k}{1-k} I_O$$

$$I_{L1} = i_{C2-off} + I_O = \frac{k}{1-k} i_{C2-on} + I_O = \frac{1}{1-k} I_O$$

Variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{2L_1 I_O} = \frac{k(1-k)}{G_1} \frac{R}{2fL_1} \quad (4.5)$$

Usually ξ_1 is small (much lower than unity), it means this converter works in the continuous conduction mode (CCM). The ripple voltage of output voltage v_o is

$$\Delta v_O = \frac{\Delta Q}{C_2} = \frac{I_O(1-k)T}{C_2} = \frac{1-k}{fC_2} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_2} \quad (4.6)$$

Usually R is in $k\Omega$, f in 10 kHz, and C_2 in μF , this ripple is very small.

4.2.2 N/O Re-Lift Circuit

N/O re-lift circuit is derived from N/O elementary circuit by adding the parts (L_2 - D_3 - D_4 - D_5 - C_3 - C_4). Its circuit diagram and equivalent circuits during switch-on and -off are shown in Figure 4.2. The voltage across capacitor C_1 is charged to V_{in} . As described in previous section the voltage V_1 across capacitor C_2 is

$$V_1 = \frac{1}{1-k} V_{in}$$

The voltage across capacitor C_3 is charged to $(V_1 + V_{in})$. The current flowing through inductor L_2 increases with slop $(V_1 + V_{in})/L_2$ during switch-on period kT and decreases with slop $-(V_O - 2V_1 - V_{in})/L_2$ during switch-off $(1-k)T$. Therefore, the variation of current i_{L2} is

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{V_O - 2V_1 - V_{in}}{L_2} (1-k)T \quad (4.7)$$

$$V_O = \frac{(2-k)V_1 + V_{in}}{1-k} = \left[\left(\frac{2-k}{1-k} \right)^2 - 1 \right] V_{in} \quad (4.8)$$

The voltage transfer gain is

$$G_2 = \frac{V_O}{V_{in}} = \left(\frac{2-k}{1-k} \right)^2 - 1 \quad (4.9)$$

The input current i_{in} is equal to $(i_{L1} + i_{C1} + i_{L2} + i_{C3})$ during switch-on, and zero during switch-off. In steady-state, the following relations are available:

$$i_{in-on} = i_{L1-on} + i_{C1-on} + i_{L2-on} + i_{C3-on}$$

$$i_{C4-on} = I_O$$

$$i_{C4-off} = \frac{k}{1-k} I_O$$

$$i_{C3-off} = I_{L2} = I_O + i_{C4-off} = \frac{I_O}{1-k}$$

$$i_{C3-on} = \frac{I_O}{k}$$

$$i_{C2-on} = I_{L2} + i_{C3-on} = \frac{I_O}{1-k} + \frac{I_O}{k} = \frac{I_O}{k(1-k)}$$

$$i_{C2-off} = \frac{I_O}{(1-k)^2}$$

$$i_{C1-off} = I_{L1} = I_{L2} + i_{C2-off} = \frac{I_O}{1-k} + \frac{I_O}{(1-k)^2} = \frac{2-k}{(1-k)^2} I_O \quad i_{C1-on} = \frac{2-k}{k(1-k)} I_O$$

Thus

$$i_{in-on} = i_{L1-on} + i_{C1-on} + i_{L2-on} + i_{C3-on} = \frac{1}{k} (I_{L1} + I_{L2}) = \frac{3-2k}{k(1-k)^2} I_O$$

Therefore

$$I_{in} = k i_{in-on} = \frac{3-2k}{(1-k)^2} I_O$$

Since

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{2-k}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{1-k} \frac{kT}{L_2} V_{in} \quad I_{L2} = \frac{1}{1-k} I_O$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_{in}}{\frac{2-k}{(1-k)^2} 2L_1 I_O} = \frac{k(1-k)^2}{(2-k)G_2} \frac{R}{2fL_1} \quad (4.10)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(2-k)TV_{in}}{2L_2 I_O} = \frac{k(2-k)}{G_2} \frac{R}{2fL_2} \quad (4.11)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_4} = \frac{I_O(1-k)T}{C_4} = \frac{1-k}{fC_4} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_4} \quad (4.12)$$

4.2.3 N/O Triple-Lift Circuit

N/O triple-lift circuit is derived from N/O re-lift circuit by double adding the parts (L_2 - D_3 - D_4 - D_5 - C_3 - C_4). Its circuit diagram and equivalent circuits during switch-on and -off are shown in Figure 4.3. The voltage across capacitor C_1 is charged to V_{in} . As described in previous section the, voltage V_1 across capacitor C_2 is $V_1 = ((2-k)/(1-k)-1)V_{in} = (1/1-k)V_{in}$, and voltage V_2 across capacitor C_4 is $V_2 = [(2-k/1-k)^2 - 1]V_{in} = (3-2k/(1-k)^2)V_{in}$.

The voltage across capacitor C_5 is charged to $(V_2 + V_{in})$. The current flowing through inductor L_3 increases with slop $(V_2 + V_{in})/L_3$ during switch-on period kT and decreases with slop $-(V_O - 2V_2 - V_{in})/L_3$ during switch-off $(1-k)T$. Therefore, the variation of current i_{L3} is

$$\Delta i_{L3} = \frac{V_2 + V_{in}}{L_3} kT = \frac{V_O - 2V_2 - V_{in}}{L_3} (1-k)T \quad (4.13)$$

$$V_O = \frac{(2-k)V_2 + V_{in}}{1-k} = [(\frac{2-k}{1-k})^3 - 1]V_{in} \quad (4.14)$$

The voltage transfer gain is

$$G_3 = \frac{V_O}{V_{in}} = \left(\frac{2-k}{1-k} \right)^3 - 1 \quad (4.15)$$

The input current i_{in} is equal to $(i_{L1} + i_{C1} + i_{L2} + i_{C3} + i_{L3} + i_{C5})$ during switch-on, and zero during switch-off. In steady state, the following relations are available:

$$i_{in-on} = i_{L1-on} + i_{C1-on} + i_{L2-on} + i_{C3-on} + i_{L3-on} + i_{C5-on}$$

$$i_{C6-on} = I_O$$

$$i_{C6-off} = \frac{k}{1-k} I_O$$

$$i_{C5-off} = I_{L3} = I_O + i_{C6-off} = \frac{I_O}{1-k}$$

$$i_{C5-on} = \frac{I_O}{k}$$

$$i_{C4-on} = I_{L3} + i_{C5-on} = \frac{I_O}{1-k} + \frac{I_O}{k} = \frac{I_O}{k(1-k)}$$

$$i_{C4-off} = \frac{I_O}{(1-k)^2}$$

$$i_{C3-off} = I_{L2} = I_{L3} + i_{C4-off} = \frac{2-k}{(1-k)^2} I_O$$

$$i_{C3-on} = \frac{2-k}{k(1-k)} I_O$$

$$i_{C2-on} = I_{L2} + i_{C3-on} = \frac{2-k}{k(1-k)^2} I_O$$

$$i_{C2-off} = \frac{2-k}{(1-k)^3} I_O$$

$$i_{C1-off} = I_{L1} = I_{L2} + i_{C2-off} = \frac{(2-k)^2}{(1-k)^3} I_O$$

$$i_{C1-on} = \frac{(2-k)^2}{k(1-k)^2} I_O$$

Thus

$$\begin{aligned} i_{in-on} &= i_{L1-on} + i_{C1-on} + i_{L2-on} + i_{C3-on} + i_{L3-on} + i_{C5-on} \\ &= \frac{1}{k} (I_{L1} + I_{L2} + I_{L3}) = \frac{7-9k+3k^2}{k(1-k)^3} I_O \end{aligned}$$

Therefore

$$I_{in} = k i_{in-on} = \frac{7-9k+3k^2}{(1-k)^3} I_O = [(\frac{2-k}{1-k})^3 - 1] I_O$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT$$

$$I_{L1} = \frac{(2-k)^2}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{(1-k)L_2} kTV_{in}$$

$$I_{L2} = \frac{2-k}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2 + V_{in}}{L_3} kT = (\frac{2-k}{1-k})^2 \frac{kT}{L_3} V_{in}$$

$$I_{L3} = \frac{I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)^2 L_1 I_O} = \frac{k(1-k)^3}{(2-k)^2 G_3} \frac{R}{2fL_1} \quad (4.16)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k) TV_{in}}{2L_2 I_O} = \frac{k(1-k)}{G_3} \frac{R}{2fL_2} \quad (4.17)$$

The variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(2-k)^2 TV_{in}}{2(1-k)L_3 I_O} = \frac{k(2-k)^2}{(1-k)G_3} \frac{R}{2fL_3} \quad (4.18)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_6} = \frac{I_O(1-k)T}{C_6} = \frac{1-k}{fC_6} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_6} \quad (4.19)$$

4.2.4 N/O Higher Order Lift Circuit

N/O higher order lift circuits can be designed by repeating the parts (L_2 - D_3 - D_4 - D_5 - C_3 - C_4) multiple times. For n th order lift circuit, the final output voltage across capacitor C_{2n} is

$$V_O = \left[\left(\frac{2-k}{1-k} \right)^n - 1 \right] V_{in} \quad (4.20)$$

The voltage transfer gain is

$$G_n = \frac{V_O}{V_{in}} = \left(\frac{2-k}{1-k} \right)^n - 1 \quad (4.21)$$

The variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^n}{(2-k)^{(n-1)}G_n} \frac{R}{2fL_i} \quad (4.22)$$

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(2-k)^{(3-n)}}{(1-k)^{(n-3)}G_n} \frac{R}{2fL_i} \quad (4.23)$$

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(2-k)^{(n-i+2)}}{(1-k)^{(n-i+1)}G_n} \frac{R}{2fL_3} \quad (4.24)$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{2n}} \quad (4.25)$$

4.3 Additional Series

All circuits of negative output super-lift Luo-converters — additional series — are derived from the corresponding circuits of the main series by adding a double/enhanced circuit (DEC). The first three stages of this series are shown in Figure 4.4 to Figure 4.6. For convenience they are called elementary additional circuits, re-lift additional circuit, and triple-lift additional circuit respectively, and numbered as $n = 1, 2$ and 3 .

4.3.1 N/O Elementary Additional Circuit

This circuit is derived from the N/O elementary circuit by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 4.4. The voltage across capacitor C_1 is charged to V_{in} . The voltage across capacitor C_2 is charged to V_1 and C_{11} is charged to $(V_1 + V_{in})$. The current i_{L1} flowing through inductor L_1 increases with slope V_{in}/L_1 during switch-on period kT and decreases with slope $-(V_1 - V_{in})/L_1$ during switch-off $(1-k)T$.

Therefore,

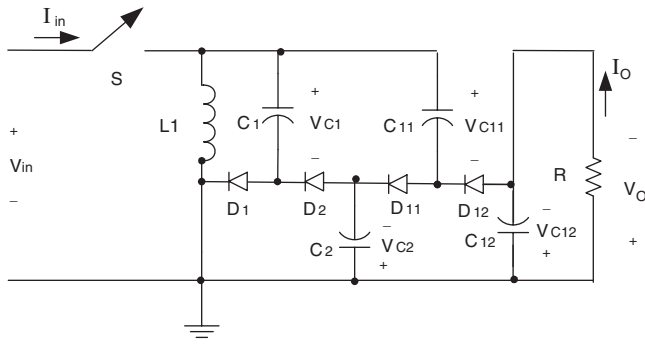
$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1} (1-k)T \quad (4.26)$$

$$V_1 = \frac{1}{1-k} V_{in} = \left(\frac{2-k}{1-k} - 1 \right) V_{in}$$

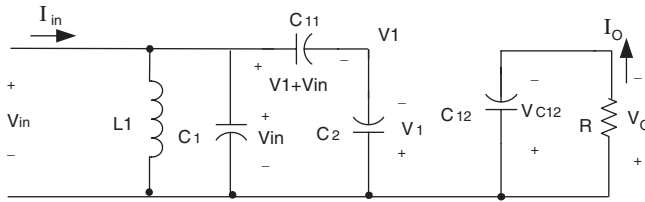
$$V_{L1-off} = \frac{k}{1-k} V_{in}$$

The output voltage is

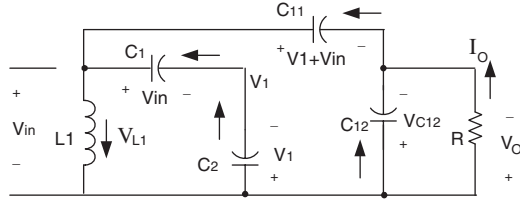
$$V_o = V_{in} + V_{L1} + V_1 = \frac{2}{1-k} V_{in} = \left[\frac{3-k}{1-k} - 1 \right] V_{in} \quad (4.27)$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.4

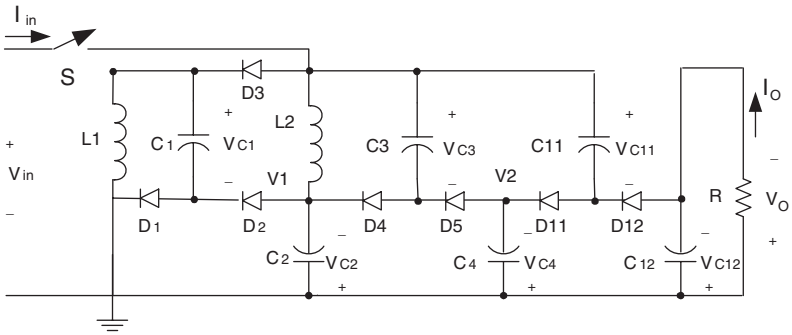
N/O elementary additional (enhanced) circuit.

The voltage transfer gain is

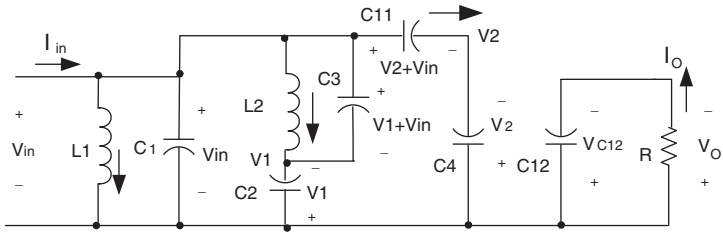
$$G_1 = \frac{V_O}{V_{in}} = \frac{3-k}{1-k} - 1 \quad (4.28)$$

Following relations are obtained:

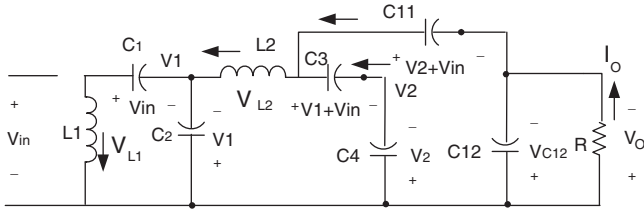
$$i_{C12-on} = I_O \quad i_{C12-off} = \frac{kI_O}{1-k}$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.5

N/O re-lift additional circuit.

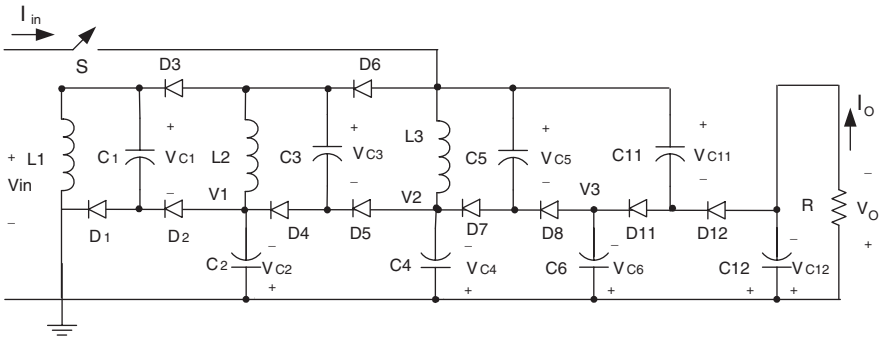
$$i_{C11-off} = I_O + i_{C12-off} = \frac{I_O}{1-k}$$

$$i_{C11-on} = i_{C2-on} = \frac{I_O}{k}$$

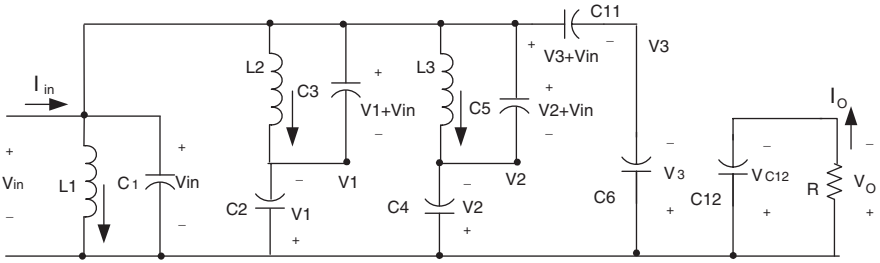
$$i_{C2-off} = i_{C1-off} = \frac{I_O}{1-k}$$

$$i_{C1-on} = \frac{I_O}{k}$$

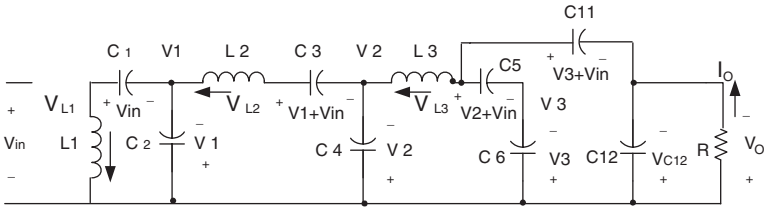
$$I_{L1} = i_{C1-off} + i_{C11-on} = \frac{2I_O}{1-k}$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.6

N/O triple-lift additional circuit.

$$i_{in} = I_{L1} + i_{C1-on} + i_{C11-on} = \left(\frac{2}{1-k} + \frac{1}{k} + \frac{1}{k} \right) I_O = \frac{2}{k(1-k)} I_O$$

Therefore,

$$I_{in} = k i_{in} = \frac{2}{1-k} I_O = \left[\frac{3-k}{1-k} - 1 \right] I_O$$

The variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1 I_O} = \frac{k(1-k)}{2G_1} \frac{R}{2fL_1} \quad (4.29)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (4.30)$$

4.3.2 N/O Re-Lift Additional Circuit

The N/O re-lift additional circuit is derived from the N/O re-lift circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 4.5](#). The voltage across capacitor C_1 is charged to v_{in} . As described in a previous section the voltage across C_2 is

$$V_1 = \frac{1}{1-k} V_{in}$$

The voltage across capacitor C_3 is charged to $(V_1 + V_{in})$, voltage across capacitor C_4 is charged to V_2 and voltage across capacitor C_{11} is charged to $(V_2 + V_{in})$. The current flowing through inductor L_2 increases with voltage $(V_1 + V_{in})$ during switch-on kT and decreases with voltage $-(V_2 - 2V_1 - V_{in})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{V_2 - 2V_1 - V_{in}}{L_2} (1-k)T \quad (4.31)$$

$$V_2 = \frac{(2-k)V_1 + V_{in}}{1-k} = \frac{3-2k}{(1-k)^2} = \left[\left(\frac{2-k}{1-k} \right)^2 - 1 \right] V_{in}$$

and

$$V_{L2-off} = V_2 - 2V_1 - V_{in} = \frac{k(2-k)}{(1-k)^2} V_{in} \quad (4.32)$$

The output voltage is

$$V_O = V_2 + V_{in} + V_{L2} + V_1 = \frac{5-3k}{(1-k)^2} V_{in} = \left[\frac{3-k}{1-k} \frac{2-k}{1-k} - 1 \right] V_{in} \quad (4.33)$$

The voltage transfer gain is

$$G_2 = \frac{V_O}{V_{in}} = \frac{2-k}{1-k} \frac{3-k}{1-k} - 1 \quad (4.34)$$

Following relations are obtained:

$$i_{C12-on} = I_O \quad i_{C12-off} = \frac{kI_O}{1-k}$$

$$i_{C11-off} = I_O + i_{C12-off} = \frac{I_O}{1-k} \quad i_{C11-on} = i_{C4-on} = \frac{I_O}{k}$$

$$i_{C4-off} = i_{C3-off} = \frac{I_O}{1-k} \quad i_{C3-on} = \frac{I_O}{k}$$

$$I_{L2} = i_{C11-off} + i_{C3-off} = \frac{2I_O}{1-k}$$

$$i_{C2-on} = I_{L2} + i_{C3-on} = \frac{1+k}{k(1-k)} I_O \quad i_{C2-off} = \frac{1+k}{(1-k)^2} I_O$$

$$I_{L1} = i_{C1-off} = I_{L2} + i_{C2-off} = \frac{3-k}{(1-k)^2} I_O \quad i_{C1-on} = \frac{3-k}{k(1-k)} I_O$$

$$i_{in} = I_{L1} + i_{C1-on} + i_{C2-on} + i_{C4-on} = \left[\frac{3-k}{(1-k)^2} + \frac{3-k}{k(1-k)} + \frac{1+k}{k(1-k)} + \frac{1}{k} \right] I_O = \frac{5-3k}{k(1-k)^2} I_O$$

Therefore,

$$I_{in} = k i_{in} = \frac{5-3k}{(1-k)^2} I_O = \left[\frac{3-k}{1-k} \frac{2-k}{1-k} - 1 \right] I_O$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_2} kT \quad I_{L1} = \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{(1-k)L_2} kTV_{in} \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_O} = \frac{k(1-k)^2}{(3-k)G_2} \frac{R}{2fL_1} \quad (4.35)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(2-k)TV_{in}}{4L_2 I_O} = \frac{k(2-k)}{2G_2} \frac{R}{2fL_2} \quad (4.36)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (4.37)$$

4.3.3 N/O Triple-Lift Additional Circuit

This circuit is derived from the N/O triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 4.6](#). The voltage across capacitor C_1 is charged to V_{in} . As described in a previous section the voltage across C_2 is

$$V_1 = \frac{1}{1-k} V_{in}$$

and voltage across C_4 is

$$V_2 = \frac{3-2k}{1-k} V_1 = \frac{3-2k}{(1-k)^2} V_{in}$$

The voltage across capacitor C_5 is charged to $(V_2 + V_{in})$, voltage across capacitor C_6 is charged to V_3 and voltage across capacitor C_{11} is charged to $(V_3 + V_{in})$. The current flowing through inductor L_3 increases with voltage

$(V_2 + V_{in})$ during switch-on period kT and decreases with voltage $-(V_3 - 2V_2 - V_{in})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L3} = \frac{V_2 + V_{in}}{L_3} kT = \frac{V_3 - 2V_2 - V_{in}}{L_3} (1 - k)T \quad (4.38)$$

$$V_3 = \frac{(2 - k)V_2 + V_{in}}{1 - k} = \frac{7 - 9k + 3k^2}{(1 - k)^3} V_{in} = \left[\left(\frac{2 - k}{1 - k} \right)^3 - 1 \right] V_{in}$$

and

$$V_{L3-off} = V_3 - 2V_2 - V_{in} = \frac{k(2 - k)^2}{(1 - k)^3} V_{in} \quad (4.39)$$

The output voltage is

$$V_O = V_3 + V_{in} + V_{L3} + V_2 = \frac{11 - 13k + 4k^2}{(1 - k)^3} V_{in} = \left[\frac{3 - k}{1 - k} \left(\frac{2 - k}{1 - k} \right)^2 - 1 \right] V_{in} \quad (4.40)$$

The voltage transfer gain is

$$G_3 = \frac{V_O}{V_{in}} = \left(\frac{2 - k}{1 - k} \right)^2 \frac{3 - k}{1 - k} - 1 \quad (4.41)$$

Following relations are available:

$$i_{C12-on} = I_O \quad i_{C12-off} = \frac{kI_O}{1 - k}$$

$$i_{C11-off} = I_O + i_{C12-off} = \frac{I_O}{1 - k} \quad i_{C11-on} = i_{C6-on} = \frac{I_O}{k}$$

$$i_{C6-off} = i_{C5-off} = \frac{I_O}{1 - k} \quad i_{C5-on} = \frac{I_O}{k}$$

$$I_{L3} = i_{C11-off} + i_{C5-off} = \frac{2I_O}{1 - k}$$

$$i_{C4-on} = I_{L3} + i_{C5-on} = \frac{1 + k}{k(1 - k)} I_O \quad i_{C4-off} = \frac{1 + k}{(1 - k)^2} I_O$$

$$\begin{aligned}
I_{L2} = i_{C3-off} = I_{L3} + i_{C4-off} &= \frac{3-k}{(1-k)^2} I_O & i_{C3-on} &= \frac{3-k}{k(1-k)} I_O \\
i_{C2-on} = I_{L2} + i_{C3-on} &= \frac{3-k}{k(1-k)^2} I_O & i_{C2-off} &= \frac{3-k}{(1-k)^3} I_O \\
I_{L1} = i_{C1-off} = I_{L2} + i_{C2-off} &= \frac{(3-k)(2-k)}{(1-k)^3} I_O & i_{C1-on} &= \frac{(3-k)(2-k)}{k(1-k)^2} I_O \\
i_{in} = I_{L1} + i_{C1-on} + i_{C2-on} + i_{C4-on} + i_{C6-on} \\
&= \left[\frac{(3-k)(2-k)}{(1-k)^3} + \frac{(3-k)(2-k)}{k(1-k)^2} + \frac{3-k}{k(1-k)^2} + \frac{1+k}{k(1-k)} + \frac{1}{k} \right] I_O \\
&= \frac{11-13k+4k^2}{k(1-k)^3} I_O
\end{aligned}$$

Therefore,

$$I_{in} = k i_{in} = \frac{11-13k+4k^2}{(1-k)^3} I_O = \left[\frac{3-k}{1-k} \left(\frac{2-k}{1-k} \right)^2 - 1 \right] I_O$$

Analogously,

$$\begin{aligned}
\Delta i_{L1} &= \frac{V_{in}}{L_2} kT & I_{L1} &= \frac{(2-k)(3-k)}{(1-k)^3} I_O \\
\Delta i_{L2} &= \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{(1-k)L_2} kTV_{in} & I_{L2} &= \frac{3-k}{(1-k)^2} I_O \\
\Delta i_{L3} &= \frac{V_2 + V_{in}}{L_3} kT = \frac{(2-k)^2}{(1-k)^2 L_3} kTV_{in} & I_{L3} &= \frac{2I_O}{1-k}
\end{aligned}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_O} = \frac{k(1-k)^3}{(2-k)(3-k)G_3} \frac{R}{2fL_1} \quad (4.42)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)(2-k)TV_1}{2(3-k)L_2 I_O} = \frac{k(1-k)(2-k)}{(3-k)G_3} \frac{R}{2fL_2} \quad (4.43)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(2-k)^2 TV_{in}}{4(1-k)L_3 I_O} = \frac{k(2-k)^2}{2(1-k)G_3} \frac{R}{2fL_3} \quad (4.44)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (4.45)$$

4.3.4 N/O Higher Order Lift Additional Circuit

Higher order N/O lift additional circuits can be derived from the corresponding circuits of the main series by adding a DEC. Each stage voltage V_i ($i = 1, 2, \dots, n$) is

$$V_i = \left[\left(\frac{2-k}{1-k} \right)^i - 1 \right] V_{in} \quad (4.46)$$

This means V_1 is the voltage across capacitor C_2 , V_2 is the voltage across capacitor C_4 and so on. For n^{th} order lift additional circuit, the final output voltage is

$$V_O = \left[\frac{3-k}{1-k} \left(\frac{2-k}{1-k} \right)^{n-1} - 1 \right] V_{in} \quad (4.47)$$

The voltage transfer gain is

$$G_n = \frac{V_O}{V_{in}} = \frac{3-k}{1-k} \left(\frac{2-k}{1-k} \right)^{n-1} - 1 \quad (4.48)$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^n}{2^{h(1-n)} [(2-k)^{(n-2)} (3-k)]^{u(n-2)} G_n} \frac{R}{fL_1} \quad (4.49)$$

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^{(n-2)}(2-k)}{2^{h(n-2)}(3-k)^{(n-2)}G_n} \frac{R}{2fL_2} \quad (4.50)$$

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(2-k)^{(n-1)}}{2^{h(n-3)}(1-k)^{(n-2)}G_n} \frac{R}{2fL_3} \quad (4.51)$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \leq 0 \end{cases} \text{ is the **Hong function**}$$

and

$$u(x) = \begin{cases} 1 & x \geq 0 \\ 0 & x < 0 \end{cases} \text{ is the **unit-step function**}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12}} \quad (4.52)$$

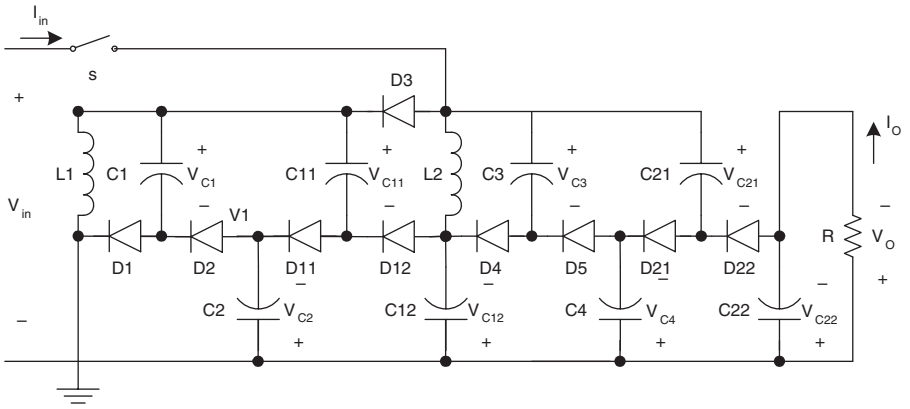
4.4 Enhanced Series

All circuits of the negative output super-lift Luo-converters — enhanced series — are derived from the corresponding circuits of the main series by adding the DEC into each stage circuit of all series converters.

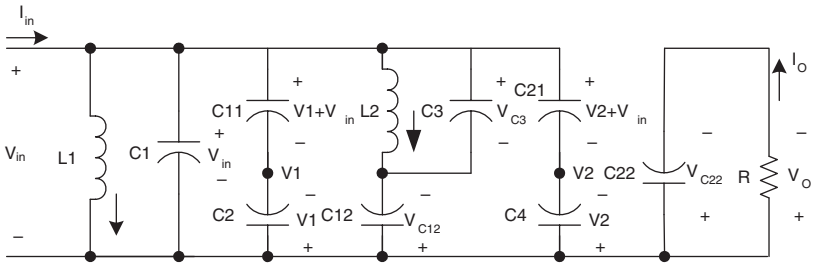
The first three stages of this series are shown in [Figures 4.4, 4.7, and 4.8](#). For convenience they are called elementary enhanced circuits, re-lift enhanced circuits, and triple-lift enhanced circuits respectively, and numbered as $n = 1, 2$ and 3 .

4.4.1 N/O Elementary Enhanced Circuit

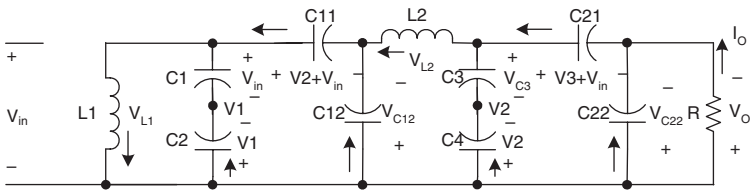
This circuit is derived from N/O elementary circuit with adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 4.4](#).



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.7

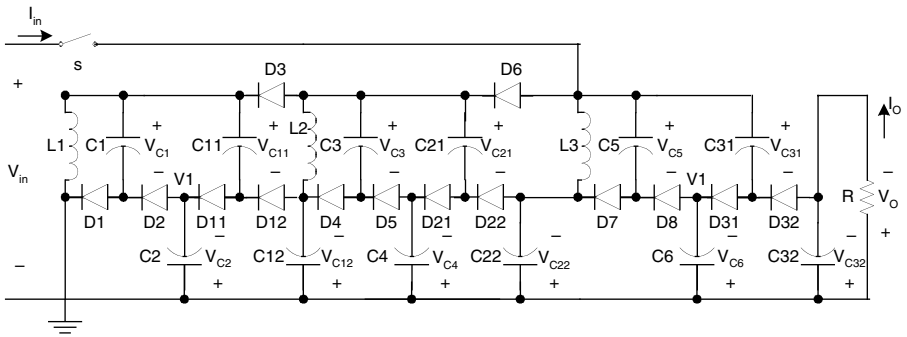
N/O re-lift enhanced circuit.

The output voltage is

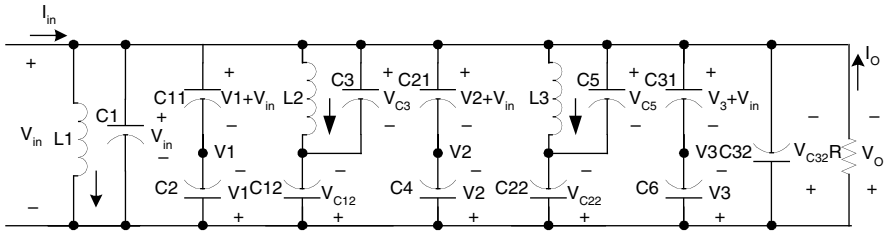
$$V_O = V_{in} + V_{L1} + V_1 = \frac{2}{1-k} V_{in} = \left[\frac{3-k}{1-k} - 1 \right] V_{in} \quad (4.27)$$

The voltage transfer gain is

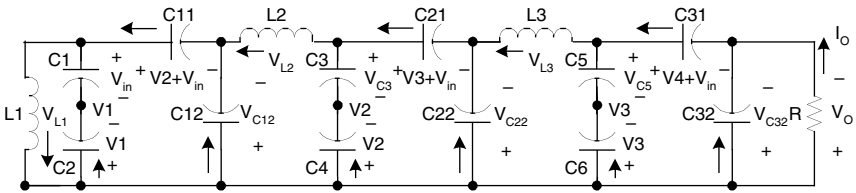
$$G_1 = \frac{V_O}{V_{in}} = \frac{3-k}{1-k} - 1 \quad (4.28)$$



(a) Circuit diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.8

N/O triple-lift enhanced circuit.

4.4.2 N/O Re-Lift Enhanced Circuit

The N/O re-lift enhanced circuit is derived from N/O re-lift circuit of the main series by adding the DEC into each stage. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 4.7. The voltage across capacitor C_{12} is charged to

$$V_{C12} = \frac{3}{1-k} V_{in} \quad (4.53)$$

The voltage across capacitor C_3 is charged to V_{C12} , and the voltage across capacitor C_4 and C_{12} is charged to V_{C4}

$$V_{C4} = \frac{2-k}{1-k} V_{C12} = \frac{2-k}{1-k} \frac{3-k}{1-k} V_{in} \quad (4.54)$$

The current flowing through inductor L_2 increases with voltage V_{C12} during switch-on kT and decreases with voltage $-(V_{C21} - V_{C4} - V_{C12})$ during switch-off $(1-k)T$.

Therefore,

$$\Delta i_{L2} = \frac{kT}{L_2} (V_{C12} - V_{in}) = \frac{V_{C21} - V_{C4} - V_{C12}}{L_2} (1-k)T \quad (4.55)$$

$$V_{C21} = \left(\frac{3-k}{1-k}\right)^2 V_{in}$$

The output voltage is

$$V_O = V_{C21} - V_{in} = \left[\left(\frac{3-k}{1-k}\right)^2 - 1\right] V_{in} \quad (4.56)$$

The voltage transfer gain is

$$G_2 = \frac{V_O}{V_{in}} = \left(\frac{3-k}{1-k}\right)^2 - 1 \quad (4.57)$$

Following relations are obtained:

$$i_{C22-on} = I_O \qquad i_{C22-off} = \frac{kI_O}{1-k}$$

$$i_{C21-off} = I_O + i_{C22-off} = \frac{I_O}{1-k} \qquad i_{C21-on} = i_{C4-on} = \frac{I_O}{k}$$

$$i_{C4-off} = i_{C3-off} = \frac{I_O}{1-k} \qquad i_{C3-on} = \frac{I_O}{k}$$

$$I_{L2} = i_{C21-off} + i_{C3-off} = \frac{2I_O}{1-k}$$

$$i_{C12-on} = I_{L2} + i_{C3-on} = \frac{1+k}{k(1-k)} I_O \qquad i_{C12-off} = \frac{1+k}{(1-k)^2} I_O$$

$$i_{C11-off} = I_{L2} + i_{C12-off} = \frac{3-k}{(1-k)^2} I_O$$

$$i_{C2-off} = \frac{3-k}{(1-k)^2} I_O$$

$$i_{C11-on} = i_{C2-on} = \frac{3-k}{k(1-k)} I_O$$

$$I_{L1} = i_{C11-off} + i_{C2-off} = 2 \frac{3-k}{(1-k)^2} I_O$$

$$i_{C1-on} = \frac{3-k}{k(1-k)} I_O$$

$$i_{in} = I_{L1} + i_{C1-on} + i_{C11-on} + i_{C12-on} + i_{C21-on} = \frac{4(2-k)}{k(1-k)^2} I_O$$

Therefore,

$$I_{in} = k i_{in} = \frac{4(2-k)}{(1-k)^2} I_O = \left[\frac{(3-k)^2}{(1-k)^2} - 1 \right] I_O$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_2} kT$$

$$I_{L1} = 2 \frac{3-k}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_{C12} - V_{in}}{L_2} kT = \frac{2+k}{(1-k)L_2} kTV_{in} \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{4(3-k)L_1 I_O} = \frac{k(1-k)^2}{2(3-k)G_2} \frac{R}{2fL_1} \quad (4.58)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(2+k)TV_{in}}{4L_2 I_O} = \frac{k(2+k)}{2G_2} \frac{R}{2fL_2} \quad (4.59)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{22}} = \frac{I_O(1-k)T}{C_{22}} = \frac{1-k}{fC_{22}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{22}} \quad (4.60)$$

4.4.3 N/O Triple-Lift Enhanced Circuit

This circuit is derived from the N/O triple-lift circuit of main series by adding the DEC into each stage. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 4.8](#). The voltage across capacitor C_{12} is charged to V_{C12} . As described in the previous section the voltage across C_{C12} is

$$V_{C12} = \frac{3-k}{1-k} V_{in}$$

and voltage across C_4 and C_{C22} is

$$V_{C22} = \frac{3-k}{1-k} V_{C12} = \left(\frac{3-k}{1-k}\right)^2 V_{in}$$

The voltage across capacitor C_5 is charged to V_{C22} , voltage across capacitor C_6 is charged to V_{C6}

$$V_{C6} = \frac{2-k}{1-k} V_{C22} = \frac{2-k}{1-k} \left(\frac{3-k}{1-k}\right)^2 V_{in}$$

The current flowing through inductor L_3 increases with voltage V_{C22} during switch-on period kT and decreases with voltage $-(V_{C32} - V_{C6} - V_{C22})$ during switch-off $(1-k)T$.

Therefore,

$$\Delta i_{L3} = \frac{kT}{L_3} (V_{C22} - V_{in}) = \frac{V_{C31} - V_{C6} - V_{C22}}{L_3} (1-k)T \quad (4.61)$$

$$V_{C31} = \left(\frac{3-k}{1-k}\right)^3 V_{in}$$

and

$$V_O = V_{C31} - V_{in} = \left[\left(\frac{3-k}{1-k}\right)^3 - 1\right] V_{in} \quad (4.62)$$

The voltage transfer gain is

$$G_3 = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^2 - 1 \quad (4.63)$$

The following relations are obtained:

$$i_{C32-on} = I_o$$

$$i_{C32-off} = \frac{kI_o}{1-k}$$

$$i_{C31-off} = I_o + i_{C32-off} = \frac{I_o}{1-k}$$

$$i_{C31-on} = i_{C6-on} = \frac{I_o}{k}$$

$$i_{C6-off} = i_{C5-off} = \frac{I_o}{1-k}$$

$$i_{C6-on} = i_{C5-on} = \frac{I_o}{k}$$

$$I_{L3} = i_{C31-off} + i_{C5-off} = \frac{2I_o}{1-k}$$

$$i_{C22-on} = I_{L3} + i_{C5-on} = \frac{1+k}{k(1-k)} I_o$$

$$i_{C22-off} = \frac{1+k}{(1-k)^2} I_o$$

$$i_{C21-off} = i_{C4-off} = I_{L3} + i_{C22-off} = \frac{3-k}{(1-k)^2} I_o$$

$$i_{C4-on} = \frac{3-k}{k(1-k)} I_o$$

$$I_{L2} = i_{C4-off} + i_{C21-off} = 2 \frac{3-k}{(1-k)^2} I_o$$

$$i_{C3-on} = \frac{3-k}{k(1-k)} I_o$$

$$i_{C12-on} = I_{L2} + i_{C3-on} = \frac{(3-k)(2-k)}{k(1-k)^2} I_o$$

$$i_{C12-off} = \frac{(3-k)(2-k)}{(1-k)^3} I_o$$

$$i_{C11-off} = I_{L2} + i_{C12-off} = \frac{(3-k)(4-3k)}{(1-k)^3} I_o$$

$$i_{C11-on} = \frac{(3-k)(4-k)}{k(1-k)^2} I_o$$

$$I_{L1} = i_{C11-off} + i_{C1-off} = 2 \frac{(3-k)(4-k)}{(1-k)^3} I_o$$

$$i_{C1-on} = i_{C2-on} = \frac{(3-k)(4-k)}{k(1-k)^2} I_o$$

$$i_{in} = I_{L1} + i_{C1-on} + i_{C2-on} + i_{C12-on} + i_{C4-on} + i_{C22-on} + i_{C6-on} = \frac{2(13-12k+3k^2)}{k(1-k)^3} I_o$$

Therefore,

$$I_{in} = ki_{in} = 2 \frac{13 - 12k + 3k^2}{(1 - k)^3} I_O = \left[\left(\frac{3 - k}{1 - k} \right)^3 - 1 \right] I_O$$

Analogously:

$$\Delta i_{L1} = \frac{V_{in}}{L_2} kT \quad I_{L1} = \frac{2(4 - k)(3 - k)}{(1 - k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2 - k}{(1 - k)L_2} kTV_{in} \quad I_{L2} = 2 \frac{3 - k}{(1 - k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2 + V_{in}}{L_3} kT = \frac{(2 - k)^2}{(1 - k)^2 L_3} kTV_{in} \quad I_{L3} = \frac{2I_O}{1 - k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1 - k)^3 TV_{in}}{4(4 - k)(3 - k)L_1 I_O} = \frac{k(1 - k)^3}{2(4 - k)(3 - k)G_3} \frac{R}{2fL_1} \quad (4.64)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1 - k)(2 - k)TV_1}{4(3 - k)L_2 I_O} = \frac{k(1 - k)(2 - k)}{2(3 - k)G_3} \frac{R}{2fL_2} \quad (4.65)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(2 - k)^2 TV_{in}}{4(1 - k)L_3 I_O} = \frac{k(2 - k)^2}{2(1 - k)G_3} \frac{R}{2fL_3} \quad (4.66)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32}} = \frac{I_O(1 - k)T}{C_{32}} = \frac{1 - k}{fC_{32}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1 - k}{2RfC_{32}} \quad (4.67)$$

4.4.4 N/O Higher Order Lift Enhanced Circuit

Higher order N/O lift enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC in each stage. Each stage final voltage V_{Ci1} ($i = 1, 2, \dots n$) is

$$V_{Ci1} = \left(\frac{3-k}{1-k}\right)^i V_{in} \quad (4.68)$$

For n th order lift enhanced circuit, the final output voltage is

$$V_O = \left[\left(\frac{3-k}{1-k}\right)^n - 1\right] V_{in} \quad (4.69)$$

The voltage transfer gain is

$$G_n = \frac{V_O}{V_{in}} = \left(\frac{3-k}{1-k}\right)^n - 1 \quad (4.70)$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{n2}} \quad (4.71)$$

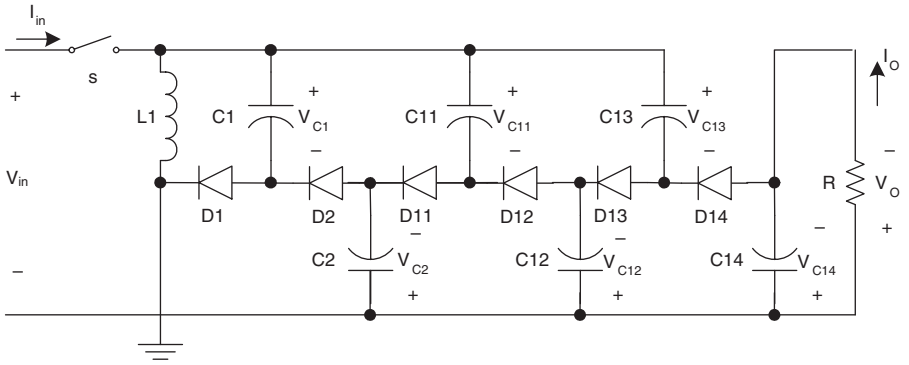
4.5 Re-Enhanced Series

All circuits of negative output super-lift Luo-converters — re-enhanced series — are derived from the corresponding circuits of the main series by adding the DEC twice in each stage circuit.

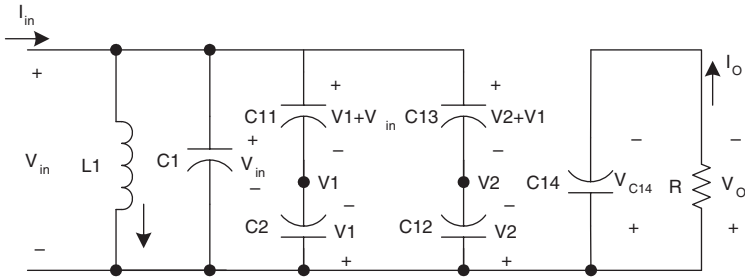
The first three stages of this series are shown in [Figure 4.9](#) through [Figure 4.11](#). For convenience they are called elementary re-enhanced circuits, re-lift re-enhanced circuits, and triple-lift re-enhanced circuits respectively, and numbered as $n = 1, 2$, and 3 .

4.5.1 N/O Elementary Re-Enhanced Circuit

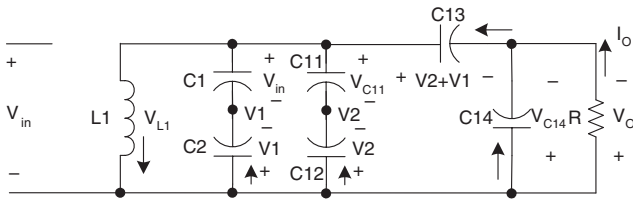
This circuit is derived from the N/O elementary circuit by adding the DEC twice. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 4.9](#). The voltage across capacitor C_1 is charged to V_{in} . The voltage across capacitor C_{12} is charged to V_{C12} . The voltage across capacitor C_{13} is charged to V_{C13} .



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

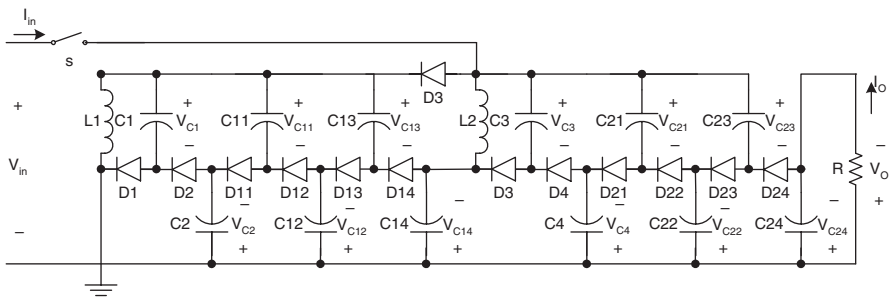
FIGURE 4.9
N/O elementary re-enhanced circuit.

$$V_{C13} = \frac{4-k}{1-k} V_{in} \quad (4.72)$$

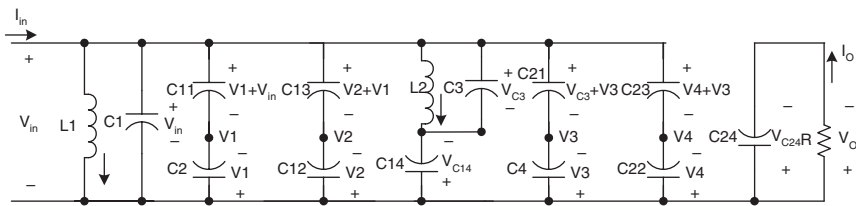
The output voltage is

$$V_O = V_{C13} - V_{in} = \left[\frac{4-k}{1-k} - 1 \right] V_{in} \quad (4.73)$$

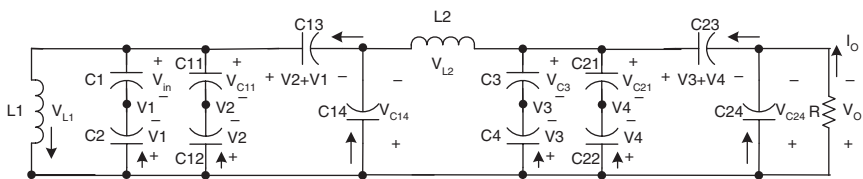
The voltage transfer gain is



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.10

N/O re-lift re-enhanced circuit.

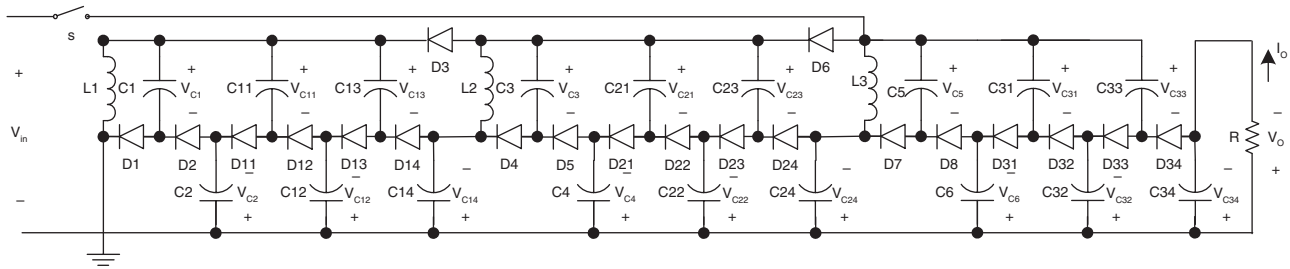
$$G_1 = \frac{V_o}{V_{in}} = \frac{4-k}{1-k} - 1 \quad (4.74)$$

The ripple voltage of output voltage v_o is

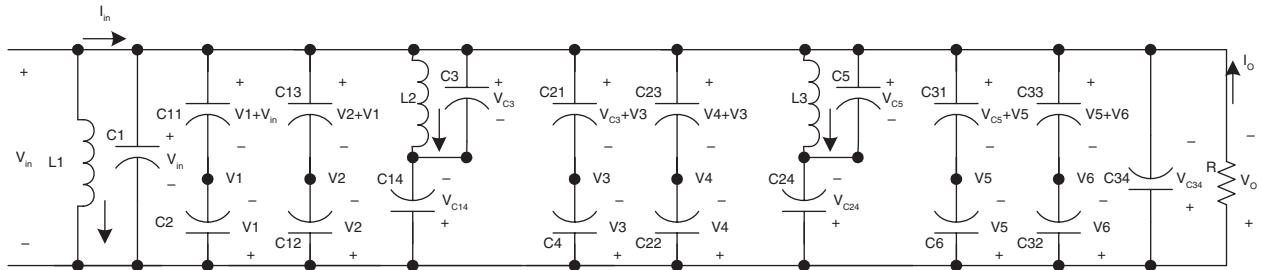
$$\Delta v_o = \frac{\Delta Q}{C_{14}} = \frac{I_o(1-k)T}{C_{14}} = \frac{1-k}{fC_{14}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

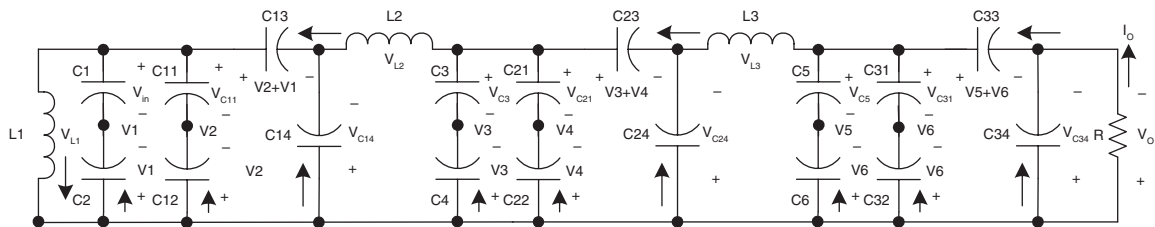
$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{14}} \quad (4.75)$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.11
N/O triple-lift re-enhanced circuit.

4.5.2 N/O Re-Lift Re-Enhanced Circuit

The N/O re-lift re-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC twice in each stage. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 4.10](#). The voltage across capacitor C_{13} is charged to V_{C13} . As described in the previous section the voltage across C_{13} is

$$V_{C13} = \frac{4-k}{1-k} V_{in}$$

Analogously,

$$V_{C23} = \left(\frac{4-k}{1-k}\right)^2 V_{in} \quad (4.76)$$

The output voltage is

$$V_O = V_{C23} - V_{in} = \left[\left(\frac{4-k}{1-k}\right)^2 - 1\right] V_{in} \quad (4.77)$$

The voltage transfer gain is

$$G_2 = \frac{V_O}{V_{in}} = \left(\frac{4-k}{1-k}\right)^2 - 1 \quad (4.78)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{24}} = \frac{I_O(1-k)T}{C_{24}} = \frac{1-k}{fC_{24}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{24}} \quad (4.79)$$

4.5.3 N/O Triple-Lift Re-Enhanced Circuit

This circuit is derived from N/O triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 4.11](#). The voltage across capacitor C_{13} is

$$V_{C13} = \frac{4-k}{1-k} V_{in}$$

The voltage across capacitor C_{23} is

$$V_{C23} = \left(\frac{4-k}{1-k}\right)^2 V_{in}$$

Analogously, the voltage across capacitor C_{33} is

$$V_{C33} = \left(\frac{4-k}{1-k}\right)^3 V_{in} \quad (4.80)$$

The output voltage is

$$V_O = V_{C33} - V_{in} = \left[\left(\frac{4-k}{1-k}\right)^3 - 1\right] V_{in} \quad (4.81)$$

The voltage transfer gain is

$$G_3 = \frac{V_O}{V_{in}} = \left(\frac{4-k}{1-k}\right)^3 - 1 \quad (4.82)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{34}} = \frac{I_O(1-k)T}{C_{34}} = \frac{1-k}{fC_{34}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\epsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{34}} \quad (4.83)$$

4.5.4 N/O Higher Order Lift Re-Enhanced Circuit

Higher order N/O lift re-enhanced circuits can be derived from the corresponding circuits of the main series by adding the DEC twice in each stage circuit. Each stage final voltage V_{Ci3} ($i = 1, 2, \dots, n$) is

$$V_{Ci3} = \left(\frac{4-k}{1-k}\right)^i V_{in} \quad (4.84)$$

For n th order lift additional circuit, the final output voltage is

$$V_O = V_{Cn3} - V_{in} = \left[\left(\frac{4-k}{1-k} \right)^n - 1 \right] V_{in} \quad (4.85)$$

The voltage transfer gain is

$$G_n = \frac{V_O}{V_{in}} = \left(\frac{4-k}{1-k} \right)^n - 1 \quad (4.86)$$

The variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{n4}} \quad (4.87)$$

4.6 Multiple-Enhanced Series

All circuits of negative output super-lift Luo-converters — multiple-enhanced series are derived from the corresponding circuits of the main series by adding the DEC multiple (j) times in each stage circuit.

The first three stages of this series are shown in [Figure 4.12](#) to [Figure 4.14](#). For convenience they are called elementary multiple-enhanced circuits, re-lift multiple-enhanced circuits, and triple-lift multiple-enhanced circuits respectively, and numbered as $n = 1, 2$, and 3 .

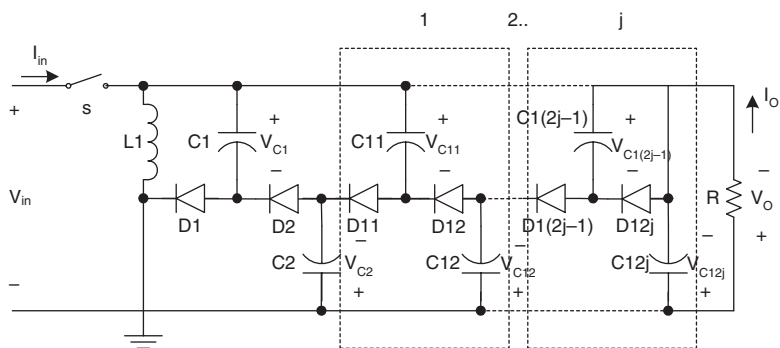
4.6.1 N/O Elementary Multiple-Enhanced Circuit

This circuit is derived from the N/O elementary circuit by adding the DEC multiple (j) times. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 4.12](#). The voltage across capacitor C_{12j-1} is

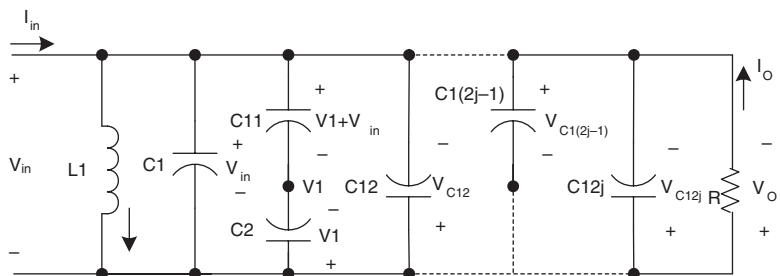
$$V_{C12j-1} = \frac{j+2-k}{1-k} V_{in} \quad (4.88)$$

The output voltage is

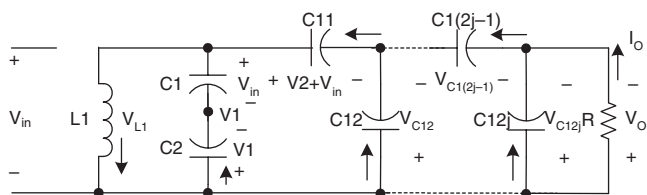
$$V_O = V_{C12j-1} - V_{in} = \left[\frac{j+2-k}{1-k} - 1 \right] V_{in} \quad (4.89)$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.12

N/O elementary multiple-enhanced circuit.

The voltage transfer gain is

$$G_1 = \frac{V_O}{V_{in}} = \frac{j+2-k}{1-k} - 1 \quad (4.90)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12j}} = \frac{I_o(1-k)T}{C_{12j}} = \frac{1-k}{fC_{12j}} \frac{V_O}{R}$$

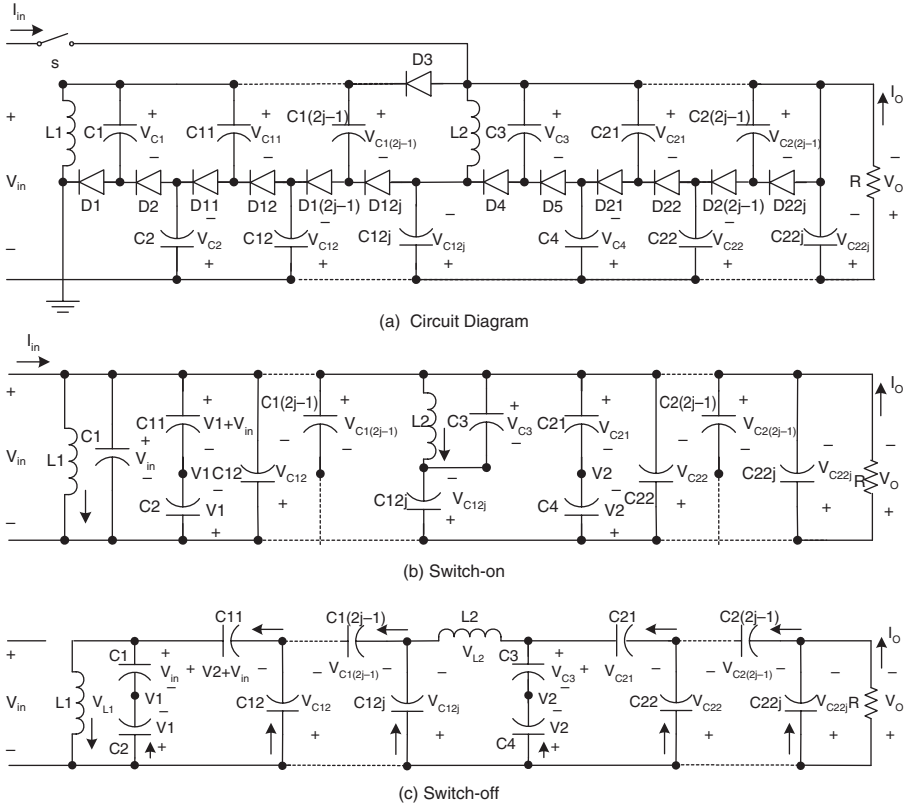


FIGURE 4.13
N/O re-lift multiple-enhanced circuit.

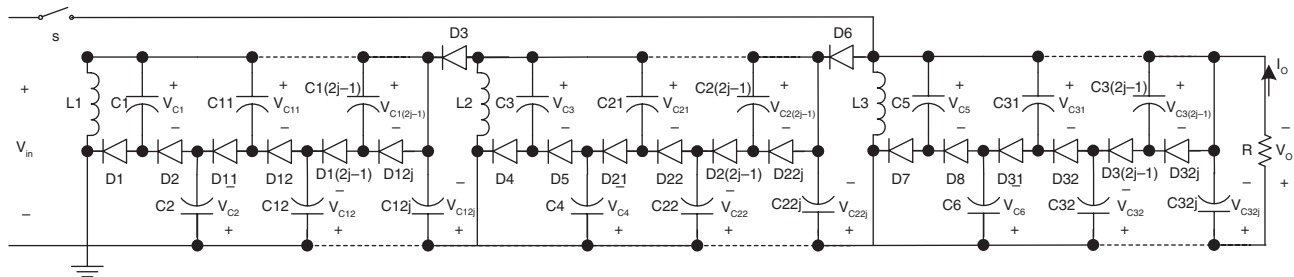
Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12j}} \quad (4.91)$$

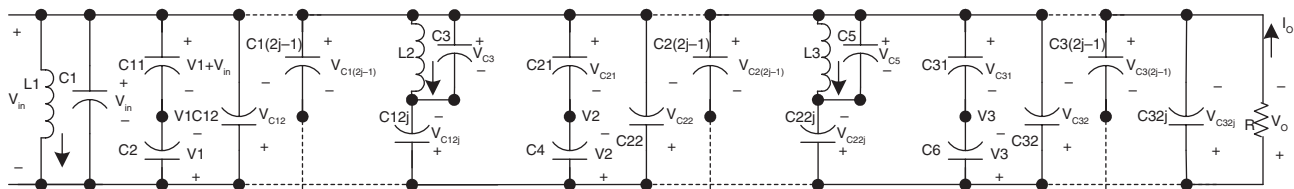
4.6.2 N/O Re-Lift Multiple-Enhanced Circuit

The N/O re-lift multiple-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC multiple (j) times into each stage. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 4.13. The voltage across capacitor C_{22j-1} is

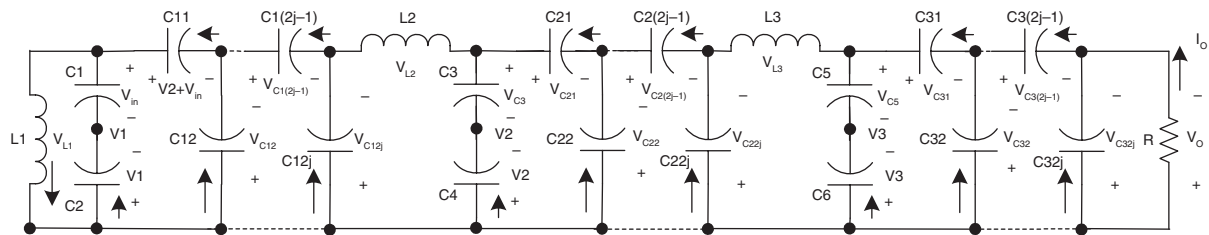
$$V_{C_{22j-1}} = \left(\frac{j+2-k}{1-k} \right)^2 V_{in} \quad (4.92)$$



(a) Circuit Diagram



(b) Switch-on



(c) Switch-off

FIGURE 4.14
N/O triple-lift multiple-enhanced circuit.

The output voltage is

$$V_O = V_{C22j-1} - V_{in} = \left[\left(\frac{j+2-k}{1-k} \right)^2 - 1 \right] V_{in} \quad (4.93)$$

The voltage transfer gain is

$$G_2 = \frac{V_O}{V_{in}} = \left(\frac{j+2-k}{1-k} \right)^2 - 1 \quad (4.94)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{22j}} = \frac{I_O(1-k)T}{C_{22j}} = \frac{1-k}{fC_{22j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{22j}} \quad (4.95)$$

4.6.3 N/O Triple-Lift Multiple-Enhanced Circuit

This circuit is derived from N/O triple-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 4.14](#). The voltage across capacitor C_{32j-1} is

$$V_{C32j-1} = \left(\frac{j+2-k}{1-k} \right)^3 V_{in} \quad (4.96)$$

The output voltage is

$$V_O = V_{C32j-1} - V_{in} = \left[\left(\frac{j+2-k}{1-k} \right)^3 - 1 \right] V_{in} \quad (4.97)$$

The voltage transfer gain is

$$G_3 = \frac{V_O}{V_{in}} = \left(\frac{j+2-k}{1-k} \right)^3 - 1 \quad (4.98)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32j}} = \frac{I_o(1-k)T}{C_{32j}} = \frac{1-k}{fC_{32j}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{32j}} \quad (4.99)$$

4.6.4 N/O Higher Order Lift Multiple-Enhanced Circuit

The higher order N/O lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple (j) times in each stage circuit. Each stage final voltage V_{Ci2j-1} ($i = 1, 2, \dots n$) is

$$V_{Ci2j-1} = \left(\frac{j+2-k}{1-k}\right)^i V_{in} \quad (4.100)$$

For n th order lift multiple-enhanced circuit, the final output voltage is

$$V_o = \left[\left(\frac{j+2-k}{1-k}\right)^n - 1\right] V_{in} \quad (4.101)$$

The voltage transfer gain is

$$G_n = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^n - 1 \quad (4.102)$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{n2j}} \quad (4.103)$$

4.7 Summary of Negative Output Super-Lift Luo-Converters

All circuits of the negative output super-lift Luo-converters as a family can be shown in [Figure 4.15](#). From the analysis in previous sections the common formula to calculate the output voltage can be presented:

$$V_O = \begin{cases} [(\frac{2-k}{1-k})^n - 1]V_{in} & \text{main_series} \\ [(\frac{2-k}{1-k})^{n-1}(\frac{3-k}{1-k}) - 1]V_{in} & \text{additional_series} \\ [(\frac{3-k}{1-k})^n - 1]V_{in} & \text{enhanced_series} \\ [(\frac{4-k}{1-k})^n - 1]V_{in} & \text{re-enhanced_series} \\ [(\frac{j+2-k}{1-k})^n - 1]V_{in} & \text{multiple-enhanced_series} \end{cases} \quad (4.104)$$

The corresponding voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \begin{cases} (\frac{2-k}{1-k})^n - 1 & \text{main_series} \\ (\frac{2-k}{1-k})^{n-1}(\frac{3-k}{1-k}) - 1 & \text{additional_series} \\ (\frac{3-k}{1-k})^n - 1 & \text{enhanced_series} \\ (\frac{4-k}{1-k})^n - 1 & \text{re-enhanced_series} \\ (\frac{j+2-k}{1-k})^n - 1 & \text{multiple-enhanced_series} \end{cases} \quad (4.105)$$

In order to show the advantages of N/O super-lift converters, their voltage transfer gains can be compared to that of buck converters,

$$G = \frac{V_O}{V_{in}} = k$$

Forward converters,

$$G = \frac{V_O}{V_{in}} = kN \quad (N \text{ is the transformer turn's ratio})$$

Cúk-converters,

$$G = \frac{V_O}{V_{in}} = \frac{k}{1-k}$$

fly-back converters,

$$G = \frac{V_O}{V_{in}} = \frac{kN}{1-k} \quad (N \text{ is the transformer turn's ratio})$$

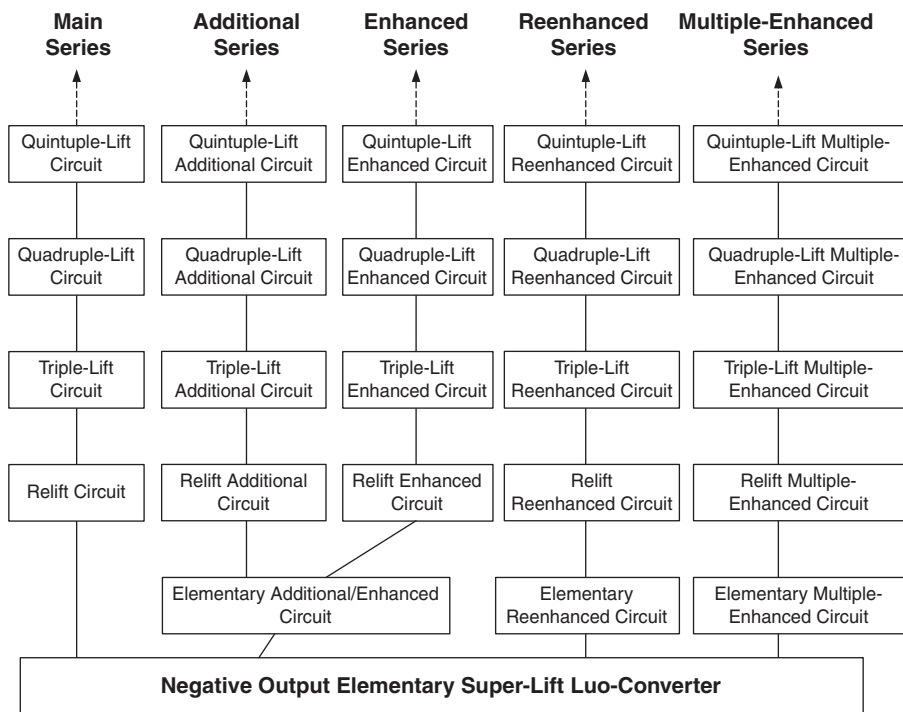


FIGURE 4.15
The family of negative output super-lift Luo-converters.

boost converters,

$$G = \frac{V_O}{V_{in}} = \frac{1}{1-k}$$

and negative output Luo-converters

$$G = \frac{V_O}{V_{in}} = \frac{n}{1-k} \quad (4.106)$$

If we assume the conduction duty k is 0.2, the output voltage transfer gains are listed in [Table 4.1](#), if the conduction duty k is 0.5, the output voltage transfer gains are listed in [Table 4.2](#), and if the conduction duty k is 0.8, the output voltage transfer gains are listed in [Table 4.3](#).

TABLE 4.1

Voltage Transfer Gains of Converters in the Condition $k = 0.2$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.2		
Forward converter		0.2N (N is the transformer turn's ratio)				
Cúk-converter				0.25		
Fly-back converter		0.25N (N is the transformer turn's ratio)				
Boost converter				1.25		
Negative output Luo-converters	1.25	2.5	3.75	5	6.25	$1.25n$
Negative output super-lift converters — main series	1.25	4.06	10.39	24.63	56.67	2.25^{n-1}
Negative output super-lift converters — additional series	2.5	6.88	16.72	38.87	88.7	$3.5 * 2.25^{(n-1)-1}$

TABLE 4.2

Voltage Transfer Gains of Converters in the Condition $k = 0.5$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.5		
Forward converter		0.5N (N is the transformer turn's ratio)				
Cúk-converter				1		
Fly-back converter		N (N is the transformer turn's ratio)				
Boost converter				2		
Negative output Luo-converters	2	4	6	8	10	$2n$
Negative output super-lift converters — main series	2	8	26	80	242	3^{n-1}
Negative output super-lift converters — additional series	4	14	44	134	404	$5 * 3^{(n-1)-1}$

TABLE 4.3

Voltage Transfer Gains of Converters in the Condition $k = 0.8$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.8		
Forward converter		0.8N (N is the transformer turn's ratio)				
Cúk-converter				4		
Fly-back converter		4N (N is the transformer turn's ratio)				
Boost converter				5		
Negative output Luo-converters	5	10	15	20	25	$5n$
Negative output super-lift converters — main series	5	35	215	1295	7775	$6^n - 1$
Negative output super-lift converters — additional series	10	65	395	2375	14,255	$11 * 6^{(n-1)-1}$

4.8 Simulation Results

To verify the design and calculation results, PSpice simulation package was applied to these converters. Choosing $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F, and $R = 30$ k, and using $k = 0.5$ and $f = 100$ kHz.

4.8.1 Simulation Results of a N/O Triple-Lift Circuit

The voltage values V_1 , V_2 , and V_O of a N/O triple-lift circuit are -46 V, -174 V, and -639 V respectively and current waveforms i_{L1} (its average value $I_{L1} = 603$ mA), i_{L2} , and i_{L3} . The simulation results are shown in [Figure 4.16](#). The voltage values are matched to the calculated results.

4.8.2 Simulation Results of a N/O Triple-Lift Additional Circuit

The voltage values V_1 , V_2 , V_3 , and V_O of a N/O triple-lift additional circuit are -38 V, -146 V, -517 V, and -889 V respectively and current waveforms i_{L1} (its average value $I_{L1} = 1.79$ A), i_{L2} , and i_{L3} . The simulation results are shown in [Figure 4.17](#). The voltage values are matched to the calculated results.

4.9 Experimental Results

A test rig was constructed to verify the design and calculation results, and compare with PSpice simulation results. The testing conditions are the same: $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F and $R = 30$ k, and using $k = 0.5$ and $f = 100$ kHz. The component of the switch is a MOSFET device IRF950 with the rates 950 V/5 A/2 MHz. The output voltage and the first diode current values are measured in the following converters.

4.9.1 Experimental Results of a N/O Triple-Lift Circuit

After careful measurement, the current value of $I_{L1} = 0.6$ A (shown in channel 1 with 1 A/Div) and voltage value of $V_O = -640$ V (shown in channel 2 with 200 V/Div) are obtained. The experimental results (current and voltage values) in [Figure 4.18](#) are identically matched to the calculated and simulation results, which are $I_{L1} = 0.603$ A and $V_O = -639$ V shown in [Figure 4.16](#).

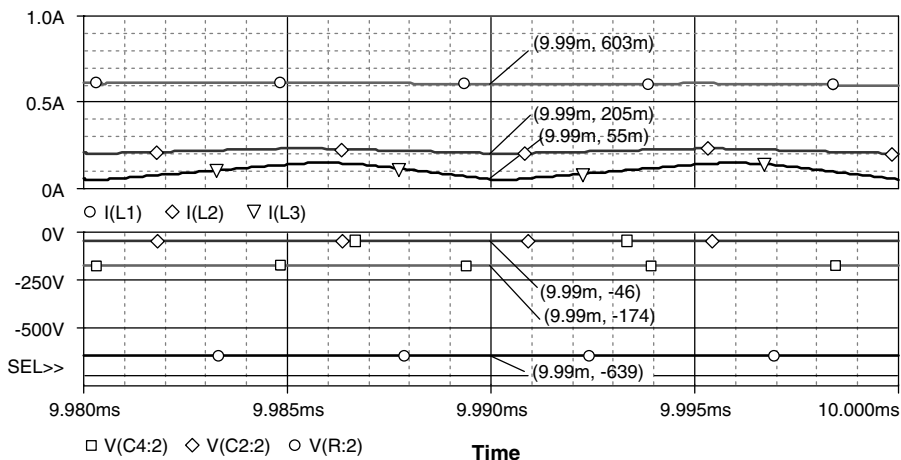


FIGURE 4.16

Simulation results of a N/O triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

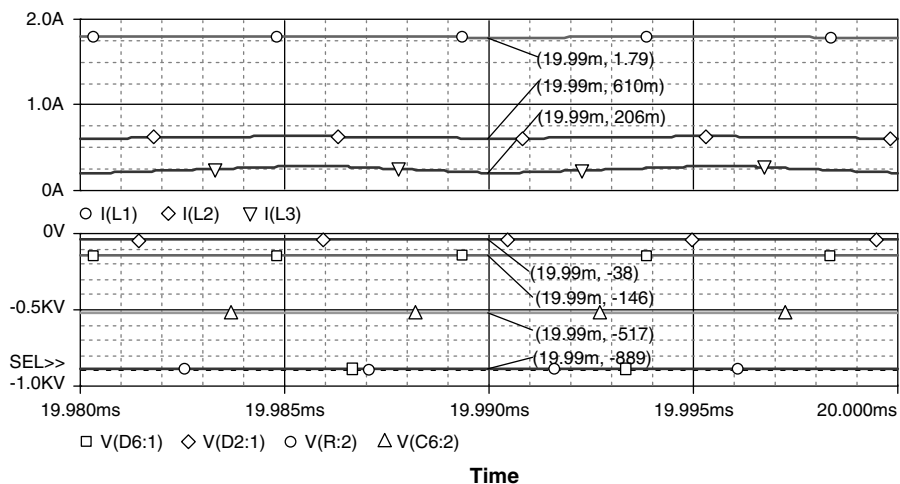


FIGURE 4.17

Simulation results of a N/O triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

4.9.2 Experimental Results of a N/O Triple-Lift Additional Circuit

The experimental results (voltage and current values) are identically matched to the calculated and simulation results as shown in Figure 4.19. The current value of $I_{L1} = 1.78$ A (shown in channel 1 with 1 A/Div) and voltage value of $V_O = -890$ V (shown in channel 2 with 200 V/Div) are obtained. The experimental results are identically matched to the calculated and simulation results, which are $I_{L1} = 1.79$ A and $V_O = -889$ V shown in Figure 4.17.

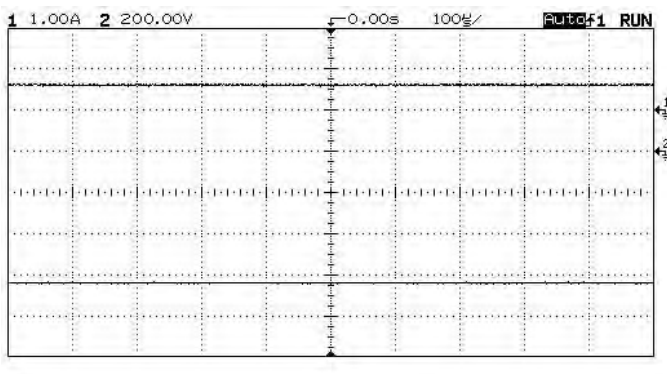


FIGURE 4.18

Experimental results of a N/O triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

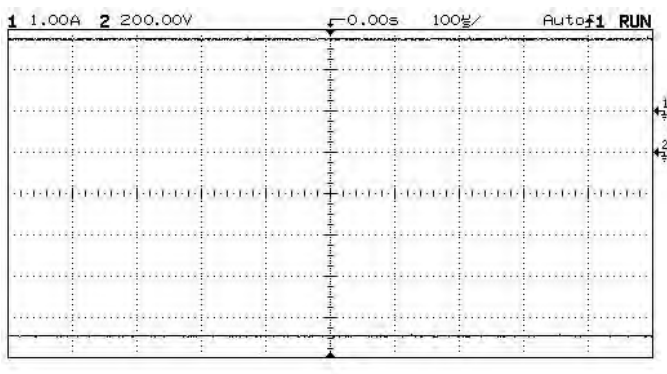


FIGURE 4.19

Experimental results of a N/O triple-lift additional circuit at $k = 0.5$ and $f = 100$ kHz.

4.9.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully, but efficiency, particularly the efficiencies of the tested circuits are 51 to 78%, which is good for high voltage output equipment. Comparison of the simulation and experimental results, which are listed in the [Table 4.4](#) and [Table 4.5](#), demonstrates that all results are well identified with each other.

4.9.4 Transient Process and Stability Analysis

Usually, there is high inrush current during the first power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick lasting only a few milliseconds.

TABLE 4.4

Comparison of Simulation and Experimental Results of a N/O Triple-Lift Circuit

Stage No. (<i>n</i>)	I_{L1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	$ V_o $ (V)	P_o (W)	η (%)
Simulation results	0.603	0.871	20	17.42	639	13.61	78.12
Experimental results	0.6	0.867	20	17.33	640	13.65	78.75

TABLE 4.5

Comparison of Simulation and Experimental Results
of a N/O Triple-Lift Additional Circuit

Stage No. (<i>n</i>)	I_{L1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	$ V_o $ (V)	P_o (W)	η (%)
Simulation results	1.79	2.585	20	51.7	889	26.34	51
Experimental results	1.78	2.571	20	51.4	890	26.4	51

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Positive Output Cascade Boost Converters

Super-lift technique increases the voltage transfer gain in geometric progression. However, these circuits are a bit complex. This chapter introduces a novel approach — the positive output cascade boost converter — that implements the output voltage increasing in geometric progression, but with simpler structure. They also effectively enhance the voltage transfer gain in power-law.

5.1 Introduction

In order to sort these converters differently from existing voltage-lift (VL) and super-lift (SL) converters, these converters are entitled *positive output cascade boost converters*. There are several subseries:

- Main series — Each circuit of the main series has one switch S , n inductors, n capacitors, and $(2n - 1)$ diodes.
- Additional series — Each circuit of the additional series has one switch S , n inductors, $(n + 2)$ capacitors, and $(2n + 1)$ diodes.
- Double series — Each circuit of the double series has one switch S , n inductors, $3n$ capacitors, and $(3n - 1)$ diodes.
- Triple series — Each circuit of the triple series has one switch S , n inductors, $5n$ capacitors, and $(5n - 1)$ diodes.
- Multiple series — Each multiple series circuit has one switch S and a higher number of capacitors and diodes.

In order to concentrate the super-lift function, these converters work in the steady state with the condition of continuous conduction mode (CCM).

The conduction duty ratio is k , switching frequency is f , switching period is $T = 1/f$, the load is resistive load R . The input voltage and current are V_{in} and I_{in} , output voltage and current are V_O and I_O . Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_O \times I_O$. The voltage transfer gain is G :

$$G = \frac{V_O}{V_{in}}$$

5.2 Main Series

The first three stages of positive output cascade boost converters — main series — are shown in [Figure 5.1](#) to [Figure 5.3](#). For convenience they are called elementary boost converter, two-stage circuit, and three-stage circuit respectively, and numbered as $n = 1, 2$, and 3.

5.2.1 Elementary Boost Circuit

The elementary boost converter is the fundamental boost converter introduced in [Chapter 1](#) (see [Figure 1.24](#)). Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in [Figure 5.1](#). The voltage across capacitor C_1 is charged to V_O . The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_O - V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L1} is

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_O - V_{in}}{L_1} (1 - k)T \quad (5.1)$$

$$V_O = \frac{1}{1 - k} V_{in} \quad (5.2)$$

The voltage transfer gain is

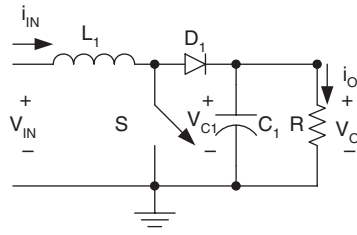
$$G = \frac{V_O}{V_{in}} = \frac{1}{1 - k} \quad (5.3)$$

The inductor average current is

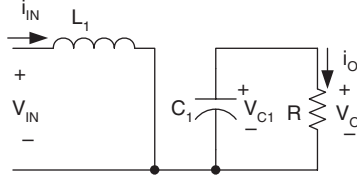
$$I_{L1} = (1 - k) \frac{V_O}{R} \quad (5.4)$$

The variation ratio of current i_{L1} through inductor L_1 is

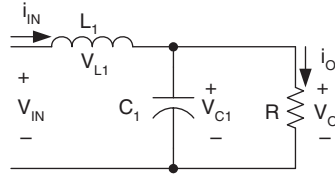
$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_{in}}{(1 - k)2L_1V_O / R} = \frac{k}{2} \frac{R}{fL_1} \quad (5.5)$$



(a) Circuit diagram



(b) Switching-on



(c) Switching-off

FIGURE 5.1
Elementary boost converter.

Usually ξ_1 is small (much lower than unity), which means this converter works in the continuous mode. The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_1} = \frac{I_o(1-k)T}{C_1} = \frac{1-k}{fC_1} \frac{V_o}{R}$$

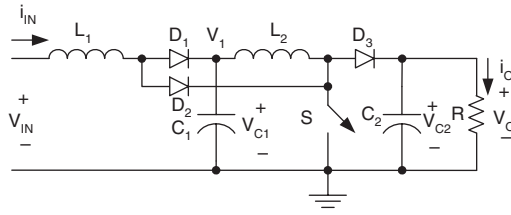
Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_1} \quad (5.6)$$

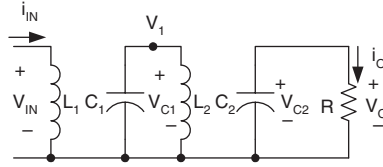
Usually R is in $k\Omega$, f in 10 kHz, and C_1 in μF , the ripple is smaller than 1%.

5.2.2 Two-Stage Boost Circuit

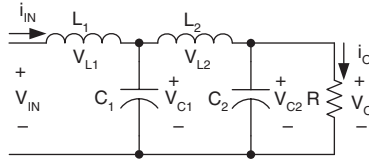
The two-stage boost circuit is derived from elementary boost converter by adding the parts $(L_2-D_2-D_3-C_2)$. Its circuit diagram and equivalent circuits



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.2

Two-stage boost circuit.

during switch-on and switch-off are shown in Figure 5.2. The voltage across capacitor C_1 is charged to V_1 . As described in previous section the voltage V_1 across capacitor C_1 is

$$V_1 = \frac{1}{1-k} V_{in}$$

The voltage across capacitor C_2 is charged to V_O . The current flowing through inductor L_2 increases with voltage V_1 during switching-on period kT and decreases with voltage $-(V_O - V_1)$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_1}{L_2} kT = \frac{V_O - V_1}{L_2} (1-k)T \quad (5.7)$$

$$V_O = \frac{1}{1-k} V_1 = \left(\frac{1}{1-k}\right)^2 V_{in} \quad (5.8)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1-k}\right)^2 \quad (5.9)$$

Analogously,

$$\begin{aligned} \Delta i_{L1} &= \frac{V_{in}}{L_1} kT & I_{L1} &= \frac{I_O}{(1-k)^2} \\ \Delta i_{L2} &= \frac{V_1}{L_2} kT & I_{L2} &= \frac{I_O}{1-k} \end{aligned}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2L_1 I_O} = \frac{k(1-k)^4}{2} \frac{R}{fL_1} \quad (5.10)$$

the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k) TV_1}{2L_2 I_O} = \frac{k(1-k)^2}{2} \frac{R}{fL_2} \quad (5.11)$$

and the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_2} \quad (5.12)$$

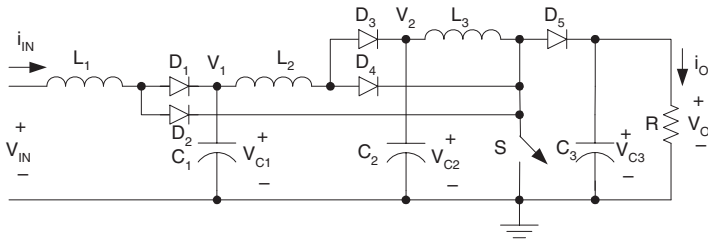
5.2.3 Three-Stage Boost Circuit

The three-stage boost circuit is derived from the two-stage boost circuit by double adding the parts (L_2 - D_2 - D_3 - C_2). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 5.3](#). The voltage across capacitor C_1 is charged to V_1 . As described previously, the voltage V_1 across capacitor C_1 is

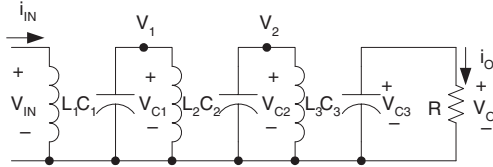
$$V_1 = \frac{1}{1-k} V_{in}$$

and voltage V_2 across capacitor C_2 is

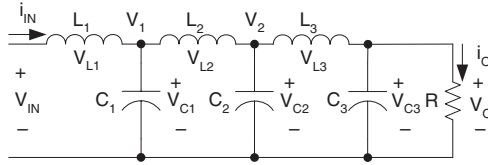
$$V_2 = \left(\frac{1}{1-k}\right)^2 V_{in}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.3

Three-stage boost circuit.

The voltage across capacitor C_3 is charged to V_O . The current flowing through inductor L_3 increases with voltage V_2 during switching-on period kT and decreases with voltage $-(V_O - V_2)$ during switch-off $(1 - k)T$. Therefore, the ripple of the inductor current i_{L3} is

$$\Delta i_{L3} = \frac{V_2}{L_3} kT = \frac{V_O - V_2}{L_3} (1 - k)T \quad (5.13)$$

$$V_O = \frac{1}{1 - k} V_2 = \left(\frac{1}{1 - k}\right)^2 V_1 = \left(\frac{1}{1 - k}\right)^3 V_{in} \quad (5.14)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1 - k}\right)^3 \quad (5.15)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{I_O}{(1-k)^3}$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{I_O}{(1-k)^2}$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2L_1 I_O} = \frac{k(1-k)^6}{2} \frac{R}{fL_1} \quad (5.16)$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{2L_2 I_O} = \frac{k(1-k)^4}{2} \frac{R}{fL_2} \quad (5.17)$$

The variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k) TV_2}{2L_3 I_O} = \frac{k(1-k)^2}{2} \frac{R}{fL_3} \quad (5.18)$$

and the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_3} \quad (5.19)$$

5.2.4 Higher Stage Boost Circuit

Higher stage boost circuit can be designed by just multiple repeating of the parts (L_2 - D_2 - D_3 - C_2). For n^{th} stage boost circuit, the final output voltage across capacitor C_n is

$$V_O = \left(\frac{1}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1-k}\right)^n \quad (5.20)$$

the variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{L_i} / 2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2} \frac{R}{fL_i} \quad (5.21)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_n} \quad (5.22)$$

5.3 Additional Series

All circuits of positive output cascade boost converters — additional series — are derived from the corresponding circuits of the main series by adding a DEC.

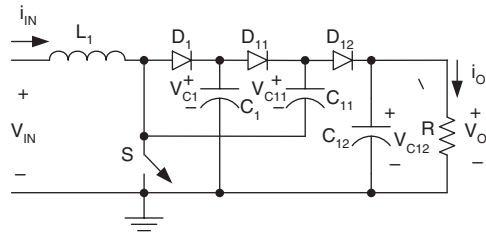
The first three stages of this series are shown in [Figure 5.4](#) to [Figure 5.6](#). For convenience they are called elementary additional circuits, two-stage additional circuits, and three-stage additional circuits respectively, and numbered as $n = 1, 2$, and 3 .

5.3.1 Elementary Boost Additional (Double) Circuit

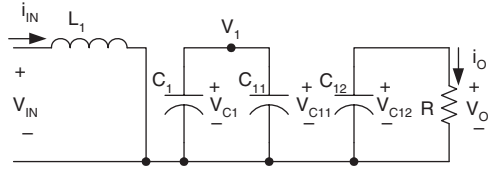
This elementary boost additional circuit is derived from elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 5.4](#). The voltage across capacitor C_1 and C_{11} is charged to V_1 and voltage across capacitor C_{12} is charged to $V_O = 2 V_1$. The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switching-on period kT and decreases with voltage $-(V_1 - V_{in})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1} (1-k)T \quad (5.23)$$

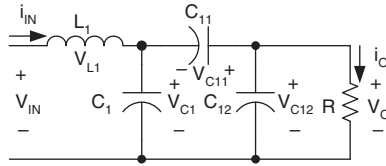
$$V_1 = \frac{1}{1-k} V_{in}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.4

Elementary boost additional (double) circuit.

The output voltage is

$$V_O = 2V_1 = \frac{2}{1-k} V_{in} \quad (5.24)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{2}{1-k} \quad (5.25)$$

and

$$i_{in} = I_{L1} = \frac{2}{1-k} I_O \quad (5.26)$$

The variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_1} \quad (5.27)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = \frac{I_o(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12}} \quad (5.28)$$

5.3.2 Two-Stage Boost Additional Circuit

The two-stage additional boost circuit is derived from the two-stage boost circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 5.5](#). The voltage across capacitor C_1 is charged to V_1 . As described in the previous section the voltage V_1 across capacitor C_1 is

$$V_1 = \frac{1}{1-k} V_{in}$$

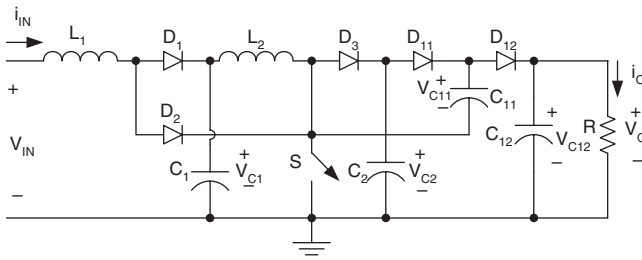
The voltage across capacitor C_2 and capacitor C_{11} is charged to V_2 and voltage across capacitor C_{12} is charged to V_o . The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_2 - V_1)$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_1}{L_2} kT = \frac{V_2 - V_1}{L_2} (1-k)T \quad (5.29)$$

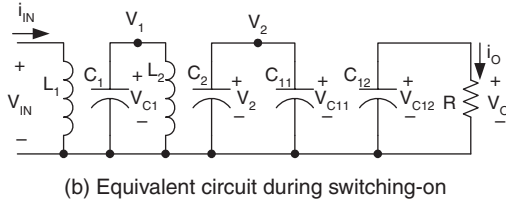
$$V_2 = \frac{1}{1-k} V_1 = \left(\frac{1}{1-k}\right)^2 V_{in} \quad (5.30)$$

The output voltage is

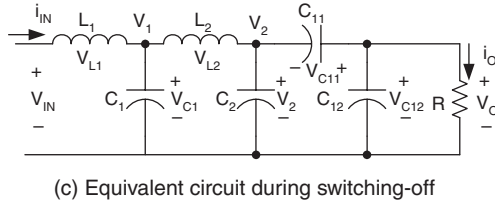
$$V_o = 2V_2 = \frac{2}{1-k} V_1 = 2\left(\frac{1}{1-k}\right)^2 V_{in} \quad (5.31)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.5
Two-stage boost additional circuit.

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = 2\left(\frac{1}{1-k}\right)^2 \quad (5.32)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{2}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{4L_1 I_O} = \frac{k(1-k)^4}{8} \frac{R}{fL_1} \quad (5.33)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \quad (5.34)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (5.35)$$

5.3.3 Three-Stage Boost Additional Circuit

This circuit is derived from the three-stage boost circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 5.6](#). The voltage across capacitor C_1 is charged to V_1 . As described previously the voltage V_1 across capacitor C_1 is $V_1 = (1/1-k)V_{in}$, and voltage V_2 across capacitor C_2 is $V_2 = (1/1-k)^2 V_{in}$.

The voltage across capacitor C_3 and capacitor C_{11} is charged to V_3 . The voltage across capacitor C_{12} is charged to V_O . The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_3 - V_2)$ during switch-off $(1-k)T$. Therefore,

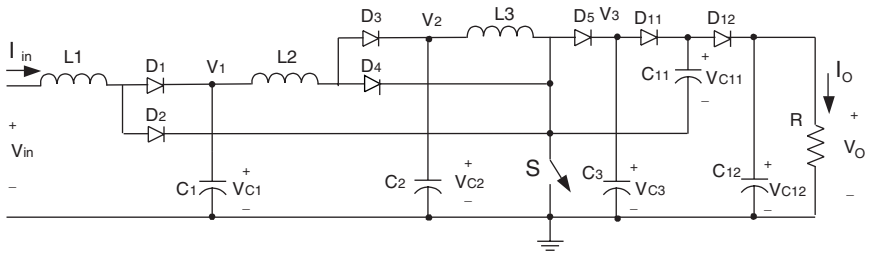
$$\Delta i_{L3} = \frac{V_2}{L_3} kT = \frac{V_3 - V_2}{L_3} (1-k)T \quad (5.36)$$

and

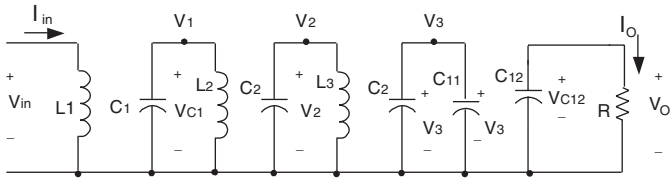
$$V_3 = \frac{1}{1-k} V_2 = \left(\frac{1}{1-k}\right)^2 V_1 = \left(\frac{1}{1-k}\right)^3 V_{in} \quad (5.37)$$

The output voltage is

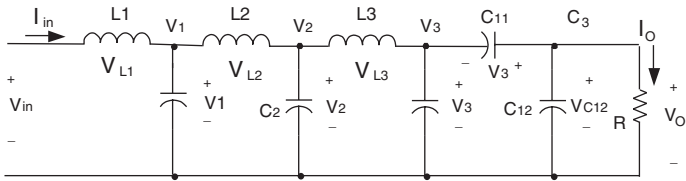
$$V_O = 2V_3 = 2\left(\frac{1}{1-k}\right)^3 V_{in} \quad (5.38)$$



(a) Circuit diagram



(b) Equivalent circuit during switch-on



(b) Equivalent circuit during switch-off

FIGURE 5.6

Three-stage boost additional circuit.

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = 2 \left(\frac{1}{1-k} \right)^3 \quad (5.39)$$

Analogously:

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{2}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{4L_1 I_O} = \frac{k(1-k)^6}{8} \frac{R}{fL_1} \quad (5.40)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{4L_2 I_O} = \frac{k(1-k)^4}{8} \frac{R}{fL_2} \quad (5.41)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k) TV_2}{4L_3 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_3} \quad (5.42)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12}} \quad (5.43)$$

5.3.4 Higher Stage Boost Additional Circuit

Higher stage boost additional circuits can be designed by repeating the parts (L_2 - D_2 - D_3 - C_2) multiple times. For n th stage additional circuit, the final output voltage is

$$V_o = 2\left(\frac{1}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^n \quad (5.44)$$

Analogously, the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{8} \frac{R}{fL_i} \quad (5.45)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{12}} \quad (5.46)$$

5.4 Double Series

All circuits of the positive output cascade boost converter — double series — are derived from the corresponding circuits of the main series by adding a DEC in each stage circuit. The first three stages of this series are shown in [Figures 5.4, 5.7, and 5.8](#). For convenience to explain, they are called elementary double circuits, two-stage double circuits, and three-stage double circuits respectively, and numbered as $n = 1, 2$, and 3.

5.4.1 Elementary Double Boost Circuit

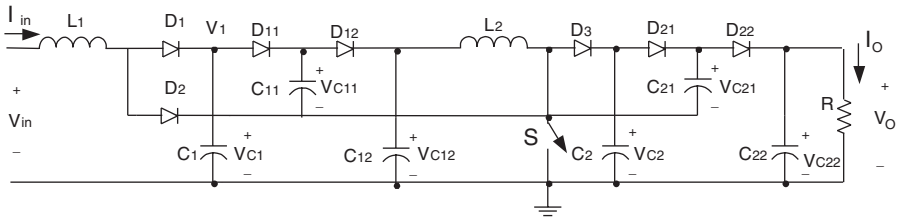
From the construction principle, the elementary double boost circuit is derived from the elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 5.4](#), which is the same as the elementary boost additional circuit.

5.4.2 Two-Stage Double Boost Circuit

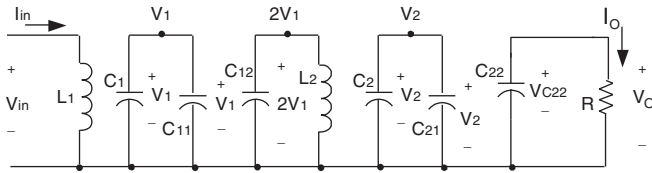
The two-stage double boost circuit is derived from the two-stage boost circuit by adding a DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 5.7](#). The voltage across capacitor C_1 and capacitor C_{11} is charged to V_1 . As described in the previous section, the voltage V_1 across capacitor C_1 and capacitor C_{11} is $V_1 = (1/1-k)V_{in}$. The voltage across capacitor C_{12} is charged to $2V_1$.

The current flowing through inductor L_2 increases with voltage $2V_1$ during switch-on period kT and decreases with voltage $-(V_2 - 2V_1)$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

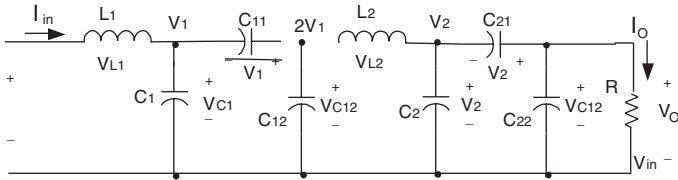
$$\Delta i_{L2} = \frac{2V_1}{L_2} kT = \frac{V_2 - 2V_1}{L_2} (1-k)T \quad (5.47)$$



(a) Circuit diagram



(b) Equivalent circuit during switch-on



(c) Equivalent circuit during switch-off

FIGURE 5.7

Two-stage boost double circuit.

$$V_2 = \frac{2}{1-k} V_1 = 2 \left(\frac{1}{1-k} \right)^2 V_{in} \quad (5.48)$$

The output voltage is

$$V_O = 2V_2 = \left(\frac{2}{1-k} \right)^2 V_{in} \quad (5.49)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2}{1-k} \right)^2 \quad (5.50)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \left(\frac{2}{1-k}\right)^2 I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_O} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \quad (5.51)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \quad (5.52)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = \frac{I_O(1-k)T}{C_{22}} = \frac{1-k}{fC_{22}} \frac{V_O}{R}$$

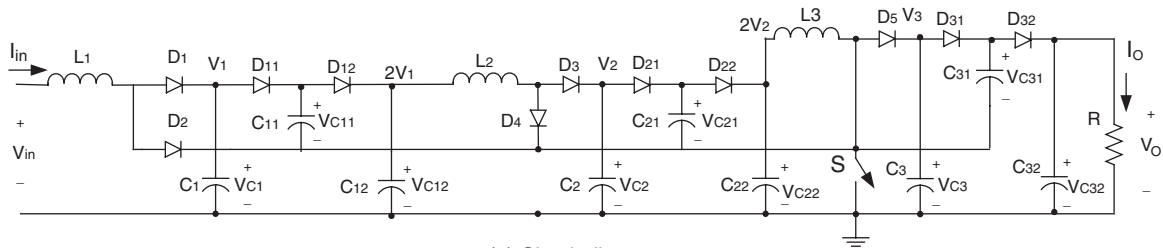
Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{22}} \quad (5.53)$$

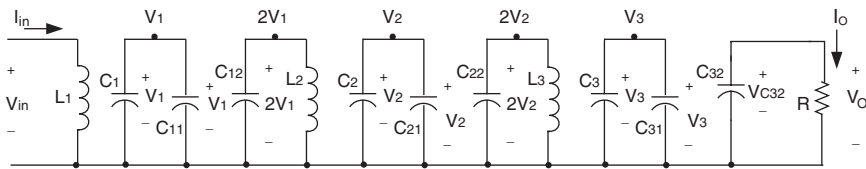
5.4.3 Three-Stage Double Boost Circuit

This circuit is derived from the three-stage boost circuit by adding a DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 5.8](#). The voltage across capacitor C_1 and capacitor C_{11} is charged to V_1 . As described earlier the voltage V_1 across capacitor C_1 and capacitor C_{11} is $V_1 = (1/1-k)V_{in}$, and voltage V_2 across capacitor C_2 and capacitor C_{12} is $V_2 = 2(1/1-k)^2 V_{in}$.

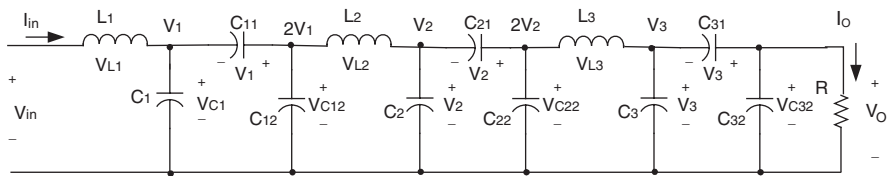
The voltage across capacitor C_{22} is $2V_2 = (2/1-k)^2 V_{in}$. The voltage across capacitor C_3 and capacitor C_{31} is charged to V_3 . The voltage across capacitor C_{12} is charged to V_O . The current flowing through inductor L_3 increases with



(a) Circuit diagram



(b) Equivalent circuit during switch-on



(c) Equivalent circuit during switch-off

FIGURE 5.8

Three-stage boost double circuit.

voltage V_2 during switch-on period kT and decreases with voltage $-(V_3 - 2V_2)$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L3} = \frac{2V_2}{L_3} kT = \frac{V_3 - 2V_2}{L_3} (1 - k)T \quad (5.54)$$

and

$$V_3 = \frac{2V_2}{(1 - k)} = \frac{4}{(1 - k)^3} V_{in} \quad (5.55)$$

The output voltage is

$$V_O = 2V_3 = \left(\frac{2}{1 - k}\right)^3 V_{in} \quad (5.56)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2}{1 - k}\right)^3 \quad (5.57)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{8}{(1 - k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{4}{(1 - k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1 - k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1 - k)^3 TV_{in}}{16L_1 I_O} = \frac{k(1 - k)^6}{128} \frac{R}{fL_1} \quad (5.58)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1 - k)^2 TV_1}{8L_2 I_O} = \frac{k(1 - k)^4}{32} \frac{R}{fL_2} \quad (5.59)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k)TV_2}{4L_3I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_3} \quad (5.60)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32}} = \frac{I_O(1-k)T}{C_{32}} = \frac{1-k}{fC_{32}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{32}} \quad (5.61)$$

5.4.4 Higher Stage Double Boost Circuit

The higher stage double boost circuits can be derived from the corresponding main series circuits by adding a DEC in each stage circuit. For n th stage additional circuit, the final output voltage is

$$V_O = \left(\frac{2}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

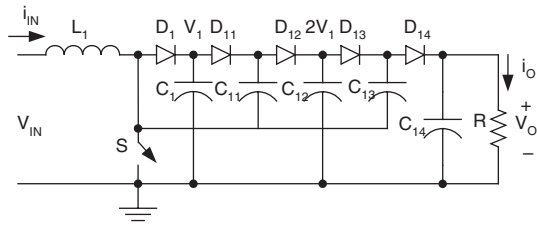
$$G = \frac{V_O}{V_{in}} = \left(\frac{2}{1-k}\right)^n \quad (5.62)$$

Analogously, the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

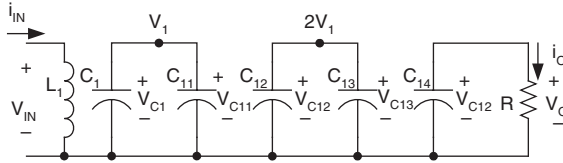
$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{2 * 2^{2n}} \frac{R}{fL_i} \quad (5.63)$$

The variation ratio of output voltage v_O is

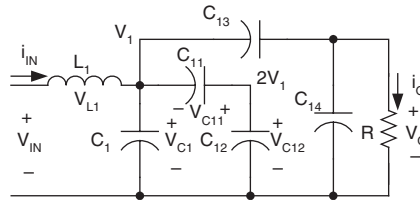
$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{n2}} \quad (5.64)$$



(a) Circuit Diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.9
Cascade boost re-double circuit.

5.5 Triple Series

All circuits of P/O cascade boost converters — triple series — are derived from the corresponding circuits of the double series by adding the DEC twice in each stage circuit. The first three stages of this series are shown in Figure 5.9 to Figure 5.11. For convenience they are called elementary triple boost circuit, two-stage triple boost circuit, and three-stage triple boost circuit respectively, and numbered as $n = 1, 2$ and 3 .

5.5.1 Elementary Triple Boost Circuit

From the construction principle, the elementary triple boost circuit is derived from the elementary double boost circuit by adding another DEC. Its circuit

and switch-on and -off equivalent circuits are shown in [Figure 5.9](#). The output voltage of first stage boost circuit is V_1 , $V_1 = V_{in}/(1-k)$.

The voltage across capacitors C_1 and C_{11} is charged to V_1 and voltage across capacitors C_{12} and C_{13} is charged to $V_{C13} = 2V_1$. The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_1 - V_{in})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1} (1-k)T \quad (5.65)$$

$$V_1 = \frac{1}{1-k} V_{in}$$

The output voltage is

$$V_O = V_{C1} + V_{C13} = 3V_1 = \frac{3}{1-k} V_{in} \quad (5.66)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{3}{1-k} \quad (5.67)$$

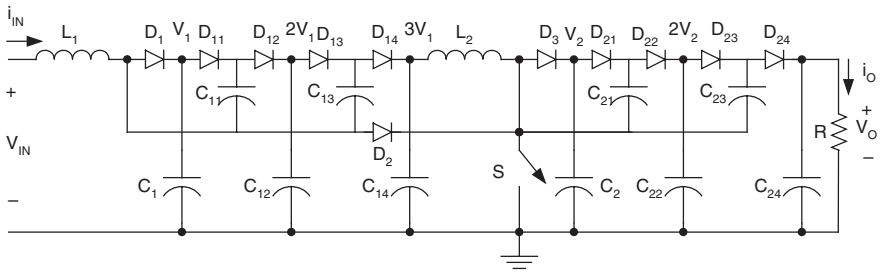
5.5.2 Two-Stage Triple Boost Circuit

The two-stage triple boost circuit is derived from the two-stage double boost circuit by adding another DEC in each stage circuit. Its circuit diagram and switch-on and -off equivalent circuits are shown in [Figure 5.10](#). As described in the previous section the voltage V_1 across capacitors C_1 and C_{11} is $V_1 = (1/(1-k))V_{in}$. The voltage across capacitor C_{14} is charged to $3V_1$.

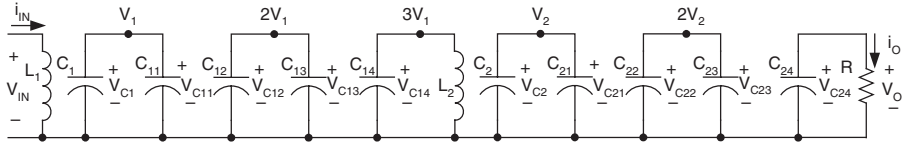
The voltage across capacitors C_2 and C_{21} is charged to V_2 and voltage across capacitors C_{22} and C_{23} is charged to $V_{C23} = 2V_2$. The current flowing through inductor L_2 increases with voltage $3V_1$ during switch-on period kT , and decreases with voltage $-(V_2 - 3V_1)$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{3V_1}{L_2} kT = \frac{V_2 - 3V_1}{L_2} (1-k)T \quad (5.68)$$

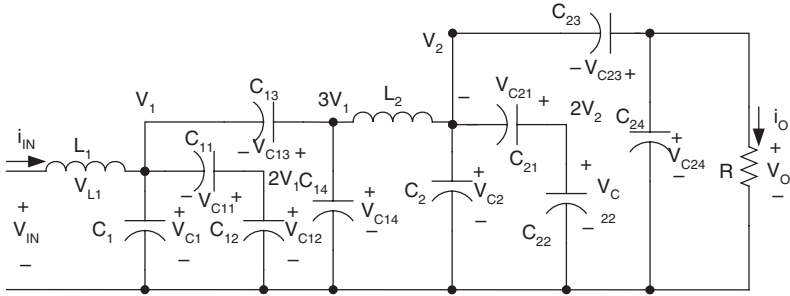
$$V_2 = \frac{3}{1-k} V_1 = 3\left(\frac{1}{1-k}\right)^2 V_{in} \quad (5.69)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.10

Two-stage boost re-double circuit.

The output voltage is

$$V_O = V_{C2} + V_{C23} = 3V_2 = \left(\frac{3}{1-k}\right)^2 V_{in} \quad (5.70)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{3}{1-k}\right)^2 \quad (5.71)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \left(\frac{2}{1-k}\right)^2 I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_O} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \quad (5.72)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \quad (5.73)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = \frac{I_O(1-k)T}{C_{22}} = \frac{1-k}{fC_{22}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{22}} \quad (5.74)$$

5.5.3 Three-Stage Triple Boost Circuit

This circuit is derived from the three-stage double boost circuit by adding another DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 5.11](#). As described earlier the voltage V_2 across capacitors C_2 and C_{11} is $V_2 = 3V_1 = (3/1-k)V_{in}$, and voltage across capacitor C_{24} is charged to $3V_2$.

The voltage across capacitors C_3 and C_{31} is charged to V_3 and voltage across capacitors C_{32} and C_{33} is charged to $V_{C33} = 2V_3$. The current flowing through inductor L_3 increases with voltage $3V_2$ during switch-on period kT and decreases with voltage $-(V_3 - 3V_2)$ during switch-off $(1-k)T$. Therefore, the ripple of the inductor current i_{L3} is

$$\Delta i_{L3} = \frac{3V_2}{L_3} kT = \frac{V_3 - 3V_2}{L_3} (1-k)T \quad (5.75)$$

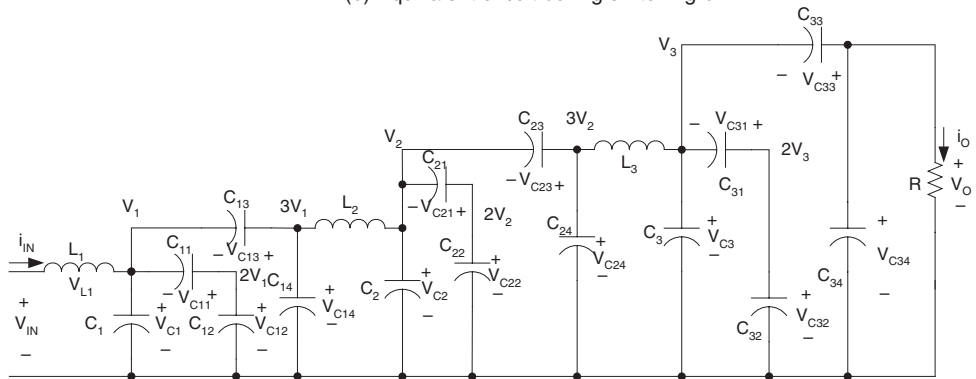
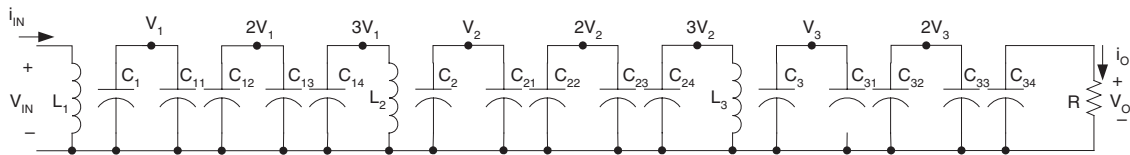
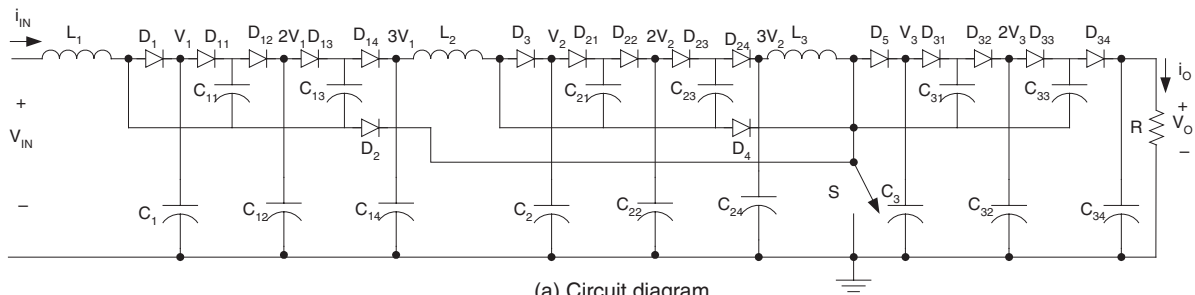


FIGURE 5.11

Three-stage boost re-double circuit.

and

$$V_3 = \frac{3}{1-k} V_2 = 9\left(\frac{1}{1-k}\right)^3 V_{in} \quad (5.76)$$

The output voltage is

$$V_O = V_{C3} + V_{C33} = 3V_3 = \left(\frac{3}{1-k}\right)^3 V_{in} \quad (5.77)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{3}{1-k}\right)^3 \quad (5.78)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{32}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{8}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2}{1-k} I_O$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{64L_1 I_O} = \frac{k(1-k)^6}{12^3} \frac{R}{fL_1} \quad (5.79)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{16L_2 I_O} = \frac{k(1-k)^4}{12^2} \frac{R}{fL_2} \quad (5.80)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k) TV_2}{4L_3 I_O} = \frac{k(1-k)^2}{12} \frac{R}{fL_3} \quad (5.81)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32}} = \frac{I_o(1-k)T}{C_{32}} = \frac{1-k}{fC_{32}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{32}} \quad (5.82)$$

5.5.4 Higher Stage Triple Boost Circuit

Higher stage triple boost circuits can be derived from the corresponding circuit of double boost series by adding another DEC in each stage circuit. For n th stage additional circuit, the final output voltage is

$$V_o = \left(\frac{3}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^n \quad (5.83)$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{L_i} / 2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{12^{(n-i+1)}} \frac{R}{fL_i} \quad (5.84)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{n2}} \quad (5.85)$$

5.6 Multiple Series

All circuits of P/O cascade boost converters — multiple series — are derived from the corresponding circuits of the main series by adding DEC multiple

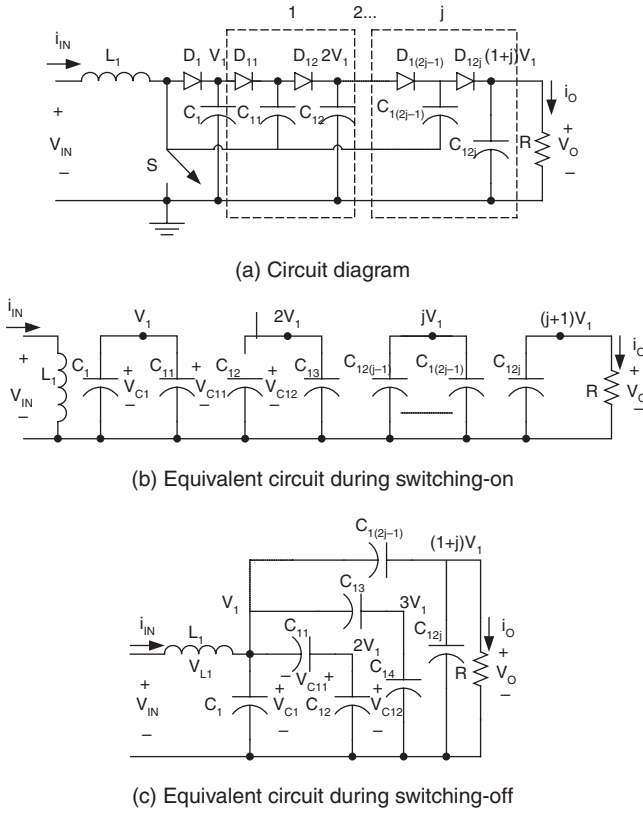


FIGURE 5.12
Cascade boost multiple-double circuit.

(j) times in each stage circuit. The first three stages of this series are shown in Figure 5.12 to Figure 5.14. For convenience they are called elementary multiple boost circuits, two-stage multiple boost circuits, and three-stage multiple boost circuits respectively, and numbered as $n = 1, 2$, and 3.

5.6.1 Elementary Multiple Boost Circuit

From the construction principle, the elementary multiple boost circuit is derived from the elementary boost converter by adding DEC multiple (j) times in the circuit. Its circuit and switch-on and -off equivalent circuits are shown in Figure 5.12.

The voltage across capacitors C_1 and C_{11} is charged to V_1 and voltage across capacitors C_{12} and C_{13} is charged to $V_{C13} = 2V_1$. The voltage across capacitors $C_{1(2j-2)}$ and $C_{1(2j-1)}$ is charged to $V_{C1(2j-1)} = jV_1$. The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_1 - V_{in})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1} (1-k)T \quad (5.86)$$

$$V_1 = \frac{1}{1-k} V_{in} \quad (5.87)$$

The output voltage is

$$V_O = V_{C1} + V_{C1(2j-1)} = (1+j)V_1 = \frac{1+j}{1-k} V_{in} \quad (5.88)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{1+j}{1-k} \quad (5.89)$$

5.6.2 Two-Stage Multiple Boost Circuit

The two-stage multiple boost circuit is derived from the two-stage boost circuit by adding multiple (j) DEC's in each stage circuit. Its circuit diagram and switch-on and -off equivalent circuits are shown in [Figure 5.13](#). The voltage across capacitor C_1 and capacitor C_{11} is charged to $V_1 = (1/(1-k))V_{in}$. The voltage across capacitor $C_{1(2j)}$ is charged to $(1+j)V_1$.

The current flowing through inductor L_2 increases with voltage $(1+j)V_1$ during switch-on period kT and decreases with voltage $-[V_2 - (1+j)V_1]$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{1+j}{L_2} kTV_1 = \frac{V_2 - (1+j)V_1}{L_2} (1-k)T \quad (5.90)$$

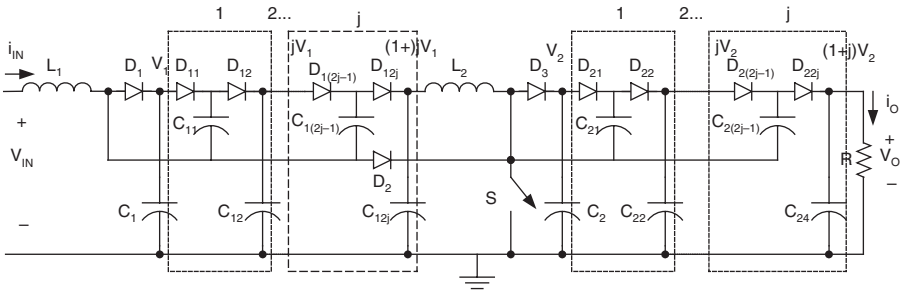
$$V_2 = \frac{1+j}{1-k} V_1 = (1+j)\left(\frac{1}{1-k}\right)^2 V_{in} \quad (5.91)$$

The output voltage is

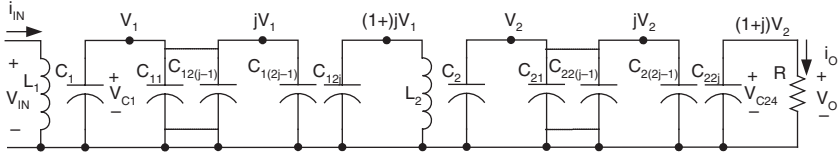
$$V_O = V_{C1} + V_{C1(2j-1)} = (1+j)V_2 = \left(\frac{1+j}{1-k}\right)^2 V_{in} \quad (5.92)$$

The voltage transfer gain is

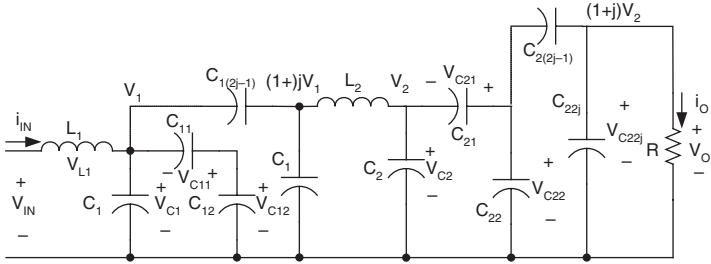
$$G = \frac{V_O}{V_{in}} = \left(\frac{1+j}{1-k}\right)^2 \quad (5.93)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.13

Two-stage boost multiple-double circuit.

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22j}} = \frac{I_o(1-k)T}{C_{22j}} = \frac{1-k}{fC_{22j}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{22j}} \quad (5.94)$$

5.6.3 Three-Stage Multiple Boost Circuit

This circuit is derived from the three-stage boost circuit by adding multiple (j) DEC's in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 5.14](#). The voltage across capacitor C_1 and capacitor C_{11} is charged to $V_1 = (1/(1-k))V_{in}$. The voltage across capacitor $C_{1(2j)}$ is charged to $(1+j)V_1$. The voltage V_2 across capacitor C_2 and capacitor $C_{2(2j)}$ is charged to $(1+j)V_2$.

The current flowing through inductor L_3 increases with voltage $(1+j)V_2$ during switch-on period kT and decreases with voltage $-[V_3 - (1+j)V_2]$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L3} = \frac{1+j}{L_3} kTV_2 = \frac{V_3 - (1+j)V_2}{L_3} (1-k)T \quad (5.95)$$

and

$$V_3 = \frac{(1+j)V_2}{(1-k)} = \frac{(1+j)^2}{(1-k)^3} V_{in} \quad (5.96)$$

The output voltage is

$$V_O = V_{C3} + V_{C3(2j-1)} = (1+j)V_3 = \left(\frac{1+j}{1-k}\right)^3 V_{in} \quad (5.97)$$

The voltage transfer gain is

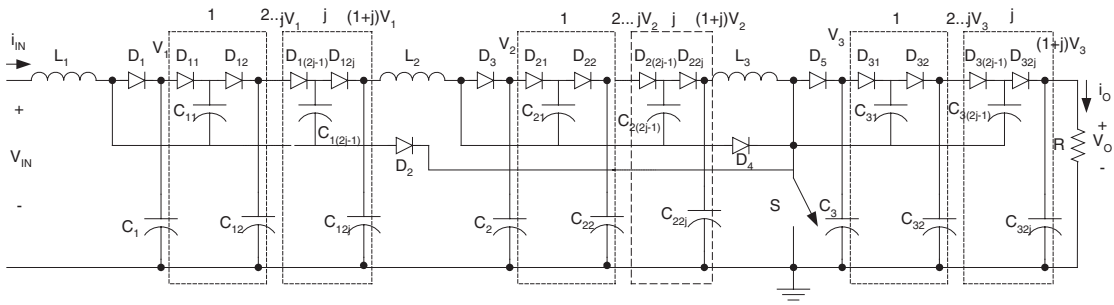
$$G = \frac{V_O}{V_{in}} = \left(\frac{1+j}{1-k}\right)^3 \quad (5.98)$$

The ripple voltage of output voltage v_o is

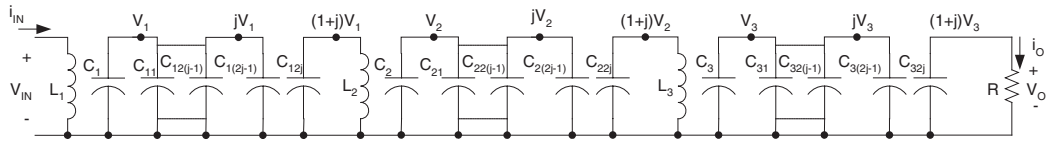
$$\Delta v_O = \frac{\Delta Q}{C_{32j}} = \frac{I_O(1-k)T}{C_{32j}} = \frac{1-k}{fC_{32j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

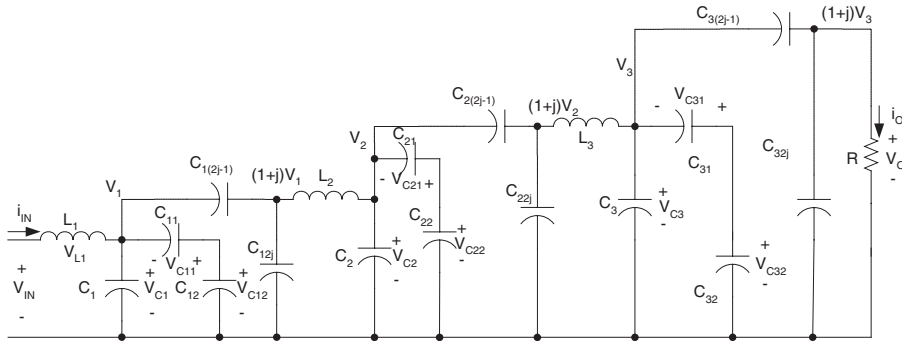
$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{32j}} \quad (5.99)$$



(a) Circuit Diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 5.14
Three-stage boost multiple-double circuit.

5.6.4 Higher Stage Multiple Boost Circuit

Higher stage multiple boost circuit is derived from the corresponding circuit of the main series by adding multiple (j) DEC's in each stage circuit. For n^{th} stage additional circuit, the final output voltage is

$$V_O = \left(\frac{1+j}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1+j}{1-k}\right)^n \quad (5.100)$$

Analogously, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{n2j}} \quad (5.101)$$

5.7 Summary of Positive Output Cascade Boost Converters

All circuits of the positive output cascade boost converters as a family are shown in [Figure 5.15](#) as the family tree. From the analysis of the previous two sections we have the common formula to calculate the output voltage:

$$V_O = \begin{cases} \left(\frac{1}{1-k}\right)^n V_{in} & \text{main_series} \\ 2 * \left(\frac{1}{1-k}\right)^n V_{in} & \text{additional_series} \\ \left(\frac{2}{1-k}\right)^n V_{in} & \text{double_series} \\ \left(\frac{3}{1-k}\right)^n V_{in} & \text{triple_series} \\ \left(\frac{j+1}{1-k}\right)^n V_{in} & \text{multiple}(j)_\text{series} \end{cases} \quad (5.102)$$

The voltage transfer gain is

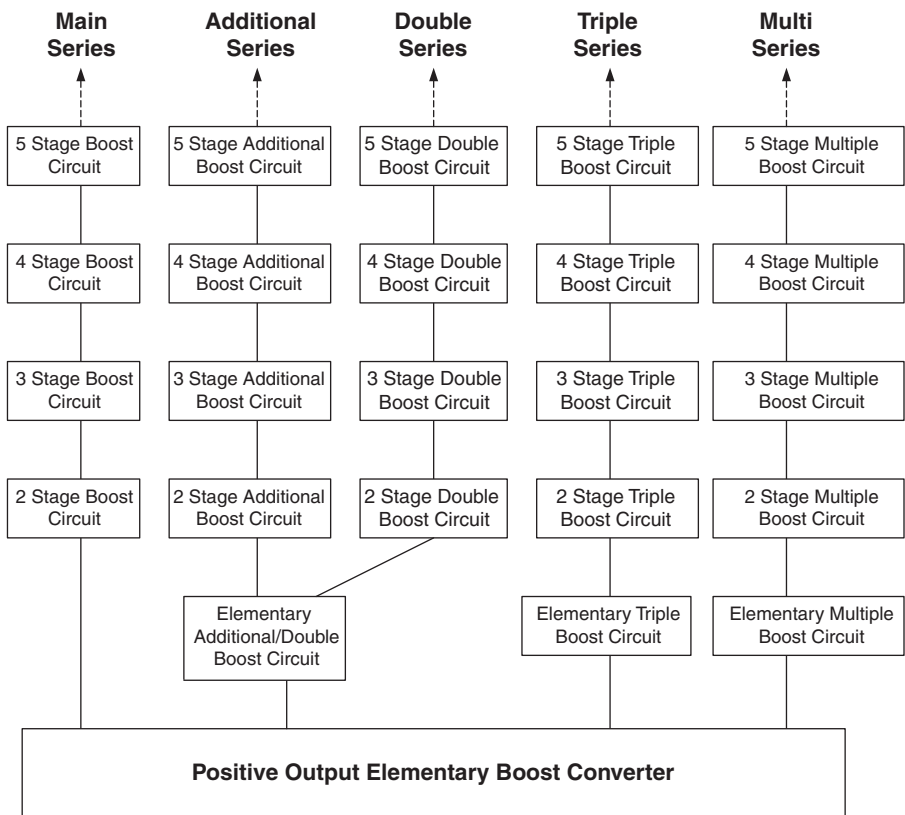


FIGURE 5.15

The family of positive output cascade boost converters

$$G = \frac{V_O}{V_{in}} = \begin{cases} \left(\frac{1}{1-k}\right)^n & \text{main_series} \\ 2 * \left(\frac{1}{1-k}\right)^n & \text{additional_series} \\ \left(\frac{2}{1-k}\right)^n & \text{double_series} \\ \left(\frac{3}{1-k}\right)^n & \text{triple_series} \\ \left(\frac{j+1}{1-k}\right)^n & \text{multiple}(j)_series \end{cases} \quad (5.103)$$

In order to show the advantages of the positive output cascade boost converters, we compare their voltage transfer gains to that of the buck converter,

$$G = \frac{V_O}{V_{in}} = k$$

forward converter,

$$G = \frac{V_o}{V_{in}} = kN \quad N \text{ is the transformer turn ratio}$$

Cúk-converter,

$$G = \frac{V_o}{V_{in}} = \frac{k}{1-k}$$

fly-back converter,

$$G = \frac{V_o}{V_{in}} = \frac{k}{1-k} N \quad N \text{ is the transformer turn ratio}$$

boost converter,

$$G = \frac{V_o}{V_{in}} = \frac{1}{1-k}$$

and positive output Luo-converters

$$G = \frac{V_o}{V_{in}} = \frac{n}{1-k} \quad (5.104)$$

If we assume that the conduction duty k is 0.2, the output voltage transfer gains are listed in [Table 5.1](#); if the conduction duty k is 0.5, the output voltage transfer gains are listed in [Table 5.2](#); if the conduction duty k is 0.8, the output voltage transfer gains are listed in [Table 5.3](#).

5.8 Simulation and Experimental Results

5.8.1 Simulation Results of a Three-Stage Boost Circuit

To verify the design and calculation results, the PSpice simulation package was applied to a three-stage boost converter. Choosing $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F, and $R = 30$ k Ω , $k = 0.7$ and $f = 100$ kHz. The

TABLE 5.1

Voltage Transfer Gains of Converters in the Condition $k = 0.2$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.2		
Forward converter		$0.2N$ (N is the transformer turn ratio)				
Cúk-converter			0.25			
Fly-back converter		$0.25N$ (N is the transformer turn ratio)				
Boost converter			1.25			
Positive output Luo-converters	1.25	2.5	3.75	5	6.25	$1.25n$
Positive output cascade boost converters — main series	1.25	1.563	1.953	2.441	3.052	1.25^n
Positive output cascade boost converters — additional series	2.5	3.125	3.906	4.882	6.104	$2 * 1.25^n$
Positive output cascade boost converters — double series	2.5	6.25	15.625	39.063	97.66	$(2 * 1.25)^n$
Positive output cascade boost converters — triple series	3.75	14.06	52.73	197.75	741.58	$(3 * 1.25)^n$
Positive output cascade boost ($j = 3$) converters — multiple series	5	25	125	625	3125	$(4 * 1.25)^n$

TABLE 5.2

Voltage Transfer Gains of Converters in the Condition $k = 0.5$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.5		
Forward converter		$0.5N$ (N is the transformer turn ratio)				
Cúk-converter			1			
Fly-back converter		N (N is the transformer turn ratio)				
Boost converter			2			
Positive output Luo-converters	2	4	6	8	10	$2n$
Positive output cascade boost converters — main series	2	4	8	16	32	2^n
Positive output cascade boost converters — additional series	4	8	16	32	64	$2 * 2^n$
Positive output cascade boost converters — double series	4	16	64	256	1024	$(2 * 2)^n$
Positive output cascade boost converters — triple series	6	36	216	1296	7776	$(3 * 2)^n$
Positive output cascade boost ($j = 3$) converters — multiple series	8	64	512	4096	32,768	$(4 * 2)^n$

obtained voltage values V_1 , V_2 , and V_O of a triple-lift circuit are 66 V, 194 V, and 659 V respectively and inductor current waveforms i_{L1} (its average value $I_{L1} = 618$ mA), i_{L2} , and i_{L3} . The simulation results are shown in [Figure 5.16](#). The voltage values match the calculated results.

TABLE 5.3

Voltage Transfer Gains of Converters in the Condition $k = 0.8$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.8		
Forward converter		$0.8N$ (N is the transformer turn ratio)				
Cúk-converter				4		
Fly-back converter		$4N$ (N is the transformer turn ratio)				
Boost converter				5		
Positive output Luo-converters	5	10	15	20	25	$5n$
Positive output cascade boost converters — main series	5	25	125	625	3125	5^n
Positive output cascade boost converters — additional series	10	50	250	1250	6250	$2 \cdot 5^n$
Positive output cascade boost converters — double series	10	100	1000	10,000	100,000	$(2 \cdot 5)^n$
Positive output cascade boost converters — triple series	15	225	3375	50,625	759,375	$(3 \cdot 5)^n$
Positive output cascade boost ($j=3$) converters — multiple series	20	400	8000	160,000	$32 \cdot 10^5$	$(4 \cdot 5)^n$

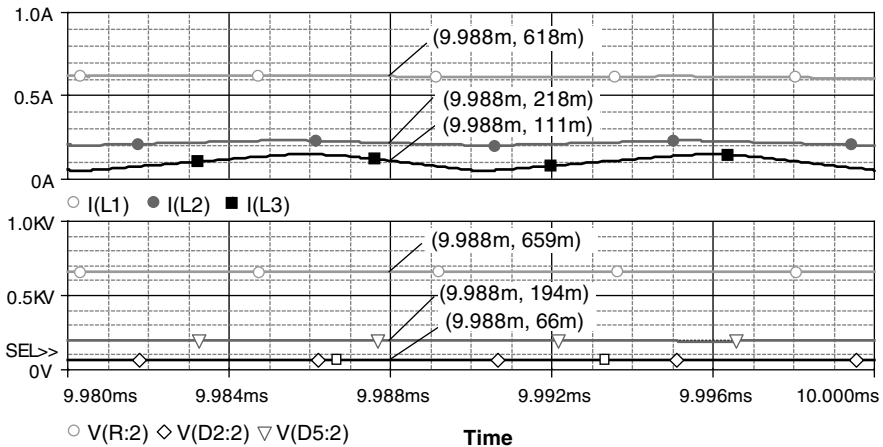


FIGURE 5.16

The simulation results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

5.8.2 Experimental Results of a Three-Stage Boost Circuit

A test rig was constructed to verify the design and calculation results, and compared with PSpice simulation results. The test conditions are still $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F and $R = 30$ k Ω , $k = 0.7$, and $f = 100$ kHz. The component of the switch is a MOSFET device IRF950 with the rate 950 V/5 A/2 MHz. The measured values of the output voltage and

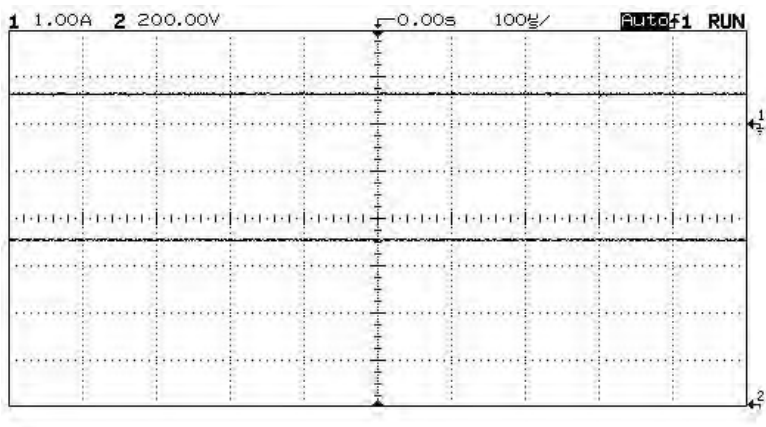


FIGURE 5.17

The experimental results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz

TABLE 5.4

Comparison of Simulation and Experimental Results of a Triple-Lift Circuit

Stage No. (n)	I_{L1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_O (V)	P_O (W)	η (%)
Simulation results	0.618	0.927	20	18.54	659	14.47	78
Experimental results	0.62	0.93	20	18.6	660	14.52	78

first inductor current in a three-stage boost converter. After careful measurement, we obtained the current value of $I_{L1} = 0.62$ A (shown in channel 1 with 1 A/Div) and voltage value of $V_O = 660$ V (shown in channel 2 with 200 V/Div). The experimental results (current and voltage values) in Figure 5.17 match the calculated and simulation results, which are $I_{L1} = 0.618$ A and $V_O = 659$ V shown in [Figure 5.16](#).

5.8.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully, and efficiently. Particularly, the efficiency of the tested circuits is 78%, which is good for high voltage output equipment. Comparison of the simulation and experimental results is shown in Table 5.4.

5.8.4 Transient Process

Usually, there is high inrush current during the first power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick taking only a few milliseconds.

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Negative Output Cascade Boost Converters

6.1 Introduction

This chapter introduces negative output cascade boost converters. Just as with positive output cascade boost converters these converters use the super-lift technique. There are several sub-series:

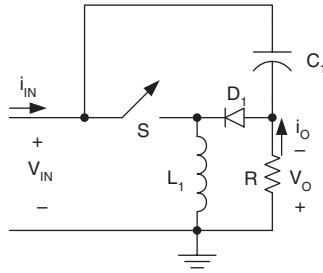
- Main series — Each circuit of the main series has one switch S , n inductors, n capacitors, and $(2n - 1)$ diodes.
- Additional series — Each circuit of the additional series has one switch S , n inductors, $(n + 2)$ capacitors, and $(2n + 1)$ diodes.
- Double series — Each circuit of the double series has one switch S , n inductors, $3n$ capacitors, and $(3n - 1)$ diodes.
- Triple series — Each circuit of the triple series has one switch S , n inductors, $5n$ capacitors, and $(5n - 1)$ diodes.
- Multiple series — Multiple series circuits have one switch S and a higher number of capacitors and diodes.

The conduction duty ratio is k , switching frequency is f , switching period is $T = 1/f$, the load is resistive load R . The input voltage and current are V_{in} and I_{in} , output voltage and current are V_O and I_O . Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_O \times I_O$. The voltage transfer gain is G :

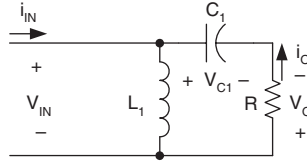
$$G = \frac{V_O}{V_{in}}$$

6.2 Main Series

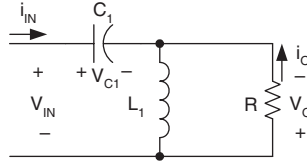
The first three stages of the negative output cascade boost converters — main series — are shown in [Figure 6.1](#) to [Figure 6.3](#). For convenience they are



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.1

Elementary boost converter.

called elementary boost converter, two-stage boost circuit and three-stage boost circuit respectively, and numbered as $n = 1, 2$ and 3 .

6.2.1 N/O Elementary Boost Circuit

The N/O elementary boost converter and its equivalent circuits during switch-on and -off are shown in Figure 6.1. The voltage across capacitor C_1 is charged to V_{C1} . The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_{C1} - V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L1} is

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_{C1} - V_{in}}{L_1} (1 - k)T \quad (6.1)$$

$$V_{C1} = \frac{1}{1 - k} V_{in}$$

$$V_O = V_{C1} - V_{in} = \frac{k}{1-k} V_{in} \quad (6.2)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{1}{1-k} - 1 \quad (6.3)$$

The inductor average current is

$$I_{L1} = (1-k) \frac{V_O}{R} \quad (6.4)$$

The variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_{in}}{(1-k)2L_1V_O / R} = \frac{k}{2} \frac{R}{fL_1} \quad (6.5)$$

Usually ξ_1 is small (much lower than unity), it means this converter works in the continuous mode.

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_1} = \frac{I_O(1-k)T}{C_1} = \frac{1-k}{fC_1} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

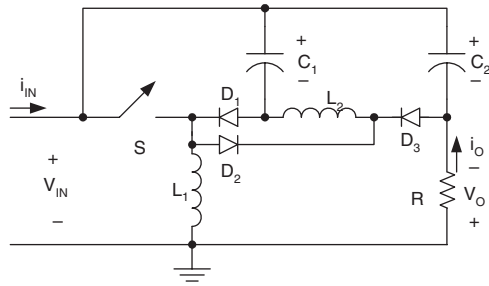
$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_1} \quad (6.6)$$

Usually R is in $k\Omega$, f in 10 kHz, and C_1 in μF , this ripple is smaller than 1%.

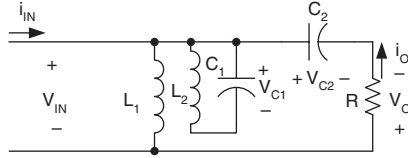
6.2.2 N/O Two-Stage Boost Circuit

The N/O two-stage boost circuit is derived from elementary boost converter by adding the parts (L_2 - D_2 - D_3 - C_2). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 6.2](#). The voltage across capacitor C_1 is charged to V_1 . As described in the previous section the voltage V_1 across capacitor C_1 is

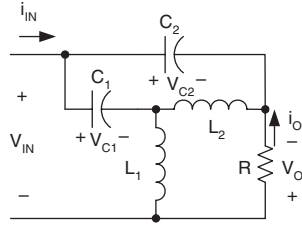
$$V_1 = \frac{1}{1-k} V_{in}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.2

Two-stage boost circuit.

The voltage across capacitor C_2 is charged to V_{C2} . The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_{C2} - V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_1}{L_2} kT = \frac{V_{C2} - V_1}{L_2} (1 - k)T \quad (6.7)$$

$$V_{C2} = \frac{1}{1 - k} V_1 = \left(\frac{1}{1 - k}\right)^2 V_{in}$$

$$V_O = V_{C2} - V_{in} = \left[\left(\frac{1}{1 - k}\right)^2 - 1\right] V_{in} \quad (6.8)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1-k}\right)^2 - 1 \quad (6.9)$$

Analogously,

$$\begin{aligned} \Delta i_{L1} &= \frac{V_{in}}{L_1} kT & I_{L1} &= \frac{I_O}{(1-k)^2} \\ \Delta i_{L2} &= \frac{V_1}{L_2} kT & I_{L2} &= \frac{I_O}{1-k} \end{aligned}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{2L_1 I_O} = \frac{k(1-k)^4}{2} \frac{R}{fL_1} \quad (6.10)$$

the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{2L_2 I_O} = \frac{k(1-k)^2}{2} \frac{R}{fL_2} \quad (6.11)$$

and the variation ratio of output voltage v_O is

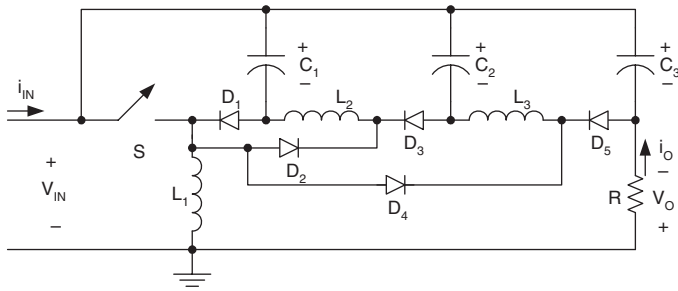
$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_2} \quad (6.12)$$

6.2.3 N/O Three-Stage Boost Circuit

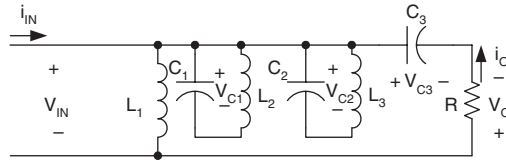
The N/O three-stage boost circuit is derived from the two-stage boost circuit by double adding the parts (L_2 - D_2 - D_3 - C_2). Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 6.3](#). The voltage across capacitor C_1 is charged to V_1 . As described previously the voltage V_{C1} across capacitor C_1 is $V_{C1} = (1/1-k)V_{in}$, and voltage V_{C2} across capacitor C_2 is $V_{C2} = (1/1-k)^2 V_{in}$.

The voltage across capacitor C_3 is charged to V_O . The current flowing through inductor L_3 increases with voltage V_{C2} during switch-on period kT and decreases with voltage $-(V_{C3} - V_{C2})$ during switch-off $(1-k)T$. Therefore, the ripple of the inductor current i_{L3} is

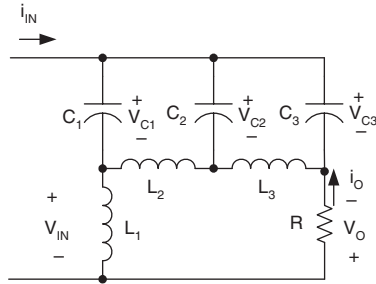
$$\Delta i_{L3} = \frac{V_{C2}}{L_3} kT = \frac{V_{C3} - V_{C2}}{L_3} (1-k)T \quad (6.13)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.3

Three-stage boost circuit.

$$V_{C3} = \frac{1}{1-k} V_{C2} = \left(\frac{1}{1-k}\right)^2 V_{C1} = \left(\frac{1}{1-k}\right)^3 V_{in}$$

$$V_O = V_{C3} - V_{in} = \left[\left(\frac{1}{1-k}\right)^3 - 1\right] V_{in} \quad (6.14)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1-k}\right)^3 - 1 \quad (6.15)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{I_O}{(1-k)^3}$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{I_O}{(1-k)^2}$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{2L_1 I_O} = \frac{k(1-k)^6}{2} \frac{R}{fL_1} \quad (6.16)$$

the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{2L_2 I_O} = \frac{k(1-k)^4}{2} \frac{R}{fL_2} \quad (6.17)$$

the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k) TV_2}{2L_3 I_O} = \frac{k(1-k)^2}{2} \frac{R}{fL_3} \quad (6.18)$$

and the variation ratio of output voltage v_O is

$$\epsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_3} \quad (6.19)$$

6.2.4 N/O Higher Stage Boost Circuit

N/O higher stage boost circuit can be designed by multiple repetition of the parts (L_2 - D_2 - D_3 - C_2). For n th stage boost circuit, the final output voltage across capacitor C_n is

$$V_O = \left[\left(\frac{1}{1-k} \right)^n - 1 \right] V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1-k}\right)^n - 1 \quad (6.20)$$

the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{2} \frac{R}{fL_i} \quad (6.21)$$

and the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_n} \quad (6.22)$$

6.3 Additional Series

All circuits of negative output cascade boost converters — additional series — are derived from the corresponding circuits of the main series by adding a DEC.

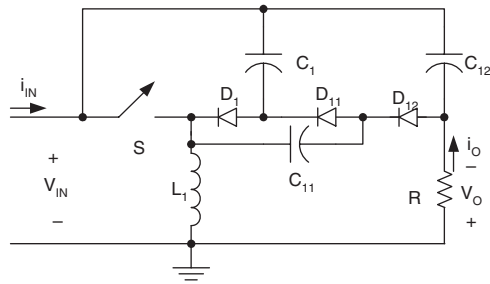
The first three stages of this series are shown in [Figure 6.4](#) to [Figure 6.6](#). For convenience they are called elementary additional boost circuit, two-stage additional boost circuit, and three-stage additional boost circuit respectively, and numbered as $n = 1, 2$ and 3 .

6.3.1 N/O Elementary Additional Boost Circuit

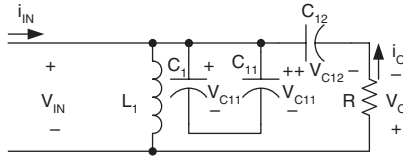
This N/O elementary boost additional circuit is derived from N/O elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 6.4](#). The voltage across capacitor C_1 and C_{11} is charged to V_{C1} and voltage across capacitor C_{12} is charged to $V_{C12} = 2V_{C1}$. The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_{C1} - V_{in})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_{C1} - V_{in}}{L_1} (1-k)T \quad (6.23)$$

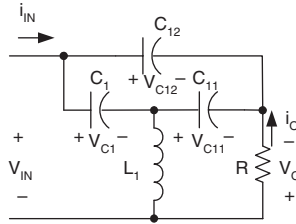
$$V_{C1} = \frac{1}{1-k} V_{in}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.4

Elementary boost additional (double) circuit.

The voltage V_{C12} is

$$V_{C12} = 2V_{C1} = \frac{2}{1-k} V_{in} \quad (6.24)$$

The output voltage is

$$V_O = V_{C12} - V_{in} = \left[\frac{2}{1-k} - 1 \right] V_{in} \quad (6.25)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{2}{1-k} - 1 \quad (6.26)$$

The variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)TV_{in}}{4L_1 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_1} \quad (6.27)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (6.28)$$

6.3.2 N/O Two-Stage Additional Boost Circuit

The N/O two-stage additional boost circuit is derived from the N/O two-stage boost circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in [Figure 6.5](#). The voltage across capacitor C_1 is charged to V_{C1} . As described in the previous section the voltage V_{C1} across capacitor C_1 is

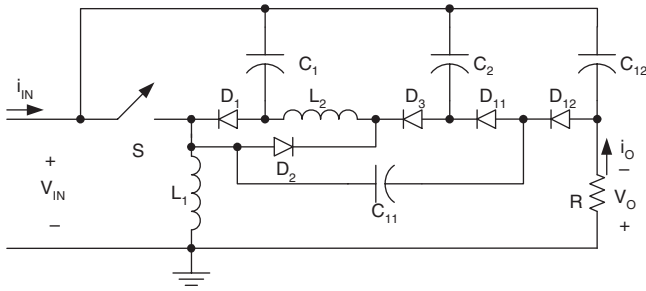
$$V_{C1} = \frac{1}{1-k} V_{in}$$

The voltage across capacitor C_2 and capacitor C_{11} is charged to V_{C2} and voltage across capacitor C_{12} is charged to V_{C12} . The current flowing through inductor L_2 increases with voltage V_{C1} during switch-on period kT and decreases with voltage $-(V_{C2} - V_{C1})$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

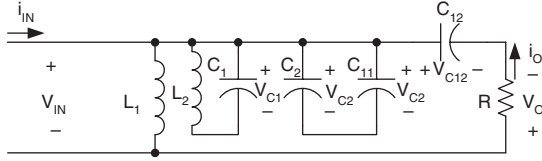
$$\Delta i_{L2} = \frac{V_{C1}}{L_2} kT = \frac{V_{C2} - V_{C1}}{L_2} (1-k)T \quad (6.29)$$

$$V_{C2} = \frac{1}{1-k} V_{C1} = \left(\frac{1}{1-k}\right)^2 V_{in} \quad (6.30)$$

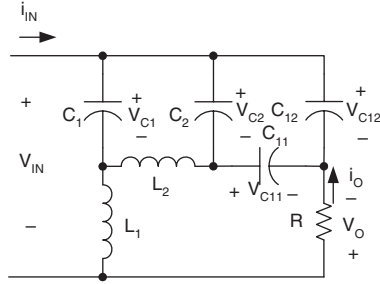
$$V_{C12} = 2V_{C2} = \frac{2}{1-k} V_{C1} = 2\left(\frac{1}{1-k}\right)^2 V_{in}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.5

Two-stage additional boost circuit.

The output voltage is

$$V_O = V_{C12} - V_{in} = [2(\frac{1}{1-k})^2 - 1]V_{in} \quad (6.31)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = 2(\frac{1}{1-k})^2 - 1 \quad (6.32)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{2}{(1-k)^2} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{4L_1 I_O} = \frac{k(1-k)^4}{8} \frac{R}{fL_1} \quad (6.33)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \quad (6.34)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

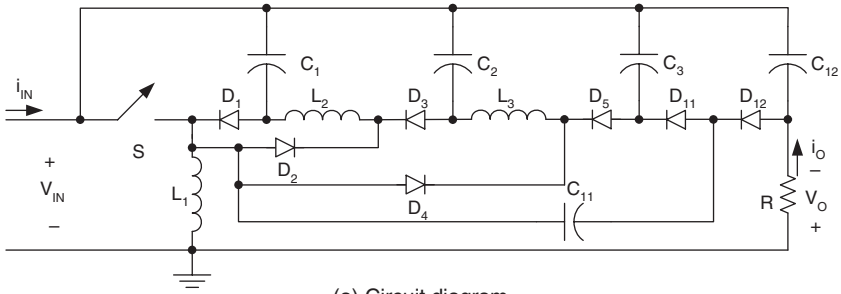
$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (6.35)$$

6.3.3 N/O Three-Stage Additional Boost Circuit

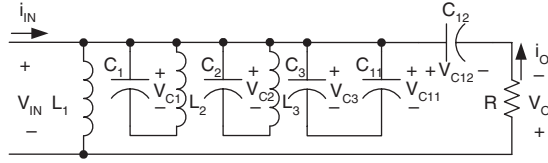
This N/O circuit is derived from three-stage boost circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 6.6](#). The voltage across capacitor C_1 is charged to V_{C1} . As described previously, the voltage V_{C1} across capacitor C_1 is $V_{C1} = (1/1-k)V_{in}$, and voltage V_2 across capacitor C_2 is $V_{C2} = (1/1-k)^2 V_{in}$.

The voltage across capacitor C_3 and capacitor C_{11} is charged to V_{C3} . The voltage across capacitor C_{12} is charged to V_{C12} . The current flowing through inductor L_3 increases with voltage V_{C2} during switch-on period kT and decreases with voltage $-(V_{C3} - V_{C2})$ during switch-off $(1-k)T$. Therefore,

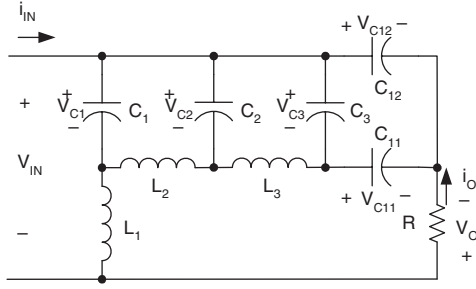
$$\Delta i_{L3} = \frac{V_{C2}}{L_3} kT = \frac{V_{C3} - V_{C2}}{L_3} (1-k)T \quad (6.36)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.6

Three-stage additional boost circuit.

and

$$V_{C3} = \frac{1}{1-k} V_{C2} = \left(\frac{1}{1-k}\right)^2 V_{C1} = \left(\frac{1}{1-k}\right)^3 V_{in} \quad (6.37)$$

The voltage V_{C12} is

$$V_{C12} = 2V_{C3} = 2\left(\frac{1}{1-k}\right)^3 V_{in}$$

The output voltage is

$$V_O = V_{C12} - V_{in} = [2\left(\frac{1}{1-k}\right)^3 - 1]V_{in} \quad (6.38)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = 2\left(\frac{1}{1-k}\right)^3 - 1 \quad (6.39)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{2}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{4L_1 I_O} = \frac{k(1-k)^6}{8} \frac{R}{fL_1} \quad (6.40)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{4L_2 I_O} = \frac{k(1-k)^4}{8} \frac{R}{fL_2} \quad (6.41)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k) TV_2}{4L_3 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_3} \quad (6.42)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{12}} = \frac{I_O(1-k)T}{C_{12}} = \frac{1-k}{fC_{12}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (6.43)$$

6.3.4 N/O Higher Stage Additional Boost Circuit

The N/O higher stage boost additional circuit is derived from the corresponding circuit of the main series by adding a DEC. For the n th stage additional circuit, the final output voltage is

$$V_O = [2(\frac{1}{1-k})^n - 1]V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = 2(\frac{1}{1-k})^n - 1 \quad (6.44)$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{L_i} / 2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{8} \frac{R}{fL_i} \quad (6.45)$$

and the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{12}} \quad (6.46)$$

6.4 Double Series

All circuits of N/O cascade boost converters — double series — are derived from the corresponding circuits of the main series by adding a DEC in each stage circuit. The first three stages of this series are shown in [Figures 6.4, 6.7, and 6.8](#). For convenience they are called elementary double boost circuit, two-stage double boost circuit, and three-stage double boost circuit respectively, and numbered as $n = 1, 2$ and 3 .

6.4.1 N/O Elementary Double Boost Circuit

This N/O elementary double boost circuit is derived from the elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 6.4, which is the same as the elementary boost additional circuit.

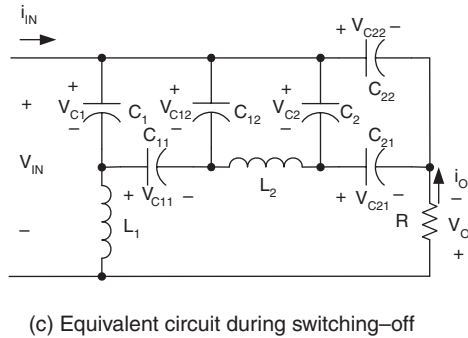
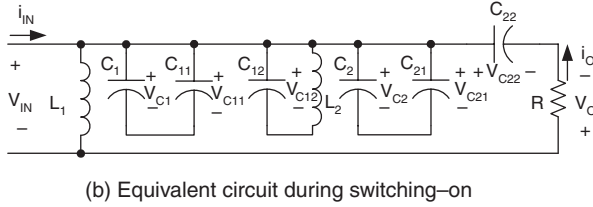
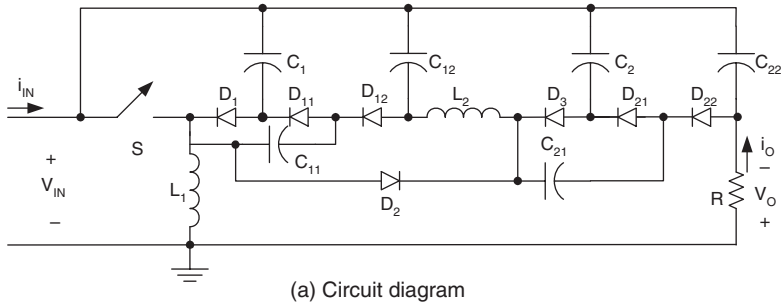


FIGURE 6.7
Two-stage double boost circuit.

6.4.2 N/O Two-Stage Double Boost Circuit

The N/O two-stage double boost circuit is derived from two-stage boost circuit by adding a DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 6.7. The voltage across capacitor C_1 and capacitor C_{11} is charged to V_1 . As described in the previous section the voltage V_{C1} across capacitor C_1 and capacitor C_{11} is $V_{C1} = (1/k)V_{in}$. The voltage across capacitor C_{12} is charged to $2V_{C1}$.

The current flowing through inductor L_2 increases with voltage $2V_{C1}$ during switch-on period kT and decreases with voltage $-(V_{C2} - 2V_{C1})$ during switch-off period $(1-k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{2V_{C1}}{L_2} kT = \frac{V_{C2} - 2V_{C1}}{L_2} (1-k)T \quad (6.47)$$

$$V_{C2} = \frac{2}{1-k} V_{C1} = 2\left(\frac{1}{1-k}\right)^2 V_{in} \quad (6.48)$$

The voltage V_{C22} is

$$V_{C22} = 2V_{C2} = \left(\frac{2}{1-k}\right)^2 V_{in}$$

The output voltage is

$$V_O = V_{C22} - V_{in} = \left[\left(\frac{2}{1-k}\right)^2 - 1\right] V_{in} \quad (6.49)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2}{1-k}\right)^2 - 1 \quad (6.50)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \left(\frac{2}{1-k}\right)^2 I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

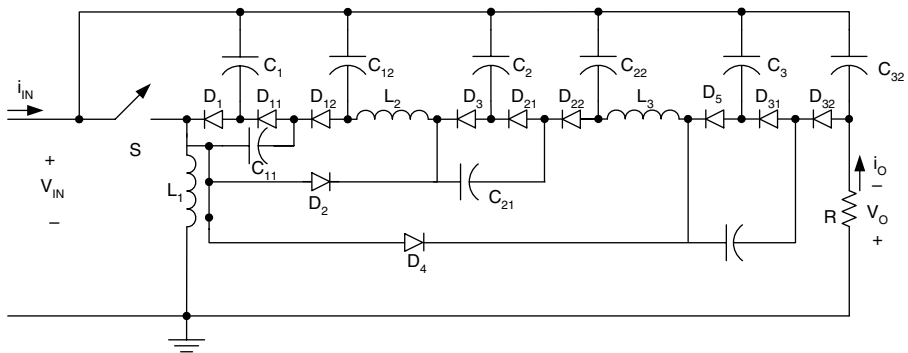
$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_O} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \quad (6.51)$$

and the variation ratio of current i_{L2} through inductor L_2 is

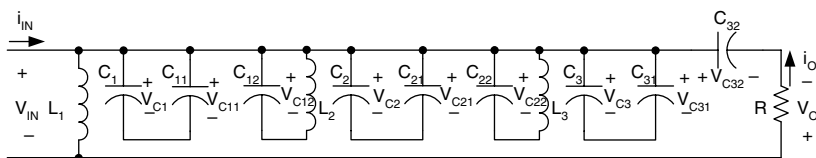
$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \quad (6.52)$$

The ripple voltage of output voltage v_O is

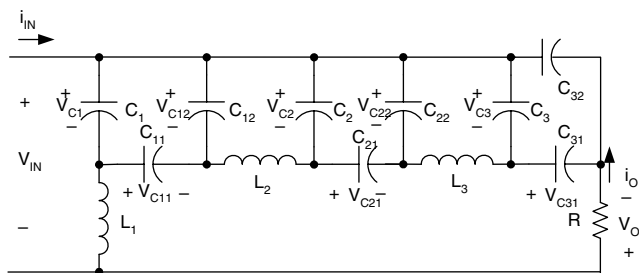
$$\Delta v_O = \frac{\Delta Q}{C_{22}} = \frac{I_O(1-k)T}{C_{22}} = \frac{1-k}{fC_{22}} \frac{V_O}{R}$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.8

Three-stage double boost circuit.

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{22}} \quad (6.53)$$

6.4.3 N/O Three-Stage Double Boost Circuit

This N/O circuit is derived from the three-stage boost circuit by adding DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.8. The voltage across capacitor C_1 and capacitor C_{11} is charged to V_{C1} . As described previously, the voltage V_{C1} across capacitor C_1 and capacitor C_{11} is $V_{C1} = (1/(1-k))V_{in}$, and voltage V_{C2} across capacitor C_2 and capacitor C_{12} is $V_{C2} = 2(1/(1-k))^2 V_{in}$.

The voltage across capacitor C_{22} is $2V_{C2} = (2/1-k)^2 V_{in}$. The voltage across capacitor C_3 and capacitor C_{31} is charged to V_3 . The voltage across capacitor C_{12} is charged to V_O . The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_{C3} - 2V_{C2})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L3} = \frac{2V_{C2}}{L_3} kT = \frac{V_{C3} - 2V_{C2}}{L_3} (1-k)T \quad (6.54)$$

and

$$V_{C3} = \frac{2V_{C2}}{(1-k)} = \frac{4}{(1-k)^3} V_{in} \quad (6.55)$$

The voltage V_{C32} is

$$V_{C32} = 2V_{C3} = \left(\frac{2}{1-k}\right)^3 V_{in}$$

The output voltage is

$$V_O = V_{C32} - V_{in} = \left[\left(\frac{2}{1-k}\right)^3 - 1\right] V_{in} \quad (6.56)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{2}{1-k}\right)^3 - 1 \quad (6.57)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{8}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{4}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{16L_1 I_O} = \frac{k(1-k)^6}{128} \frac{R}{fL_1} \quad (6.58)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{8L_2 I_O} = \frac{k(1-k)^4}{32} \frac{R}{fL_2} \quad (6.59)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k)TV_2}{4L_3 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_3} \quad (6.60)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32}} = \frac{I_O(1-k)T}{C_{32}} = \frac{1-k}{fC_{32}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{32}} \quad (6.61)$$

6.4.4 N/O Higher Stage Double Boost Circuit

The N/O higher stage double boost circuit is derived from the corresponding circuit of the main series by adding DEC in each stage circuit. For n th stage additional circuit, the final output voltage is

$$V_O = [(\frac{2}{1-k})^n - 1]V_{in}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = (\frac{2}{1-k})^n - 1 \quad (6.62)$$

Analogously, the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{2 * 2^{2n}} \frac{R}{fL_i} \quad (6.63)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{n2}} \quad (6.64)$$

6.5 Triple Series

All circuits of N/O cascade boost converters — triple series — are derived from the corresponding circuits of the main series by adding DEC twice in each stage circuit. The first three stages of this series are shown in [Figure 6.9](#) to [Figure 6.11](#). For convenience they are called elementary triple boost (or additional) circuit, two-stage triple boost circuit, and three-stage triple boost circuit respectively, and numbered as $n = 1, 2$ and 3 .

6.5.1 N/O Elementary Triple Boost Circuit

This N/O elementary triple boost circuit is derived from the elementary boost converter by adding DEC twice. Its circuit and switch-on and switch-off equivalent circuits are shown in [Figure 6.9](#). The output voltage of the first stage boost circuit is V_{C1} , $V_{C1} = V_{in}/(1-k)$.

After the first DEC, the voltage (across capacitor C_{12}) increases to

$$V_{C12} = 2V_{C1} = \frac{2}{1-k} V_{in} \quad (6.65)$$

After the second DEC, the voltage (across capacitor C_{14}) increases to

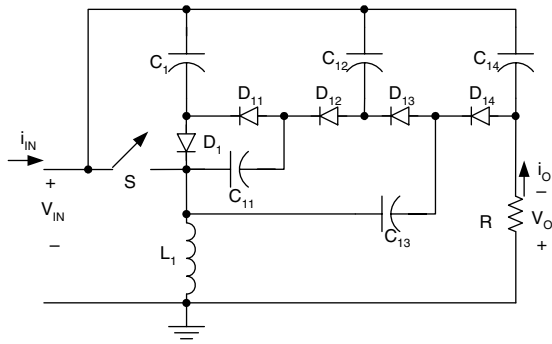
$$V_{C14} = V_{C12} + V_{C1} = \frac{3}{1-k} V_{in} \quad (6.66)$$

The final output voltage V_o is equal to

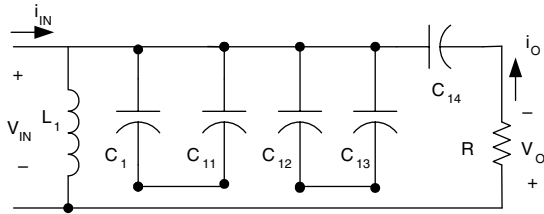
$$V_o = V_{C14} - V_{in} = \left[\frac{3}{1-k} - 1 \right] V_{in} \quad (6.67)$$

The voltage transfer gain is

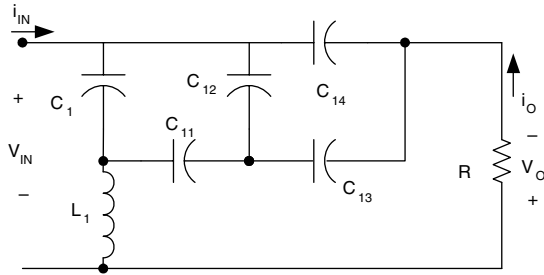
$$G = \frac{V_o}{V_{in}} = \frac{3}{1-k} - 1 \quad (6.68)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.9

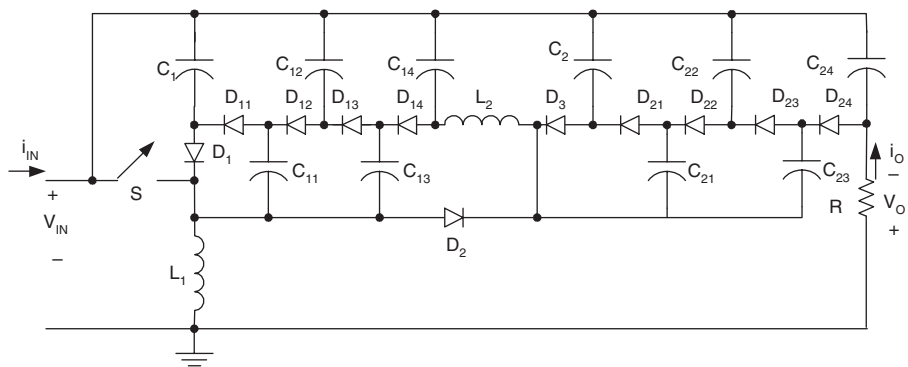
Elementary triple boost circuit.

6.5.2 N/O Two-Stage Triple Boost Circuit

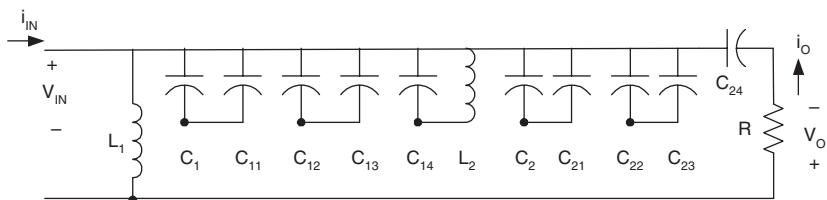
The N/O two-stage triple boost circuit is derived from two-stage boost circuit by adding DEC twice in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 6.10.

As described in the previous section the voltage across capacitor C_{14} is $V_{C14} = (3/1-k)V_{in}$. Analogously, the voltage across capacitor C_{24} is.

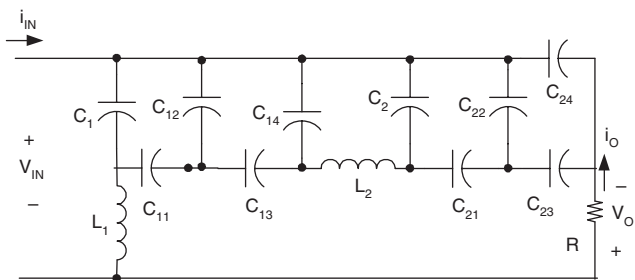
$$V_{C24} = \left(\frac{3}{1-k}\right)^2 V_{in} \quad (6.69)$$



(a) Circuit diagram



(b) Switch on



(c) Switch off

FIGURE 6.10

Two-stage triple boost circuit.

The final output voltage V_O is equal to

$$V_O = V_{C24} - V_{in} = \left[\left(\frac{3}{1-k} \right)^2 - 1 \right] V_{in} \quad (6.70)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{3}{1-k} \right)^2 - 1 \quad (6.71)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \left(\frac{2}{1-k}\right)^2 I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{2I_O}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_O} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \quad (6.72)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)TV_1}{4L_2 I_O} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \quad (6.73)$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = \frac{I_O(1-k)T}{C_{22}} = \frac{1-k}{fC_{22}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{22}} \quad (6.74)$$

6.5.3 N/O Three-Stage Triple Boost Circuit

This N/O circuit is derived from the three-stage boost circuit by adding DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 6.11](#).

As described in the previous section the voltage across capacitor C_{14} is $V_{C14} = (3/1-k)V_{in}$, and the voltage across capacitor C_{24} is $V_{C24} = (3/1-k)^2 V_{in}$. Analogously, the voltage across capacitor C_{34} is

$$V_{C34} = \left(\frac{3}{1-k}\right)^3 V_{in} \quad (6.75)$$

The final output voltage V_O is equal to

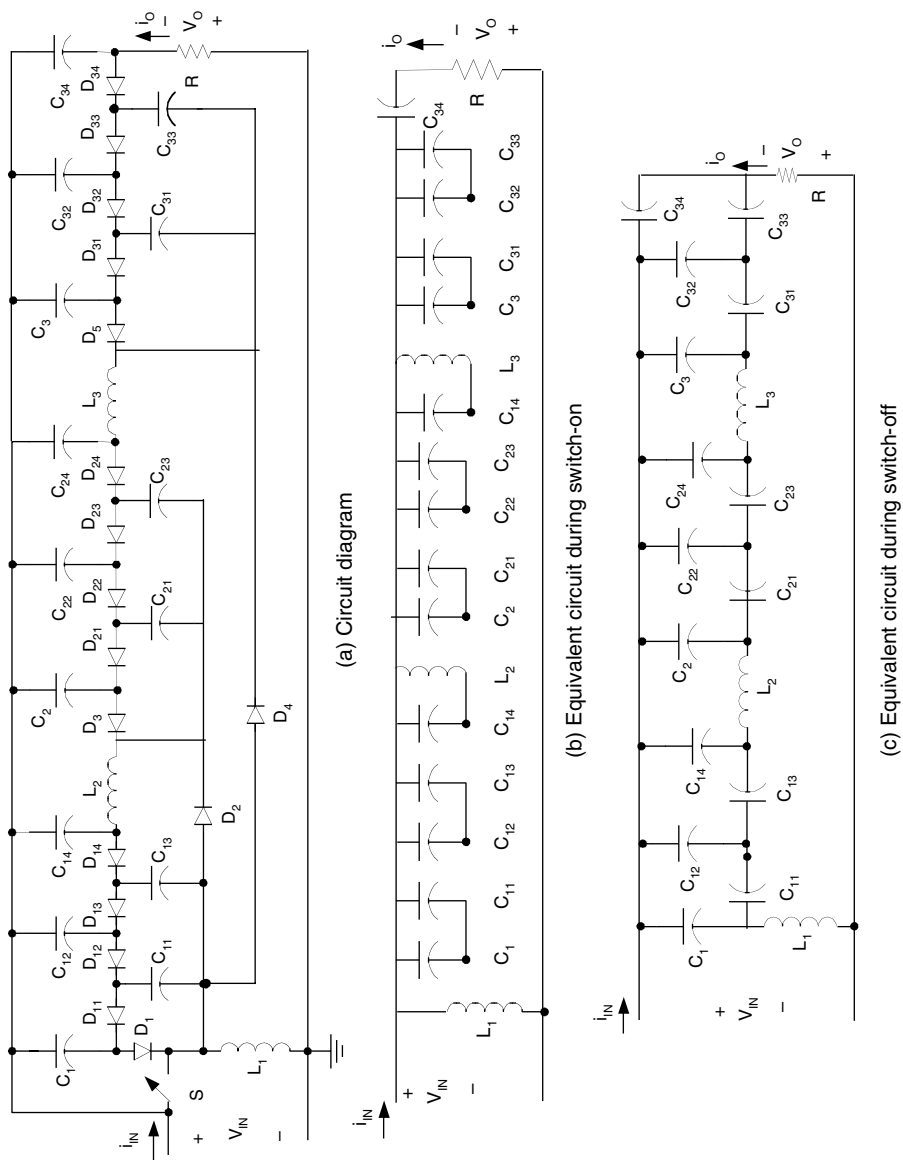


FIGURE 6.11
Three-stage triple boost circuit.

$$V_O = V_{C34} - V_{in} = \left[\left(\frac{3}{1-k} \right)^3 - 1 \right] V_{in} \quad (6.76)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{3}{1-k} \right)^3 - 1 \quad (6.77)$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT \quad I_{L1} = \frac{32}{(1-k)^3} I_O$$

$$\Delta i_{L2} = \frac{V_1}{L_2} kT \quad I_{L2} = \frac{8}{(1-k)^2} I_O$$

$$\Delta i_{L3} = \frac{V_2}{L_3} kT \quad I_{L3} = \frac{2}{1-k} I_O$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{k(1-k)^3 TV_{in}}{64 L_1 I_O} = \frac{k(1-k)^6}{12^3} \frac{R}{f L_1} \quad (6.78)$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{k(1-k)^2 TV_1}{16 L_2 I_O} = \frac{k(1-k)^4}{12^2} \frac{R}{f L_2} \quad (6.79)$$

and the variation ratio of current i_{L3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L3} / 2}{I_{L3}} = \frac{k(1-k) TV_2}{4 L_3 I_O} = \frac{k(1-k)^2}{12} \frac{R}{f L_3} \quad (6.80)$$

Usually ξ_1 , ξ_2 , and ξ_3 are small, this means that this converter works in the continuous mode. The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32}} = \frac{I_O(1-k)T}{C_{32}} = \frac{1-k}{f C_{32}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{32}} \quad (6.81)$$

6.5.4 N/O Higher Stage Triple Boost Circuit

The N/O higher stage triple boost circuit is derived from the corresponding circuit of the main series by adding DEC twice in each stage circuit. For n th stage additional circuit, the voltage across capacitor C_{n4} is

$$V_{Cn4} = \left(\frac{3}{1-k}\right)^n V_{in}$$

The output voltage is

$$V_o = V_{Cn4} - V_{in} = \left[\left(\frac{3}{1-k}\right)^n - 1\right] V_{in} \quad (6.82)$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^n - 1 \quad (6.83)$$

Analogously, the variation ratio of current i_{Li} through inductor L_i ($i = 1, 2, 3, \dots, n$) is

$$\xi_i = \frac{\Delta i_{Li} / 2}{I_{Li}} = \frac{k(1-k)^{2(n-i+1)}}{12^{(n-i+1)}} \frac{R}{fL_i} \quad (6.84)$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1-k}{2RfC_{n2}} \quad (6.85)$$

6.6 Multiple Series

All circuits of N/O cascade boost converters — multiple series — are derived from the corresponding circuits of the main series by adding DEC multiple

(j) times in each stage circuit. The first three stages of this series are shown in Figure 6.12 to Figure 6.14. For convenience they are called elementary multiple boost circuit, two-stage multiple boost circuit, and three-stage multiple boost circuit respectively, and numbered as $n = 1, 2$ and 3 .

6.6.1 N/O Elementary Multiple Boost Circuit

This N/O elementary multiple boost circuit is derived from elementary boost converter by adding a DEC multiple (j) times. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 6.12.

The output voltage of the first DEC (across capacitor C_{12j}) increases to

$$V_{C_{12j}} = \frac{j+1}{1-k} V_{in} \quad (6.86)$$

The final output voltage V_O is equal to

$$V_O = V_{C_{12j}} - V_{in} = \left[\frac{j+1}{1-k} - 1 \right] V_{in} \quad (6.87)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{j+1}{1-k} - 1 \quad (6.88)$$

6.6.2 N/O Two-Stage Multiple Boost Circuit

The N/O two-stage multiple boost circuit is derived from the two-stage boost circuit by adding DEC multiple (j) times in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 6.13.

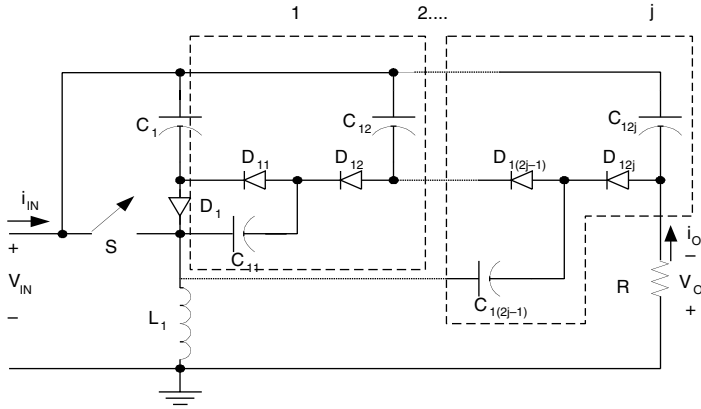
As described in the previous section the voltage across capacitor C_{12j} is

$$V_{C_{12j}} = \frac{j+1}{1-k} V_{in}$$

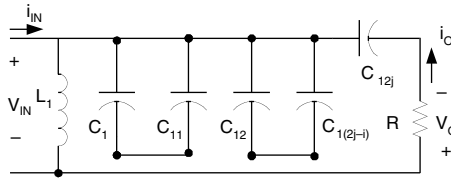
Analogously, the voltage across capacitor C_{22j} is.

$$V_{C_{22j}} = \left(\frac{j+1}{1-k} \right)^2 V_{in} \quad (6.89)$$

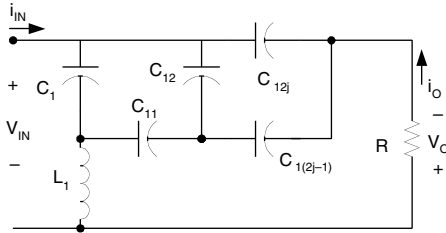
The final output voltage V_O is equal to



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

FIGURE 6.12

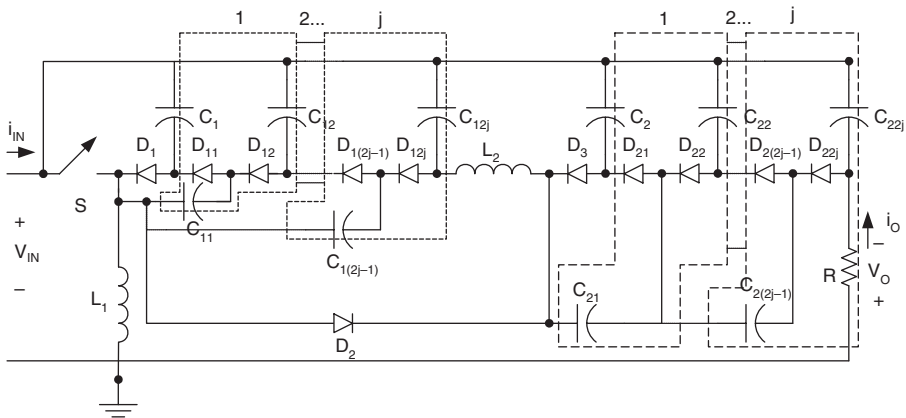
Elementary multiple boost circuit.

$$V_O = V_{C22j} - V_{in} = \left[\left(\frac{j+1}{1-k} \right)^2 - 1 \right] V_{in} \quad (6.90)$$

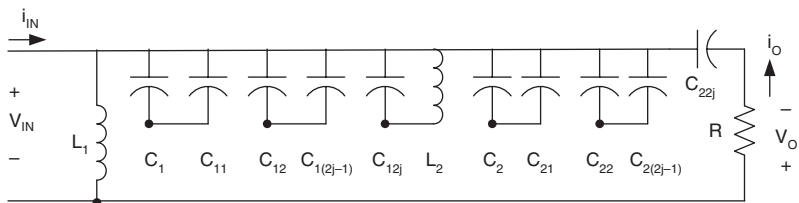
The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{j+1}{1-k} \right)^2 - 1 \quad (6.91)$$

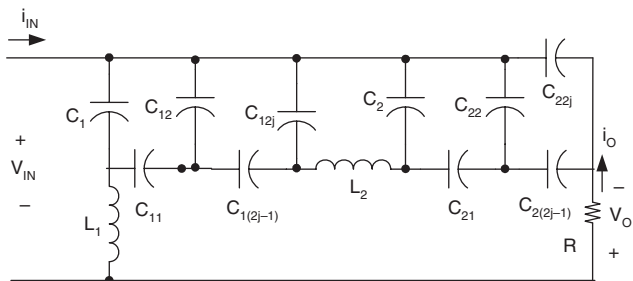
The ripple voltage of output voltage v_O is



(a) Circuit diagram



(b) Switch on



(c) Switch off

FIGURE 6.13

Two-stage multiple boost circuit.

$$\Delta v_O = \frac{\Delta Q}{C_{22j}} = \frac{I_O(1-k)T}{C_{22j}} = \frac{1-k}{fC_{22j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{22j}} \quad (6.92)$$

6.6.3 N/O Three-Stage Multiple Boost Circuit

This N/O circuit is derived from the three-stage boost circuit by adding DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 6.14](#).

As described in the previous section the voltage across capacitor C_{12j} is $V_{C12j} = (j+1/1-k)V_{in}$, and the voltage across capacitor C_{22j} is $V_{C22j} = (j+1/1-k)^2 V_{in}$. Analogously, the voltage across capacitor C_{32j} is

$$V_{C32j} = \left(\frac{j+1}{1-k}\right)^3 V_{in} \quad (6.93)$$

The final output voltage V_O is equal to

$$V_O = V_{C32j} - V_{in} = \left[\left(\frac{j+1}{1-k}\right)^3 - 1\right] V_{in} \quad (6.94)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{j+1}{1-k}\right)^3 - 1 \quad (6.95)$$

The ripple voltage of output voltage v_O is

$$\Delta v_O = \frac{\Delta Q}{C_{32j}} = \frac{I_O(1-k)T}{C_{32j}} = \frac{1-k}{fC_{32j}} \frac{V_O}{R}$$

Therefore, the variation ratio of output voltage v_O is

$$\varepsilon = \frac{\Delta v_O / 2}{V_O} = \frac{1-k}{2RfC_{32j}} \quad (6.96)$$

6.6.4 N/O Higher Stage Multiple Boost Circuit

The N/O higher stage multiple boost circuit is derived from the corresponding circuit of the main series by adding DEC multiple (j) times in each stage circuit. For n th stage multiple boost circuit, the voltage across capacitor C_{n2j} is

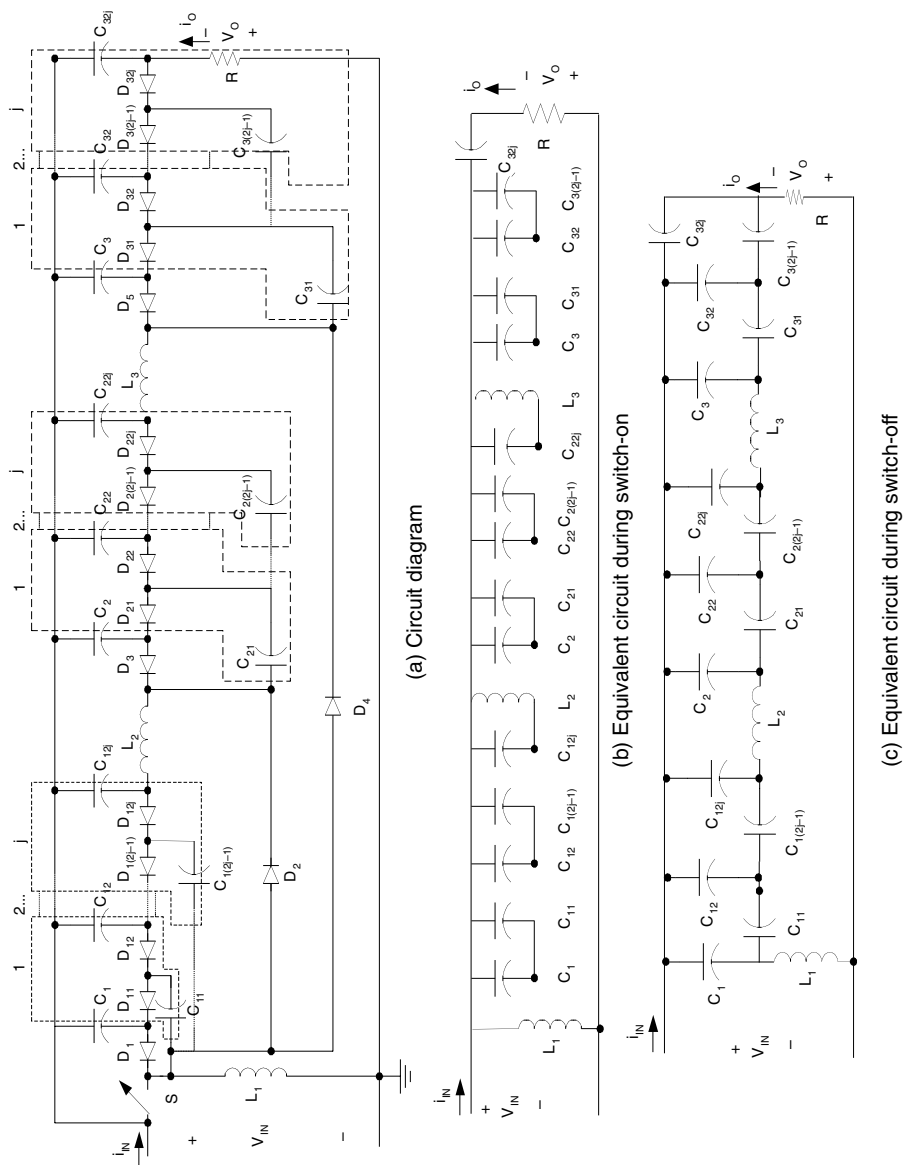


FIGURE 6.14
Three-stage multiple boost circuit.

$$V_{Cn2j} = \left(\frac{j+1}{1-k}\right)^n V_{in}$$

The output voltage is

$$V_O = V_{Cn2j} - V_{in} = \left[\left(\frac{j+1}{1-k}\right)^n - 1\right] V_{in} \quad (6.97)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{j+1}{1-k}\right)^n - 1 \quad (6.98)$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_O} = \frac{1-k}{2RfC_{n2j}} \quad (6.99)$$

6.7 Summary of Negative Output Cascade Boost Converters

All the circuits of the N/O cascade boost converters as a family can be shown in [Figure 6.15](#). From the analysis of the previous two sections we have the common formula to calculate the output voltage:

$$V_O = \begin{cases} \left[\left(\frac{1}{1-k}\right)^n - 1\right] V_{in} & \text{main_series} \\ \left[2 * \left(\frac{1}{1-k}\right)^n - 1\right] V_{in} & \text{additional_series} \\ \left[\left(\frac{2}{1-k}\right)^n - 1\right] V_{in} & \text{double_series} \\ \left[\left(\frac{3}{1-k}\right)^n - 1\right] V_{in} & \text{triple_series} \\ \left[\left(\frac{j+1}{1-k}\right)^n - 1\right] V_{in} & \text{multiple}(j)_series \end{cases} \quad (6.100)$$

The voltage transfer gain is

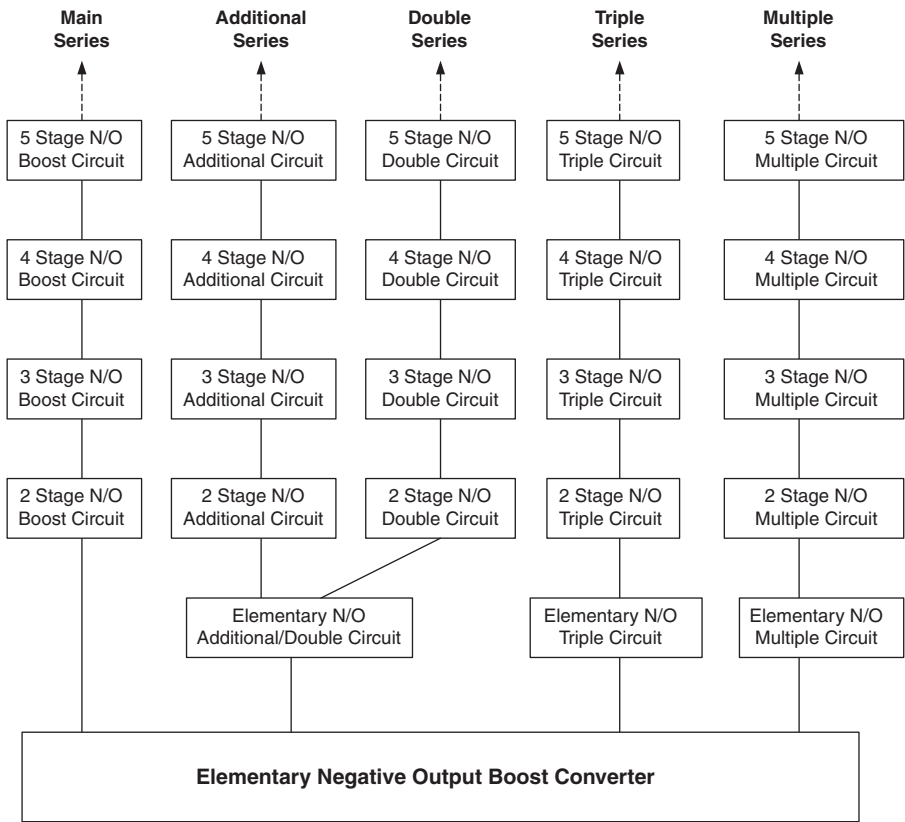


FIGURE 6.15
The family of negative output cascade boost converters.

$$G = \frac{V_o}{V_{in}} = \begin{cases} \left(\frac{1}{1-k}\right)^n - 1 & \text{main_series} \\ 2 * \left(\frac{1}{1-k}\right)^n - 1 & \text{additional_series} \\ \left(\frac{2}{1-k}\right)^n - 1 & \text{double_series} \\ \left(\frac{3}{1-k}\right)^n - 1 & \text{triple_series} \\ \left(\frac{j+1}{1-k}\right)^n - 1 & \text{multiple}(j)_series \end{cases} \quad (6.101)$$

In order to show the advantages of N/O cascade boost converters, we compare their voltage transfer gains to that of the buck converter,

$$G = \frac{V_o}{V_{in}} = k$$

forward converter,

$$G = \frac{V_O}{V_{in}} = kN \quad N \text{ is the transformer turn ratio}$$

Cúk-converter,

$$G = \frac{V_O}{V_{in}} = \frac{k}{1-k}$$

fly-back converter,

$$G = \frac{V_O}{V_{in}} = \frac{k}{1-k} N \quad N \text{ is the transformer turn ratio}$$

boost converter,

$$G = \frac{V_O}{V_{in}} = \frac{1}{1-k}$$

and negative output Luo-converters

$$G = \frac{V_O}{V_{in}} = \frac{n}{1-k} \quad (6.102)$$

If we assume that the conduction duty k is 0.2, the output voltage transfer gains are listed in [Table 6.1](#), if the conduction duty k is 0.5, the output voltage transfer gains are listed in [Table 6.2](#), if the conduction duty k is 0.8, the output voltage transfer gains are listed in [Table 6.3](#).

6.8 Simulation and Experimental Results

6.8.1 Simulation Results of a Three-Stage Boost Circuit

To verify the design and calculation results, PSpice simulation package was applied to a three-stage boost circuit. Choosing $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F and $R = 30$ k Ω , and using $k = 0.7$ and $f = 100$ kHz. The voltage values V_1 , V_2 , and V_O of a triple-lift circuit are 66 V, 194 V, and 659 V respectively, and inductor current waveforms i_{L1} (its average value $I_{L1} = 618$ mA), i_{L2} , and i_{L3} . The simulation results are shown in [Figure 6.16](#). The voltage values are matched to the calculated results.

TABLE 6.1Voltage Transfer Gains of Converters in the Condition $k = 0.2$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.2		
Forward converter		0.2N (N is the transformer turn ratio)				
Cúk-converter				0.25		
Fly-back converter		0.25N (N is the transformer turn ratio)				
Boost converter				1.25		
Negative output Luo-converters	1.25	2.5	3.75	5	6.25	$1.25n$
Negative output cascade boost converters — main series	0.25	0.563	0.953	1.441	2.052	1.25^{n-1}
Negative output cascade boost converters — additional series	1.5	2.125	2.906	3.882	5.104	$2 * 1.25^{n-1}$
Negative output cascade boost converters — double series	1.5	5.25	14.625	38.063	96.66	$(2 * 1.25)^{n-1}$
Negative output cascade boost converters — triple series	2.75	13.06	51.73	196.75	740.58	$(3 * 1.25)^{n-1}$
Negative output cascade boost converters — multiple series ($j=3$)	4	24	124	624	3124	$(4 * 1.25)^{n-1}$

TABLE 6.2Voltage Transfer Gains of Converters in the Condition $k = 0.5$

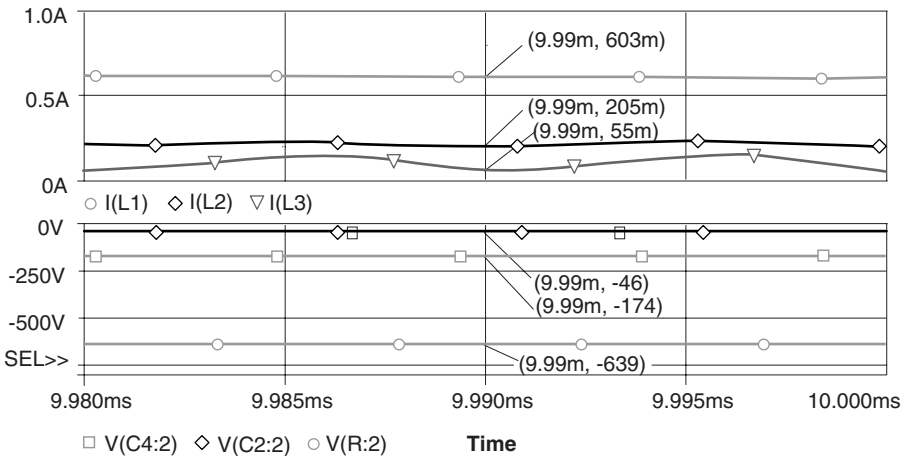
Stage No. (n)	1	2	3	4	5	n
Buck converter				0.5		
Forward converter		0.5N (N is the transformer turn ratio)				
Cúk-converter				1		
Fly-back converter		N (N is the transformer turn ratio)				
Boost converter				2		
Negative output Luo-converters		2	4	6	8	$2n$
Negative output cascade boost converters — main series		1	3	7	15	2^{n-1}
Negative output cascade boost converters — additional series		3	7	15	31	$2 * 2^{n-1}$
Negative output cascade boost converters — double series		3	15	63	255	$(2 * 2)^{n-1}$
Negative output cascade boost converters — triple series		5	35	215	1295	$(3 * 2)^{n-1}$
Negative output cascade boost converters — multiple series ($j=3$)		7	63	511	4095	$(4 * 2)^{n-1}$

6.8.2 Experimental Results of a Three-Stage Boost Circuit

A test rig was constructed to verify the design and calculation results, and compare with PSpice simulation results. The test conditions are still $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all C_1 to $C_8 = 2$ μ F and $R = 30$ k Ω , and using $k = 0.7$ and $f = 100$ kHz. The component of the switch is a MOSFET device IRF950

TABLE 6.3Voltage Transfer Gains of Converters in the Condition $k = 0.8$

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.8		
Forward converter		$0.8N$ (N is the transformer turn ratio)				
Cúk-converter				4		
Fly-back converter		$4N$ (N is the transformer turn ratio)				
Boost converter				5		
Negative output Luo-converters	5	10	15	20	25	$5n$
Negative output cascade boost converters — main series	4	24	124	624	3124	5^{n-1}
Negative output cascade boost converters — additional series	9	49	249	1249	6249	$2 \cdot 5^{n-1}$
Negative output cascade boost converters — double series	9	99	999	9999	99999	$(2 \cdot 5)^{n-1}$
Negative output cascade boost converters — triple series	14	224	3374	50624	759374	$(3 \cdot 5)^{n-1}$
Negative output cascade boost converters — multiple series ($j=3$)	19	399	7999	15999	32×10^5	$(4 \cdot 5)^{n-1}$

**FIGURE 6.16**

The simulation results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

with the rates 950 V/5 A/2 MHz. We measured the values of the output voltage and first inductor current in the following converters.

After careful measurement, the current value of $I_{L1} = 0.62$ A (shown in channel 1 with 1 A/Div) and voltage value of $V_O = 660$ V (shown in Channel 2 with 200 V/Div) are obtained. The experimental results (current and voltage values) in Figure 6.17 match the calculated and simulation results, which are $I_{L1} = 0.618$ A and $V_O = 659$ V shown in Figure 6.16.

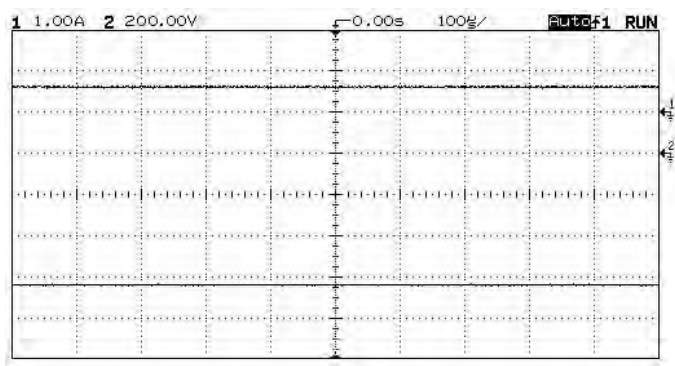


FIGURE 6.17
 The experimental results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

TABLE 6.4
 Comparison of Simulation and Experimental Results of a Triple-Lift Circuit.

Stage No. (n)	I_{L1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_o (V)	P_o (W)	η (%)
Simulation results	0.618	0.927	20	18.54	659	14.47	78
Experimental results	0.62	0.93	20	18.6	660	14.52	78

6.8.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully, and efficiently. Particularly, the efficiencies of the tested circuits is 78%, which is good for high output voltage equipment. To compare the simulation and experimental results, see Table 6.4. All results are well identified with each other.

6.8.4 Transient Process

Usually, there is high inrush current during the first power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick taking only a few milliseconds. It is difficult to demonstrate it in this section.

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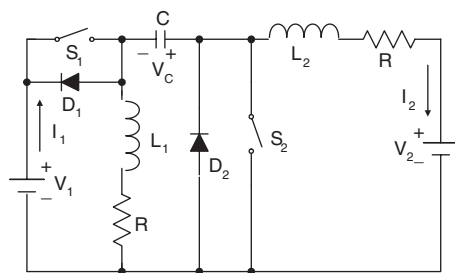
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Multiple Quadrant Operating Luo-Converters

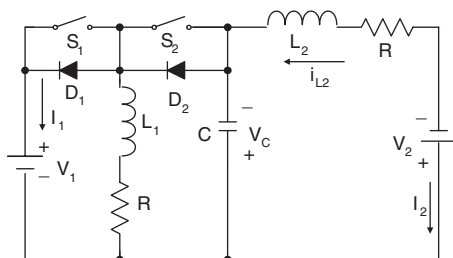
Classical DC-DC converters usually perform in single quadrant operation, such as buck converter, and Luo-converters. Multiple-quadrant operation is required in industrial applications, e.g., a DC motor running forward and reverse in motoring and regenerative braking states. This chapter introduces three new converters that can perform two- and four-quadrant DC/DC conversion. One particular application is the MIT $42/\pm 14$ V DC/DC converter used for new car power supply systems. Because this converter implements dual-direction energy transference, it is a second-generation DC/DC converter. Simulation and experimental results have verified its characteristics.

7.1 Introduction

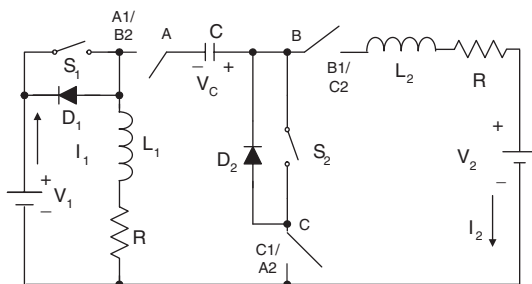
Multiple-quadrant operation converters can be derived from the multiple-quadrant chopper. Correspondingly, class B converters can be derived from type B choppers (two-quadrant operation), class E converters from type E choppers (four-quadrant operation) and so on. Also, multiple-quadrant operating converters can be derived from other first generation converters. This paper introduces two- and four-quadrant operation Luo-converters, which are derived from positive, negative and double output Luo-converters. They correspond to a DC motor drive in forward and reverse running with motoring and regenerative braking states. These converters are shown in [Figure 7.1](#). The input source and output load are usually certain voltages as shown V_1 and V_2 . Switches S_1 and S_2 in this diagram are power MOSFET devices, and driven by a pulse-width-modulated (PWM) switching signal with repeating frequency f and conduction duty k . In this paper the switch repeating period is $T = 1/f$, the switch-on period is kT and switch-off period is $(1 - k)T$. The equivalent resistance is R for each inductor. During switch-on the voltage drop across the switches and diodes are V_s and V_D . When the switch is turned off, the free-wheeling diode current descends in whole switch-off period $(1 - k)T$. If the diode current does not become zero before



(a) Circuit 1



(b) Circuit 2



(c) Circuit 3

FIGURE 7.1

Multiple-quadrant operating Luo-converters.

the switch is turned on again, we define this working state to be the continuous region. If the current becomes zero before the switch is turned on again, this working state is the discontinuous conduction region.

In this chapter, variation ratio of current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}}$$

Variation ratio of current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}}$$

Variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D / 2}{I_D}$$

Variation ratio of voltage v_C is

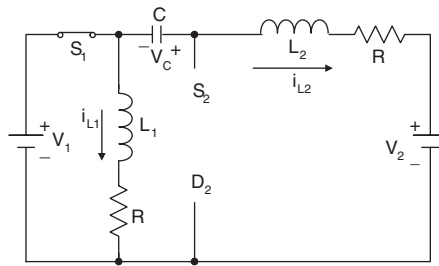
$$\rho = \frac{\Delta v_C / 2}{V_C}$$

7.2 Circuit Explanation

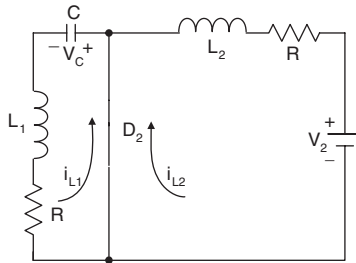
Each converter shown in [Figure 7.1](#) consists of two switches with two passive diodes, two inductors and one capacitor. Circuit 1 performs a two-quadrant (forward) operation, and circuit 2 performs a two-quadrant (reverse) operation. Circuit 1 and circuit 2 can be converted to each other by a three-pole (A, B, and C) double-through (A1/A2, B1/B2, and C1/C2) auxiliary changeover switch as circuit 3. Circuit 3 performs a four-quadrant operation. Since the change-over process between forward and reverse operations is not very frequent, so that the auxiliary change-over switch can be isolated-gate bipolar transistor (IGBT), power relay and contactor. The source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back electromotive force (EMF). For example, when the source voltage is 42 V and load voltage is ± 14 V there are four modes of operation:

1. Mode A (Quadrant I): electrical energy is transferred from source side V_1 to load side V_2
2. Mode B (Quadrant II): electrical energy is transferred from load side V_2 to source side V_1
3. Mode C (Quadrant III): electrical energy is transferred from source side V_1 to load side $-V_2$
4. Mode D (Quadrant IV): electrical energy is transferred from load side $-V_2$ to source side V_1

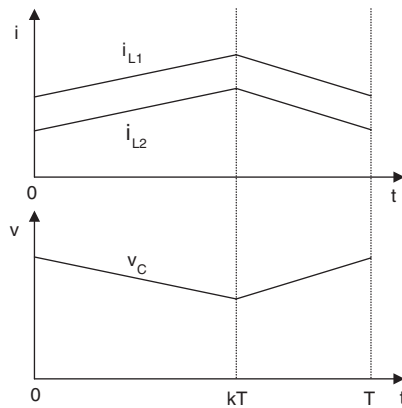
Each mode has two states: *on* and *off*. Circuit 1 in [Figure 7.1a](#) implements Modes A and B, and Circuit 2 in [Figure 7.1b](#) implements Modes C and D.



(a) Switch on



(b) Switch off



(c) Waveforms with enlarged variations

FIGURE 7.2

Mode A.

7.2.1 Mode A

Mode A implements the characteristics of the buck-boost conversion. For mode A, state-on is shown in Figure 7.2a: switch S_1 is closed, switch S_2 and diodes D_1 and D_2 are not conducted. In this case inductor currents i_{L1} and i_{L2} increase, and $i_1 = i_{L1} + i_{L2}$. State-off is shown in Figure 7.2b: switches S_1 , S_2 , and diode D_1 are off and diode D_2 is conducted. In this case current i_{L1}

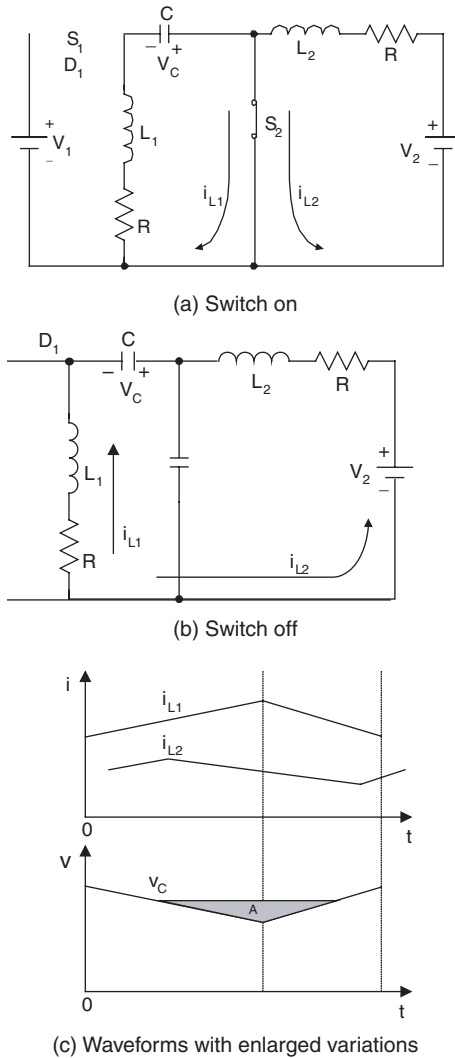


FIGURE 7.3
Mode B.

flows via diode D_2 to charge capacitor C , in the meantime current i_{L2} is kept to flow through load battery V_2 . The free-wheeling diode current $i_{D2} = i_{L1} + i_{L2}$. Some currents' and voltages' waveforms are shown in [Figure 7.2c](#).

7.2.2 Mode B

Mode B implements the characteristics of the boost conversion. For mode B, state-on is shown in Figure 7.3a: switch S_2 is closed, switch S_1 and diodes D_1 and D_2 are not conducted. In this case inductor current i_{L2} increases by biased

V_2 , inductor current i_{L1} increases by biased V_C . Therefore capacitor voltage V_C reduces. State-off is shown in [Figure 7.3b](#): switches S_1 , S_2 and diode D_2 are not on, and only diode D_1 is on. In this case source current $i_1 = i_{L1} + i_{L2}$ which is a negative value to perform the regenerative operation. Inductor current i_{L2} flows through capacitor C , it is charged by current i_{L2} . After capacitor C , i_{L2} then flows through the source V_1 . Inductor current i_{L1} flows through the source V_1 via diode D_1 . Some currents' and voltages' waveforms are shown in [Figure 7.3c](#).

7.2.3 Mode C

Mode C implements the characteristics of the buck-boost conversion. For mode C, state-on is shown in [Figure 7.4a](#): switch S_1 is closed, switch S_2 and diodes D_1 and D_2 are not conducted. In this case inductor currents i_{L1} and i_{L2} increase, and $i_1 = i_{L1}$. State-off is shown in [Figure 7.4b](#): switches S_1 , S_2 , and diode D_1 are off and diode D_2 is conducted. In this case current i_{L1} flows via diode D_2 to charge capacitor C and the load battery V_2 via inductor L_2 . The free-wheeling diode current $i_{D2} = i_{L1} = i_C + i_2$. Some waveforms are shown in [Figure 7.4c](#).

7.2.4 Mode D

Mode D implements the characteristics of the boost conversion. For mode D, state-on is shown in [Figure 7.5a](#): switch S_2 is closed, switch S_1 and diodes D_1 and D_2 are not conducted. In this case inductor current i_{L1} increases by biased V_2 , inductor current i_{L2} decreases by biased $(V_2 - V_C)$. Therefore capacitor voltage V_C reduces. Current $i_{L1} = i_{C-on} + i_2$. State-off is shown in [Figure 7.5b](#): switches S_1 , S_2 , and diode D_2 are not on, and only diode D_1 is on. In this case source current $i_1 = i_{L1}$ which is a negative value to perform the regenerative operation. Inductor current i_2 flows through capacitor C that is charged by current i_2 , i.e., $i_{C-off} = i_2$. Some currents and voltages waveforms are shown in [Figure 7.5c](#).

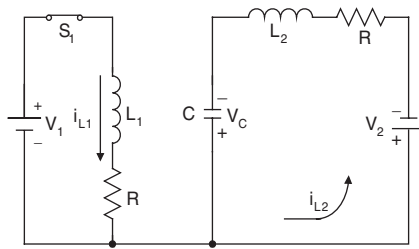
7.2.5 Summary

The switch status of all modes is listed in [Table 7.1](#). From the table it can be seen that only one switch works in one mode, so that this converter is very simple and effective.

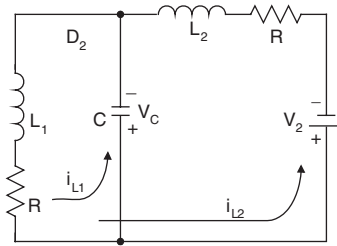
7.3 Mode A (Quadrant I Operation)

As shown in [Figure 7.2a](#) and b the voltage across capacitor C increases during switch-on, and decreases during switch off. Capacitor C acts as the primary

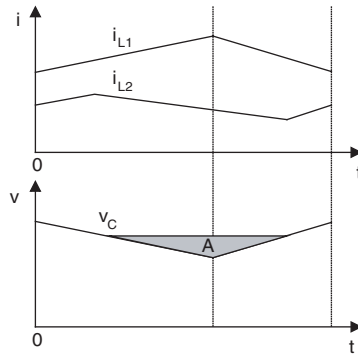
© 2003 by CRC Press LLC



(a) Switch on



(b) Switch off



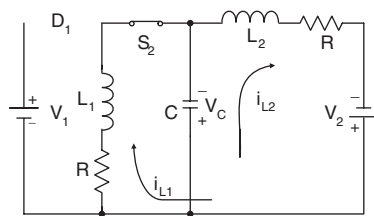
(c) Waveforms with enlarged variations

FIGURE 7.4
Mode C.

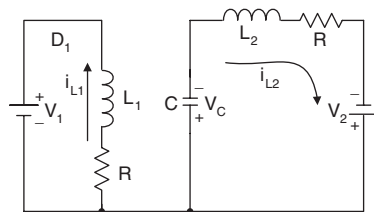
means of storing and transferring energy from the input source to the output load via the pump inductor L_1 . Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, i.e., $v_C(t) \approx V_C$, even though it stores and transfers energy from the input to the output.

7.3.1 Circuit Description

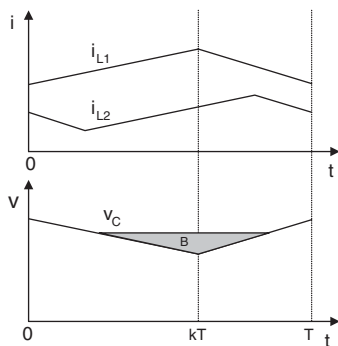
When switch S_1 is on, the source current $i_1 = i_{L1} + i_{L2}$. Inductor L_1 absorbs energy from the source. In the mean time inductor L_2 absorbs energy from



(a) Switch on



(b) Switch off



(c) Waveforms with enlarged variations

FIGURE 7.5
Mode D.

TABLE 7.1

Switch Status

Switch or Diode	Mode A (QI)		Mode B (QII)		Mode C (QIII)		Mode D (QIV)	
	State-on	State-off	State-on	State-off	State-on	State-off	State-on	State-off
Circuit	Circuit 1				Circuit 2			
S_1	ON				ON			
D_1				ON				ON
S_2			ON				ON	
D_2		ON				ON		

Note: The blank status means OFF.

source and capacitor C , both currents i_{L1} and i_{L2} increase. When switch S_1 is off, source current $i_1 = 0$. Current i_{L1} flows through the free-wheeling diode D_2 to charge capacitor C . Inductor L_1 transfers its stored energy to capacitor C . In the mean time current i_{L2} flows through the load V_2 and free-wheeling diode D_2 to keep itself continuous. Both currents i_{L1} and i_{L2} decrease. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in [Figure 7.2c](#). The equivalent circuits in switch-on and -off states are shown in Figure 2a and b.

Actually, the variations of currents i_{L1} and i_{L2} are small so that

$$i_{L1} \approx I_{L1} \quad \text{and} \quad i_{L2} \approx I_{L2}$$

The charge on capacitor C increases during switch off and on:

$$Q_+ = (1 - k)T I_{L1}$$

$$Q_- = kT I_{L2}$$

In a whole period investigation, $Q_+ = Q_-$.

Thus,

$$I_{L2} = \frac{1-k}{k} I_{L1} \quad (7.1)$$

Since capacitor C performs as a low-pass filter, the output current

$$I_{L2} = I_2$$

The source current $i_1 = i_{L1} + i_{L2}$ during switch-on, and $i_1 = 0$ during switch-off. Average source current I_1 is

$$I_1 = k \times i_1 = k(i_{L1} + i_{L2}) = k\left(1 + \frac{1-k}{k}\right)I_{L1} = I_{L1}$$

Hence, the output current is

$$I_2 = \frac{1-k}{k} I_1 \quad (7.2)$$

The input and output powers are

$$P_I = V_1 I_1 \quad \text{and} \quad P_O = V_2 I_2$$

The power losses are

- $V_S I_1$ — Switch power loss
- $R I_{L1}^2$ — Power loss across inductor L_1
- $V_D I_1$ — Diode power loss
- $R I_{L2}^2$ — Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R(I_1^2 + I_2^2) \quad (7.3)$$

Since

$$P_I = P_O + P_{loss}$$

hence

$$V_1 I_1 = V_2 I_2 + (V_S + V_D) I_1 + R(I_1^2 + I_2^2) \quad (7.4)$$

or

$$V_1 = V_2 \frac{1-k}{k} + (V_S + V_D) + R I_2 \left(\frac{k}{1-k} + \frac{1-k}{k} \right) \quad (7.5)$$

The output current is

$$I_2 = \frac{V_1 - V_S - V_D - V_2 \frac{1-k}{k}}{R \left(\frac{k}{1-k} + \frac{1-k}{k} \right)} \quad (7.6)$$

The minimum conduction duty k corresponding to $I_2 = 0$ is

$$k_{min} = \frac{V_2}{V_1 + V_2 - V_S - V_D} \quad (7.7)$$

The power transfer efficiency is

$$\eta_A = \frac{P_O}{P_I} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + \frac{V_S + V_D}{V_2} \frac{k}{1-k} + \frac{R I_2}{V_2} \left[1 + \left(\frac{1-k}{k} \right)^2 \right]} \quad (7.8)$$

7.3.2 Variations of Currents and Voltages

Because the voltage across the inductor L_1 is $(V_1 - RI_1)$ during switch-on and $(V_C + RI_1)$ during switch-off, the average voltage across capacitor C is

$$kT(V_1 - RI_1) = (V_C + RI_1)(1 - k)T$$

Hence

$$V_C = \frac{k}{1 - k} V_1 - \frac{1}{1 - k} RI_1 = \frac{k}{1 - k} V_1 - RI_2 \frac{k}{(1 - k)^2} = \frac{k}{1 - k} (V_1 - \frac{RI_2}{1 - k}) \quad (7.9)$$

The peak-to-peak variation of capacitor voltage v_c is

$$\Delta v_c = \frac{Q_-}{C} = \frac{kTI_2}{C} = \frac{kI_2}{fC}$$

The variation ratio of capacitor voltage v_c is

$$\rho = \frac{\Delta v_c / 2}{V_C} = \frac{(1 - k)I_2}{2fC(V_1 - RI_2 \frac{1}{1 - k})} \quad (7.10)$$

The peak-to-peak variation of inductor current i_{L1} is

$$\Delta i_{L1} = \frac{V_1 - V_s - RI_1}{L_1} kT$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = k \frac{V_1 - V_s - RI_1}{2fL_1 I_1} \quad (7.11)$$

The peak-to-peak variation of inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_1 - V_s - V_2 + V_C - RI_2}{L_2} kT = \frac{V_1 - V_s - RI_1}{L_2} kT$$

The variation ratio of inductor current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = k \frac{V_1 - V_s - RI_1}{2fL_2 I_2} \quad (7.12)$$

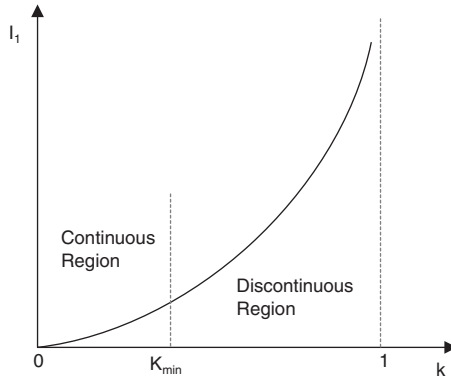


FIGURE 7.6

Boundary between continuous and discontinuous regions of Mode A.

The free-wheeling diode's current i_{D2} during switch off is: $i_{D2} = i_{L1} + i_{L2}$. Its peak-to-peak variation is

$$\Delta i_{D2} = \Delta i_{L1} + \Delta i_{L2} = \frac{V_1 - V_s - RI_1}{L} kT$$

where

$$L = L_1 L_2 / (L_1 + L_2).$$

The variation ratio of the diode current i_{D2} is

$$\zeta_{D2} = \frac{\Delta i_{D2} / 2}{I_{L1} + I_{L2}} = k \frac{V_1 - V_s - RI_1}{2fL(I_1 + I_2)} = k^2 \frac{V_1 - V_s - RI_1}{2fLI_1} \quad (7.13)$$

7.3.3 Discontinuous Region

If the diode current becomes zero before S_1 switch is on again, the converter works in discontinuous region. The condition $i_D \zeta_{D2} = 1$, i.e.,

$$k^2 = \frac{2fLI_1}{V_1 - V_s - RI_1} \quad (7.14)$$

From Equations (7.7) and (7.14) the boundary between continuous and discontinuous regions is shown in [Figure 7.6](#). Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

7.4 Mode B (Quadrant II Operation)

As shown in Figure 7.3a and b the voltage across capacitor C decreases during switch-on, and increases during switch off. Capacitor C acts as the primary means of storing and transferring energy from the load battery to the source via inductor L_2 . Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, i.e., $v_C(t) \approx V_C$, even though it stores and transfers energy from the load V_2 to the source V_1 .

7.4.1 Circuit Description

When switch S_2 is off, source current $i_1 = 0$. Current i_{L1} flows through the switch S_2 and capacitor C , and increases. Current i_{L1} flows through the switch S_2 , and increases. When switch S_2 is off, the source current $i_1 = i_{L1} + i_{L2}$. The free-wheeling diode D_1 is conducted. Both currents i_{L1} and i_{L2} decrease. Inductor L_1 transfers its stored energy to capacitor C . In the mean time current i_{L2} flows through the source V_1 . In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 7.3c. The equivalent circuits in switch-on and -off states are shown in Figures 7.3a and b.

Actually, the variations of currents i_{L1} and i_{L2} are small so that

$$i_{L1} \approx I_{L1} \quad \text{and} \quad i_{L2} \approx I_{L2}$$

The charge on capacitor C increases during switch off and on:

$$Q+ = (1 - k)T I_{L2}$$

$$Q- = kT I_{L1}$$

In a whole period investigation, $Q+ = Q-$.

Thus,

$$I_{L1} = \frac{1-k}{k} I_{L2} \quad (7.15)$$

Since capacitor C performs as a low-pass filter, the output current

$$I_{L2} = I_2$$

The source current $i_1 = i_{L1} + i_{L2}$ during switch-on, and $i_1 = 0$ during switch-off. Average source current I_1 is

$$I_1 = (1-k)i_1 = (1-k)(i_{L1} + i_{L2}) = (1-k)\left(1 + \frac{1}{1-k}\right)I_{L1} = I_{L1}$$

Hence, the output current is

$$I_1 = \frac{1-k}{k} I_2 \quad (7.16)$$

The input and output powers are

$$P_I = V_2 I_2 \quad \text{and} \quad P_O = V_1 I_1$$

The power losses are

- $V_S I_1$ — Switch power loss
- $R I_{L1}^2$ — Power loss across inductor L_1
- $V_D I_1$ — Diode power loss
- $R I_{L2}^2$ — Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R(I_1^2 + I_2^2) \quad (7.17)$$

Since

$$P_I = P_O + P_{loss}$$

hence

$$V_2 I_2 = V_1 I_1 + (V_S + V_D) I_1 + R(I_1^2 + I_2^2) \quad (7.18)$$

or

$$V_2 = \frac{1-k}{k} (V_1 + V_S + V_D) + R I_1 \left(\frac{k}{1-k} + \frac{1-k}{k} \right) \quad (7.19)$$

The output current is

$$I_1 = \frac{V_2 - (V_1 + V_S + V_D) \frac{1-k}{k}}{R \left(\frac{k}{1-k} + \frac{1-k}{k} \right)} \quad (7.20)$$

The minimum conduction duty k corresponding to $I_1 = 0$ is

$$k_{\min} = \frac{V_1 + V_s + V_D}{V_1 + V_2 + V_s + V_D} \quad (7.21)$$

The power transfer efficiency is

$$\eta_B = \frac{P_O}{P_I} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + \frac{V_s + V_D}{V_1} + \frac{R I_1}{V_1} [1 + (\frac{1-k}{k})^2]} \quad (7.22)$$

7.4.2 Variations of Currents and Voltages

Because the voltage across the inductor L_2 is $(V_2 - R I_2)$ during switch-on and $(V_1 - V_2 + V_C + R I_2)$ during switch-off, the average voltage across capacitor C is

$$kT(V_2 - R I_2) = (V_1 - V_2 + V_C + R I_2)(1-k)T$$

Hence

$$V_C = \frac{V_2}{1-k} - V_1 - \frac{1}{1-k} R I_2 = \frac{V_2}{1-k} - V_1 - R I_1 \frac{k}{(1-k)^2} \quad (7.23)$$

The peak-to-peak variation of capacitor voltage v_c is

$$\Delta v_C = \frac{Q_-}{C} = \frac{k T I_1}{C} = \frac{k I_1}{f C}$$

The variation ratio of capacitor voltage v_c is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{k I_1}{2 f C [\frac{V_2}{1-k} - V_1 - R I_1 \frac{k}{(1-k)^2}]} \quad (7.24)$$

The peak-to-peak variation of current i_{L1} is

$$\Delta i_{L1} = \frac{V_C - V_s - R I_1}{L_1} k T = \frac{V_2 - V_s - R I_2}{L_1} k T$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = k \frac{V_2 - V_s - RI_2}{2fL_1I_1} \quad (7.25)$$

The peak-to-peak variation of inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_2 - V_s - RI_2}{L_2} kT$$

The variation ratio of inductor current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = k \frac{V_2 - V_s - RI_2}{2fL_2I_2} \quad (7.26)$$

The free-wheeling diode's current i_{D1} during switch off is: $i_{D1} = i_{L1} + i_{L2}$. Its peak-to-peak variation is

$$\Delta i_{D2} = \Delta i_{L1} + \Delta i_{L2} = \frac{V_2 - V_s - RI_2}{L} kT$$

where $L = L_1L_2 / (L_1 + L_2)$. The variation ratio of diode current i_{D1} is

$$\zeta_{D1} = \frac{\Delta i_{D2} / 2}{I_{L1} + I_{L2}} = k \frac{V_2 - V_s - RI_2}{2fL(I_1 + I_2)} = k^2 \frac{V_2 - V_s - RI_2}{2fLI_2} \quad (7.27)$$

7.4.3 Discontinuous Region

If the diode current becomes zero before S_2 is switched on again, the converter works in discontinuous region. The condition is: $\zeta_{D1} = 1$, i.e.,

$$k^2 = \frac{2fLI_2}{V_2 - V_s - RI_2} \quad (7.28)$$

From Equations (7.21) and (7.28) the boundary between continuous and discontinuous regions is shown in [Figure 7.7](#). Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

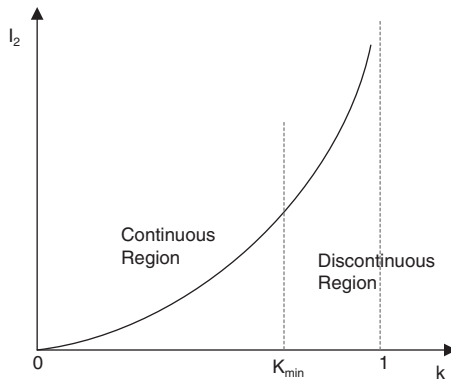


FIGURE 7.7

Boundary between continuous and discontinuous regions of Mode B.

7.5 Mode C (Quadrant III Operation)

As shown in Figure 7.4a and b the voltage across capacitor C increases during switch-off, and decreases during switch on. Capacitor C acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductor L_1 . Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, i.e., $v_C(t) \approx V_C$, even though it stores and transfers energy from the input to the output.

7.5.1 Circuit Description

The equivalent circuits in switch-on and -off states are shown in Figure 7.4a and b. When switch S_1 is on, the source current $i_1 = i_{L1}$. Inductor L_1 absorbs energy from the source. In the mean time inductor L_2 absorbs energy from capacitor C , current i_{L1} increases and i_2 decreases. When switch S_1 is off, source current $i_1 = 0$. Current i_{L1} flows through the free-wheeling diode D_2 to charge capacitor C and increase current i_2 . Inductor L_1 transfers its stored energy to capacitor C and the load V_2 . Current i_{L1} decreases and i_2 increases. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 7.4c.

Actually, the variations of currents i_{L1} and i_{L2} are small so that $i_{L1} \approx I_{L1}$ and $i_{L2} \approx I_{L2} = I_2$.

Since the capacitor current i_{C-on} is equal to I_2 during switch-on, i_{C-off} should be:

$$i_{C-off} = \frac{k}{1-k} I_2 \quad (7.29)$$

Inductor current i_{L1} during switch-off is

$$i_{L1} = I_2 + i_{C-off} = (1 + \frac{k}{1-k})I_2 = \frac{1}{1-k}I_2 \quad (7.30)$$

The source average current I_1 is

$$I_1 = ki_{L1} = \frac{k}{1-k}I_2 \quad \text{or} \quad I_{L1} = \frac{1}{k}I_1 \quad (7.31)$$

The input and output powers are

$$P_I = V_1 I_1$$

and

$$P_O = V_2 I_2$$

The power losses are

- $V_S I_1$ — Switch power loss
- $R I_{L1}^2$ — Power loss across inductor L_1
- $V_D I_1$ — Diode power loss
- $R I_{L2}^2$ — Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R[(\frac{I_1}{k})^2 + I_2^2] \quad (7.32)$$

Since

$$P_I = P_O + P_{loss}$$

hence

$$V_1 I_1 = V_2 I_2 + (V_S + V_D) I_1 + R[(\frac{I_1}{k})^2 + I_2^2] \quad (7.33)$$

or

$$V_1 = V_2 \frac{1-k}{k} + (V_S + V_D) + R I_2 [\frac{1}{k(1-k)} + \frac{1-k}{k}] \quad (7.34)$$

The output current is

$$I_2 = \frac{V_1 - V_S - V_D - V_2 \frac{1-k}{k}}{R[\frac{1}{k(1-k)} + \frac{1-k}{k}]} \quad (7.35)$$

The minimum conduction duty k corresponding to $I_2 = 0$ is

$$k_{\min} = \frac{V_2}{V_1 + V_2 - V_S - V_D} \quad (7.36)$$

The power transfer efficiency is

$$\eta_c = \frac{P_O}{P_I} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + \frac{V_S + V_D}{V_2} \frac{k}{1-k} + \frac{R I_2}{V_2} [1 + (\frac{1}{1-k})^2]} \quad (7.37)$$

7.5.2 Variations of Currents and Voltages

Because the voltage across the inductor L_1 is $(V_1 - R I_{L1})$ during switch-on and $(V_C + R I_{L1})$ during switch-off, the average voltage across capacitor C is

$$kT(V_1 - R I_{L1}) = (V_C + R I_{L1})(1-k)T$$

Hence

$$V_C = \frac{k}{1-k} V_1 - \frac{1}{1-k} R I_{L1} = \frac{k}{1-k} V_1 - R I_2 \frac{1}{(1-k)^2} \quad (7.38)$$

The peak-to-peak variation of capacitor voltage v_c is

$$\Delta v_c = \frac{k T I_2}{C} = \frac{k I_2}{f C}$$

The variation ratio of capacitor voltage v_c is

$$\rho = \frac{\Delta v_c / 2}{V_C} = \frac{k I_2}{2 f C [\frac{k}{1-k} V_1 - \frac{R I_2}{(1-k)^2}]} \quad (7.39)$$

The peak-to-peak variation of inductor current i_{L1} is

$$\Delta i_{L1} = \frac{V_1 - V_s - RI_1}{L_1} kT$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = k \frac{V_1 - V_s - RI_1}{2fL_1 I_1} \quad (7.40)$$

Diode's current i_{D2} during switch-off is: $i_{D2} = i_{L1}$. Its peak-to-peak variation is

$$\Delta i_{D2} = \Delta i_{L1} = \frac{V_1 - V_s - RI_1}{L_1} kT$$

and the variation ratio of inductor current i_{D2} is

$$\zeta_{D2} = \xi_1 = \frac{\Delta i_{D2} / 2}{I_{L1}} = k \frac{V_1 - V_s - RI_1}{2fL_1 I_1} \quad (7.40a)$$

Since voltage v_C varies very little, the peak-to-peak variation of inductor current i_{L2} is calculated by the area **A** of a triangle with width $T/2$ and height $\Delta v_C/2$:

$$\Delta i_{L2} = \frac{A}{L_2} = \frac{1}{2} \frac{T}{2} \frac{kTI_2}{2CL_2} = \frac{k}{8f^2 CL_2} I_2$$

The variation ratio of inductor current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_2} = \frac{k}{16f^2 CL_2} \quad (7.41)$$

7.5.3 Discontinuous Region

If the diode current becomes zero before S_1 is switched on again, the converter works in discontinuous region. The condition is $\zeta_{D2} = 1$, i.e.,

$$k = \frac{2fL_1 I_1}{V_1 - V_s - RI_1} \quad (7.42)$$

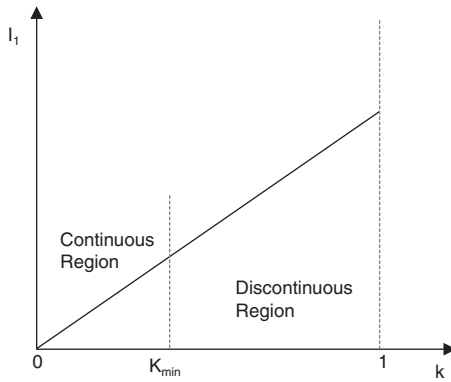


FIGURE 7.8

Boundary between continuous and discontinuous regions of Mode C.

From Equations (7.36) and (7.42) the boundary between continuous and discontinuous regions is shown in Figure 7.8. Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

7.6 Mode D (Quadrant IV Operation)

As shown in Figure 7.5a and b the voltage across capacitor C decreases during switch-on, and increases during switch off. Capacitor C acts as the primary means of storing and transferring energy from the load battery to the source via inductor L_1 . Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, i.e., $v_C(t) \approx V_C$, even though it stores and transfers energy from the load V_2 to the source V_1 .

7.6.1 Circuit Description

When switch S_2 is on, source current $i_1 = 0$. Current i_{L1} flows through the switch S_2 , then capacitor C and load battery V_2 . It increases and $i_{L1} = i_{C-on} + i_2$, when switch S_2 is off. The source current is $i_1 = i_{L1}$. The free-wheeling diode D_1 is conducted. Current i_{L1} decreases. Inductor L_1 transfers its stored energy to source V_1 . In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 7.5c. The equivalent circuits in switch-on and -off states are shown in Figure 7.5a and b.

Actually, the variations of currents i_{L1} and i_{L2} are small so that $i_{L1} \approx I_{L1}$ and $i_{L2} \approx I_2$.

Since the capacitor current i_{C-off} is equal to I_2 during switch-off, i_{C-on} should be:

$$i_{C-on} = \frac{1-k}{k} I_2 \quad (7.43)$$

Inductor current i_{L1} during switch-on is

$$i_{L1} = I_2 + i_{C-on} = (1 + \frac{1-k}{k}) I_2 = \frac{1}{k} I_2 \quad (7.44)$$

The source average current I_1 is

$$I_1 = (1-k)i_{L1} = \frac{1-k}{k} I_2$$

or

$$I_{L1} = \frac{1}{1-k} I_1 \quad (7.45)$$

The input and output powers are

$$P_I = V_2 I_2$$

and

$$P_O = V_1 I_1$$

The power losses are

$V_S I_1$ — Switch power loss

$R I_{L1}^2$ — Power loss across inductor L_1

$V_D I_1$ — Diode power loss

$R I_{L2}^2$ — Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R(I_{L1}^2 + I_2^2) \quad (7.46)$$

Since

$$P_I = P_O + P_{loss}$$

hence

$$V_2 I_2 = V_1 I_1 + (V_S + V_D) I_1 + R(I_{L1}^2 + I_2^2) \quad (7.47)$$

or

$$V_2 = \frac{1-k}{k}(V_1 + V_S + V_D) + RI_1 \left[\frac{1}{k(1-k)} + \frac{k}{1-k} \right] \quad (7.48)$$

The output current is

$$I_1 = \frac{V_2 - (V_1 + V_S + V_D) \frac{1-k}{k}}{R \left[\frac{1}{k(1-k)} + \frac{k}{1-k} \right]} \quad (7.49)$$

The minimum conduction duty k corresponding to $I_1 = 0$ is

$$k_{\min} = \frac{V_1 + V_S + V_D}{V_1 + V_2 + V_S + V_D} \quad (7.50)$$

The power transfer efficiency is

$$\eta_D = \frac{P_O}{P_I} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + \frac{V_S + V_D}{V_1} + \frac{RI_1}{V_1} \left[\frac{1}{(1-k)^2} + \left(\frac{k}{1-k} \right)^2 \right]} \quad (7.51)$$

7.6.2 Variations of Currents and Voltages

Because the voltage across the inductor L_1 is $(V_C - RI_{L1})$ during switch-on and $(V_1 + RI_{L1})$ during switch-off, the average voltage across capacitor C is

$$kT(V_C - RI_{L1}) = (V_1 + RI_{L1})(1-k)T$$

Hence

$$V_C = \frac{1-k}{k}V_1 + \frac{1}{k}RI_{L1} = \frac{1-k}{k}V_1 + RI_1 \frac{1}{k(1-k)} \quad (7.52)$$

The peak-to-peak variation of capacitor voltage v_C is

$$\Delta v_C = \frac{(1-k)TI_2}{C} = \frac{kI_1}{fC}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{kI_1}{2fC[\frac{1-k}{k}V_1 + \frac{RI_1}{k(1-k)}]} \quad (7.53)$$

The peak-to-peak variation of current i_{L1} is

$$\Delta i_{L1} = kT \frac{V_C - V_S - RI_1}{L_1} = (1-k) \frac{V_2 - V_S - RI_2}{fL_1}$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = (1-k) \frac{V_2 - V_S - RI_2}{2fL_1 I_1} \quad (7.54)$$

Current i_{D1} during switch-off is $i_{D1} = i_{L1}$. Its peak-to-peak variation is

$$\Delta i_{D1} = \Delta i_{L1} = (1-k) \frac{V_C - V_S - RI_2}{fL_1}$$

and the variation ratio of inductor current i_{D1} is

$$\zeta_{D1} = \xi_1 = \frac{\Delta i_{D1} / 2}{I_{L1}} = k \frac{V_2 - V_S - RI_2}{2fL_1 I_2} \quad (7.54a)$$

Since voltage v_C varies very little, the peak-to-peak variation of inductor current i_{L2} is calculated by the area **B** of a triangle with width $T/2$ and height $\Delta v_C/2$:

$$\Delta i_{L2} = \frac{B}{L_2} = \frac{1}{2} \frac{T}{2} \frac{kTI_1}{2CL_2} = \frac{k}{8f^2 CL_2} I_1$$

The variation ratio of inductor current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_2} = \frac{1-k}{16f^2 CL_2} \quad (7.55)$$

7.6.3 Discontinuous Region

If the diode current becomes zero before S_2 is switched on again, the converter works in discontinuous region. The condition is $\zeta_{D1} = 1$, i.e.,

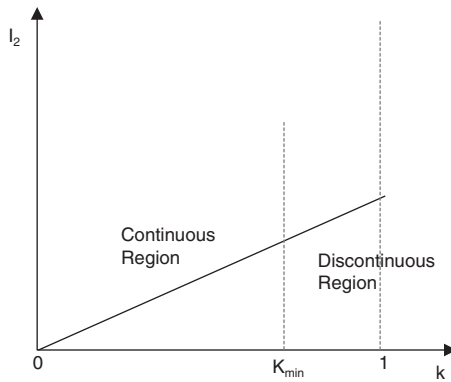


FIGURE 7.9

Boundary between continuous and discontinuous regions of Mode D.

$$k = \frac{2fL_1I_2}{V_2 - V_s - RI_2} \quad (7.56)$$

From Equations (7.50) and (7.56) the boundary between continuous and discontinuous regions is shown in Figure 7.9. Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

7.7 Simulation Results

In order to verify the above analysis and calculation formulae, and the characteristics of this converter, we applied the PSpice simulation methodology to obtain the results shown in Figure 7.10 to Figure 7.13. The first plot is current i_{L1} , the second plot is current i_{L2} , and the third plot is voltage v_C . The repeating frequency $f = 50$ Hz. The conduction duty cycle $k = 0.4$ for modes A and C, 0.8 for modes B and D. These results agree with the analysis and calculations in the previous sections.

7.8 Experimental Results

In order to verify the above analysis and calculation formulae, and the characteristics of this converter, we collected the following experimental results. The experimental testing conditions are

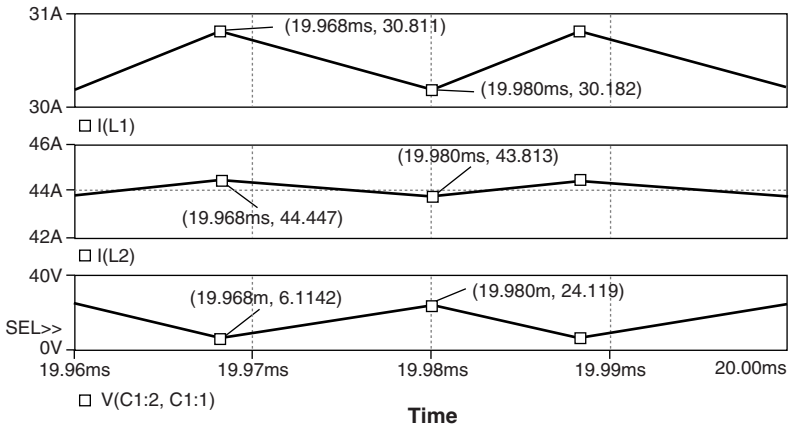


FIGURE 7.10
Simulation results of Mode A.

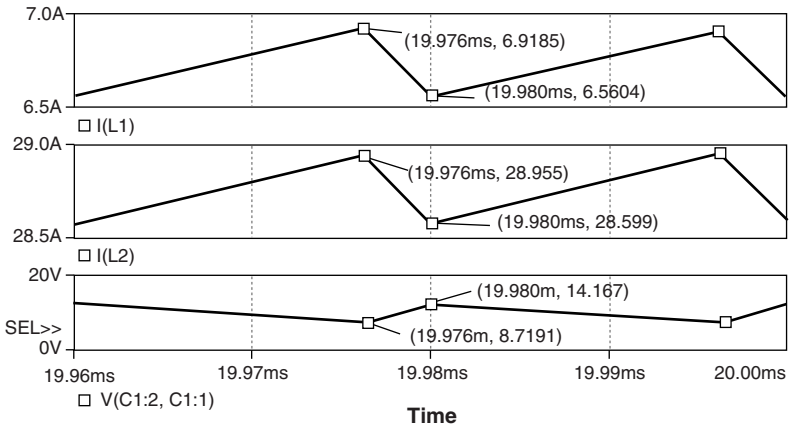


FIGURE 7.11
Simulation results of Mode B.

$$V_1 = 42 \text{ V}, V_2 = 14 \text{ V}, V_s = 0.3 \text{ V}, V_D = 0.5 \text{ V}, R = 0.05 \Omega,$$

$$L_1 = L_2 = L = L_O = 0.5 \text{ mH}, C = 20 \mu\text{F}, f = 50 \text{ kHz}$$

The experimental results corresponding to various conduction duty k are shown in [Table 7.2](#) for the Mode A, [Table 7.3](#) for the Mode B, [Table 7.4](#) for the Mode C and [Table 7.5](#) for the Mode D.

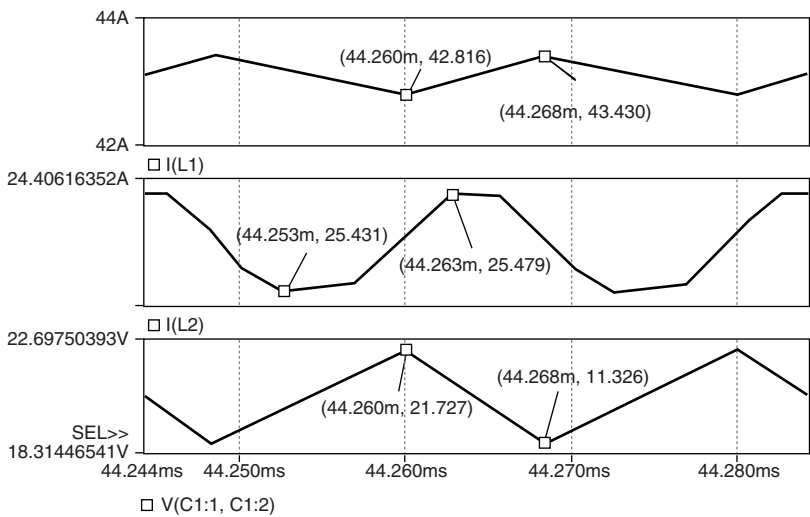


FIGURE 7.12
Simulation results of Mode C.

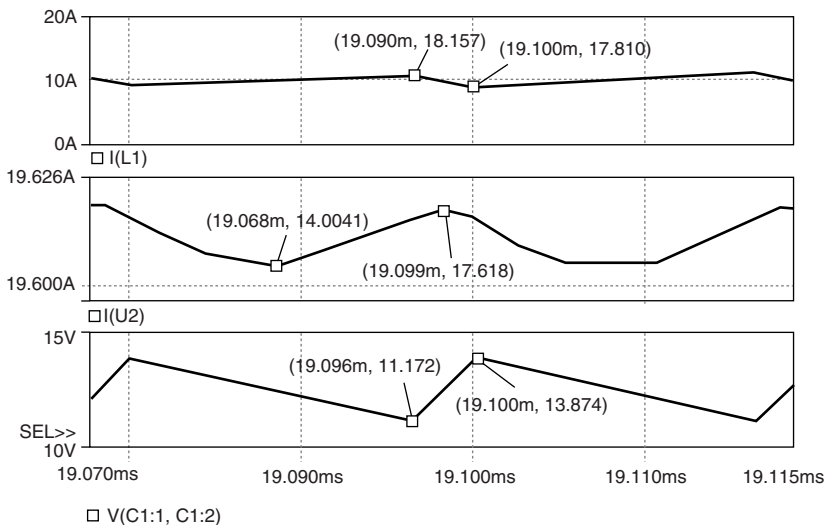


FIGURE 7.13
Simulation results of Mode D.

When compared with the analysis and calculations, the experimental results are reasonable. From these data we can see that the function of this converter has been verified.

TABLE 7.2

The Experimental Results for Mode A (Quadrant Q_I)
with $k_{min} = 0.2536$

k	I_1 (A)	I_2 (A)	V_C (V)	P_I (W)	P_O (W)	η_A (%)
0.26	3.0	8.5	14.28	126	119	94.4
0.28	13.7	35.1	15.07	575	491	85.4
0.30	26.5	61.8	15.77	1113	865	77.7
0.32	41.5	88.2	16.33	1743	1235	70.8
0.34	58.8	114.2	18.77	2470	1599	64.7

TABLE 7.3

The Experimental Results for Mode B (Quadrant Q_{II})
with $k_{min} = 0.7535$

k	I_2 (A)	I_1 (A)	V_C (V)	P_I (W)	P_O (W)	η_B
0.76	8.81	2.78	13.70	123	117	94.9
0.78	35.72	10.08	12.72	500	423	84.6
0.80	62.0	15.5	11.67	870	652	75.0
0.82	87.7	19.3	10.57	1230	810	65.9
0.84	112.9	21.5	9.43	1580	903	57.1

TABLE 7.4

The Experimental Results for Mode C (Quadrant Q_{III})
with $k_{min} = 0.2536$

k	I_1 (A)	I_2 (A)	V_C (V)	P_I (W)	P_O (W)	η_C (%)
0.26	3.0	8.5	14.28	126	119	94.4
0.28	13.7	35.1	15.07	575	491	85.4
0.30	26.5	61.8	15.77	1113	865	77.7
0.32	41.5	88.2	16.33	1743	1235	70.8
0.34	58.8	114.2	18.77	2470	1599	64.7

TABLE 7.5

The Experimental Results for Mode D (Quadrant Q_{IV})
with $k_{min} = 0.7535$

k	I_2 (A)	I_1 (A)	V_C (V)	P_I (W)	P_O (W)	η_D
0.76	8.81	2.78	13.70	123	117	94.9
0.78	35.72	10.08	12.72	500	423	84.6
0.80	62.0	15.5	11.67	870	652	75.0
0.82	87.7	19.3	10.57	1230	810	65.9
0.84	112.9	21.5	9.43	1580	903	57.1

7.9 Discussion

7.9.1 Discontinuous-Conduction Mode

Usually, the industrial applications require that the DC-DC converters work in continuous mode. However, it is irresistible that DC-DC converter works in discontinuous mode sometimes. The analysis in Sections 3.3, 4.3, 5.3, and 6.3 shows that during switch-off if current i_{D2} and i_{D1} becomes zero before next period switch on, the state is called discontinuous mode. The following factors affect the diode current to become discontinuous:

1. Switching frequency f is too low
2. Conduction duty cycle k is too small and close k_{min}
3. Inductor L is too small

7.9.2 Comparison with the Double-Output Luo-Converter

The analysis of the double output Luo-converter is based on ideal components. For example, all voltage drops are zero and inductor resistance is zero, i.e., $V_S = V_D = 0$ and $R = 0$. If we use these conditions the corresponding formulae will return back to those forms for double output Luo-converter.

From Equation (7.5):

$$k = \frac{V_2}{V_1 + V_2}$$

or

$$V_2 = \frac{k}{1-k} V_1$$

and

$$I_2 = \frac{1-k}{k} I_1$$

From Equation (7.19):

$$k = \frac{V_1}{V_1 + V_2}$$

or

$$V_1 = \frac{k}{1-k} V_2$$

and

$$I_1 = \frac{1-k}{k} I_2$$

From Equation (7.34):

$$k = \frac{V_2}{V_1 + V_2}$$

or

$$V_2 = \frac{k}{1-k} V_1$$

and

$$I_2 = \frac{1-k}{k} I_1$$

From Equation (7.48):

$$k = \frac{V_1}{V_1 + V_2}$$

or

$$V_1 = \frac{k}{1-k} V_2$$

and

$$I_1 = \frac{1-k}{k} I_2$$

because the power losses are zero, the power transfer efficiency is 100%.

7.9.3 Conduction Duty k

Since the source and load voltages are fixed, conduction duty k does not affect the voltage transfer gain. We have considered the power losses on the switches, diodes, and inductors. Therefore, the conduction duty k affects the output and input currents and power transfer efficiency. Usually, large k causes large currents and power losses. For each mode there is a minimum conduction duty k_{min} . When $k = k_{min}$ the input and output currents are zero. In order to limit the overcurrent, the values of the conduction duty k are usually selected in the range of

$$k_{min} < k < k_{min} + 0.12$$

7.9.4 Switching Frequency f

In this paper the repeating frequency $f = 50$ kHz was selected. Actually, switching frequency f can be selected in the range between 10 kHz and 500 kHz. Usually, the higher the frequency, the lower the current ripples.

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Switched Component Converters

Classic DC/DC converters consist of inductors and capacitors. They are large because of the mixture of inductors and capacitors. On engineering design experience, a circuit constructed by only inductor or capacitor may be small in size. In order to reduce the converter size and enlarge the power density, a third generation of DC/DC converters have been developed, and they are called switched component converters. Particularly, they are switched-capacitor (SC) DC/DC converters and switched-inductor (SI) DC/DC converters. The switched capacitor DC/DC converter is a new prototype of DC/DC conversion technology. Since a switched capacitor can be integrated into a power IC chip, these converters are small and have a high power density. However, most of the published papers avoid discussing the efficiency because most switched capacitor converters possess low power transfer efficiency. This section introduces a switched capacitor two-quadrant DC/DC converter implementing voltage lift and current amplification techniques with high efficiency, high power density, and low electromagnetic interference (EMI). Experimental results verified the advantages of this converter. Four-quadrant operation is required by industrial applications. SC converters can perform four-quadrant operations as well.

SC converters always perform in push-pull state, and the control circuitry is complex. A large number of capacitors are required, especially in the case of large differences between input and output voltages.

Switched inductor DC/DC converters are a prototype of DC/DC conversion technology from SC converters. Switched inductor DC/DC converters have advantages such as simple structure, simple control circuitry, high efficiency, large power, and high power density. Usually, one inductor is required for a SI DC/DC converter. Since it consists of only an inductor, it is small. This converter has advantages: no matter how many quadrant operations and how large the difference between input and output voltages, only one inductor is usually employed in one DC/DC SI converter.

8.1 Introduction

A new type DC/DC converter consisting of capacitors only was developed around the 1980s. Since it can be integrated into a power semiconductor IC chip, it has attracted much attention in recent years. However, most of the converters introduced in the literature perform single-quadrant operations. Some of them work in the flip-flop status, and their control circuit and topologies are very complex.

A newly designed DC/DC converter, *two-quadrant DC/DC converter with switched capacitors* was developed from the prototype of the authors' research work. This converter implements the voltage-lift and current-amplification technique, so that it reaches high power density and high power transfer efficiency. In order to successfully reduce electromagnetic interference (EMI), a lower switching frequency $f = 5$ kHz was applied in this converter. It can perform step-down and step-up two-quadrant positive to positive DC-DC voltage conversion with high power density, low EMI, and cheap topology in simple structure.

The conduction duty k is usually selected to be $k = 0.5$ in most of the papers in the literature. We have carefully analyzed this problem, and verified its reasonableness.

Multiple-quadrant operation is required by industrial applications. Switched-capacitor multiple quadrant converters and switched inductor multiple quadrant converters will be introduced in this chapter as well.

8.2 A Two-Quadrant SC DC/DC Converter

A two-quadrant SC converter is shown in [Figure 8.1](#). It consists of nine switches, seven diodes, and three capacitors. The high voltage (HV) source and low voltage (LV) load are usually constant voltages. The load can be a battery or motor back electromotive force (EMF). For example, the source voltage is 48 V and load voltage is 14 V. There are two modes of operation:

1. Mode A (quadrant I): electrical energy is transferred from HV side to LV side;
2. Mode B (quadrant II): electrical energy is transferred from LV side to HV side.

8.2.1 Circuit Description

Each mode has two states: *on* and *off*. Usually, each state operates in different conduction duty k . The switching period is T where $T = 1/f$. The parasitic

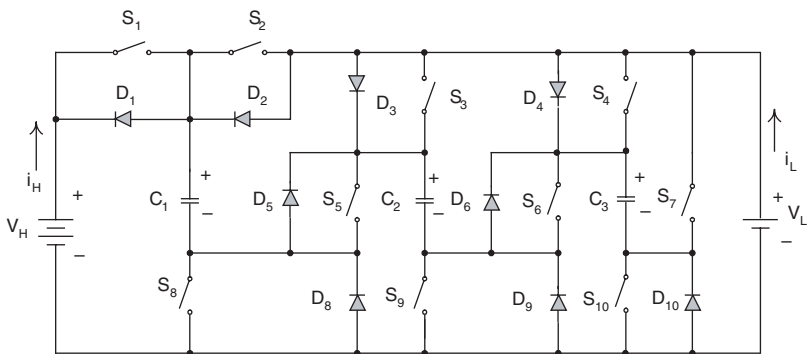


FIGURE 8.1

Two-quadrant DC/DC switched-capacitor converter.

resistance of all switches is r_s , the equivalent resistance of all capacitors is r_c and the equivalent voltage drop of all diodes is V_D . Usually select the three capacitors have same capacitance $C_1 = C_2 = C_3 = C$. Some reference data are useful: $r_s = 0.03 \Omega$, $r_c = 0.02 \Omega$, and $V_D = 0.5 \text{ V}$, $f = 5 \text{ kHz}$, and $C = 5000 \mu\text{F}$.

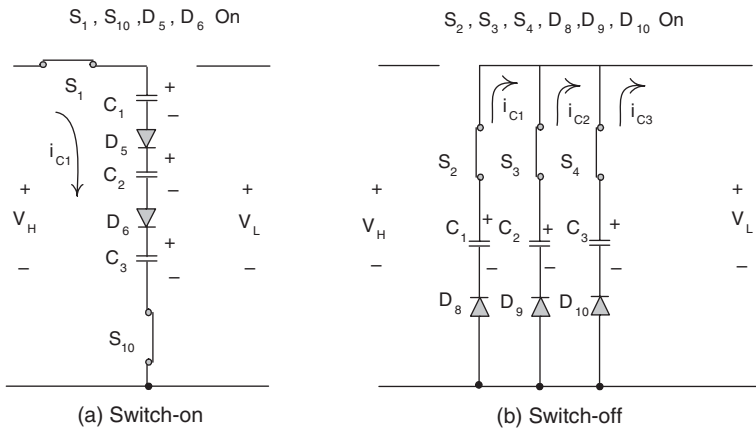
8.2.1.1 Mode A

For mode A, state-on is shown in Figure 8.2a: switches S_1 and S_{10} are closed and diodes D_5 and D_5 are conducted. Other switches and diodes are open. In this case capacitors C_1 , C_2 , and C_3 are charged via the circuit $V_H - S_1 - C_1 - D_5 - C_2 - D_6 - C_3 - S_{10}$, and the voltage across capacitors C_1 , C_2 , and C_3 is increasing. The equivalent circuit resistance is $R_{AN} = (2r_s + 3r_c) = 0.12 \Omega$, and the voltage deduction is $2V_D = 1 \text{ V}$. State-off is shown in Figure 8.2b: switches S_2 , S_3 , and S_4 are closed and diodes D_8 , D_9 , and D_9 are conducted. Other switches and diodes are open. In this case capacitor C_1 (C_2 and C_3) is discharged via the circuit $S_2(S_3 \text{ and } S_4) - V_L - D_8(D_9 \text{ and } D_{10}) - C_1(C_2 \text{ and } C_3)$, and the voltage across capacitor C_1 (C_2 and C_3) is decreasing. The equivalent circuit resistance is $R_{AF} = r_s + r_c = 0.05 \Omega$, and the voltage deduction is $V_D = 0.5 \text{ V}$. Capacitors C_1 , C_2 , and C_3 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 8.2c.

Mode A uses the **current-amplification technique**. All three capacitors are charged in series during state-on. The input current flows through three capacitors and the charges accumulated on the three capacitors should be the same. These three capacitors are discharged in parallel during state-off. Therefore, the output current is amplified by three.

8.2.1.2 Mode B

For mode B, state-on is shown in Figure 8.3a: switches S_8 , S_9 , and S_{10} are closed and diodes D_2 , D_3 , and D_4 are conducted. Other switches and diodes are off. In this case all three capacitors are charged via each circuit $V_L - D_2(\text{and } D_3, D_4) - C_1(\text{and } C_2, C_3) - S_8(\text{and } S_9, S_{10})$, and the voltage across three capacitors



(c) Some voltage and current waveforms

FIGURE 8.2
Mode A operation.

is increasing. The equivalent circuit resistance is $R_{BN} = r_s + r_c$ and the voltage deduction is V_D . State-off is shown in Figure 8.3b: switches S_5 , S_6 , and S_7 are closed and diode D_1 is on. Other switches and diodes are open. In this case all capacitors are discharged via the circuit $V_L - S_7 - C_3 - S_6 - C_2 - S_5 - C_1 - D_1 - V_H$, and the voltage across all capacitors is decreasing. The equivalent circuit resistance is $R_{BF} = 3(r_s + r_c)$ and the voltage deduction is V_D . The voltage waveform across capacitor C_1 is shown in Figure 8.3c.

Mode B implements the **voltage-lift technique**. All three capacitors are charged in parallel during state-on. The input voltage is applied to the three

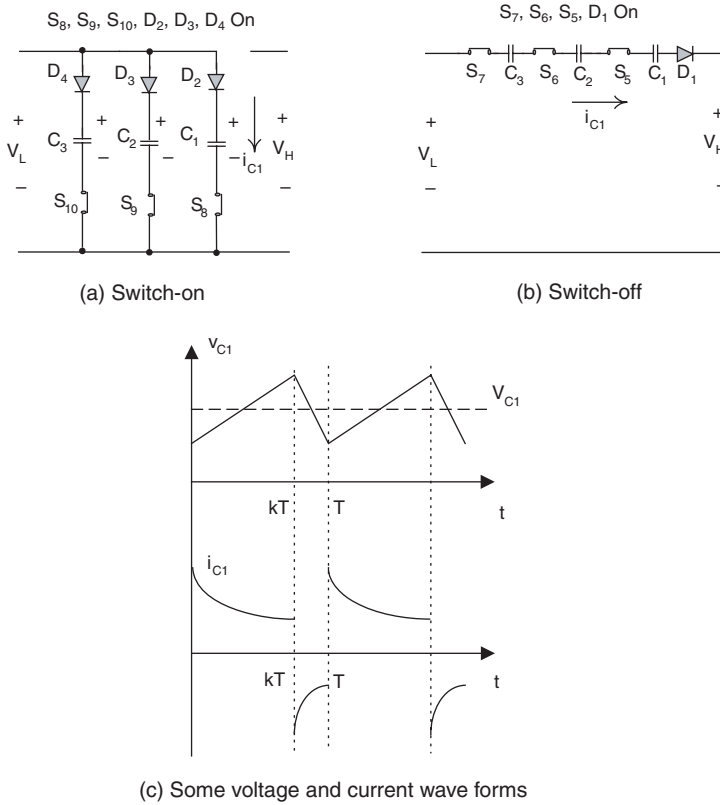


FIGURE 8.3

Mode B operation.

capacitors symmetrically, so that the voltages across these three capacitors should be the same. They are discharged in series during state-off. Therefore, the output voltage is lifted by three.

Summary. In this circuit we have $R_{AN} = 0.12 \, \Omega$, $R_{AF} = 0.05 \, \Omega$, $R_{BN} = 0.05 \, \Omega$, $R_{BF} = 0.15 \, \Omega$. The switch status is shown in [Table 8.1](#).

8.2.2 Mode A (Quadrant I Operation)

Refer to [Figure 8.2a](#) and b the voltage across capacitor C_1 increases during switch-on, and decreases during switch-off according to the integration of the current i_{C1} . If the switching period T is small enough (comparing with the circuit time constant) we can use average current to replace its instantaneous value for the integration. Therefore the voltage across capacitor C_1 is

TABLE 8.1

Switch Status

Switches and Diodes	Mode A		Mode B	
	State-on	State-off	State-on	State-off
S_1	ON			
D_1				ON
S_2, S_3, S_4		ON		
D_2, D_3, D_4			ON	
S_5, S_6, S_7				ON
D_5, D_6	ON			
S_8, S_9			ON	
S_{10}	ON		ON	
D_8, D_9, D_{10}		ON		

Note: The blank status means off.

$$v_{C1}(t) = \begin{cases} v_{C1}(0) + \frac{1}{C} \int_0^t i_{C1}(t) dt \approx v_{C1}(0) + \frac{t}{C} \bar{i}_H & 0 \leq t < kT \\ v_{C1}(kT) + \frac{1}{C} \int_{kT}^t i_{C1}(t) dt \approx v_{C1}(kT) - \frac{t - kT}{C} \bar{i}_L & kT \leq t < T \end{cases} \quad (8.1)$$

The current flowing through the three capacitors is an exponential function. If the switching period T is small enough (comparing with the circuit time constant) we can use their initial values while ignoring their variations. Therefore the current flowing through capacitor C_1 is

$$i_{C1}(t) = \begin{cases} \frac{V_H - 3v_{C1}(0) - 2V_D}{R_{AN}} (1 - e^{-t/R_{AN}C}) \approx \frac{V_H - 3V_{C1} - 2V_D}{R_{AN}} = \bar{i}_H & 0 \leq t < kT \\ -\frac{v_{C1}(kT) - V_L - V_D}{R_{AF}} e^{-t/R_{AF}C} \approx -\frac{V_{C1} - V_L - V_D}{R_{AF}} = -\bar{i}_L & kT \leq t < T \end{cases} \quad (8.2)$$

Therefore,

$$\bar{i}_H = 3 \frac{1-k}{k} \bar{i}_L \quad (8.3)$$

Where \bar{i}_H is the average input current in the switch-on period kT that is equal to I_H/k , and \bar{i}_L is the average output current in the switch-off period $(1-k)T$ that is equal to $I_L/3(1-k)$. Therefore, we have $3I_H = I_L$.

The variation of the voltage across capacitor C_1 is

$$\Delta v_{C1} = \frac{1}{C} \int_0^{kT} i_{C1}(t) dt = \frac{kT}{C} \bar{i}_H = \frac{k(V_H - 3V_{C1} - 2V_D)}{fCR_{AN}} \quad 0 \leq t < kT$$

or

$$\Delta v_{C1} = \frac{1}{C} \int_{kT}^T i_{C1}(t) dt = \frac{(1-k)T}{C} \bar{i}_L = \frac{(1-k)(V_{C1} - V_L - V_D)}{fCR_{AF}} \quad kT \leq t < (1-k)T$$

After calculation,

$$V_{C1} = \frac{k(V_H - 2V_D) + 2.4(1-k)(V_L + V_D)}{2.4 + 0.6k} \quad (8.4)$$

Hence

$$\Delta v_{C1} = \frac{k(V_H - 3V_{C1} - 2V_D)}{fCR_{AN}} = \frac{2.4k(1-k)(V_H - 3V_L - 5V_D)}{(2.4 + 0.6k)fCR_{AN}} \quad (8.5)$$

We have

$$v_{C1}(0) = V_{C1} - \frac{\Delta v_{C1}}{2} \quad \text{and} \quad v_{C1}(kT) = V_{C1} + \frac{\Delta v_{C1}}{2}$$

The average output current is

$$I_L = \frac{3}{T} \int_{kT}^T i_{C1}(t) dt \approx 3(1-k) \frac{V_{C1} - V_L - V_D}{R_{AF}} \quad (8.6)$$

The average input current is

$$I_H = \frac{1}{T} \int_0^{kT} i_{C1}(t) dt \approx k \frac{V_H - 3V_{C1} - 2V_D}{R_{AN}} \quad (8.7)$$

Output power is

$$P_O = V_L I_L = 3(1-k)V_L \frac{V_{C1} - V_L - V_D}{R_{AF}} \quad (8.8)$$

TABLE 8.2

The Calculation Results for Mode A

k	V_{C1} (V)	Δv_{C1} (V)	I_H (A)	I_L (A)	P_I (W)	P_O (W)	η_A
0.4	15.03	0.255	6.36	19.08	305.3	267.1	0.875
0.5	15.15	0.259	6.48	19.44	311.0	272.2	0.875
0.6	15.26	0.243	6.08	18.24	291.8	255.4	0.875

Input power is

$$P_I = V_H I_H = k V_H \frac{V_H - 3V_{C1} - V_D}{R_{AN}} \quad (8.9)$$

The transfer efficiency is

$$\eta_A = \frac{P_O}{P_I} = \frac{1-k}{k} \frac{3V_L}{V_H} \frac{V_{C1} - V_L - V_D}{V_H - 3V_{C1} - V_D} \frac{R_{AN}}{R_{AF}} = \frac{3V_L}{V_H} \quad (8.10)$$

If $f = 5$ kHz, $V_H = 48$ V and $V_L = 14$ V, and all $C = 5000$ μ F, for the various k values, the data are shown in [Table 8.2](#).

From this analysis, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent upon R , C , f , and k . The conduction duty k does not affect the power transfer efficiency, it affects the input and output power in a small region. The maximum output power corresponds at $k = 0.5$.

8.2.3 Mode B (Quadrant II Operation)

Refer to [Figure 8.3a and b](#), the voltage across capacitor C_1 increases during switch-on, and decreases during switch-off according to the integration of the current i_{C1} . If the switching period T is small enough we can use average current to replace its instantaneous value for the integration. Therefore the voltage across capacitor C_1 is

$$v_{C1}(t) = \begin{cases} v_{C1}(0) + \frac{1}{C} \int_0^t i_{C1}(t) dt \approx v_{C1}(0) + \frac{t}{C} \bar{i}_L & 0 \leq t < kT \\ v_{C1}(kT) + \frac{1}{C} \int_{kT}^t i_{C1}(t) dt \approx v_{C1}(kT) - \frac{t - kT}{C} \bar{i}_H & kT \leq t < T \end{cases} \quad (8.11)$$

The current flowing through the three capacitors is an exponential function. If the switching period T is small enough we can use their initial values and ignore their variations. Therefore the current flowing through capacitor C_1 is

$$i_{C1}(t) = \begin{cases} \frac{V_L - v_{C1}(0) - V_D}{R_{BN}} (1 - e^{-t/R_{BN}C}) \approx \frac{V_L - V_{C1} - V_D}{R_{BN}} = \bar{i}_L & 0 \leq t < kT \\ -\frac{3v_{C1}(kT) + V_L - V_H - V_D}{R_{BF}} e^{-t/R_{BF}C} \approx -\frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} = -\bar{i}_H & kT \leq t < T \end{cases} \quad (8.12)$$

Therefore,

$$\bar{i}_L = \frac{1-k}{k} \bar{i}_H \quad (8.13)$$

Where \bar{i}_L is the average input current in the switch-on period kT that is equal to I_L/k , and \bar{i}_H is the average output current in the switch-off period $(1-k)T$ that is equal to $I_H/3(1-k)$. Therefore, we have $4I_H = I_L$.

The variation of the voltage across capacitor C is

$$\Delta v_{C1} = \frac{1}{C} \int_0^{kT} i_{C1}(t) dt = \frac{kT}{C} \bar{i}_L = \frac{k(V_L - V_{C1} - V_D)}{fCR_{BN}} \quad 0 \leq t < kT$$

or

$$\Delta v_{C1} = \frac{1}{C} \int_{kT}^T i_{C1}(t) dt = \frac{(1-k)T}{C} \bar{i}_H = \frac{(1-k)(3V_{C1} + V_L - V_H - V_D)}{fCR_{BF}} \quad kT \leq t < (1-k)T$$

After calculation,

$$V_{C1} = k(V_L - V_D) + \frac{1-k}{3}(V_H - V_L + V_D) \quad (8.14)$$

Hence

$$\Delta v_{C1} = \frac{k(1-k)[4(V_L - V_D) - V_H]}{fCR_{BN}} \quad (8.15)$$

$$v_{C1}(0) = V_{C1} - \frac{\Delta v_{C1}}{2} \quad \text{and} \quad v_{C1}(kT) = V_{C1} + \frac{\Delta v_{C1}}{2}$$

TABLE 8.3

The Calculation Results for Mode B

k	V_{C1} (V)	ΔV_{C1} (V)	I_H (A)	I_L (A)	P_I (W)	P_O (W)	η_B
0.4	12.3	1.152	9.6	38.4	537.6	460.8	0.857
0.5	12.5	1.2	10	40	560	480	0.857
0.6	12.7	1.152	9.6	38.4	537.6	460.8	0.857

The average input current is

$$I_L = \frac{1}{T} \left[3 \int_0^{kT} i_{C1}(t) dt + \int_{kT}^T i_{C1}(t) dt \right] \approx 3k \frac{V_L - V_{C1} - V_D}{R_{BN}} + (1-k) \frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} \quad (8.16)$$

The average output current is

$$I_H = \frac{1}{T} \int_{kT}^T i_{C1}(t) dt \approx (1-k) \frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}} \quad (8.17)$$

Input power is

$$P_I = V_L I_L = V_L \left[3k \frac{V_L - V_C - V_D}{R_{BN}} + (1-k) \frac{3V_C + V_L - V_H - V_D}{R_{BF}} \right] \quad (8.18)$$

Output power is

$$P_O = V_H I_H = V_H (1-k) \frac{3V_C + V_L - V_H - V_D}{R_{BF}} \quad (8.19)$$

The transfer efficiency is

$$\eta_B = \frac{P_O}{P_I} = \frac{V_H}{4V_L} \quad (8.20)$$

If $f = 5$ kHz, $V_H = 48$ V and $V_L = 14$ V, and all $C = 5000$ μ F, for the various k values the data are shown in [Table 8.3](#).

From this analysis, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R , C , f , and k . The conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds at $k = 0.5$.

TABLE 8.4
Experimental Results

Mode	I_L (A)	I_H (A)	V_{CI} (V)	P_I (W)	P_O (W)	η (%)	\bar{P} (W)	Volume (in ³)	PD (W/in ³)
A	18.9	6.4	15.15	307	264	86	286	24	11.9
B	40	9.8	12.5	560	470	84	515	24	21.5
Average	29.45	8.1	13.8	434	367	85	400	24	16.7

8.2.4 Experimental Results

A two-quadrant DC/DC converter operates the conversion between 14 V and 48 VDC. The converter has been developed and is introduced in this paper. This converter is a two-quadrant DC/DC converter with switched-capacitors for the dual-direction conversion between 14 V and 48 VDC. A testing rig was constructed and consists of a modern car battery 14 VDC as a load and a 48 VDC source power supply. The testing conditions are

- Switching frequency: $f = 5 \text{ kHz}$
- Conduction duty: $k = 0.5$
- High and low voltages: $V_H = 48 \text{ V}$ and $V_L = 14 \text{ V}$
- All capacitance: $C = 5000 \text{ }\mu\text{F}$

The experimental results are shown in [Table 8.4](#). The average power transfer efficiency is 85%. The total average power density (PD) is 16.7 W/in³. This figure is much higher than the PD of classical converters, which are usually less than 5 W/in³. Since the switching frequency is low, the electromagnetic interference (EMI) is weak.

8.2.5 Discussion

8.2.5.1 Efficiency

From theoretical analysis and experimental results we find that the power transfer efficiency of switched capacitor converters is limited. The reason to spoil the power transfer efficiency is the power consumption on the circuit parasitic resistors and the diodes.

In steady state, the increase and decrease of the charge across a capacitor should be equal to each other. Therefore, its average input current I_I must be equal to the average output current I_O . If only one capacitor is applied in a switched capacitor DC/DC converter, its power transfer efficiency is

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = \frac{V_O}{V_I} \tag{8.21}$$

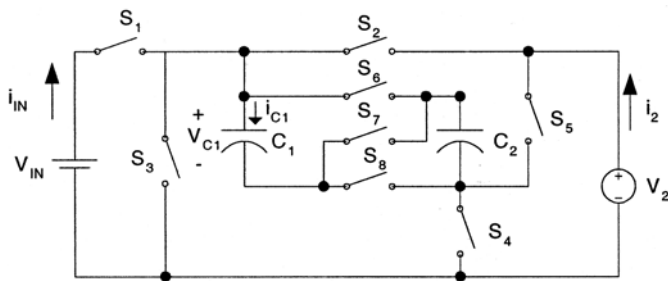


FIGURE 8.4
Four-quadrant switched-capacitor DC/DC Luo-converters.

Since the voltage-lift and current-amplification technique are applied in the circuit, the power transfer efficiency is around 86.6%, which is much higher than those of the circuits introduced by the literature.

8.2.5.2 Conduction Duty k

From the data calculated in previous sections, it can be seen that if $k = 0.4$, 0.5 , or 0.6 the efficiencies η_A and η_B are not changed. The output power is slightly affected by k , and its maximum value corresponds $k = 0.5$. Therefore, we can take the typical data corresponding to $k = 0.5$.

8.2.5.3 Switching Frequency f

Because the switching frequency $f = 5$ kHz is very low, its electromagnetic interference (EMI) is much lower than that of the traditional classical converters. The switching frequency applied in the traditional classical converters normally ranges between 50 kHz to 200 kHz.

8.3 Four-Quadrant Switched Capacitor DC/DC Luo-Converter

Since most SC DC/DC converters published in the literature perform in single-quadrant operation working in the push-pull status their control circuit and topologies are very complex. This section introduces an SC four-quadrant DC/DC Luo-converter. The experimental results verified our analysis and calculation. This converter, shown in Figure 8.4, consists of eight switches and two capacitors. The source voltage V_1 and load voltage V_2 (e.g., a battery or DC motor back EMF) are usually constant voltages. In this paper they are assumed to be 21 V and 14 V. Capacitors C_1 and C_2 are the same and $C_1 = C_2 = 2000$ μF . The circuit equivalent resistance $R = 50$ m Ω . Therefore, there are four modes of operation for this converter:

TABLE 8.5

Switch Status

Q No	Condition	ON	OFF	Source	Load
Q _I , Mode A Forw. Mot.	$V_1 > V_2$ $V_1 < V_2$	$S_{1,4,6,8}$ $S_{1,4,6,8}$	$S_{2/4/6/8}$ $S_{2/4/7}$	V_1+ I_1+	V_2+ I_2+
Q _{II} , Mode B Forw. Reg.	$V_1 > V_2$ $V_1 < V_2$	$S_{2,4,6,8}$ $S_{2,4,6,8}$	$S_{1/4/7}$ $S_{1/4/6/8}$	V_1+ I_1-	V_2+ I_2-
Q _{III} , Mode C Rev. Mot.	$V_1 > V_2 $ $V_1 < V_2 $	$S_{1,4,6,8}$ $S_{1,4,6,8}$	$S_{3/5/6/8}$ $S_{3/5/7}$	V_1+ I_1+	V_2- I_2-
Q _{IV} , Mode D Rev. Reg.	$V_1 > V_2 $ $V_1 < V_2 $	$S_{3,5,6,8}$ $S_{3,5,6,8}$	$S_{1/4/7}$ $S_{1/4/6/8}$	V_1+ I_1-	V_2- I_2+

Note: Omitted switches are off.

- Mode A (quadrant I, Q_I): energy is transferred from source to positive voltage load
- Mode B (quadrant II, Q_{II}): energy is transferred from positive voltage load to source
- Mode C (quadrant III, Q_{III}): energy is transferred from source to negative voltage load
- Mode D (quadrant IV, Q_{IV}): energy is transferred from negative voltage load to source

The first quadrant is called the forward motoring (Forw. Mot.) operation. V_1 and V_2 are positive, and I_1 and I_2 are positive as well. The second quadrant is called the forward regenerative (Forw. Reg.) braking operation. V_1 and V_2 are positive, and I_1 and I_2 are negative. The third quadrant is called the reverse motoring (Rev. Mot.) operation. V_1 and I_1 are positive, and V_2 and I_2 are negative. The fourth quadrant is called the reverse regenerative (Rev. Reg.) braking operation. V_1 and I_2 are positive, and I_1 and V_2 are negative.

Each mode has two conditions: $V_1 > V_2$ and $V_1 < V_2$. Each condition has two states: *on* and *off*. Usually, each state operates in a different conduction duty k . The switching period is T where $T = 1/f$. The switch status is shown in Table 8.5.

For mode A1, condition $V_1 > V_2$ is shown in Figure 8.5. Since $V_1 > V_2$ two capacitors C_1 and C_2 can be used in parallel. During switch-**on** state, switches S_1 , S_4 , S_6 , and S_8 are closed and other switches are open. In this case capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-**off** state, switches S_2 , S_4 , S_6 , and S_8 are closed and other switches are open. In this case capacitors $C_1//C_2$ are discharged via the circuit $S_2-V_2-S_4-C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 8.5c.

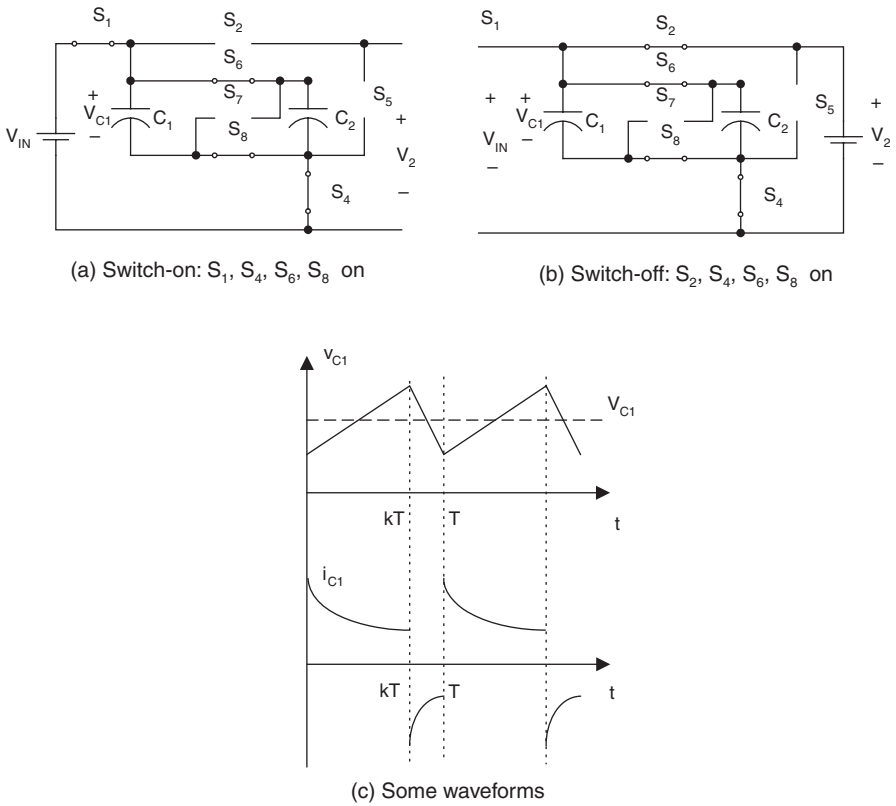
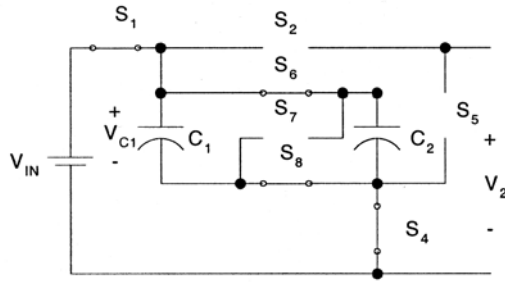


FIGURE 8.5

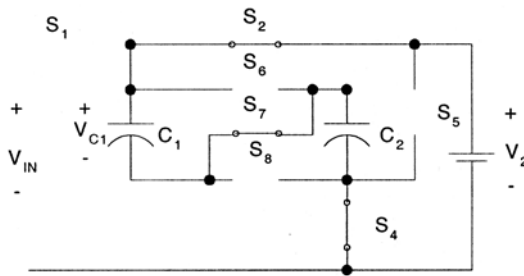
Mode A1 (quadrant I) forward motoring operation with $V_1 > V_2$.

For mode A2, condition $V_1 < V_2$ is shown in Figure 8.6. Since $V_1 < V_2$ two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off. This is the voltage lift technique. During switch-on state, switches S_1, S_4, S_6 , and S_8 are closed and other switches are open. In this case capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_2, S_4 , and S_7 are closed and other switches are open. In this case capacitors C_1 and C_2 are discharged via the circuit $S_2-V_2-S_4-C_1-S_7-C_2$, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 8.6c.

For mode B1, condition $V_1 > V_2$ is shown in Figure 8.7. Since $V_1 > V_2$ two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off. The voltage lift technique is applied. During switch-on state, switches S_2, S_4, S_6 , and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit $V_2-S_2-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_1, S_4 , and S_7 are



(a) Switch-on: S1, S4, S6 and S8 on.



(b) Switch-off: S2, S4 and S7 on.

FIGURE 8.6

Mode A2 (quadrant I) forward motoring operation with $V_1 < V_2$.

closed. In this case capacitors C_1 and C_2 are discharged via the circuit S_1 – V_1 – S_4 – C_2 – S_7 – C_1 , and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 8.7c.

For mode B2, condition $V_1 < V_2$ is shown in Figure 8.8. Since $V_1 < V_2$ two capacitors C_1 and C_2 can be used in parallel. During switch-on state, switches S_2 , S_4 , S_6 , and S_8 are closed. In this case capacitors C_1 and C_2 are charged via the circuit V_2 – S_2 – C_1 and C_2 – S_4 , and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_1 , S_4 , S_6 , and S_8 are closed. In this case capacitors C_1 and C_2 are discharged via the circuit S_1 – V_1 – S_4 – C_1 and C_2 , and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 8.8c.

For mode C1, condition $V_1 > |V_2|$ is shown in Figure 8.9. Since $V_1 > |V_2|$ two capacitors C_1 and C_2 can be used in parallel. During switch-on state, switches S_1 , S_4 , S_6 , and S_8 are closed. In this case capacitors C_1 and C_2 are

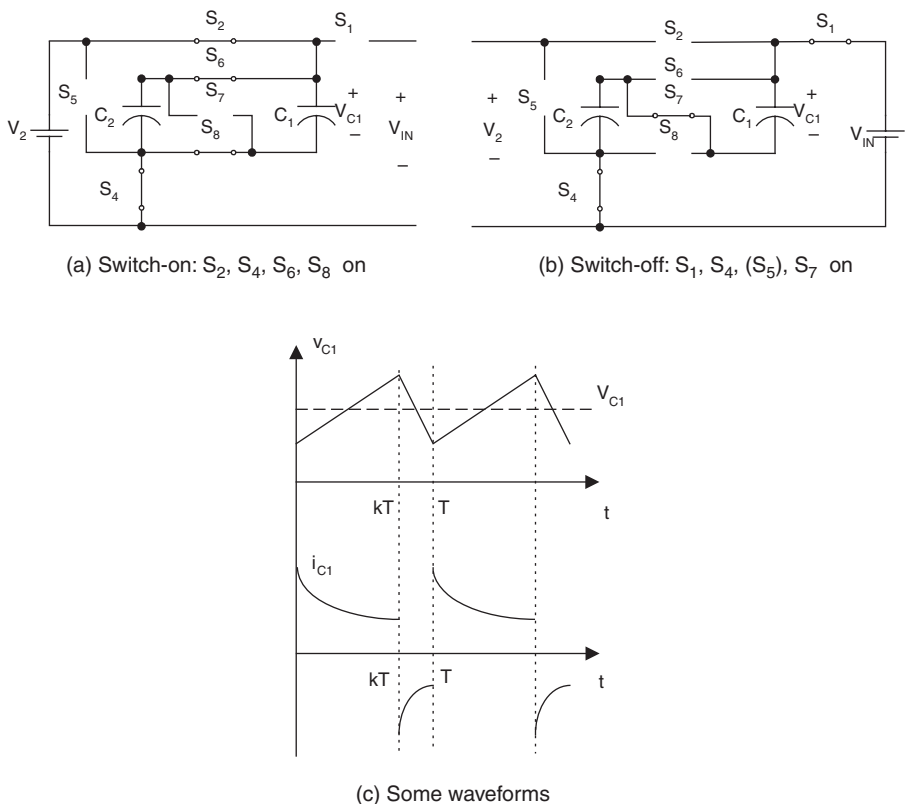


FIGURE 8.7

Mode B1 (quadrant II) forward motoring operation with $V_1 > V_2$.

charged via the circuit V_1 – S_1 – C_1 // C_2 – S_4 , and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_3, S_5, S_6 , and S_8 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_3 – V_2 – S_5 – C_1 // C_2 , and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 8.9c.

For mode C2, condition $V_1 < |V_2|$ is shown in Figure 8.10. Since $V_1 < |V_2|$ two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off, applying the voltage lift technique. During switch-on state, switches S_1, S_4, S_6 , and S_8 are closed. Capacitors C_1 and C_2 are charged via the circuit V_1 – S_1 – C_1 // C_2 – S_4 , and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_3, S_5 , and S_7 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_3 – V_2 – S_5 – C_1 – S_7 – C_2 , and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 8.10c.

For mode D1, condition $V_1 > |V_2|$ is shown in Figure 8.11. Since $V_1 > |V_2|$ two capacitors C_1 and C_2 are in parallel during switch-on and in series

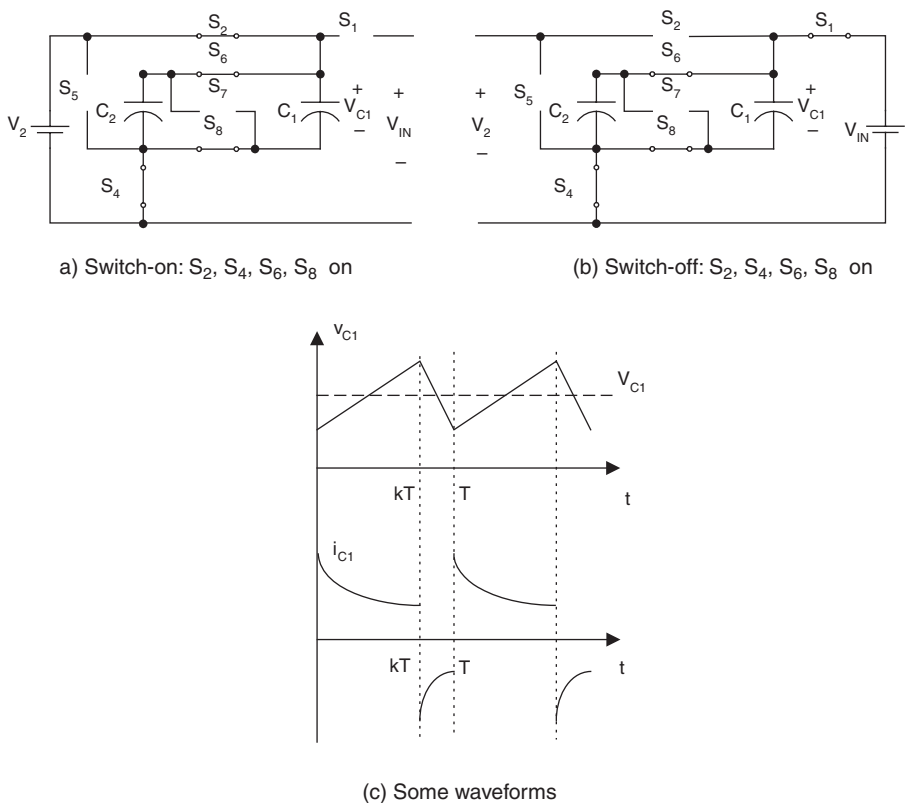


FIGURE 8.8

Mode B2 (quadrant II) forward motoring operation with $V_1 < V_2$.

during switch-off, applying the voltage lift technique. During switch-on state, switches S_3, S_5, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit $V_2-S_3-C_1//C_2-S_5$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_1, S_4 and S_7 are closed. Capacitors C_1 and C_2 are discharged via the circuit $S_1-V_1-S_4-C_2-S_7-C_1$, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 8.11c.

For Mode D2, condition $V_1 < |V_2|$ is shown in Figure 8.12. Since $V_1 < |V_2|$ two capacitors C_1 and C_2 can be used in parallel. During switch-on state, switches S_3, S_5, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit $V_2-S_3-C_1//C_2-S_5$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state, switches S_1, S_4, S_6 and S_8 are closed. Capacitors C_1 and C_2 are discharged via the circuit $S_1-V_1-S_4-C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 8.12c.

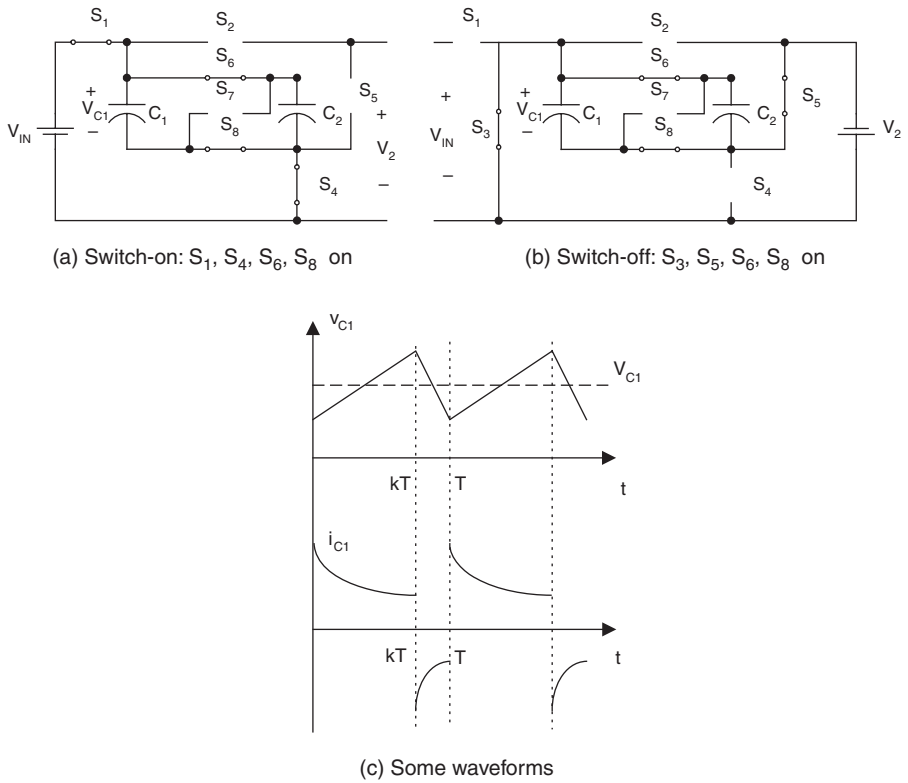


FIGURE 8.9
Mode C1 (quadrant III) forward motoring operation with $V_1 > V_2$.

8.3.1 Mode A (Q_I: Forward Motoring)

8.3.1.1 Mode A1: Condition $V_1 > V_2$

Mode A1, condition $V_1 > V_2$, is shown in Figure 8.5. Because two capacitors are connected in parallel, the total capacitance is $C = C_1 + C_2 = 4000 \mu\text{F}$. Suppose that the equivalent circuit resistance is $R = 50 \text{ m}\Omega$, $V_1 = 21 \text{ V}$ and $V_2 = 14 \text{ V}$, and the switching frequency is $f = 5 \text{ kHz}$. The voltage and current across the capacitors are

$$v_c(t) = \begin{cases} v_c(0) + \frac{1}{C} \int_0^t i_c(t) dt \approx v_c(0) + \frac{t}{C} \bar{i}_1 & 0 \leq t < kT \\ v_c(kT) + \frac{1}{C} \int_{kT}^t i_c(t) dt \approx v_c(kT) - \frac{t - kT}{C} \bar{i}_2 & kT \leq t < T \end{cases} \quad (8.22)$$

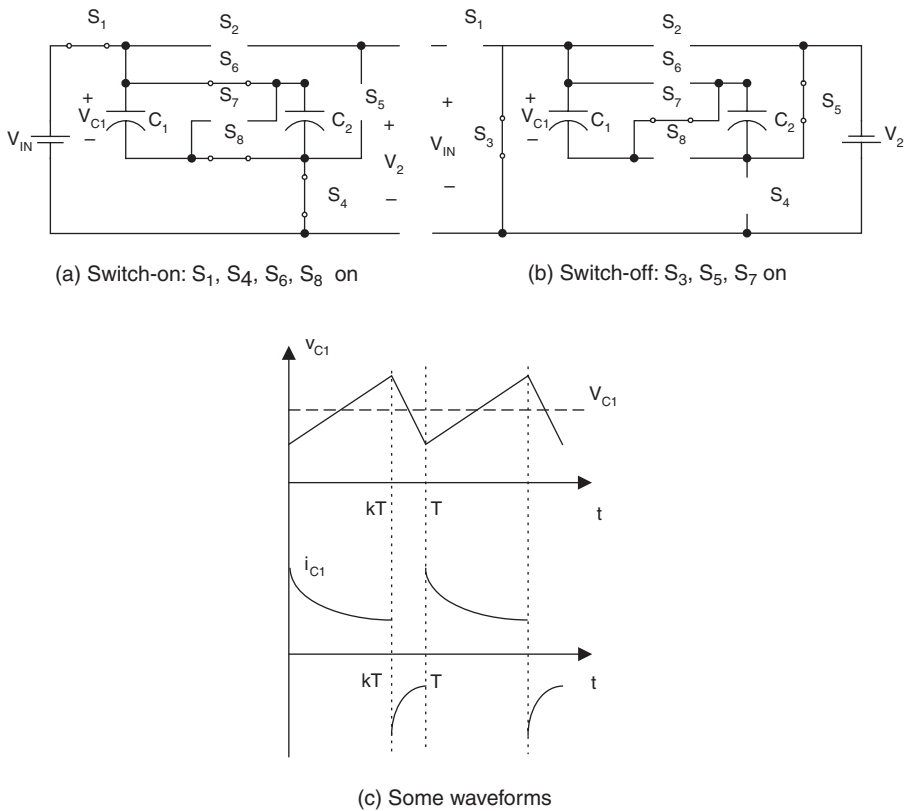


FIGURE 8.10

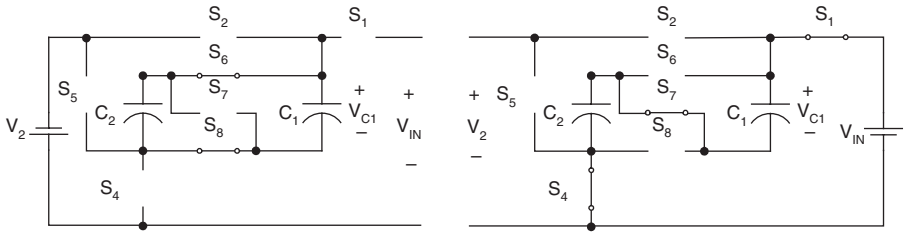
Mode C2 (quadrant III) forward motoring operation with $V_1 < V_2$.

$$i_C(t) = \begin{cases} \frac{V_1 - v_C(0)}{R} (1 - e^{-t/RC}) \approx \frac{V_1 - V_C}{R} = \bar{i}_1 & 0 \leq t < kT \\ -\frac{v_C(kT) - V_2}{R} e^{-t/RC} \approx -\frac{V_C - V_2}{R} = -\bar{i}_2 & kT \leq t < T \end{cases} \quad (8.23)$$

Therefore,

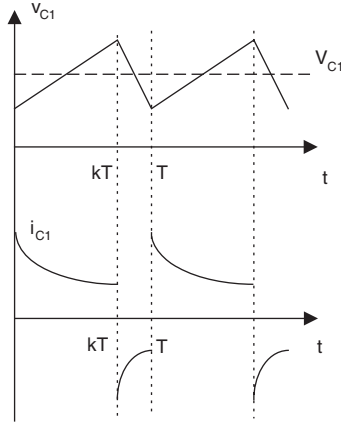
$$\bar{i}_1 = \frac{1-k}{k} \bar{i}_2 \quad (8.24)$$

Where \bar{i}_1 is the average input current in the switch-on period kT that is equal to I_1/k , and \bar{i}_2 is the average output current in the switch-off period $(1-k)T$ that is equal to $I_2/(1-k)$. Therefore, we have $I_1 = I_2$. The variation of the voltage across capacitor C is



(a) Switch-on: S_3, S_5, S_6, S_8 on

(b) Switch-off: S_1, S_4, S_7 on



(c) Some waveforms

FIGURE 8.11

Mode D1 (quadrant IV) forward motoring operation with $V_1 > V_2$.

$$\Delta v_C = \frac{1}{C} \int_0^{kT} i_C(t) dt = \frac{kT}{C} \bar{i}_1 = \frac{k(V_1 - V_C)}{fCR} \quad 0 \leq t < kT$$

or

$$\Delta v_C = \frac{1}{C} \int_{kT}^T i_C(t) dt = \frac{(1-k)T}{C} \bar{i}_2 = \frac{(1-k)(V_C - V_2)}{fCR} \quad kT \leq t < T$$

After calculation,

$$V_C = kV_1 + (1-k)V_2 \quad (8.25)$$

Hence

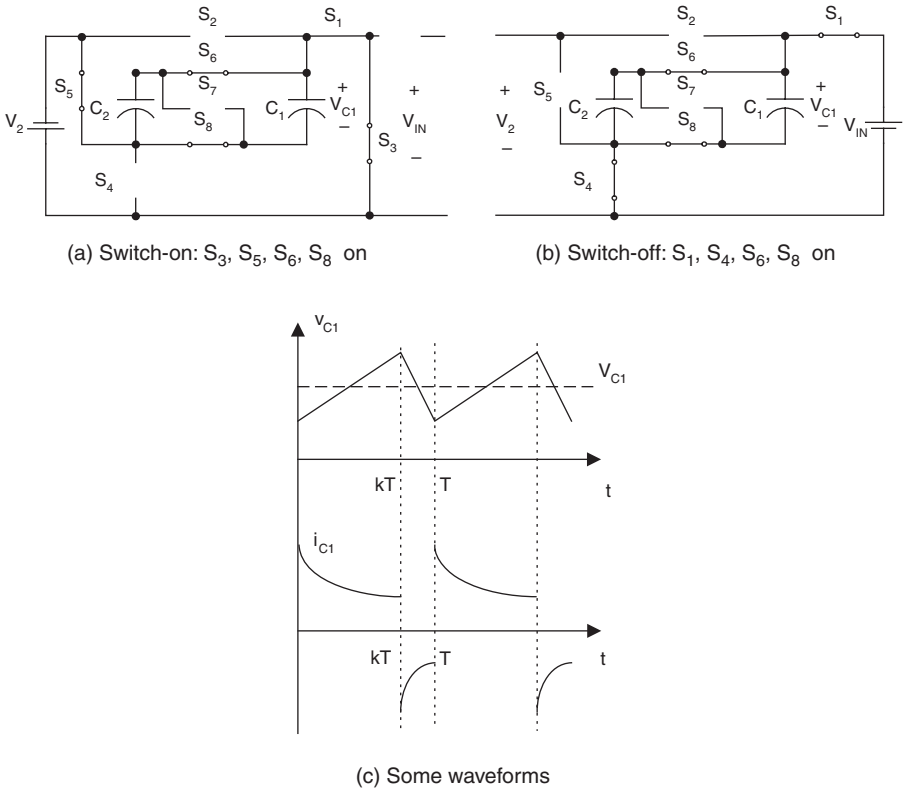


FIGURE 8.12

Mode D2 (quadrant IV) forward motoring operation with $V_1 < V_2$.

$$\Delta v_C = \frac{k(1-k)(V_1 - V_2)}{fCR} \quad (8.26)$$

We then have

$$v_C(0) = V_C - \frac{\Delta v_C}{2}$$

and

$$v_C(kT) = V_C + \frac{\Delta v_C}{2}$$

The average output current is

TABLE 8.6The Calculation Results for Mode A1 ($V_1 > V_2$)

k	V_C	Δv_C	I_1	I_2	η_{A1}
0.4	16.8 V	1.68 V	33.6 A	33.6 A	0.67
0.5	17.5 V	1.75 V	35 A	35 A	0.67
0.6	18.2 V	1.68 V	33.6 A	33.6 A	0.67

$$I_2 = \frac{1}{T} \int_{kT}^T i_C(t) dt \approx (1-k) \frac{V_C - V_2}{R} \quad (8.27)$$

$$I_1 = \frac{1}{T} \int_0^{kT} i_C(t) dt \approx k \frac{V_1 - V_C}{R} \quad (8.28)$$

Output power is

$$P_O = V_2 I_2 = (1-k) V_2 \frac{V_C - V_2}{R} \quad (8.29)$$

Input power is

$$P_I = V_1 I_1 = k V_1 \frac{V_1 - V_C}{R} \quad (8.30)$$

The transfer efficiency is

$$\eta_{A1} = \frac{P_O}{P_I} = \frac{1-k}{k} \frac{V_2}{V_1} \frac{V_C - V_2}{V_1 - V_C} = \frac{V_2}{V_1} \quad (8.31)$$

From this equation it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R , C , f , and k . If $f = 5$ kHz, $V_1 = 21$ V and $V_2 = 14$ V, and total $C = 4000$ μ F, $R = 50$ m Ω , for three k values the data are found in [Table 8.6](#).

From the analysis and calculation, it can be seen that the conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds at $k = 0.5$.

8.3.1.2 Mode A2: Condition $V_1 < V_2$

Mode A2, condition $V_1 < V_2$, is shown in [Figure 8.6](#). Because two capacitors are connected in parallel during switch-on, the total capacitance $C = 2 \times C_1$

= 4000 μF . Input current i_1 is two times that of capacitor current i_{C1} . Two capacitors are connected in series during switch-off, the total capacitance $C' = C_1/2 = 1000 \mu\text{F}$. Output current i_2 is equal to capacitor current i_{C1} . Suppose that the equivalent circuit resistance $R = 50 \text{ m}\Omega$, $V_1 = 14 \text{ V}$ and $V_2 = 21 \text{ V}$, and the switching frequency is $f = 5 \text{ kHz}$. The voltage and current across each capacitor are

$$v_{C1}(t) = \begin{cases} v_{C1}(0) + \frac{1}{C_1} \int_0^t i_{C1}(t) dt \approx v_{C1}(0) + \frac{t}{2C_1} \bar{i}_1 & 0 \leq t < kT \\ v_{C1}(kT) + \frac{1}{C_1} \int_{kT}^t i_{C1}(t) dt \approx v_{C1}(kT) - \frac{t - kT}{C_1} \bar{i}_2 & kT \leq t < T \end{cases} \quad (8.32)$$

$$i_{C1}(t) = \begin{cases} \frac{V_1 - v_{C1}(0)}{R} (1 - e^{-t/RC}) \approx \frac{V_1 - V_{C1}}{R} = \bar{i}_1 / 2 & 0 \leq t < kT \\ -\frac{2v_{C1}(kT) - V_2}{R} e^{-t/RC} \approx -\frac{2V_{C1} - V_2}{R} = -\bar{i}_2 & kT \leq t < T \end{cases} \quad (8.33)$$

Therefore,

$$\bar{i}_1 = 2 \frac{1-k}{k} \bar{i}_2 \quad (8.34)$$

Where \bar{i}_1 is the average input current in the switch-on period kT that is equal to I_1/k , and $2 \bar{i}_2$ is the average output current in the switch-off period $(1-k)T$ that is equal to $I_2/(1-k)$. Therefore, we have $I_1 = 2I_2$. The variation of the voltage across capacitor C is

$$\Delta v_C = \frac{1}{C} \int_0^{kT} i_C(t) dt = \frac{kT}{2C} \bar{i}_1 = \frac{k(V_1 - V_C)}{2fCR} \quad 0 \leq t < kT$$

or

$$\Delta v_C = \frac{1}{C} \int_{kT}^T i_C(t) dt = \frac{(1-k)T}{C} \bar{i}_2 = \frac{(1-k)(2V_C - V_2)}{fCR} \quad kT \leq t < T$$

To simplify the calculation, set $k = 0.5$ we have:

$$V_C = \frac{0.5V_1 + V_2}{2.5} = 11.2 \text{ V} \quad (8.35)$$

Hence

$$\Delta v_c = \frac{k(V_1 - V_c)}{2fCR} = 0.7 \text{ V} \quad (8.36)$$

We then have

$$v_c(0) = V_c - \frac{\Delta v_c}{2} = 10.85 \text{ V}$$

and

$$v_c(kT) = V_c + \frac{\Delta v_c}{2} = 11.55 \text{ V}$$

The average output current is

$$I_2 = \frac{1}{T} \int_{kT}^T i_c(t) dt \approx (1-k) \frac{2V_c - V_2}{R} \quad (8.37)$$

The average input current is

$$I_1 = \frac{1}{T} \int_0^{kT} i_c(t) dt \approx k \frac{V_1 - V_c}{R} \quad (8.38)$$

Output power is

$$P_O = V_2 I_2 = (1-k) V_2 \frac{2V_c - V_2}{R} \quad (8.39)$$

Input power is

$$P_I = V_1 I_1 = k V_1 \frac{V_1 - V_c}{R} \quad (8.40)$$

The transfer efficiency is

$$\eta_{A2} = \frac{P_O}{P_I} = \frac{1-k}{k} \frac{V_2}{V_1} \frac{2V_c - V_2}{V_1 - V_c} = \frac{V_2}{2V_1} \quad (8.41)$$

TABLE 8.7The Calculation Results for Mode A2 ($V_1 < V_2$)

k	V_c (V)	Δv_c (V)	I_1 (A)	I_2 (A)	P_1 (W)	P_O (W)	η_{A2}
0.5	11.2	0.7 V	28	14	392	294	0.75

TABLE 8.8

Experimental Results

I_1 (A)	I_2 (A)	V_c (V)	P_1 (W)	P_O (W)	h	\bar{P} (W)	PD (W/in ³)
33	32	17.5	693	448	0.646	571	23.8

From this equation it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R , C , f , and k . If $f = 5$ kHz, $V_1 = 14$ V and $V_2 = 21$ V and total $C = 4000$ μ F, $R = 50$ m Ω . For $k = 0.5$ the data are listed in Table 8.7.

From the analysis and calculation, it can be seen the power transfer efficiency only depends on the source and load voltages.

8.3.1.3 Experimental Results

A testing rig of two batteries 14 VDC and 21 VDC was prepared. The testing conditions were $f = 5$ kHz, $V_1 = 21$ V and $V_2 = 14$ V, total $C = 4000$ μ F, $R = 50$ m Ω . The experimental results for mode A are shown in Table 8.8. The equipment volume is 24 in³. The total average power density (PD) is 23.8 W/in³. This figure is much higher than the classical converters whose PD is usually less than 5 W/in³. Since the switching frequency is low, the electromagnetic interference (EMI) is weak.

8.3.2 Mode B (Q_{II} : Forward Regenerative Braking)

8.3.2.1 Mode B1: Condition $V_1 > V_2$

Mode B1, condition $V_1 > V_2$ is shown in Figure 8.7. This mode operation is similar to mode A2. Because two capacitors are connected in parallel during switch-on, the total capacitance $C = 2 \times C_1 = 4000$ μ F. Input current i_1 is two times the capacitor current i_{C1} . Two capacitors are connected in series during switch-off, the total capacitance $C' = C_1/2 = 1000$ μ F. Output current i_2 is equal to capacitor current i_{C1} . Suppose that the equivalent circuit resistance $R = 50$ m Ω , $V_1 = 21$ V and $V_2 = 14$ V, and the switching frequency $f = 5$ kHz, in order to save the description we quote the results as follows. The voltage and current across each capacitor are

$$v_{C1}(t) = \begin{cases} v_{C1}(0) + \frac{1}{C_1} \int_0^t i_{C1}(t) dt \approx v_{C1}(0) + \frac{t}{2C_1} \bar{i}_2 & 0 \leq t < kT \\ v_{C1}(kT) + \frac{1}{C_1} \int_{kT}^t i_{C1}(t) dt \approx v_{C1}(kT) - \frac{t - kT}{C_1} \bar{i}_1 & kT \leq t < T \end{cases} \quad (8.42)$$

$$i_{C1}(t) = \begin{cases} \frac{V_2 - v_{C1}(0)}{R} (1 - e^{-t/RC}) \approx \frac{V_2 - V_{C1}}{R} = \bar{i}_2 / 2 & 0 \leq t < kT \\ -\frac{2v_{C1}(kT) - V_1}{R} e^{-t/RC} \approx -\frac{2V_{C1} - V_1}{R} = -\bar{i}_1 & kT \leq t < T \end{cases} \quad (8.43)$$

Therefore,

$$\bar{i}_2 = 2 \frac{1-k}{k} \bar{i}_1 \quad (8.44)$$

where \bar{i}_2 is the average input current in the switch-on period, kT is equal to I_2/k , and $2\bar{i}_1$ is the average output current in the switch-off period $(1-k)T$ that is equal to $I_1/(1-k)$. Therefore, we have $I_2 = 2I_1$. The variation of the voltage across capacitor C is

$$\Delta v_C = \frac{1}{C} \int_0^{kT} i_C(t) dt = \frac{kT}{2C} \bar{i}_2 = \frac{k(V_2 - V_C)}{2fCR} \quad 0 \leq t < kT$$

or

$$\Delta v_C = \frac{1}{C} \int_{kT}^T i_C(t) dt = \frac{(1-k)T}{C} \bar{i}_1 = \frac{(1-k)(2V_C - V_1)}{fCR} \quad kT \leq t < T$$

To simplify the calculation, set $k = 0.5$:

$$V_C = \frac{0.5V_2 + V_1}{2.5} = 11.2 \text{ V} \quad (8.45)$$

Hence

$$\Delta v_C = \frac{k(V_2 - V_C)}{2fCR} = 0.7 \text{ V} \quad (8.46)$$

$$v_c(0) = V_c - \frac{\Delta v_c}{2} = 10.85 \text{ V}$$

and

$$v_c(kT) = V_c + \frac{\Delta v_c}{2} = 11.55 \text{ V}$$

The average output current is

$$I_1 = \frac{1}{T} \int_{kT}^T i_c(t) dt \approx (1-k) \frac{2V_c - V_1}{R} \quad (8.47)$$

The average input current is

$$I_2 = \frac{1}{T} \int_0^{kT} i_c(t) dt \approx k \frac{V_2 - V_c}{R} \quad (8.48)$$

Output power is

$$P_O = V_1 I_1 = (1-k) V_1 \frac{2V_c - V_1}{R} \quad (8.49)$$

Input power is

$$P_I = V_2 I_2 = k V_2 \frac{V_2 - V_c}{R} \quad (8.50)$$

The transfer efficiency is

$$\eta_{B1} = \frac{P_O}{P_I} = \frac{1-k}{k} \frac{V_1}{V_2} \frac{2V_c - V_1}{V_2 - V_c} = \frac{V_1}{2V_2} \quad (8.51)$$

From this equation it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R , C , f , and k . If $f = 5 \text{ kHz}$, $V_1 = 21 \text{ V}$ and $V_2 = 14 \text{ V}$ and total $C = 4000 \text{ } \mu\text{F}$, $R = 50 \text{ m}\Omega$, for $k = 0.5$ the data are listed in [Table 8.9](#).

From the analysis and calculation, it can be seen the power transfer efficiency only depends on the source and load voltages.

TABLE 8.9The Calculation Results for Mode B1 ($V_1 > V_2$)

k	V_C (V)	Δv_C (V)	I_1 (W)	I_2 (W)	P_1 (W)	P_O (W)	η_{B1}
0.5	11.2	0.7	28	14	392	294	0.75

8.3.2.2 Mode B2: Condition $V_1 < V_2$

Mode B2, condition $V_1 < V_2$ is shown in [Figure 8.8](#). This mode is similar to the mode A1. Because two capacitors are connected in parallel, the total capacitance $C = C_1 + C_2 = 4000 \mu\text{F}$. Suppose that the equivalent circuit resistance $R = 50 \text{ m}\Omega$, $V_2 = 21 \text{ V}$ and $V_1 = 14 \text{ V}$, and the switching frequency $f = 5 \text{ kHz}$, the voltage and current across the capacitors are

$$v_C(t) = \begin{cases} v_C(0) + \frac{1}{C} \int_0^t i_C(t) dt \approx v_C(0) + \frac{t}{C} \bar{i}_2 & 0 \leq t < kT \\ v_C(kT) + \frac{1}{C} \int_{kT}^t i_C(t) dt \approx v_C(kT) - \frac{t - kT}{C} \bar{i}_1 & kT \leq t < T \end{cases} \quad (8.52)$$

$$i_C(t) = \begin{cases} \frac{V_2 - v_C(0)}{R} (1 - e^{-t/RC}) \approx \frac{V_2 - V_C}{R} = \bar{i}_2 & 0 \leq t < kT \\ -\frac{v_C(kT) - V_1}{R} e^{-t/RC} \approx -\frac{V_C - V_1}{R} = -\bar{i}_1 & kT \leq t < T \end{cases} \quad (8.53)$$

Therefore,

$$\bar{i}_2 = \frac{1-k}{k} \bar{i}_1 \quad (8.54)$$

Where \bar{i}_2 is the average input current in the switch-on period kT that is equal to I_2/k , and \bar{i}_1 is the average output current in the switch-off period $(1-k)T$ that is equal to $I_1/(1-k)$. Therefore, we have $I_2 = I_1$. The variation of the voltage across capacitor C is

$$\Delta v_C = \frac{1}{C} \int_0^{kT} i_C(t) dt = \frac{kT}{C} \bar{i}_2 = \frac{k(V_2 - V_C)}{fCR} \quad 0 \leq t < kT$$

or

$$\Delta v_C = \frac{1}{C} \int_{kT}^T i_C(t) dt = \frac{(1-k)T}{C} \bar{i}_1 = \frac{(1-k)(V_C - V_1)}{fCR} \quad kT \leq t < T$$

After calculation,

$$V_C = kV_2 + (1-k)V_1 \quad (8.55)$$

Hence

$$\Delta v_C = \frac{k(1-k)(V_2 - V_1)}{fCR} \quad (8.56)$$

We then have

$$v_C(0) = V_C - \frac{\Delta v_C}{2}$$

and

$$v_C(kT) = V_C + \frac{\Delta v_C}{2}$$

The average output current is

$$I_1 = \frac{1}{T} \int_{kT}^T i_C(t) dt \approx (1-k) \frac{V_C - V_1}{R} \quad (8.57)$$

The average input current is

$$I_2 = \frac{1}{T} \int_0^{kT} i_C(t) dt \approx k \frac{V_2 - V_C}{R} \quad (8.58)$$

Output power is

$$P_O = V_1 I_1 = (1-k) V_1 \frac{V_C - V_1}{R} \quad (8.59)$$

Input power is

$$P_I = V_2 I_2 = k V_2 \frac{V_2 - V_C}{R} \quad (8.60)$$

The transfer efficiency is

TABLE 8.10The Calculation Results for Mode B2 ($V_1 < V_2$)

k	V_C	Δv_C	I_1	I_2	η_{A1}
0.4	16.8 V	1.68 V	33.6 A	33.6 A	0.67
0.5	17.5 V	1.75 V	35 A	35 A	0.67
0.6	18.2 V	1.68 V	33.6A	33.6A	0.67

$$\eta_{B2} = \frac{P_O}{P_I} = \frac{1-k}{k} \frac{V_1}{V_2} \frac{V_C - V_1}{V_2 - V_C} = \frac{V_1}{V_2} \quad (8.61)$$

The transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R , C , f , and k . If $f = 5$ kHz, $V_2 = 21$ V and $V_1 = 14$ V and total $C = 4000$ μ F, $R = 50$ m Ω . For three k values we obtain the data in [Table 8.10](#).

From the analysis and calculation, it can be seen that the conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds at $k = 0.5$.

8.3.3 Mode C (Q_{III} : Reverse Motoring)

This mode is similar to the mode A.

8.3.4 Mode D (Q_{IV} : Reverse Regenerative Braking)

This mode is similar to the mode B.

8.4 Switched Inductor Four-Quadrant DC/DC Luo-Converter

Although switched-capacitor DC/DC converters can reach high power density, their circuits are always very complex with difficult control. If the difference between input and output voltages is large, multiple switch-capacitor stages must be employed. Switched inductor DC/DC converters successfully overcome this disadvantage. Usually, only one inductor is required for each converter with 1-quadrant, 2-quadrant or 4-quadrant operation no matter how large the difference between the input and output voltages. Therefore, the switched inductor converter is a very simple circuit and consequently has high power density. This section introduces an SI four-quadrant DC/DC Luo-converter working in four-quadrant operation.

This converter is shown in [Figure 8.13a](#) consisting of three switches, two diodes, and only one inductor L . The source voltage V_1 and load voltage V_2 (e.g., a battery or DC motor back EMF) are usually constant voltages. R is the equivalent resistance of the circuit, it is usually small. Its equivalent circuits for quadrant I and II, and quadrant III and IV operation are shown in [Figure 8.13b and c](#). Assuming the condition $V_1 > |V_2|$, they are +42 V and ± 14 V, respectively. Therefore, there are four quadrants (modes) of operation:

- Mode A (quadrant I: Q_I): the energy is transferred from source to positive voltage load
- Mode B (quadrant II: Q_{II}): the energy is transferred from positive voltage load to source
- Mode C (quadrant III: Q_{III}): the energy is transferred from source to negative voltage load
- Mode D (quadrant IV: Q_{IV}): the energy is transferred from negative voltage load to source

The first quadrant is called the forward motoring (Forw. Mot.) operation. V_1 and V_2 are positive, and I_1 and I_2 are positive as well. The second quadrant is called the forward regenerative (Forw. Reg.) braking operation. V_1 and V_2 are positive, and I_1 and I_2 are negative. The third quadrant is called the reverse motoring (Rev. Mot.) operation. V_1 and I_1 are positive, and V_2 and I_2 are negative. The fourth quadrant is called the reverse regenerative (Rev. Reg.) braking operation. V_1 and I_2 are positive, and I_1 and V_2 are negative. Each mode has two states: *on* and *off*. Usually, each state is operating in different conduction duty k . The switching period is T where $T = 1 / f$. The switch status is shown in [Table 8.11](#).

Mode A operation is shown in [Figure 8.14a](#) (switch on) and b (switch off). During switch-**on** state, switch S_1 is closed. In this case the source voltage V_1 supplies the load V_2 and inductor L , inductor current i_L increases. During switch-**off** state, diode D_2 is on. In this case current i_L flows through the load V_2 via the free-wheeling diode D_2 , and it decreases.

Mode B operation is shown in [Figure 8.15 a](#) (switch on) and b (switch off). During switch-**on** state, switch S_2 is closed. In this case the load voltage V_2 supplies the inductor L , inductor current i_L increases. During switch-**off** state, diode D_1 is on, current i_L flows through the source V_1 and load V_2 via the diode D_1 , and it decreases.

Mode C operation is shown in [Figure 8.16 a](#) (switch on) and b (switch off). During switch-**on** state, switch S_1 is closed. The source voltage V_1 supplies the inductor L , inductor current i_L increases. During switch-**off** state, diode D_2 is on. Current i_L flows through the load V_2 via the free-wheeling diode D_2 , and it decreases.

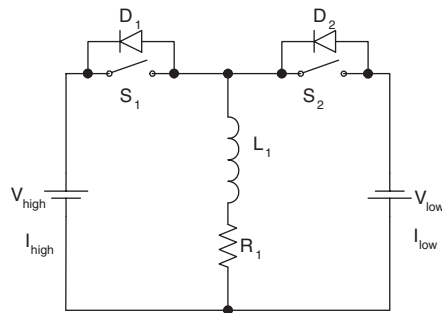
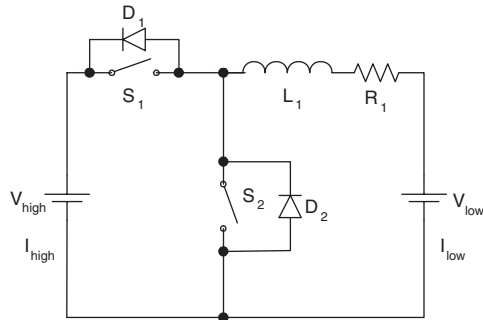
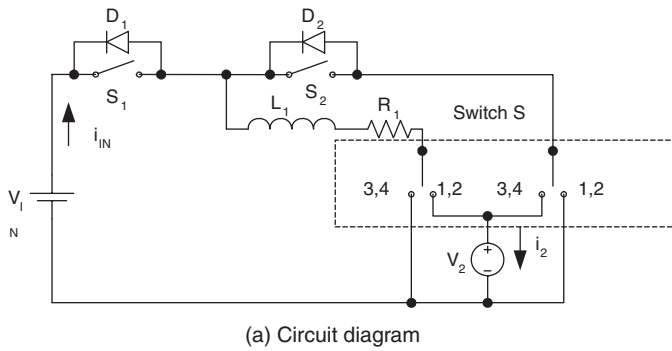


FIGURE 8.13

Four-quadrant switched-inductor DC/DC Luo-converters.

Mode D operation is shown in [Figure 8.17 a](#) (switch on) and [b](#) (switch off). During switch-on state, switch S_2 is closed. The load voltage V_2 supplies the inductor L , inductor current i_L increases. During switch-off state, diode D_1 is on. Current i_L flows through the source V_1 via the diode D_1 , and it decreases.

TABLE 8.11

Switch Status

Q No.	State	S ₁	D ₁	S ₂	D ₂	S ₃	Source	Load
Q _I , Mode A	on	ON				ON 1/2	V ₁ +	V ₂ +
Forw. Mot.	off				ON	ON 1/2	I ₁ +	I ₂ +
Q _{II} , Mode B	on			ON		ON 1/2	V ₁ +	V ₂ +
Forw. Reg.	off		ON			ON 1/2	I ₁ -	I ₂ -
Q _{III} , Mode C	on	ON				ON 3/4	V ₁ +	V ₂ -
Rev. Mot.	off				ON	ON 3/4	I ₁ +	I ₂ -
Q _{IV} , Mode D	on			ON		ON 3/4	V ₁ +	V ₂ -
Rev. Reg.	off		ON			ON 3/4	I ₁ -	I ₂ +

Note: Omitted switches are off.

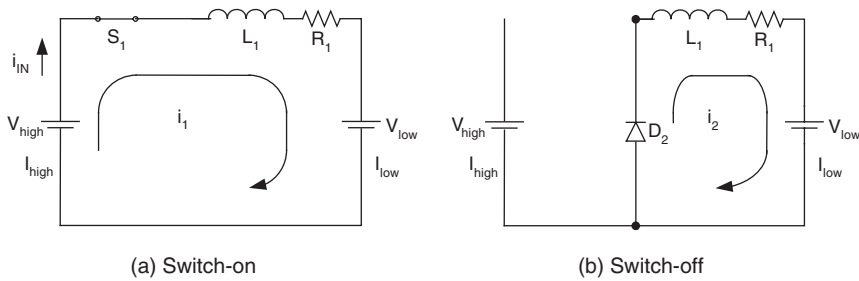


FIGURE 8.14
Mode A (quadrant I) operation.

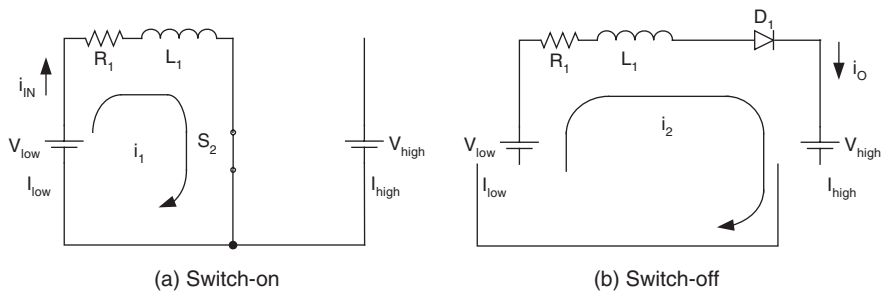


FIGURE 8.15
Mode B (quadrant II) operation.

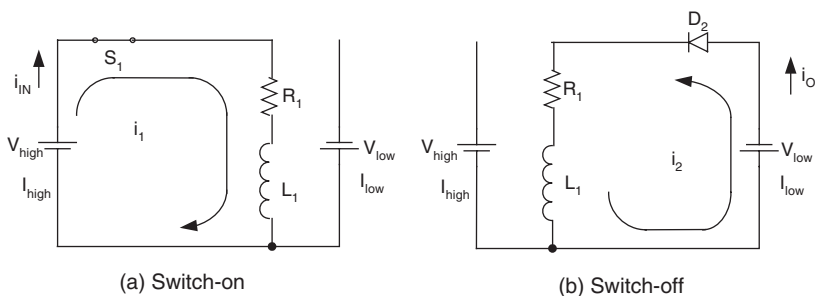


FIGURE 8.16
Mode C (quadrant III) operation.

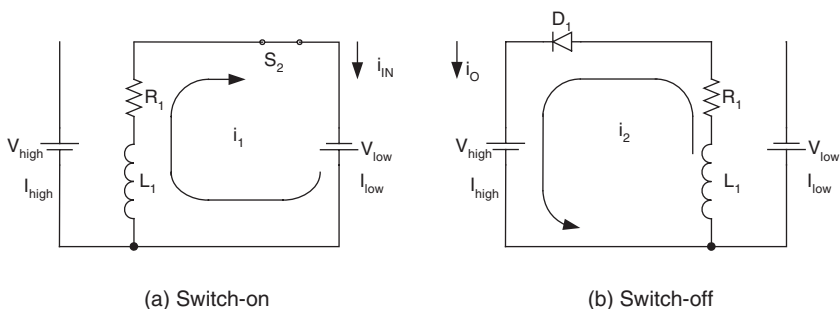


FIGURE 8.17
Mode D (quadrant IV) operation.

8.4.1 Mode A (Q_1 : Forward Motoring)

8.4.1.1 Continuous Mode

Refer to [Figure 8.14a](#) and suppose that $V_1 = +42$ V and $V_2 = +14$ V, $L = 0.3$ mH and the parasitic resistance $R = 3$ m Ω

$$v_L(t) = \begin{cases} V_1 - V_2 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < T \end{cases} \quad (8.62)$$

$$i_L(t) = \begin{cases} i_L(0) + \frac{V_1 - V_2 - RI_L}{L} t & 0 \leq t < kT \\ i_L(kT) - \frac{V_2 + RI_L}{L} (t - kT) & kT \leq t < T \end{cases} \quad (8.63)$$

where

$$i_L(0) = I_L - \Delta i_L / 2 \quad (8.64)$$

$$i_L(kT) = I_L + \Delta i_L / 2 \quad (8.65)$$

From Equations (8.62) and (8.63) the average inductor current is

$$I_L = \frac{kV_1 - V_2}{R} \quad (8.66)$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1-k)V_1}{fL} \quad (8.67)$$

The variation ratio is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2} \frac{R}{2fL} \quad (8.68)$$

Substituting Equations (8.66) and (8.67) into Equations (8.64) and (8.65), we have

$$i_L(0) = \frac{kV_1 - V_2}{R} - \frac{k(1-k)V_1}{2fL} \quad (8.69)$$

and

$$i_L(kT) = \frac{kV_1 - V_2}{R} + \frac{k(1-k)V_1}{2fL} \quad (8.70)$$

The average input current is

$$I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt \approx k \frac{kV_1 - V_2}{R} \quad (8.71)$$

The average output current is

$$I_O = \frac{1}{T} \int_0^T i_L(t) dt \approx \frac{kV_1 - V_2}{R} \quad (8.72)$$

Input power is

$$P_I = V_1 I_I = kV_1 \frac{kV_1 - V_2}{R} \quad (8.73)$$

Output power is

$$P_O = V_2 I_O = V_2 \frac{kV_1 - V_2}{R} \quad (8.74)$$

The transfer efficiency is

$$\eta_A = \frac{P_O}{P_I} = \frac{V_2}{kV_1} \quad (8.75)$$

The transfer efficiency only relies on conduction duty k , the source and load voltages. It is independent of R , L , and f .

If $f = 1$ kHz, $L = 300$ μ H, $R = 3$ m Ω , $k = 0.35$, $V_1 = 42$ V and $V_2 = 14$ V, we find that

$$I_L = 233 \text{ A}, \quad \Delta i_L = 31.85 \text{ A} \quad \zeta = 6.83\% \quad I_I = I_1 = 81.6 \text{ A}, \quad I_O = I_2 = 233 \text{ A},$$

$$P_O = 32,672 \text{ W} \quad P_I = 3427 \text{ W} \quad \eta_A = 95\%$$

8.4.1.2 Discontinuous Mode

From Equation (8.68), when $\zeta \geq 1$ the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined:

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2} \frac{R}{2fL} \geq 1$$

i.e.,

$$\frac{k(1-k)V_1}{kV_1 - V_2} \frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_2}{V_1} + k(1-k) \frac{R}{2fL} \quad (8.76)$$

From Equation (8.76) the discontinuous conduction region is caused by the following factors:

- Switching frequency f is too low
- Duty cycle k is too small

- Inductance L is too small
- Load resistor R is too big

The whole conduction period is smaller than T . Assuming the conduction period is in the region between 0 and t_1 that is smaller than T . The filling coefficient m_A is defined as

$$m_A = \frac{t_1 - kT}{(1 - k)T} \quad kT < t_1 \leq T \quad (8.77)$$

The voltage and current across inductor L are

$$v_L(t) = \begin{cases} V_1 - V_2 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < t_1 \\ 0 & t_1 \leq t < T \end{cases} \quad (8.78)$$

$$i_L(t) = \begin{cases} \frac{V_1 - V_2 - RI_L}{L} t & 0 \leq t < kT \\ \frac{V_1}{L} kT - \frac{V_2 + RI_L}{L} t & kT \leq t < t_1 \\ 0 & t_1 \leq t < T \end{cases} \quad (8.79)$$

because

$$i_L(0) = 0$$

$$i_L(kT) = \frac{V_1 - V_2 - RI_L}{L} kT$$

$i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L . From Equation (8.79) when $t = t_1$, $i_L(t_1) = 0$. Therefore, we have the following relation:

$$i_L(t_1) = \frac{V_1}{L} kT - \frac{V_2 + RI_L}{L} t_1 = 0$$

Therefore,

$$t_1 = \frac{V_1}{V_2 + RI_L} kT \quad (8.80)$$

Considering Equation (8.76),

$$kT < t_1 < T$$

Since R is usually small, we can get

$$t_1 \approx \frac{V_1}{V_2} kT$$

The average inductor current is

$$I_L = \frac{1}{T} \int_0^{t_1} i_L(t) dt = \frac{t_1}{2T} i_L(kT_s) = \frac{V_1}{V_2 + RI_L} \frac{V_1 - V_2 - RI_L}{2fL} k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1}{V_2} \frac{V_1 - V_2}{2fL} k^2$$

The average input current is

$$I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt = \frac{i_L(kT)}{2T} kT = \frac{V_1 - V_2 - RI_L}{2fL} k^2$$

The average output current is

$$I_O = \frac{1}{T} \int_0^{t_1} i_L(t) dt = \frac{i_L(kT)}{2T} t_1 = \frac{V_1 - V_2 - RI_L}{2fL} \frac{V_1}{V_2 + RI_L} k^2$$

Input power is

$$P_I = V_1 I_I = V_1 \frac{V_1 - V_2 - RI_L}{2fL} k^2$$

Output power is

$$P_O = V_2 I_O = V_2 \frac{V_1 - V_2 - RI_L}{2fL} \frac{V_1}{V_2 + RI_L} k^2$$

The transfer efficiency is

$$\eta_{A-dis} = \frac{P_O}{P_I} = \frac{V_2}{V_2 + RI_L} \quad (8.81)$$

with

$$k \leq \frac{V_2}{V_1} + k(1-k) \frac{R}{2fL}$$

8.4.2 Mode B (Q_{II} : Forward Regenerative Braking)

8.4.2.1 Continuous Mode

Refer to [Figure 8.15a](#), and suppose that $V_1 = +42$ V and $V_2 = +14$ V, $L = 0.3$ mH and the parasitic resistance $R = 3$ m Ω

$$v_L(t) = \begin{cases} V_2 - RI_L & 0 \leq t < kT \\ -(V_1 - V_2 + RI_L) & kT \leq t < T \end{cases} \quad (8.82)$$

$$i_L(t) = \begin{cases} i_L(0) + \frac{V_2 - RI_L}{L} t & 0 \leq t < kT \\ i_L(kT) - \frac{V_1 - V_2 + RI_L}{L} (t - kT) & kT \leq t < T \end{cases} \quad (8.83)$$

Where

$$i_L(0) = I_L - \Delta i_L / 2 \quad (8.84)$$

$$i_L(kT) = I_L + \Delta i_L / 2 \quad (8.85)$$

Since the inductor average voltage is zero, we have

$$k(V_2 - RI_L) = (1-k)(V_1 - V_2 + RI_L)$$

then:

$$I_L = \frac{V_2 - (1-k)V_1}{R} \quad (8.86)$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1-k)V_1}{fL} \quad (8.87)$$

The variation ratio is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{V_2 - (1-k)V_1} \frac{R}{2fL} \quad (8.88)$$

Substituting Equations (8.86) and (8.87) into Equations (8.84) and (8.85),

$$i_L(0) = \frac{V_2 - (1-k)V_1}{R} - \frac{k(1-k)V_1}{2fL} \quad (8.89)$$

and

$$i_L(kT) = \frac{V_2 - (1-k)V_1}{R} + \frac{k(1-k)V_1}{2fL} \quad (8.90)$$

The average input current is

$$I_I = \frac{1}{T} \int_0^T i_L(t) dt = \frac{V_2 - (1-k)V_1}{R} \quad (8.91)$$

The average output current is

$$I_O = \frac{1}{T} \int_{kT}^T i_L(t) dt = (1-k) \frac{V_2 - (1-k)V_1}{R} \quad (8.92)$$

Input power is

$$P_I = V_2 I_I = V_2 \frac{V_2 - (1-k)V_1}{R} \quad (8.93)$$

Output power is

$$P_O = V_1 I_O = (1-k)V_1 \frac{V_2 - (1-k)V_1}{R} \quad (8.94)$$

The transfer efficiency is

$$\eta_B = \frac{P_O}{P_I} = \frac{(1-k)V_1}{V_2} \quad (8.95)$$

The transfer efficiency only relies on conduction duty k , the source and load voltages. It is independent of R , L , and f .

8.4.2.2 Discontinuous Mode

From Equation (8.88), when $\zeta \geq 1$ the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined as:

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{V_2 - (1-k)V_1} \frac{R}{2fL} \geq 1$$

i.e.,

$$\frac{k(1-k)V_1}{V_2 - (1-k)V_1} \frac{R}{2fL} \geq 1$$

or

$$k \leq \left(1 - \frac{V_2}{V_1}\right) + k(1-k) \frac{R}{2fL} \quad (8.96)$$

The whole conduction period is smaller than T . Assume that the conduction period is in the region between 0 and t_2 that is smaller than T . The filling coefficient m_B is defined as

$$m_B = \frac{t_2 - kT}{(1-k)T} \quad kT < t_2 \leq T \quad (8.97)$$

The voltage and current across inductor L are

$$v_L(t) = \begin{cases} V_2 - RI_L & 0 \leq t < kT \\ -(V_1 - V_2 + RI_L) & kT \leq t < t_2 \\ 0 & t_2 \leq t < T \end{cases} \quad (8.98)$$

$$i_L(t) = \begin{cases} \frac{V_2 - RI_L}{L} t & 0 \leq t < kT \\ \frac{V_1}{L} kT - \frac{V_1 - V_2 + RI_L}{L} t & kT \leq t < t_2 \\ 0 & t_2 \leq t < T \end{cases} \quad (8.99)$$

because

$$i_L(0) = 0$$

$$i_L(kT) = \frac{V_2 - RI_L}{L} kT$$

$i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L . From Equation (8.99) when $t = t_2$, $i_L(t_2) = 0$. Therefore, we have the following relation:

$$i_L(t_2) = \frac{V_1}{L} kT - \frac{V_1 - V_2 + RI_L}{L} t_2 = 0$$

Therefore,

$$t_2 = \frac{V_1}{V_1 - V_2 + RI_L} kT \quad (8.100)$$

Considering Equation (8.86),

$$kT < t_2 < T$$

Since R is usually small,

$$t_2 \approx \frac{V_1}{V_1 - V_2} kT$$

The average inductor current is

$$I_L = \frac{1}{T} \int_0^t i_L(t) dt = \frac{t_2}{2T} i_L(kT) = \frac{V_1}{V_1 - V_2 + RI_L} \frac{V_2 - RI_L}{2fL} k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1}{V_1 - V_2} \frac{V_2}{2fL} k^2$$

The average input current is

$$I_I = \frac{1}{T} \int_0^t i_L(t) dt = \frac{i_L(kT)}{2T} t_2 = \frac{V_1}{V_1 - V_2 + RI_L} \frac{V_2 - RI_L}{2fL} k^2$$

The average output current is

$$I_O = \frac{1}{T} \int_{kT}^{t_2} i_L(t) dt = \frac{i_L(kT)}{2T} (t_2 - kT) = \frac{1}{2fL} \frac{(V_2 - RI_L)^2}{V_1 - V_2 + RI_L} k^2$$

Input power is

$$P_I = V_2 I_I = V_2 \frac{V_1}{V_1 - V_2 + RI_L} \frac{V_2 - RI_L}{2fL} k^2$$

Output power is

$$P_O = V_1 I_O = V_1 \frac{V_2 - RI_L}{2fL} \frac{V_2 - RI_L}{V_1 - V_2 + RI_L} k^2$$

The transfer efficiency is

$$\eta_{B-dis} = \frac{P_O}{P_I} = \frac{V_2 - RI_L}{V_2} \quad (8.101)$$

with

$$k \leq (1 - \frac{V_2}{V_1}) + k(1 - k) \frac{R}{2fL}$$

8.4.3 Mode C (Q_{III} : Reverse Motoring)

8.4.3.1 Continuous Mode

Refer to [Figure 8.16a](#) and suppose that $V_1 = +42$ V and $V_2 = -14$ V, $L = 0.3$ mH and the parasitic resistance $R = 3$ m Ω

$$v_L(t) = \begin{cases} V_1 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < T \end{cases} \quad (8.102)$$

$$i_L(t) = \begin{cases} i_L(0) + \frac{V_1 - RI_L}{L} t & 0 \leq t < kT \\ i_L(kT) - \frac{V_2 + RI_L}{L} (t - kT) & kT \leq t < T \end{cases} \quad (8.103)$$

where

$$i_L(0) = I_L - \Delta i_L / 2 \quad (8.104)$$

$$i_L(kT) = I_L + \Delta i_L / 2 \quad (8.105)$$

Since the inductor average voltage is zero,

$$k(V_1 - RI_L) = (1 - k)(V_2 + RI_L)$$

$$I_L = \frac{kV_1 - (1 - k)V_2}{R} \quad (8.106)$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1 - k)(V_1 + V_2)}{fL} \quad (8.107)$$

The variation ratio is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1 - k)(V_1 + V_2)}{kV_1 - (1 - k)V_2} \frac{R}{2fL} \quad (8.108)$$

Substituting Equations (8.106) and (8.107) into Equations (8.104) and (8.105), we have

$$i_L(0) = \frac{kV_1 - (1 - k)V_2}{R} - \frac{k(1 - k)(V_1 + V_2)}{2fL} \quad (8.109)$$

and

$$i_L(kT) = \frac{kV_1 - (1 - k)V_2}{R} + \frac{k(1 - k)(V_1 + V_2)}{2fL} \quad (8.110)$$

The average input current is

$$I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt = k \frac{kV_1 - (1 - k)V_2}{R} \quad (8.111)$$

The average output current is

$$I_O = \frac{1}{T} \int_{kT}^T i_L(t) dt = (1 - k) \frac{kV_1 - (1 - k)V_2}{R} \quad (8.112)$$

Input power is

$$P_I = V_1 I_I = k V_1 \frac{k V_1 - (1-k) V_2}{R} \quad (8.113)$$

Output power is

$$P_O = V_2 I_O = (1-k) V_2 \frac{k V_1 - (1-k) V_2}{R} \quad (8.114)$$

The transfer efficiency is

$$\eta_c = \frac{P_O}{P_I} = \frac{(1-k) V_2}{k V_1} \quad (8.115)$$

The transfer efficiency only relies on conduction duty k , the source and load voltages. It is independent of R , L , and f .

8.4.3.2 *Discontinuous Mode*

From Equation (8.108), when $\zeta \geq 1$ the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined:

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)(V_1 + V_2)}{k V_1 - (1-k) V_2} \frac{R}{2fL} \geq 1$$

i.e.,

$$\frac{k(1-k)(V_1 + V_2)}{k V_1 - (1-k) V_2} \frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_2}{V_1 + V_2} + k(1-k) \frac{R}{2fL} \quad (8.116)$$

The whole conduction period is smaller than T . Assuming that the conduction period is in the region between 0 and t_3 . The filling coefficient m_c is defined as

$$m_c = \frac{t_3 - kT}{(1-k)T} \quad kT < t_3 \leq T \quad (8.117)$$

The voltage and current across inductor L are

$$v_L(t) = \begin{cases} V_1 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < t_3 \\ 0 & t_3 \leq t < T \end{cases} \quad (8.118)$$

$$i_L(t) = \begin{cases} \frac{V_1 - RI_L}{L} t & 0 \leq t < kT \\ \frac{V_1 + V_2}{L} kT - \frac{V_2 + RI_L}{L} t & kT \leq t < t_3 \\ 0 & t_3 \leq t < T \end{cases} \quad (8.119)$$

because

$$i_L(0) = 0$$

$$i_L(kT) = \frac{V_1 - RI_L}{L} kT$$

$i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L . From Equation (8.119) when $t = t_3$, $i_L(t_3) = 0$. Therefore, we have the following relation:

$$i_L(t_3) = \frac{V_1 + V_2}{L} kT - \frac{V_2 + RI_L}{L} t_3 = 0$$

Therefore,

$$t_3 = \frac{V_1 + V_2}{V_2 + RI_L} kT \quad (8.120)$$

Considering Equation (8.80),

$$kT < t_3 < T$$

Since R is usually small,

$$t_3 \approx \frac{V_1 + V_2}{V_2} kT$$

The average inductor current is

$$I_L = \frac{1}{T} \int_0^{t_3} i_L(t) dt = \frac{t_3}{2T} i_L(kT) = \frac{V_1 + V_2}{V_2 + RI_L} \frac{V_1 - RI_L}{2fL} k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1 + V_2}{V_2} \frac{V_1}{2fL} k^2$$

The average input current is

$$I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt = \frac{i_L(kT)}{2T} kT = \frac{V_1 - RI_L}{2fL} k^2$$

The average output current is

$$I_O = \frac{1}{T} \int_{kT}^{t_3} i_L(t) dt = \frac{i_L(kT)}{2T} (t_3 - kT) = \frac{(V_1 - RI_L)^2}{2fL(V_2 + RI_L)} k^2$$

Input power is

$$P_I = V_1 I_I = V_1 \frac{V_1 - RI_L}{2fL} k^2$$

Output power is

$$P_O = V_2 I_O = V_2 \frac{(V_1 - RI_L)^2}{2fL(V_2 + RI_L)} k^2$$

The transfer efficiency is

$$\eta_{C-dis} = \frac{P_O}{P_I} = \frac{V_2}{V_1} \frac{V_1 - RI_L}{V_2 + RI_L}$$

with

$$k \leq \frac{V_2}{V_1 + V_2} + k(1 - k) \frac{R}{2fL} \quad (8.121)$$

8.4.4 Mode D (Q_{IV} : Reverse Regenerative Braking)

8.4.4.1 Continuous Mode

Refer to Figure 8.17a and suppose that $V_1 = +42$ V and $V_2 = -14$ V, $L = 0.3$ mH and the parasitic resistance $R = 3$ m Ω

$$v_L(t) = \begin{cases} V_2 - RI_L & 0 \leq t < kT \\ -(V_1 + RI_L) & kT \leq t < T \end{cases} \quad (8.122)$$

$$i_L(t) = \begin{cases} i_L(0) + \frac{V_2 - RI_L}{L} t & 0 \leq t < kT \\ i_L(kT) - \frac{V_1 + RI_L}{L} (t - kT) & kT \leq t < T \end{cases} \quad (8.123)$$

Where

$$i_L(0) = I_L - \Delta i_L / 2 \quad (8.124)$$

$$i_L(kT) = I_L + \Delta i_L / 2 \quad (8.125)$$

Since the inductor average voltage is zero we have

$$k(V_2 - RI_L) = (1 - k)(V_1 + RI_L)$$

then:

$$I_L = \frac{kV_2 - (1 - k)V_1}{R} \quad (8.126)$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1 - k)(V_1 + V_2)}{fL} \quad (8.127)$$

The variation ratio is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1 - k)(V_1 + V_2)}{kV_2 - (1 - k)V_1} \frac{R}{2fL} \quad (8.128)$$

Substituting Equations (8.126) and (8.127) into Equations (8.124) and (8.125),

$$i_L(0) = \frac{kV_2 - (1-k)V_1}{R} - \frac{k(1-k)(V_1 + V_2)}{2fL} \quad (8.129)$$

and

$$i_L(kT) = \frac{kV_2 - (1-k)V_1}{R} + \frac{k(1-k)(V_1 + V_2)}{2fL} \quad (8.130)$$

The average input current is

$$I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt = k \frac{kV_2 - (1-k)V_1}{R} \quad (8.131)$$

The average output current is

$$I_O = \frac{1}{T} \int_{kT}^T i_L(t) dt = (1-k) \frac{kV_2 - (1-k)V_1}{R} \quad (8.132)$$

Input power is

$$P_I = V_2 I_I = kV_2 \frac{kV_2 - (1-k)V_1}{R} \quad (8.133)$$

Output power is

$$P_O = V_1 I_O = (1-k)V_1 \frac{kV_2 - (1-k)V_1}{R} \quad (8.134)$$

The transfer efficiency is

$$\eta_D = \frac{P_O}{P_I} = \frac{(1-k)V_1}{kV_2} \quad (8.135)$$

The transfer efficiency only relies on conduction duty k , the source and load voltages. It is independent of R , L , and f .

8.4.4.2 Discontinuous Mode

From Equation (8.118), when $\zeta \geq 1$ the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined:

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)(V_1 + V_2)}{kV_2 - (1-k)V_1} \frac{R}{2fL} \geq 1$$

i.e.,

$$\frac{k(1-k)(V_1 + V_2)}{kV_2 - (1-k)V_1} \frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_1}{V_1 + V_2} + k(1-k) \frac{R}{2fL} \quad (8.136)$$

The whole conduction period is smaller than T . Assuming that the conduction period is in the region between 0 and t_4 , the filling coefficient m_D is defined as

$$m_D = \frac{t_4 - kT}{(1-k)T} \quad kT < t_4 \leq T \quad (8.137)$$

The voltage and current across inductor L are

$$v_L(t) = \begin{cases} V_2 - RI_L & 0 \leq t < kT \\ -(V_1 + RI_L) & kT \leq t < t_4 \\ 0 & t_4 \leq t < T \end{cases} \quad (8.138)$$

$$i_L(t) = \begin{cases} \frac{V_2 - RI_L}{L} t & 0 \leq t < kT \\ \frac{V_1 + V_2}{L} kT - \frac{V_1 + RI_L}{L} t & kT \leq t < t_4 \\ 0 & t_4 \leq t < T \end{cases} \quad (8.139)$$

because

$$i_L(0) = 0$$

$$i_L(kT) = \frac{V_2 - RI_L}{L} kT$$

$i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L . From Equation (8.139) when $t = t_4$, $i_L(t_4) = 0$. Therefore, we have the following relation:

$$i_L(t_4) = \frac{V_1 + V_2}{L} kT - \frac{V_1 + RI_L}{L} t_4 = 0$$

Therefore,

$$t_4 = \frac{V_1 + V_2}{V_1 + RI_L} kT \quad (8.140)$$

Considering Equation (8.136),

$$kT < t_4 < T$$

Since R is usually small, we can get

$$t_4 \approx \frac{V_1 + V_2}{V_1} kT$$

The average inductor current is

$$I_L = \frac{1}{T} \int_0^{t_4} i_L(t) dt = \frac{t_4}{2T} i_L(kT) = \frac{V_1 + V_2}{V_1 + RI_L} \frac{V_2 - RI_L}{2fL} k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1 + V_2}{V_1} \frac{V_2}{2fL} k^2$$

The average input current is

$$I_I = \frac{1}{T} \int_0^{kT} i_L(t) dt = \frac{i_L(kT)}{2T} kT = \frac{V_2 - RI_L}{2fL} k^2$$

The average output current is

$$I_O = \frac{1}{T} \int_{kT}^{t_4} i_L(t) dt = \frac{i_L(kT)}{2T} (t_4 - kT) = \frac{1}{2fL} \frac{(V_2 - RI_L)^2}{V_1 + RI_L} k^2$$

Input power is

$$P_I = V_2 I_I = V_2 \frac{V_2 - RI_L}{2fL} k^2$$

Output power is

$$P_O = V_1 I_O = V_1 \frac{1}{2fL} \frac{(V_2 - RI_L)^2}{V_1 + RI_L} k^2$$

The transfer efficiency is

$$\eta_{D-dis} = \frac{P_O}{P_I} = \frac{V_1}{V_2} \frac{V_2 - RI_L}{V_1 + RI_L} \quad (8.141)$$

with

$$k \leq \frac{V_1}{V_1 + V_2} + k(1 - k) \frac{R}{2fL}$$

8.4.5 Experimental Results

A testing rig of a battery 14 VDC as a load and a source 42 VDC as the power supply was tested. The testing conditions were $f = 1$ to 5 kHz, $V_H = 42$ V and $V_L = -14$ V, $L = 0.3$ mH, $R = 3$ m Ω , Volume = 2750(in³). The experimental results show that the total average PD is 28.8 W/in³. This figure is much higher than the classical converters whose PD is usually less than 5 W/in³. Since the switching frequency is low, the EMI is weak.

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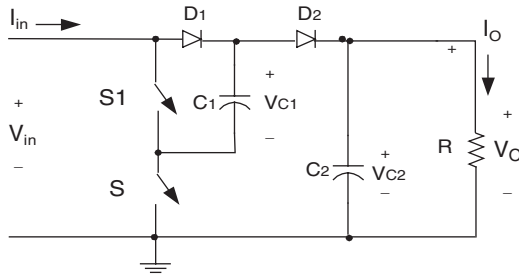
Positive Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters

The micro-power-consumption technique requires high power density DC/DC converters and power supply sources. The voltage lift technique is a popular application in electronic circuit design. Since the switched-capacitor can be integrated into the power integrated circuit (IC) chip, its size is small. Combining the switched-capacitor and voltage lift technique create a DC/DC converter with small size, high power density, high voltage transfer gain, high power efficiency, and low EMI.

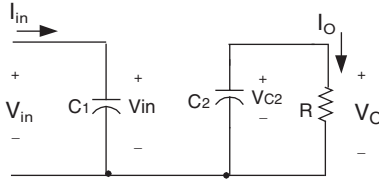
9.1 Introduction

Switched-capacitor (SC) converters can perform in push-pull state with conduction duty cycle $k = 0.5$. This chapter introduces positive output multiple-lift push-pull switched-capacitor DC/DC Luo-converters. These converters can be sorted into several sub-series:

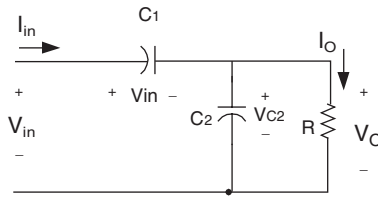
- Main series
- Additional series
- Enhanced series
- Re-enhanced series
- Multiple-enhanced series



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 on)

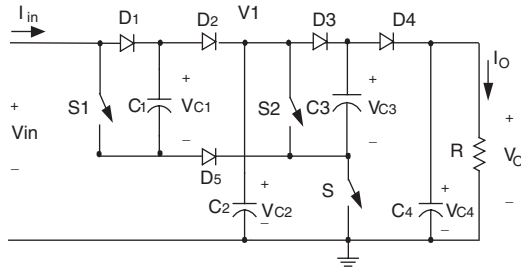
FIGURE 9.1

Elementary circuit of P/O push-pull SC Luo-converter.

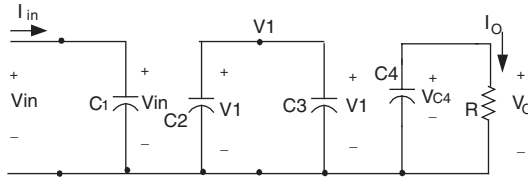
Each circuit has one main switch S and several slave switches as S_i ($i = 1, 2, 3, \dots, n$). The number n is called stage number. The main switch S is on and slaves off during switch-on period kT , and S is off and slaves on during switch-off period $(1 - k)T$. The load is resistive load R . Input voltage and current are V_{in} and I_{in} , output voltage and current are V_O and I_O .

9.2 Main Series

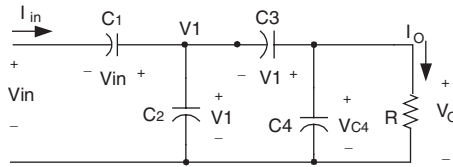
The first three stages of the main series are shown in Figure 9.1 to Figure 9.3. For convenience they are called elementary circuit, re-lift circuit, and triple-lift circuit respectively, and are numbered as $n = 1, 2$ and 3 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 and S_2 on)

FIGURE 9.2

Re-lift push-pull SC circuit.

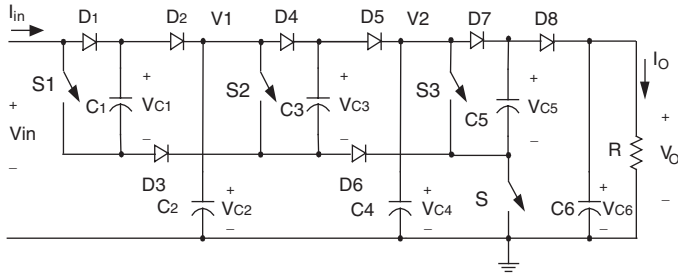
9.2.1 Elementary Circuit

The elementary circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 9.1. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitor C_2 is charged to $V_o = 2V_{in}$ during switch-off. Therefore, the output voltage is

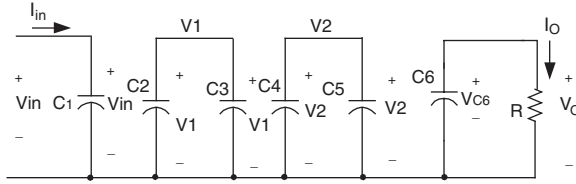
$$V_o = 2V_{in} \quad (9.1)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 . The real output voltage is

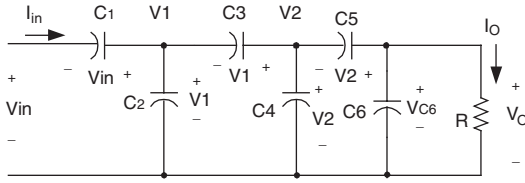
$$V_o = 2V_{in} - \Delta V_1 \quad (9.2)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 and S_3 on)

FIGURE 9.3

Triple-lift push-pull SC circuit.

9.2.2 Re-Lift Circuit

The re-lift circuit is derived from the elementary circuit by adding a parts-set: one slave switch, two switched-capacitors and three diodes (S_2 - C_3 - C_4 - D_3 - D_4 - D_5). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 9.2. The switches S and (S_1 , S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} and voltage across capacitor C_3 is charged to V_1 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$ and voltage across capacitor C_4 is charged to $V_O = 2V_1 - \Delta V_2$ during switch-off. Therefore, the output voltage is

$$V_O = 2V_1 - \Delta V_2 = 4V_{in} - 2\Delta V_1 - \Delta V_2 \quad (9.3)$$

where ΔV_2 is set for the same reason as ΔV_1 .

9.2.3 Triple-Lift Circuit

The triple-lift circuit is derived from re-lift circuit by adding a parts-set: one more slave switch, two switched-capacitors and three diodes (S_3 - C_5 - C_6 - D_6 - D_7 - D_8). Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 9.3](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to v_1 and voltage across capacitor C_5 is charged to v_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_O = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = 2V_2 - \Delta V_3 = 4V_1 - 2\Delta V_2 - \Delta V_3 = 8V_{in} - 4\Delta V_1 - 2\Delta V_2 - \Delta V_3 \quad (9.4)$$

where ΔV_3 is set as same reason as ΔV_1 .

9.2.4 Higher Order Lift Circuit

The higher order lift circuit is designed by just multiple repeating of the parts mentioned in previous sections. The output voltage of the n^{th} -order lift circuit is

$$V_O = 2^n V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-i} \quad (9.5)$$

9.3 Additional Series

The first three stages of the additional series are shown in [Figure 9.4](#) to [Figure 9.6](#). For convenience they are called elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit respectively, and are numbered as $n = 1, 2$, and 3 .

9.3.1 Elementary Additional Circuit

The elementary additional circuit is derived from elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in [Figure 9.4](#). Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

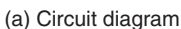


FIGURE 9.4
Elementary additional/enhanced circuit.

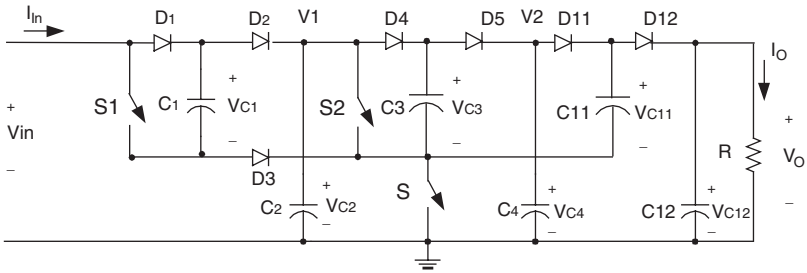
$$V_O = V_1 + V_{in} = 3V_{in} \quad (9.6)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

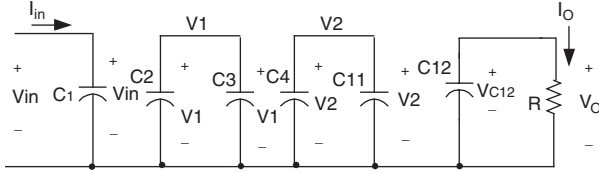
$$V_Q = 3V_{in} - \Delta V_1 - \Delta V_Q \quad (9.7)$$

9.3.2 Re-Lift Additional Circuit

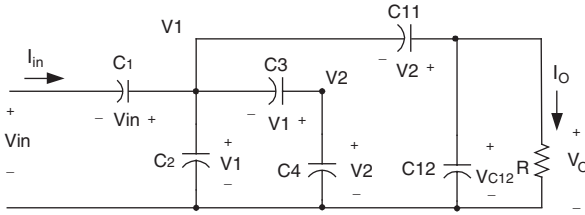
The re-lift additional circuit is derived from re-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 9.5](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 and S_2 on)

FIGURE 9.5

Re-lift additional circuit.

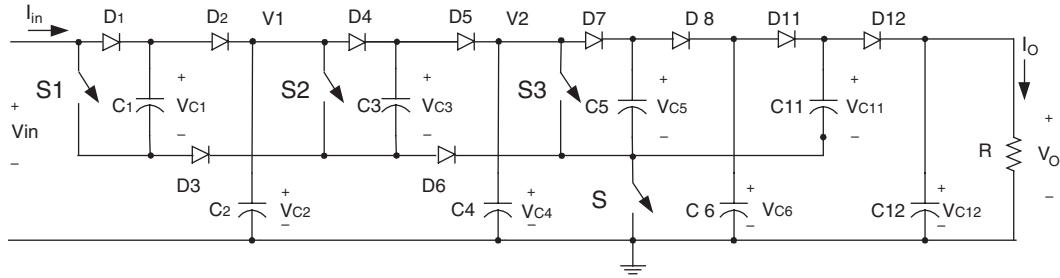
is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (9.8)$$

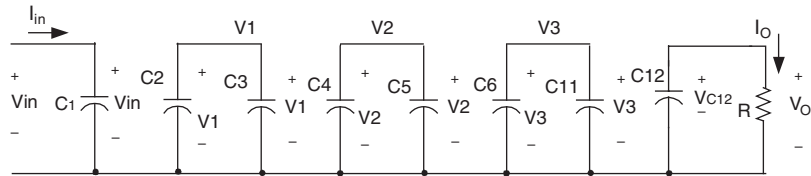
where ΔV_2 is set for the same reason as ΔV_1 .

9.3.3 Triple-Lift Additional Circuit

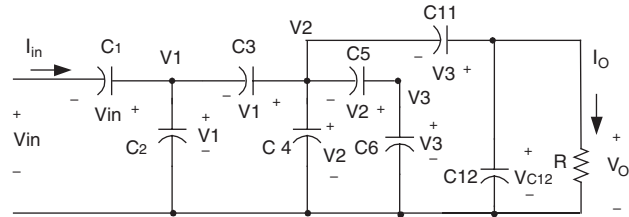
The triple-lift additional circuit is derived from triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and -off



(a) Circuit diagram



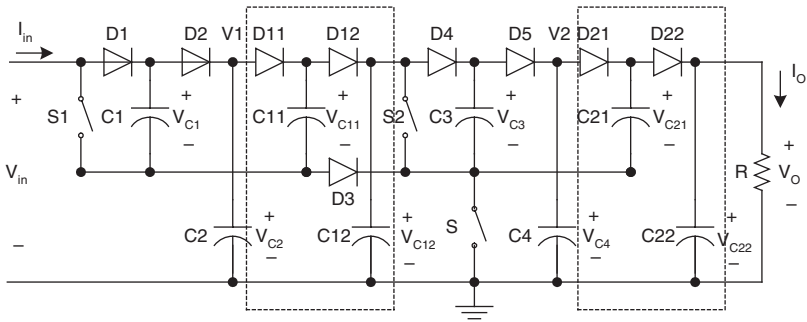
(b) Equivalent circuit during switching-on (S on)



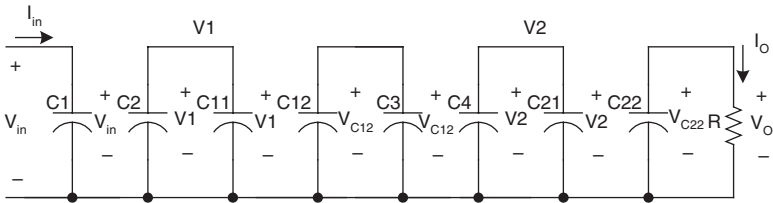
(c) Equivalent circuit during switching-off (S_1 , S_2 and S_3 on)

FIGURE 9.6

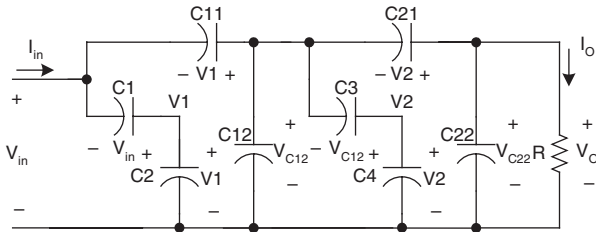
Triple-lift additional circuit.



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 and S_2 on)

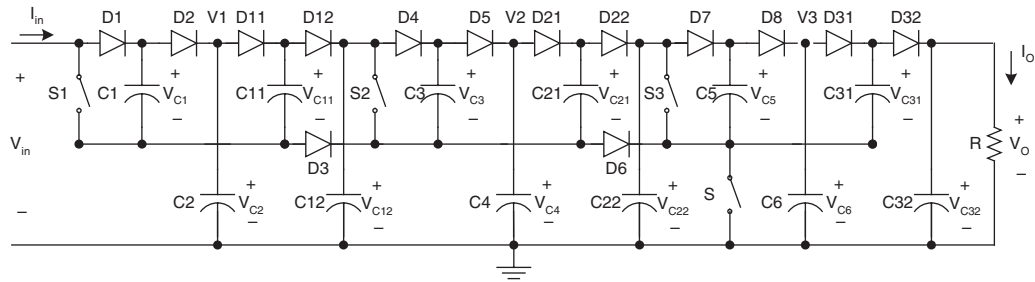
FIGURE 9.7

Re-lift enhanced circuit.

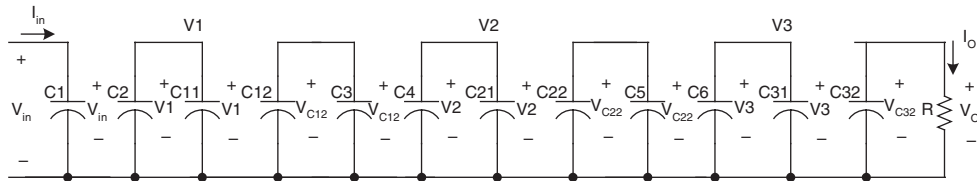
are shown in Figure 9.6. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (9.9)$$

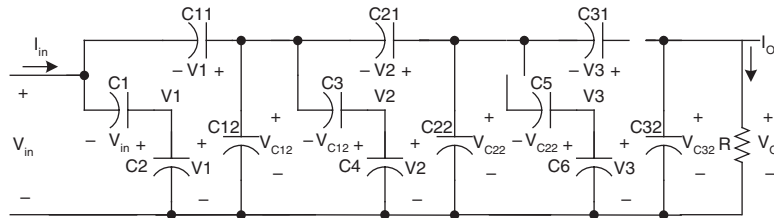
where ΔV_3 is set for the same reason as ΔV_1 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 and S_3 on)

FIGURE 9.8

Triple-lift enhanced circuit.

9.3.4 Higher Order Lift Additional Circuit

Higher order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. The output voltage of n th-lift additional circuit is

$$V_{O-m} = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}) - \Delta V_n - \Delta V_O \quad (9.10)$$

9.4 Enhanced Series

The first three stages of the enhanced series are shown in [Figures 9.4, 9.7, and 9.8](#). For convenience they are called elementary enhanced circuit, re-lift enhanced circuit, and triple-lift enhanced circuit respectively, and are numbered as $n = 1, 2$, and 3 .

9.4.1 Elementary Enhanced Circuit

The elementary enhanced circuit is derived from elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in [Figure 9.4](#). The output voltage is

$$V_O = V_1 + V_{in} = 3V_{in} \quad (9.6)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

$$V_O = 3V_{in} - \Delta V_1 - \Delta V_O \quad (9.7)$$

9.4.2 Re-Lift Enhanced Circuit

The re-lift enhanced circuit is derived from re-lift circuit by adding one DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 9.7](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 9V_{in} - 6\Delta V_1 - 2\Delta V_2 - \Delta V_O \quad (9.11)$$

where ΔV_2 is set for the same reason as ΔV_1 .

9.4.3 Triple-Lift Enhanced Circuit

The triple-lift enhanced circuit is derived from re-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and -off are shown in [Figure 9.8](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O = 27V_{in} - 18\Delta V_1 - 6\Delta V_2 - 2\Delta V_3 - \Delta V_O \quad (9.12)$$

where ΔV_3 is set for the same reason as ΔV_1 .

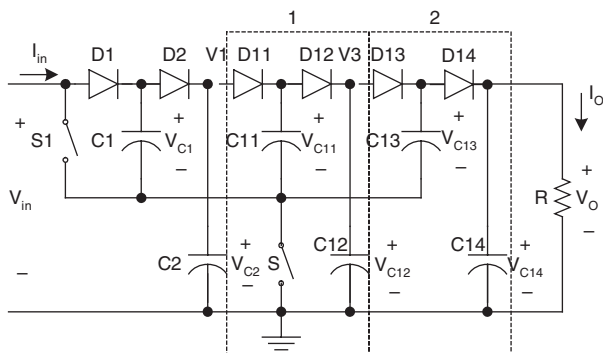
9.4.4 Higher Order Enhanced Lift Circuit

Higher order enhanced lift circuit is derived from the corresponding circuit of the main series circuit by adding the DEC in each stage circuit. The output voltage of the n th-order lift enhanced circuit is

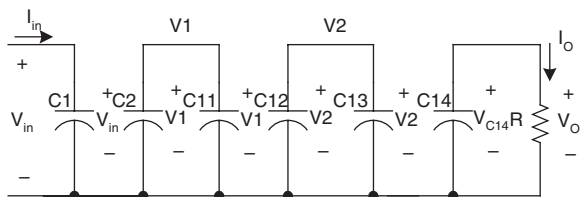
$$V_O = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}) - \Delta V_n - \Delta V_O \quad (9.13)$$

9.5 Re-Enhanced Series

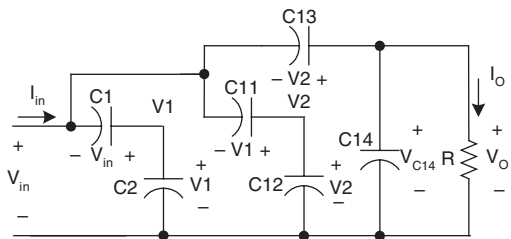
The first three stages of the re-enhanced series are shown in [Figure 9.9](#) to [Figure 9.11](#). For convenience they are called elementary re-enhanced circuit, re-lift re-enhanced circuit, and triple-lift re-enhanced circuit respectively, and are numbered as $n = 1, 2$, and 3 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



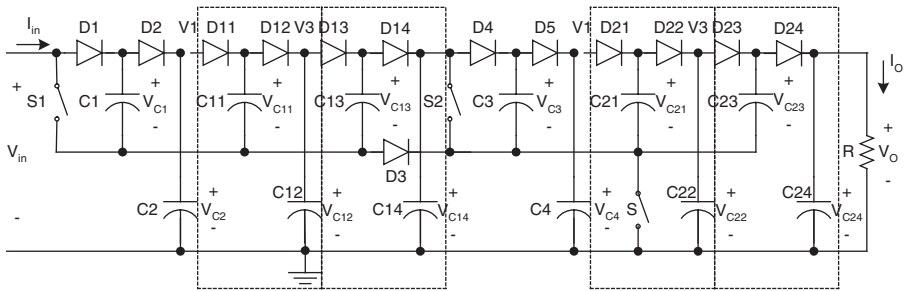
(c) Equivalent circuit during switching-off (S_1 on)

FIGURE 9.9
Elementary re-enhanced circuit.

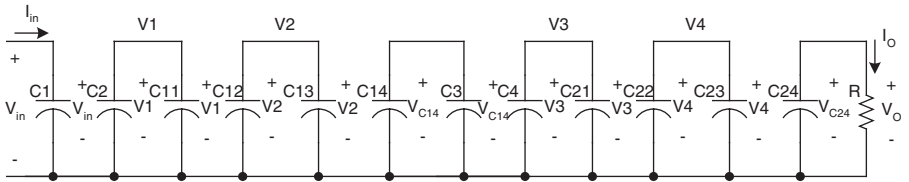
9.5.1 Elementary Re-Enhanced Circuit

The elementary re-enhanced circuit is derived from elementary circuit by adding the DEC twice. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 9.9. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

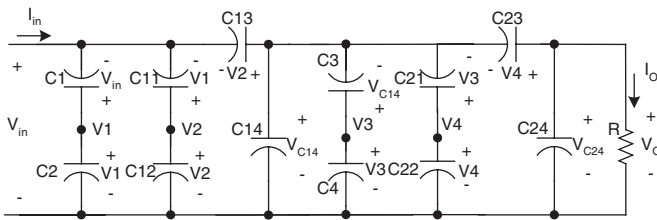
$$V_O = V_1 + V_{in} = 4V_{in} \quad (9.14)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 and S_2 on)

FIGURE 9.10

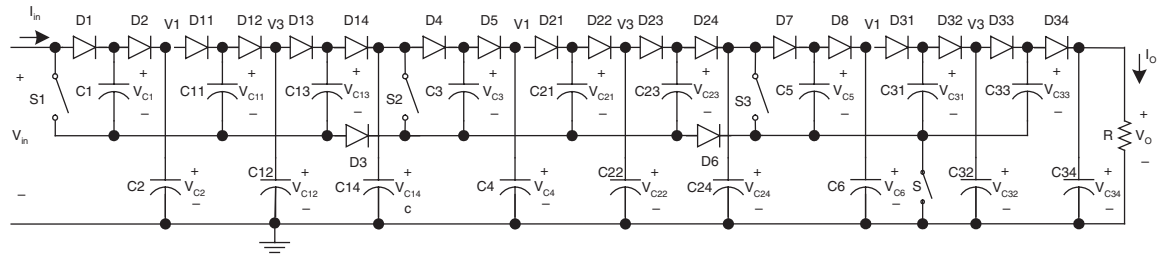
Re-lift re-enhanced circuit.

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

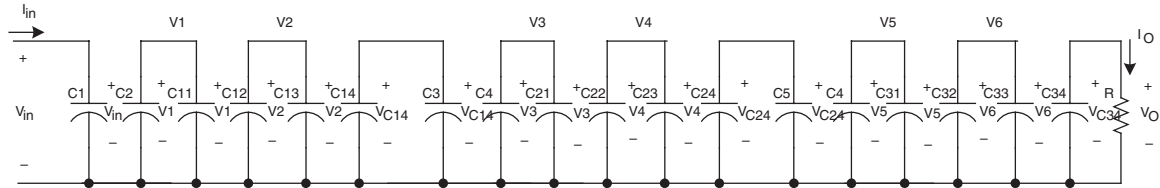
$$V_O = 4V_{in} - \Delta V_1 - \Delta V_O \quad (9.15)$$

9.5.2 Re-Lift Re-Enhanced Circuit

The re-lift re-enhanced circuit is derived from re-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 9.10. The switches S and (S_1 , S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)

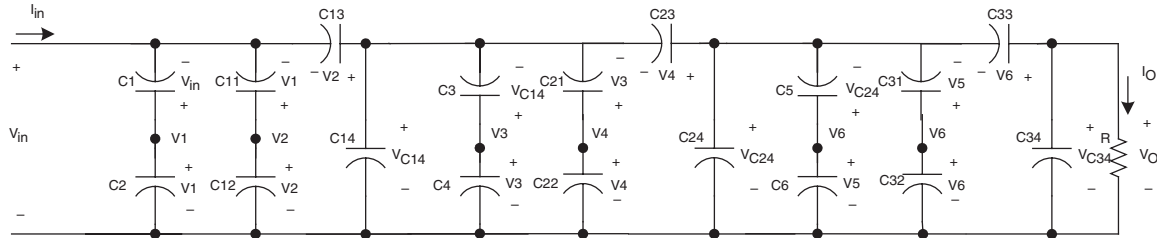

 (c) Equivalent circuit during switching-off (S_1 , S_2 and S_3 on)

FIGURE 9.11
Triple-lift re-enhanced circuit.

C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (9.16)$$

where ΔV_2 is set for the same reason as ΔV_1 .

9.5.3 Triple-Lift Re-Enhanced Circuit

The triple-lift re-enhanced circuit is derived from triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 9.11](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (9.17)$$

where ΔV_3 is set for the same reason as ΔV_1 .

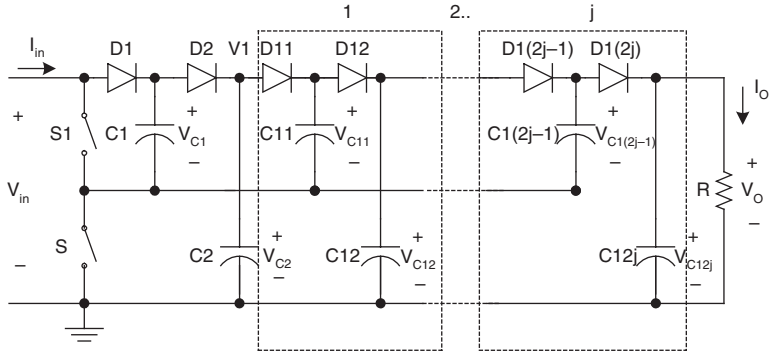
9.5.4 Higher Order Lift Re-Enhanced Circuit

Higher order lift re-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. The output voltage of the n th-lift re-enhanced circuit is

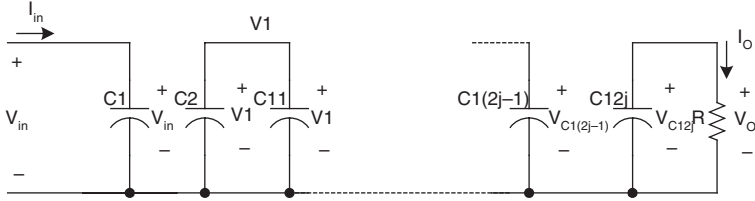
$$V_O = (1.5 \times 2)^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} - \Delta V_m - \Delta V_O \quad (9.18)$$

9.6 Multiple-Enhanced Series

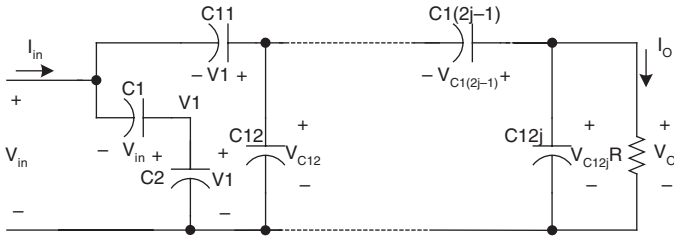
The first three stages of the multiple-enhanced series are shown in [Figure 9.12](#) to [Figure 9.14](#). For convenience they are called elementary multiple-enhanced circuit, re-lift multiple-enhanced circuit, and triple-lift multiple-enhanced circuit respectively, and are numbered as $n = 1, 2$, and 3 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 on)

FIGURE 9.12
Elementary multiple-enhanced circuit.

9.6.1 Elementary Multiple-Enhanced Circuit

The elementary multiple-enhanced circuit is derived from elementary circuit by adding the DEC multiple (j) times. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 9.12. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_O = V_1 + V_{in} = (1 + j)V_{in} \quad (9.19)$$

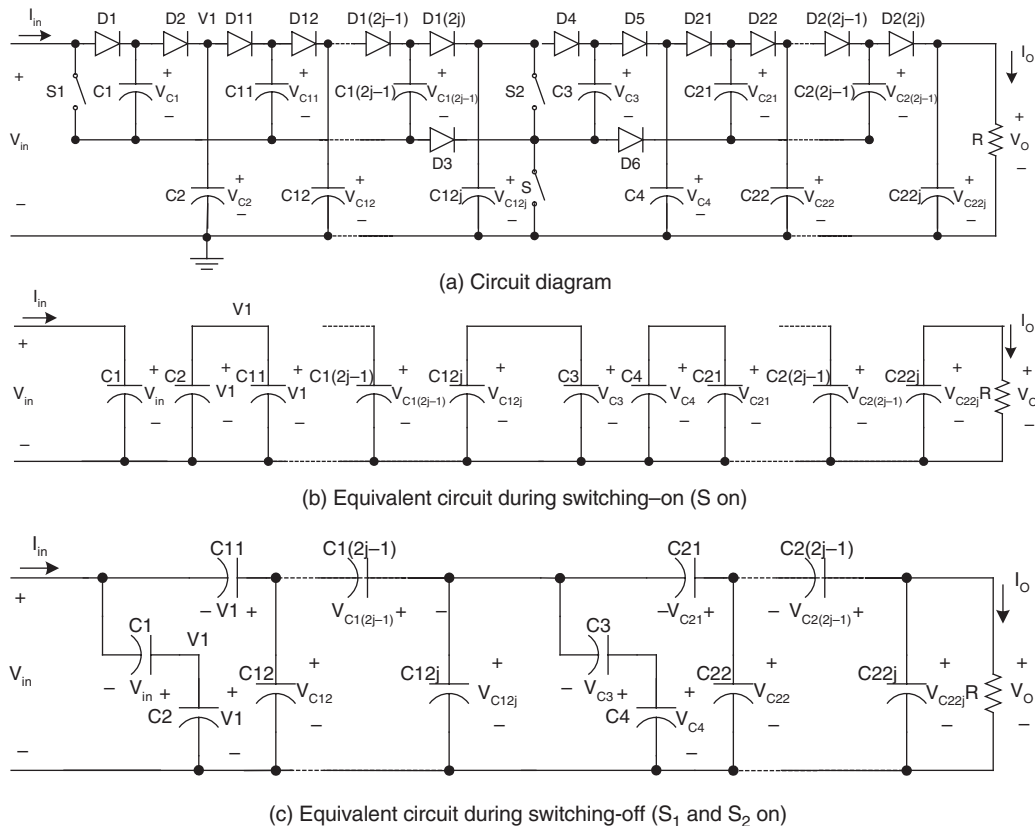


FIGURE 9.13
Re-lift multiple-enhanced circuit.

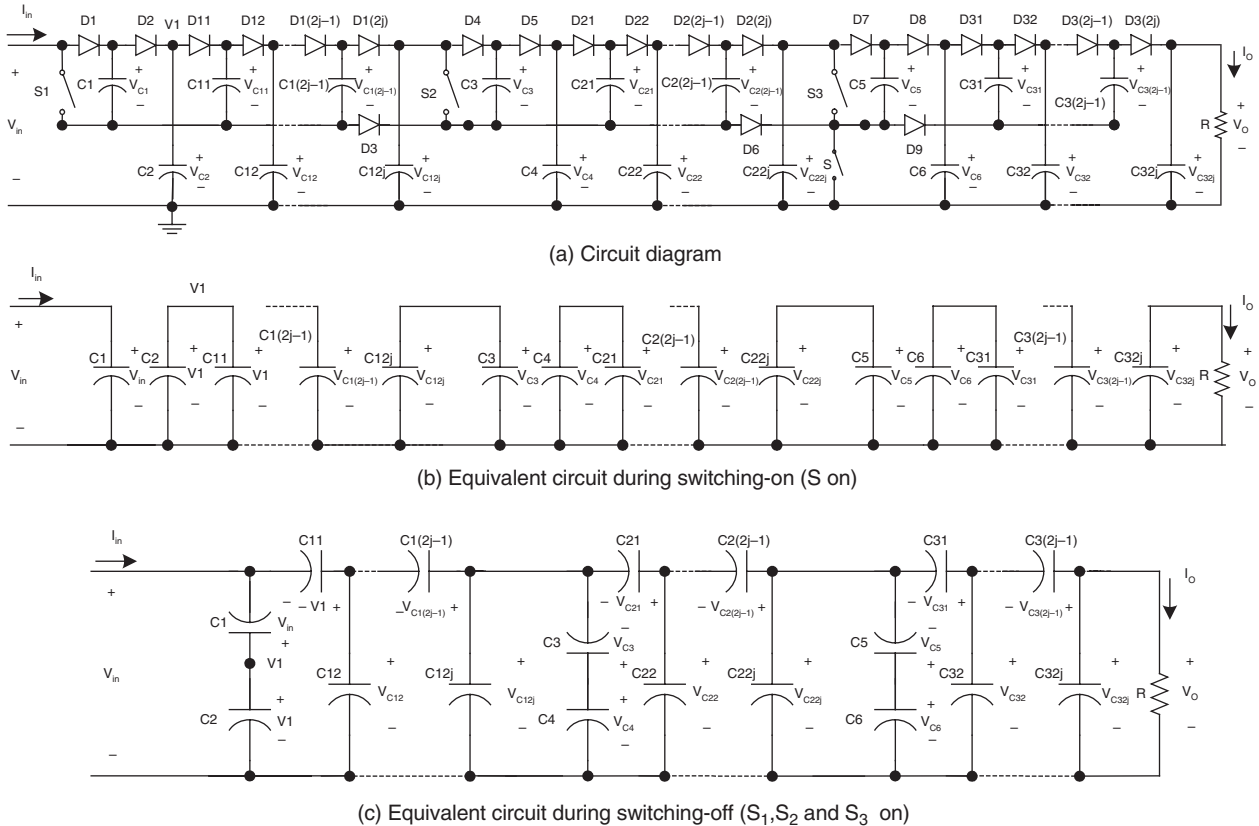


FIGURE 9.14
Triple-lift multiple-enhanced circuit.

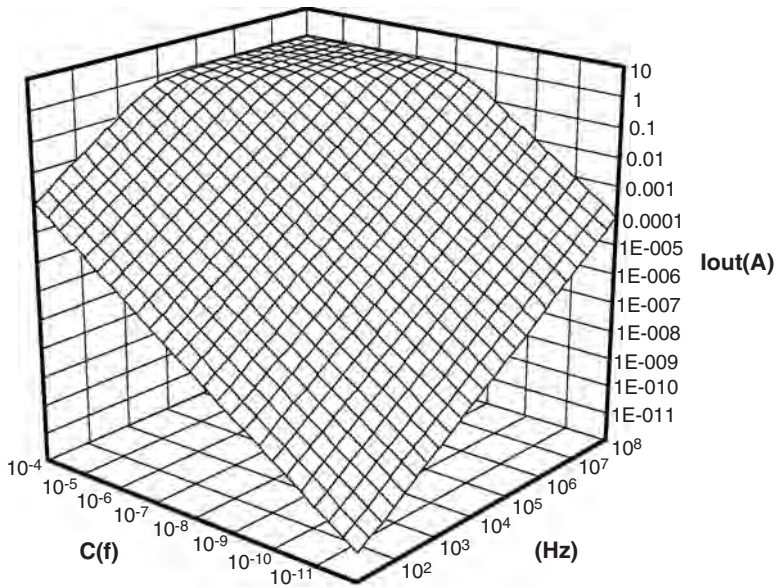


FIGURE 9.15

The relationship among output current I_o , operation frequency f and capacitance C .

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

$$V_O = (1 + j)V_{in} - \Delta V_1 - \Delta V_O \quad (9.20)$$

9.6.2 Re-Lift Multiple-Enhanced Circuit

The re-lift multiple-enhanced circuit is derived from re-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 9.13](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (9.21)$$

where ΔV_2 is set for the same reason as ΔV_1 .

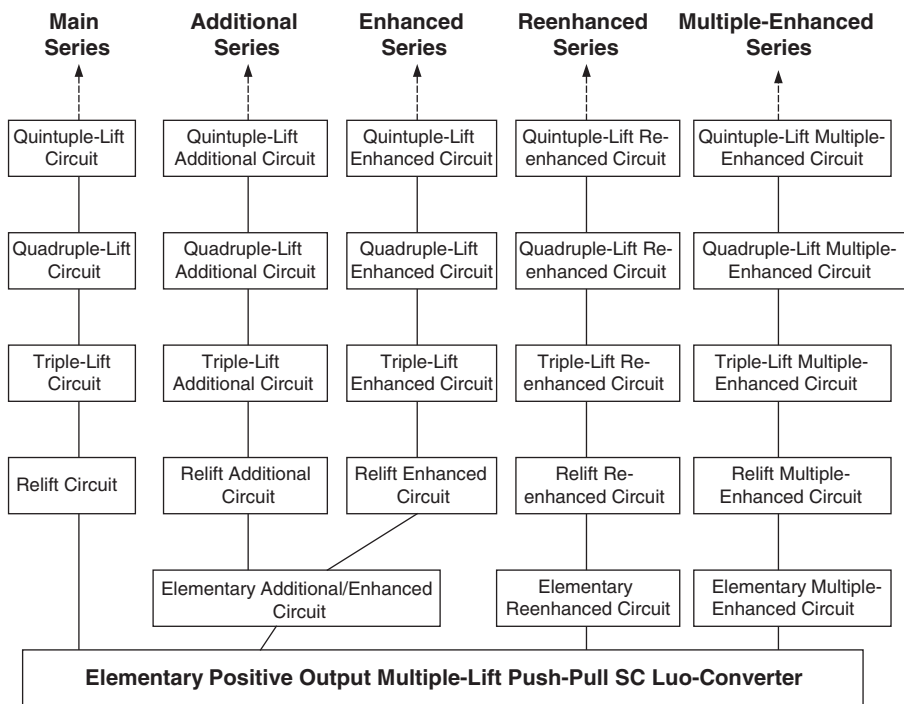


FIGURE 9.16

The family tree of multiple-lift push-pull switched-capacitor Luo-converters.

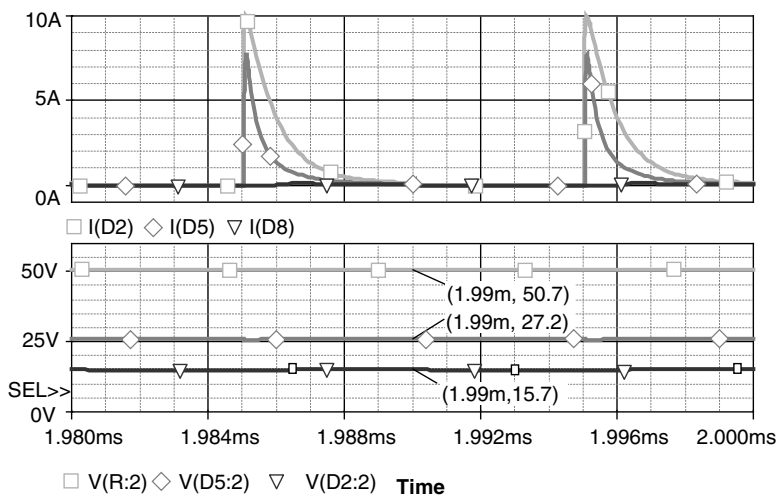


FIGURE 9.17

The simulation result of a triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

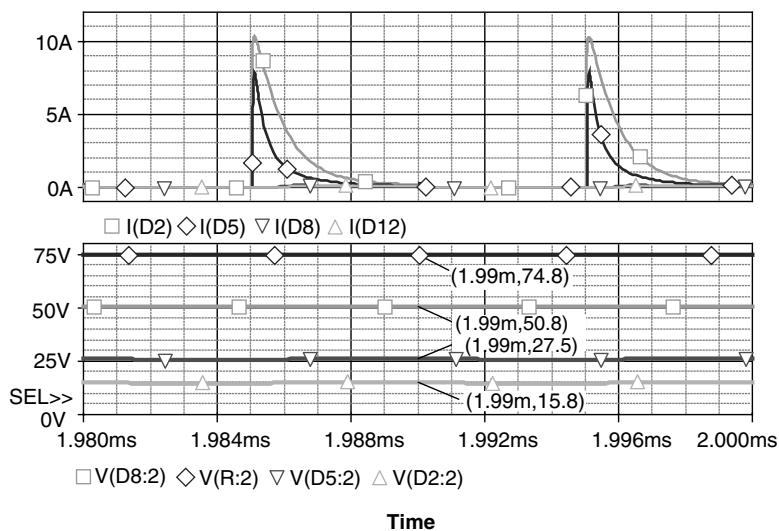


FIGURE 9.18

The simulation result of a triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

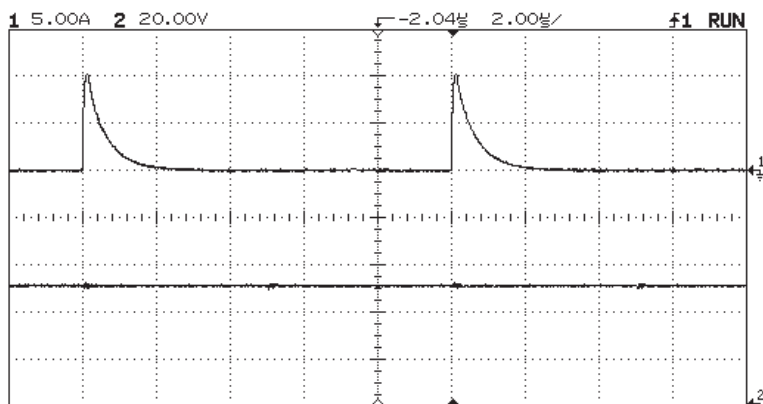


FIGURE 9.19

The experimental result of a triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

9.6.3 Triple-Lift Multiple-Enhanced Circuit

The triple-lift multiple-enhanced circuit is derived from triple-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 9.14](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is

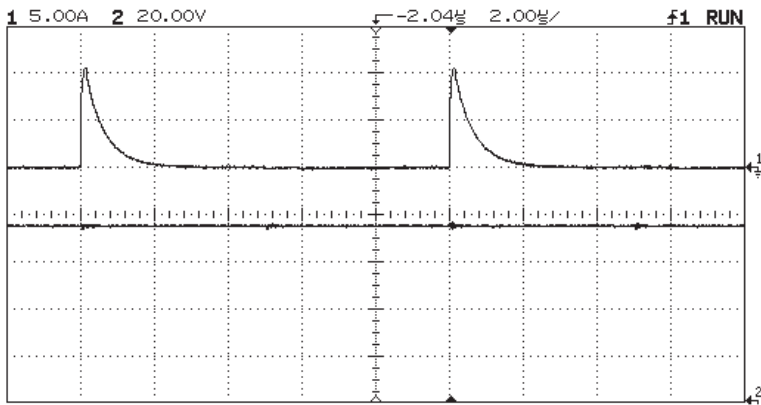


FIGURE 9.20

The experimental result of a triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (9.22)$$

where ΔV_3 is set for the same reason as ΔV_1 .

9.6.4 Higher Order Lift Multiple-Enhanced Circuit

Higher order lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple (j) times in each stage circuit. The output voltage of the n th-lift multiple-enhanced circuit is

$$V_O = 1.5 \times (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}) - \Delta V_n - \Delta V_O \quad (9.23)$$

9.7 Theoretical Analysis

The maximum output current is a key parameter of the DC-DC converter. The output voltage of DC-DC step-up converter can be shown as

$$V_o = \frac{k_s V_{in} - k_d V_d}{1 + \frac{T}{R} \sum_{i=1}^{m+1} \frac{n_i}{C_i} [1 - e^{-\frac{kTn_i}{R_i C_i}}] \prod_{j=1}^{m+1} n_j^2} \quad (9.24)$$

where $k_s = \frac{1 + \sum_{i=1}^{m+1} \prod_{j=1}^i n_j}{\prod_{i=1}^{m+1} n_i}$ and $k_d = \sum_{i=1}^{m+1} \frac{n_i(n_i + 1)}{m + 1}$

In Equation (9.24), m and n are the step-number of the converter and the number of the serial-parallel capacitors network respectively. T and k are the switch period and the duty-cycle ratio in the state 1, respectively. For the three-lift circuit, $m = 1$, $n_1 = n_2 = 1$ and $f = 1/T$, we can write the Equation (9.24) as follows

$$V_o = \frac{3V_{in} - 4V_d}{1 + \frac{1}{fR} \left(\frac{1/C_2}{1 - e^{-\frac{1}{2fR_2C_2}}} + \frac{1/C_1}{1 - e^{-\frac{1}{2fR_1C_1}}} \right)} \quad (9.25)$$

Since $I_o = V_o/R$, we can write the output current of this three-lift circuit as follows

$$I_o = \frac{3V_{in} - 4V_d - V_o}{\frac{1/C_2}{1 - e^{-\frac{1}{2fR_2C_2}}} + \frac{1/C_1}{1 - e^{-\frac{1}{2fR_1C_1}}}} f \quad (9.26)$$

where V_{in} is the source voltage assuming 10 V, V_o is the output voltage assuming 21.6 V, V_d is the voltage drop across diode, R_i which corresponds to the wire resistor of capacitor C_i . In order to increase the output current of the converter, we selected Schottky barrier diode ($V_d = 0.4$ V), then

$$3V_{in} - 4V_d - V_o = 6.8 \text{ V} \quad (9.27)$$

For getting the maximum output current, $C_1 = C_2 = C$ have to be chosen. In addition we assumed $R_1 = R_2 = R$. Therefore, the description of the output current can be simplified as

$$I_o = 0.9 f C [1 - \exp(-1/2RfC)] \quad (9.28)$$

Figure 9.15 shows the relationship among output current I_o , operation frequency f and capacitance C on the basis of the equation. From the result, it is concluded that

1. Higher frequency can result in bigger output current, especially the capacitance of C if the serial-parallel capacitors is not elevated for integration.
2. For a certain capacitor, there is a maximum frequency restriction, and it reduces when the capacitance is raised.
3. The output current can be up to 1A if the operation frequency f of the converter and the capacitance C of the serial-parallel capacitors are suitably chosen.

In addition, it can be shown from the equation deducing that the maximum ratio P_o/C can be obtained by using the same capacitance of the serial-parallel capacitors in the structure. The theoretical analysis for the higher order lift circuits is similar to above description.

9.8 Summary of This Technique

Using this technique, it is easy to design the Higher Order Lift circuit to obtain high output voltage. All these converters can be sorted in several sub-series: main series, additional series, enhanced series, re-enhanced series and multiple-enhanced series. The output voltage of the n th-lift circuit is

$$V_O = \begin{cases} 2^m V_{in} - \sum_{i=0}^{m-1} 2^i \Delta V_{m-i} & \text{Main_series} \\ 1.5 * (2^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}) - \Delta V_m - \Delta V_O & \text{Additional_series} \\ (3^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}) - \Delta V_m - \Delta V_O & \text{Enhanced_series} \\ (4^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}) - \Delta V_m - \Delta V_O & \text{Re-Enhanced_series} \\ [(j+2)^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i}] - \Delta V_m - \Delta V_O & \text{Multiple-Enhanced_series} \end{cases} \quad (9.29)$$

From above formula, the family tree of positive output multiple-lift push-pull switched-capacitor Luo-converters is shown in [Figure 9.16](#).

9.9 Simulation Results

To verify the design and calculation results, the PSpice simulation package was applied to these circuits. Choosing $V_I = 10$ V, all capacitors $C_i = 2$ μ F, R

= 60 k, $k = 0.5$ and $f = 100$ kHz, we obtain the current and voltage values in the following converters.

9.9.1 A Triple-Lift Circuit

Assume that the voltage drops ΔV_1 , ΔV_2 , and ΔV_3 are about 4.2 V, the current waveforms of I_{D2} , I_{D5} , and I_{D8} , then voltage values of V_1 , V_2 , and V_O are 15.7 V, 27.2 V, and 50.7 V. The simulation results (current and voltage values) in [Figure 9.17](#) are identically matched to the calculated results.

9.9.2 A Triple-Lift Additional Circuit

Assume that the voltage drops ΔV_1 , ΔV_2 , ΔV_3 , and ΔV_O are about 4.2 V, the current waveforms of I_{D2} , I_{D5} , I_{D8} , and I_{D12} , then voltage values of V_1 , V_2 , V_3 , and V_O are 15.8 V, 27.5 V, 50.8 V, and 74.8 V. The simulation results (current and voltage values) shown in [Figure 9.18](#) are identically matched to the calculated results.

9.10 Experimental Results

A test rig was constructed to verify the design and calculation results, and was compared with PSpice simulation results. With $V_I = 10$ V, all capacitors $C_i = 2$ μ F, $R = 60$ k, $k = 0.5$ and $f = 100$ kHz, we measured the output voltage and the first diode current values in following converters.

9.10.1 A Triple-Lift Circuit

After careful measurement, we obtained the current waveform of I_{D2} (shown in channel 1 with 5 A/Div in [Figure 9.19](#)) and voltage value of V_O of 50.8 V (shown in channel 2 with 20 V/Div). The experimental results (current and voltage values) in [Figure 9.17](#) are identically matched to the calculated and simulation results.

9.10.2 A Triple-Lift Additional Circuit

The experimental results (voltage and current values) are identically matching to the calculated and simulation results, as shown in [Figure 9.20](#). The current waveform of I_{D2} (shown in channel 1 with 5 A/Div) and voltage value of V_O of 75 V (shown in channel 2 with 20 V/Div) have been obtained.

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Negative Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters

Positive output multiple-lift push-pull switched-capacitor Luo-converters have been introduced in the previous chapter. Correspondingly, negative output multiple-lift push-pull switched-capacitor Luo-converters will be introduced in this chapter.

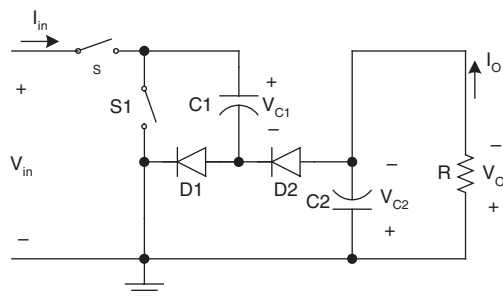
10.1 Introduction

Negative output multiple-lift push-pull switched-capacitor Luo-converters can be sorted into several sub-series:

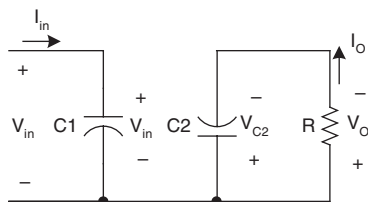
- Main series
- Additional series
- Enhanced series
- Re-enhanced series
- Multiple-enhanced series

Each circuit has one main switch S and several slave switches as S_i ($i = 1, 2, 3, \dots, n$). The number n is called stage number. The main switch S is on and slaves off during switching-on period kT , and S is off and slaves on during switch-off period $(1 - k)T$. The load is resistive load R . Input voltage and current are V_{in} and I_{in} , output voltage and current are V_O and I_O .

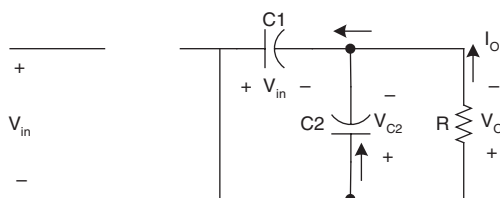
Each circuit in the main series has one main switch S and n slave switches for n th stage circuit, $2n$ capacitors and $(3n - 1)$ diodes. Each circuit in the additional series has one main switch S and n slave switches for n th stage circuit, $2(n + 1)$ capacitors and $(3n + 1)$ diodes. Each circuit in the enhanced series has one main switch S and n slave switches for n th stage circuit, $4n$ capacitors and $(5n - 1)$ diodes. Each circuit in the re-enhanced series has one main switch S and n slave switches for n th stage circuit, $6n$ capacitors, and



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 on)

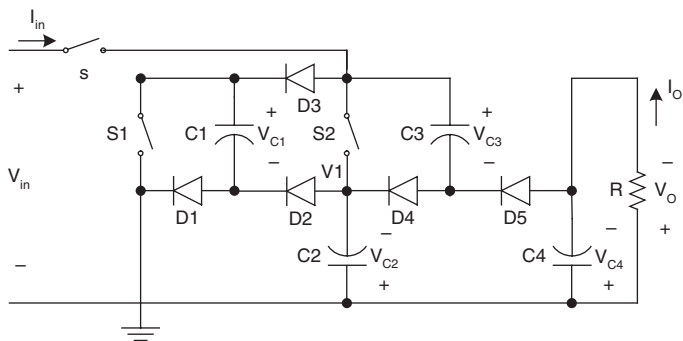
FIGURE 10.1

Elementary circuit of N/O push-pull SC Luo-converter.

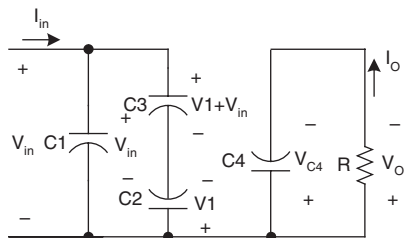
$(7n - 1)$ diodes. Each circuit in the multiple (j times)-enhanced series has one main switch S and n slave switches for n th stage circuit, $2(1 + j)n$ capacitors and $[(3 + 2j)n - 1]$ diodes. To simplify the calculation and explanation, all output values are the absolute values. The output voltage polarity is shown in the corresponding figure.

10.2 Main Series

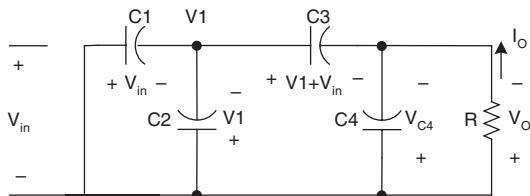
The first three stages of the main series are shown in Figure 10.1 to Figure 10.3. For convenience they are called negative out-put (N/O) elementary



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 and S_2 on)

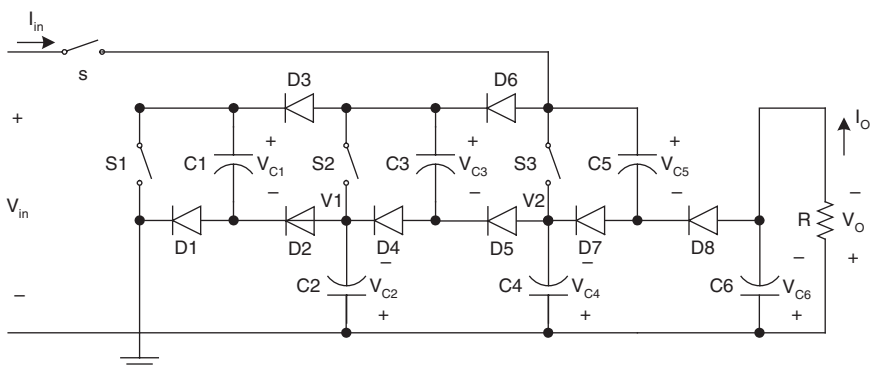
FIGURE 10.2

N/O re-lift push-pull SC circuit.

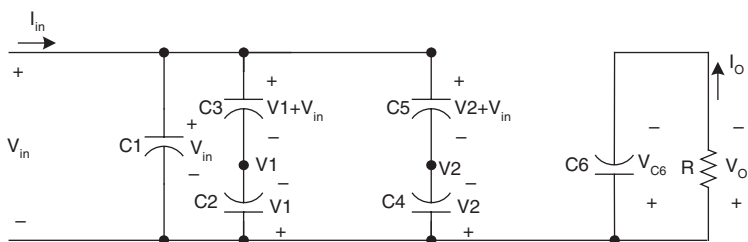
circuit, N/O re-lift circuit, and N/O triple-lift circuit respectively, and are numbered as $n = 1, 2$, and 3 .

10.2.1 N/O Elementary Circuit

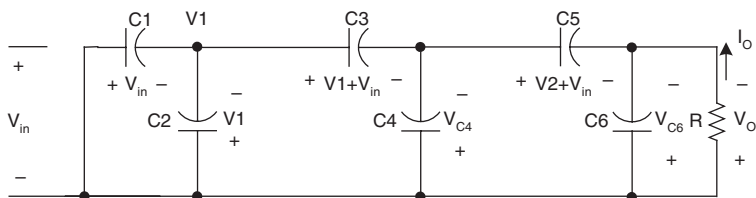
The elementary circuit and its equivalent circuits during switch-on and switch-off are shown in [Figure 10.1](#). Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitor C_2 is charged to $V_o = 2V_{in}$ during switch-off. Therefore, the output voltage is (absolute value):



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 , and S_3 on)

FIGURE 10.3

N/O triple-lift push-pull SC circuit.

$$V_O = 2V_{in} - V_{in} = V_{in} \quad (10.1)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 . The real output voltage is

$$V_O = V_{in} - \Delta V_1 \quad (10.2)$$

10.2.2 N/O Re-Lift Circuit

The N/O re-lift circuit is derived from N/O elementary circuit by adding one slave switch, two switched-capacitors, and three diodes (S_2 - C_3 - C_4 - D_3 - D_4 - D_5). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 10.2. The switches S and (S_1 , S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} and voltage across capacitor C_3 is charged to V_1 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$ and voltage across capacitor C_4 is charged to $V_O = 2V_1 - \Delta V_2$ during switch-off. Therefore, the output voltage is

$$V_O = 2V_1 - \Delta V_2 - V_{in} = 3V_{in} - 2\Delta V_1 - \Delta V_2 \quad (10.3)$$

where ΔV_2 is set for the same reason as ΔV_1 .

10.2.3 N/O Triple-Lift Circuit

The N/O triple-lift circuit is derived from N/O re-lift circuit by adding one more slave switch, two switched-capacitors, and three diodes (S_3 - C_5 - C_6 - D_6 - D_7 - D_8). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 10.3. The switches S and (S_1 , S_2 , S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_5 is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in}$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_O = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

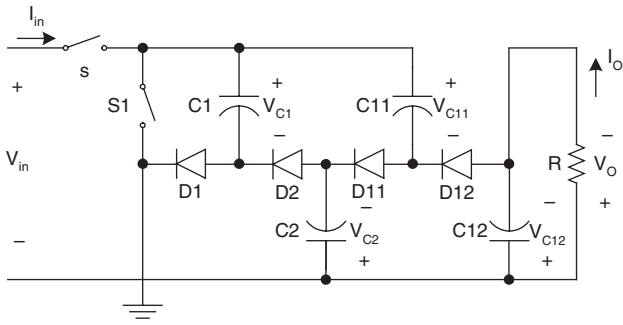
$$\begin{aligned} V_O &= 2V_2 - \Delta V_3 - V_{in} = 4V_1 - 2\Delta V_2 - \Delta V_3 - V_{in} \\ &= 7V_{in} - 4\Delta V_1 - 2\Delta V_2 - \Delta V_3 \end{aligned} \quad (10.4)$$

where ΔV_3 is set for the same reason as ΔV_1 .

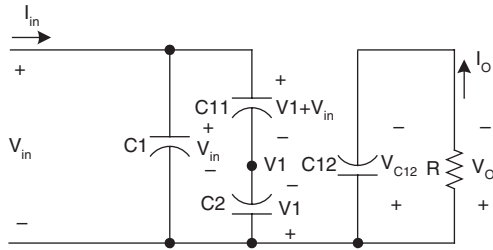
10.2.4 N/O Higher Order Lift Circuit

The N/O higher order lift circuit is can be designed by multiple repeating of the parts mentioned in previous sections. If the slave switches' number is n , the output voltage of the n th-lift circuit is

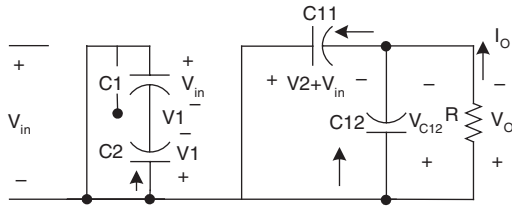
$$V_O = (2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-i} \quad (10.5)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 on)

FIGURE 10.4

N/O elementary additional/enhanced circuit.

10.3 Additional Series

The first three stages of the additional series are shown in Figure 10.4 to Figure 10.6. For convenience they are called N/O elementary additional circuit, N/O re-lift additional circuit, and N/O triple-lift additional circuit respectively, and are numbered as $n = 1, 2$, and 3.

10.3.1 N/O Elementary Additional Circuit

The N/O elementary additional circuit is derived from the N/O elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in [Figure 10.4](#). Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_O = V_1 + V_{in} - V_{in} = 2V_{in} \quad (10.6)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

$$V_O = 2V_{in} - \Delta V_1 - \Delta V_O \quad (10.7)$$

10.3.2 N/O Re-Lift Additional Circuit

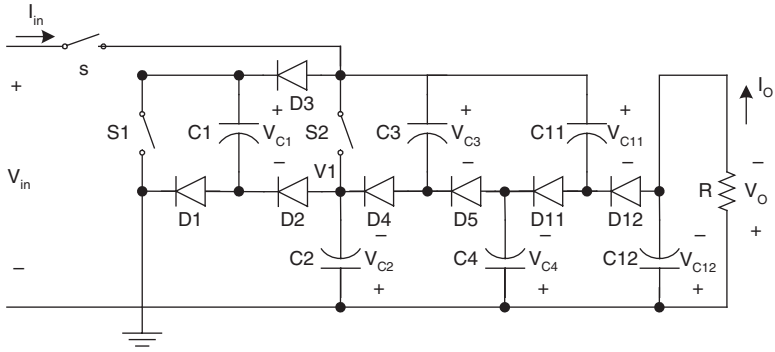
The N/O re-lift additional circuit is derived from the N/O re-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.5](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = 5V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (10.8)$$

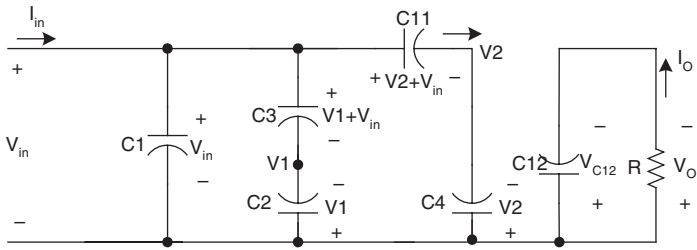
where ΔV_2 is set for the same reason as ΔV_1 .

10.3.3 N/O Triple-Lift Additional Circuit

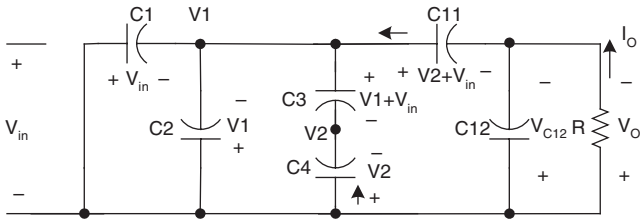
The N/O triple-lift additional circuit is derived from the N/O triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.6](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(b) Equivalent circuit during switching-off (S_1 and S_2 on)

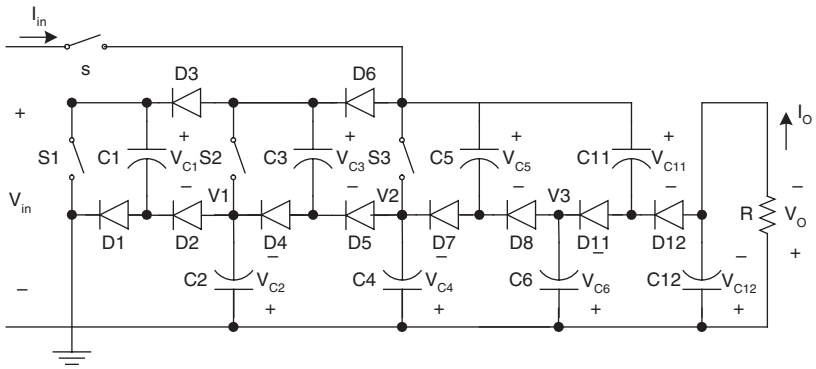
FIGURE 10.5

N/O re-lift additional circuit.

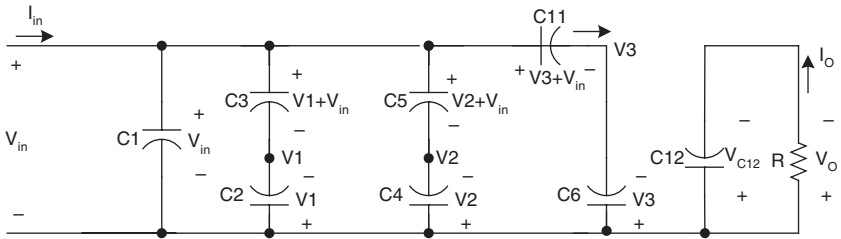
capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} = 11V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (10.9)$$

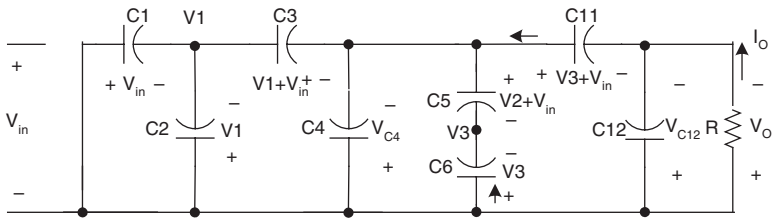
where ΔV_3 is set for the same reason as ΔV_1 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 , and S_3 on)

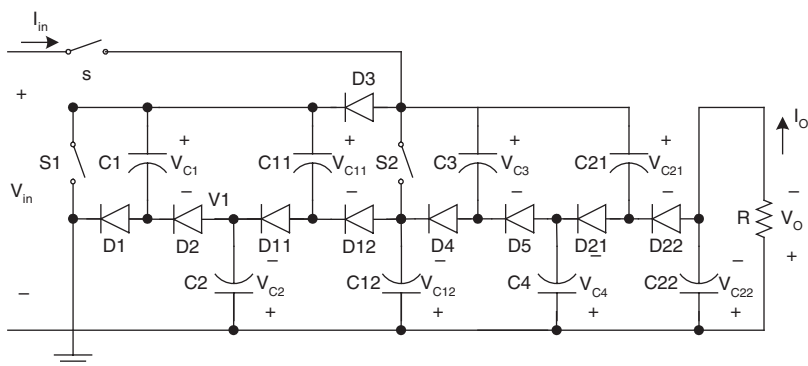
FIGURE 10.6

N/O triple-lift additional circuit.

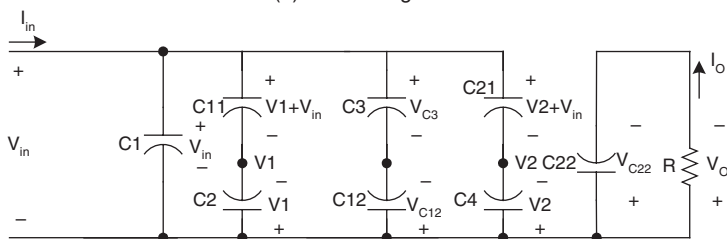
10.3.4 N/O Higher Order Lift Additional Circuit

The N/O higher order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. The output voltage of the n th-lift circuit is

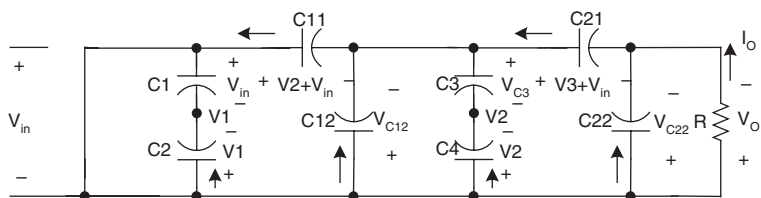
$$V_O = 1.5 * (2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}) - V_{in} - \Delta V_n - \Delta V_O \quad (10.10)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 , and S_3 on)

FIGURE 10.7
N/O re-lift enhanced circuit.

10.4 Enhanced Series

The first three stages of the enhanced series are shown in [Figures 10.4](#), [10.7](#), and [10.8](#). For convenience, they are called N/O elementary enhanced circuit, N/O re-lift enhanced circuit, and N/O triple-lift enhanced circuit respectively, and are numbered as $n = 1, 2$, and 3 .

10.4.1 N/O Elementary Enhanced Circuit

The N/O elementary enhanced circuit is derived from N/O elementary circuit by adding a DEC. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in [Figure 10.4](#). Therefore, the output voltage is

$$V_O = V_1 + V_{in} - V_{in} = 2V_{in} \quad (10.6)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

$$V_O = 2V_{in} - \Delta V_1 - \Delta V_O \quad (10.7)$$

10.4.2 N/O Re-Lift Enhanced Circuit

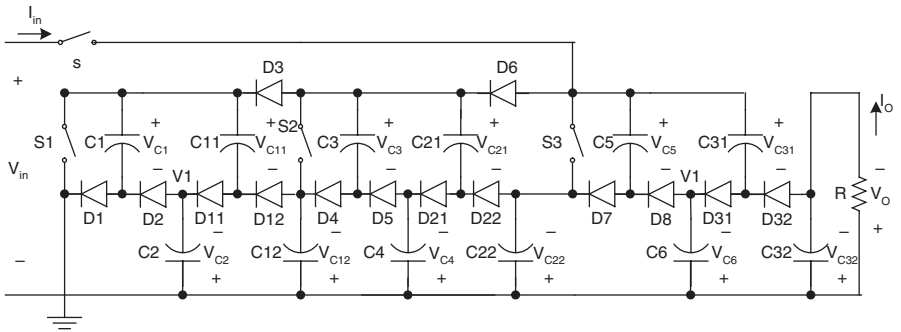
The N/O re-lift enhanced circuit is derived from the N/O re-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.7](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = 8V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (10.11)$$

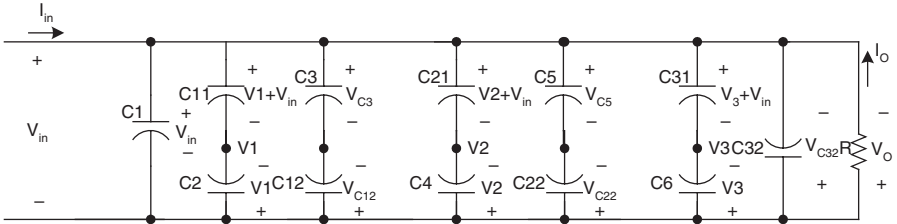
where ΔV_2 is set for the same reason as ΔV_1 .

10.4.3 N/O Triple-Lift Enhanced Circuit

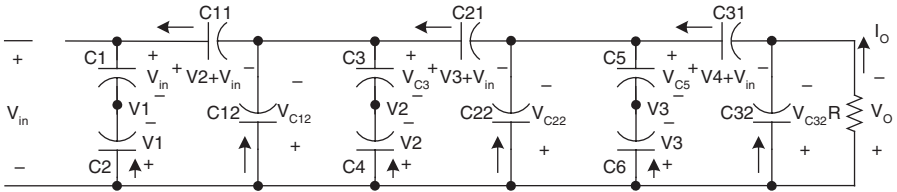
The N/O triple-lift enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.8](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 , and S_3 on)

FIGURE 10.8

N/O triple-lift enhanced circuit.

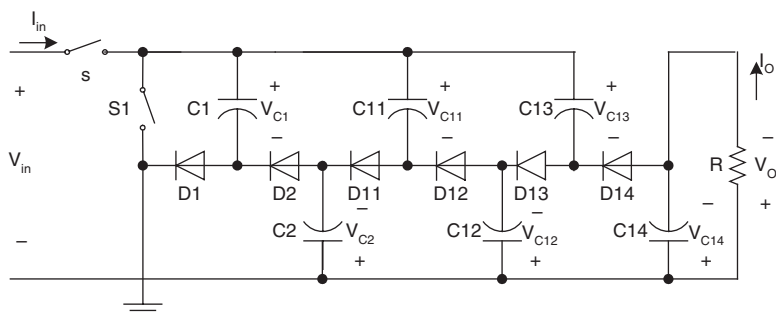
$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} = 26V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (10.12)$$

where ΔV_3 is set for the same reason as ΔV_1 .

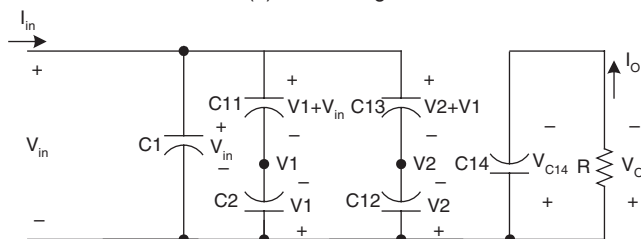
10.4.4 N/O Higher Order Lift Enhanced Circuit

The N/O higher order lift enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC in each stage circuit. The output voltage of the n th-lift circuit is

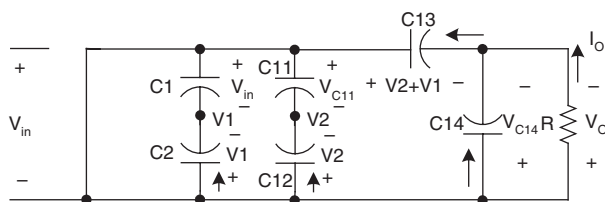
$$V_O = [(3^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}] - \Delta V_n - \Delta V_O \quad (10.13)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 on)

FIGURE 10.9

N/O elementary re-enhanced circuit.

10.5 Re-Enhanced Series

The first three stages of the re-enhanced series are shown in Figure 10.9 to Figure 10.11. For convenience, they are called N/O elementary re-enhanced circuit, N/O re-lift re-enhanced circuit, and N/O triple-lift re-enhanced circuit respectively, and are numbered as $n = 1, 2$, and 3 .

10.5.1 N/O Elementary Re-Enhanced Circuit

The N/O elementary re-enhanced circuit is derived from N/O elementary circuit by adding the DEC twice. Its circuit diagram and its equivalent circuits

during switch-on and switch-off are shown in [Figure 10.9](#). Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. The voltage across capacitors C_{12} and C_{13} is charged to $V_{C12} = 4V_{in}$ during switch-off. Therefore, the output voltage is

$$V_O = V_{C12} - V_{in} = 3V_{in} \quad (10.14)$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

$$V_O = 3V_{in} - \Delta V_1 - \Delta V_O \quad (10.15)$$

10.5.2 N/O Re-Lift Re-Enhanced Circuit

The N/O re-lift re-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.10](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

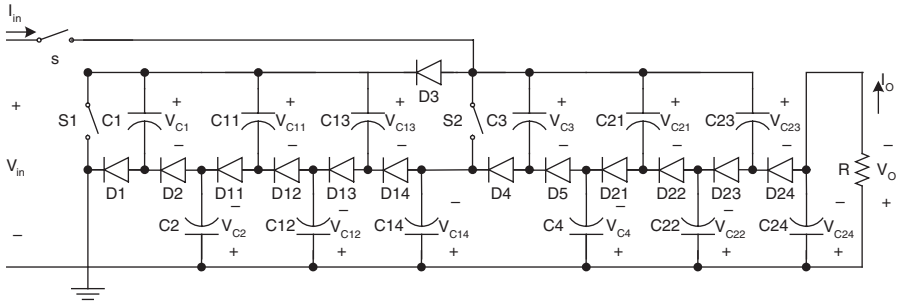
$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = 15V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (10.16)$$

where ΔV_2 is set for the same reason as ΔV_1 .

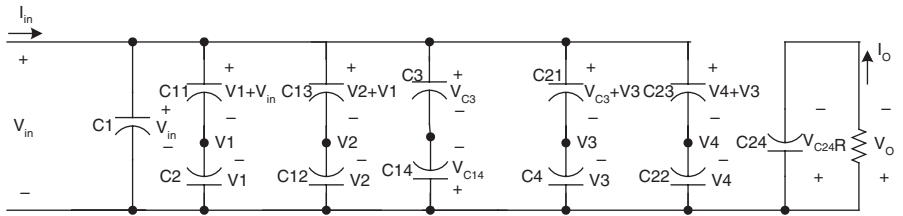
10.5.3 N/O Triple-Lift Re-Enhanced Circuit

The N/O triple-lift re-enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.11](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

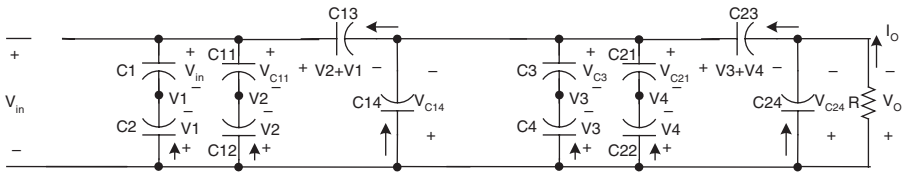
$$V_O = V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} = 63V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \quad (10.17)$$



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 , S_2 , and S_3 on)

FIGURE 10.10

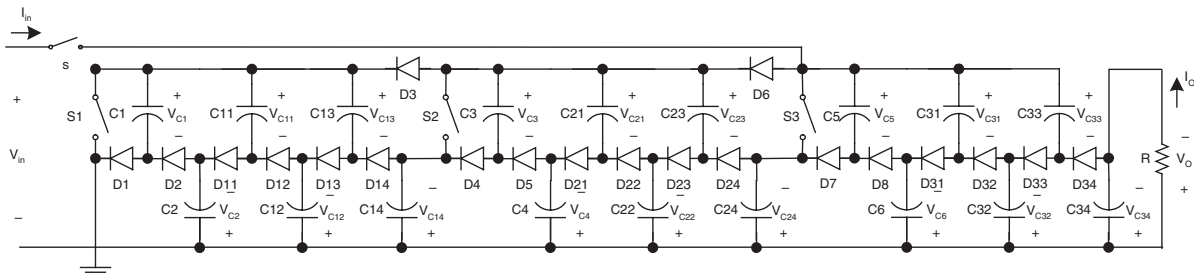
N/O re-lift re-enhanced circuit.

where ΔV_3 is set for the same reason as ΔV_1 .

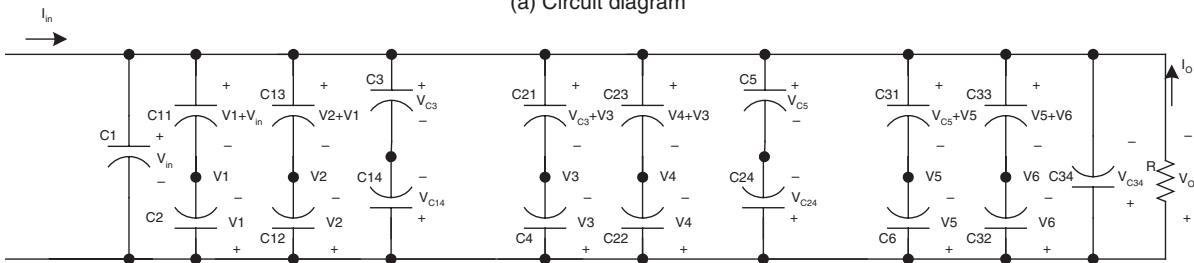
10.5.4 N/O Higher Order Lift Re-Enhanced Circuit

The N/O higher order lift re-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. The output voltage of the n th-lift circuit is

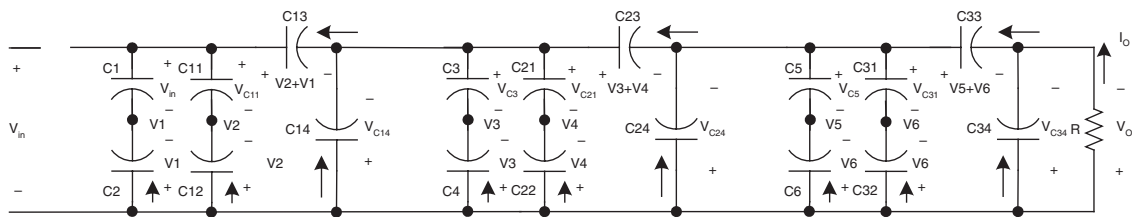
$$V_O = [(4^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}] - \Delta V_n - \Delta V_O \quad (10.18)$$



(a) Circuit diagram



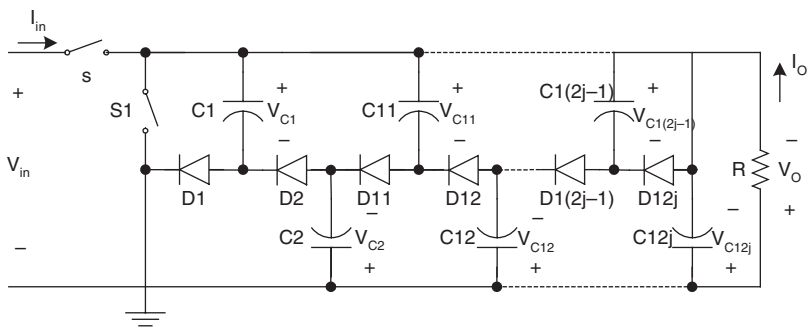
(b) Equivalent circuit during switching-on (S on)



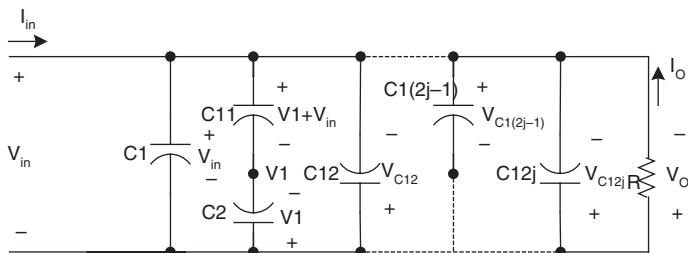
(c) Equivalent circuit during switching-off (S_1 , S_2 , and S_3 on)

FIGURE 10.11

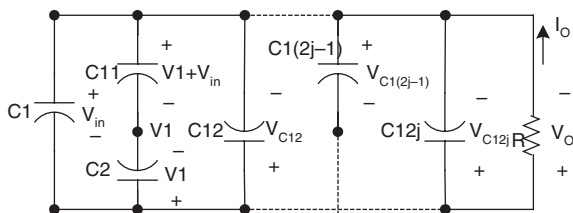
N/O triple-lift re-enhanced circuit.



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



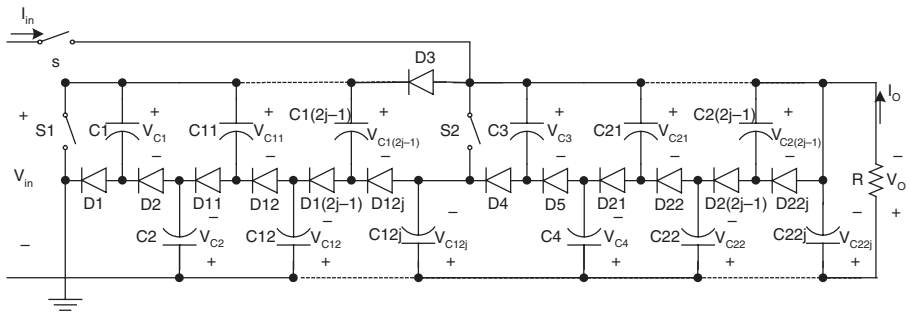
(c) Equivalent circuit during switching-off (S1 on)

FIGURE 10.12

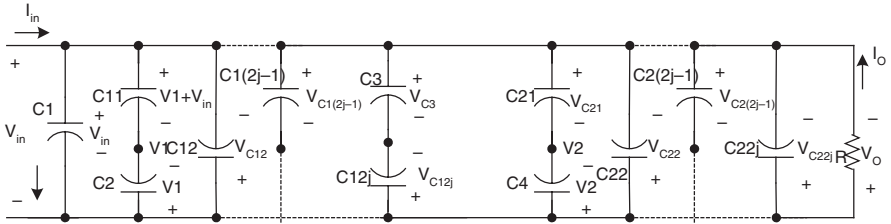
N/O elementary multiple-enhanced circuit.

10.6 Multiple-Enhanced Series

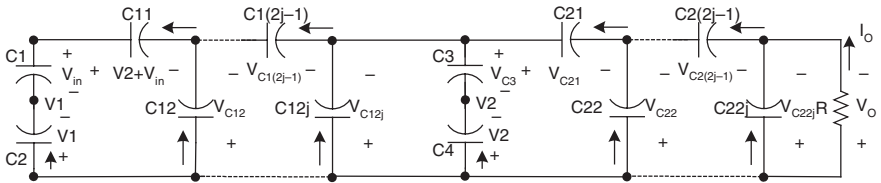
The first three stages of the multiple-enhanced series are shown in Figure 10.12 to Figure 10.14. For convenience they are called N/O elementary multiple-enhanced circuit, N/O re-lift multiple-enhanced circuit and N/O triple-lift multiple-enhanced circuit respectively, and are numbered as $n = 1, 2$, and 3 .



(a) Circuit diagram



(b) Equivalent circuit during switching-on (S on)



(c) Equivalent circuit during switching-off (S_1 and S_2 on)

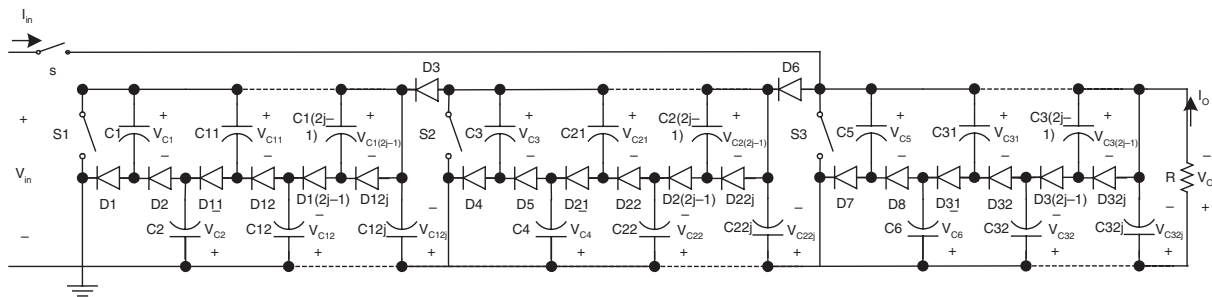
FIGURE 10.13

N/O re-lift multiple-enhanced circuit.

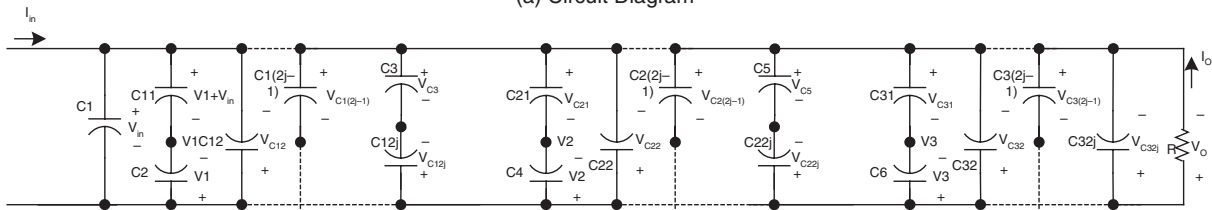
10.6.1 N/O Elementary Multiple-Enhanced Circuit

The N/O elementary multiple-enhanced circuit is derived from the N/O elementary circuit by adding the DEC multiple (j) times. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 10.12. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. The voltage across capacitors $C_{1(2j-1)}$ is charged to $V_{C1(2j-1)} = (1 + j)V_{in}$ during switch-off. Therefore, the output voltage is

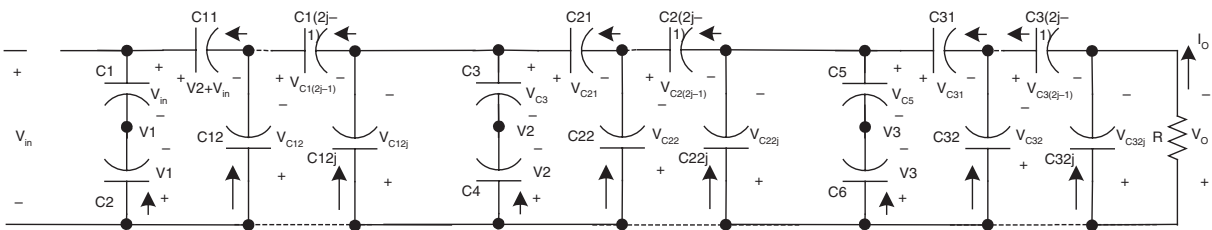
$$V_O = V_{C1(2j-1)} - V_{in} = jV_{in} \quad (10.19)$$



(a) Circuit Diagram



(b) Equivalent circuit switching-on (\$S\$ on)



(c) Equivalent circuit switching-off (\$S_1\$ and \$S_2\$ and \$S_3\$ on)

FIGURE 10.14

N/O triple-lift multiple-enhanced circuit.

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_O (for additional output parts). The real output voltage is

$$V_O = jV_{in} - \Delta V_1 - \Delta V_O \quad (10.20)$$

10.6.2 N/O Re-Lift Multiple-Enhanced Circuit

The N/O re-lift multiple-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.13](#). The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 and voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_{12} is charged to $V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O$ during switch-off. Therefore, the output voltage is

$$V_O = V_2 + V_1 - \Delta V_2 - \Delta V_O - V_{in} = [(1+j)^2 - 1]V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_O \quad (10.21)$$

where ΔV_2 is set for the same reason as ΔV_1 .

10.6.3 N/O Triple-Lift Multiple-Enhanced Circuit

The N/O triple-lift multiple-enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC multiple (j) times in each stage circuit.. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in [Figure 10.14](#). The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} , voltage across capacitor C_3 is charged to V_1 , voltage across capacitor C_5 is charged to V_2 and voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$ and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$\begin{aligned} V_O &= V_3 + V_2 - \Delta V_3 - \Delta V_O - V_{in} \\ &= [(1+j)^3 - 1]V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_O \end{aligned} \quad (10.22)$$

where ΔV_3 is set for the same reason as ΔV_1 .

10.6.4 N/O Higher Order Lift Multiple-Enhanced Circuit

The N/O higher order lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple (j) times in each stage circuit. The output voltage of the n th order lift circuit is

$$V_O = [(1+j)^n - 1]V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} - \Delta V_n - \Delta V_O \quad (10.23)$$

10.7 Summary of This Technique

Using this technique, it is easy to design N/O higher order lift circuits to obtain high output voltage. All these converters can be sorted in several subseries: main series, additional series, enhanced series, re-enhanced series, and multiple-enhanced series. The output voltage of the n th-lift circuit is

$$V_O = \begin{cases} (2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} & \text{Main_series} \\ (1.5 * 2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Additional_series} \\ (3^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Enhanced_series} \\ (4^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Re-Enhanced_series} \\ [(2+j)^n - 1]V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-1} - \Delta V_n - \Delta V_O & \text{Multiple-Enhanced_series} \end{cases} \quad (10.24)$$

From above formula, the family tree of negative output multiple-lift push-pull switched-capacitor Luo-converters is shown in [Figure 10.15](#).

10.8 Simulation and Experimental Results

To verify the design and calculation results, PSpice simulation package was applied for these circuits. Choosing $V_1 = 10$ V, all capacitors $C_i = 2$ μ F, $R = 60$ k, $k = 0.5$ and $f = 100$ kHz, the voltage and current values are obtained from a N/O triple-lift circuit. The same conditions are applied to a test rig, experimental results are then obtained.

10.8.1 Simulation Results

Assume that the voltage drops ΔV_1 , ΔV_2 , and ΔV_3 are about 4.2 V, the voltage values of V_1 , V_2 , and V_O to be -5.2 V, -16 V, and -41 V respectively and

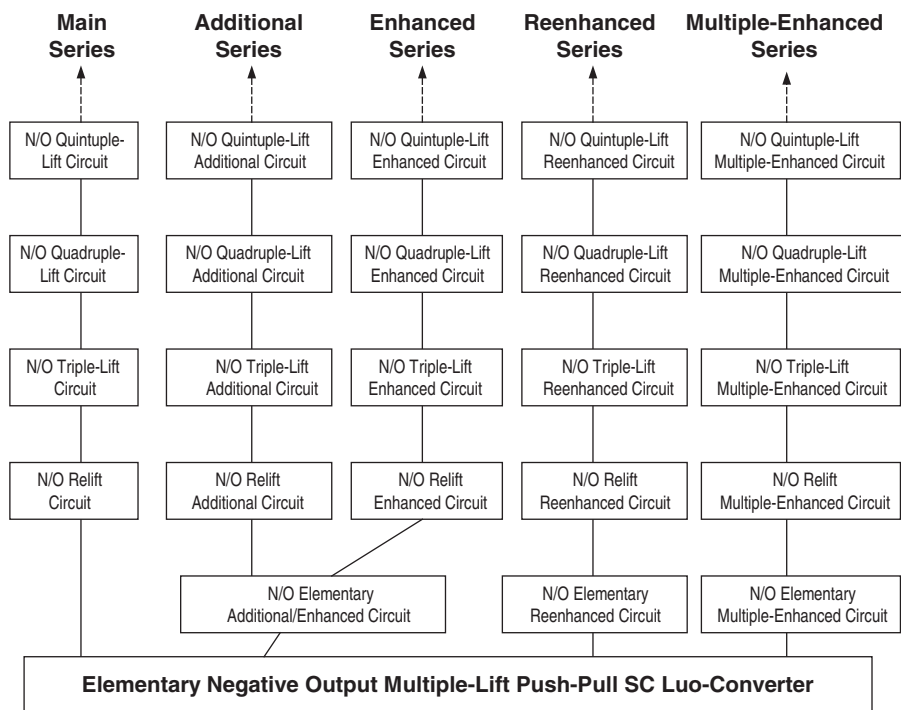


FIGURE 10.15

The family tree of N/O multiple-lift push-pull switched-capacitor Luo-converters.

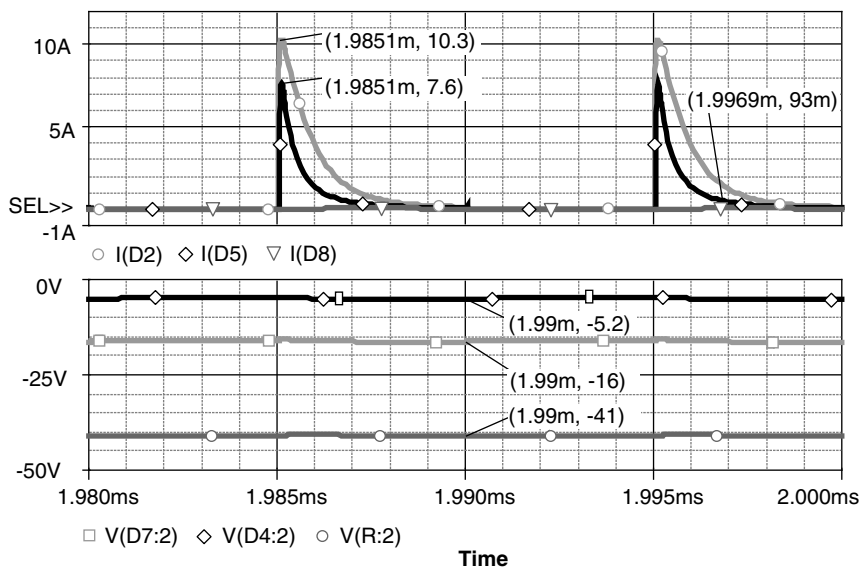


FIGURE 10.16

The simulation results of a N/O triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

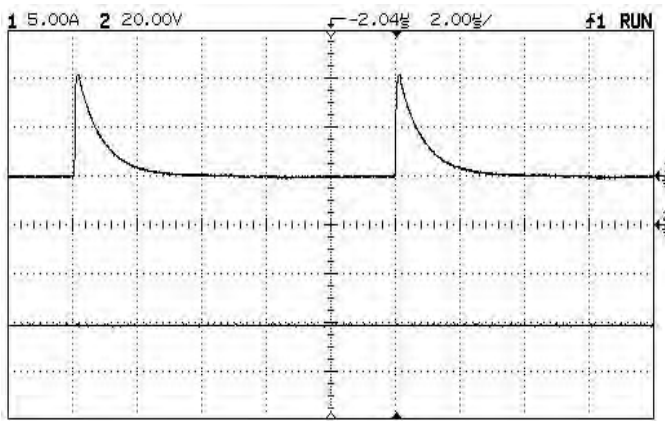


FIGURE 10.17

Experimental results of a N/O triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

current waveforms of I_{D2} , I_{D5} , and I_{D8} (the leak values are 103 A, 6.7 A, and 0.093 A respectively) are obtained. The simulation results voltage values in Figure 10.16 are identically matched to the calculated results.

10.8.2 Experimental Results

Assuming that the voltage drops ΔV_1 , ΔV_2 , and ΔV_3 are still about 4.2 V, the output voltage V_O (−41 V) and current waveform of I_{D2} (leak value is 10.3 A) are obtained and shown in Figure 10.17, which are identically matched to the calculated and simulation results.

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Multiple-Quadrant Soft-Switch Converters

The third generation converters can transfer large amounts of power with high power density to actuators. However, its power losses are usually high during the transfer of large amounts of power since the power losses across the switch devices are high. The soft switch technique is an effective way to reduce the converter power losses and improve the efficiency. Therefore, it is a very popular method in industrial applications.

The fourth generation converters are called soft-switch converters. The soft-switch technique involves many methods implementing resonance characteristics. A popular method is the resonant-switch. Soft-switch converters are mainly implemented by the resonant technique. The resonant converters have drawn much attention in research applications. They are sorted into four categories:

- Load-resonant converters
- Resonant-DC-link converters
- High-frequency-link integral-half-cycle converters
- Resonant-switch converters

The converters of the first, second, and third categories can be applied in those cases depending on the load components and linking-cable. The converters of the fourth category are applied in the case depending on the resonant circuit in the switch-end, which are independent from load and link components. After about two decades of investigation and application, most industrial applications use **resonant-switch converters**.

Resonant-switch converters can perform in the over-resonant state, critical/optimum-resonant state, and quasi-resonant state. In order to determine two (current/voltage) zero-cross points for switch-on and switch-off, the quasi-resonant state is usually employed. The corresponding converter is called quasi-resonant converter (QRC). The quasi-resonant state can perform in full-waveform mode and half-waveform mode. The clue of soft switch technique focuses on the zero-cross point rather than the resonance. Consequently, there is no need in performing full-waveform mode. Most soft switch converters perform in half-waveform mode.

The zero-current-switch (ZCS) quasi-resonant-converters (QRC), zero-voltage-switch (ZVS) quasi-resonant-converters (QRC) and zero-transition (ZT) converters will be discussed in this chapter.

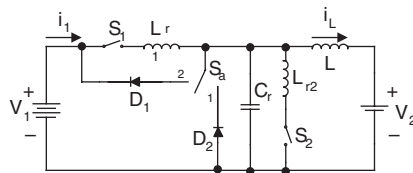
11.1 Introduction

Zero-current-switch quasi-resonant-converters implement ZCS operation. Since switches turn-on and turn-off at the moment that the current is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low. Therefore, the electromagnetic interference (EMI) is low, and electromagnetic susceptibility (EMS) and electromagnetic compatibility (EMC) are reasonable.

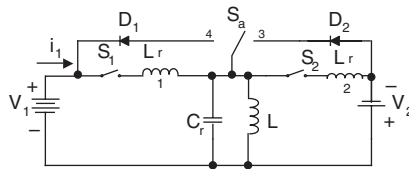
Zero-voltage-switch quasi-resonant-converters use the ZVS technique. Since switches turn-on and turn-off at the moment that the voltage is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low, so that the EMI is low, and EMS and EMC are reasonable.

ZCS-QRC and ZVS-QRC have large voltage and current stresses. In addition the conduction duty cycle k and switch frequency f are not individually adjusted. In order to overcome these drawbacks we designed zero-voltage-plus-zero-current-switches (ZV/ZCS) and zero-transition (ZT) converters, which implement the ZVS and ZCS technique. Since switches turn-on and -off at the moment that the voltage and/or current is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low, so that the EMI is low, and EMS and EMC are reasonable.

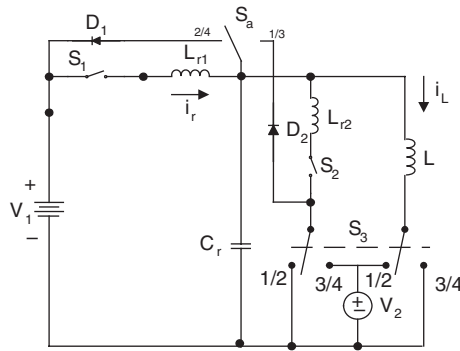
The ZCS technique significantly reduces the power losses across the switches during the switch-on and switch-off. Unfortunately, most papers discuss the converters only working at single quadrant operation. This paper introduces the multiple-quadrant DC/DC ZCS quasi-resonant Luo-converter. It performs the soft switch technique with a four-quadrant operation, which effectively reduces the power losses and largely increases the power transfer efficiency. The results obtained from analysis and design were compared and verified by practical test results.



(a) Circuit 1 for the operation in Quadrant I and Quadrant II



(b) Circuit 2 for the operation in Quadrant III and Quadrant IV



(c) Circuit 3 for the Four-quadrant operation

FIGURE 11.1

Four-quadrant DC/DC ZCS quasi-resonant Luo-converter.

11.2 Multiple-Quadrant DC/DC ZCS Quasi-Resonant Luo-Converters

A multiple-quadrant DC/DC ZCS quasi-resonant Luo-converter is shown in Figure 11.1. Circuit 1 implements the operation in quadrants I and II, i.e., two quadrant (I and II) 2CS quasi-resonant Luo-converters. Circuit 2 implements the operation in quadrants III and IV, i.e., two quadrant (III and IV) 2CS quasi-resonant Luo-converters. Circuit 1 and circuit 2 can be converted to each other by auxiliary changeover switch S_3 . Auxiliary switch S_a assists the two-quadrant operation in the same circuit. It is controlled by a logic quadrant-operation controller. Each circuit consists of one main inductor L and two switches. Assuming that the main inductance L is sufficient large,

TABLE 11.1

Switch Status

Circuit //Switch or Diode	Mode A (Q-I)		Mode B (Q-II)		Mode C (Q-III)		Mode D (Q-IV)	
	State-on	State-off	State-on	State-off	State-on	State-off	State-on	State-off
Circuit	Circuit 1				Circuit 2			
S_1	ON				ON			
D_1								
S_2					ON			
D_2	ON				ON			
S_a	Position 1		Position 2		Position 3		Position 4	

Note: The blank status means off.

the current i_L remains constant. The source and load voltages are usually constant, e.g., $V_1 = 42$ V and $V_2 = \pm 28$ V. There are four modes of operation:

1. Mode A (quadrant I) : electrical energy is transferred from V_1 side to V_2 side.
2. Mode B (quadrant II): electrical energy is transferred from V_2 side to V_1 side.
3. Mode C (quadrant III) : electrical energy is transferred from V_1 side to $-V_2$ side.
4. Mode D (quadrant IV): electrical energy is transferred from $-V_2$ side to V_1 side.

Each mode has two states: *on* and *off*. The switch status of each state is shown in Table 11.1.

11.2.1 Mode A

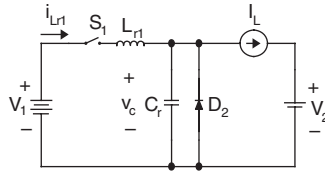
Mode A is a ZCS buck converter. The equivalent circuit, current, and voltage waveforms are shown in [Figure 11.2](#). There are four time regions for the switch-on and -off period. The conduction duty cycle is $kT = (t_1 + t_2)$ when the input current flows through the switch S_1 and the main inductor L . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r1} - C_r$.

The natural resonance frequency is

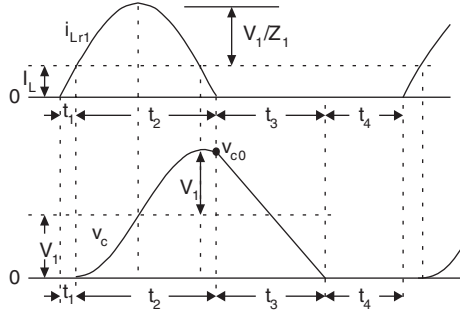
$$\omega_1 = \frac{1}{\sqrt{L_{r1}C_r}} \tag{11.1}$$

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_{r1}}{C_r}} \tag{11.2}$$



(a) Equivalent Circuit



(b) Waveforms

FIGURE 11.2
Mode A operation.

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_1} \sin(\omega_1 t + \alpha_1) \quad (11.3)$$

Considering the DC component I_L , the peak current is

$$i_{1-peak} = I_L + \frac{V_1}{Z_1} \quad (11.4)$$

11.2.1.1 Interval $t = 0$ to t_1

Switch S_1 turns on at $t = 0$, the source current increases linearly with the slope V_1/L_{r1} ; this is called current linear rising interval. This current is smaller than the constant load current I_L . Therefore, no current flows through the resonant capacitor C_r .

When $t = t_1$, it is equal to I_L . Therefore, the time is

$$t_1 = \frac{I_L L_{r1}}{V_1} \quad (11.5)$$

And corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{I_L Z_1}{V_1}\right) \quad (11.6)$$

11.2.1.2 Interval $t = t_1$ to t_2

In this period the current flows through the resonant capacitor C_r . Circuit $L_{r1} - C_r$ resonates; this is the resonance interval. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L and then 0 if the converter works in subresonance state. Switch S_1 turns off at $t = t_2$. At this point we can see that the switch S_1 turns off at zero current condition. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad (11.7)$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. When $t = t_2$, the corresponding value v_{CO} of the capacitor voltage v_C is

$$v_{CO} = V_1[1 + \sin(\pi/2 + \alpha_1)] = V_1(1 + \cos \alpha_1) \quad (11.8)$$

11.2.1.3 Interval $t = t_2$ to t_3

Since the switch S_1 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L ; this is the linear recovering interval. Because load current I_L is a constant current the voltage v_C decreases linearly from v_{CO} to 0 at $t = t_3$.

$$t_3 = \frac{v_{CO} C_r}{I_L} \quad (11.9)$$

11.2.1.4 Interval $t = t_3$ to t_4

Capacitor voltage v_C cannot decrease to negative value because of the free-wheeling diode D_2 ; this is the normal switch-off interval. The load current commutates from C_r to D_2 at $t = t_3$. Since then, the load current free-wheels through the main inductor L , load voltage source V_2 and free-wheeling diode D_2 . The time length t_4 of this period depends on the design requirement. Ignoring the power losses and $I_2 = I_L$, we have the input average current I_1 :

$$I_1 = \frac{I_L V_2}{V_1} = \frac{t_1 + t_2}{T} \left(I_L + \frac{V_1}{Z_1} \frac{2 \cos \alpha_1}{\pi/2 + \alpha_1} \right) \quad (11.10)$$

Therefore,

$$t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_L} (I_L + \frac{V_1}{Z_1} \frac{2 \cos \alpha_1}{\pi / 2 + \alpha_1}) - (t_1 + t_2 + t_3) \quad (11.11)$$

We have the conduction duty

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \quad (11.12)$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \quad (11.13)$$

And corresponding frequency is

$$f = 1 / T \quad (11.14)$$

11.2.2 Mode B

Mode B is a ZCS boost converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.3](#). There are four time regions for the switch-on and -off period. The conduction duty cycle is $kT = (t_1 + t_2)$, but the output current only flows through the source V_1 in the period t_4 . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r2} - C_r$.

The resonance frequency is

$$\omega_2 = \frac{1}{\sqrt{L_{r2} C_r}} \quad (11.15)$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} \quad (11.16)$$

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_2} \sin(\omega_2 t + \alpha_2) \quad (11.17)$$

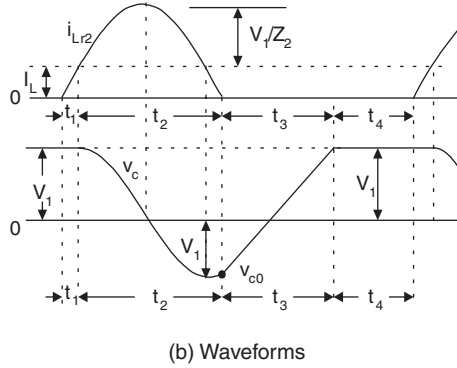
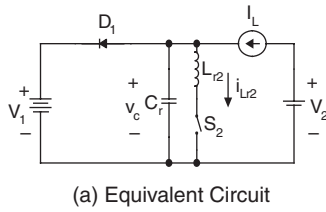


FIGURE 11.3
Mode B operation.

Considering the DC component I_L , the peak current is

$$i_{2-peak} = I_L + \frac{V_1}{Z_2} \quad (11.18)$$

11.2.2.1 Interval $t = 0$ to t_1

Switch S_2 turns on at $t = 0$, the voltage across capacitor C_r is equal to V_1 . The inductor current i_{Lr2} increases linearly with the slope V_1/L_{r2} . This current is smaller than the constant load current I_L . Therefore, no current flows through the resonant capacitor C_r .

When $t = t_1$, it is equal to I_L . Therefore, the time is

$$t_1 = \frac{I_L L_{r2}}{V_1} \quad (11.19)$$

and corresponding angular position is

$$\alpha_2 = \sin^{-1} \left(\frac{I_L Z_2}{V_1} \right) \quad (11.20)$$

11.2.2.2 Interval $t = t_1$ to t_2

In this period the current flows through the resonant capacitor C_r . Circuit $L_{r2} - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L , and then 0 if the converter works in subresonance state. Switch S_2 turns off at $t = t_2$.

At this point we can see that the switch S_2 turns off at zero current condition. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad (11.21)$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. When $t = t_2$, the corresponding value v_{CO} of the capacitor voltage v_c is

$$v_{CO} = -V_1 \sin(\pi / 2 + \alpha_2) = -V_1 \cos \alpha_2 \quad (11.22)$$

11.2.2.3 Interval $t = t_2$ to t_3

Since the switch S_2 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L . Because load current I_L is a constant current the voltage v_c increases linearly from v_{CO} to V_1 at $t = t_3$.

$$t_3 = \frac{(V_1 - v_{CO})C_r}{I_L} \quad (11.23)$$

11.2.2.4 Interval $t = t_3$ to t_4

Capacitor voltage v_c cannot be higher than V_1 because of the diode D_1 conducted. The main inductor current commutates from C_r to D_1 at $t = t_3$. Since then, the load current flows through the main inductor L , diode D_1 source voltage V_1 and load voltage V_2 . The time length t_4 of this period depends on the design requirement. Ignoring the power losses and $I_2 = I_L$, we have the output average current I_1 :

$$I_1 = \frac{I_L V_2}{V_1} = \frac{t_4}{T} I_L \quad (11.24)$$

or

$$\frac{V_2}{V_1} = \frac{t_4}{T} = \frac{t_4}{t_1 + t_2 + t_3 + t_4} \quad (11.25)$$

Therefore,

$$t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1} \quad (11.26)$$

We have the conduction duty

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \quad (11.27)$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \quad (11.28)$$

and corresponding frequency is

$$f = 1 / T \quad (11.29)$$

11.2.3 Mode C

Mode C is a ZCS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.4](#). There are four time regions for the switch-on and -off period. The conduction duty cycle is $kT = (t_1 + t_2)$ when the input current flows through the switch S_1 and the main inductor L . The output current only flows through V_2 in t_4 . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r1} - C_r$.

The resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_{r1} C_r}} \quad (11.30)$$

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_{r1}}{C_r}} \quad (11.31)$$

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_1} \sin(\omega_1 t + \alpha_1) \quad (11.32)$$

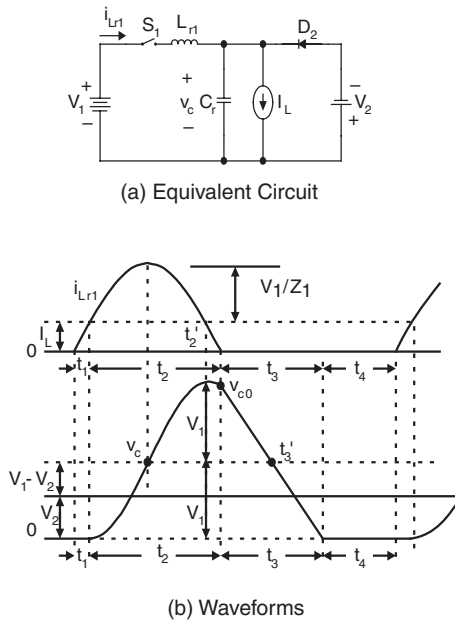


FIGURE 11.4
Mode C operation.

Considering the DC component I_L , the peak current is

$$i_{1-peak} = I_L + \frac{V_1}{Z_1} \quad (11.33)$$

11.2.3.1 Interval $t = 0$ to t_1

Switch S_1 turns on at $t = 0$, the voltage across capacitor C_r is equal to V_2 . The inductor current i_{Lr1} increases linearly with the slope $(V_1 + V_2)/L_{r1}$. This current is smaller than the constant load current I_L . Therefore, no current flows through the resonant capacitor C_r .

When $t = t_1$, it is equal to I_L . Therefore, the time

$$t_1 = \frac{I_L L_{r1}}{V_1 + V_2} \quad (11.34)$$

and corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{I_L Z_1}{V_1}\right) \quad (11.35)$$

Before S_1 turns on at $t = 0$, free-wheeling diode D_2 is conducted. Therefore the capacitor voltage v_c across the resonant capacitor C_r is equal to V_2 in this interval.

11.2.3.2 Interval $t = t_1$ to t_2

In this period the current flows through the resonant capacitor C_r . Circuit $L_{r1} - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L , and then 0 if the converter works in subresonance state. Switch S_1 turns off at $t = t_2$.

At this point we can see that the switch S_1 turns off at zero current condition. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad (11.36)$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. The resonant amplitude is equal to V_1 . When $t = t_2$, the corresponding value v_{CO} of the capacitor voltage v_c is

$$v_{CO} = V_1 - V_2 + V_1 \sin(\pi / 2 + \alpha_1) = V_1(1 + \cos \alpha_1) - V_2 \quad (11.37)$$

11.2.3.3 Interval $t = t_2$ to t_3

Since the switch S_1 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L . Because load current I_L is a constant current the voltage v_c decreases linearly from v_{CO} to $-|V_2|$ at $t = t_3$. In this interval, the free-wheeling diode D_2 does not conduct because it is reversibly biased.

$$t_3 = \frac{(v_{CO} + V_2)C_r}{I_L} \quad (11.38)$$

11.2.3.4 Interval $t = t_3$ to t_4

Capacitor voltage v_c is equal to V_2 at $t = t_3$, the free-wheeling diode D_2 then conducted. The main inductor current commutates from C_r to V_2 at $t = t_3$. Since then, the load current free-wheels through the main inductor L , load voltage source V_2 and free-wheeling diode D_2 . The time length t_4 of this period depends on the design requirement. Ignoring the power losses, we have the input average current I_1 :

$$I_1 = \frac{t_1 + t_2}{T} (I_L + \frac{V_1}{Z_1} \frac{2 \cos \alpha_1}{\pi / 2 + \alpha_1}) \quad (11.39)$$

and

$$I_2 = \frac{t_4}{T} I_L \quad (11.40)$$

Therefore,

$$t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_L} \left(I_L + \frac{V_1}{Z_1} \frac{2 \cos \alpha_1}{\pi / 2 + \alpha_1} \right) \quad (11.41)$$

We have the conduction duty

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \quad (11.42)$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \quad (11.43)$$

and corresponding frequency is

$$f = 1 / T \quad (11.44)$$

11.2.4 Mode D

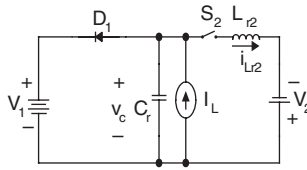
Mode D is a ZCS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.5](#). There are four time regions for the switch-on and -off period. The conduction duty cycle is $kT = (t_1 + t_2)$, but the output current only flows through the source V_1 in the period t_4 . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r2} - C_r$.

The resonance frequency is

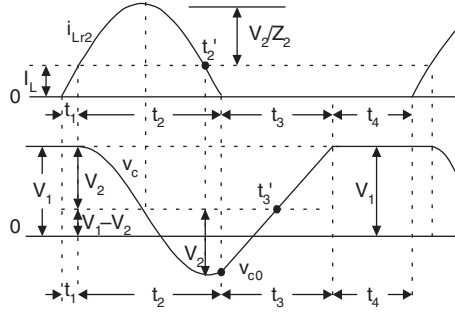
$$\omega_2 = \frac{1}{\sqrt{L_{r2} C_r}} \quad (11.45)$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} \quad (11.46)$$



(a) Equivalent Circuit



(b) Waveforms

FIGURE 11.5
Mode D operation.

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_2} \sin(\omega_2 t + \alpha_2) \quad (11.47)$$

Considering the DC component I_L the peak current is

$$i_{2-peak} = I_L + \frac{V_1}{Z_2} \quad (11.48)$$

11.2.4.1 Interval $t = 0$ to t_1

Switch S_2 turns on at $t = 0$, the voltage across capacitor C_r is equal to V_1 . The inductor current i_{Lr2} increases linearly with the slope $(V_1 + V_2)/L_{r2}$. This current is smaller than the constant load current I_L . Therefore, no current flows through the resonant capacitor C_r .

When $t = t_1$, it is equal to I_L . Therefore, the time

$$t_1 = \frac{I_L L_{r2}}{V_1 + V_2} \quad (11.49)$$

and corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{I_L Z_2}{V_2}\right) \quad (11.50)$$

11.2.4.2 Interval $t = t_1$ to t_2

In this period the current flows through the resonant capacitor C_r . Circuit $L_{r2} - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L , and then 0 if the converter works in subresonance state. Switch S_2 turns off at $t = t_2$.

At this point we can see that the switch S_2 turns off at zero current condition. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad (11.51)$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. When $t = t_2$, the corresponding value v_{CO} of the capacitor voltage v_C is

$$v_{CO} = (V_1 - V_2) - V_2 \sin(\pi / 2 + \alpha_2) = V_1 - V_2(1 + \cos \alpha_2) \quad (11.52)$$

11.2.4.3 Interval $t = t_2$ to t_3

Since the switch S_2 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L . Because load current I_L is a constant current the voltage v_C increases linearly from v_{CO} to V_1 at $t = t_3$.

$$t_3 = \frac{(V_1 - v_{CO})C_r}{I_L} = \frac{V_2 C_r}{I_L}(1 + \cos \alpha_2) \quad (11.53)$$

11.2.4.4 Interval $t = t_3$ to t_4

Capacitor voltage v_C cannot be higher than V_1 because of the diode D_1 conducted. The main inductor current commutates from C_r to D_1 at $t = t_3$. Since then, the output current I_1 flows through the main inductor L , diode D_1 source voltage V_1 and load voltage V_2 . The time length t_4 of this period depends on the design requirement. Ignoring the power losses, we have the output average current I_1 :

$$I_1 = \frac{I_L V_2}{V_1} = \frac{t_4}{T} I_L \quad (11.54)$$

and

$$I_2 = \frac{t_1 + t_2}{T} (I_L + \frac{V_2}{Z_2} \frac{2 \cos \alpha_2}{\pi / 2 + \alpha_2}) \quad (11.55)$$

Therefore,

$$t_4 = \frac{V_2(t_1 + t_2)}{V_1 I_L} (I_L + \frac{V_2}{Z_2} \frac{2 \cos \alpha_2}{\pi / 2 + \alpha_2}) \quad (11.56)$$

We have the conduction duty

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \quad (11.57)$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \quad (11.58)$$

And corresponding frequency is

$$f = 1 / T \quad (11.59)$$

11.2.5 Experimental Results

A testing rig with a battery of ± 28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are : $V_1 = 42$ V and $V_2 = \pm 28$ V, $L = 30$ μ H, $L_{r1} = L_{r2} = 1$ μ H, $C_r = 4$ μ F and the volume is 40 in³. The experimental results are shown in [Table 11.2](#). The average power transfer efficiency is 96.3%, and the total average power density (PD) is 17.1 W/in³. This figure is much higher than the classical converters whose PD is usually less than 5 W/in³. Since the switch frequency is low ($f < 41$ kHz) and this converter works at the mono-resonance frequency, the components of the high-order harmonics are small. Applying FFT analysis, the total harmonic distortion (THD) is very small, thus the EMI is weak, and the EMS and EMC are reasonable.

11.3 Multiple-Quadrant DC/DC ZVS Quasi Resonant Luo-Converter

Many industrial applications require the multi-quadrant operation with ZVS technique, since it significantly reduces the power losses. Unfortunately,

TABLE 11.2

Experimental Results for Different Frequencies

Mode	$f(\text{kHz})$	$L_{r1}=L_{r2} (\mu\text{H})$	$C_r (\mu\text{F})$	$I_l (\text{A})$	$I_o (\text{A})$	$I_L (\text{A})$	$P_l (\text{W})$	$P_o (\text{W})$	$\eta (\%)$	$\text{PD} (\text{W/in}^3)$
A	20.5	1	4	16.98	25	25	713	700	98.2	17.66
A	21	1	4	17.4	25	25	730.6	700	95.8	17.88
A	21.5	1	4	17.81	25	25	748	700	93.5	18.1
B	16.5	1	4	25	16.4	25	700	688.8	98.4	17.36
B	17	1	4	25	16.2	25	700	680.4	97.2	17.25
B	17.5	1	4	25	15.97	25	700	670.1	95.8	17.13
C	19	1	4	16.17	23.82	35	679.1	667	98.2	16.83
C	19.3	1	4	16.42	23.64	35	689.7	662	96	16.9
C	19.5	1	4	16.59	23.53	35	696.8	658.8	94.5	16.95
D	40	1	4	24.05	15.64	35	663.4	656.8	97.5	16.5
D	40.3	1	4	24.23	15.49	35	678.5	650.6	95.9	16.6
D	40.5	1	4	24.35	15.4	35	681.8	646.7	94.8	16.61

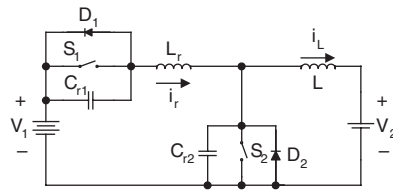
most of the papers discuss the ZVS converters only working at single quadrant operation. Four-quadrant DC/DC ZCS quasi-resonant Luo-converter effectively reduces the power losses and largely increases the power transfer efficiency. This is shown in [Figure 11.6](#). Circuit 1 implements the operation in quadrants I and II, circuit 2 implements the operation in quadrants III and IV. Circuit 1 and circuit 2 can be converted to each other by an auxiliary change-over switch S_3 , which is illustrated in circuit 3. Each circuit consists of one main inductor L and two switches. Assuming that the main inductance L is sufficient large, the current i_L is constant. The source and load voltages are usually constant, e.g., $V_1 = 42 \text{ V}$ and $V_2 = \pm 28 \text{ V}$. There are four modes of operation:

1. Mode A (quadrant I) : electrical energy is transferred from V_1 side to V_2 side.
2. Mode B (quadrant II): electrical energy is transferred from V_2 side to V_1 side.
3. Mode C (quadrant III) : electrical energy is transferred from V_1 side to $-V_2$ side.
4. Mode D (quadrant IV): electrical energy is transferred from $-V_2$ side to V_1 side.

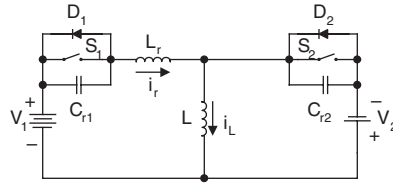
Each mode has two states: *on* and *off*. The switch/diode status of each state are shown in [Table 11.3](#).

11.3.1 Mode A

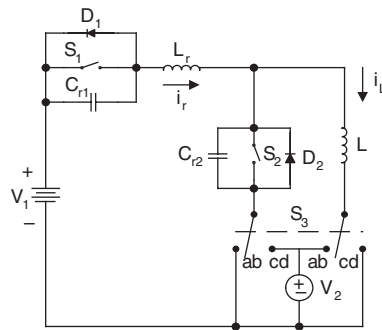
Mode A is a ZVS buck converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.7](#). There are four time regions for the switch-off and -on period. The conduction duty cycle is $kT = (t_3 + t_4)$ when



(a) Circuit 1 for the operation in Quadrant I and Quadrant II



(b) Circuit 2 for the operation in Quadrant III and Quadrant IV



(c) Circuit 3 for four Quadrant operation

FIGURE 11.6
Four-quadrant DC/DC ZVS quasi-resonant Luo-converter.

TABLE 11.3

Switch Status

Circuit //Switch or Diode	Mode A (Q-I)		Mode B (Q-II)		Mode C (Q-III)		Mode D (Q-IV)	
	State-on	State-off	State-on	State-off	State-on	State-off	State-on	State-off
Circuit	Circuit 1				Circuit 2			
S_1	ON				ON			
D_1				ON				ON
S_2			ON				ON	
D_2		ON			ON			

Note: The blank status means off.

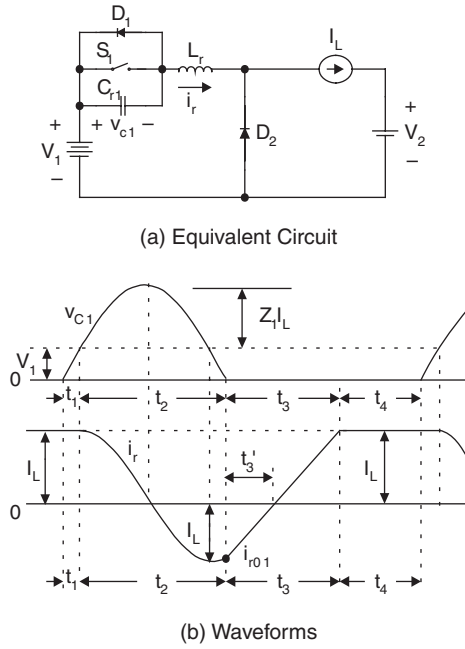


FIGURE 11.7
Mode A operation.

the input current flows through the switch S_1 and the main inductor L . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_r - C_{r1}$.

The resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_r C_{r1}}} \quad (11.60)$$

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_r}{C_{r1}}} \quad (11.61)$$

The resonant voltage (AC component) is

$$v_{c1}(t) = Z_1 I_L \sin(\omega_1 t + \alpha_1) \quad (11.62)$$

Considering the DC component V_1 , the peak voltage is

$$v_{c1-peak} = V_1 + Z_1 I_L \quad (11.63)$$

11.3.1.1 Interval $t = 0$ to t_1

Switch S_1 turns off at $t = 0$, the capacitor voltage v_{C1} increases linearly with the slope I_L/C_{r1} ; this is the voltage linear rising interval. This voltage is smaller than the source voltage V_1 . Therefore, no current flows through the diode D_2 .

When $t = t_1$, it is equal to V_1 . Therefore, the time is

$$t_1 = \frac{V_1 C_{r1}}{I_L} \quad (11.64)$$

and corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{V_1}{Z_1 I_L}\right) \quad (11.65)$$

11.3.1.2 Interval $t = t_1$ to t_2

In this period, since the voltage v_{C1} is higher than source voltage V_1 , the current flows through the diode D_2 . Circuit $L_r - C_{r1}$ resonates; this is the resonance interval. The voltage waveform is a sinusoidal function. After its peak value $v_{C1\text{-peak}}$, it descends down to zero ($t = t_2$). If the converter works in subresonance state, switch S_1 turns on at $t = t_2$. At this point we can see that the switch S_1 turns off and on at zero voltage condition. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad (11.66)$$

Simultaneously, the current i_r flows through the inductor L_r , it is a sinusoidal function as well. When $t = t_2$, the corresponding value i_{rO1} of the inductor current i_r is

$$i_{rO1} = -I_L \sin(\pi/2 + \alpha_1) = -I_L \cos \alpha_1 \quad (11.67)$$

11.3.1.3 Interval $t = t_2$ to t_3

Since the diode D_1 does not allow the resonant voltage v_{C1} to become a negative value, then $v_{C1} = 0$. The free-wheeling diode D_2 conducts and the current i_r increases linearly with the slope V_1/L_r ; this is the linear recovering interval. Because load current I_L is a constant current the current i_r increases linearly from i_{rO1} to 0 at $t = t'_3$, and $i_{rO1} = I_L$ at $t = t_3$.

$$t'_3 = -\frac{i_{rO1} L_r}{V_1} \quad (11.68)$$

and

$$t_3 = \frac{(I_L - i_{rO1})L_r}{V_1} = \frac{I_L(1 + \cos \alpha_1)L_r}{V_1} \quad (11.69)$$

11.3.1.4 Interval $t = t_3$ to t_4

In this period the load current is supplied by the source. Diode D_2 is blocked until $t = t_4$; this is the normal switch-on interval. The output current is equal to the main inductor current I_L , so the average input current I_1 is

$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T} \int_{t_3}^{t_4} i_r dt \approx \frac{1}{T} (I_L t_4) = \frac{t_4}{T} I_L \quad (11.70)$$

Therefore,

$$t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1} \quad (11.71)$$

We have the conduction duty

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \quad (11.72)$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \quad (11.73)$$

and corresponding frequency is

$$f = 1 / T \quad (11.74)$$

11.3.2 Mode B

Mode B is a ZVS boost converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.8](#). There are four time regions for the switch-off and -on period. The conduction duty cycle is $kT = (t_3 + t_4)$, but the output current only flows through the source V_1 in the period t_4 . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_r - C_{r2}$.

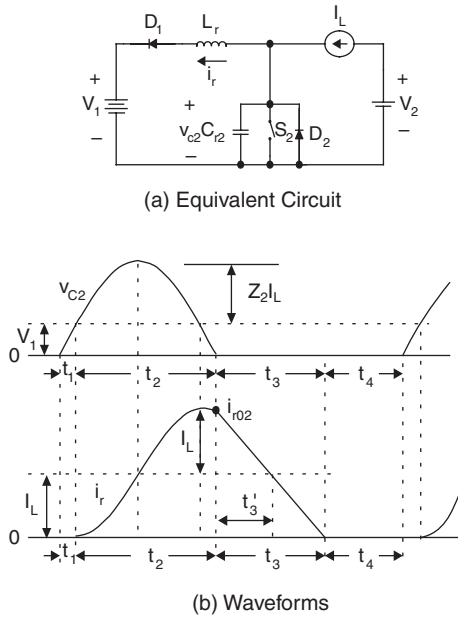


FIGURE 11.8
Mode B operation.

The resonance frequency is

$$\omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \quad (11.75)$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_r}{C_{r2}}} \quad (11.76)$$

The resonant voltage (AC component) is

$$v_{C2}(t) = Z_2 I_L \sin(\omega_2 t + \alpha_2) \quad (11.77)$$

Considering the DC component V_1 , the peak current is

$$v_{C2-peak} = V_1 + Z_2 I_L \quad (11.78)$$

11.3.2.1 Interval $t = 0$ to t_1

Switch S_2 turns off at $t = 0$, the capacitor voltage v_{C2} increases linearly with the slope I_L/C_{r2} . This voltage is equal to V_1 when $t = t_1$.

$$t_1 = \frac{V_1 C_{r2}}{I_L} \quad (11.79)$$

and corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{V_1}{Z_2 I_L}\right) \quad (11.80)$$

11.3.2.2 Interval $t = t_1$ to t_2

In this period the voltage v_{C2} is higher than the source voltage V_1 . Circuit $L_r - C_{r2}$ resonates. The voltage waveform is a sinusoidal function. After its peak value, it descends down to 0 when $t = t_2$. If the converter works in subresonance state, switch S_2 turns on at $t = t_2$. Until this point we can see that the switch S_2 turns-off and -on at zero voltage condition. This period length is

$$t_2 = \frac{1}{\omega_2} (\pi + \alpha_2) \quad (11.81)$$

Simultaneously, the inductor current i_r flows through inductor L_r , it is a sinusoidal function as well. When $t = t_2$, the corresponding value i_{rO2} of the inductor current i_r is

$$i_{rO2} = I_L [1 + \sin(\pi / 2 + \alpha_2)] = I_L (1 + \cos \alpha_2) \quad (11.82)$$

11.3.2.3 Interval $t = t_2$ to t_3

Since the diode D_2 does not allow the resonant voltage to become a negative value, the voltage across the capacitor C_{r2} will be 0. The inductor current i_r decreases linearly with the slope $-V_1/L_r$. Because load current I_L is a constant current, the current i_r decreases linearly from i_{rO2} to I_L at $t = t'_3$, and $i_r = 0$ at $t = t_3$.

$$t'_3 = \frac{(i_{rO2} - I_L)L_r}{V_1} \quad (11.83)$$

$$t_3 = \frac{i_{rO2} L_r}{V_1} \quad (11.84)$$

11.3.2.4 Interval $t = t_3$ to t_4

In this period the switch S_2 is on. Load current I_L does not flow through the source. Ignoring the power losses, and $I_2 = I_L$ we have the output average current I_1 :

$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T} \int_{t_1}^{t_3} i_r dt \approx \frac{1}{T} [I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L \quad (11.85)$$

or

$$\frac{V_2}{V_1} = \frac{1}{T} (t_2 + t_3) = \frac{t_2 + t_3}{t_1 + t_2 + t_3 + t_4} \quad (11.86)$$

Therefore,

$$t_4 = \left(\frac{V_1}{V_2} - 1 \right) (t_2 + t_3) - t_1 \quad (11.87)$$

We have the conduction duty

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \quad (11.88)$$

The whole repeating period is

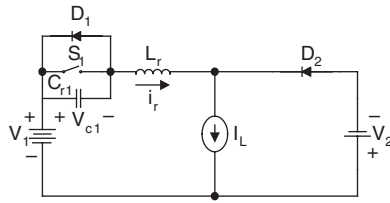
$$T = t_1 + t_2 + t_3 + t_4 \quad (11.89)$$

and corresponding frequency is

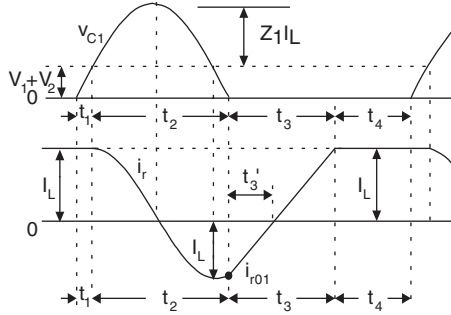
$$f = 1 / T \quad (11.90)$$

11.3.3 Mode C

Mode C is a ZVS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.9](#). There are four time regions for the switch-off and -on period. The conduction duty cycle is $kT = (t_3 + t_4)$ when the input current I_1 flows through the switch S_1 and the main inductor L . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_r - C_{r1}$.



(a) Equivalent Circuit



(b) Waveforms

FIGURE 11.9
Mode C operation.

The resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_r C_{r1}}} \quad (11.91)$$

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_r}{C_{r1}}} \quad (11.92)$$

The resonant voltage (AC component) is

$$v_{c1}(t) = Z_1 I_L \sin(\omega_1 t + \alpha_1) \quad (11.93)$$

Considering the DC component V_1 , the peak voltage is

$$v_{c1-peak} = V_1 + V_2 + Z_1 I_L \quad (11.94)$$

11.3.3.1 Interval $t = 0$ to t_1

Switch S_1 turns off at $t = 0$, the capacitor voltage v_{C1} increases linearly with the slope I_L/C_{r1} . This voltage v_{C1} is smaller than $(V_1 + V_2)$. Therefore, no current flows through the diode D_2 . When $t = t_1$, it is equal to $(V_1 + V_2)$. Therefore,

$$t_1 = \frac{(V_1 + V_2)C_{r1}}{I_L} \quad (11.95)$$

and corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_1 I_L}\right) \quad (11.96)$$

11.3.3.2 Interval $t = t_1$ to t_2

In this period, since the voltage v_{C1} is higher than source voltage V_1 , the current flows through the diode D_2 . Circuit $L_r - C_{r1}$ resonates. The voltage waveform is a sinusoidal function. After its peak value $v_{C1-\text{peak}}$ it descends down to zero ($t = t_2$). If the converter works in subresonance state, switch S_1 turns on at $t = t_2$. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad (11.97)$$

Simultaneously, the current i_r flows through the inductor L_r , it is a sinusoidal function as well. When $t = t_2$, the corresponding value i_{rO1} of the inductor current i_r is

$$i_{rO1} = -I_L \sin(\pi/2 + \alpha_1) = -I_L \cos \alpha_1 \quad (11.98)$$

11.3.3.3 Interval $t = t_2$ to t_3

Since the diode D_1 does not allow the resonant voltage v_{C1} to become a negative value, then $v_{C1} = 0$. The free-wheeling diode D_2 conducts and the current i_r increases linearly with the slope $(V_1 + V_2)/L_r$. Because load current I_L is a constant current the current i_r increases linearly from i_{rO1} to 0 at $t = t'_3$ and $i_{rO1} = I_L$ at $t = t_3$.

$$t'_3 = -\frac{i_{rO1}L_r}{V_1 + V_2} \quad (11.99)$$

and

$$t_3 = \frac{(I_L - i_{rO1})L_r}{V_1 + V_2} = \frac{I_L(1 + \cos \alpha_1)L_r}{V_1 + V_2} \quad (11.100)$$

11.3.3.4 Interval $t = t_3$ to t_4

In this period the load current is supplied by the source. Diode D_2 is blocked until $t = t_4$. The output current is equal to the main inductor current I_L , so the average input current I_1 is

$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T} \int_{t_3}^{t_4} i_r dt \approx \frac{1}{T} (I_L t_4) = \frac{t_4}{T} I_L \quad (11.101)$$

and

$$I_2 = \frac{1}{T} \int_{t_2}^{t_3} (I_L - i_r) dt \approx \frac{t_2 + t_3}{T} I_L \quad (11.102)$$

Therefore,

$$t_4 = \frac{V_2(t_2 + t_3)}{V_1} \quad (11.103)$$

We have the conduction duty

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \quad (11.104)$$

The whole repeating period is

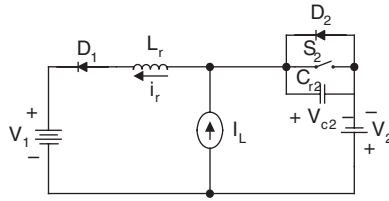
$$T = t_1 + t_2 + t_3 + t_4 \quad (11.105)$$

and corresponding frequency is

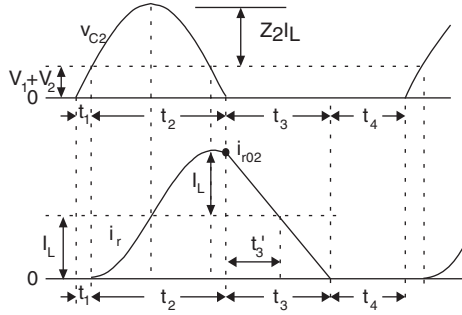
$$f = 1/T \quad (11.106)$$

11.3.4 Mode D

Mode D is a cross ZVS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in [Figure 11.10](#). There are four time



(a) Equivalent Circuit



(b) Waveforms

FIGURE 11.10
Mode D operation.

regions for the switch-off and -on period. The conduction duty cycle is $kT = (t_3 + t_4)$, but the output current only flows through the source V_1 in the period t_4 . The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_r - C_{r2}$.

The resonance frequency is

$$\omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \quad (11.107)$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_r}{C_{r2}}} \quad (11.108)$$

The resonant voltage (AC component) is

$$v_{C2}(t) = Z_2 I_L \sin(\omega_2 t + \alpha_2) \quad (11.109)$$

Considering the DC component V_1 , the peak current is

$$v_{C2-peak} = V_1 + Z_2 I_L \quad (11.110)$$

11.3.4.1 Interval $t = 0$ to t_1

Switch S_2 turns off at $t = 0$, the capacitor voltage v_{C2} increases linearly with the slope I_L/C_{r2} . It is equal to $(V_1 + V_2)$ when $t = t_1$.

$$t_1 = \frac{(V_1 + V_2)C_{r2}}{I_L} \quad (11.111)$$

and corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_2 I_L}\right) \quad (11.112)$$

11.3.4.2 Interval $t = t_1$ to t_2

In this period the voltage v_{C2} is higher than the sum-voltage $(V_1 + V_2)$. Circuit $L_r - C_{r2}$ resonates. The voltage waveform is a sinusoidal function. After its peak value, it descends down to 0 when $t = t_2$. If the converter works in subresonance state, switch S_2 turns on at $t = t_2$. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad (11.113)$$

Simultaneously, the inductor current i_r flows through inductor L_r , it is a sinusoidal function as well. When $t = t_2$, the corresponding value i_{rO2} of the inductor current i_r is

$$i_{rO2} = I_L[1 + \sin(\pi/2 + \alpha_2)] = I_L(1 + \cos \alpha_2) \quad (11.114)$$

11.3.4.3 Interval $t = t_2$ to t_3

Since the diode D_2 does not allow the resonant voltage to become a negative value, the voltage across the capacitor C_{r2} will be 0. The inductor current i_r decreases linearly with the slope $-(V_1 + V_2)/L_r$. Because the main inductor current I_L is a constant current, the current i_r decreases linearly from i_{rO2} to I_L at $t = t_3'$ and $i_r = 0$ at $t = t_3$.

$$t_3' = \frac{(i_{rO2} - I_L)L_r}{V_1 + V_2} \quad (11.115)$$

$$t_3 = \frac{i_{rO2}L_r}{V_1 + V_2} \quad (11.116)$$

11.3.4.4 Interval $t = t_3$ to t_4

In this period since the switch S_2 is on, the main inductor current I_L does not flow through the source. Ignoring the power losses, we have the output average current I_L :

$$I_1 = \frac{1}{T} \int_{t_1}^{t_3} i_r dt \approx \frac{1}{T} [I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L \quad (11.117)$$

and

$$I_2 = \frac{1}{T} \int_{t_3}^{t_4} i_r dt \approx \frac{1}{T} (I_L t_4) = \frac{t_4}{T} I_L \quad (11.118)$$

Therefore,

$$t_4 = \frac{V_1}{V_2} (t_2 + t_3) \quad (11.119)$$

We have the conduction duty

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \quad (11.120)$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \quad (11.121)$$

and corresponding frequency is

$$f = 1 / T \quad (11.122)$$

TABLE 11.4
Experimental Results for Different Frequencies

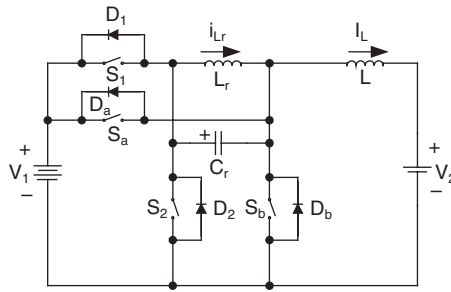
Mode	$f(\text{kHz})$	$L_{r1} (\mu\text{H})$	$C_{r1} = C_{r2} (\mu\text{F})$	$I_I (\text{A})$	$I_O (\text{A})$	$I_L (\text{A})$	$P_I (\text{W})$	$P_O (\text{W})$	$\eta (\%)$	$\text{PD} (\text{W}/\text{in}^3)$
A	23	4	1	17.16	25	25	720.8	700	97.1	17.76
A	23.5	4	1	16.99	25	25	713.7	700	98.1	17.67
A	24	4	1	16.82	25	25	706.6	700	99	17.58
B	54	4	1	25	16.13	25	700	677.6	96.8	17.22
B	54.5	4	1	25	16.28	25	700	683.8	97.7	17.3
B	55	4	1	25	16.43	25	700	690.1	98.6	17.38
C	44	4	1	17.64	24.27	45	740.9	679.6	91.7	17.76
C	44.5	4	1	17.32	24.55	45	727.6	687.5	94.5	17.69
C	45	4	1	17.01	24.83	45	714.5	695.2	97.3	17.62
D	29.5	4	1	26.65	16.27	45	746.3	683.5	91.6	17.87
D	30	4	1	26.34	16.55	45	737.6	695.1	94.2	17.91
D	30.5	4	1	26.28	16.83	45	735.9	706.7	96	18.03

11.3.5 Experimental Results

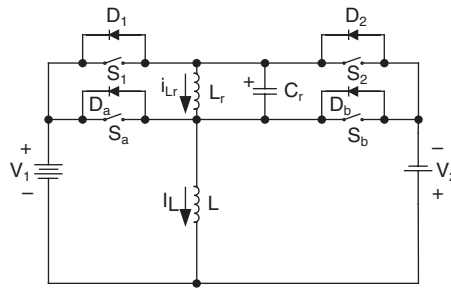
A testing rig with a battery of ± 28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are: $V_1 = 42$ V and $V_2 = \pm 28$ V, $L = 30 \mu\text{H}$, $L_r = 4 \mu\text{H}$, $C_{r1} = C_{r2} = 1 \mu\text{F}$; the volume is 40 in^3 . The experimental results are shown in Table 11.4. The average power transfer efficiency is higher than 96%, and total average PD is $17.6 \text{ W}/\text{in}^3$. This figure is much higher than that of the classical converters whose PD is usually less than $5 \text{ W}/\text{in}^3$. Since the switch frequency is low ($f < 56 \text{ kHz}$) and this converter works at the mono-resonance frequency, the components of the high-order harmonics are small. Applying FFT analysis, the THD is very small, so that the EMI is weak, and the EMS and EMC are reasonable.

11.4 Multiple-Quadrant Zero-Transition DC/DC Luo-Converters

Zero-transition (ZT) technique significantly reduces the power losses across the switches during switch-on and -off. Unfortunately, the literature discusses the converters only working at single quadrant operation. The four-quadrant ZT DC/DC Luo-converters perform soft switch four-quadrant operation without significant voltage and current stresses. They effectively reduce the power losses and greatly increase the power transfer efficiency. These converters are shown in [Figure 11.11a and b](#). Circuit 1 implements the operation in quadrants I and II, circuit 2 implements the operation in quadrants III and IV. Circuit 1 and circuit 2 can be converted each other via an auxiliary switch. Each circuit consists of one main inductor L and two main



(a) Circuit 1 for Modes A & B Operation



(b) Circuit 2 for Modes C & D Operation

FIGURE 11.11

Four-quadrant zero-transition DC/DC Luo-converters.

switches. The source and load voltages are usually constant, e.g., $V_1 = 42$ V and $V_2 = \pm 28$ V. There are four modes of operation:

1. Mode A (quadrant I): electrical energy is transferred from V_1 side to V_2 side.
2. Mode B (quadrant II): electrical energy is transferred from V_2 side to V_1 side.
3. Mode C (quadrant III): electrical energy is transferred from V_1 side to $-V_2$ side.
4. Mode D (quadrant IV): electrical energy is transferred from $-V_2$ side to V_1 side.

Each mode has two states: *on* and *off*. The switch and diode status of each state for modes A and B are shown in Table 11.5; the status of each state for modes C and D are shown in Table 11.6.

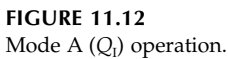
The equivalent circuits for modes A, B, C, and D are shown in Figures 11.12, 11.14, 11.16, and 11.18. The corresponding waveforms for each mode are shown in Figures 11.13, 11.15, 11.17, and 11.19 respectively.

Switch/Diode Status

Note: The blank status means off referring to circuit 1 of Figure 11.11a.

Switch/Diode Status

Note: The blank status means off referring to circuit 2 of [Figure 11.11b](#).



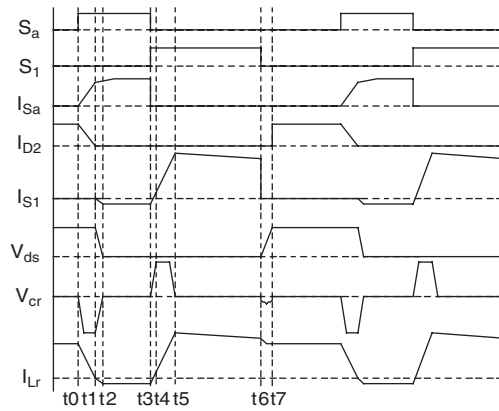


FIGURE 11.13
Waveforms of mode A (Q_1).

11.4.1 Mode A (Quadrant I Operation)

Mode A performs quadrant I operation. The equivalent circuit for Mode A, is shown in Figure 11.12. The corresponding waveforms are shown in Figure 11.13.

Stage 1 ($t_0 - t_1$): prior to t_0 , S_1 and S_a are all off. The circuit current is freewheeling through the antiparallel diode D_b and D_2 . C_r voltage is zero, $I_L = I_{Lr} + I_{D_b}$. At t_0 , the auxiliary switch S_a is turned on with zero current. Capacitor C_r is charged in reverse, so that diode D_b is reverse-biased in soft commutation. The current of L_r decreases linearly while the current of S_a increases gradually. At $t = t_1$, the current of L_r falls to zero; D_2 is turned off with soft commutation. Meanwhile, current of S_a reaches to I_L . The current of resonant inductor L_r is

$$i_{Lr} = \frac{V_1}{L_r} t$$

The time interval of the first stage Δt_1 is given by equation

$$\Delta t_1 = \frac{I_L L_r}{V_1} \quad (11.123)$$

Stage 2 ($t_1 - t_3$): the main switch S_1 junction capacitor C_j (not shown in Figure 11.12) discharges through L_r , S_a . Capacitor C_r also discharges through L_r . V_{cr} , and V_{ds} fall to zero rapidly at t_2 . Thereafter, the antiparallel diode of S_1 starts to conduct and a small reverse current flows through L_r . The resonant time interval of stage 2, Δt_2 , is given by

$$\Delta t_2 = \frac{\pi}{2} \sqrt{L_r C_j} \quad (11.124)$$

Stage 3 ($t_2 - t_3$): at t_3 , S_1 is turned on with zero current and zero voltage. At the same moment, turn off S_a . It should be noted that the turn on/off point is not critical. S_1 and S_a could be turn on and off prior to t_2 . If so, t_2 does not exist in the stage. Therefore,

$$\Delta t_3 = t_{Sa-on} - \Delta t_1 - \Delta t_2 \quad (11.125)$$

Stage 4 ($t_3 - t_4$): when S_a is turned off, I_L charges C_r and L_r through the conducted S_1 . The voltage of C_r increases gradually, enabling S_a to be turned off with zero voltage. After i_{L_r} reaches I_L , capacitor C_r starts to discharge through L_r . At $t = t_4$, V_{cr} reaches zero again.

$$\Delta t_4 = \frac{V_1 C_r}{I_L} \quad (11.126)$$

Stage 5 ($t_4 - t_5$): During this period, the circuit current flows through main switch S_1 , and inductor L_r , L , like the conventional PWM converter. The length is determined by the control of the PWM signal.

$$\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r} \quad (11.127)$$

Stage 6 ($t_5 - t_6$): at t_5 , main switch S_1 is turned off. Inductor and capacitor C_r are in resonance. The voltage of C_r increases gradually at first, so that the voltage across the main switch S_1 rises gradually. S_1 is therefore turned off with zero voltage. At t_6 , the voltage of C_r becomes zero; D_2 and D_b start to conduct. The time interval is given by

$$\Delta t_6 = kT - \Delta t_4 - \Delta t_5 \quad (11.128)$$

Stage 7 ($t_6 - t_7$): During this period, the circuit current is freewheeling through D_2 and D_{br} , like the conventional PWM converter.

$$\Delta t_7 = \pi \sqrt{L_r C_r} \quad (11.129)$$

Stage 8 ($t_7 - t_0$): at t_0 , S_a is turned on once more, to start the next switch cycle. The length of this period is determined by the control of the PWM.

$$\Delta t_8 = (1 - k)T - t_{Sa-on} - \Delta t_7 \quad (11.130)$$

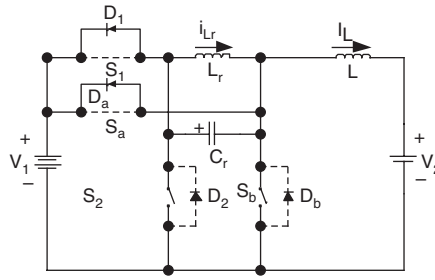


FIGURE 11.14
Mode B (Q_{II}) operation.

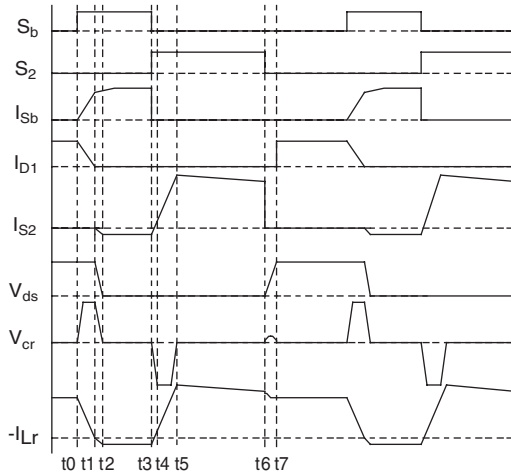


FIGURE 11.15
Waveforms of mode B (Q_{II}).

11.4.2 Mode B (Quadrant II Operation)

Mode B performs quadrant II operations. The equivalent circuit for mode B, is shown in Figure 11.14. The operational process is analogous to mode A operation. The corresponding waveforms are shown in Figure 11.15. The calculation formulae for mode B are listed below:

$$\Delta t_1 = \frac{I_L L_r}{V_1} \quad \Delta t_2 = \frac{\pi}{2} \sqrt{L_r C_j}$$

$$\Delta t_3 = t_{Sb-on} - \Delta t_1 - \Delta t_2 \quad \Delta t_4 = \frac{V_1 C_r}{I_L}$$

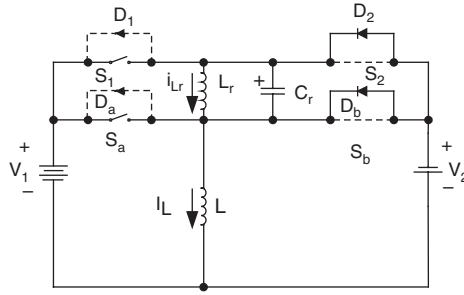


FIGURE 11.16
Mode C (Q_{III}) operation.

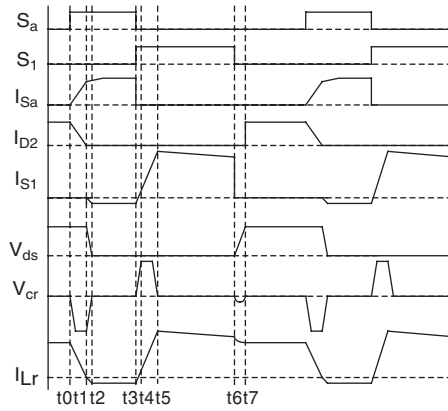


FIGURE 11.17
Waveforms of mode C (Q_{III}).

$$\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r} \quad \Delta t_6 = kT - \Delta t_4 - \Delta t_5$$

$$\Delta t_7 = \pi \sqrt{L_r C_r} \quad \Delta t_8 = (1 - k)T - t_{Sb-on} - \Delta t_7$$

11.4.3 Mode C (Quadrant III Operation)

Mode C performs quadrant III operation. The equivalent circuit for mode C, is shown in Figure 11.16. The operational process is analogous to mode A operation. The corresponding waveforms are shown in Figure 11.17. The calculation formulae of mode C are listed below:

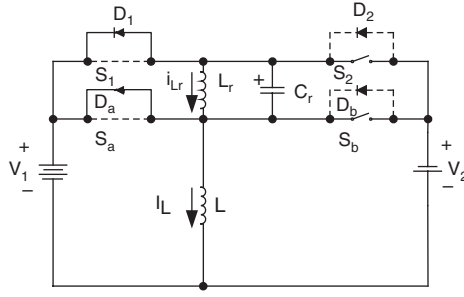


FIGURE 11.18
Mode D (Q_{IV}) operation.

$$\Delta t_1 = \frac{I_L L_r}{V_1 + V_2}$$

$$\Delta t_2 = \frac{\pi}{2} \sqrt{L_r C_j}$$

$$\Delta t_3 = t_{Sa-on} - \Delta t_1 - \Delta t_2$$

$$\Delta t_4 = \frac{V_1 + V_2}{I_L} C_r$$

$$\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r}$$

$$\Delta t_6 = kT - \Delta t_4 - \Delta t_5$$

$$\Delta t_7 = \pi \sqrt{L_r C_r}$$

$$\Delta t_8 = (1 - k)T - t_{Sa-on} - \Delta t_7$$

11.4.4 Mode D (Quadrant IV Operation)

Mode D performs in quadrant IV operation. The equivalent circuit for mode D, is shown in Figure 11.18. The operational process is analogous to mode B operation. The corresponding waveforms are shown in Figure 11.19. The calculation formulae of mode D are listed below:

$$\Delta t_1 = \frac{I_L L_r}{V_1 + V_2}$$

$$\Delta t_2 = \frac{\pi}{2} \sqrt{L_r C_j}$$

$$\Delta t_3 = t_{Sb-on} - \Delta t_1 - \Delta t_2$$

$$\Delta t_4 = \frac{V_1 + V_2}{I_L} C_r$$

$$\Delta t_5 = \frac{\pi}{2} \sqrt{L_r C_r}$$

$$\Delta t_6 = kT - \Delta t_4 - \Delta t_5$$

$$\Delta t_7 = \pi \sqrt{L_r C_r}$$

$$\Delta t_8 = (1 - k)T - t_{Sb-on} - \Delta t_7$$

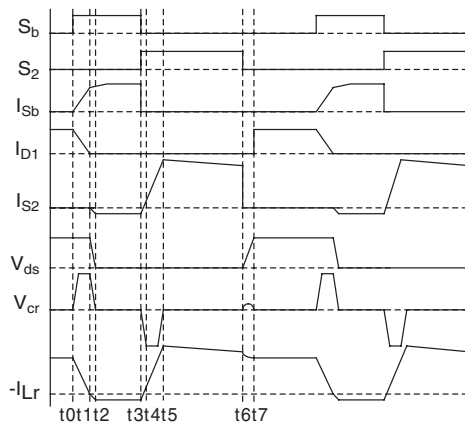


FIGURE 11.19
Waveforms of mode D (Q_{IV}).

11.4.5 Simulation Results

PSpice is a popular simulation method to test and verify electronic circuit design. In order to implement this ZV-ZCS two-quadrant DC/DC converter with 3 kW delivery, the rig of a modern car battery ± 28 VDC as a load and a 42 VDC as a source power supply was tested. The testing conditions are $V_1 = 42$ V and $V_2 = 28$ V, $L_r = 2 \mu\text{H}$, $C_r = 0.8$ nF, and $L = 550 \mu\text{H}$, $f = 100$ kHz. The simulation result for Q_I is shown in Figure 11.20, the simulation result for Q_{II} is shown in Figure 11.21. From these waveform and data, we can see that the main switches in the converter are switched on at ZC and ZVS condition; switched off at ZVS condition. Moreover, all the auxiliary switches and diode are operated under soft commutation. The testing conditions are $V_1 = 42$ V and $V_2 = -28$ V, $L_r = 2 \mu\text{H}$, $C_r = 0.8$ nF, and $L = 550 \mu\text{H}$, $f = 100$ kHz. The simulation results for Q_{III} are shown in Figure 11.22, the simulation results for Q_{IV} are shown in Figure 11.23. From these waveforms we can see that the main switches in the converter are switched on at ZC and ZVS condition; switched off at ZVS condition. Moreover, all the auxiliary switches and diodes are operated under soft commutation.

11.4.6 Experimental Results

A testing rig battery of ± 28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are: $V_1 = 42$ V and $V_2 = \pm 28$ V, $L = 30 \mu\text{H}$, $L_{r1} = L_{r2} = 1 \mu\text{H}$, $C_r = 4 \mu\text{F}$, $I_L = 25$ A (for Q_I and Q_{II})/35 A (for Q_{III} and Q_{IV}) and the volume is 40 in^3 . The experimental results are shown in Table 11.7. The average power transfer efficiency is higher than 89.7% and the total average PD is 17.5 W/in^3 . This figure is much higher than the classical converters whose PD is usually less than 5 W/in^3 . Since the switch

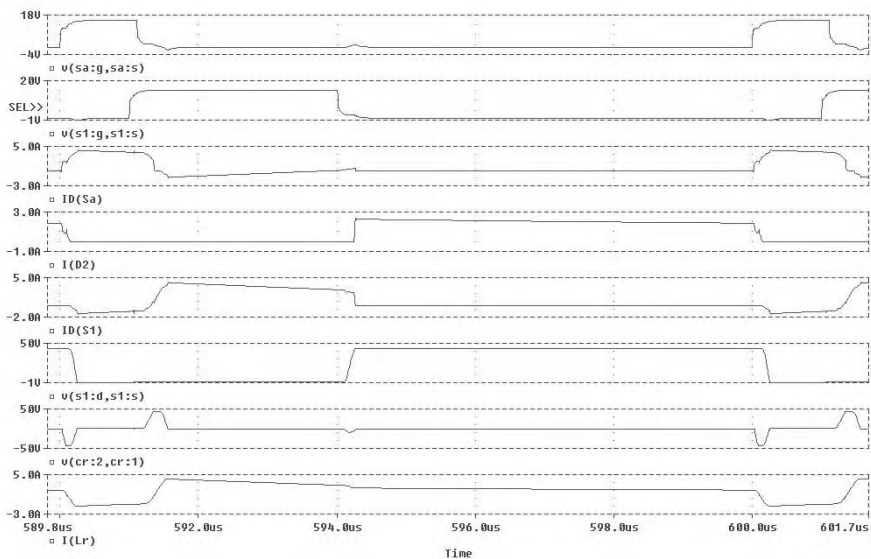


FIGURE 11.20

Simulation result for ZV-ZCS mode A operation ($f = 100 \text{ kHz}$; $k = 30\%$).

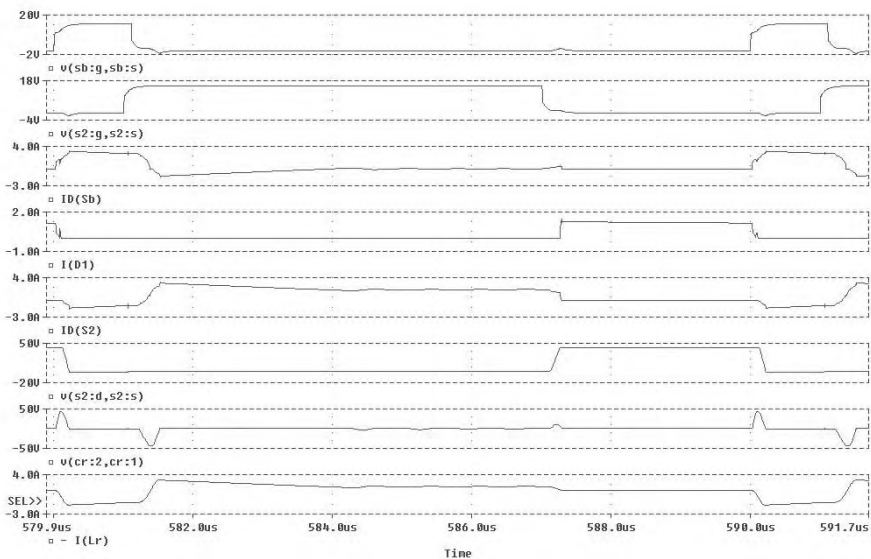


FIGURE 11.21

Simulation result for ZV-ZCS mode B operation ($f = 100 \text{ kHz}$; $k = 60\%$).

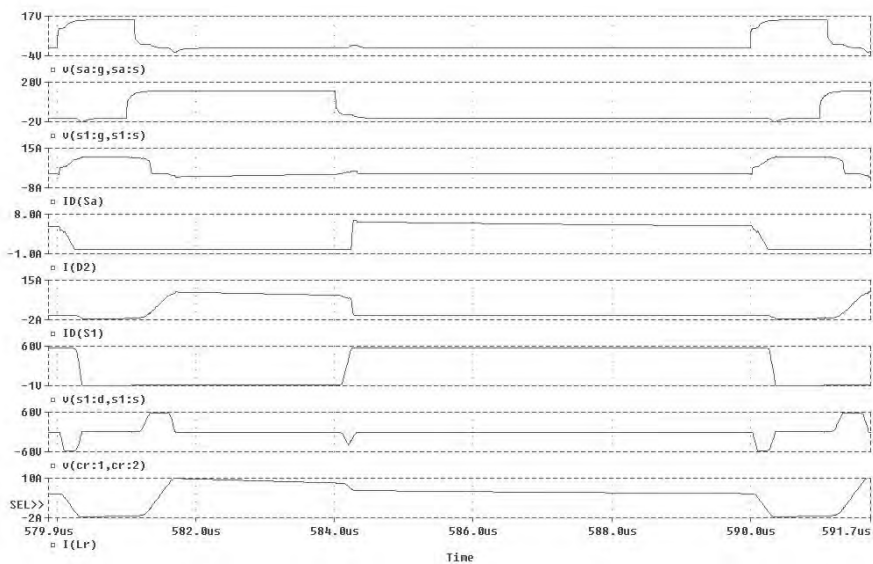


FIGURE 11.22

Simulation result for ZV-ZCS mode C operation ($f = 100 \text{ kHz}$; $k = 30\%$).

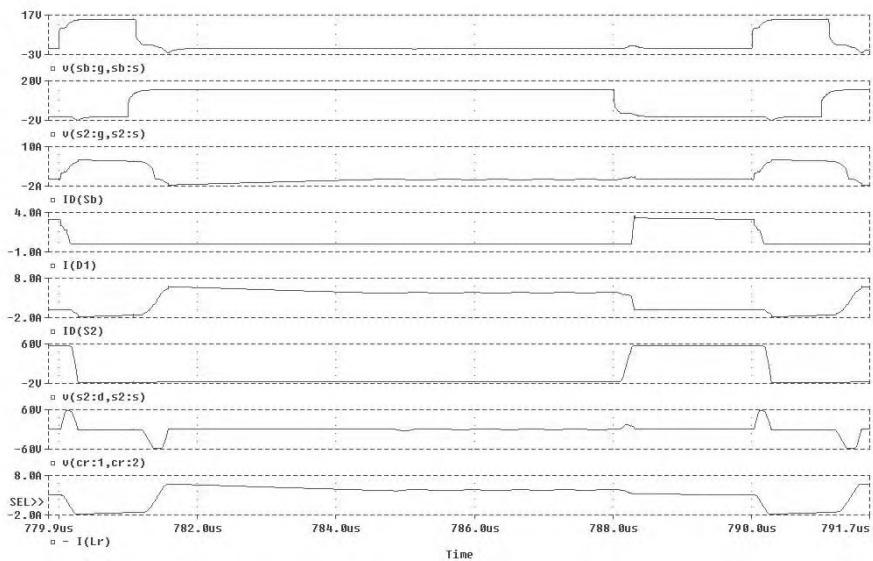


FIGURE 11.23

Simulation result for ZV-ZCS mode D operation ($f = 100 \text{ kHz}$; $k = 70\%$).

TABLE 11.7

Experimental Results for Different Frequencies

Mode	$f(\text{kHz})$	$L_{r1}=L_{r2} (\mu\text{H})$	$C_r (\mu\text{F})$	$I_l (\text{A})$	$I_o (\text{A})$	$I_L (\text{A})$	$P_l (\text{W})$	$P_o (\text{W})$	$\eta (\%)$	$\text{PD}(\text{W/in}^3)$
A	20.5	1	4	16.98	25	25	713	700	98.2	17.66
A	21	1	4	17.4	25	25	730.6	700	95.8	17.88
A	21.5	1	4	17.81	25	25	748	700	93.5	18.1
B	16.5	1	4	25	16.4	25	700	688.8	98.4	17.36
B	17	1	4	25	16.2	25	700	680.4	97.2	17.25
B	17.5	1	4	25	15.97	25	700	670.1	95.8	17.13
C	18.3	1	4	16.24	24.03	35	682.1	672.8	98.6	16.94
C	18.5	1	4	16.42	23.91	35	689.6	669.4	97.1	17
C	18.7	1	4	16.59	23.79	35	696.8	666.1	95.6	17.04
D	37.2	1	4	24.42	16.02	35	683.8	672.7	98.4	16.95
D	37.5	1	4	24.62	15.87	35	689.4	666.4	96.7	16.94
D	37.8	1	4	24.81	15.71	35	694.7	660	95	16.93

frequency and conduction duty k can be adjusted individually, we chose $f = 100 \text{ kHz}$ and a suitable conduction duty cycle k to obtain the proper operation state.

11.4.7 Design Considerations

In a practical design, for ease of implementation, the control of the two switches can adopt the constant time-delay method:

1. Turn-on of the main switch should delay turn-on of the auxiliary switch at least by ΔT_{ONmin} . The auxiliary switch could be turned off simultaneously with the turn-on of the main switch. But it is better to turn off S_a shortly after turn-on of the main switch to secure soft turnoff of the auxiliary switch.
2. For prompt soft turn-off of main switch (S_1 or S_2) and energy recovery, turn-off of the auxiliary switch should precede turn-off of the main switch by a minimum time of ΔT_{OFFmin} . This means that for prompt soft switch, the above constraint should be met under the minimum duty cycle k_{min} . The simple timing constraints are calculated as follows:

$$T_D \geq T_{ONmin} = \Delta t_1 + \Delta t_2 = \frac{I_L L_r}{V_1} + \frac{\pi}{2} \sqrt{L_r C_j} \quad (11.131)$$

$$T_P \geq \Delta T_{OFFmin} = \frac{C_r V_1}{i_p} + \frac{L_r}{V_1} i_p \quad (11.132)$$

$$i_p = \sqrt{I_L^2 + \frac{V_1^2}{\rho}} \quad \rho = \sqrt{\frac{L_r}{C_j}} \quad (11.133)$$

Where C_j is the junction capacitor across the main switch's drain and source, T_D is the time that turn-on of main switch delays turn-on of auxiliary switch. T_p is the time that turn-off of auxiliary switch precedes turn-off of main switch. i_p is L_r peak current.

For engineering implementation, as no capacitor is directly paralleled with the main switch, the time interval Δt_2 is very small; moreover, the turn-on loss caused by the junction capacitor is minimum if the main switch is turned-on before V_{ds} falls to zero. So, Δt_2 in Equation (11.131) can be ignored for simple design:

$$T_D \geq T_{ON\min} = \Delta t_1 = \frac{I_L L_r}{V_1} \quad (11.134)$$

To secure the soft switch under minimum duty cycle k_{\min} , Equation (11.132) can be expressed as:

$$k_{\min} T_s \geq \Delta T_{OFF\min} = \frac{C_r V_1}{i_p} + \frac{L_r}{V_1} i_p \quad (11.135)$$

To achieve the similar conversion ratios of its hard switch PWM counterpart, the commutation transition i.e., $\Delta T_{ON\min}$ is normally set as 10 to 15% cycle in practical design:

$$T_{ON\min} = \frac{I_{L\max} L_r}{V_1} \leq (10\% - 15\%) T_s \quad (11.136)$$

From Equation (11.136) L_r can be obtained, for practical implementation, turn-on of the main switch delays turn-on of the auxiliary switch a constant time T_D :

$$T_D = \frac{I_{L\max} L_r}{V_1} \quad (11.137)$$

To reduce the auxiliary switch's conduction loss, the auxiliary switch is turned off right after turn-on of the main switch. From Equation (11.133), it is obvious that the peak current of L_r does not relate to C_r . So, C_r can be set large enough to reduce the turn-off loss of the main switch most effectively. But C_r should meet the constraint of Equation (11.135) as well.

Compared with other soft-switch circuits, besides the soft switch of the auxiliary switch, the proposed circuit possesses the simplicity in topology. Another merit is that C_r is not directly paralleled with the main switch. It not only provides soft turn-off for all the switches, but also does not discharge to L_r . A lower peak current in the auxiliary switch could, therefore,

be expected, particularly in cases where a small snubber inductor is used in high-frequency operation. Moreover, as the charge of C_r does not increase L_r current, the design trade-off between C_r and current stress on the auxiliary switch does not exist, and the design of L_r and C_r become easy, as the above design analysis indicates. Also, with the help of inductor L_r , the reverse-recovery current of the main diode is effectively minimized.

It should be also noted here that the turn-on point of the main switch is not critical. The main switch could be turned on prior to t_2 , because the turn-on loss caused by the junction capacitor is very small.

The control principle adopted here is simple, as it does not need the cross-zero voltage detection of the main switch. So it is easy to implement, but it has its limitations in light-load or no-load operation. Since the duty cycle of the main switch may be smaller than the duty cycle of the auxiliary switch at no load or light load, the constant duty cycle of the auxiliary switch will charge up the output capacitor without control. In such a case, certain current or voltage cross-zero detection is required to adjust the duty cycle of the auxiliary switch. On the other hand, the conduction loss is increased, as the auxiliary switch is not optimized with the minimum conduction at light load by using this control method.

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Synchronous Rectifier DC/DC Converters

The global merchant dollar market for DC/DC converters is projected to increase from about \$3.6 billion in 2001 to about \$6.0 billion in 2006, a compound annual growth rate of 10.6%. North American sales of DC/DC converters in networking and telecom equipment are expected to grow from \$2.3 billion in 1999 to \$4.6 billion in 2004, a yearly compounded growth rate of 15.3%. The first quarter of 1995 was the first time that shipments of 3.3 V microprocessor and memory integrated chips (ICs) exceeded the shipments of 5 V parts. Once this transition occurred in memories and microprocessors, the demand for low-voltage power conversion began to grow at an increasing rate. The primary application of DC/DC converters is in computer power supplies and communication equipment.

The computer power supply shift from 5 V to 3.3 V digital IC has taken over 5 years to occur, from the first indication that voltages below 5 V would be needed until the realization of volume sales. Now that the 5 V barrier has been broken, the trend toward lower and lower voltages is accelerating. Within 2 years, 2.5 V parts are expected to become common with the introduction of the next-generation microprocessors. In fact, current plans for next-generation microprocessors call for a dual voltage of 1.5/2.5 V with 1.5 V used for the memory bus and 2.5 V used for logic functions. Within another few years, voltages are expected to move as low as 0.9 V, with mainstream, high-volume parts operating at 1.5 V.

A low-voltage plus high-current DC power supply is urgently required in the next-generation computer and communications equipment. The first idea is to use a forward converter, refer to [Figure 1.26](#), which can perform low-voltage plus high-current output voltage. A modified circuit with dynamic clamp circuit is shown in [Figure 12.1](#). The two diodes D_1 and D_2 can be normal rectifier diode, rectifier Schottky diode, or MOSFET. [Figure 12.2](#) shows the efficiency gain of the following three types of forward converters needed to construct a low-voltage high-current power supply:

- Forward converter using traditional diodes
- Forward converter using Schottky diode
- Synchronous rectifier using low forward-resistance MOSFET

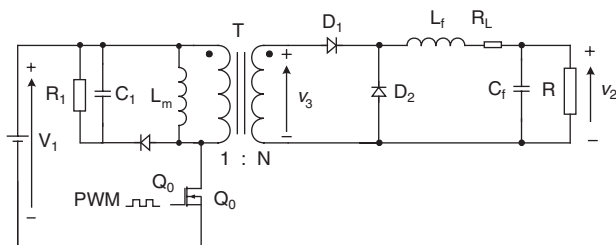


FIGURE 12.1
Forward converter with dynamic clamp circuit.

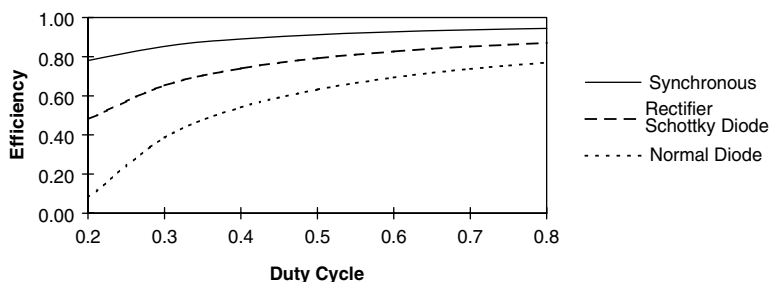


FIGURE 12.2
Efficiencies of different types of forward converter.

As the operating voltages ratchet downward, the design of rectifiers requires more attention because the devices forward-voltage drop constitutes an increasing fraction of the output voltage. The forward-voltage drop across a switch-mode rectifier is in series with the output voltage, so losses in this rectifier will almost entirely determine its efficiency. The synchronous rectifier circuit has been designed primarily to reduce this loss.

12.1 Introduction

A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. At 3.3 V, the traditional diode-rectifier loss is significant with very low efficiency (say less than 70%). For step-down regulators with a 3.3 V output and 12 V battery input voltage, a 0.4 V forward voltage of a Schottky diode represents a typical efficiency penalty of about 12%, aside from other loss mechanisms. The losses are not as bad at lower

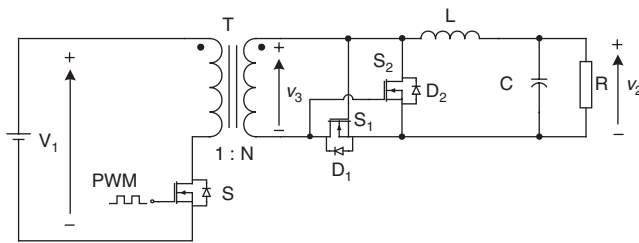


FIGURE 12.3

Synchronous rectifier converter with low-resistance MOSFET.

input voltages because the rectifier has a lower duty cycle and, thus, a shorter conduction time. However, the Schottky rectifier's forward drop is usually the dominant loss mechanism.

For an input voltage of 7.2 V and output of 3.3 V, a synchronous rectifier improves on the Schottky diode rectifier's efficiency by around 4%. Figure 12.1 also shows that, as output voltage decreases, the synchronous rectifier provides even larger gains in efficiency.

A practical circuit arrangement of a synchronous rectifier (SR) DC/DC converter with purely resistive load is shown in Figure 12.3. It has one MOSFET switch S on the primary side of the transformer. Two MOSFETs S_1 and S_2 on the secondary side of the transformer are functioning as the synchronous rectifier. T is the isolating transformer with a turn ratio of $1:N$. an L - C circuit is the low-pass filter and R is the load. V_1 is the input voltage and V_2 is the output voltage. The main switch S is driven by a PWM pulse-train signal. Repeating frequency f and turn-on duty cycle K of the PWM signal can be adjusted.

When the PWM signal is in the positive state, the main switch S conducts. The primary voltage of the transformer is V_1 , and subsequently the secondary voltage of the transformer is $v_3 = NV_1$. In the mean time the MOSFET S_1 is forward biased, so it turns ON and inversely conducts.

When the PWM signal is in the negative state, the main switch S is switched off. The voltage of the transformer, v_3 , at this moment in time is approximately $-NV_{C1}$. At the mean time the MOSFET S_2 is forward biased, so it turns ON and inversely conducts. It functions as free-wheeling diode and lets the load current remain continuous through the filter L - C and load R .

A lot of papers in literature with practical hardware circuit achievements on synchronous rectifier have been presented about the recent *IEEE Transactions* and *IEE Proceedings*. The paper "Evaluation of Synchronous-Rectification Efficiency Improvement Limits in Forward Converters" supported by Virginia Power Electronics Center is one of the few outstanding research publications on synchronous rectifiers (Jovanovic et al., 1995). This chapter provides a practical design of a 3.3V/20A FSR (forward synchronous rectifier) with an efficiency of 85.5%. Similarly, another paper in 1993 also showed the principle of a RCD clamp forward converter with an efficiency of 87.3%

at low output current (Cobos et al., 1993). Two Japanese researchers from Kumamoto Institute of Technology designed an FSR with an additional winding and switching element that is able to hold the gate charge for the freewheeling MOSFET (Sakai and Harada, 1995). Their experimental results for a 5 V/10 A SR gives a maximum efficiency of approximately 91% at a load of 7 A and an efficiency of 89% at 10 A. Another comparable FSR project was made by James Blanc from Siliconix Incorporated (Blanc, 1991). In his paper, he has included a lot of practical and useful simulation and experimental waveform data from his 3.3 V/10 A FSR. As the output voltage decreased, the operating efficiency decreased. Until now, no recent paper has been published on any practical hardware FSR that is able to provide 1.8 V/20 A output current at high efficiency.

Analysis and design of DC/DC converters has been the subject of many papers in the past. From the moment averaging techniques were used to model these converters, interest has been focused on finding the best approach to analyze and predict the behavior of the averaged small signal or large signal models. The main difficulty encountered is that the converter models are multiple-input multiple-output nonlinear systems and thus, using the well-known transfer function control design approach is not straightforward. The most common approach has been that of considering the linearized small signal model of these converters as a multi-loop system, with an outer voltage loop and an inner current loop. Since the current loop has a much faster response than that of the outer loop, the analysis is greatly simplified and the transfer functions obtained allow the designer to predict the closed loop behavior of the system. Another approach in analysis and design has been that of state-space techniques where the linearized state-space equations are used together with design technique such as pole placement or optimal control.

Synchronous rectifier DC/DC converters are called the fifth generation converters. The developments in microelectronics and computer science require power supplies with low output voltage and strong current. Traditional diode bridge rectifiers are not available for this requirement. Soft-switching technique can be applied in synchronous rectifier DC/DC converters. We have created converters with very low voltage (5 V, 3.3 V, and 1.8 ~ 1.5 V) and strong current (30 A, 60 A, 200 A) and high power transfer efficiency (86%, 90%, 93%). In this section new circuits different from the ordinary synchronous rectifier DC/DC converters are introduced:

- Flat transformer synchronous rectifier Luo-converter
- Active clamped flat transformer synchronous rectifier Luo-converter
- Double current synchronous rectifier Luo-converter with active clamp circuit
- Zero-current-switching synchronous rectifier Luo-converter
- Zero-voltage-switching synchronous rectifier Luo-converter

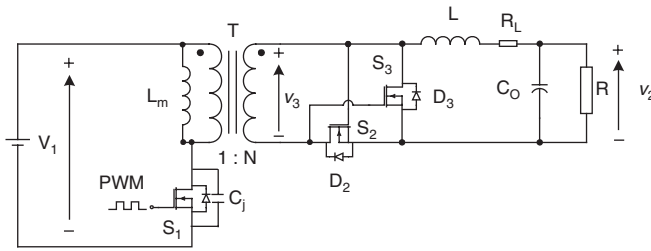


FIGURE 12.4
Flat transformer synchronous rectifier Luo-converter.

12.2 Flat Transformer Synchronous Rectifier Luo-Converter

The flat transformer is a new design for AC/AC energy conversion. Since its structure is very compatible and well-shielded, its size is very small and likely a flin cardboard. Applying frequency can be 100 KHz to 5 MHz, its power density can be as high as 300 W/inch³. Therefore, it is a good component to use to construct the synchronous rectifier DC/DC converter.

The flat transformer SR DC/DC Luo-converter is shown in Figure 12.4. The switches S_1 , S_2 , and S_3 are the low-resistance MOSFET devices with resistance R_S (6 to 8 m Ω). Since we use a flat transformer, its leakage inductance L_m , $L_m = 1$ nH, and resistance are small. Other parameters are $C_j = 50 \sim 100$ nF, $R_L = 2$ m Ω , $L = 5$ μ H, $C_O = 10$ μ F. The input voltage is $V_1 = 30$ VDC and output voltage is V_2 , the output current is I_O . The transformer turn ratio is N that is usually much smaller than unity in SR DC/DC converters, e.g., $N = 1:12$ or $1/12$. The repeating period is $T = 1/f$ and conduction duty is k . There are four working modes:

- Transformer Is in magnetizing
- Forward on
- Transformer Is in demagnetizing
- Switched off

12.2.1 Transformer Is in Magnetizing Process

The natural resonant frequency is

$$\omega = \frac{1}{\sqrt{L_m C_j}} \quad (12.1)$$

where the L_m is the leakage inductance of the primary winding, the C_j is the drain-source junction capacitance of the main switch MOSFET S.

If C_j is very small in nF , its charging process is very quickly completed. The primary current increases with slope V_1/L_m , then the time interval of this period can be estimated

$$t_1 = \frac{L_m}{V_1} NI_O \quad (12.2)$$

This is the process used to establish the primary current from 0 to rated value NI_O .

12.2.2 Switching-On

Switching-on period is controlled by the PWM signal, therefore,

$$t_2 \approx kT \quad (12.3)$$

12.2.3 Transformer Is in Demagnetizing Process

The transformer demagnetizing process is estimated in

$$t_3 = \sqrt{L_m C_j} \left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + \frac{L_m}{C_j} (NI_O)^2}} \right] \quad (12.4)$$

When the main switch is switching-off there is a voltage stress, which can be very high. The voltage stress is dependent on the energy stored in the inductor and the capacitor:

$$V_{peak} = \sqrt{\frac{L_m}{C_j}} NI_O \quad (12.5)$$

The voltage stress peak value can be tens to hundreds of volts since C_j is small.

12.2.4 Switching-Off

The switch-off period is controlled by the PWM signal, therefore,

$$t_4 \approx (1 - k)T \quad (12.6)$$

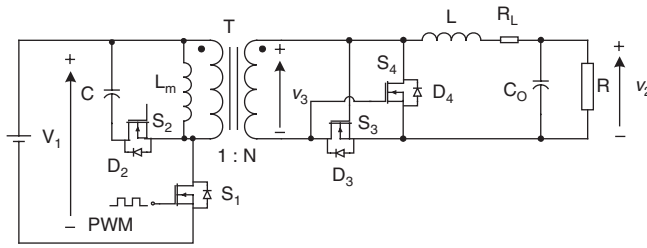


FIGURE 12.5

Active clamped flat transformer synchronous rectifier Luo-converter.

12.2.5 Summary

Average output voltage V_2 and input current I_1 are

$$V_2 = kNV_1 - (R_L + R_S + \frac{L_m}{T} N^2) I_O \quad (12.7)$$

and

$$I_1 = kNI_O \quad (12.8)$$

The power transfer efficiency:

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_m}{T} N^2}{kNV_1} I_O \quad (12.9)$$

When we set the frequency $f = 150$ to 200 kHz, we obtained the $V_2 = 1.8$ V, $N = 1/12$, $I_O = 0$ to 30 A, Volume = 2.5 (in.³). The average power transfer efficiency is 92.3% and the maximum PD is 21.6 W/in.³.

12.3 Active Clamped Synchronous Rectifier Luo-Converter

Active clamped flat transformer SR Luo-converter is shown in [Figure 12.5](#). The clamped circuit effectively suppresses the voltage stress during the main switch turn-off.

Comparing the circuit in [Figure 12.5](#) with the circuit in [Figure 12.4](#), one more switch S_2 is set in the primary side. It is switched-on and -off exclusively to the main switch S_1 . When S_1 is turning-off, S_2 is switching-on. A large clamp capacitor C is connected in the primary winding to absorb the energy

stored in the leakage inductor L_m . Since the clamp capacitor C is much larger than the drain-source capacitor C_j by usually hundreds of times, the stress voltage peak value remains at only a few volts.

There are four working modes:

- Transformer Is in magnetizing
- Forward on
- Transformer Is in demagnetizing
- Switched off

12.3.1 Transformer Is in Magnetizing

The natural resonant frequency is

$$\omega = \frac{1}{\sqrt{L_m C_j}} \quad (12.10)$$

where the L_m is the leakage inductance of the primary winding, the C_j is the drain-source junction capacitance of the main switch MOSFET S .

If C_j is very small in nF , its charging process is very quickly completed. The primary current increases with slope V_1/L_m , then the time interval of this period can be estimated

$$t_1 = \frac{L_m}{V_1} N I_O \quad (12.11)$$

This is the process to establish the primary current from 0 to rated value $N I_O$.

12.3.2 Switching-On

Switching-on period is controlled by the PWM signal, therefore,

$$t_2 \approx kT \quad (12.12)$$

12.3.3 Transformer Is in Demagnetizing

The transformer demagnetizing process is estimated by

$$t_3 = \sqrt{L_m C} \left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + \frac{L_m}{C} (N I_O)^2}} \right] \quad (12.13)$$

where C is the active clamp capacitor in μF . The voltage stress depends on the energy stored in the inductor and the capacitor:

$$V_{peak} = \sqrt{\frac{L_m}{C}} NI_O \quad (12.14)$$

The voltage stress peak value is very small since capacitor C is large, measured in μF .

12.3.4 Switching-Off

Switching-off period is controlled by the PWM signal, therefore,

$$t_4 \approx (1 - k)T \quad (12.15)$$

12.3.5 Summary

Average output voltage is V_2 and input current is I_1 :

$$V_2 = kNV_1 - (R_L + R_S + \frac{L_m}{T} N^2) I_O \quad (12.16)$$

and

$$I_1 = kNI_O \quad (12.17)$$

The power transfer efficiency:

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_m}{T} N^2}{kNV_1} I_O \quad (12.18)$$

When we set the frequency $f = 150$ to 200 kHz, we obtained the $V_2 = 1.8$ V, $N = 1/12$, $I_O = 0$ to 30 A, volume = 2.5 (in.³). The average power transfer efficiency is 92.3% and the maximum power density (PD) is 21.6 W/in.³.

12.4 Double Current Synchronous Rectifier Luo-Converter

The converter in [Figure 12.5](#) likes a half wave rectifier. The double current synchronous rectifier Luo-converter with active clamp circuit is shown in

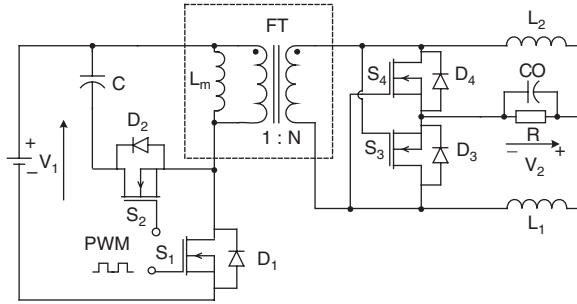


FIGURE 12.6
Double-current synchronous rectifier Luo-converter.

Figure 12.6. The switches S_1 to S_4 are the low-resistance MOSFET devices with very low resistance R_s (6 to 8 m Ω). Since S_3 and S_4 plus L_1 and L_2 form a double current circuit and S_2 plus C is the active clamp circuit, this converter likes a full wave rectifier and obtains strong output current. Other parameters are $C = 1 \mu\text{F}$, $L_m = 1 \text{ nH}$, $R_L = 2 \text{ m}\Omega$, $L = 5 \mu\text{H}$, $C_O = 10 \mu\text{F}$. The input voltage is $V_1 = 30 \text{ VDC}$ and output voltage is V_2 , the output current is I_O . The transformer turn ratio is $N = 1:12$. The repeating period is $T = 1/f$ and conduction duty is k . There are four working modes:

- Transformer Is in magnetizing
- Forward on
- Transformer Is in demagnetizing
- Switched off

12.4.1 Transformer Is in Magnetizing

The natural resonant frequency is

$$\omega = \frac{1}{\sqrt{L_m C_j}} \quad (12.19)$$

where the L_m is the leakage inductance of the primary winding, the C_j is the drain-source junction capacitance of the main switch MOSFET S .

If C_j is very small in nF, its charging process is very quickly completed. The primary current increases with slope V_1/L_m , and the time interval of this period can be estimated

$$t_1 = \frac{L_m}{V_1} N I_O \quad (12.20)$$

This is the process used to establish the primary current from 0 to rated value NI_O .

12.4.2 Switching-On

Switching-on period is controlled by the PWM signal, therefore,

$$t_2 \approx kT \quad (12.21)$$

12.4.3 Transformer Is in Demagnetizing

The transformer demagnetizing process is estimated in

$$t_3 = \sqrt{L_m C} \left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + \frac{L_m}{C} (NI_O)^2}} \right] \quad (12.22)$$

When the main switch is switching-off there is a very low voltage stress since the active clamp circuit is applied.

12.4.4 Switching-Off

Switching-off period is controlled by the PWM signal, therefore,

$$t_4 \approx (1 - k)T \quad (12.23)$$

12.4.5 Summary

Average output voltage V_2 and input current I_1 are

$$V_2 = kNV_1 - (R_L + R_S + \frac{L_m}{T} N^2) I_O \quad (12.24)$$

and

$$I_1 = kNI_O \quad (12.25)$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_m}{T} N^2}{kNV_1} I_O \quad (12.26)$$

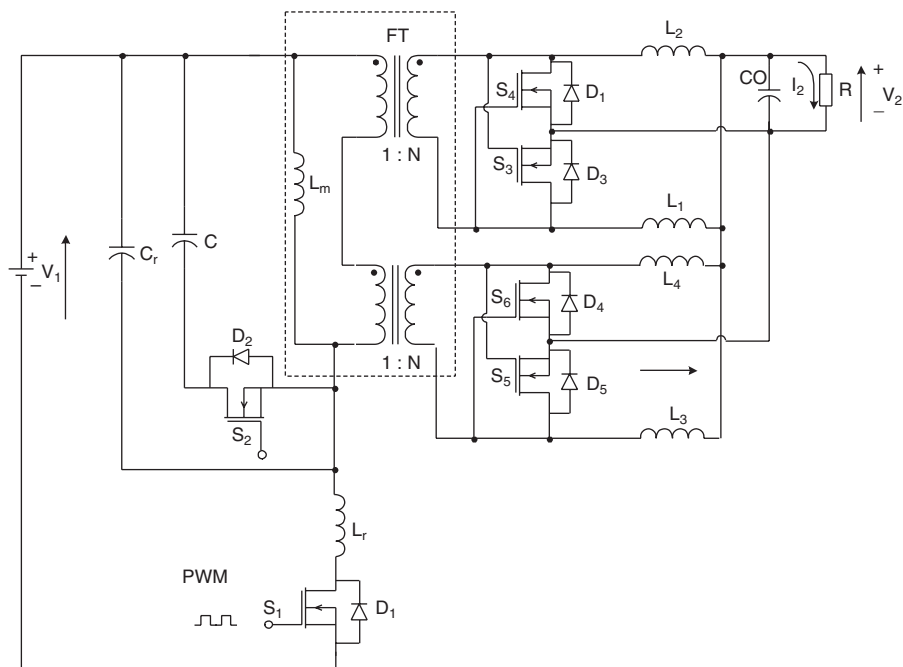


FIGURE 12.7
ZCS synchronous rectifier Luo-converter.

When we set the frequency $f = 200$ to 250 kHz, we obtained the $V_2 = 1.8$ V, $N = 12$, $I_O = 0$ to 35 A, volume = 2.5 (in.³). The average power transfer efficiency is 94% and the maximum PD is 25 W/in.³.

12.5 Zero-Current-Switching Synchronous Rectifier Luo-Converter

The zero-current-switching (ZCS) synchronous rectifier Luo-converter is shown in Figure 12.7. Since the power loss across the main switch S_1 is high in the double current SR Luo-converter, we designed the ZCS, DC SR Luo-Converter shown in Figure 12.7. This converter is based on the DC SR Luo-converter plus ZCS technique. It employs a double core flat transformer. There are four working modes:

- Transformer Is in magnetizing
- Resonant period
- Transformer Is in demagnetizing
- Switched off

12.5.1 Transformer Is in Magnetizing

The ZCS resonant frequency is

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (12.27)$$

The normalized impedance is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad (12.28)$$

The shift-angular distance is

$$\alpha = \sin^{-1}\left(\frac{I_1 Z_r}{V_1}\right) \quad (12.29)$$

where the L_r is the resonant inductor and the C_r is the resonant capacitor.

The primary current increases with slope V_1/L_r , then the time interval of this period can be estimated

$$t_1 = \frac{I_1 L_r}{V_1} \quad (12.30)$$

12.5.2 Resonant Period

The resonant period is,

$$t_2 = \frac{1}{\omega_r}(\pi + \alpha) \quad (12.31)$$

12.5.3 Transformer Is in Demagnetizing

The transformer demagnetizing process is estimated in

$$t_3 = \frac{V_1(1 + \cos \alpha)C_r}{I_1} \quad (12.32)$$

When the main switch is switching-off there is a very low voltage stress since active clamp circuit is applied.

12.5.4 Switching-Off

Switching-off period is controlled by the PWM signal, therefore,

$$t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_1} \left(I_L + \frac{V_1}{Z_r} \frac{\cos \alpha}{\pi / 2 + \alpha} \right) - (t_1 + t_2 + t_3) \quad (12.33)$$

12.5.5 Summary

Average output voltage V_2 and input current I_1 are

$$V_2 = kNV_1 - (R_L + R_S + \frac{L_r + L_m}{T} N^2) I_O \quad (12.34)$$

and

$$I_1 = kNI_O \quad (12.35)$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_r + L_m}{T} N^2}{kNV_1} I_O \quad (12.36)$$

Since L_r is larger than L_m , therefore L_m can be ignored in the above formulae.

When we set the $V_1 = 60$ V and frequency $f = 200$ to 250 kHz, we obtained the $V_2 = 1.8$ V, $N = 1/12$, $I_O = 0$ to 60 A, volume = 4 (in.³). The average power transfer efficiency is 94.5% and the maximum PD is 27 W/in.³.

12.6 Zero-Voltage-Switching Synchronous Rectifier Luo-Converter

The zero-voltage-switching synchronous rectifier Luo-converter is shown in [Figure 12.8](#), which is derived from the DC SR Luo-converter plus ZVS technique. It employs a double core flat transformer. There are four working modes:

- Transformer Is in magnetizing
- Resonant period
- Transformer Is in demagnetizing
- Switched off

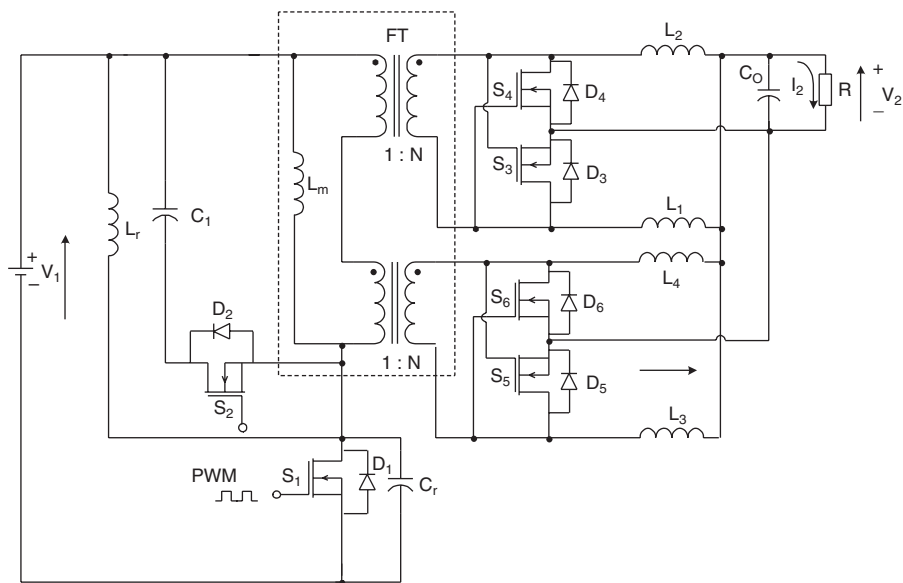


FIGURE 12.8
ZVS synchronous rectifier Luo-converter.

12.6.1 Transformer Is in Magnetizing

The ZVS resonant frequency is

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (12.37)$$

The normalized impedance is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad (12.38)$$

The shift-angular distance is

$$\alpha = \sin^{-1}\left(\frac{V_1}{Z_r I_1}\right) \quad (12.39)$$

where the L_r is the resonant inductor and the C_r is the resonant capacitor.

The switch voltage increases with slope I_1/C_r , then the time interval of this period can be estimated

$$t_1 = \frac{V_1 C_r}{I_1} \quad (12.40)$$

12.6.2 Resonant Period

The resonant period is,

$$t_2 = \frac{1}{\omega_r}(\pi + \alpha) \quad (12.41)$$

12.6.3 Transformer Is in Demagnetizing

The transformer demagnetizing process is estimated in

$$t_3 = \frac{I_1(1 + \cos \alpha)L_r}{V_1} \quad (12.42)$$

While the main switch is switching-off there is a very low voltage stress since active clamp circuit is applied.

12.6.4 Switching-Off

Switching-off period is controlled by the PWM signal, therefore,

$$t_4 = \frac{t_1 + t_2 + t_3}{\frac{V_1}{V_2} - 1} \quad (12.43)$$

12.6.5 Summary

Average output voltage V_2 and input current I_1 are

$$V_2 = kNV_1 - (R_L + R_S + \frac{L_r}{T} / L_m N^2)I_O \quad (12.44)$$

and

$$I_1 = kNI_O \quad (12.45)$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_r}{T} / \frac{L_m}{N^2}}{k N V_1} I_O \quad (12.46)$$

Since L_r is larger than L_m , therefore L_r can be ignored in the above formulae.

When we set the $V_1 = 60$ V and frequency $f = 200$ to 250 kHz, we obtained the $V_2 = 1.8$ V, $N = 12$, $I_O = 0$ to 60 A, volume = 4 (in.³). The average power transfer efficiency is 94.5% and the maximum PD is 27 W/in.³.

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Multiple Energy-Storage Element Resonant Power Converters

13.1 Introduction

Multiple energy-storage element resonant power converters (x-element RPC) are the sixth generation converters. As the transfer power becomes higher and higher, traditional methods are unable to deliver large amounts of power from the source to the final actuators with high efficiency. In order to reduce the power losses during the conversion process the sixth generation converters — multiple energy-storage elements resonant power converters (x-element RPC), were created. They can be classified into two main groups

- DC/DC resonant converters
- DC/AC resonant inverters

Both groups consist of multiple energy-storage elements: two, three, or four elements. These energy-storage elements are passive parts: inductors and capacitors. They can be connected in series or parallel in various methods. The circuits of the multiple energy-storage elements converters are

- Eight topologies of two-element RPC shown in [Figure 13.1](#).
- Thirty-eight topologies of three-element RPC shown in [Figure 13.2](#).
- Ninety-eight topologies of four-element (2L-2C) RPC shown in [Figure 13.3](#).

If no restriction such as 2L-2C for four-element RPC, the number of the topologies of four-element RPC can be very large. How to investigate the large quantity of converters is a task of vital importance. This problem was outstanding in the last decade of last century. Unfortunately, it was not paid very much attention. This generation of converters were not well discussed, only a limited number of papers were published in the literature.

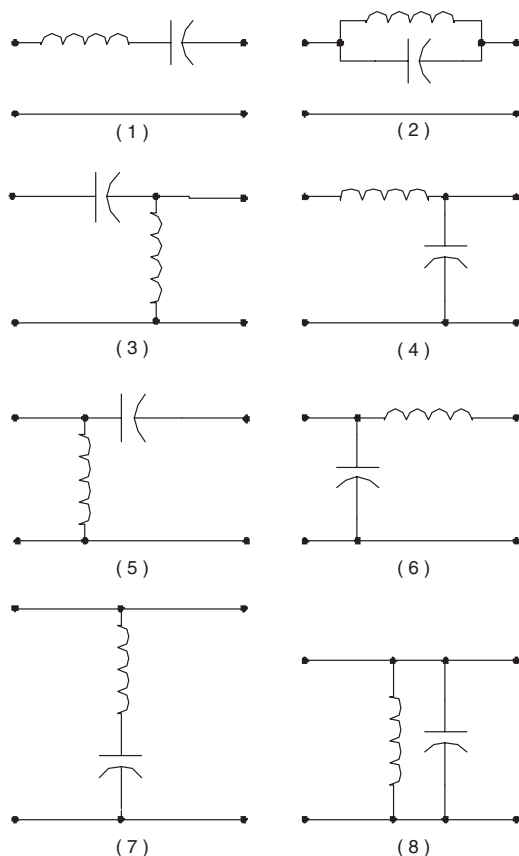


FIGURE 13.1
The eight topologies of two-element RPC.

13.1.1 Two-Element RPC

There are eight topologies of two-element RPCs shown in Figure 13.1. These topologies have simple circuit structure and minimal components. Consequently, they can transfer the power from source to end-users with higher power efficiency and lower power losses. A particular circuitry analysis will be carried out in the next section.

Usually, the two-element RPC has a very narrow response frequency band, which is defined as the frequency width between the two half-power points. The working point must be selected in the vicinity of the natural resonant frequency

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

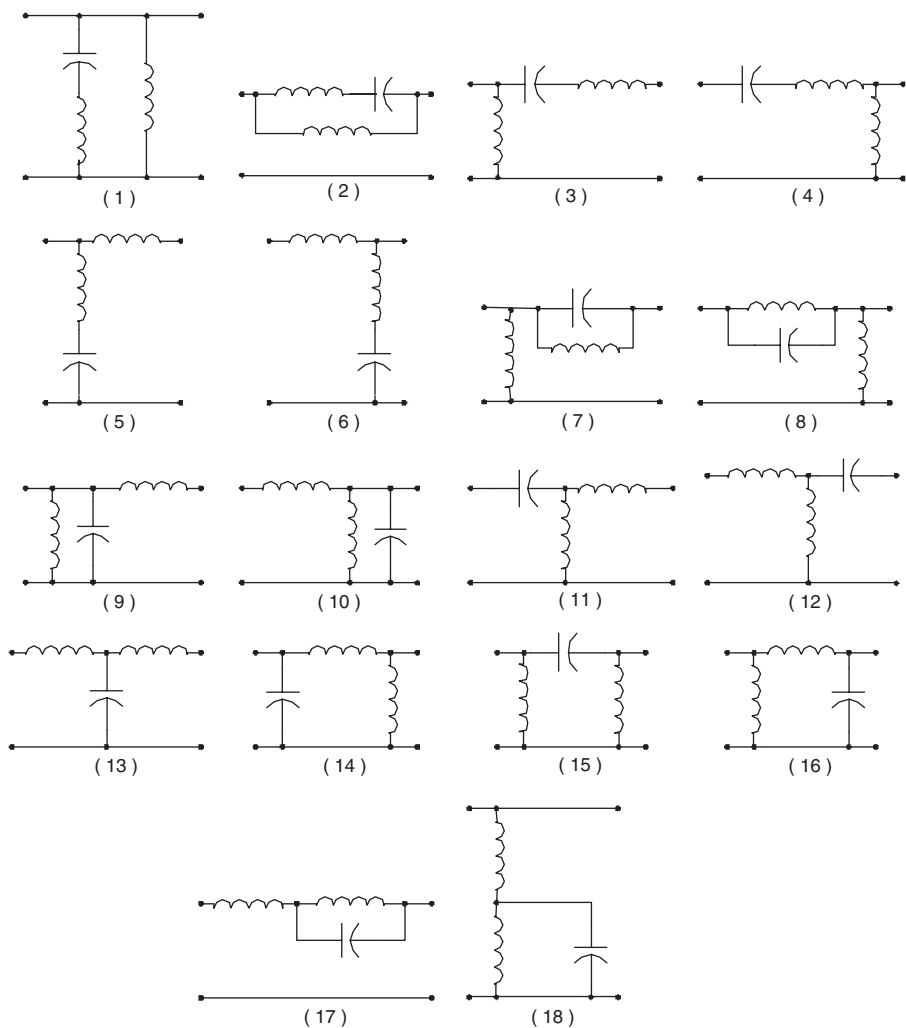


FIGURE 13.2
The thirty-eight topologies of three-element RPC.

Another drawback is that the transferred waveform is usually not sinusoidal, i.e., the output waveform total harmonic distortion (THD) is not zero.

Since total power losses are mainly contributed by the power losses across the main switches using resonant conversion technique, the two-element RPC has a high power transferring efficiency.

13.1.2 Three-Element RPC

There are 38 topologies of three-element RPC that are shown in Figure 13.2. These topologies have one more component in comparison to the two-element

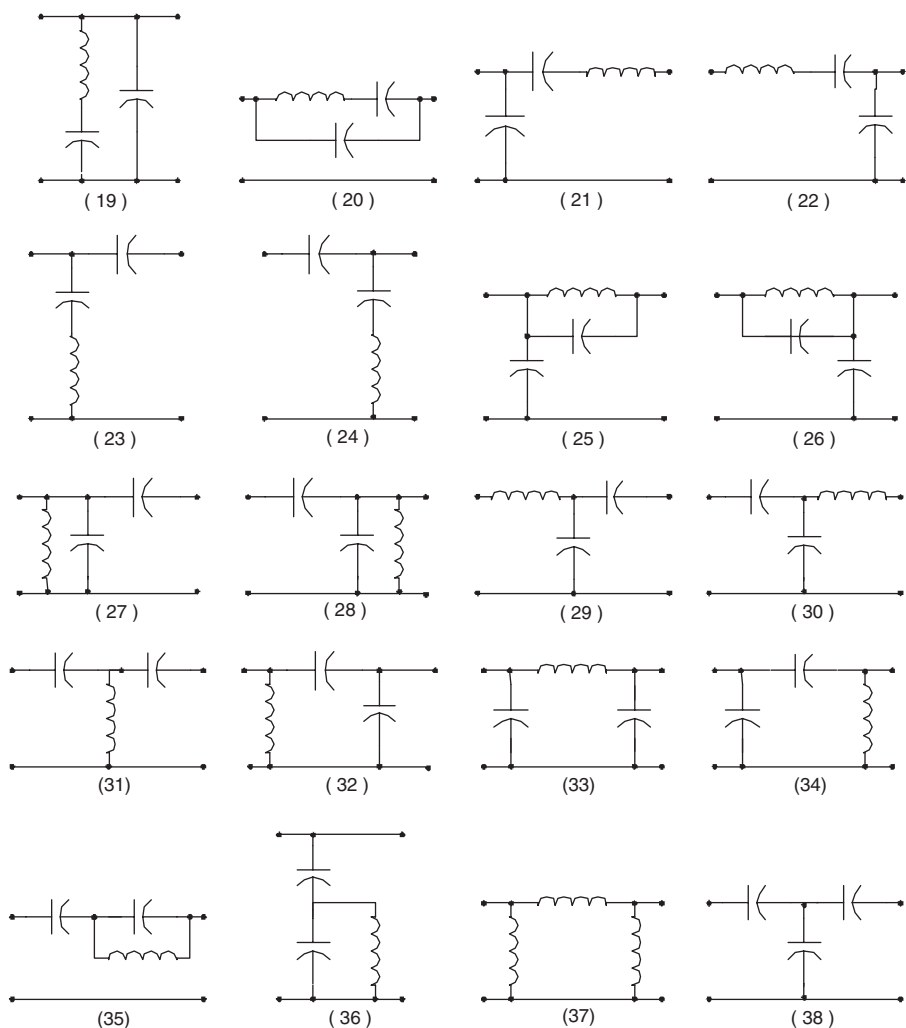


FIGURE 13.2 (continued)

RPC topologies. Consequently, they can transfer the power from source to end-users with higher power and high power transfer efficiency. A particular circuitry analysis will be carried out in the next chapter.

Usually, the three-element RPC has a much wider response frequency band, which is defined as the frequency width between the two half-power points. If the circuit is a low-pass filter, the frequency bands can cover the frequency range from 0 to the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. The working point can be selected in the much wider frequency width which is lower than the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. Another advantage over the two-element RPC topologies is that the transferred waveform can usually be sinusoidal, i.e., the output waveform THD is nearly zero. A well-known mono-frequency waveform transferring operation has very low EMI.

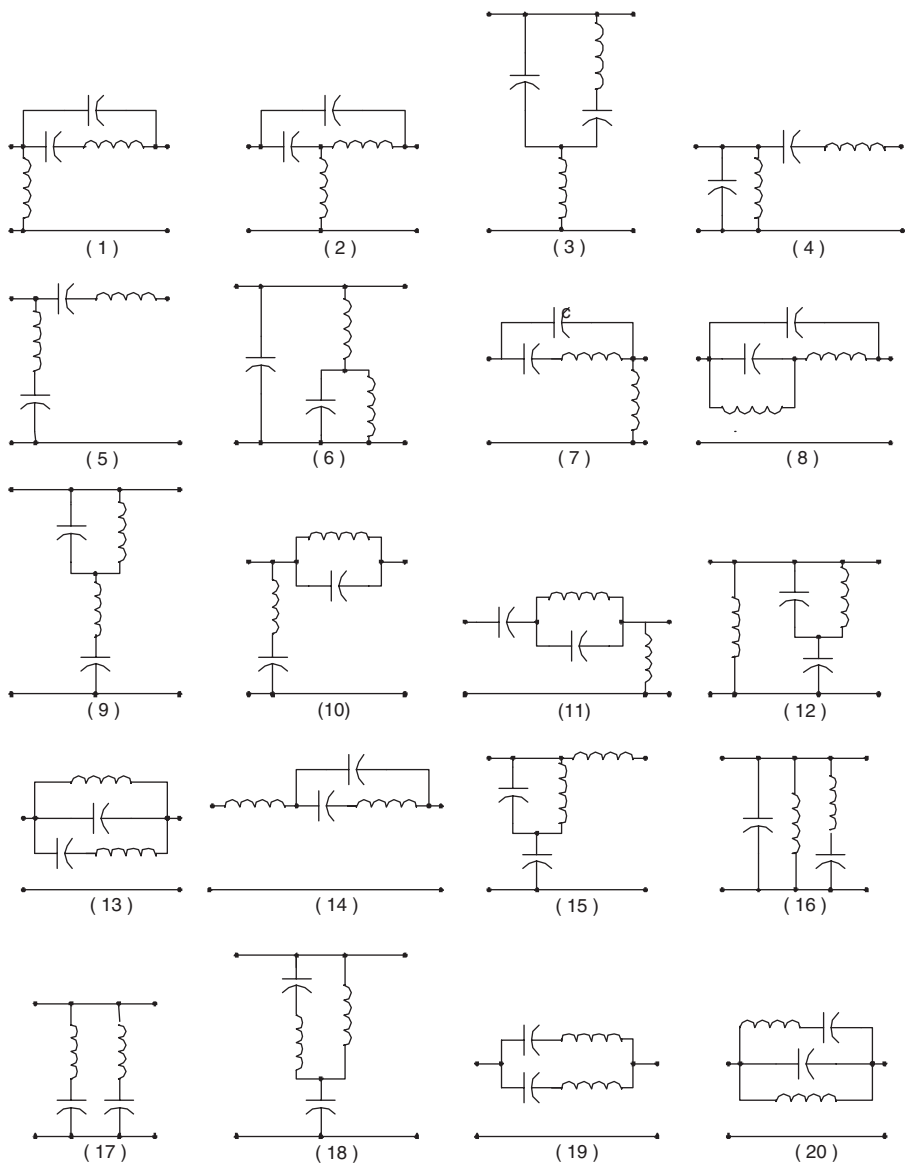


FIGURE 13.3
The ninety-eight topologies of four-element (2L-2C).

13.1.3 Four-Element RPC

There are 98 topologies of four-element RPC (2L-2C) that are shown in Figure 13.3. Although these topologies have comparable complex circuit structures, they can still transfer the power from source to end-users with higher power efficiency and lower power losses. Particular circuitry analysis will be carried out in the next chapter.

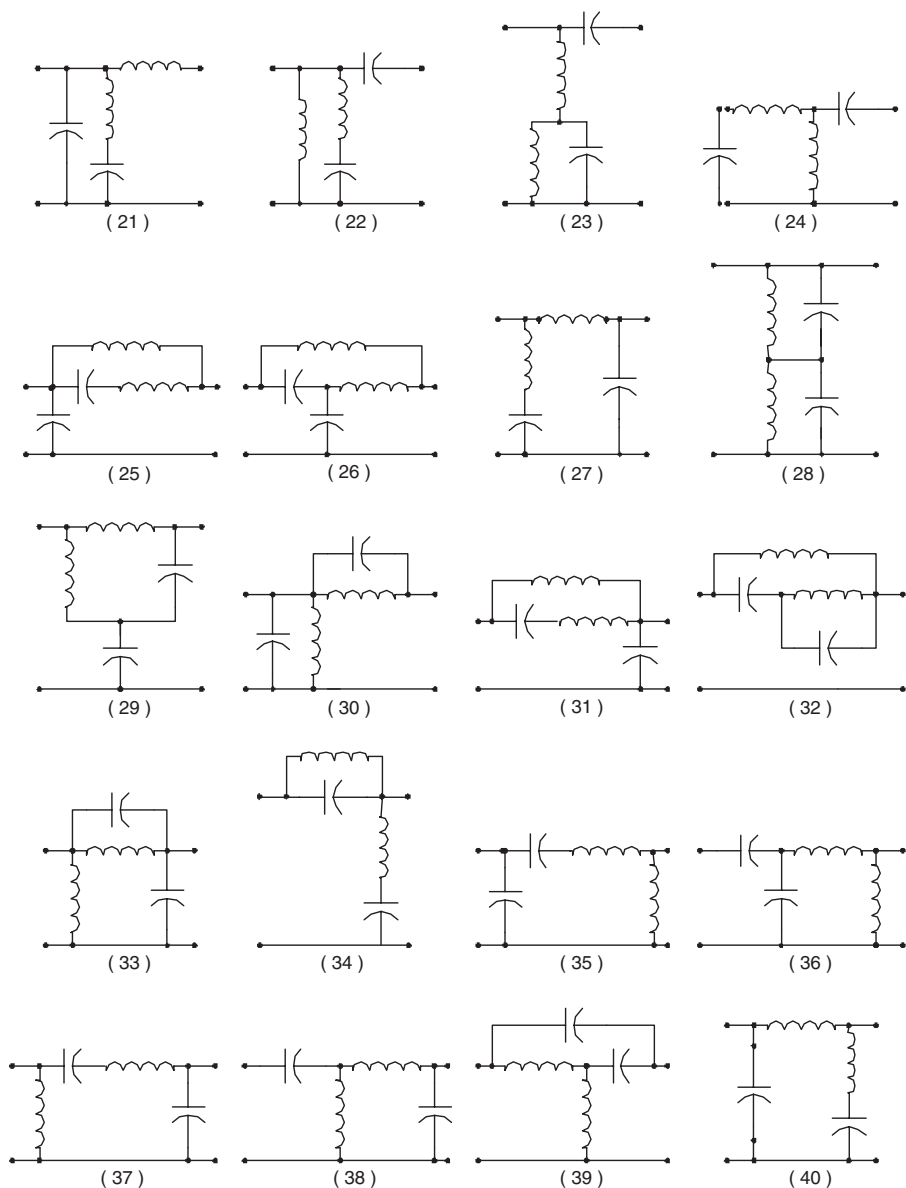


FIGURE 13.3 (continued)

Usually, the four-element RPC has a wide response frequency band, which is defined as the frequency width between the two half-power points. If the circuit is a low-pass filter, the frequency bands can cover the frequency range from 0 to the high half-power point, which is definitely higher than the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. The working point can be selected in a wide area across (lower and higher than) the natural resonant frequency

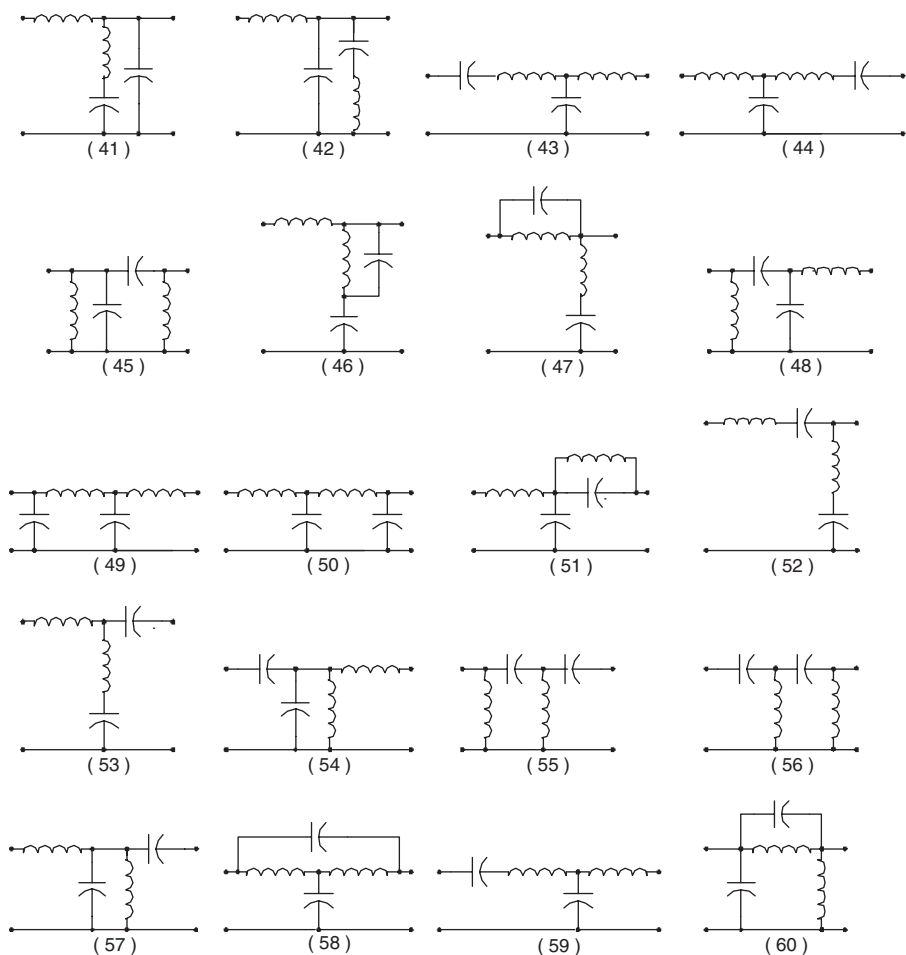


FIGURE 13.3 (continued)

$\omega_0 = 1/\sqrt{LC}$. Another advantage is that the transferred waveform is sinusoidal, i.e., the output waveform THD is very close to zero. As is well-known, the mono-frequency-waveform transferring operation has a very low electromagnetic interference (EMI) and a reasonable electromagnetic susceptibility (EMS) and electromagnetic compatibility (EMC).

13.2 Bipolar Current and Voltage Source

Depending on the application, a resonant network can be low-pass filter, high-pass filter, or band-pass filter. For a large power transferring process,

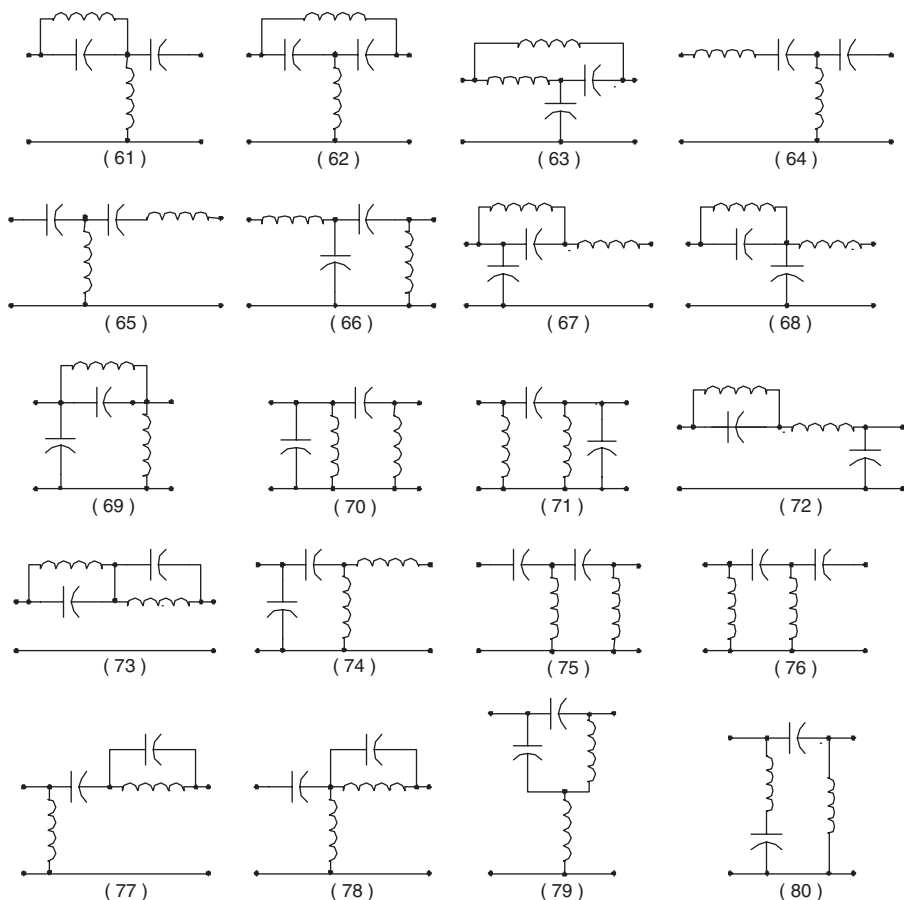


FIGURE 13.3 (continued)

a low-pass filter is usually employed. In this case, inductors are arranged in series arms and capacitors are arranged in shunt arms. If the first component is an inductor, only voltage source can be applied since inductor current is continuous. Vice versa, if the first component is a capacitor, only current source can be applied since capacitor voltage is continuous. Unipolar current and voltage source are easier to obtain using various pumps, such as buck pump, boost pump, and buck-boost pump, which are introduced in Chapter 1.

Bipolar current and voltage sources are more difficult to obtain using these pumps. There are some fundamental bipolar current and voltage sources listed in the following sections.

13.2.1 Bipolar Voltage Source

There are various methods to obtain bipolar voltage sources using pumps.

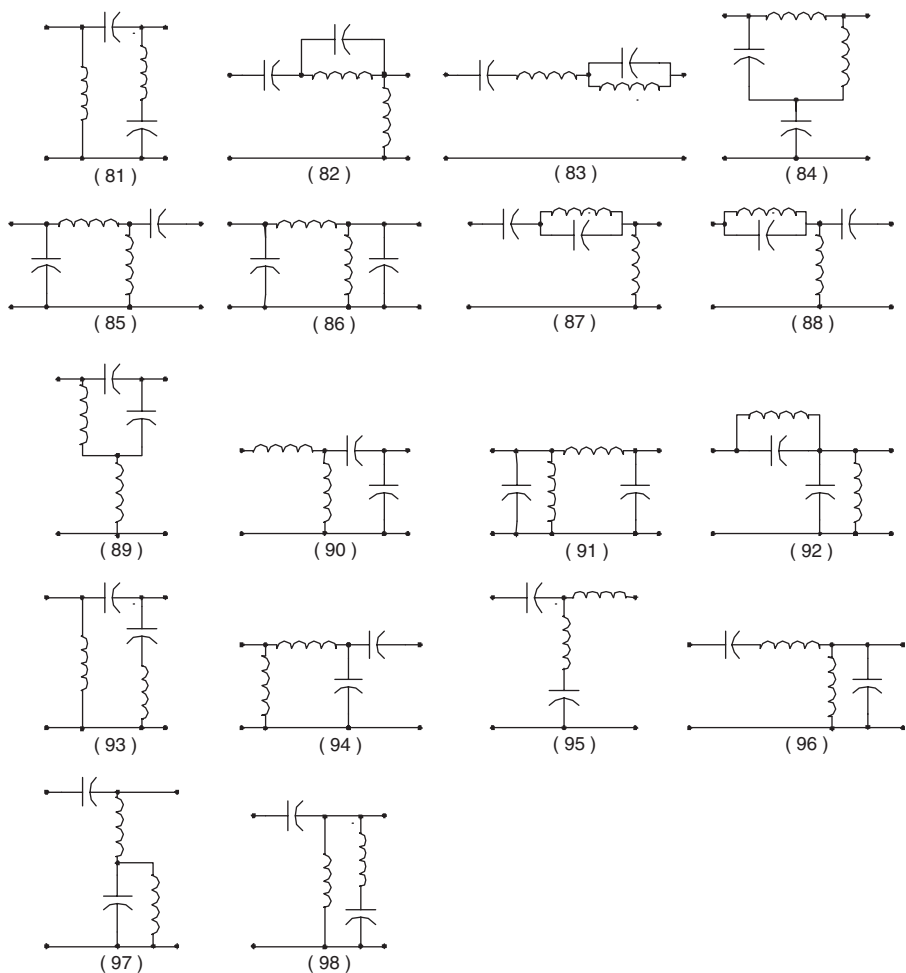


FIGURE 13.3 (continued)

13.2.1.1 Two Voltage Source Circuit

A bipolar voltage source using two voltage sources is shown in [Figure 13.4](#). These two voltage sources have the same voltage amplitude and reverse polarity. There are two switches applied alternately switching-on or -off to supply positive and negative voltage to the network. In the figure, the load is a resistance R .

The circuit of this voltage source is likely a two-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons the particular circuitry design has to consider some small gap between the turn over (commutation) operations to avoid a short-circuit.

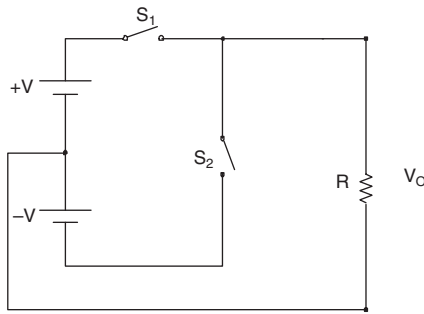


FIGURE 13.4
A bipolar voltage source using two voltage sources.

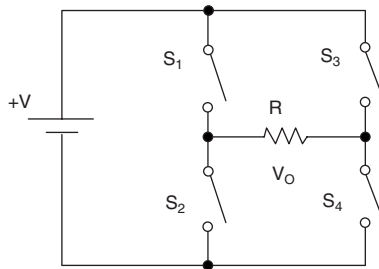


FIGURE 13.5
A bipolar voltage source using single voltage source.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz to 5 MHz depending on the application conditions.

13.2.1.2 One Voltage Source Circuit

A bipolar voltage source using single voltage source is shown in Figure 13.5. Since only one voltage source is applied, there are four switches applied alternately switching-on or switching-off to supply positive and negative voltage to the network. In the figure, the load is a resistance R .

The circuit of this voltage source is likely to be a four-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons the particular circuitry design has to consider some small gap between the turn over (commutation) operations to avoid a short-circuit.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz to 5 MHz depending on the application conditions.

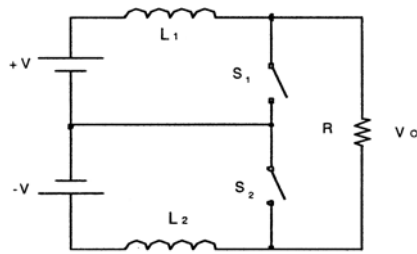


FIGURE 13.6
A bipolar current source using two voltage sources.

13.2.2 Bipolar Current Source

There are various methods used to obtain bipolar current sources using the pumps.

13.2.2.1 Two Voltage Source Circuit

A bipolar current voltage source using two voltage sources is shown in Figure 13.6. These two voltage sources have the same voltage amplitude and reverse polarity. To obtain stable current each voltage source in series is connected by a large inductor. There are two switches applied alternately switching-on or switching-off to supply positive and negative current to the network. In Figure 13.6, the load is a resistance R .

The circuit of this current source is a two-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons the particular circuitry design has to consider some small gap between the turn over (commutation) operations to avoid a short-circuit.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz to 5 MHz depending on the application conditions.

13.2.2.2 One Voltage Source Circuit

A bipolar current voltage source using single voltage sources is shown in Figure 13.7. To obtain stable current the voltage source in series is connected by a large inductor. There are two switches applied alternately switching-on or -off to supply positive and negative current to the network. In the figure, the load is a resistance R .

The circuit of this current source is likely a two-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons the particular circuitry design has to consider some small gap between the turn over (commutation) operations to avoid a short-circuit.

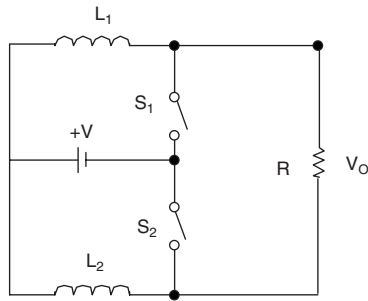


FIGURE 13.7
A bipolar current source using single voltage source.

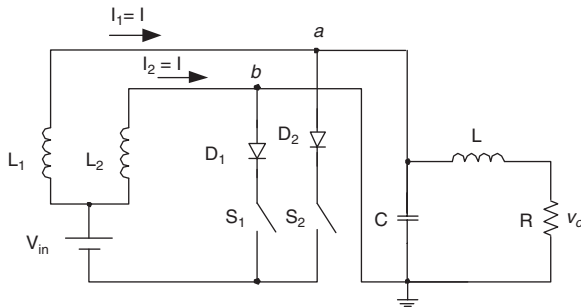


FIGURE 13.8
A two-element RPC.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz to 5 MHz depending on the application conditions.

13.3 A Two-Element RPC Analysis

This two-element RPC is the circuit number six in Figure 13.1. The network is a low-pass capacitor-inductor (CL) filter, and the first component is a capacitor. By previous analysis, the source should be a bipolar current source. Therefore, the circuit diagram of this two-element RPC is shown in Figure 13.8. To simplify the analysis, the load can be considered resistive R . The energy source V_{in} is chopped by two main switches S_1 and S_2 , it is a bipolar current source applied to the two-element filter and load. The whole RPC equivalent circuit diagram is shown in Figure 13.9.

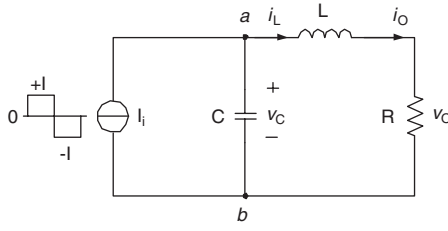


FIGURE 13.9
The equivalent circuit diagram of the two-element RPC.

13.3.1 Input Impedance

The whole network impedance including the load R is calculated by

$$Z = \frac{R + j\omega L}{1 + j\omega C(R + j\omega L)} = \frac{R + j\omega L}{1 - \omega^2 CL + j\omega RC} \quad (13.1)$$

The natural resonance angular frequency is

$$\omega_0 = \frac{1}{\sqrt{CL}} \quad (13.2)$$

Using the relevant frequency β

$$\beta = \frac{\omega}{\omega_0} = \frac{\omega}{\sqrt{CL}} \quad (13.3)$$

and the quality factor Q

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \quad (13.4)$$

we rewrite the input impedance

$$\frac{Z}{R} = \frac{1 + j\beta Q}{1 - \beta^2 + j\beta/Q} = \left| \frac{Z}{R} \right| \angle \phi \quad (13.5)$$

where

$$\left| \frac{Z}{R} \right| = \sqrt{\frac{1 + (\beta Q)^2}{(1 - \beta^2)^2 + (\beta/Q)^2}} \quad \phi = \tan^{-1} \beta Q - \tan^{-1} \frac{\beta/Q}{1 - \beta^2}$$

13.3.2 Current Transfer Gain

The current transfer gain is calculated by

$$G(\omega) = \frac{i_O}{i_{in}} = \frac{1}{1 + j\omega C(R + j\omega L)} = \frac{1}{1 - \omega^2 CL + j\omega RC} \quad (13.6)$$

Defining an auxiliary parameter B

$$B(\omega) = 1 + j\omega C(R + j\omega L) \quad (13.7)$$

Hence,

$$G(\omega) = \frac{1}{B(\omega)} = |G| \angle \theta \quad (13.8)$$

Using the relevant frequency and quality factor,

$$G(\beta) = \frac{i_O}{i_{in}} = \frac{1}{1 - \beta^2 + j \frac{\beta}{Q}} \quad (13.9)$$

$$B(\beta) = 1 - \beta^2 + j \frac{\beta}{Q} \quad (13.10)$$

and

$$|G| = \sqrt{\frac{1}{(1 - \beta^2)^2 + (\beta/Q)^2}} \quad \theta = -\tan^{-1} \frac{\beta/Q}{1 - \beta^2}$$

13.3.3 Operation Analysis

Based on the equivalent circuit in [Figure 13.9](#), the state equation is established as:

$$\begin{pmatrix} \dot{i}_L \\ \dot{v}_C \end{pmatrix} = \begin{pmatrix} -\frac{R}{L} & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} + \begin{pmatrix} 0 \\ \frac{I}{C} \end{pmatrix} \quad (13.11)$$

By Laplace transform, the state equation in time domain could be transferred into s -domain, given by:

$$\begin{cases} sLI_L(s) - LI_L(0) = V_C(s) - I_L(s)R \\ sCV_C(s) - CV_C(0) = I / s - I_L(s) \end{cases} \quad (13.12)$$

yielding:

$$I_L(s) = \frac{sLCI_L(0) + I / s + CV_C(0)}{s^2LC + sRC + 1} = \frac{s[I_L(0) - I] + [V_C(0) - IR] / L}{(s + \frac{R}{2L})^2 + \frac{1}{LC} - \frac{R^2}{4L^2}} + \frac{I}{s} \quad (13.13)$$

The inductor current in time domain is then derived by taking the inverse Laplace transform, giving:

$$i_L(t) = a_1 e^{-\alpha t} \cos \beta t + \frac{b_1 - a_1 \alpha}{\beta} e^{-\alpha t} \sin \beta t + I \quad (13.14)$$

where

$$a_1 = I_L(0) - I \quad b_1 = [V_C(0) - IR] / L$$

α is the damping ratio, $\alpha = R/2L$. β is the resonant angular frequency, $\beta = \sqrt{(1/LC) - (R^2/4L^2)}$.

Similarly, the resonant capacitor voltage in s -domain is attained as:

$$\begin{aligned} V_C(s) &= \frac{sLCV_C(0) + \frac{IR}{s} + [L(I_L(0) - I) + RCV_C(0)]}{s^2LC + sRC + 1} \\ &= \frac{sLC[V_C(0) - IR] + \{L[I - I_L(0)] + RCV_C(0) - IR^2C\}}{s^2LC + sRC + 1} + \frac{IR}{s} \end{aligned} \quad (13.15)$$

The corresponding expression in time domain is written by:

$$v_C(t) = a_2 e^{-\alpha t} \cos \beta t + \frac{b_2 - a_2 \alpha}{\beta} e^{-\alpha t} \sin \beta t + IR \quad (13.16)$$

where

$$a_2 = V_C(0) - IR \quad b_2 = \{L[I - I_L(0)] + RCV_C(0) - IR^2C\} / LC$$

To make the analytic Equation (13.14) and Equation (13.16) available, the initial conditions must be known at first. Here the periodic nature is applied

under steady state operation. Namely, during one switching cycle, the resonant voltage and current at the initial instant should be the same absolute values with negative sign as those at the half cycle, that is

$$i_L(0) = I_L(0) = -i_L(\frac{T_s}{2}) \quad v_C(0) = V_C(0) = -v_C(\frac{T_s}{2}) \quad (13.17)$$

Substituting Equation (13.17) into Equation (13.14) and Equation (13.16), respectively, yields:

$$\begin{cases} -I_L(0) = a_1 e^{-\frac{\alpha T_s}{2}} \cos(\frac{\beta T_s}{2}) + \frac{b_1 - a_1 \alpha}{\beta} e^{-\frac{\alpha T_s}{2}} \sin(\frac{\beta T_s}{2}) + I \\ -V_C(0) = a_2 e^{-\frac{\alpha T_s}{2}} \cos(\frac{\beta T_s}{2}) + \frac{b_2 - a_2 \alpha}{\beta} e^{-\frac{\alpha T_s}{2}} \sin(\frac{\beta T_s}{2}) + IR \end{cases} \quad (13.18)$$

Rearranging,

$$\begin{cases} m_{11} V_C(0) + m_{12} I_L(0) = n_1 \\ m_{21} V_C(0) + m_{22} I_L(0) = n_2 \end{cases} \quad (13.19)$$

Where

$$m_{11} = \frac{1}{L} e^{-\frac{\alpha T_s}{2}} \sin(\frac{\beta T_s}{2})$$

$$m_{12} = e^{-\frac{\alpha T_s}{2}} [\beta \cos(\frac{\beta T_s}{2}) - \alpha \sin(\frac{\beta T_s}{2})] + \beta$$

$$n_1 = I e^{-\frac{\alpha T_s}{2}} [\beta \cos(\frac{\beta T_s}{2}) + \alpha \sin(\frac{\beta T_s}{2})] - \beta I$$

$$m_{21} = e^{-\frac{\alpha T_s}{2}} [\beta \cos(\frac{\beta T_s}{2}) + \alpha \sin(\frac{\beta T_s}{2})] + \beta$$

$$m_{22} = -\frac{1}{C} e^{-\frac{\alpha T_s}{2}} \sin(\frac{\beta T_s}{2})$$

$$n_2 = I e^{-\frac{\alpha T_s}{2}} [R\beta \cos(\frac{\beta T_s}{2}) - \frac{1 - \alpha RC}{C} \sin(\frac{\beta T_s}{2})] - \beta IR$$

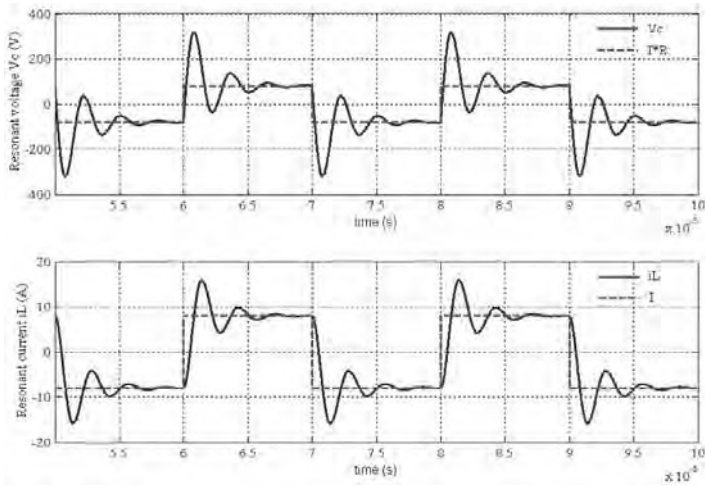


FIGURE 13.10

General waveforms of the resonant voltage v_c and current i_L .

Since all the parameters shown in the coefficients of Equation (13.19) are constant for a given circuit, the initial values of the resonant voltage and current can be calculated. Thus, the complete expressions of the resonant voltage and current are obtained by substituting $V_c(0)$ and $I_L(0)$ into Equation (13.14) and Equation (13.16).

Figure 13.10 shows the general waveforms of resonant voltage $v_c(t)$ and current $i_L(t)$. As seen, both of them are oscillatory and track-following. Actually, further investigation of Equation (13.14) states that inductor current can be rewritten as:

$$i_L(t) = a_1 e^{-\alpha t} \cos \beta t + \frac{b_1 - a_1 \alpha}{\beta} e^{-\alpha t} \sin \beta t + I = A e^{-\alpha t} \sin(\beta t + \varphi) + I \quad (13.20)$$

where

$$A = \sqrt{a_1^2 + \left(\frac{b_1 - a_1 \alpha}{\beta}\right)^2} \quad \varphi = \tan^{-1}\left(\frac{a_1 \beta}{b_1 - a_1 \alpha}\right)$$

It is apparent that the inductor current is composed of two different components. One is the oscillatory component, consisting of the sinusoidal function. The other is the compulsory component, given as the input current I . The oscillatory component is time-attenuation. With the time increasing, it will be attenuated to zero and the inductor current is then convergent to the compulsory component. The attenuating rate is determined by the damping ratio α . Larger ratios cause faster attenuation. Similar conclusions can also be made about the capacitor voltage $v_c(t)$.

When the value of damping factor $e^{-\alpha T_s/2}$ is approaching 1, the resonant voltage and current will contain an undamped oscillatory component. Hence, the coefficients in Equation (13.19) can be simplified accordingly, giving:

$$m'_{11} = \frac{1}{L} \sin\left(\frac{\beta T_s}{2}\right)$$

$$m'_{12} = \beta \cos\left(\frac{\beta T_s}{2}\right) - \alpha \sin\left(\frac{\beta T_s}{2}\right) + \beta$$

$$n'_1 = \beta \left[\cos\left(\frac{\beta T_s}{2}\right) - 1 \right] I + \alpha \sin\left(\frac{\beta T_s}{2}\right) I$$

$$m'_{21} = \beta \cos\left(\frac{\beta T_s}{2}\right) + \alpha \sin\left(\frac{\beta T_s}{2}\right) + \beta$$

$$m'_{22} = -\frac{1}{C} \sin\left(\frac{\beta T_s}{2}\right)$$

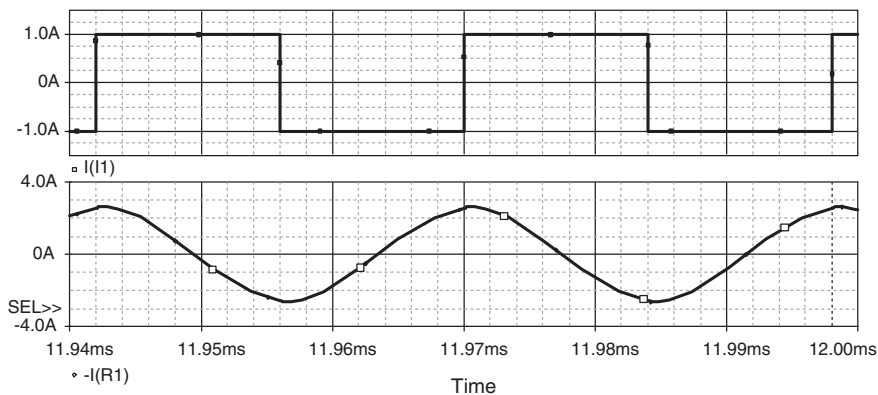
$$n'_2 = I \left[R \beta \cos\left(\frac{\beta T_s}{2}\right) - \frac{1 - \alpha RC}{C} \sin\left(\frac{\beta T_s}{2}\right) \right] - \beta IR$$

13.3.4 Simulation Results

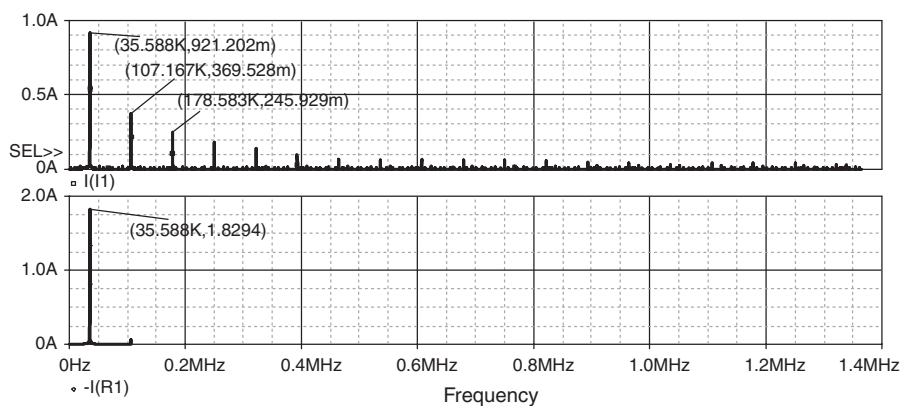
For the purpose of verifying the mathematical derivations, a prototype bipolar current source resonant inverter is proposed for simulation and experiments. The simulation is carried out by Pspice and the results are presented in [Figure 13.11a](#), where the upper channel is the input square-wave current I_i and the lower channel is the output current i_o , respectively. The corresponding FFT spectrums are shown in [Figure 13.11b](#). From the results, it can be found that the output current is very sleekly sinusoidal with the amplitude larger than the input fundamental current. The THD value is only 1.2%. It is obvious that the resonant network has the capability of attenuating the higher order harmonics in the input square-wave current and transferring their energy into the output current. Due to the advantages of high current transfer gain and negligible output harmonics, this inverter could be widely used in many high-frequency huge-current applications.

13.3.5 Experimental Results

The corresponding resonant waveforms under this condition are shown in [Figure 13.12](#), where both the capacitor voltage and the inductor current, i.e., output current are undamped oscillatory.



(a) The input and output current waveforms



(b) The corresponding FFT spectra

FIGURE 13.11

The simulation waveforms of the input and output currents.

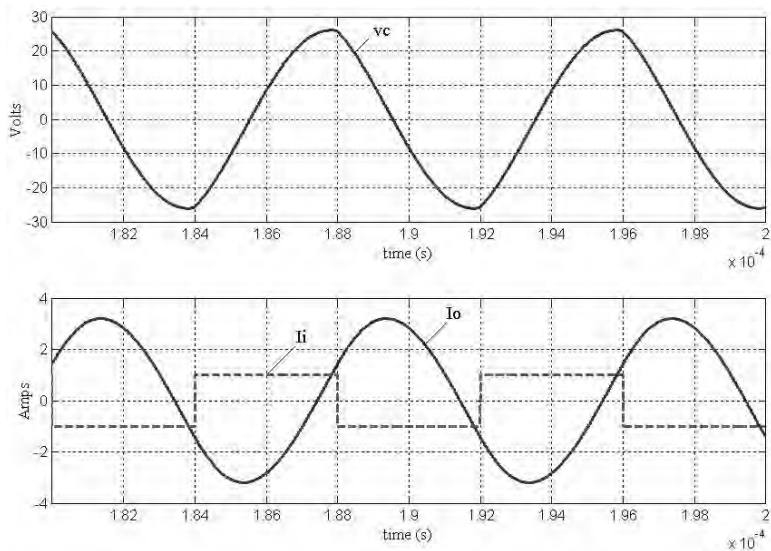


FIGURE 13.12

Tested waveforms of the resonant voltage and current under undamped condition.

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Π-CLL Current Source Resonant Inverter

14.1 Introduction

This chapter introduces a three-element current source resonant inverter (CSRI): Π -CLL CSRI consists of three energy-storage elements CLL, the Π -CLL. A bipolar current source is employed in this circuit as described in the previous chapter and shown in [Figure 13.7](#). Since there is no transformer and the circuit is not working in push-pull operation, the control circuit is very simple and power losses are low. This Π -CLL CSRI is shown in [Figure 14.1](#). The energy source is a DC voltage V_{in} , which is chopped by two mains switches S_1 and S_2 . The three energy-storing elements are C , L_1 and L_2 . Two inductors can be different, i.e., $L_2 = p L_1$ with p as a random value. The load can be a coil, transformer or HF annealing equipment. A resistance R_{eq} is assumed. Its equivalent circuit diagram is shown in [Figure 14.2](#).

14.1.1 Pump Circuits

In this application two boost pumps are used working at the conduction duty $k = 0.5$. Each pump consists of the common DC voltage source V_{in} , a switch S , and a large inductor L . The pump-out energy is usually measured by output current injection.

14.1.2 Current Source

An ideal current source has infinite impedance and constant output current. If the inductance of the pump circuits is large enough, the current flowing through it may keep a nearly constant value. The internal equivalent impedance of the pump is very high. The ripple of the inductor current depends on the input voltage, inductor's inductance, switching frequency, and conduction duty.

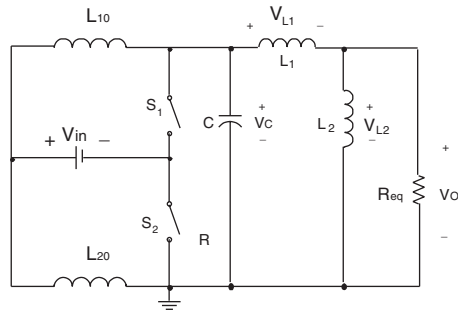


FIGURE 14.1
The Π -CLL current source resonant inverter.

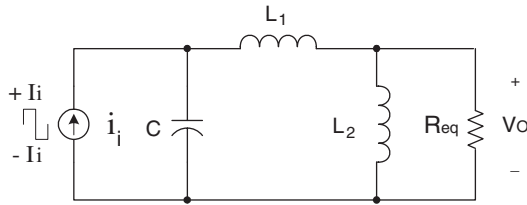


FIGURE 14.2
The equivalent circuit.

14.1.3 Resonant Circuit

Like other resonant inverters, this Π -CLL CSRI consists of a resonant circuit sandwiched between the current source (input switching circuit) and the output load. The resonant circuit can be considered as a Π -CLL low-pass filter. By network theory, these three components construct a circuit that is no longer a real low-pass filter. Therefore, the Π -CLL circuit has two peak resonant points. It gives more convenience to designers to match in the industrial applications.

14.1.4 Load

Load is usually resistive load or inductive plus resistive load. To simplify the problem we use R_{eq} to represent either an actual or an equivalent resistance, to consume the output power. This assumption is reasonable, because the load inductance can be considered the parallel part to the inductor L_2 .

14.1.5 Summary

The switching circuit consists of two pumps (two boost pumps employed): the R_{eq} is as mentioned, either an actual or an equivalent AC load resistance.

The source current i_i is a constant current yielded by input voltage V_i via large inductors L_{10} and L_{20} . To operate this circuit, S_1 is turned on and off in 180° (S_2 is idle) at the frequency $\omega = 2\pi f$. After the switching circuit, input current can be considered a bipolar square-wave current alternating in value between $+I_i$ and $-I_i$ that is then input to the resonant circuit section. The equivalent circuit is shown in [Figure 14.2](#).

14.2 Mathematic Analysis

In order to concentrate the function analysis of this Π -CLL, we assume:

1. The inverter's source is a constant current source determined by the pump circuits.
2. Two MOSFETs in the switching circuit are turned-on and turned-off 180° out of phase with each other at same switching frequency and with a duty cycle of 50%.
3. Two switches are ideal components without on-resistance, and negligible parasitic capacitance and zero switching time.
4. Two diodes are components having a zero forward voltage drop and forward resistance.
5. Four energy-storage elements are passive, linear, time-invariant, and do not have parasitic reactive components.

Using these assumptions, the following analyses are based on using [Figure 14.2](#).

14.2.1 Input Impedance

This CSRI is a third-order system. The mathematic analysis of operation and stability is more complex than three energy-storage element current source resonant inverters. The input impedance is given by

$$Z(\omega) = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq} (L_1 + L_2)}{R_{eq} [1 - \omega^2 (L_1 + L_2)C] + j\omega L_2 (1 - \omega^2 L_1 C)} \quad (14.1)$$

The corresponding phase angle is

$$\phi(\omega) = \tan^{-1} \left\{ \frac{\omega R_{eq} (L_1 + L_2)}{-\omega^2 L_1 L_2} \right\} - \tan^{-1} \left\{ \frac{\omega L_2 (1 - \omega^2 L_1 C)}{R_{eq} [1 - \omega^2 (L_1 + L_2)C]} \right\} \quad (14.2)$$

Define

$$B(\omega) = R_{eq}[1 - \omega^2(L_1 + L_2)C] + j\omega L_2(1 - \omega^2 L_1 C) \quad (14.3)$$

So that

$$Z(\omega) = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq}(L_1 + L_2)}{B(\omega)} \quad (14.4)$$

14.2.2 Components' Voltages and Currents

This Π -CLL CSRI has three resonant components C , L_1 , and L_2 , and the output equivalent resistance R_{eq} . In order to compare with the parameters easily, all components' voltages and currents are responded to the input fundamental current I_i . All transfer functions are in frequency domain (ω -domain).

Voltage and current on capacitor C :

$$\frac{V_C(\omega)}{I_{in}(\omega)} = Z(\omega) = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq}(L_1 + L_2)}{B(\omega)} \quad (14.5)$$

$$\frac{I_C(\omega)}{I_i(\omega)} = \frac{-\omega^2 R_{eq} C(L_1 + L_2) - j\omega^3 C L_1 L_2}{B(\omega)} \quad (14.6)$$

Voltage and current on inductor L_1 :

$$\frac{V_{L1}(\omega)}{I_{in}(\omega)} = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq} L_1}{B(\omega)} \quad (14.7)$$

$$\frac{I_{L1}(\omega)}{I_{in}(\omega)} = \frac{R_{eq} + j\omega L_2}{B(\omega)} \quad (14.8)$$

Voltage and current on inductor L_2 :

$$\frac{V_{L2}(\omega)}{I_{in}(\omega)} = \frac{j\omega R_{eq} L_2}{B(\omega)} \quad (14.9)$$

$$\frac{I_{L2}(\omega)}{I_{in}(\omega)} = \frac{R_{eq}}{B(\omega)} \quad (14.10)$$

The output voltage and current on the resistor R_{eq} :

$$\frac{V_O(\omega)}{I_{in}(\omega)} = \frac{V_{L_2}(\omega)}{I_{in}(\omega)} = \frac{j\omega R_{eq} L_2}{B(\omega)} \quad (14.11)$$

The current transfer gain is given by

$$\begin{aligned} g(\omega) &= \frac{I_O(\omega)}{I_{in}(\omega)} = \frac{j\omega L_2}{B(\omega)} = \frac{j\omega L_2}{R_{eq}[1 - \omega^2(L_1 + L_2)C] + j\omega L_2(1 - \omega^2 L_1 C)} \\ &= \frac{1}{(1 - \omega^2 L_1 C) - j \frac{R_{eq}[1 - \omega^2(L_1 + L_2)C]}{\omega L_2}} = |g| \angle \theta \end{aligned} \quad (14.12)$$

Thus,

$$|g(\omega)| = \frac{1}{\sqrt{(1 - \omega^2 L_1 C)^2 + \frac{R_{eq}^2 [1 - \omega^2(L_1 + L_2)C]^2}{(\omega L_2)^2}}} \quad (14.13)$$

$$\theta(\omega) = \tan^{-1} \frac{R_{eq} [1 - \omega^2(L_1 + L_2)C]}{\omega L_2 (1 - \omega^2 L_1 C)} \quad (14.14)$$

14.2.3 Simplified Impedance and Current Gain

Usually, we are interested in the input impedance and output current gain rather than all transfer functions listed in previous section. To simplify the operation, we can select:

$$\omega_0 = \frac{1}{\sqrt{L_1 C}} \quad \beta = \frac{\omega}{\omega_0} \quad Q = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 C R_{eq}} \quad \text{and} \quad p = \frac{L_2}{L_1}$$

Hence

$$\begin{aligned} Z(\omega) &= \frac{-\beta^2 \omega_0^2 L_1 L_2 + j\beta \omega_0 R_{eq} (L_1 + L_2)}{R_{eq} [1 - \beta^2 \omega_0^2 (L_1 + L_2)C] + j\beta \omega_0 L_2 (1 - \beta^2 \omega_0^2 L_1 C)} \\ &= \frac{-\beta^2 \omega_0^2 p L_1^2 + j\beta \omega_0 R_{eq} L_1 (1 + p)}{R_{eq} [1 - \beta^2 \omega_0^2 L_1 (1 + p)C] + j\beta \omega_0 p L_1 (1 - \beta^2 \omega_0^2 L_1 C)} \\ &= \frac{-p(\beta Q R_{eq})^2 + j(1 + p)\beta Q R_{eq}^2}{R_{eq} \{[1 - (1 + p)\beta^2] + jp\beta Q(1 - \beta^2)\}} = |Z| \angle \phi \end{aligned} \quad (14.15)$$

Then obtain,

$$B(\beta) = R_{eq}[1 - (1 + p)\beta^2 + jp\beta Q(1 - \beta^2)] \quad (14.16)$$

and

$$\begin{aligned} \phi(\omega) &= \tan^{-1} \left\{ \frac{\beta \omega_0 R_{eq} L_1 (1 + p)}{-p\beta^2 \omega_0^2 L_1^2} \right\} - \tan^{-1} \left\{ \frac{p\beta \omega_0 L_1 (1 - \beta^2 \omega_0^2 L_1 C)}{R_{eq}[1 - \beta^2 \omega_0^2 L_1 (1 + p)C]} \right\} \\ &= \tan^{-1} \frac{1 + p}{-p\beta Q} - \tan^{-1} \frac{p\beta Q(1 - \beta^2)}{1 - \beta^2(1 + p)} \\ &= \pi - \tan^{-1} \frac{1 + p}{p\beta Q} - \tan^{-1} \frac{p\beta Q(1 - \beta^2)}{1 - \beta^2(1 + p)} \end{aligned} \quad (14.17)$$

Therefore,

$$Z = \frac{-p\beta^2 Q^2 + j\beta Q(1 + p)}{1 - (1 + p)\beta^2 + jp\beta Q(1 - \beta^2)} R_{eq} = |Z| \angle \theta \quad (14.18)$$

where

$$\begin{aligned} |Z| &= \frac{\sqrt{p^2 \beta^4 Q^4 + \beta^2 Q^2 (1 + p)^2}}{\sqrt{[1 - (1 + p)\beta^2]^2 + [p\beta Q(1 - \beta^2)]^2}} R_{eq} \\ |Z| &= \frac{\sqrt{(p\beta^2 Q^2)^2 + [\beta Q(1 + p)]^2}}{\sqrt{[1 - (1 + p)\beta^2]^2 + [p\beta Q(1 - \beta^2)]^2}} R_{eq} \end{aligned} \quad (14.19)$$

and

$$\phi = \pi - \tan^{-1} \frac{1 + p}{p\beta Q} - \tan^{-1} \frac{p\beta Q(1 - \beta^2)}{1 - (1 + p)\beta^2}$$

The characteristics of input impedance $|Z|/R_{eq}$ vs. relevant frequency β referring to $p = 0.5$ and various Q , is shown in [Figure 14.3](#) and [Table 14.1](#).

The characteristics of phase angle ϕ vs. relevant frequency β referring to $p = 0.5$ and various Q , is shown in [Figure 14.4](#) and [Table 14.2](#).

The current transfer gain becomes

$$g = \frac{1}{\frac{1 - (1 + p)\beta^2}{jpQ} + 1 - \beta^2} = |g| \angle \theta \quad (14.20)$$

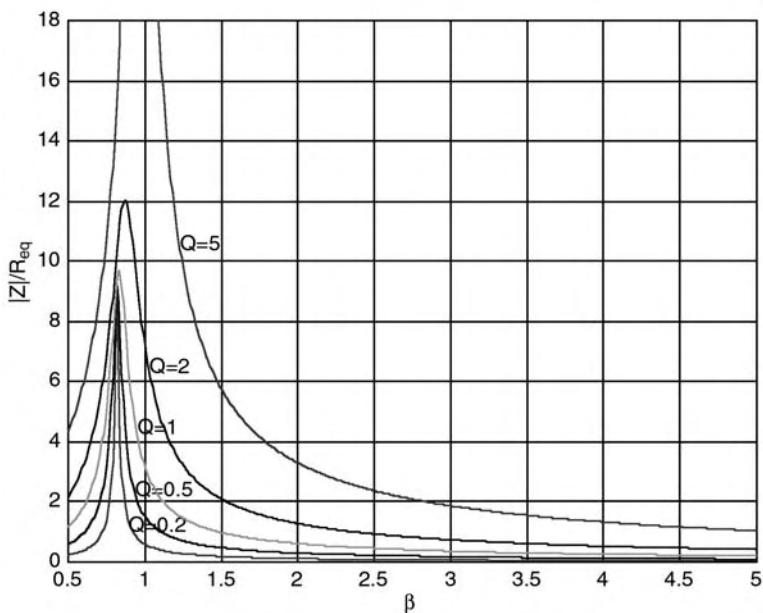


FIGURE 14.3
The curves of $|Z|/R_{eq}$ vs. β referring to Q .

TABLE 14.1

$|Z|/R_{eq}$ vs. β Referring to $p = 0.5$ and Various Q

	$\beta = 0.5$	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.2397	0.6513	1.5266	5.9126	0.6013	0.1898	0.1202	0.0721	0.0412
0.5	0.5954	1.5809	3.4353	8.6490	1.5207	0.4790	0.3029	0.1814	0.1033
1	1.1652	2.8924	5.3662	9.6875	3.1623	0.9852	0.6183	0.3673	0.2076
2	2.1693	4.6483	7.1323	10.9302	7.2111	2.1031	1.2804	0.7437	0.4162
5	4.3323	7.9346	11.0396	16.4384	29.1548	5.7645	3.3015	1.8719	1.0415

where

$$|g| = \frac{1}{\sqrt{\left[\frac{1-(1+p)\beta^2}{pQ}\right]^2 + (1-\beta^2)^2}} \quad (14.21)$$

and

$$\theta = -\tan^{-1} \frac{1-(1+p)\beta^2}{p(1-\beta^2)Q}$$

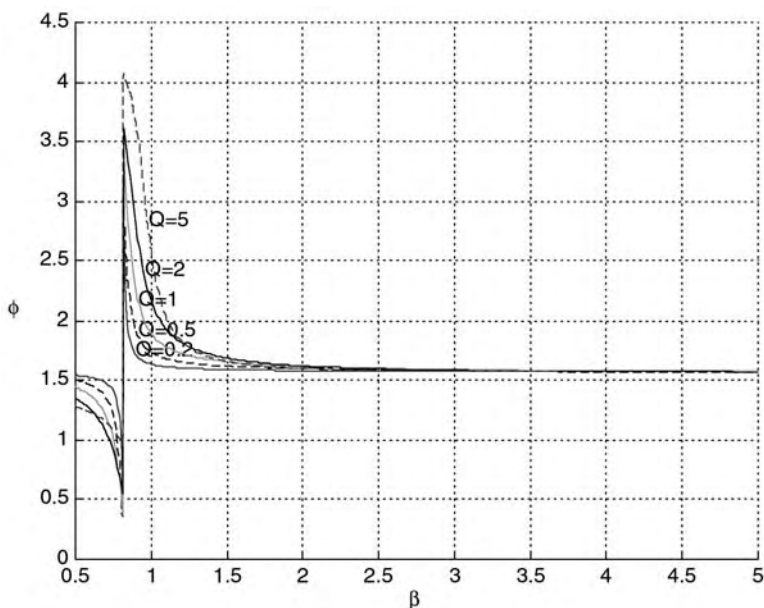


FIGURE 14.4
The curves of ϕ vs. β referring to Q .

TABLE 14.2

ϕ vs. β Referring to $p = 0.5$ and Various Q

	$\beta = 0.5$	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	1.5442	1.4985	1.4008	2.2849	1.6374	1.5917	1.5839	1.5785	1.5749
0.5	1.5050	1.3965	1.1856	2.8022	1.7359	1.6209	1.6011	1.5869	1.5776
1	1.4445	1.2601	0.9755	3.1587	1.8925	1.6585	1.6184	1.5912	1.5769
2	1.3521	1.1276	0.8863	3.5185	2.1588	1.6879	1.6220	1.5873	1.5746
5	1.2827	1.1732	1.0760	4.0348	2.6012	1.6593	1.6011	1.5788	1.5724

The characteristics of current transfer gain $|g|$ vs. relevant frequency β referring to $p = 0.5, 1$ and 2 , and various Q , is shown in [Figure 14.5](#) to [Figure 14.7](#) and [Table 14.3](#) to [Table 14.5](#).

The characteristics of the phase angle θ vs. relevant frequency β referring to $p = 0.5$ and various Q , is shown in [Figure 14.8](#) and [Table 14.6](#).

For various β and Q we have different current transfer gain. For example, when $\beta^2 = 1$ with any p , we have $g = -jQ = Q \angle 90^\circ$. It means that the output current can be larger than the fundamental harmonic of the input current! The larger the value of Q is, the higher the gain g .

Actually, set $\beta^2 = t$, we can find the maximum $|g|$ from

$$\frac{d}{dt}|g| = 0$$

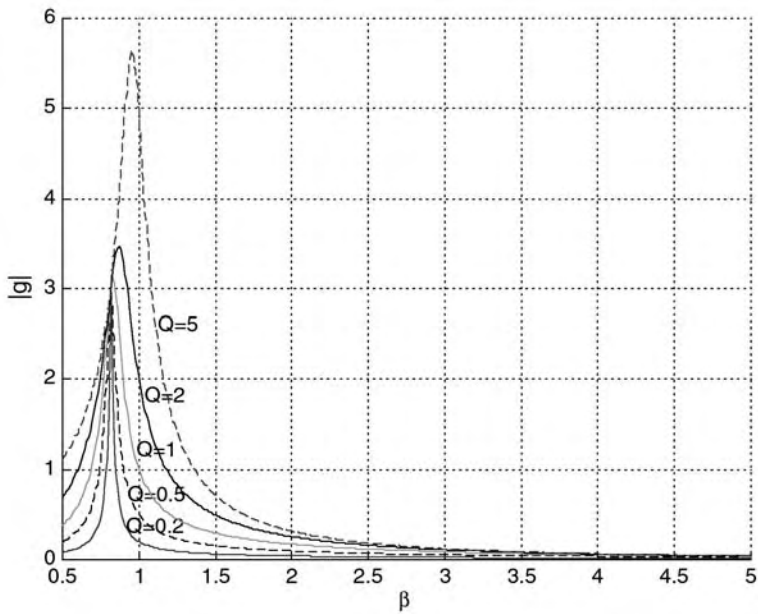


FIGURE 14.5

The curves of $|g|$ vs. β referring to Q .

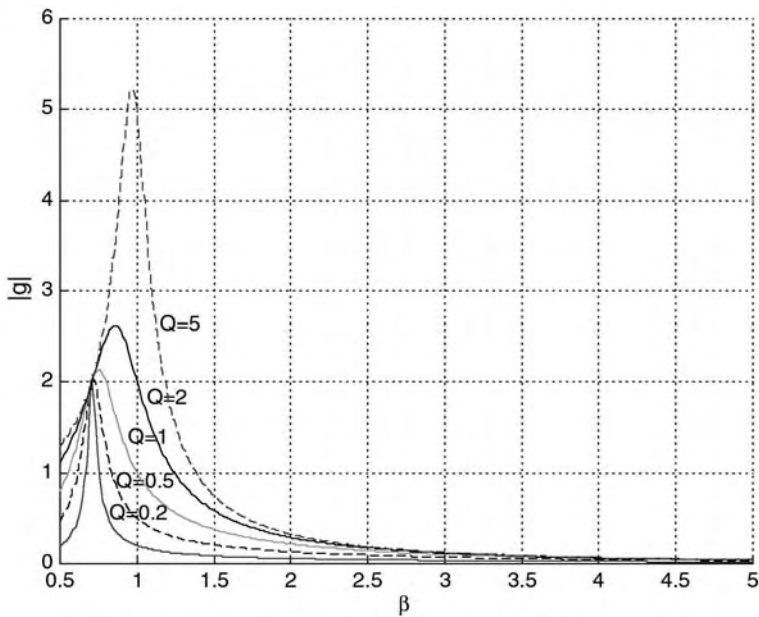


FIGURE 14.6

The curves of $|g|$ vs. β referring to Q .

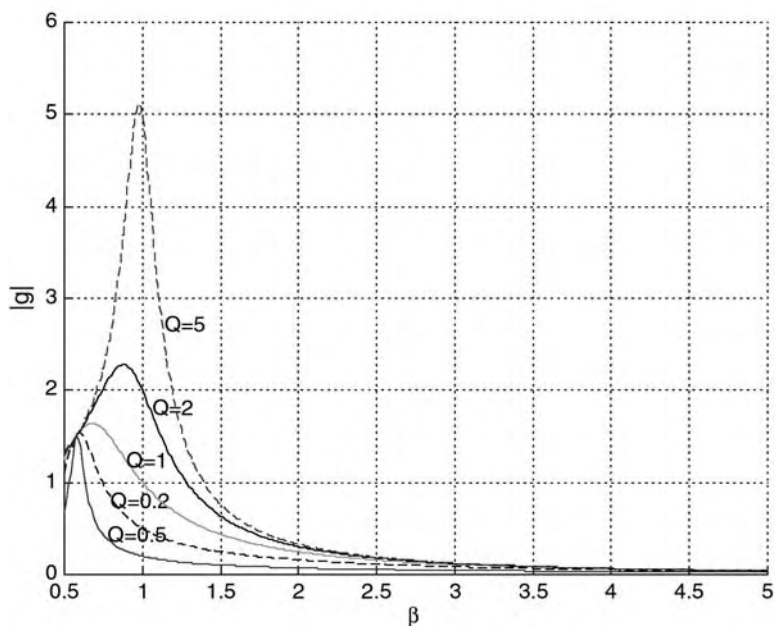


FIGURE 14.7
The curves of $|g|$ vs. β referring to Q .

TABLE 14.3

$|g|$ vs. β Referring to $p = 0.5$ and Various Q

	$\beta = 0.5$	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.0799	0.2169	0.5082	1.9679	0.2000	0.0630	0.0397	0.0236	0.0130
0.5	0.1978	0.5236	1.1361	2.8558	0.5000	0.1549	0.0958	0.0541	0.0265
1	0.3831	0.9404	1.7346	3.1122	1.0000	0.2937	0.1715	0.0866	0.0356
2	0.6860	1.4119	2.1236	3.1879	2.0000	0.4957	0.2561	0.1109	0.0399
5	1.1094	1.7528	2.2895	3.2101	5.0000	0.7136	0.3162	0.1224	0.0414

TABLE 14.4

$|g|$ vs. β Referring to $p = 1$ and Various Q

	$\beta = 0.5$	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.1978	1.2446	0.9782	0.4353	0.2000	0.0852	0.0563	0.0340	0.0183
0.5	0.4682	1.6939	1.7609	1.0394	0.5000	0.2070	0.1313	0.0721	0.0323
1	0.8000	1.8075	2.1355	1.8138	1.0000	0.3778	0.2169	0.1020	0.0386
2	1.1094	1.8397	2.2734	2.5943	2.0000	0.5848	0.2879	0.1178	0.0408
5	1.2883	1.8490	2.3171	3.0850	5.0000	0.7495	0.3246	0.1238	0.0415

or

TABLE 14.5

$|g|$ vs. β Referring to $p = 2$ and Various Q

	$\beta = 0.5$	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.6860	0.6673	0.4184	0.3098	0.2000	0.1035	0.0711	0.0433	0.0227
0.5	1.1094	1.2862	0.9670	0.7563	0.5000	0.2480	0.1596	0.0848	0.0355
1	1.2649	1.6438	1.5694	1.4007	1.0000	0.4370	0.2457	0.1099	0.0398
2	1.3152	1.7918	2.0406	2.2360	2.0000	0.6349	0.3030	0.1207	0.0412
5	1.3304	1.8409	2.2720	2.9709	5.0000	0.7648	0.3279	0.1243	0.0416

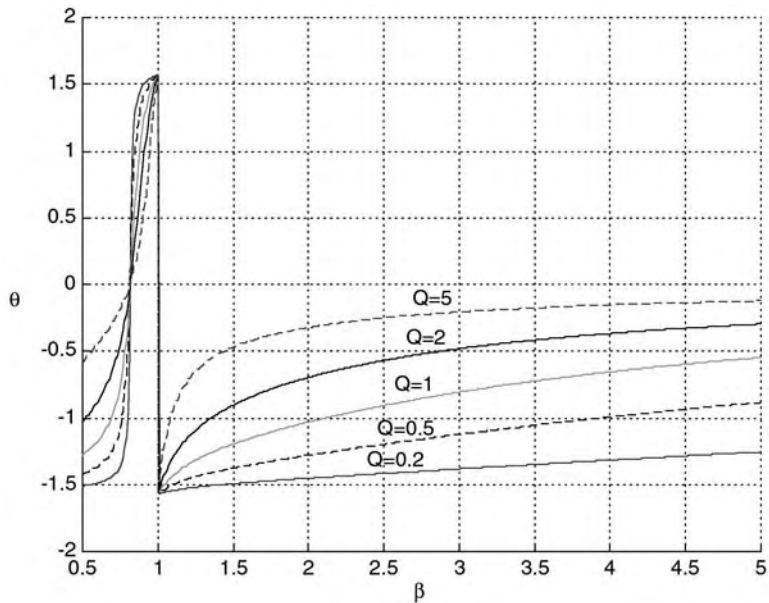


FIGURE 14.8
The curves of θ vs. β referring to Q .

TABLE 14.6

θ vs. β Referring to $p = 0.5$ and Various Q

	$\beta = 0.5$	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	-1.5109	-1.4533	-1.3505	0.9120	1.5708	-1.4920	-1.4514	-1.3811	-1.2532
0.5	-1.4219	-1.2840	-1.0604	0.4769	1.5708	-1.3759	-1.2793	-1.1233	-0.8828
1	-1.2793	-1.0378	-0.7290	0.2528	1.5708	-1.1948	-1.0304	-0.8058	-0.5465
2	-1.0304	-0.7030	-0.4200	0.1284	1.5708	-0.9025	-0.6947	-0.4802	-0.2953
5	-0.5880	-0.3268	-0.1768	0.0516	1.5708	-0.4690	-0.3218	-0.2054	-0.1211

$$\frac{1-(i+p)t}{pQ}(1+p)+(1-t)=0 \quad (14.22)$$

We obtain

$$t = \frac{1+p+pQ}{1+2p+p^2+pQ} = \frac{1}{1+\frac{p+p^2}{1+p+pQ}}$$

If taking $Q = 1$, $t = \beta^2 = 0.6$, or $\beta = 0.7746$, $|g| = 2.236$.

If this inverter is working at the conditions: $\beta = 1$ and $Q \gg 1$,

$$Z = \frac{jQ}{-1+j\frac{1}{Q}} R_{eq} \doteq -jQR_{eq} \quad (14.23)$$

$$\phi = \frac{\pi}{2} - \tan^{-1} \frac{1}{-Q} \doteq \frac{\pi}{2} - \pi = -\frac{\pi}{2}$$

correspondingly

$$g = \frac{1}{-jp/pQ} \doteq jQ \quad (14.24)$$

$$\theta = -\pi/2$$

The Π -CLL circuit is not only the resonant circuit, but the band-pass filter as well. All higher order harmonic components in the input current are effectively filtered by the Π -CLL circuit. The output current is nearly a pure sinusoidal waveform with the fundamental frequency $\omega = 2\pi f$.

14.2.4 Power Transfer Efficiency

The power transfer efficiency is a very important parameter and is calculated here. From [Figure 14.5](#) we know the input current is $i_i(\omega t)$, i.e.,

$$i_i(\omega t) = \begin{cases} +I_i & 2n\pi \leq \omega t \leq (2n+1)\pi \\ -I_i & (2n+1)\pi \leq \omega t \leq 2(n+1)\pi \end{cases} \quad \text{with } n = 0, 1, 2, 3, \dots \infty \quad (14.25)$$

where $I_i = V_1/Z + j\omega L_{10}$ that varies with different frequency.

This is a square waveform pulse-train. Using fast fourier transform (FFT), we have the spectrum form as

$$i_i(\omega t) = \frac{2I_i}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n+1)\omega t}{2n+1} \quad (14.26)$$

The fundamental frequency component is

$$i_{fund}(\omega t) = \frac{2I_i}{\pi} \sin \omega t \quad (14.27)$$

Output current is

$$i_2(\omega t) = g \frac{2I_i}{\pi} \sin \omega t \quad (14.28)$$

Because of the assumptions no power losses were considered. The power transfer efficiency from DC source to AC output is calculated in following equations. The total input power is

$$P_{in} = I_i^2 * \text{real}(Z) \quad (14.29)$$

The AC output power is gathered in the fundamental component that is

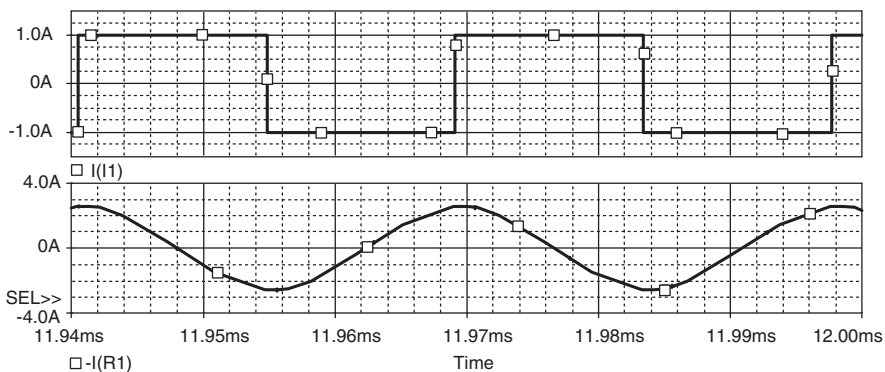
$$P_{fund} = (|g| \frac{2I_i}{\pi\sqrt{2}})^2 R_{eq} \quad (14.30)$$

The power transfer efficiency is

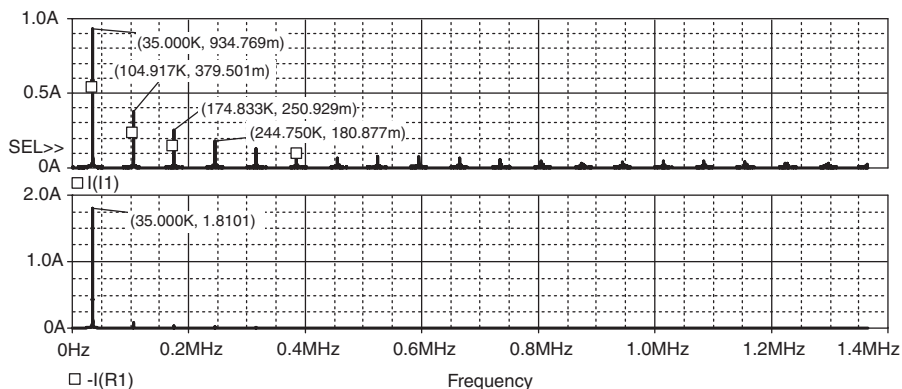
$$\eta = \frac{P_{fund}}{P_{in}} = \frac{\frac{2(I_i |g|)^2}{\pi^2} R_{eq}}{I_i^2 * \text{real}(Z)} = \frac{2|g|^2}{\pi^2} \cos \phi \quad (14.31)$$

14.3 Simulation Results

To verify the design and calculation results, PSpice simulation package was applied for these circuits. Choosing $V_I = 30$ V, all pump inductors $L_i = 10$ mH, the resonant capacitor $C = 0.2$ μ F, and inductors $L_1 = L_2 = 70$ μ H, load $R = 10$ Ω , $k = 0.5$ and $f = 35$ kHz. The input and output current waveforms are



(a) Input and output circuit waveforms of pi-CLL CSRI



(b) Corresponding FFT

FIGURE 14.9

Input and output current waveforms of Π -CLL circuit at $f = 35\text{KHz}$.

shown in Figure 14.9a. Their corresponding FFT spectrums are shown in Figure 14.9b. It is obviously illustrated that the output waveform is nearly a sinusoidal function, and its corresponding THD is nearly unity.

14.4 Discussion

14.4.1 Function of the Π -CLL Circuit

As a Π -CLC filter, it is a typical low-pass filter. All harmonics with frequency $\omega > \omega_0$ will be blocked. Π -CLL filter circuit has thoroughly different characteristics from that of low-pass filters. It allows the signal with higher frequency $\omega > \omega_0$ (it means $\beta > 1$ in Section 14.2) passing it and enlarging the energy.

14.4.2 Applying Frequency to this Π -CLL CSRI.

From our analysis and verifications we found the fact that the effective applying frequency to this Π -CLL current source resonant inverter is $(0.8 \text{ to } 2.0)f_0$. Outside this region both current transfer gain and efficiency are falling fast.

14.4.3 Explanation of $g > 1$

We recognized the fact that current transfer gain is greater than unity from mathematical analysis, and simulation and experimental results. The reason to enlarge the fundamental current is that the resonant circuit transfers the energy of other higher order harmonics to the fundamental component. Therefore the gain of the fundamental current can be greater than unity.

14.4.4 DC Current Component Remaining

Since the Π -CLL resonant circuit could not block the DC component, the output current still remains the same DC current component. This is not useful for most ordinary inverter applications.

14.4.5 Efficiency

From mathematical calculation and analysis, and simulation and experimental results, we can obtain very high efficiency. Its maximum value can be nearly unity! It means this Π -CLL resonant circuit can transfer the energy from not only higher order harmonics, but also a DC component into the fundamental component.

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Cascade Double Γ -CL Current Source Resonant Inverter

15.1 Introduction

This chapter introduces a four-element current source resonant inverter (CSRI): a cascade double Γ -type C-L circuit CSRI. Its circuit diagram is shown in [Figure 15.1](#). It consists of four energy-storage elements, the double Γ -CL: C_1 - L_1 and C_2 - L_2 . The energy source is a DC voltage V_{in} chopped by two main switches S_1 and S_2 to construct a bipolar current source, $i_i = \pm I_i$. The pump inductors L_{10} and L_{20} are equal to each other, and are large enough to keep the source current nearly constant during operation. The real load absorbs the delivered energy, its equivalent load should be proposed resistive, R_{eq} . The equivalent circuit diagram is shown in [Figure 15.2](#).

15.2 Mathematic Analysis

In order to concentrate the function analysis of this double cascade Γ -CL CSRI, assume:

1. The inverter's source is a constant current source determined by the pump circuits.
2. Two MOSFETs in the switching circuit are turned-on and turned-off 180° out of phase with each other at same switching frequency and with a duty cycle of 50%.
3. Two switches are ideal components without on-resistance, and negligible parasitic capacitance and zero switching time.
4. Two diodes are components having a zero forward voltage drop and forward resistance.
5. Four energy-storage elements are passive, linear, time-invariant, and do not have parasitic reactive components.

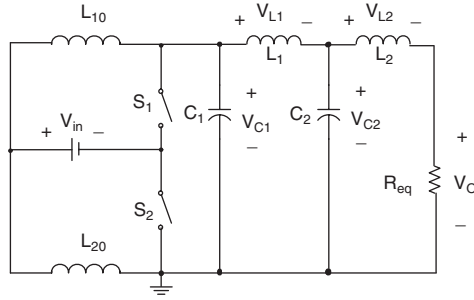


FIGURE 15.1
Cascade double Γ -CL CSRI.

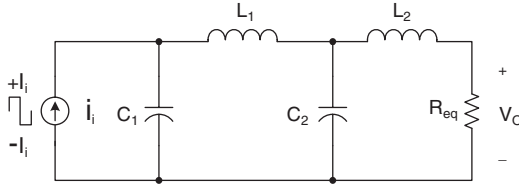


FIGURE 15.2
Equivalent circuit.

Based on these assumptions and the equivalent circuit the following analysis is derived.

15.2.1 Input Impedance

This CSRI is a fourth-order system. The mathematic analysis of operation and stability is more complex than three energy-storage element current source resonant inverters. The input impedance is given by

$$Z(\omega) = \frac{R_{eq}(1 - \omega^2 L_1 C_2) + j\omega(L_1 + L_2 - \omega^2 L_1 L_2 C_2)}{\left(1 - \omega^2(L_1 C_1 + L_2 C_1 + L_2 C_2) + \omega^4 L_1 L_2 C_1 C_2 \right) + j\omega R_{eq}(C_1 + C_2 - \omega^2 L_1 C_1 C_2)} \quad (15.1)$$

or

$$Z(\omega) = \frac{R_{eq}(1 - \omega^2 L_1 C_2) + j\omega(L_1 + L_2 - \omega^2 L_1 L_2 C_2)}{B(\omega)} \quad (15.2)$$

where

$$B(\omega) = 1 - \omega^2(L_1C_1 + L_2C_1 + L_2C_2) + \omega^4L_1L_2C_1C_2 + j\omega R_{eq}(C_1 + C_2 - \omega^2L_1C_1C_2) \quad (15.3)$$

15.2.2 Components, Voltages, and Currents

This CSRI has four resonant components C_1 , C_2 , L_1 and L_2 , plus the output equivalent resistance R_{eq} . In order to compare with the parameters easily, all components voltages and currents are responded to the input fundamental current I_i .

Voltage and current on capacitor C_1 is

$$\frac{V_{C1}(\omega)}{I_i(\omega)} = \frac{R_{eq}(1 - \omega^2L_1C_2) + j\omega(L_1 + L_2 - \omega^2L_1L_2C_2)}{B(\omega)} \quad (15.4)$$

$$\frac{I_{C1}(\omega)}{I_i(\omega)} = \frac{R_{eq}(1 - \omega^2L_1C_2) + j\omega(L_1 + L_2 - \omega^2L_1L_2C_2)}{B(\omega) / j\omega C_1} \quad (15.5)$$

Voltage and current on inductor L_1 is

$$\frac{V_{L1}(\omega)}{I_i(\omega)} = \frac{-R_{eq}\omega^2L_1C_2 + j\omega L_1(1 - \omega^2L_2C_2)}{B(\omega)} \quad (15.6)$$

$$\frac{I_{L1}(\omega)}{I_i(\omega)} = \frac{(1 - \omega^2L_2C_2) + jR_{eq}\omega C_2}{B(\omega)} \quad (15.7)$$

Voltage and current on capacitor C_2 is

$$\frac{V_{C2}(\omega)}{I_i(\omega)} = \frac{R_{eq} + j\omega L_2}{B(\omega)} \quad (15.8)$$

$$\frac{I_{C2}(\omega)}{I_i(\omega)} = \frac{-\omega^2L_2C_2 + jR_{eq}\omega C_2}{B(\omega)} \quad (15.9)$$

Voltage and current on inductor L_2 is

$$\frac{V_{L2}(\omega)}{I_i(\omega)} = \frac{j\omega L_2}{B(\omega)} \quad (15.10)$$

$$\frac{I_{L2}(\omega)}{I_i(\omega)} = \frac{1}{B(\omega)} \quad (15.11)$$

The output voltage and current on the resistor R_{eq} :

$$\frac{V_o(\omega)}{I_i(\omega)} = \frac{R_{eq}}{B(\omega)} \quad (15.12)$$

The current transfer gain is given by

$$g(\omega) = \frac{I_o(\omega)}{I_i(\omega)} = \frac{1}{B(\omega)} \quad (15.13)$$

15.2.3 Simplified Impedance and Current Gain

Usually, the input impedance and output current gain are paid more attention rather than other transfer functions listed in the previous section. To simplify the operation, select:

$$L_1 = L_2 = L; \quad C_1 = C_2 = C \quad \omega_0 = \frac{1}{\sqrt{LC}}$$

$$Q = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 C R_{eq}} \quad \beta = \frac{\omega}{\omega_0}$$

Obtain

$$B(\beta) = 1 - 3\beta^2 + \beta^4 + j \frac{2 - \beta^2}{Q} \beta \quad (15.14)$$

Therefore,

$$Z = \frac{(1 - \beta^2) + jQ(2 - \beta^2)}{1 - 3\beta^2 + \beta^4 + j \frac{2 - \beta^2}{Q} \beta} R_{eq} = |Z| \angle \phi \quad (15.15)$$

where

$$|Z| = \frac{\sqrt{(1 - \beta^2)^2 + Q^2(2 - \beta^2)^2}}{\sqrt{(1 - 3\beta^2 + \beta^4)^2 + \beta^2 \left(\frac{2 - \beta^2}{Q}\right)^2}} R_{eq}$$

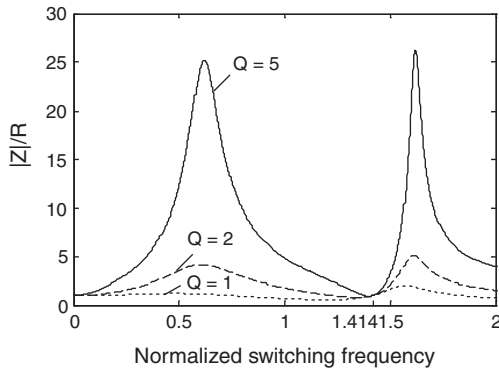


FIGURE 15.3

The curves of $|Z|/R_{eq}$ vs. β referring to Q .

TABLE 15.1

$|Z|/R_{eq}$ vs. β Referring to Various Q

	$\beta = 0.59$	1	1.2	1.414	1.59
$Q = 1$	1.1994	0.7071	0.5672	1.0000	2.0237
2	4.1662	1.7889	1.0955	1.0000	4.9137
5	23.464	4.9029	2.7031	1.0000	17.463

and

$$\phi = \tan^{-1} \frac{2 - \beta^2}{1 - \beta^2} Q - \tan^{-1} \frac{(2 - \beta^2)\beta}{(1 - 3\beta^2 + \beta^4)Q}$$

The characteristics of input impedance $|Z|/R_{eq}$ vs. relevant frequency β referring to various Q , is shown in Figure 15.3 and Table 15.1. The characteristics of phase angle ϕ vs. relevant frequency β referring to various Q , is shown in Figure 15.4 and Table 15.2. The current transfer gain becomes

$$g = \frac{1}{1 - 3\beta^2 + \beta^4 + j \frac{2 - \beta^2}{Q} \beta} = |g| \angle \theta \quad (15.20)$$

where

$$|g| = \frac{1}{\sqrt{(1 - 3\beta^2 + \beta^4)^2 + \beta^2 \left(\frac{2 - \beta^2}{Q}\right)^2}} \quad (15.21)$$

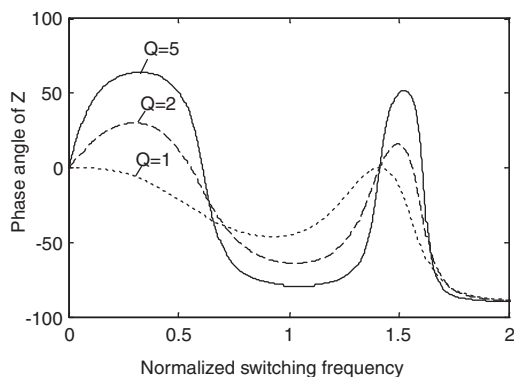


FIGURE 15.4
The curves of ϕ vs. β referring to Q .

TABLE 15.2

ϕ vs. β Referring to Various Q

	$\beta = 0.59$	1	1.2	1.414	1.59
$Q = 1$	-29.3	-45.0	-28.5	0.0	-48.3
2	-9.5	-63.4	-56.8	0.0	-17.6
5	13.9	-78.7	-76.4	0.0	29.0

and

$$\theta = -\tan^{-1} \frac{(2 - \beta^2)\beta}{(1 - 3\beta^2 + \beta^4)Q}$$

The characteristics of current transfer gain $|g|$ vs. relevant frequency β referring to various Q , is shown in [Figure 15.5](#) and [Table 15.3](#).

The characteristics of the phase angle θ vs. relevant frequency β referring to various Q , is shown in [Figure 15.6](#) and [Table 15.4](#).

For various β and Q , different current transfer gain is obtained. Actually, the maximum $|g|$ can be found from

$$\frac{d}{d\beta^2} |g| = 0$$

or

$$4\beta^6 + \left(\frac{3}{Q^2} - 18\right)\beta^4 + \left(22 - \frac{8}{Q^2}\right)\beta^2 + \left(\frac{4}{Q^2} - 6\right) = 0 \quad (15.22)$$

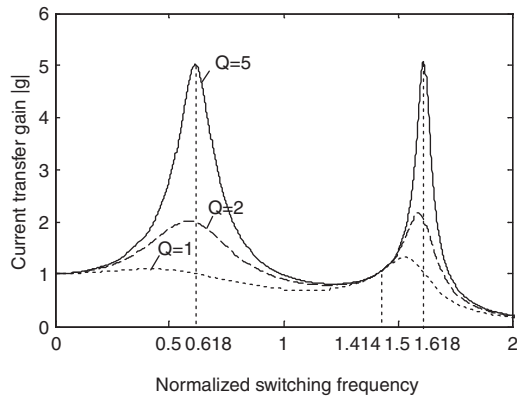


FIGURE 15.5
The curves of $|g|$ vs. β referring to Q .

TABLE 15.3

$|g|$ vs. β Referring to Various Q

	$\beta = 0.59$	1	1.2	1.414	1.59
$Q = 1$	1.0229	0.7071	0.7062	0.9994	1.1607
2	2.0270	0.8944	0.7747	0.9994	2.1641
5	4.7725	0.9806	0.7977	0.9994	3.9087

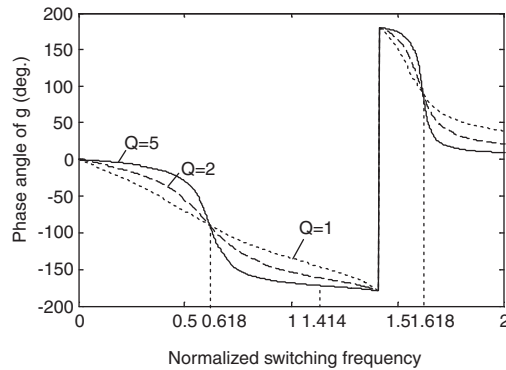


FIGURE 15.6
The curves of θ vs. β referring to Q .

when

$$Q = 2 \quad 4\beta^6 - 17.25\beta^4 + 20\beta^2 - 5 = 0 \quad (15.23)$$

TABLE 15.4 θ vs. β Referring to Various Q

	$\beta = 0.59$	1	1.2	1.414	1.59
$Q = 0.5$	-87.7	-116.6	-132.8	-180.0	96.6
1	-85.5	-135.0	-151.7	-180.0	102.9
2	-81.0	-153.4	-164.9	-180.0	114.7

yields

$$\beta_1 = 0.59 \quad \beta_2 = 1.20 \quad \beta_3 = 1.59$$

Take $\beta_3 = 1.59$ (the local maximum transfer gain is achieved at $\beta_1 = 0.59$), and the corresponding $|g(\beta)|$ is equal to 2.165.

In practice, Equation (15.23) is dependent on the qualify factor Q . For various load conditions, the maximum transfer gain will be achieved at different operating frequencies. When $Q \gg 1$, we then have

$$2\beta^6 - 9\beta^4 + 11\beta^2 - 3 = 0 \quad (15.24)$$

or

$$(2\beta^2 - 3)(1 - 3\beta^2 + \beta^4) = 0$$

yields three positive real roots as

$$\beta_4 = 0.618 \quad \beta_5 = 1.618 \quad \beta_6 = 1.225$$

It should be noted that two peaks exist in the transfer gain curves with corresponding frequencies at $\beta_4 = 0.618$ and $\beta_5 = 1.618$, respectively. The current transfer gain drops from the peak to the vale at $\beta_6 = 1.225$.

Taking further investigation, it is found that at the frequencies corresponding to peak gain, the following equation can be obtained,

$$1 - 3\beta^2 + \beta^4 = 0 \quad (15.25)$$

Thus, the current transfer gain at β_4 and β_5 is

$$|g(\beta)| = \frac{1}{\sqrt{(1 - 3\beta^2 + \beta^4)^2 + \left(\frac{2 - \beta^2}{Q}\right)^2 \beta^2}} \bigg|_{\beta_4, \beta_5} = Q \quad (15.26)$$

The relevant phase angle θ is

$$\theta_4 = -90^\circ \quad \theta_5 = 90^\circ$$

The results indicate that the current transfer gain is proportional to the quality factor Q . The larger the value of Q is, the higher the gain $|g(\beta)|$. For instance, when $Q = 1, 2$ and 5 with $\beta_4 = 0.618$ or $\beta_5 = 1.618$, $|g(\beta)|$ will have the same value. Note that although β_4 and β_5 are derived from the assumption of $Q \gg 1$, the Equation (15.26) is still valid for all the values of quality factors.

Furthermore, when $Q \ll 1$, Equation (15.22) can be rearranged as

$$3\beta^4 - 8\beta^2 + 4 = 0 \quad (15.27)$$

giving other two positive real roots as

$$\beta_7 = 0.816 \quad \beta_8 = 1.414$$

As seen from [Figure 15.5](#), the minimum transfer gain is achieved at β_7 while the maximum gain is obtained at β_8 . These characteristic points will be useful in the estimation of the transfer gain curves. Notice that for low Q values, the frequency characteristics of Cascade Double Γ -CL CSRI approach those of conventional series-loaded resonant inverters, especially when β is near to 1.414.

When $\beta = \beta_c = 1.414$ ($\beta_c^2 = 2$), all the curves will intersect at one point where the corresponding current transfer gain is

$$|g(\beta_c)| = \frac{1}{\sqrt{(1 - 3\beta_c^2 + \beta_c^4)^2 + \left(\frac{2 - \beta_c^2}{Q}\right)^2 \beta_c^2}} \equiv 1 \quad (15.28)$$

This point is always called load-independent point since the current transfer gain keeps constant with any value of quality factor Q .

If the inverter is working at the conditions:

$$\beta = 1 \text{ and } Q \gg 1$$

we then have

$$\begin{aligned} Z &= \frac{jQ}{-1 + j/Q} R_{eq} \approx -jQ R_{eq} \\ \phi &= \frac{\pi}{2} - \tan^{-1} \frac{1}{-Q} \approx \frac{\pi}{2} - \pi \approx -\frac{\pi}{2} \end{aligned} \quad (15.29)$$

and correspondingly

$$g(\beta) = \frac{1}{-1 + j/Q} = -1 \quad (15.30)$$

$$\theta = -\pi$$

The double Γ -CL circuit is not only the resonant circuit, but the band-pass filter as well. All higher order harmonic components in the input current are effectively filtered by the double Γ -CL circuit. The output current is nearly a pure sinusoidal waveform with the fundamental frequency $\omega = 2f$.

15.2.4 Power Transfer Efficiency

The power transfer efficiency is a very important parameter and it is calculated here. From [Figure 15.2](#), the input current is a bipolar value $i_i(\omega t)$:

$$i_i(\omega t) = \begin{cases} I_i & 2n\pi \leq \omega t \leq (2n+1)\pi \\ -I_i & (2n+1)\pi \leq \omega t \leq 2(n+1)\pi \end{cases} \quad \text{with } n = 0, 1, 2, 3, \dots \infty \quad (15.31)$$

where $I_i = V_1 / (Z + j\omega L_{10})$ ($L_{10} = L_{20}$) that varies with operating frequency.

This is a square waveform pulse-train. Applying fast Fourier transform (FFT), the spectrum form is

$$i_i(\omega t) = \frac{4I_i}{\pi} \sum_{n=0}^{\infty} \frac{\sin(2n+1)\omega t}{2n+1} \quad (15.32)$$

The fundamental frequency component is

$$i_{fund}(\omega t) = \frac{4I_i}{\pi} \sin \omega t \quad (15.33)$$

Output current is

$$i_o(\omega t) = g \frac{4I_i}{\pi} \sin \omega t \quad (15.34)$$

The power transfer efficiency from input current source to AC output load is analyzed and calculated. Since the input current is a square waveform the total input power is

$$P_{in} = I_i^2 |Z| \quad (15.35)$$

The output current is nearly a pure sinusoidal waveform, its root-mean-square value is its peak value times $1/\sqrt{2}$. Therefore the output power is

$$P_O = (|g| \frac{4I_i}{\pi\sqrt{2}})^2 R_{eq} = 8(|g| \frac{I_i}{\pi})^2 R_{eq} \quad (15.36)$$

We can get the power transfer efficiency as

$$\eta = \frac{P_O}{P_{in}} = \frac{8 \frac{(I_i |g|)^2}{\pi^2} R_{eq}}{I_i^2 |Z|} = \frac{8 |g|^2 R_{eq}}{\pi^2 |Z|} \quad (15.37)$$

Considering Equation (15.15) and Equation (15.21), we obtain:

$$\eta = \frac{8}{\pi^2} \frac{1}{\sqrt{(1-\beta^2)^2 + Q^2\beta^2(2-\beta^2)^2} \sqrt{(1-3\beta^2+\beta^4)^2 + \beta^2(\frac{2-\beta^2}{Q})^2}} \quad (15.38)$$

If $\beta^2 = 2$ ($\beta = 1.414$) with any Q , $\eta = 0.8106$.

If $\beta^2 = 1$ ($\beta = 1$) and $Q = 1$, $\eta = 0.5732$.

If $\beta^2 = 2.5$ ($\beta = 1.581$) and $Q = 1$, $\eta = 0.5771$.

If $\beta^2 = 2.618$ ($\beta = 1.618$) and $Q = 1$, $\eta = 0.4263$.

Therefore, the characteristics of efficiency η vs. relevant frequency β referring to various Q is obtained, and shown in [Figure 15.7](#) and [Table 15.5](#).

15.3 Simulation Result

In order to verify analysis and calculation, using PSpice software simulation method to obtain a set of simulation waveforms as shown in [Figure 15.8](#) to [Figure 15.9](#) corresponding to $Q = 2$ and $\beta = 1, 1.414$, and 1.59 . The parameter values are set below:

$$I = 1 \text{ A}, V_1 = 30 \text{ V}, L_{10} = L_{20} = 20 \text{ mH}, R_{eq} = 10 \text{ } \Omega, \\ C_1 = C_2 = C = 0.22 \text{ } \mu\text{F}, \text{ and } L_1 = L_2 = L = 100 \text{ } \mu\text{H}.$$

Therefore, $\omega_0 = 213 \text{ krad/s}$, $f_0 = 33.93 \text{ kHz}$, and $Q = 2$. The particular frequencies for the figures are $f = 33.9 \text{ kHz}$, 48.0 kHz and 54.0 kHz . In order to pick the input current a small resistance $R_0 = 0.001 \text{ } \Omega$ is employed. The load in the simulation circuit is R rather than R_{eq} .

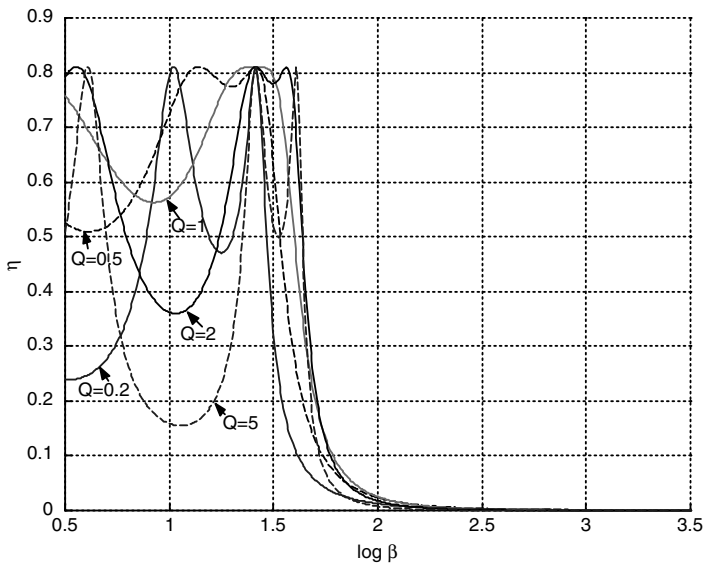
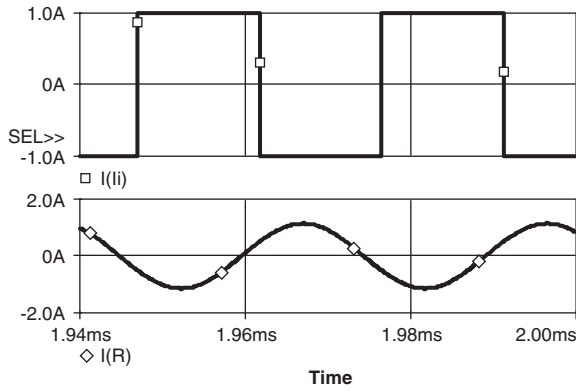


FIGURE 15.7
Curves of η vs. β referring to Q .

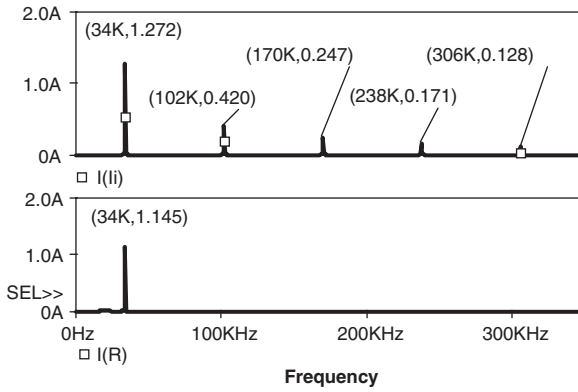
TABLE 15.5
 η vs. β Referring to Various Q

	$\beta = 0.618$	0.8	1	1.414	1.581	1.618	2	3	4	5
$Q = 0.2$	0.2496	0.3527	0.7948	0.8106	0.1359	0.0995	0.0127	0.0008	0.0001	0.0000
0.5	0.5098	0.5559	0.7250	0.8106	0.3268	0.2394	0.0238	0.0009	0.0001	0.0000
1	0.6895	0.5885	0.5732	0.8106	0.5771	0.4263	0.0253	0.0006	0.0001	0.0000
2	0.7745	0.4927	0.3625	0.8106	0.7955	0.6304	0.0176	0.0003	0.0000	0.0000
5	0.8045	0.2680	0.1590	0.8106	0.6473	0.7715	0.0079	0.0001	0.0000	0.0000

All figures have two parts a and b. Figure a shows the input and output current waveforms, and b shows the corresponding FFT spectrum. The first channel of Figure 15.11a to Figure 15.13a is the input current flowing through resistance R_o , which corresponds to the input current $i_i(\omega t)$. It is a square waveform pulse train with the pulse-width $\omega t = \pi$. The second channel of Figure 15.11a to Figure 15.13a is the output current flowing through resistance R . From Figure 15.11b to Figure 15.13b, the first channel of each figure is the corresponding input current FFT spectrum. The second channel of each figure is the corresponding output current FFT spectrum. From the spectrums, it can be clearly seen that there is only mono-frequency existing in output currents. All output current waveforms are very pure sinusoidal function.



(a) Input and output current waveforms



(b) The corresponding FFT spectrum of input and output current waveforms

FIGURE 15.8

Input and output current waveforms at $f = 33.9$ kHz.

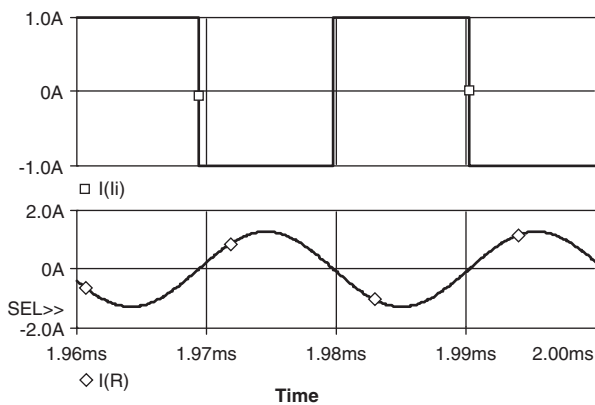
15.3.1 $\beta = 1$, $f = 33.9$ kHz, $T = 29.5$ μ s

The waveforms and corresponding FFT spectrums are shown in Figure 15.8. The THD = 0 and current transfer gain is

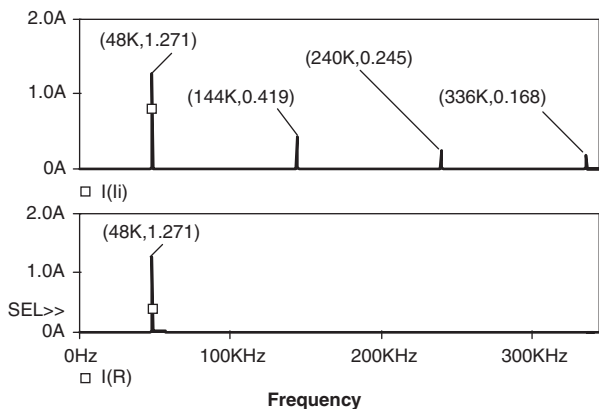
$$g = \frac{I(R)}{I(R)_1} \Big|_{f=33.9\text{kHz}} = \frac{1.145}{1.272} = 0.9002$$

15.3.2 $\beta = 1.4142$, $f = 48.0$ kHz, $T = 20.83$ μ s

The waveforms and corresponding FFT spectrums are shown in Figure 15.9. The THD = 0 and current transfer gain is



(a) Input and output current waveforms



(b) The corresponding FFT spectrum of input and output current waveforms

FIGURE 15.9

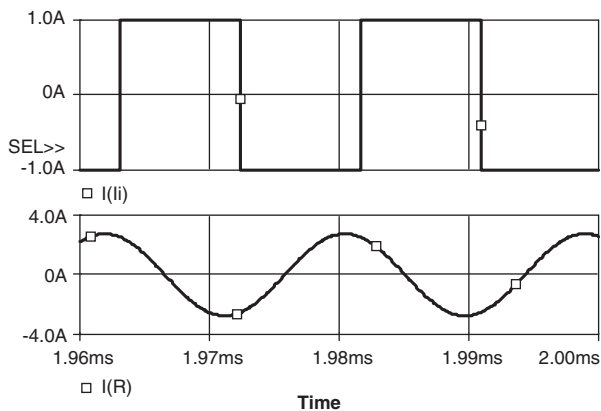
Input and output current waveforms at $f = 48$ kHz.

$$g = \frac{I(R)}{I(R)_1} \Big|_{f=48\text{kHz}} = \frac{1.271}{1.271} = 1.00$$

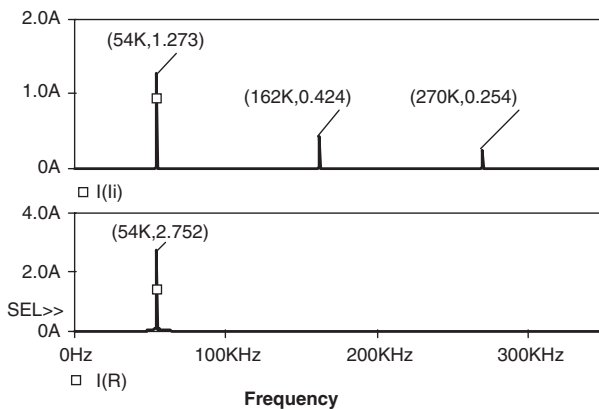
15.3.3 $\beta = 1.59$, $f = 54$ kHz, $T = 18.52$ μs

The waveforms and corresponding FFT spectrums are shown in [Figure 15.10](#). The THD = 0 and current transfer gain is

$$g = \frac{I(R)}{I(R)_1} \Big|_{f=54\text{kHz}} = \frac{2.752}{1.273} = 2.162$$



(a) Input and output current waveforms



(b) The corresponding FFT spectrum of input and output current waveforms

FIGURE 15.10

Input and output current waveforms at $f = 54$ kHz.

15.4 Experimental Result

In order to verify our analysis and calculation, a test rig with the same components was constructed:

$$I = 1 \text{ A}, V_1 = 30 \text{ V}, L_{10} = L_{20} = 20 \text{ mH}, R_{eq} = 10 \Omega, \\ C_1 = C_2 = C = 0.22 \mu\text{F}, \text{ and } L_1 = L_2 = L = 100 \mu\text{H}.$$

Therefore, $\omega_0 = 213 \text{ krad/s}$, $f_0 = 33.93 \text{ kHz}$, and $Q = 2$. The MOSFET device is IRF640 ($R_{ds} = 0.15 \text{ ohm}$, $C_{ds} = 140 \text{ pF}$). Since the junction capacitance of C_{ds}

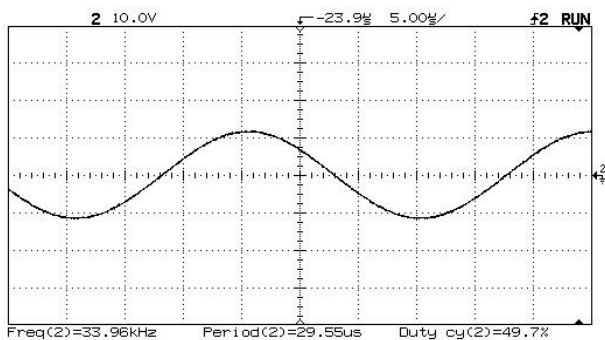


FIGURE 15.11
Testing waveform of the output voltage at $\beta = 1$.

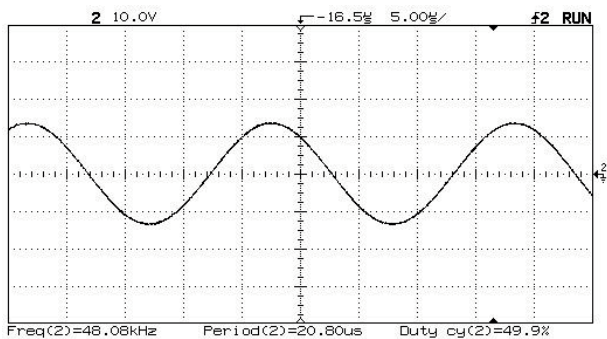


FIGURE 15.12
Testing waveform of the output voltage at $\beta = 1.414$.

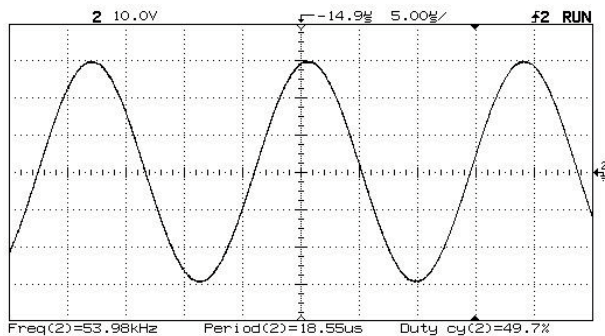


FIGURE 15.13
Testing waveform of the output voltage at $\beta = 1.59$.

is much smaller than the resonance capacitance $C = 0.22 \mu\text{F}$ ($C/C_{ds} = 1429$), it does not affect the experimental results. The output current waveform is a perfect sine function. A set of tested output voltage waveforms that correspond to the output current with $\beta = 1, 1.4142$, and 1.59 is shown in Figure 15.11 to Figure 15.13. The particular applied frequencies for the figures are $f = 33.9 \text{ kHz}$, 48.0 kHz , and 54.0 kHz , and peak-to-peak voltage $V_{pp} = 28.1 \text{ V}$, 40.3 V , 71.9 V , and 65.5 V , which are very close to the values in Figure 15.8 to Figure 15.10.

15.5 Discussion

15.5.1 Function of the Double Γ -CL Circuit

Single Γ -CL filter is a well-known circuit. As a Π -CLC filter, it is a typical low-pass filter. All harmonics with frequency $\omega > \omega_0$ will be blocked. Cascade double Γ -CL filter circuit has thoroughly different characteristics from that of low-pass filters. It allows the signal with higher frequency $\omega > \omega_0$ (it means $\beta > 1$ in Section 15.2) passing it and enlarging the energy.

15.5.2 Applying Frequency to this Double Γ -CL CSRI

From analysis and verifications it can be found the fact that the effective applying frequency to this double Γ -CL current source resonant inverter is $(0.6 \text{ to } 2.0) f_0$. Outside this region both current transfer gain and efficiency is falling fast.

15.5.3 Explanation of $g > 1$

We recognized the fact that current transfer gain is greater than unity from mathematical analysis, and simulation and experimental results. The reason to enlarge the fundamental current is that the resonant circuit transfers the energy of other higher order harmonics to the fundamental component. Therefore the gain of the fundamental current can be greater than unity.

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Cascade Reverse Double Γ -LC Resonant Power Converter

A four-element power resonant converter — cascade reverse double Γ -LC resonant power converter (RPC) — will be discussed in this chapter. Since the first element is an inductor, the power supply should be a bipolar voltage source. Do remember that the first element of CSRs in previous chapters is a capacitor, therefore, a bipolar current source was employed. The major work is concentrated on the analysis of steady-state operation, dynamic behavior, and control specialties of the novel resonant converter. The simulation and experimental results show that this resonant converter has many distinct advantages over the existing two or three element resonant converters and overcomes their drawbacks.

16.1 Introduction

Generally, a switched-mode power converter is often required to meet all or most of the following specifications:

- High switching frequency
- High power density for reduction of size and weight
- High conversion efficiency
- Low total harmonic distortion (THD)
- Controlled power factor if the source is an AC voltage
- Low electromagnetic interference (EMI)

A review of the commonly used pulse-width-modulating (PWM) converter and new generated resonant converter is presented in order to fully understand the two major branches of the high frequency switching converter. Although PWM technique is widely used in power electronic applications, it encounters serious problems when the switching converter operates at

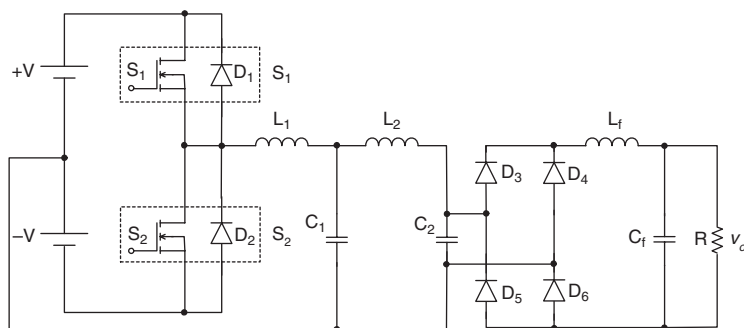


FIGURE 16.1

Circuit diagram of cascade reverse double Γ -LC RPC.

high frequencies. Due to the hard-switching transitions caused by PWM technique, switching losses possess large proportion in total power dissipations. In other words, when the switch is turned on, the current through it rises very fast, while the voltage across it cannot descend immediately due to the parasitic output capacitance. Similarly, when the switch is turned off, the voltage across it rises rapidly while the current through it cannot drop at once because of the recombination of carriers.

In general, a resonant power converter is defined as a converter in which one or more switching waveforms are resonant waveforms. It is reasonable to say that a resonant power converter usually contains a resonant circuit. In fact, there are many topologies of the resonant power converter, which are many more than ZCS and ZVS QRCs in [Chapter 11](#).

16.2 Steady-State Analysis of Cascade Reverse Double Γ -LC RPC

In this chapter, a cascade reverse double Γ -LC RPC is introduced. Under some assumptions and simplifications, the steady-state AC analysis is undertaken to study the two most interesting topics: voltage transfer gain and the input impedance.

16.2.1 Topology and Circuit Description

The circuit diagram of a half-bridge cascade reverse double Γ -LC resonant power converter is shown in [Figure 16.1](#). Like other resonant converters, this topology consists of a bipolar voltage source, resonant network — the cascade reverse double Γ -LC, the rectifier-plus-filter, and load (such as a resistive load R). The power MOSFETs S_1 and S_2 and their antiparalleled diodes

D_1 and D_2 act together as a bipolar voltage source. To operate this circuit, S_1 is turned on and off 180° out of phase with respect to the turn-off and -on of S_2 at same frequency $\omega = 2\pi f$. After the switching circuit, the input voltage can be considered as a bipolar square-wave voltage alternating in value between $+V$ and $-V$, which is then input to the resonant circuit section. L_1 , L_2 and C_1 , C_2 represent the resonant inductors and capacitors, respectively. The output DC voltage is obtained by rectifying the voltage across the second resonant capacitor C_2 . L_f and C_f comprise a low-pass filter to smooth out the output voltage and current, and R denotes either an actual or an equivalent load resistance.

The following assumptions should be made:

1. All the switches and diodes used in the converter are ideal components
2. All the inductors and capacitors are passive, linear and time-invariant
3. The output inductor is large enough to assume that the load current does not vary significantly during switching period
4. The converter operates above resonance

16.2.2 Classical Analysis on AC Side

This analysis is available on the AC side before the rectifier bridge.

16.2.2.1 Basic Operating Principles

For the cascade reverse double Γ -LC RPC considered here, the half-bridge converter applies a square wave of voltage to a resonant network. Since the resonant network has the effect of filtering the higher-order harmonic voltages, a sine wave of current will appear at the input to the resonant circuit (this is true over most of the load range of interest). This fact allows classical AC analysis techniques to be used. The analysis proceeds as follows. The fundamental component of the square wave input voltage is applied to the resonant network, and the resulting sine waves of current and voltage in the resonant circuit are computed using classical AC analysis. For a rectifier with an inductor output filter, the sine wave voltage at the input to the rectifier is rectified, and the average value is taken to arrive at the resulting DC output voltage. For a capacitive output filter, a square wave of voltage appears at the input to the rectifier while a sine wave of current is injected into the rectifier. For this case the fundamental component of the square wave voltage is used in the AC analysis.

16.2.2.2 Equivalent Load Resistance

It is necessary that the rectifier with its filter should be expressed as an equivalent load resistance before the analysis is carried out, which illustrates

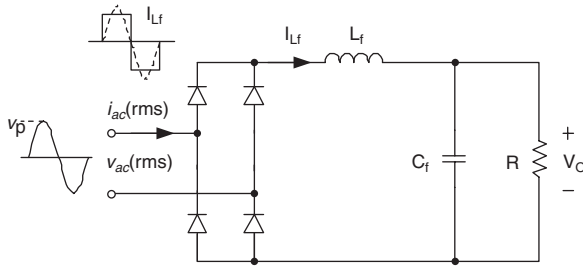


FIGURE 16.2

Equivalent load resistance R_{eq} .

the derivation of the equivalent resistance to use in loading the resonant circuit. The resonant converter uses an inductor output filter and drives the rectifier with an equivalent voltage source, i.e., a low-impedance source provided by the resonant capacitor. A square wave of current is drawn by the rectifier, and its fundamental component must be used in arriving at an equivalent AC resistance. For this case, the root-mean-square value of the voltage and current before the rectifier are given as:

$$v_{ac}(rms) = \frac{\pi}{2\sqrt{2}} V_o$$

$$i_{ac}(rms) = \frac{2\sqrt{2}}{\pi} I_{Lf}$$

$$R_{eq} = \frac{v_{ac}(rms)}{i_{ac}(rms)} = \frac{\pi^2}{8} \frac{V_o}{I_{Lf}} = \frac{\pi^2}{8} R$$

The equivalent resistance R_{eq} is shown in [Figure 16.2](#).

16.2.2.3 Equivalent AC Circuit and Transfer Functions

The equivalent AC circuit diagram of the cascade reverse double Γ -LC RPC is shown in [Figure 16.3](#). Note that all the parameters and variables are transferred to the s -domain. Using Laplace operator $s = j\omega_s$, it is a simple matter to write down the voltage transfer gain of the cascade reverse double Γ -LC RPC:

$$g(s) = \frac{V_o(s)}{V_i(s)} = R_{eq} \left/ \begin{aligned} &[s^4 L_1 L_2 R_{eq} C_1 C_2 + s^3 L_1 L_2 C_1 \\ &+ s^2 (L_1 R_{eq} C_1 + L_1 R_{eq} C_2 + L_2 R_{eq} C_2) + s(L_1 + L_2) + R_{eq}] \end{aligned} \right.$$

or

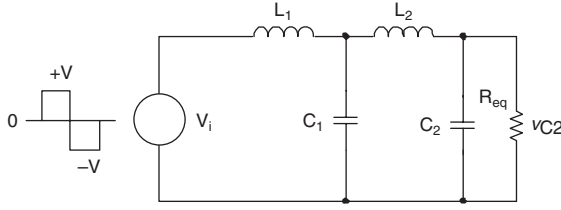


FIGURE 16.3

Equivalent circuit of the cascade reverse double Γ -LC RPC.

$$g(s) = R_{eq} / B(s) \quad (16.1)$$

where

$$B(s) = s^4 L_1 L_2 R_{eq} C_1 C_2 + s^3 L_1 L_2 C_1 + s^2 (L_1 R_{eq} C_1 + L_1 R_{eq} C_2 + L_2 R_{eq} C_2) + s(L_1 + L_2) + R_{eq} \quad (16.2)$$

The voltage and current stresses on different reactive resonant components are obtained with respect to the input fundamental voltage V_i .

Voltage and current on inductor L_1 :

$$\frac{V_{L1}(s)}{V_i(s)} = \frac{sL_1[s^3 L_2 R_{eq} C_1 C_2 + s^2 L_2 C_1 + sR_{eq}(C_1 + C_2) + 1]}{B(s)} \quad (16.3)$$

$$\frac{I_{L1}(s)}{V_i(s)} = \frac{s^3 L_2 R_{eq} C_1 C_2 + s^2 L_2 C_1 + sR_{eq}(C_1 + C_2) + 1}{B(s)} \quad (16.4)$$

Voltage and current on capacitor C_1 :

$$\frac{V_{C1}(s)}{V_i(s)} = \frac{s^2 L_2 R_{eq} C_2 + sL_2 + R_{eq}}{B(s)} \quad (16.5)$$

$$\frac{I_{C1}(s)}{V_i(s)} = \frac{sC_1(s^2 L_2 R_{eq} C_2 + sL_2 + R_{eq})}{B(s)} \quad (16.6)$$

Voltage and current on inductor L_2 :

$$\frac{V_{L2}(s)}{V_i(s)} = \frac{sL_2(sR_{eq} C_2 + 1)}{B(s)} \quad (16.7)$$

$$\frac{I_{L2}(s)}{V_i(s)} = \frac{sR_{eq}C_2 + 1}{B(s)} \quad (16.8)$$

Voltage and current on capacitor C_2 :

$$\frac{V_{C2}(s)}{V_i(s)} = \frac{R_{eq}}{sC_2 \cdot B(s)} \quad (16.9)$$

$$\frac{I_{C2}(s)}{V_i(s)} = \frac{R_{eq}}{B(s)C_2} \quad (16.10)$$

The input impedance is given by

$$Z_{in} = \frac{B(s)}{s^3L_2R_{eq}C_1C_2 + s^2L_2C_1 + sR_{eq}(C_1 + C_2) + 1} \quad (16.11)$$

16.2.2.4 Analysis of Voltage Transfer Gain and the Input Impedance

In general, the voltage gain and the input impedance have more attractions to the designer rather than other transfer functions listed above. To simplify the mathematical analysis, the resonant components are chosen as follows:

$$L_1 = L_2 = L \quad C_1 = C_2 = C \quad \omega_0 = \sqrt{\frac{1}{LC}}$$

The quality factor Q is defined as

$$Q = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 C R_{eq}} = \frac{Z_0}{R_{eq}} \quad (16.12)$$

where the characteristic impedance Z_0 is

$$Z_0 = \sqrt{\frac{L}{C}} \quad (16.13)$$

The relative switching frequency is defined as

$$\beta = \frac{\omega}{\omega_0} \quad (16.14)$$

where ω is the switching frequency and ω_0 is the natural resonance frequency:

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (16.15)$$

Under the above-simplified conditions, the voltage gain $g(s)$ given in previous section can be rewritten as

$$B(\beta) = R_{eq} [1 - 3\beta^2 + \beta^4 + j(2 - \beta^2)\beta Q]$$

$$g(\beta) = \frac{1}{(1 - 3\beta^2 + \beta^4) + j(2 - \beta^2)\beta Q} = |g(\beta)| \angle \theta \quad (16.17)$$

The determinant and phase of $g(\beta)$ are given by:

$$|g(\beta)| = \frac{1}{\sqrt{(1 - 3\beta^2 + \beta^4)^2 + (2 - \beta^2)^2 \beta^2 Q^2}}$$

and

$$\theta = -\tan^{-1} \frac{(2 - \beta^2)\beta Q}{1 - 3\beta^2 + \beta^4} \quad (16.18)$$

Analogously, the input impedance $Z_{in}(s)$ can also be simplified as:

$$Z_{in}(\beta) = \frac{R_{eq} [1 - 3\beta^2 + \beta^4 + j(2 - \beta^2)\beta Q]}{1 - \beta^2 + j(2 - \beta^2)\beta / Q} = |Z_{in}(\beta)| \angle \phi \quad (16.19)$$

where

$$|Z_{in}(\beta)| = \frac{R_{eq} \sqrt{(1 - 3\beta^2 + \beta^4)^2 + (2 - \beta^2)^2 \beta^2 Q^2}}{\sqrt{(1 - \beta^2)^2 + (2 - \beta^2)^2 \beta^2 / Q^2}}$$

and

$$\phi = \tan^{-1} \frac{(2 - \beta^2)\beta Q}{1 - 3\beta^2 + \beta^4} - \tan^{-1} \frac{(2 - \beta^2)\beta}{(1 - \beta^2)Q} \quad (16.20)$$

The characteristics of the voltage gain $|g(\beta)|$ and phase angle θ vs. relative frequency β referring to various Q is shown in [Figure 16.4](#) and [Figure 16.5](#), respectively. Note that for lower Q value, the voltage gain $|g(\beta)|$ is higher than unity at some certain switching frequencies. It means the output voltage

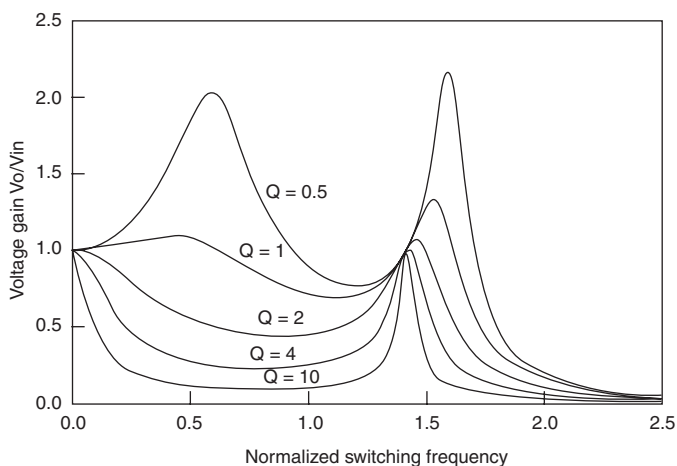


FIGURE 16.4
Voltage gain $|g(\beta)|$ vs. β referring to Q .

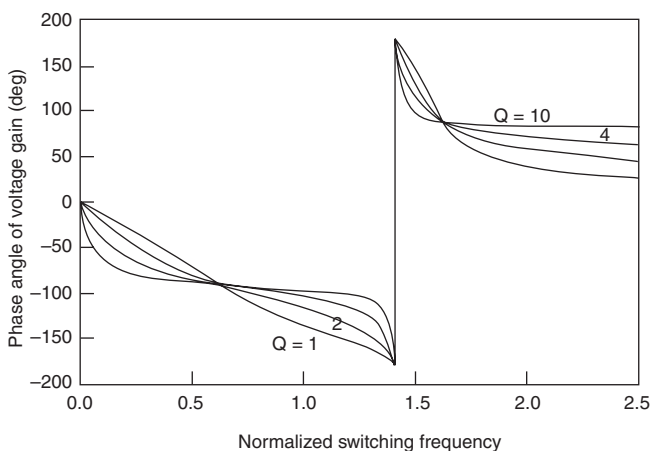


FIGURE 16.5
Phase angle θ vs. β referring to Q .

can be larger than the fundamental harmonic of the input voltage. The result could be explained thusly: the resonant network consisting of inductors and capacitors has the function of filtering the higher order harmonic components in the input quasi-square voltage. The energy of higher order harmonics is then transferred to the fundamental component thus enlarging the output voltage.

This explanation is reasonable when fast Fourier transform (FFT) is applied to the comparison to waveforms of the input voltage and the second capacitor voltage respectively. The resonant circuit in cascade reverse double Γ -LC

RPC allows the signal with higher frequency ($\beta > 1$) passing it and enlarging the energy. In other words, the bandwidth of this novel converter is wider, as it provides more options for the designer to choose the appropriate operating frequency in different applications.

The maximum voltage gain $|g(\beta)|$ can be obtained from

$$\frac{d}{d\beta^2} |g(\beta)| = 0$$

$$\text{or} \quad 4\beta^6 + (3Q^2 - 18)\beta^4 + (22 - 8Q^2)\beta^2 + 4Q^2 - 6 = 0 \quad (16.21)$$

$$\text{when} \quad Q = 1 \quad 4\beta^6 - 15\beta^4 + 14\beta^2 - 2 = 0 \quad (16.22)$$

$$\text{yields} \quad \beta_1 = 0.42 \quad \beta_2 = 1.11 \quad \beta_3 = 1.53$$

It means the local maximum or minimum values on the gain curve are achieved at these roots, respectively. Generally, the voltage gain decreases with the increase of the Q value. For instance, when $Q = 1, 2$, and 4 with $\beta^2 = 2$, the gain $|g(\beta)| = 1, 0.5$, and 0.25 , respectively. At certain switching frequencies, the smaller the value of Q is, the higher the gain.

Specifically, when $Q \ll 1$, Equation (16.21) can be simplified,

$$2\beta^6 - 9\beta^4 + 11\beta^2 - 3 = 0 \quad (16.23)$$

It yields two positive real roots as

$$\beta_1 = 0.618 \quad \beta_2 = 1.618$$

These roots indicate the existence of two peaks in the voltage gain curve, which is the main characteristics of the four-energy-storage-element resonant converters and rarely stated in most conventional two or three elements counterparts.

The voltage gain $|g(\beta)|$ at these two roots is then given by

$$|g(\beta)| = \frac{1}{\sqrt{(1 - 3\beta^2 + \beta^4)^2 + (2 - \beta^2)^2 \beta^2 Q^2}} \bigg|_{\beta_1, \beta_2} = \frac{1}{Q} \quad (16.24)$$

This result is derived under the condition $Q \ll 1$, but applicable for all Q values.

Furthermore, when $Q \gg 1$, Equation (16.21) can be rearranged,

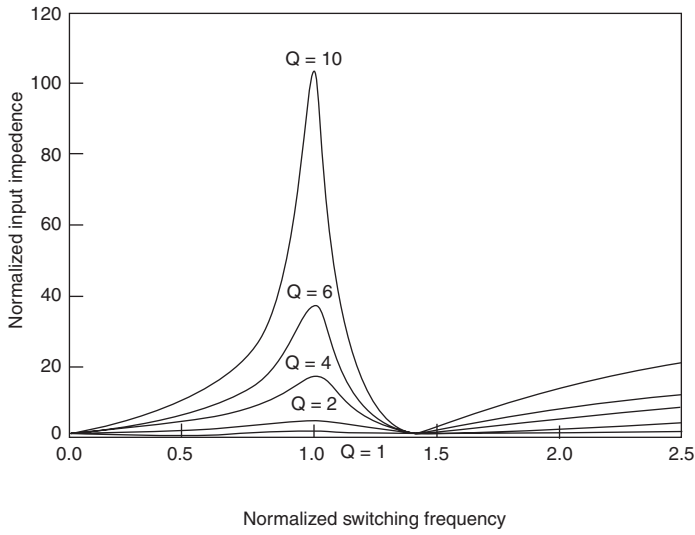


FIGURE 16.6

Input impedance $|Z_{in}(\beta)|$ vs. β referring to Q .

$$3\beta^4 - 8\beta^2 + 4 = 0 \quad (16.25)$$

It gives other two positive real roots as

$$\beta_3 = 0.816 \quad \beta_4 = 1.414$$

The former represents the switching frequency at which the local minimum gain is achieved, while at the latter the maximum voltage gain can be obtained.

From Equation (16.24), it should be noted that when $\beta = 1.414$ ($\beta^2 = 2$), the voltage gain $|g(\beta)|$ constantly keeps unity with any value of Q , as shown in [Figure 16.4](#).

The absolute value of the input impedance $|Z_{in}(\beta)|$ and phase angle ϕ vs. β referring to various Q is shown in [Figure 16.6](#) and [Figure 16.7](#), respectively. The input impedance has its maximum value when the switching frequency is equal to natural resonant frequency (i.e., $\beta = 1$), and its minimum value when the $\beta = 1.414$. The phase angle ϕ keeps zero when $\beta = 1.414$, with any Q value, which means the resonant converter can be regarded as a pure resistive load.

16.2.3 Simulation and Experimental Results

Some simulation and experimental results shown in this section are helpful to understand the design and analysis. The chosen technical data are good examples to implement a particular RPC for reader's reference.

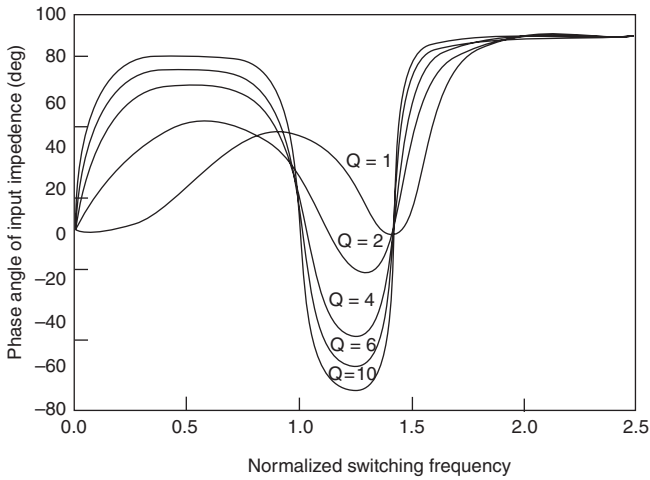


FIGURE 16.7
Phase angle ϕ vs. β referring to Q .

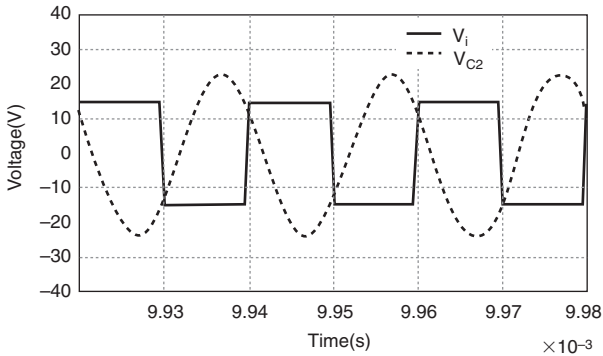


FIGURE 16.8
Simulation results at frequency $f = 50$ KHz.

16.2.3.1 Simulation Studies

In order to verify the mathematical analyses, a four-element cascade reverse double Γ -LC RPC is simulated using PSpice. The parameters used are $V_i = \pm 15$ V, $L_1 = L_2 = 100$ μ H, $C_1 = C_2 = 0.22$ μ F, and $R = 22$ Ω . The natural resonant frequency is $f_0 = 1/(2\pi\sqrt{LC}) = 34$ kHz. The applying frequency is $f = 50$ KHz, corresponding to the $\beta = 1.42$. The simulation results are shown in Figure 16.8. The input signal V_i is a square waveform and the voltage across C_2 is a very smooth sinusoidal waveform.

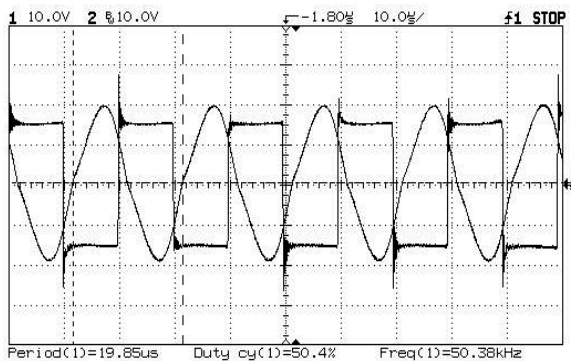


FIGURE 16.9
Experimental waveforms ($f = 50.38$ KHz).

16.2.3.2 Experimental Results

To verify the simulation results of the proposed cascade double Γ -LC RPC, a test rig was constructed with the same conditions: $V_i = \pm 15$ V, $L_1 = L_2 = 100$ μ H, $C_1 = C_2 = 0.22$ μ F and $R = 22$ Ω . The natural resonant frequency is $f_0 = 34$ kHz. For high frequency operation, the main power switch selected is IRF640 with its inner parasitic diode used as the antiparalleled diode. A high-speed integrated chip IR2104 is utilized to drive the half-bridge circuit. The switching frequency is chosen to be 50.38 KHz, corresponding to the $\beta = 1.42$. The experimental results are shown in Figure 16.9. The input signal V_i is a square waveform and the voltage across C_2 is a very smooth sinusoidal waveform.

Select the switching frequency to be 42.19 KHz, corresponding to the $\beta = 1.24$. The experimental results are shown in Figure 16.10. The input signal V_i is a square waveform and the voltage across C_2 is also a smooth sinusoidal waveform.

16.3 Resonance Operation and Modeling

From the circuit diagram in Figure 16.1, the steady-state operation of the circuit is characterized by four operating modes within one switching period, when the resonant converter operates under continuous conduction mode (CCM). The equivalent circuits corresponding to each operating mode are depicted in Figure 16.11. Note that for a large output filter inductor, the bridge rectifier and the load can be represented as an alternating current

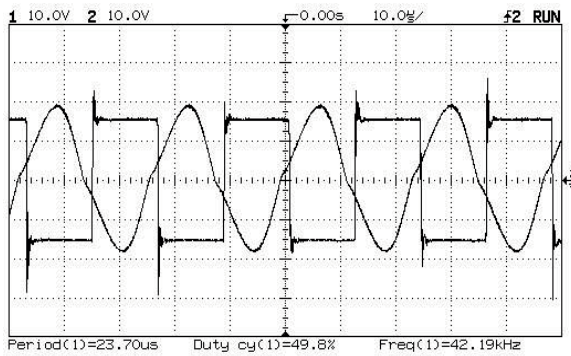


FIGURE 16.10
Experimental waveforms ($f = 42.19$ KHz).

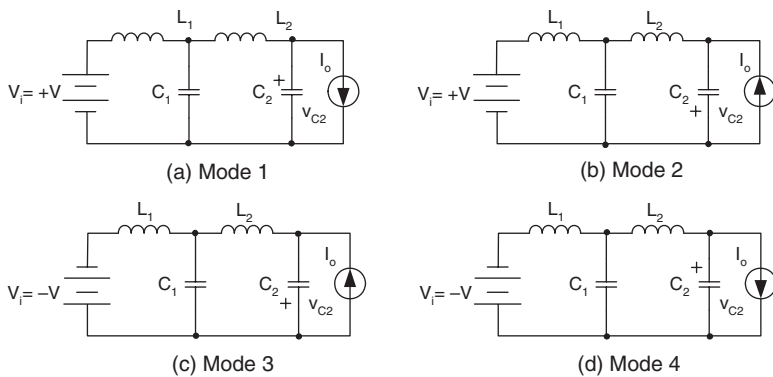


FIGURE 16.11
Different operating resonance modes.

sink with constant amplitude I_o , synchronous with the polarity of the second resonant capacitor voltage v_{C2} .

16.3.1 Operating Principle, Operating Modes and Equivalent Circuits

The operating modes of cascade reverse double Γ -LC RPC are very difficult to distinguish by analytic calculations, even under CCM conditions. However, the state of the converter should not exceed four modes when it operates above resonant frequency. The sequence among different modes is dependent on the phase angle to the voltage gain $V_{C2}(s)/V_i(s)$. In other words, when this angle is between 0° and $+180^\circ$, the voltage across the second

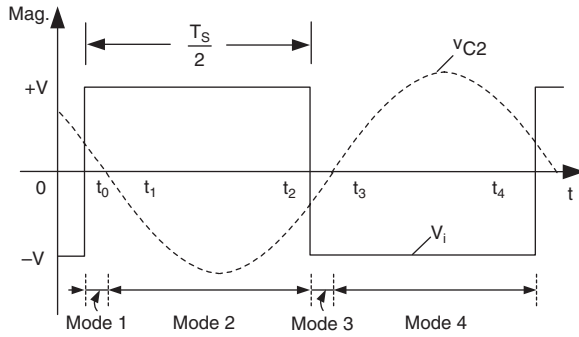


FIGURE 16.12

Voltage waveforms when v_{C2} leads V_i .

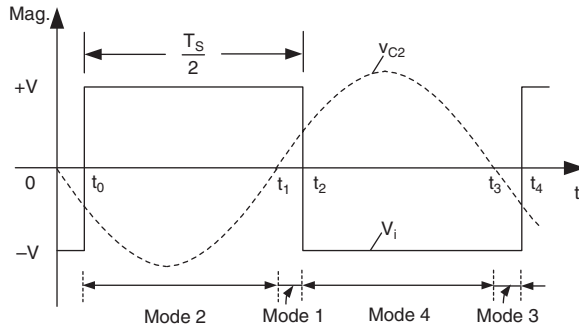


FIGURE 16.13

Voltage waveforms when v_{C2} lags behind V_i .

capacitor v_{C2} leads the input quasi-wave voltage V_i in Figure 16.12, thus the sequence from mode 1 to mode 4 should be:

- Mode 1 ($t_0 < t < t_1$): $V_i > 0$, $v_{C2} > 0$ (Figure 16.11a)
- Mode 2 ($t_1 < t < t_2$): $V_i > 0$, $v_{C2} < 0$ (Figure 16.11b)
- Mode 3 ($t_2 < t < t_3$): $V_i < 0$, $v_{C2} < 0$ (Figure 16.11c)
- Mode 4 ($t_3 < t < t_4$): $V_i < 0$, $v_{C2} > 0$ (Figure 16.11d)

Similarly, when the angle is between -180° and 0° , v_{C2} will lag behind the input voltage V_i in Figure 16.13, causing the sequence to be changed to:

- Mode 2 ($t_0 < t < t_1$): $V_i > 0$, $v_{C2} < 0$ (Figure 16.11b)
- Mode 1 ($t_1 < t < t_2$): $V_i > 0$, $v_{C2} > 0$ (Figure 16.11a)
- Mode 4 ($t_2 < t < t_3$): $V_i < 0$, $v_{C2} > 0$ (Figure 16.11d)
- Mode 3 ($t_3 < t < t_4$): $V_i < 0$, $v_{C2} < 0$ (Figure 16.11c)

In practice, when simulation is in progress, it is up to the algorithm that determines the shifting instant between different operating modes, by means of judging the switching period and the polarity of the second capacitor voltage.

16.3.2 State-Space Analysis

On the basis of the fact that the steady-state operation of resonant converter is periodic and composed of multiple operating modes, each mode stands for one state dependent on the different input voltage and rectifier current, thus, the state equation for each mode is given by:

$$\dot{x}_i = A_i x_i + B_i \quad (16.26)$$

where x_i is the state vector of the converter, A_i is the state coefficient matrix, B_i is the input vector of the converter in the i^{th} operating mode, respectively. For i^{th} mode, Equation (16.26) can be solved analytically:

$$x_i(t) = e^{A_i t} x_i(t_0) + \int_0^t e^{A_i(t-\tau)} B_i d\tau = \Phi_i x_i(t_0) + \Gamma_i \quad (16.27)$$

where $\Phi_i = \Phi(t, t_0) = e^{A_i t}$ is the state transition matrix, $\Gamma_i = \int_0^t e^{A_i(t-\tau)} B_i d\tau$ and

$x_i(t_0)$ are the initial conditions for the i^{th} mode. For the continuous operation, each state solved in i^{th} mode will be employed as the initial conditions for the next $(I + 1)^{th}$ mode.

In fact, the solving process of Equation (16.27) is very tedious and time consuming by the requirement for evaluating the integral. However, by combining A_i and B_i to form an augmented dynamic matrix, the integration overhead can be eliminated at the expense of obtaining only the cyclic steady-state description:

$$\frac{d}{dt} \begin{pmatrix} x_i(t) \\ 1 \end{pmatrix} = \begin{pmatrix} A_i & B_i \\ 0 & 0 \end{pmatrix} \begin{pmatrix} x_i(t) \\ 1 \end{pmatrix} \quad (16.28)$$

or

$$\frac{d}{dt} \hat{x}_i(t) = \hat{A}_i \hat{x}_i(t) \quad (16.29)$$

By means of the concept of state transition matrix, the solution for the state vector in different operating modes can be expressed as:

$$\hat{x}(t_1) = \hat{\Phi}_1 \hat{x}_1(t_0)$$

$$\hat{x}(t_2) = \hat{\Phi}_2 \hat{\Phi}_1 \hat{x}_1(t_0)$$

.....

For i^{th} mode:

$$\hat{x}(t_i) = \hat{\Phi}_i \hat{\Phi}_{i-1} \dots \hat{\Phi}_1 \hat{x}(t_0) = \hat{\Phi}_{tot} \hat{x}(t_0) \quad (16.30)$$

where $\hat{\Phi}_i = \begin{pmatrix} \Phi_i & \Gamma_i \\ 0 & 1 \end{pmatrix}$ and $\hat{x}(t_i)$ is the state vector at time t_i .

Due to periodic nature of the system, the state vector at initial time t_0 should be equal to the one at final time t_i in one cycle, that is,

$$x(t_i) = \Phi_{tot} x(t_0) + \Gamma_{tot} = x(t_0) \quad (16.31)$$

yields:

$$x_{init}(t_0) = (I^n - \Phi_{tot})^{-1} \Gamma_{tot} \quad (16.32)$$

Thus, the state variables at any subsequent time are solved from Equation (16.30).

To obtain the average steady-state output voltage, the average values of the state-variables over a complete cycle are found from:

$$x_{av} = \frac{1}{T} \int_{t_0}^{t_0+T} x(t) dt \quad (16.33)$$

Again, the expression includes the integral process, which can be simplified by augmenting the state vector with

$$\dot{x}_{av}(t) = \frac{1}{T} x(t) \quad (16.34)$$

Then, consider the total dynamics of the converter during the i^{th} mode, the simultaneous equations are given by:

$$\dot{x}_i = A_i x_i + B_i \quad (16.35)$$

$$\dot{x}_{i_av} = \frac{d_i}{T} x_i \quad (16.36)$$

where d_i is the duty cycle for i^{th} mode in one cycle.

Substituting Equation (16.36) into Equation (16.28), the resulting dynamic equation is

$$\frac{d}{dt} \begin{pmatrix} x_i(t) \\ 1 \\ x_{i_av}(t) \end{pmatrix} = \begin{pmatrix} A_i & B_i & 0 \\ 0 & 0 & 0 \\ \frac{d_i}{T} I^n & 0 & 0 \end{pmatrix} \begin{pmatrix} x_i(t) \\ 1 \\ x_{i_av}(t) \end{pmatrix} \quad (16.37)$$

or

$$\dot{z}_i(t) = \tilde{A}_i z_i(t) \quad (16.38)$$

Again, as discussed in previous section, the state equation can be expressed as the function of state transition matrices in different modes:

$$z(t_i) = \tilde{\Phi}_i \tilde{\Phi}_{i-1} \cdots \tilde{\Phi}_1 z(t_0) \quad (16.39)$$

with the initial conditions:

$$z(t_0) = \begin{pmatrix} x_{init}(t_0) \\ 1 \\ 0 \end{pmatrix} \quad (16.40)$$

From the state variables, i.e., the voltage across the capacitors and current through the inductors, their average values can be gained directly.

The state coefficient matrix and the input source vector are determined in terms of different operating modes of the resonant converter. Considering the operating conditions described in [Figure 16.12](#), for mode 1, suppose $V_i > 0$ and $v_{c2} > 0$, it can be obtained

$$A_1 = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 & 0 & 0 \\ 1/C_1 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 & -1/C_2 & 0 \\ 0 & 0 & 0 & 1/L_f & 0 & -1/L_f \\ 0 & 0 & 0 & 0 & 1/C_f & -1/RC_f \end{bmatrix}$$

and

$$B_1 = [V/L_1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]^T$$

where

$$x = (i_{L1}, i_{L2}, v_{C1}, v_{C2}, i_{Lf}, v_{Cf})^T$$

For mode 2, $V_i > 0$, $v_{C2} < 0$, the structure of the topology is changed due to the alteration of the polarity of the second capacitor voltage, giving:

$$A_2 = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 & 0 & 0 \\ 1/C_1 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 & 1/C_2 & 0 \\ 0 & 0 & 0 & -1/L_f & 0 & -1/L_f \\ 0 & 0 & 0 & 0 & 1/C_f & -1/(RC_f) \end{bmatrix}$$

and

$$B_2 = B_1$$

For mode 3, $V_i < 0$, $v_{C2} < 0$, because only the input source is changed, the topology of the system remains invariant, thus the state coefficient matrix A_3 is identical with A_2 , that is,

$$A_3 = A_2 \quad \text{and} \quad B_3 = [-V/L_1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]^T$$

Similarly, when operating the above resonance, for mode 4, $V_i < 0$, $v_{C2} > 0$, yielding:

$$A_4 = A_1 \quad \text{and} \quad B_4 = B_3$$

By employing the above coefficient matrices and vectors with the initial conditions, the values of all state variables in different operating modes can be obtained following Equation (16.39). Thus, the dynamic operating behavior of the resonant converter can be described by these state variables as well.

16.4 Small-Signal Modeling of Cascade Reverse Double Γ -LC RPC

In the previous section, state-space averaging technique has been applied to investigate the dynamic behavior and successfully simulated the waveforms

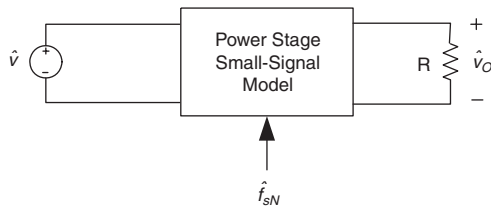


FIGURE 16.14

Small-signal perturbations in input voltage and switching frequency.

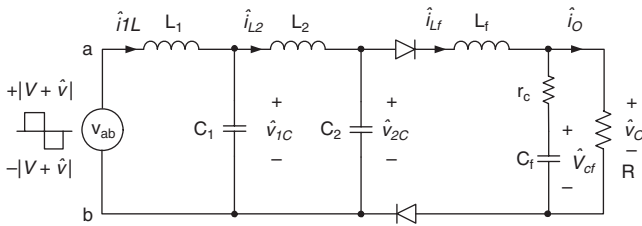


FIGURE 16.15

Equivalent circuit of cascade reverse double Γ -LC RPC.

at different time intervals, however, the numerical results cannot reveal the relations of various control specialties, e.g., frequency response, closed-loop control system stability, etc. In order to study these characteristics more deeply, a number of mathematical methods were presented among them the small-signal modeling is implemented.

16.4.1 Small-Signal Modeling Analysis

16.4.1.1 Model Diagram

The block diagram of the small-signal model is depicted in [Figure 16.14](#), where \hat{v} and \hat{f}_{sN} represent small-signal perturbation of the line voltage and the frequency control signal. The output variable is the perturbed output voltage, \hat{v}_O . With the model, it is easy to obtain the commonly used small-signal transfer functions, such as control-to-output transfer function, line-to-output transfer function, input impedance, and output impedance.

16.4.1.2 Nonlinear State Equation

The equivalent circuit of the resonant converter is shown in [Figure 16.15](#). As seen, the half-bridge circuit employing two diodes, applies a square-wave voltage, v_{abr} , to the resonant network. Suppose the converter operates above resonance, the state equations of the resonant converter can be obtained, where the nonlinear terms are in bold face:

$$\begin{aligned}
L_1 \frac{di_{L1}}{dt} + v_{C1} &= v_{ab} \\
C_1 \frac{dv_{C1}}{dt} + i_{L2} &= i_{L1} \\
L_2 \frac{di_{L2}}{dt} + v_{C2} &= v_{C1} \\
C_2 \frac{dv_{C2}}{dt} + \text{sgn}(v_{C2})i_{Lf} &= i_{L2} \\
L_f \frac{di_{Lf}}{dt} + (i_{Lf} - i_o)r_c + v_{Cf} &= |v_{C2}| \\
C_f \frac{dv_{Cf}}{dt} &= i_{Lf} - i_o
\end{aligned} \tag{16.41}$$

The output variable is the output voltage, v_o , which gives:

$$v_o = (i_{Lf} - i_o)r_c + v_{Cf} \tag{16.42}$$

In this circuit, the output voltage is regulated either by the input line voltage, v , or by the applying switching frequency, ω . Thus, the operating point \mathcal{P} can be expressed as the function of these variables $\mathcal{P} = \{v, R, \omega\}$.

16.4.1.3 Harmonic Approximation

Under the assumption that both the voltage and current inside the resonant network are quasi-sinusoidal, the so-called fundamental approximation method is applied to the derivation of the small-signal models. In other words, the variables in the resonant network are assumed as:

$$\begin{aligned}
i_{L1} &= i_{1s}(t) \sin \omega t + i_{1c}(t) \cos \omega t \\
i_{L2} &= i_{2s}(t) \sin \omega t + i_{2c}(t) \cos \omega t \\
v_{C1} &= v_{1s}(t) \sin \omega t + v_{1c}(t) \cos \omega t \\
v_{C2} &= v_{2s}(t) \sin \omega t + v_{2c}(t) \cos \omega t
\end{aligned} \tag{16.43}$$

Note that the envelope terms $\{i_{1s}, i_{1c}, i_{2s}, i_{2c}, v_{1s}, v_{1c}, v_{2s}, v_{2c}\}$ are slowly time varying, thus the dynamic behavior of these terms can be investigated. The derivatives of i_{L1}, i_{L2}, v_{C1} and v_{C2} are found to be:

$$\begin{aligned}
\frac{di_{L1}}{dt} &= \left[\frac{di_{1s}}{dt} - \omega i_{1c} \right] \sin \omega t + \left[\frac{di_{1c}}{dt} + \omega i_{1s} \right] \cos \omega t \\
\frac{di_{L2}}{dt} &= \left[\frac{di_{2s}}{dt} - \omega i_{2c} \right] \sin \omega t + \left[\frac{di_{2c}}{dt} + \omega i_{2s} \right] \cos \omega t \\
\frac{dv_{C1}}{dt} &= \left[\frac{dv_{1s}}{dt} - \omega v_{1c} \right] \sin \omega t + \left[\frac{dv_{1c}}{dt} + \omega v_{1s} \right] \cos \omega t \\
\frac{dv_{C2}}{dt} &= \left[\frac{dv_{2s}}{dt} - \omega v_{2c} \right] \sin \omega t + \left[\frac{dv_{2c}}{dt} + \omega v_{2s} \right] \cos \omega t
\end{aligned} \tag{16.44}$$

16.4.1.4 Extended Describing Function

By employing the extended describing function modeling technique stated in the literature, the nonlinear terms in Equation (16.41) can be approximated either by the fundamental harmonic terms or by the DC terms, to yield:

$$\begin{aligned}
v_{ab}(t) &\approx f_1(v) \sin \omega_s t \\
\text{sgn}(v_2) i_{Lf} &\approx f_2(v_{2s}, v_{2c}, i_{Lf}) \sin \omega_s t + f_3(v_{2s}, v_{2c}, i_{Lf}) \cos \omega_s t \\
|v_{C2}| &\approx f_4(v_{2s}, v_{2c})
\end{aligned} \tag{16.45}$$

These functions are called extended describing functions (EDFs). They are dependent on the operating conditions and the harmonic coefficients of the state variables. The EDF terms can be calculated by making Fourier expansions of the nonlinear terms, to give:

$$\begin{aligned}
f_1(v) &= \frac{4}{\pi} v \\
f_2(v_{2s}, v_{2c}, i_{Lf}) &= \frac{4}{\pi} \frac{v_{2s}}{A_p} i_{Lf} \\
f_3(v_{2s}, v_{2c}, i_{Lf}) &= \frac{4}{\pi} \frac{v_{2c}}{A_p} i_{Lf} \\
f_4(v_{2s}, v_{2c}) &= \frac{2}{\pi} A_p
\end{aligned} \tag{16.46}$$

where

$$A_p = \sqrt{v_{2s}^2 + v_{2c}^2}$$

is the peak voltage of the second capacitor voltage v_{c2} .

16.4.1.5 Harmonic Balance

Substituting Equation (16.43) to Equation (16.46) into Equation (16.41), the nonlinear large-signal model of cascade reverse double Γ -LC RPC is obtained as follows:

$$\begin{aligned}
 L_1 \left(\frac{di_{1s}}{dt} - \omega_s i_{1c} \right) + v_{1s} &= \frac{4}{\pi} v \\
 L_1 \left(\frac{di_{1c}}{dt} + \omega_s i_{1s} \right) + v_{1c} &= 0 \\
 C_1 \left(\frac{dv_{1s}}{dt} - \omega_s v_{1c} \right) &= i_{1s} - i_{2s} \\
 C_1 \left(\frac{dv_{1c}}{dt} + \omega_s v_{1s} \right) &= i_{1c} - i_{2c} \\
 L_2 \left(\frac{di_{2s}}{dt} - \omega_s i_{2c} \right) &= v_{1s} - v_{2s} \\
 L_2 \left(\frac{di_{2c}}{dt} + \omega_s i_{2s} \right) &= v_{1c} - v_{2c} \\
 C_2 \left(\frac{dv_{2s}}{dt} - \omega_s v_{2c} \right) + \frac{4}{\pi} \frac{v_{2s}}{A_p} i_{lf} &= i_{2s} \\
 C_2 \left(\frac{dv_{2c}}{dt} + \omega_s v_{2s} \right) + \frac{4}{\pi} \frac{v_{2c}}{A_p} i_{lf} &= i_{2c} \\
 L_f \frac{di_{lf}}{dt} + (i_{lf} - i_o) r_c &= \frac{2}{\pi} A_p - v_{cf} \\
 C_f \frac{dv_{cf}}{dt} &= i_{lf} - i_o
 \end{aligned} \tag{16.47}$$

The corresponding output equation is

$$v_o = (i_{lf} - i_o) r_c + v_{cf} \tag{16.48}$$

It should be noted that the small-signal modulation frequency is lower than the switching frequency, thus the nonlinear model can be linearized by perturbing the system around the operating point \mathcal{P} . The perturbed variables are the inputs, the state variables, and the outputs. Each one has the form of

$$x(t) = X + \hat{x}(t)$$

where X is the steady state at the operating point, and $\hat{x}(t)$ is a small amplitude perturbation.

Similarly, in this circuit, the input variables are found to be

$$v = V + \hat{v} \quad \omega_s = \Omega_s + \hat{\omega}_s$$

16.4.1.6 Perturbation and Linearization

Under the small amplitude perturbation assumptions, the complete linearized small-signal models can be established by applying the perturbation to Equation (16.47) and only considering the first partial derivatives, to give:

$$\begin{aligned}
 L_1 \frac{d\hat{i}_{1s}}{dt} &= Z_{L1} \hat{i}_{1c} + E_{1s} \hat{f}_{sN} - \hat{v}_{1s} + k_v \hat{v} \\
 L_1 \frac{d\hat{i}_{1c}}{dt} &= -Z_{L1} \hat{i}_{1s} - E_{1c} \hat{f}_{sN} - \hat{v}_{1c} \\
 C_1 \frac{d\hat{v}_{1s}}{dt} &= \hat{i}_{1s} - \hat{i}_{2s} + G_s \hat{v}_{1c} + J_{1s} \hat{f}_{sN} \\
 C_1 \frac{d\hat{v}_{1c}}{dt} &= \hat{i}_{1c} - \hat{i}_{2c} - G_s \hat{v}_{1s} - J_{1c} \hat{f}_{sN} \\
 L_2 \frac{d\hat{i}_{2s}}{dt} &= \hat{v}_{1s} - \hat{v}_{2s} + Z_{L2} \hat{i}_{2c} + E_{2s} \hat{f}_{sN} \\
 L_2 \frac{d\hat{i}_{2c}}{dt} &= \hat{v}_{1c} - \hat{v}_{2c} - Z_{L2} \hat{i}_{2s} - E_{2c} \hat{f}_{sN} \\
 C_2 \frac{d\hat{v}_{2s}}{dt} &= \hat{i}_{2s} - g_{ss} \hat{v}_{2s} + g_{sc} \hat{v}_{2c} - 2k_s \hat{i}_{Lf} + J_{2s} \hat{f}_{sN} \\
 C_2 \frac{d\hat{v}_{2c}}{dt} &= \hat{i}_{2c} - g_{cc} \hat{v}_{2c} + g_{cs} \hat{v}_{2s} - 2k_c \hat{i}_{Lf} + J_{2c} \hat{f}_{sN} \\
 L_f \frac{d\hat{i}_{Lf}}{dt} &= (\hat{i}_o - \hat{i}_{Lf}) r_c - \hat{v}_{Cf} + k_s \hat{v}_{2s} + k_c \hat{v}_{2c} \\
 C_f \frac{d\hat{v}_{Cf}}{dt} &= \hat{i}_{Lf} - \hat{i}_o
 \end{aligned} \tag{16.49}$$

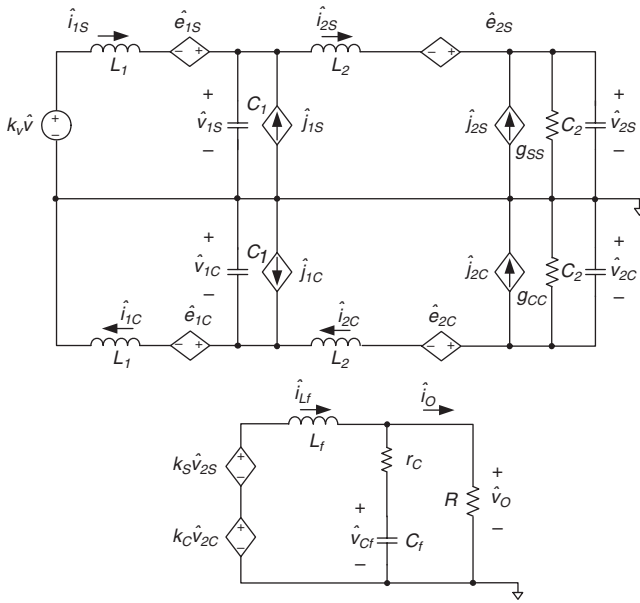


FIGURE 16.16

Equivalent small-signal circuit of cascade reverse double Γ -LC RPC.

where the input variables are \hat{v} and \hat{f}_{sN} , standing for the perturbed line voltage and normalized switching frequency, respectively.

The output part of the small-signal model is given by:

$$\hat{v}_o = (\hat{i}_{Lf} - \hat{i}_o)r_c + \hat{v}_{Cf} \quad (16.50)$$

All the parameters used in the above models are given in the Appendix.

16.4.1.7 Equivalent Circuit Model

This linearized small-signal model makes it possible to describe the operating characteristics of the resonant converter using equivalent circuit model, as shown in Figure 16.16. In this model, the circuit is divided into two parts: the resonant network and the output part. To simplify the drawing, some dependent sources are defined as:

$$\hat{e}_{1s} = Z_{L1}\hat{i}_{1c} + E_{1s}\hat{f}_{sN}$$

$$\hat{e}_{1c} = Z_{L1}\hat{i}_{1s} + E_{1c}\hat{f}_{sN}$$

$$\hat{e}_{2s} = Z_{L2}\hat{i}_{2c} + E_{2s}\hat{f}_{sN}$$

$$\hat{e}_{2c} = Z_{L2}\hat{i}_{2s} + E_{2c}\hat{f}_{sN}$$

$$\hat{j}_{1s} = G_s\hat{v}_{1c} + J_{1s}\hat{f}_{sN}$$

$$\hat{j}_{1c} = G_s\hat{v}_{1s} + J_{1c}\hat{f}_{sN}$$

$$\hat{j}_{2s} = g_{sc}\hat{v}_{2c} - 2k_s\hat{i}_{Lf} + J_{2s}\hat{f}_{sN}$$

$$\hat{j}_{2c} = g_{cs}\hat{v}_{2s} - 2k_c\hat{i}_{Lf} + J_{2c}\hat{f}_{sN}$$

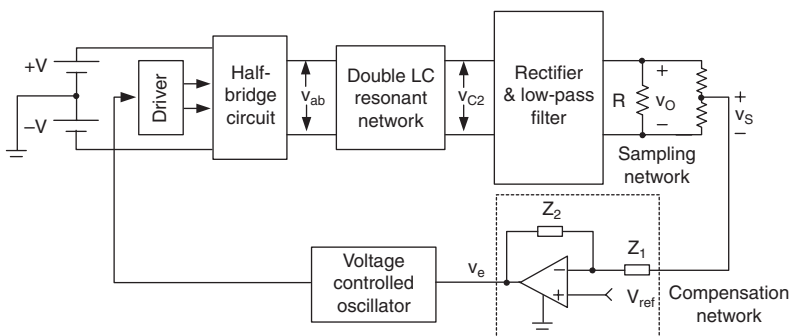


FIGURE 16.17

Closed-loop system of cascade reverse double Γ -LC RPC.

By employing the Kirchoff's current law and voltage law, the equivalent circuit can be drawn following the state-equation Equation (16.49). Note that in the output part, the voltage across the second capacitor $|\hat{v}_{C2}|$ is replaced by two voltage-controlled sources $\{k_s \hat{v}_{2s}, k_c \hat{v}_{2c}\}$. This circuit model can be implemented in general-purpose simulation software, such as PSpice or MATLAB, to obtain the frequency response of the system.

16.4.2 Closed-Loop System Design

The closed-loop control system diagram of the half-bridge cascade reverse double Γ -LC RPC is illustrated in Figure 16.17, where the feedback loop is composed of the sampling network, the compensator, and the voltage-controlled oscillator (VCO). The sampling network, R_1 and R_2 , contributes attenuation according to its sampling ratio of $R_1/(R_1 + R_2)$. Since the two resistors are chosen to be equal, the gain attenuation of the network is $20 \log (v_s/v_o) = -6\text{dB}$. The sampled voltage, v_s , is then sent to the inverting input side of the error amplifier, where it is compared with a fixed reference voltage v_{ref} and generates an error voltage, v_e . This voltage determines the frequency output of a voltage-controlled oscillator (VCO), whose gain can be obtained either in datasheet or by experiment. The Bode plot, considering all the voltage gains of the main circuit, the sampling network and VCO, is shown in Figure 16.18.

It should be noted that the slope of the magnitude response at the unity-gain crossover frequency is -40dB/decade . Both the gain margin and the phase margin of the small-signal model are not able to meet the requirements of the stability. Thus, the alleged feedback compensation is often used to shape the frequency response such that it remains stable under all operating conditions, especially in the presence of noise or disturbance injected at any point in the loop. In order to yield a -20dB/decade slope at the unity-gain crossover frequency, the magnitude response of the compensation network must have a slope of $+20\text{dB/decade}$ slope at the unity-gain crossover frequency. Hence, a three poles and double zeros compensation network is

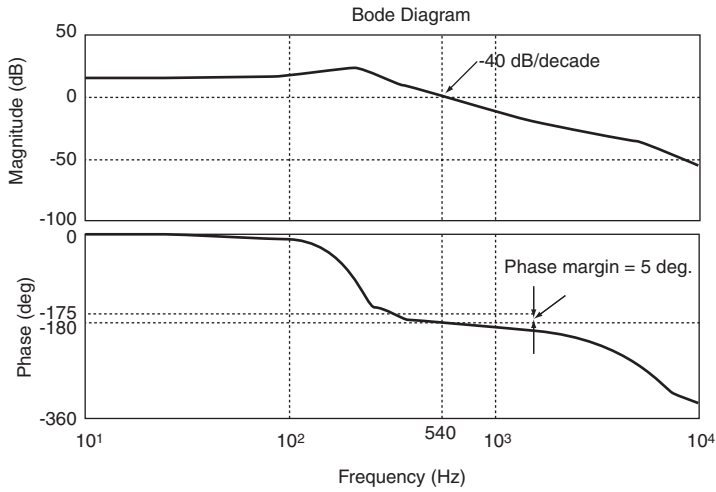


FIGURE 16.18
Bode diagram of the small-signal equivalent circuit.

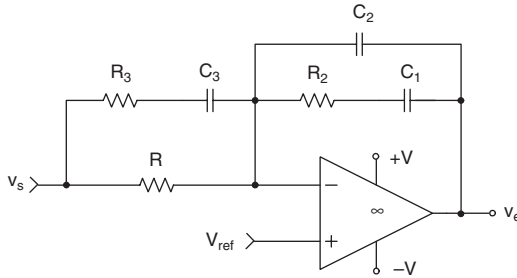


FIGURE 16.19
Compensation network.

employed, whose circuit implementation and Bode diagram are shown in Figure 16.19 and Figure 16.20 respectively.

The transfer function for this compensation network is

$$H(j\omega) = \frac{1 + j\omega R_2 C_1}{-\omega^2 R_2 C_1 C_2 + j\omega(C_1 + C_2)} \frac{1 + j\omega(R_1 + R_3)C_3}{R_1 + j\omega R_1 R_3 C_3} \quad (16.51)$$

As seen from Equation (16.51), it has two high-frequency poles, one at $f_{p1} = 1/2R_3C_3$ and the other at $f_{p2} = (C_1 + C_2)/2R_2C_1C_2$. The zeros are at $f_{z1} = 1/2R_2C_1$ and $f_{z2} = 1/2(R_1 + R_3)C_3$, respectively. The two gains of the compensation network are $K_1 = R_2/R_1$ and $K_2 = R_2(R_1 + R_3)/R_1R_3C_3$, respectively. To simplify the design process, the two high frequency poles are usually chosen to be equal to each other (i.e., $f_{p1} = f_{p2} = f_p$) such that

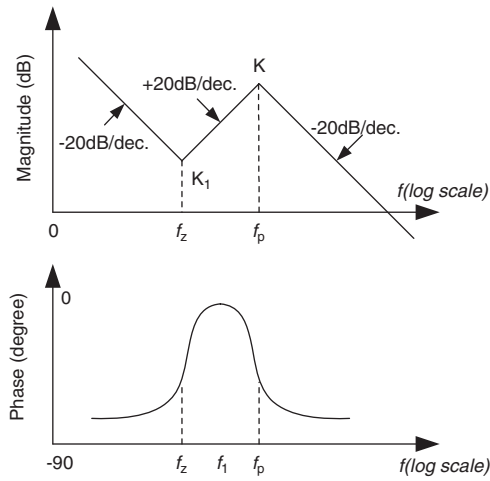


FIGURE 16.20

Bode schematic diagram of the compensation network.

$$\frac{1}{2\pi R_3 C_3} = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2} \quad (16.52)$$

The phase lag due to the double poles, θ_p , is

$$\theta_p = 2 \tan^{-1}\left(\frac{f_p}{f_1}\right) \quad (16.53)$$

where f_1 is the unity-gain crossover frequency.

Similarly, the two zeros are also chosen to be equal, such that

$$\frac{1}{2\pi R_2 C_1} = \frac{1}{2\pi (R_1 + R_3) C_3} \quad (16.54)$$

The phase boost at the double zeros, θ_z , is

$$\theta_z = 2 \tan^{-1}\left(\frac{f_1}{f_z}\right) \quad (16.55)$$

Hence the total phase lag introduced by the compensation network and the error amplifier at the unity-gain crossover frequency is

$$\theta_c = 270^\circ - 2 \tan^{-1}\left(\frac{f_1}{f_z}\right) + 2 \tan^{-1}\left(\frac{f_p}{f_1}\right) \quad (16.56)$$

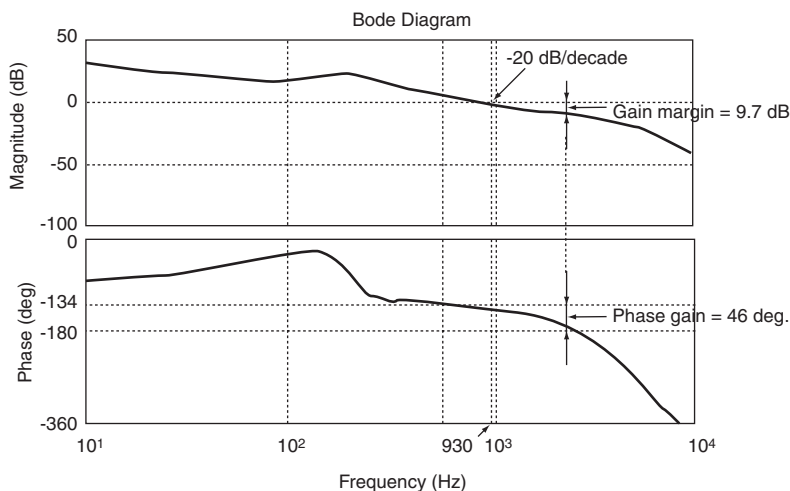


FIGURE 16.21

Bode diagram of the open loop system.

where the 270° phase lag is due to the phase inversion introduced by the inverting amplifier and the pole at the origin of the compensation network.

Consider the real system described in Figure 16.21, the unity-gain crossover frequency is chosen to be 900 Hz, where the attenuation is -16 dB. Hence, the gain of the error amplifier at the unity-gain crossover frequency is chosen to be $+16$ dB in order to yield 0 dB at the unity-gain crossover frequency.

The locations of the double poles and double zeros of the compensation network are chosen to yield the desired phase margin of 45° . The total phase shift at the unity-gain crossover frequency is $360^\circ - 45^\circ$ or 315° . Taking into account the effect of equivalent series resistor (ESR) in the output capacitor, the phase lag of the output filter with an output capacitor ESR is

$$\theta_{LC} = 180^\circ - \tan^{-1}\left(\frac{f_1}{f_{ESR}}\right) \quad (16.57)$$

where f_{ESR} is the ESR break frequency

$$f_{ESR} = \frac{1}{2\pi r_c C_f} \quad (16.58)$$

Then the phase lag contribution from the compensation network and the error amplifier is

$$\theta_{ea} = 315^\circ - \theta_{LC} \quad (16.59)$$

Hence, from Equation (16.58), the phase lag contribution from the compensation network is

$$2 \tan^{-1}\left(\frac{3}{f_z}\right) - 2 \tan^{-1}\left(\frac{f_p}{3}\right) = 270^\circ - \theta_{ea} \quad (16.60)$$

Solving this equation yields a value of 4.64 to achieve a phase lag of 65.67° . Hence, the high-frequency pole should be located at 4.64 times the unity-gain crossover frequency, or 4.2 KHz, while the low-frequency zero should be located at one-fourth of the unity-gain crossover frequency, or 190 Hz. There are six components to be selected for the compensation network. As described previously, the gain at the double zero, K_1 , is 0 dB, or 1. Assuming an R_1 value of 1 K Ω , R_2 is 1 K Ω too. The gain at the double poles, K_2 , is selected to be 20 dB, or 10. Thus, R_3 is given by

$$R_3 = \frac{R_1 R_2}{K_2 R_1 - R_2} \quad (16.61)$$

The capacitance value for C_3 is

$$C_3 = \frac{1}{2\pi f_p R_3} \quad (16.62)$$

Hence, the capacitance values of C_1 and C_2 can be calculated respectively from Equation (16.52) and Equation (16.54).

The Bode diagram of the open loop system is given in [Figure 16.21](#). Notice that the gain at the unity-gain crossover frequency in the overall magnitude response of the feedback-compensated resonant converter is 0 dB with a slope of -20 dB/decade. The unity-gain crossover frequency is enhanced from 540 KHz to 930 KHz, at which point the phase lag is reduced from -175° to -134° . The values of gain margin and phase margin are 9.7 dB and 46° , respectively. Both of them have fit the specified requirements of the stability.

In most cases, the stability plays an important role in various performance indexes of a closed-loop system. For this resonant converter, the stability can be studied by analyzing the characteristics of the poles and zeros of the closed-loop system. Since the small-signal model has been found in previous section, the state-space equations can be established from Equation (16.49), to give:

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u}$$

and

$$\hat{y} = C\hat{x} + D\hat{u}$$

where

$$\hat{x} = \left(\hat{i}_{1s}, \hat{i}_{1c}, \hat{v}_{1s}, \hat{v}_{1c}, \hat{i}_{2s}, \hat{i}_{2c}, \hat{v}_{2s}, \hat{v}_{2c}, \hat{i}_{Lf}, \hat{v}_{Cf} \right)^T$$

$$\hat{u} = \left(\hat{v}, \hat{f}_{sN}, \hat{i}_o \right)^T \quad \hat{y} = \hat{v}_o$$

Based on the relationship between the state-space equation and transfer function, these equations of the open loop system can be transformed to the transfer function $G_1(s)$, to give:

$$G_1(s) = \frac{\hat{Y}(s)}{\hat{U}(s)} = C[sI - A]^{-1}B + D \quad (16.63)$$

By considering both the expression in Equation (16.51) and $G_1(s)$, the closed-loop control system transfer function can be obtained. Hence, the poles of the closed-loop control system are found to be:

$$\begin{aligned} p_{1,2} &= -0.3138 \pm 19.3296i & p_{3,4} &= -0.8750 \pm 12.9716i \\ p_{5,6} &= -0.8809 \pm 5.2819i & p_{7,8} &= -0.3914 \pm 0.9492i \\ p_{9,10} &= -0.0071 \pm 0.0377i & p_{11,12} &= -0.7777 \pm 0.0000i \\ p_{13} &= 0 \end{aligned}$$

Notice that all the real parts of the poles are nonnegative, thus, the whole system is found stable. The root loci of the closed-loop system are given in [Figure 16.22](#).

16.5 Discussion

In all the previous sections, the analyses are undertaken on the basis of the assumption that two resonant inductors are identical, as well as two resonant capacitors. The following discussion will be focused on the condition that the resonant components have different values, that is, variable-parameters.

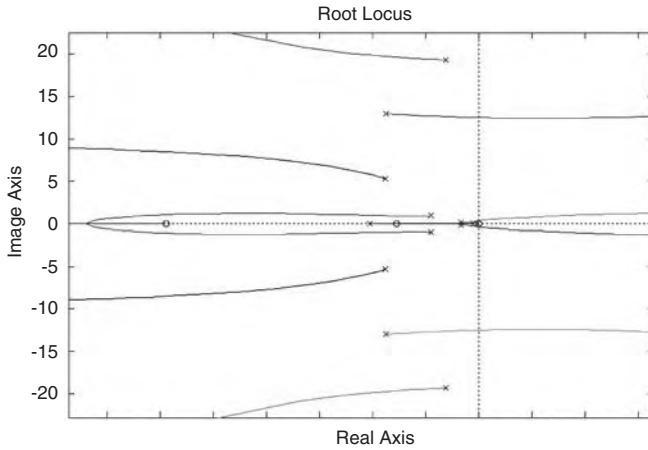


FIGURE 16.22
Root loci of the closed-loop system.

In addition, the discontinuous operation, always occurring when switching frequency is lower than the natural resonant frequency, will also be taken into consideration.

16.5.1 Characteristics of Variable-Parameter Resonant Converter

In fact, most of the derivation results and general conclusions in Section 16.3 and Section 16.4 are still valid for the variable-parameter condition, except that the curves of the voltage transfer gain are a little bit different. For instance, if the ratios of two inductors and two capacitors are defined as:

$$p = L_1 / L_2 \quad \text{and} \quad q = C_1 / C_2$$

then the expression in Equation (16.1) can be rewritten as :

$$g(\omega) = \frac{R_{eq}}{\left(\omega^4 p \beta L^2 C^2 R_{eq} - \omega^2 (pq + p + 1) L C R_{eq} \right.} \quad (16.64)$$

$$\left. + R_{eq} + j[\omega L(p + 1) - \omega^3 L^2 C p q] \right)$$

Following the same definitions of the natural resonant frequency ω_0 , Q value, and relative frequency β , the voltage transfer gain $g(\beta)$ is given by:

$$g(\beta) = \frac{1}{1 - \beta^2 (pq + p + 1) + \beta^4 pq + j[(p + 1) - pq\beta^2] \beta Q} \quad (16.65)$$

and its determinant is

$$|g(\beta)| = \frac{1}{\sqrt{[1 - \beta^2(pq + p + 1) + \beta^4 pq]^2 + [(p + 1) - pq\beta^2]^2 \beta^2 Q^2}} \quad (16.66)$$

The local maximum and minimum values of the voltage gain $g(\beta)$ can be gained by solving the resulting equation after setting the derivatives of the determinant to zero.

$$\frac{d}{d\beta^2} |g(\beta)| = 0 \quad (16.67)$$

$$\begin{aligned} &4p^2 q^2 \beta^6 + [3p^2 q^2 Q^2 - 6pq(pq + p + 1)]\beta^4 \\ &+ [4pq + 2(pq + p + 1)^2 - 4pq(p + 1)Q^2]\beta^2 \\ &+ Q^2(p + 1)^2 - 2(pq + p + 1) = 0 \end{aligned} \quad (16.68)$$

When $p = q = 1$, this equation is simplified to be

$$4\beta^6 + (3Q^2 - 18)\beta^4 + (22 - 8Q^2)\beta^2 + 4Q^2 - 6 = 0$$

which is the same as Equation (16.21).

Figure 16.23a to d depict the voltage gain $|g(\beta)|$ with different parameter ratios referring to various Q values. One can find that all the curves have the similar shape in Figure 16.4, which begins with unity at low switching frequency and displays two peaks with lower Q values. However, the different parameter ratio results in a different bandwidth. Thus, the designer will have more choice to find the most appropriate bandwidth to meet the requirements of various applications. Besides this, with certain parameter ratios (for example, $p = 2$, $q = 1$), all the curves intersect at one point, which is independent of the Q values. The corresponding switching frequency can be calculated by setting the imaginary part of the denominator in the expression in Equation (16.65) to zero, gives:

$$p + 1 = pq\tilde{\beta}^2$$

or

$$\tilde{\beta}^2 = \frac{p + 1}{pq} \quad (16.69)$$

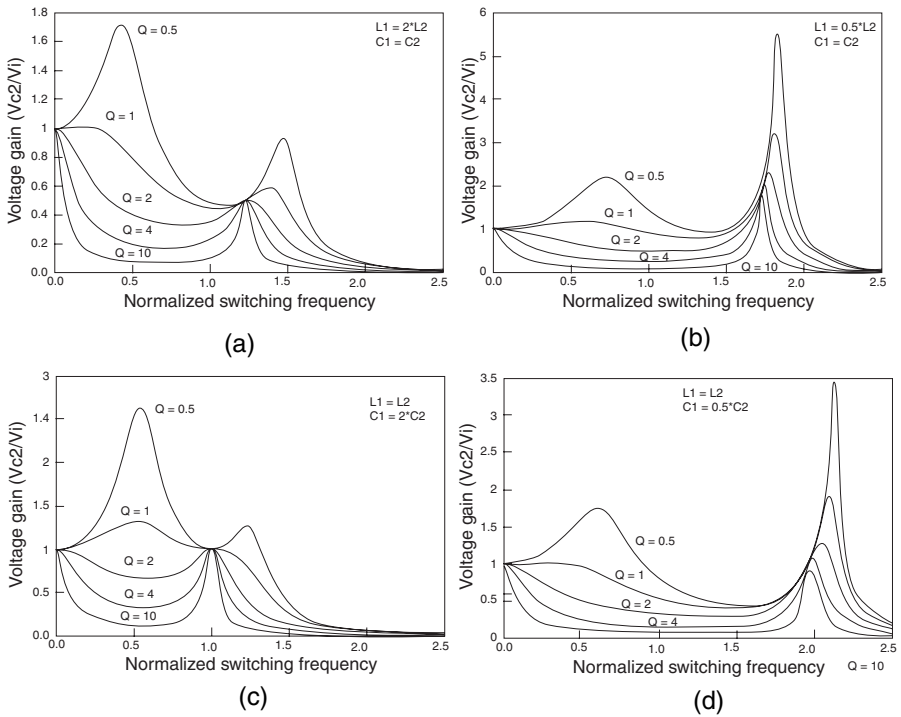


FIGURE 16.23

Voltage gain $|g(\beta)|$ with different parameter ratios referring to various Q .

Substituting Equation (16.69) into Equation (16.65), the voltage gain at this frequency is obtained as:

$$|g(\tilde{\beta})| = \frac{1}{p} \quad (16.70)$$

Hence, the voltage transfer gain is only dependent on the inductors ratio α and it determines the rough shape of the gain curve over a wide frequency range $[0 \sim \tilde{\beta}]$, which is useful for the designer to estimate the needed operating point.

Figure 16.24 gives the maximum voltage transfer gain vs. different parameter ratios of p and q , corresponding to the peak value in Figure 16.23a to d. Notice that the maximum gain is obtained with small p and large q . This is true because when L_1 is much smaller than L_2 while C_1 is larger than C_2 , the cascade reverse double Γ -LC RPC will be degraded to the conventional parallel resonant converter, which voltage gain is prominent near the natural resonant frequency. Figure 16.24 shows the three-dimensional relations.

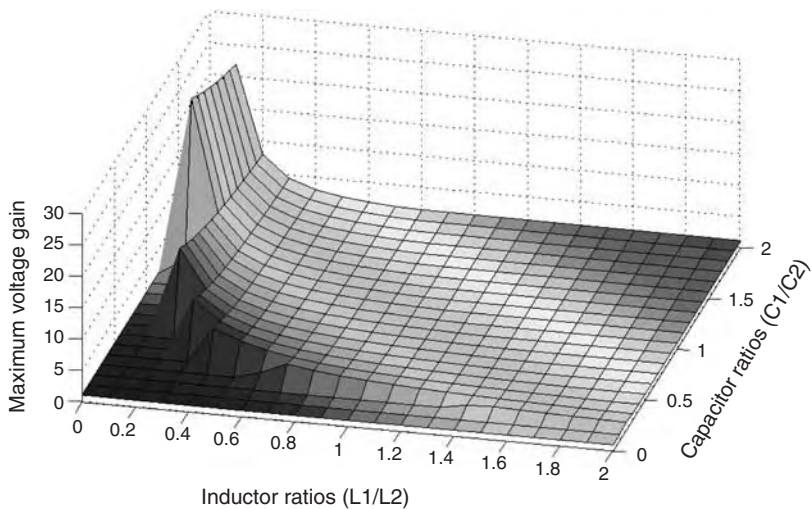


FIGURE 16.24

Maximum voltage gain vs. different parameter ratios of p and q .

The dynamic analysis of the variable-parameter resonant converter is similar to that in the previous section, except that some relevant matrices need to be amended. The waveforms of the input and the resonant voltage are shown in [Figure 16.25a](#), where some distortions can be found in the second capacitor voltage v_{c2} . Figure 16.25b is the probe output of the commonly used circuit simulation software PSpice. From this one can find a good accordance between the two figures.

The comparison of the resonant output voltage and total harmonic distortion (THD) of the variable-parameter resonant converter is given in [Table 16.1](#). Compared to other conditions, the second capacitor voltage obtains the highest amplitude when $L_1 = L_2$, $C_1 = C_2$, while it keeps the lowest total harmonic distortion value. Thus, it is reasonable to implement the practical cascade reverse double Γ -LC RPC with dual symmetric resonant network.

16.5.2 Discontinuous Conduction Mode (DCM)

When the switching frequency is lower than half of the natural resonant frequency, the current through the inductors and the voltage across the capacitors will become discontinuous. For the cascade reverse double Γ -LC PRC, in DCM operation, the energy in the resonant capacitor is consumed before the new half of a switching cycle. There are six stages of operation in one switching cycle, as shown in [Figure 16.26](#). Suppose before the beginning of a switching cycle, the second inductor current i_{L2} is zero. When stage 1 begins at time t_0 , since i_{L2} is lower than the constant-current-sink I_o , all the

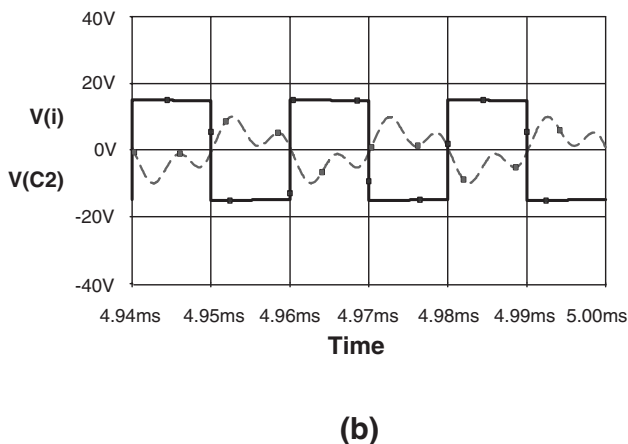
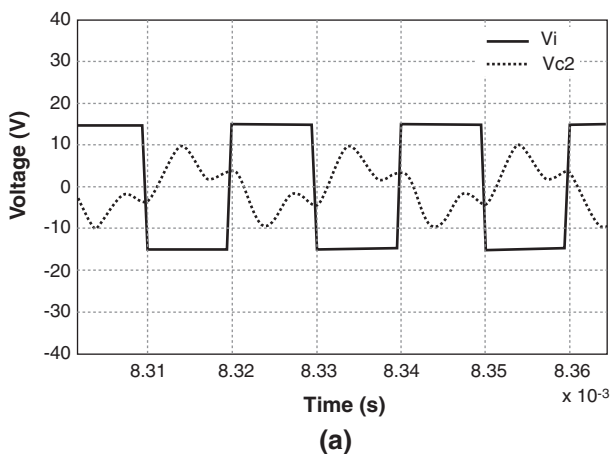


FIGURE 16.25

Simulation waveforms using Matlab (a) and PSpice (b) when $L_1 = 10 L_2$.

rectifier diodes become forward biased and conduct. The second capacitor C_2 is clamped to zero volts by the freewheeling action, which is shown in [Figure 16.27a](#). Thus, the second inductor L_2 is charged and the current through it is increased. Stage 2 commences when the current i_{L2} reaches the magnitude of the current-sink I_{or} at time t_1 . The topology at this moment is the same as that in CCM operation. Stage 3 starts when the input voltage source V_i changes its polarity at time t_2 , as depicted in [Figure 16.27c](#). This completes the first half-cycle of operation. The next half-cycle operation repeats the same way as the first half-cycle, except that the direction of the inductor current i_{L2} and the polarity of the capacitor voltage v_{C2} are reversed.

The state coefficient matrix and input source vector corresponding to two additional operating modes are given by:

TABLE 16.1

Comparison of Output Resonant Voltage and THD Values under Different Parameter Ratios

$\alpha(L_1/L_2)$	$\beta(C_1/C_2)$	Switching frequency $f_s = 50$ KHz	
		V_{c2} Amplitude (V)	THD (%)
1	1	23.5	2.41
2	1	11.0	7.90
0.5	1	17.0	6.84
1	2	6.0	5.82
1	0.5	8.0	5.93
2	2	3.5	2.72
0.5	0.5	10.0	7.14
0.5	2	19.0	8.55
2	0.5	6.0	3.91

Note: With $L_2 = 100 \mu\text{H}$, $C_2 = 0.22 \mu\text{F}$, $R = 22 \Omega$, $L_f = 2.4 \text{ mH}$, $C_f = 220 \mu\text{F}$

TABLE 16.2

Comparison of Output Voltage and THD among Different Resonant Converters

Converter	THD(%)	$V_o(\text{V})$	Harmonic Statistics			Harmonic proportion (%)		
			1st	3rd	5th	1st	3rd	5th
SRC	3.355	7.88	16.50	3.042	3.663	100	18.4	22.2
RPC	4.254	6.09	12.18	0.419	0.261	100	3.44	2.14
SRPC	4.341	15.9	59.87	2.485	0.625	100	4.15	1.04
CRD Γ -LC	2.407	12.0	23.29	0.517	0.179	100	2.22	0.77
V_i	—	—	18.83	6.366	3.820	100	33.8	18.5

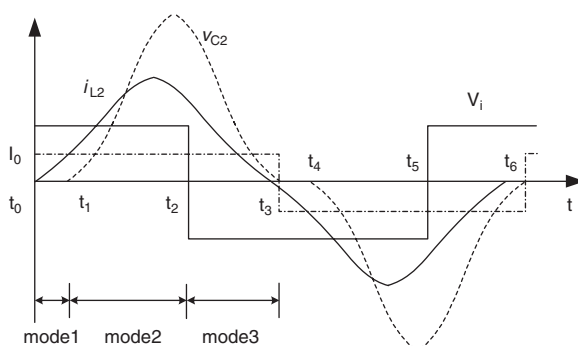


FIGURE 16.26

Switching waveforms for the discontinuous-mode cascade reverse double Γ -LC RPC.

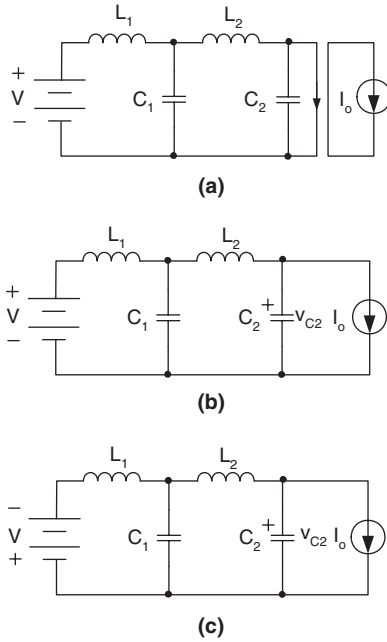


FIGURE 16.27
Discontinuous-mode equivalent circuits in half cycle.

$$A_5 = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 & 0 & 0 \\ 1/C_1 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/L_f \\ 0 & 0 & 0 & 0 & 1/C_f & -1/RC_f \end{bmatrix}$$

$$B_5 = [V/L_1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]^T$$

and

$$A_6 = A_5 \quad B_6 = [-V/L_1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]^T$$

The augmented state-space equation in Section 16.4 is still valid besides that the state transition matrices describing two additional operating modes should be considered as well. The waveforms of simulation and experimental results under DCM operation are shown in [Figure 16.28](#). Note that the

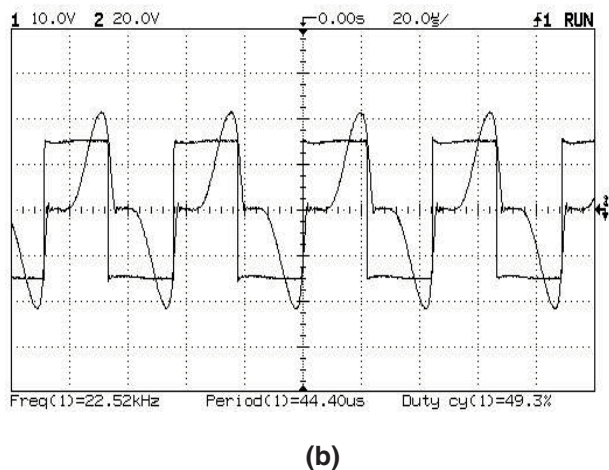
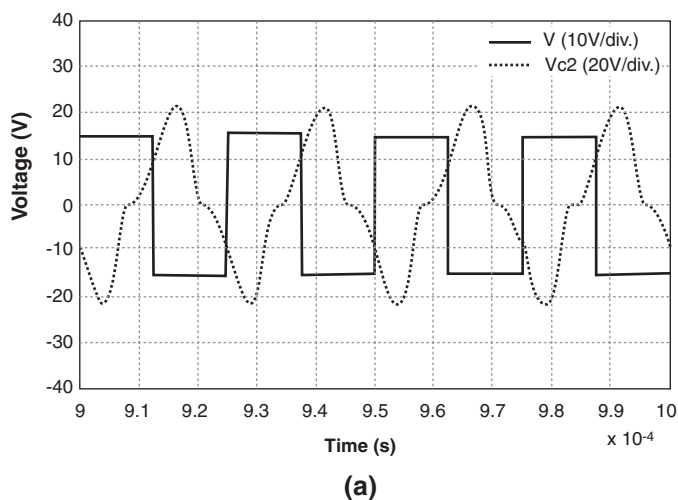


FIGURE 16.22

Simulation (a) and experimental (b) switching waveforms for DCM operation.

second capacitor voltage is discontinuous at some intervals, which verifies the description of the theoretical analysis.

In practice, the discontinuous conduction mode is often dependent on the switching frequency and the equivalent load current I_0 . Namely, under a certain load current, when the switching frequency is increased, the operating state of the resonant converter will transfer from DCM to CCM. Conversely, if the switching frequency is invariant, the increase of the load current will lead to the occurrence of DCM. Thus, it is very significant to

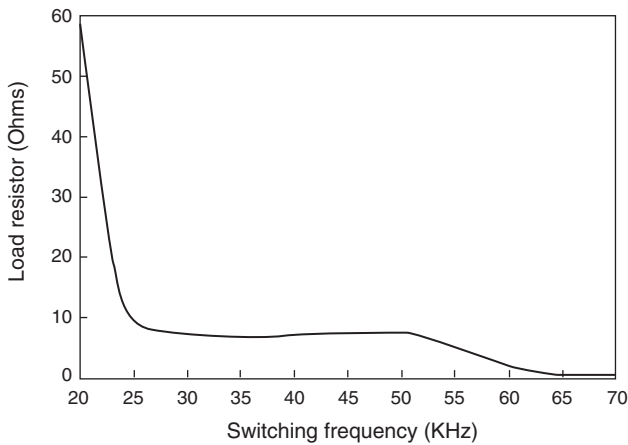


FIGURE 16.29

Critical load resistor vs. the switching frequency.

find the relationship between the load current and the switching frequency, in other words, to find the critical load current J_{cr} under a certain frequency.

In many open literatures, the critical load current is always obtained by solving the differential equations and identifying the respective duration of various subintervals. For instance, the normalized critical load current of RPC is given:

$$J_{cr} = \sqrt{\sin^2(\gamma/2) + \sin^2(\gamma)/4} - \sin(\gamma)/2 \quad (16.71)$$

This conclusion is very simple and straightforward to describe the relationship between f_s and I_0 . However, it is acquired at the cost of very complicated calculations and derivations. For SRPC, there is no similar analytical expression given in the literature. In fact, with the increase of the quantity of the resonant components, the order of the differential equations becomes very large so that it seems impossible to solve them by pen and paper. Once again, the numerical calculation offers a very useful solution to overcome such a problem.

The numerical analysis method starts at solving the higher order state equations using recursion algorithm. Once the steady state is achieved, it is up to the algorithm that judges whether the critical load current is found correctly. The drawbacks of this method are in two aspects: one is the discrete result; the other is time-consuming. However, the obtained results are proved to be precise and useful so long as the step of the loop is small enough. The critical load resistor and critical load current vs. the switching frequency are shown in Figure 16.29 and Figure 16.30 respectively.

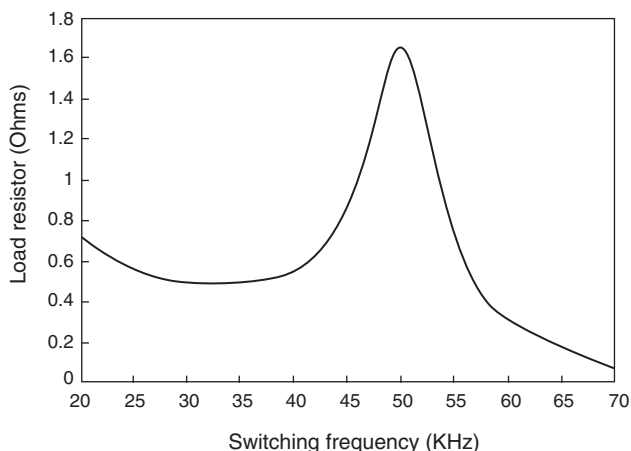


FIGURE 16.30
Critical load current vs. the switching frequency.

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APPENDIX

Parameters Used in Small-Signal Modeling

$$k_v = \frac{4}{\pi}$$

$$k_s = \frac{2}{\pi} \frac{V_{2s}}{A_p}$$

$$k_c = \frac{2}{\pi} \frac{V_{2c}}{A_p}$$

$$Z_{L1} = \Omega_s L_1$$

$$Z_{L2} = \Omega_s L_2$$

$$G_s = \Omega_s C_1$$

$$E_{1s} = \omega_0 L_1 I_{1c}$$

$$E_{1c} = \omega_0 L_1 I_{1s}$$

$$E_{2s} = \omega_0 L_2 I_{2c}$$

$$E_{2c} = \omega_0 L_2 I_{2s}$$

$$J_{1s} = \omega_0 C_1 V_{1c}$$

$$J_{1c} = \omega_0 C_1 V_{1s}$$

$$J_{2s} = \omega_0 C_2 V_{2c}$$

$$J_{2c} = -\omega_0 C_2 V_{2s}$$

$$g_{ss} = \frac{g_e \alpha^2}{\alpha^2 + \beta^2}$$

$$g_{cc} = \frac{g_e \beta^2}{\alpha^2 + \beta^2}$$

$$g_{sc} = \Omega_s C_2 + \frac{\alpha \beta}{\alpha^2 + \beta^2}$$

$$g_{cs} = -\Omega_s C_2 + \frac{\alpha \beta}{\alpha^2 + \beta^2}$$

$$V_e = \frac{4}{\pi} V_g$$

$$g_e = \frac{8}{\pi^2 R}$$

$$A_p = \frac{1}{\sqrt{\alpha^2 + \beta^2}} V_e$$

$$\alpha = g_e \Omega_s L (\Omega_s^2 LC - 2)$$

$$\beta = \Omega_s^4 L^2 C^2 - 3 \Omega_s^2 LC + 1$$

DC Energy Sources for DC/DC Converters

The DC/DC converter is used to convert a DC source voltage to another DC voltage actuator (user). In a DC/DC converter system the main parts are the DC voltage source, switches, diodes, inductors/capacitors, and load. This chapter introduces the various DC energy sources that are usually employed in DC/DC converters.

17.1 Introduction

In a DC/DC converter system the initial energy source is a DC voltage source with certain voltage and very low internal impedance, which can be usually omitted. This means the used DC voltage source is ideal. The DC voltage source can be a battery, a DC bus (usually equipped in factories and laboratories), a DC generator, and an AC/DC rectifier. As is well-known, the battery, DC bus, and DC generator can be considered an ideal voltage source. They will be not discussed in this book. AC/DC rectifiers are widely applied in industrial applications and research centers since it is easily constructed and less costly. In this chapter the AC/DC rectifiers will be discussed in detail. AC/DC rectifiers can be grouped as follows:

- Single-phase half-wave diode rectifier
- Single-phase full-wave bridge diode rectifier
- Three-phase bridge diode rectifier
- Single-phase half-wave thyristor rectifier
- Single-phase full-wave bridge thyristor rectifier
- Three-phase bridge thyristor rectifier
- Other devices rectifiers

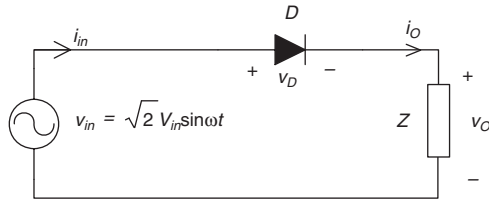


FIGURE 17.1
Half-wave diode rectifier.

17.2 Single-Phase Half-Wave Diode Rectifier

The single-phase half-wave diode rectifier is shown in Figure 17.1, it is the simplest rectifier circuit. The load Z in the figure can be any type such as resistor, inductor, capacitor, back electromotive force (EMF), and/or a combination of these. This rectifier can rectify the AC input voltage into DC output voltage. The analysis of the circuit is based on the assumption that a diode as an ideal component is used for the rectification. A diode forward biased will conduct without forward voltage-drop and resistance. A diode reverse biased will be blocked, and likely an open circuit. Since the used diode is not continuously conducted, the output current is always discontinuous in some part of negative half-cycle.

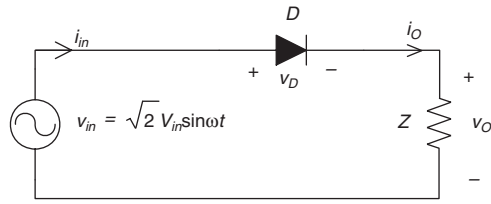
17.2.1 Resistive Load

A single-phase half wave rectifier with a purely resistive load (R) is shown in Figure 17.2a, and its input/output voltage v_{in} and v_o , and input/output current i_{in} and i_o waveforms are shown in Figure 17.2b and c. The AC supply voltage v_{in} is sinusoidal, the output voltage and current obey Ohm's law. Therefore the output voltage and current are sinusoidal half-waveforms

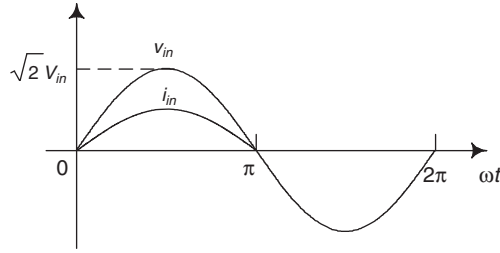
$$v_{in}(t) = \sqrt{2} V_{in} \sin \omega t \quad (17.1)$$

$$v_o(t) = \begin{cases} \sqrt{2} V_{in} \sin \omega t & 0 \leq \omega t \leq \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \quad (17.2)$$

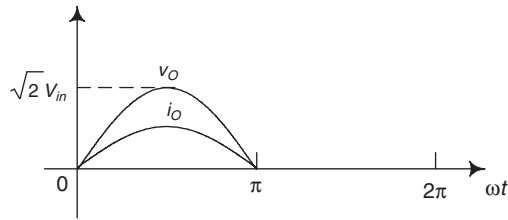
$$i_{in}(t) = i_o(t) = \begin{cases} \frac{\sqrt{2} V_{in}}{R} \sin \omega t & 0 \leq \omega t \leq \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \quad (17.3)$$



(a) Circuit diagram



(b) Input voltage and current



(c) Output voltage and current

FIGURE 17.2

A single-phase half wave rectifier with a purely resistive load (R).

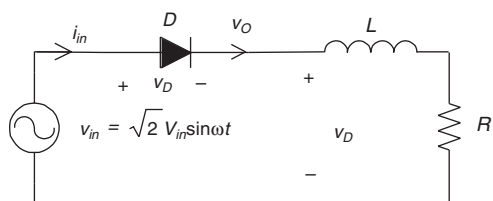
Where V_{in} is the root-mean-square (RMS) value of the input voltage. The input wave is a sinusoidal waveform, the corresponding output is half-wave of a sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output DC average voltage and current are

$$V_{O-av} = \frac{\sqrt{2}}{\pi} V_{in} = 0.45 V_{in} \quad (17.4)$$

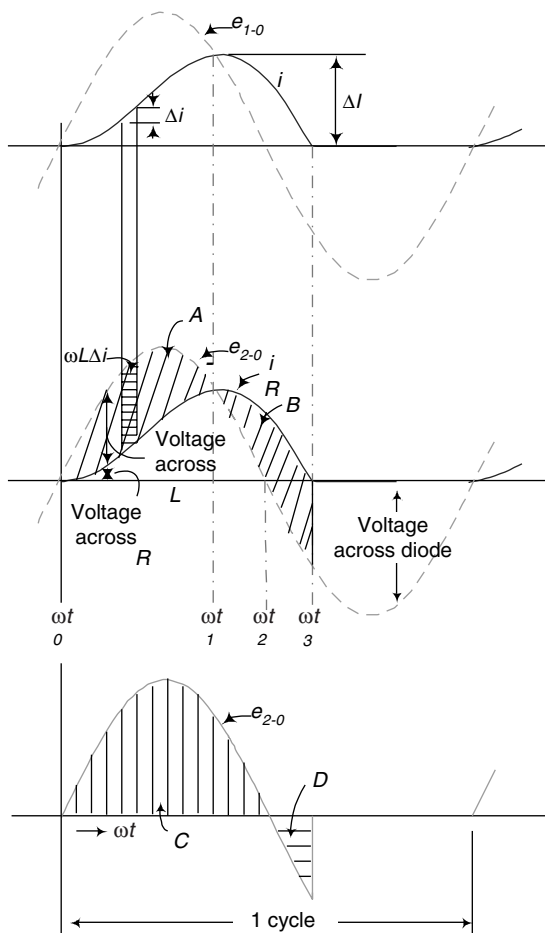
$$I_{O-av} = 0.45 \frac{V_{in}}{R} \quad (17.5)$$

17.2.2 Inductive Load

A single-phase half wave rectifier with an inductive load (a resistor R plus an inductor L) is shown in [Figure 17.3a](#). The input voltage and current v_{in} and i_{in} waveforms are shown in [Figure 17.3b](#), output voltage v_O in c and



(a) Circuit diagram



(b), (c), and (d)

FIGURE 17.3

A single-phase half wave rectifier with an inductive load ($R + L$).

output current i_o in d. The AC supply voltage is sinusoidal, the output voltage and current obey Ohm's law. The impedance of load is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{\omega L}{R}$$

Input voltage is

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

Output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & 0 \leq \omega t \leq (\pi + \phi) \\ 0 & (\pi + \phi) < \omega t < 2\pi \end{cases} \quad (17.6)$$

Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is a partial sinusoidal waveform more than half-cycle. Since it is negative value in the negative half-cycle, the output DC average voltage is

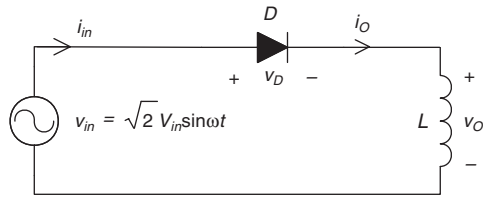
$$V_{O-av} = \frac{\sqrt{2}}{\pi} (1 - \cos \phi) V_{in} = 0.45(1 - \cos \phi) V_{in} \quad (17.7)$$

The input and output current waveform is no longer a sinusoidal waveform.

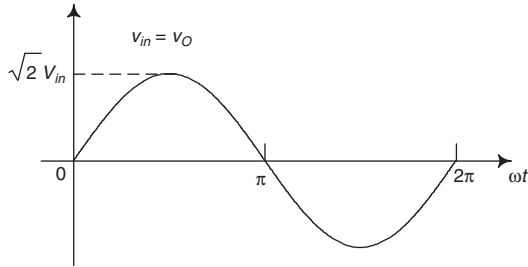
$$i_{in}(t) = i_o(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{|Z|} [\sin(\omega t - \phi) + \sin \phi \cdot e^{-t/\tau}] & 0 \leq \omega t \leq (\pi + \phi) \\ 0 & (\pi + \phi) < \omega t < 2\pi \end{cases} \quad (17.8)$$

where τ is the load time constant $\tau = L/R$. The input and output current average value is

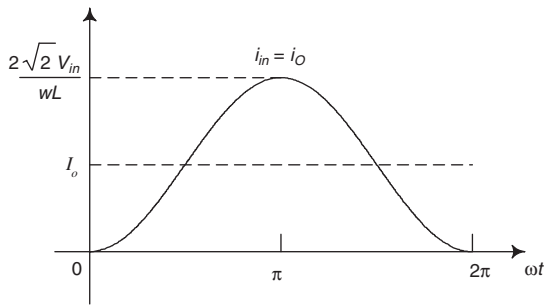
$$I_{O-av} = 0.45 \frac{V_{in}}{R} (1 - \cos \phi) \quad (17.9)$$



(a) Circuit diagram



(b) Input and output voltages



(c) Input and output currents

FIGURE 17.4

A single-phase half wave rectifier with a pure inductive load (L).

17.2.3 Pure Inductive Load

A single-phase half wave rectifier with a pure inductive load (an inductor L only) is shown in Figure 17.4a, and its input/output voltage v_{in} and v_O and input/output current i_{in} and i_O waveforms are shown in Figure 17.4b and c. The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal, the output voltage can follow it in time. The impedance of load is

$$Z = j\omega L = \omega L \angle \pi / 2$$

Input and output voltage is

$$v_{in}(t) = v_o(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1a)$$

Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output can be a full sinusoidal waveform too. Since it is negative value in full negative half-cycle, the output DC average voltage is 0.

The input and output current waveform is a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \frac{\sqrt{2}V_{in}}{\omega L} (1 - \cos \omega t) \quad (17.10)$$

17.2.4 Back EMF Plus Resistor Load

A single-phase half wave rectifier with a resistor plus an EMF load (a resistor R plus an EMF) is shown in [Figure 17.5a](#), and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in [Figure 17.5b and c](#). The EMF value is E which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m is

$$m = E / \sqrt{2}V_{in} < 1$$

and

$$\alpha = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

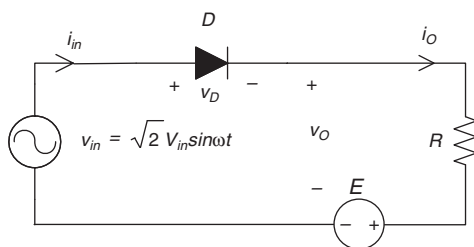
The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal, the output voltage and current obey Ohm's law. The impedance of load is

$$\text{Input voltage is } v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

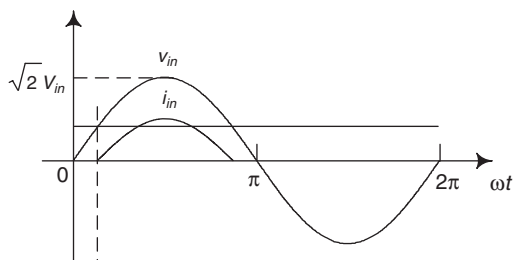
$$\text{Input voltage is } v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\pi - \alpha) \\ E & (\pi - \alpha) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.11)$$

Where V_{in} is the RMS value of the input voltage. The input wave is a sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle. The output DC average voltage is

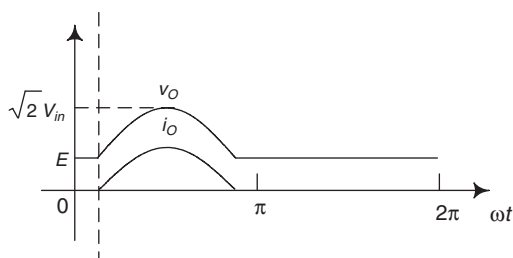
$$V_{O-av} = \frac{\sqrt{2}V_{in}}{\pi} \cos \alpha + E \left(\frac{1}{2} + \frac{\alpha}{\pi} \right) > E \quad (17.12)$$



(a) Circuit diagram



(b) Input voltage and current



(b) Output voltage and current

FIGURE 17.5

Single-phase half wave rectifier with an EMF plus resistor ($R + EMF$).

The input and output current waveform is no longer a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in} \sin \omega t - E) & \alpha \leq \omega t \leq (\pi - \alpha) \\ 0 & (\pi - \alpha) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.13)$$

The input and output current average value is

$$I_{O-av} = \frac{0.45V_{in}}{2R} [2 \cos \alpha - m(\pi - 2\alpha)] \quad (17.14)$$

17.2.5 Back EMF Plus Inductor Load

A single-phase half wave rectifier with an EMF and inductive load (an EMF plus an inductor L) is shown in Figure 17.6a, and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 17.6b and c. The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal waveform:

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

$$\text{Output voltage is } v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\pi + \gamma) \\ E & (\pi + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.15)$$

$$\text{Where } \int_{\alpha}^{\pi-\alpha} (\sqrt{2}V_{in} \sin \omega t - E)d(\omega t) = \int_{\pi-\alpha}^{\pi-\alpha+\gamma} (E - \sqrt{2}V_{in} \sin \omega t)d(\omega t)$$

Where v_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is a partial sinusoidal waveform. The output DC average voltage is E .

The input and output current waveform is no longer a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{\omega L} [(\cos \alpha - \cos \omega t) - m(\omega t - \alpha)] & \alpha \leq \omega t \leq (\pi + \alpha + \gamma) \\ 0 & (\pi + \alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.16)$$

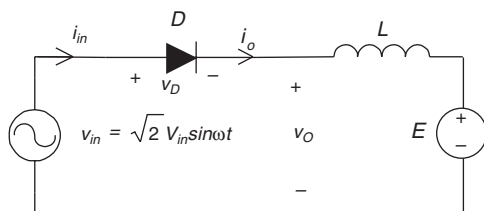
The input and output current average value is

$$I_{O-av} = \frac{0.45V_{in}}{2\omega L} [\gamma \cos \gamma - \sin(\alpha + \gamma) + \sin \alpha - \frac{m}{2} \alpha^2] \quad (17.17)$$

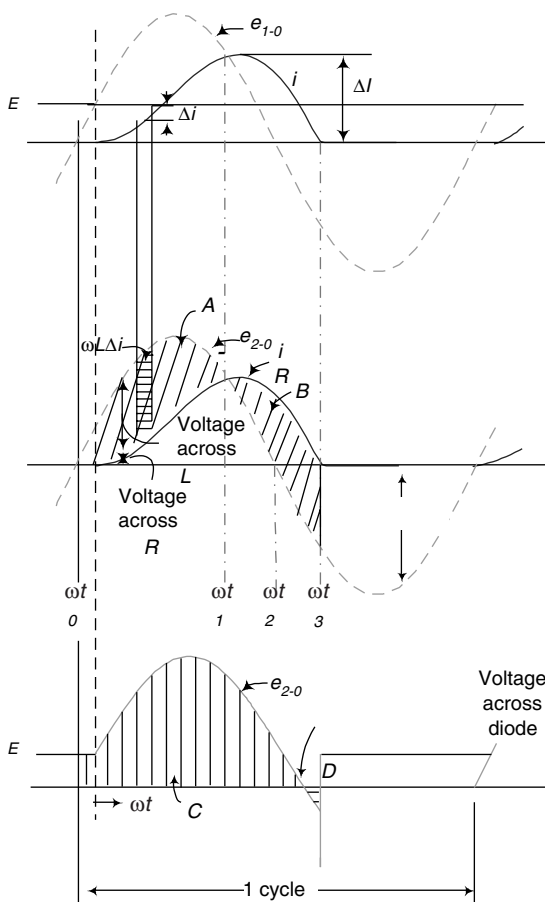
17.3 Single-Phase Bridge Diode Rectifier

Single-phase full-wave diode rectifier has two forms:

- Bridge (Graetz)
- Center-tap (mid-point)



(a) Circuit diagram

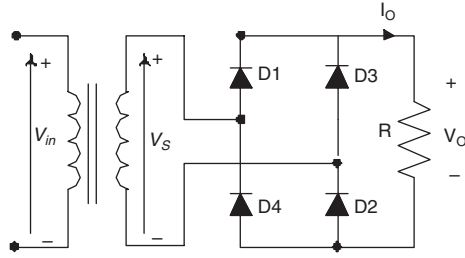


(b), (c) and (d)

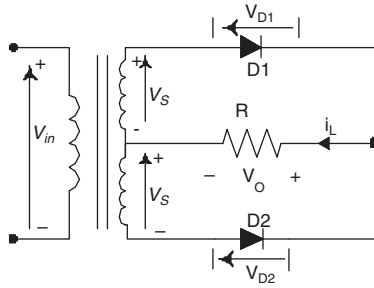
FIGURE 17.6

Single-phase half wave rectifier with EMF plus inductor ($EMF + L$).

These are shown in [Figure 17.7a and b](#). The input and output waveforms are same in both circuits. Use Graetz type for the description in the following sections.



(a) Bridge (Graetz)



(b) Center-tap (Midpoint)

FIGURE 17.7
Single-phase full-wave diode rectifier.

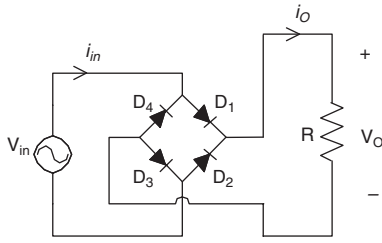
17.3.1 Resistive Load

A single-phase full-wave diode rectifier with a purely resistive load is shown in [Figure 17.8a](#), and its input/output voltage v_{in} and v_O and input/output current i_{in} and i_O waveforms are shown in [Figure 17.8b and c](#). The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal, the output voltage and current obey Ohm's law. Therefore the output voltage and current are sinusoidal half-waveforms.

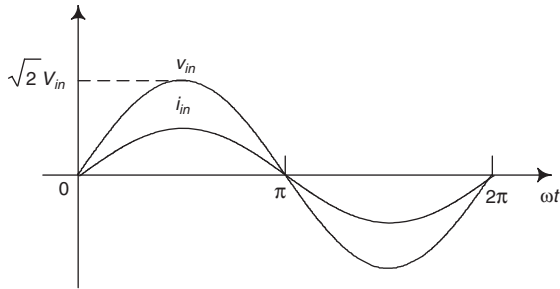
$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.18)$$

$$v_O(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & 0 \leq \omega t \leq \pi \\ \sqrt{2}V_{in} \sin(\omega t - \pi) & \pi < \omega t < 2\pi \end{cases} \quad (17.19)$$

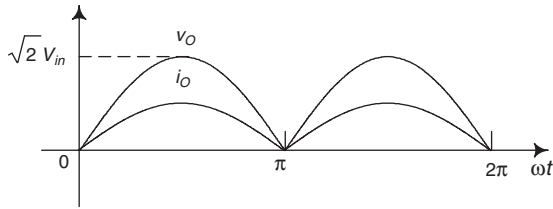
$$i_{in}(t) = i_O(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{R} \sin \omega t & 0 \leq \omega t \leq \pi \\ \frac{\sqrt{2}V_{in}}{R} \sin(\omega t - \pi) & \pi < \omega t < 2\pi \end{cases} \quad (17.20)$$



(a) Circuit diagram



(b) Input voltage and current



(c) Output voltage and current

FIGURE 17.8

Single-phase full-wave diode rectifier with a purely resistive load.

Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is repeating half-wave sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output is a DC voltage with ripple in the repeating frequency 2ω . After FFT analysis of the rectified waveform, harmonics components are shown in the frequency spectrum. From the spectrum, there are only n th ($n = 2k$) harmonics existing. The parameter ripple factor RF is defined

$$RF = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{\sum_{n=1}^{\infty} V_n^2}}{V_{dc}} \quad (17.21)$$

where V_{dc} is the DC component of the output voltage, which is the average value, V_n is the n th order harmonic component of the output voltage. The output DC average voltage and current are

$$V_{O-av} = \frac{2\sqrt{2}}{\pi} V_{in} = 0.9 V_{in} \quad (17.22)$$

$$I_{O-av} = 0.9 \frac{V_{in}}{R} \quad (17.23)$$

17.3.2 Back EMF Load

A single-phase full-wave diode rectifier with an EMF plus resistor load (a resistor R plus an EMF) is shown in [Figure 17.9a](#), and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in [Figure 17.9b and c](#). The EMF value is E which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m :

$$m = E/\sqrt{2}V_{in} < 1$$

and

$$\alpha = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal, the output voltage and current obey Ohm's law. The impedance of load is

$$\text{Input voltage is } v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

$$\text{Output voltage is } v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\pi - \alpha) \\ E & (\pi - \alpha) < \omega t < (\pi + \alpha) \end{cases} \quad (17.24)$$

Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle with repeating frequency of 2ω . The output DC average voltage is

$$V_{O-av} = \frac{2\sqrt{2}V_{in}}{\pi} \cos \alpha + \frac{2\alpha}{\pi} E > E \quad (17.25)$$

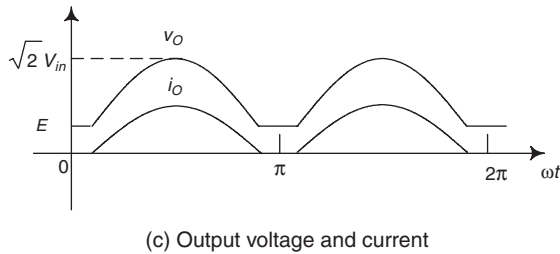
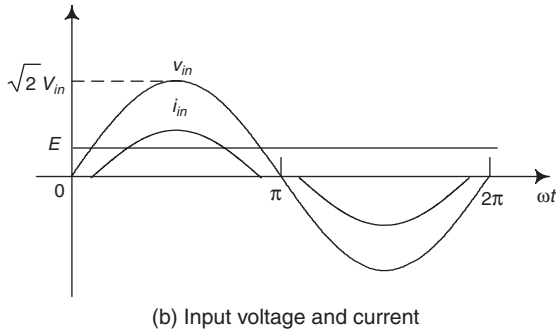
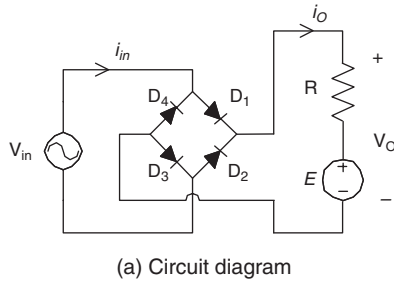


FIGURE 17.9

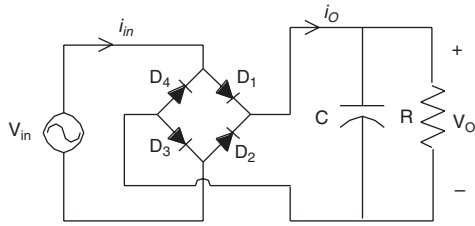
Single-phase full-wave *D*-rectifier with EMF plus resistor ($R + EMF$).

The input and output current waveform is no longer a sinusoidal waveform.

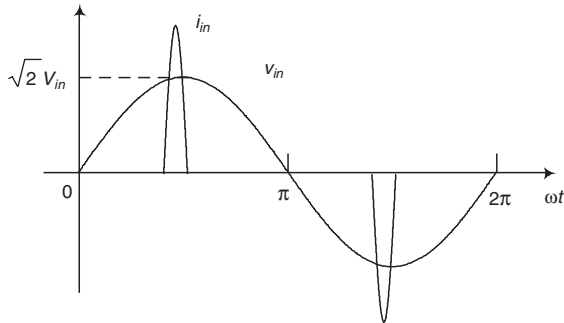
$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in} \sin \omega t - E) & \alpha \leq \omega t \leq (\pi - \alpha) \\ 0 & (\pi - \alpha) < \omega t < (\pi + \alpha) \end{cases} \quad (17.26)$$

The input and output current average value is

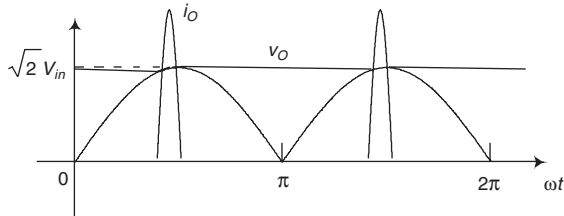
$$I_{O-av} = \frac{0.45V_{in}}{R} [\cos \alpha - m(\pi - 2\alpha)] \quad (17.27)$$



(a) Circuit diagram



(b) Input voltage and current



(c) Output voltage and current

FIGURE 17.10

Single-phase full wave *D*-rectifier with an capacitive load ($R + C$).

17.3.3 Capacitive Load

A single-phase full wave diode rectifier with a capacitive load (a resistor R plus a capacitor C) is shown in Figure 17.10a, and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 17.10b and c. The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal. The load time constant $\tau = RC$.

Input voltage is
$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

From previous section analysis, the peak value of output voltage is $V_{max} = \sqrt{2}V_{in}$. The minimum output DC voltage is V_{min} . The capacitor charges from V_{min} to V_{max} during t_1 , discharges from V_{max} to V_{min} during $t_2 = T/2 - t_1 \cong 1/2f$ since usually $t_1 \ll t_2$.

The minimum output DC voltage is V_{min}

$$V_{min} = \sqrt{2}V_{in} e^{-\frac{t_2}{\tau}} \approx \sqrt{2}V_{in} e^{-\frac{1}{2fRC}} \quad (17.28)$$

Considering the peak-to-peak variation of the output DC voltage is

$$V_{pp} = \sqrt{2}V_{in} (1 - e^{-t_2/\tau}) \approx \sqrt{2}V_{in} (t_2 / \tau) = \frac{\sqrt{2}V_{in}}{2fRC} \quad (17.29)$$

Defining

$$\beta = \cos^{-1} \frac{\sqrt{2}V_{in} - V_{pp}}{\sqrt{2}V_{in}} = \cos^{-1}(e^{-t_2/\tau}) \approx \cos^{-1}(1 - \frac{1}{2fRC}) \quad (17.30)$$

Output voltage is

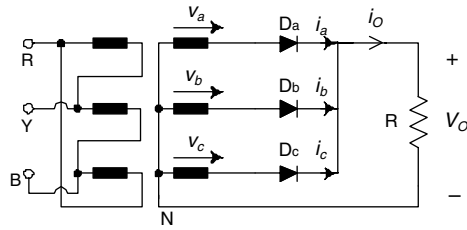
$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & (\frac{\pi}{2} - \beta) \leq \omega t \leq \pi / 2 \\ \sqrt{2}V_{in} - \frac{\omega t + \pi / 2}{\pi} V_{pp} & \frac{\pi}{2} < \omega t < (\frac{3\pi}{2} - \beta) \end{cases} \quad (17.31)$$

Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle. The repeating frequency is 2ω . The output DC average voltage is

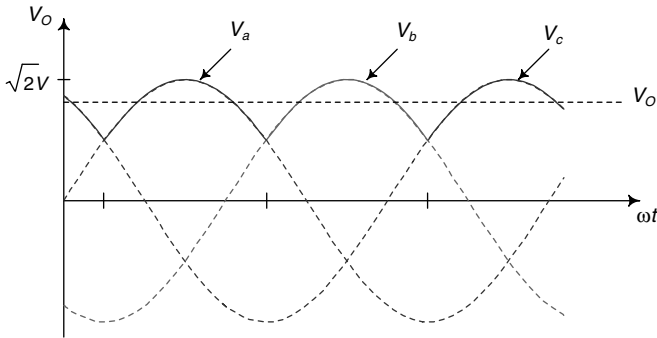
$$V_{O-av} = \sqrt{2}V_{in} (1 - \frac{1}{4fRC}) \quad (17.32)$$

The capacitor charging and discharging current waveform is nearly a rectangular-wave.

$$v_c(t) = \begin{cases} \frac{V_{av}}{R} \frac{\pi - \beta}{\beta} & (\frac{\pi}{2} - \beta) \leq \omega t \leq \pi / 2 \\ -\frac{V_{av}}{R} & \frac{\pi}{2} < \omega t < (\frac{3\pi}{2} - \beta) \end{cases} \quad (17.33)$$



(a) Circuit diagram



(b) Input voltage waveform

FIGURE 17.11

A three-phase half-bridge diode rectifier with a resistor (R).

17.4 Three-Phase Half-Bridge Diode Rectifier

A three-phase half-bridge diode rectifier is shown in Figure 17.11. The three phase AC suppliers have the same RMS value V_{in} with amplitude $\sqrt{2}V_{in}$ and frequency ω , the phase angle shift is 120° .

17.4.1 Resistive Load

A three-phase half-bridge diode rectifier with a purely resistive load is shown in Figure 17.11a, and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 17.11b. The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal. Therefore the output voltage and current are sinusoidal half-waveforms.

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.34)$$

$$v_o(t) = \sqrt{2}V_{in} \sin \omega t \quad \left(\frac{2n\pi}{3} + \frac{\pi}{6}\right) \leq \omega t \leq \left(\frac{2n\pi}{3} + \frac{5\pi}{6}\right) \quad (17.35)$$

where $n = 1, 2, 3, \dots$

$$i_{in}(t) = i_o(t) = \frac{\sqrt{2}V_{in}}{R} \sin \omega t \quad \left(\frac{2n\pi}{3} + \frac{\pi}{6}\right) \leq \omega t \leq \left(\frac{2n\pi}{3} + \frac{5\pi}{6}\right) \quad (17.36)$$

Where V_{in} is the RMS value of the input voltage. The input wave is a sinusoidal waveform, the corresponding output is a repeating partial sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output is a DC voltage with ripple in the repeating frequency 3ω . After FFT analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only n th ($n = 3k$) harmonics existing. The parameter ripple factor RF is defined

$$RF = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{\sum_{n=1}^{\infty} V_n^2}}{V_{dc}} \quad (17.37)$$

where V_{dc} is the DC component of the output voltage which is the average value, V_n is the n th order harmonic component of the output voltage. The output DC average voltage and current are

$$V_{O-av} = \frac{3\sqrt{6}}{2\pi} V_{in} = 1.17V_{in} \quad (17.38)$$

$$I_{O-av} = 1.17 \frac{V_{in}}{R} \quad (17.39)$$

17.4.2 Back EMF Load ($0.5 \sqrt{2}V_{in} < E < \sqrt{2}V_{in}$)

A three-phase half-wave diode rectifier with an EMF plus resistor load (a resistor R plus an EMF) is shown in [Figure 17.12](#). This section discusses the case that EMF value E is in condition: $0.5 \sqrt{2}V_{in} < E < \sqrt{2}V_{in}$. Suppose an auxiliary parameter m :

$$0.5 < m = E/\sqrt{2}V_{in} < 1$$

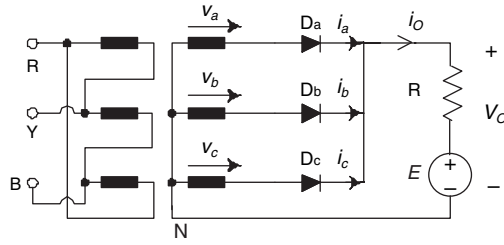


FIGURE 17.12

Three-phase half-wave diode rectifier with EMF plus resistor ($R + EMF$).

and

$$30^\circ < \alpha = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}} < 90^\circ$$

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal, the output voltage and current obey Ohm's law. The impedance of load is R

Input voltage is
$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

Output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & (\frac{2n\pi}{3} + \alpha) \leq \omega t \leq (\frac{2n\pi}{3} + \pi - \alpha) \\ E & \text{other} \end{cases} \quad (17.40)$$

Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle with repeating frequency of 3ω . The output DC average voltage is

$$V_{O-av} = \frac{3\sqrt{2}V_{in}}{\pi} \cos \alpha + (\frac{3\alpha}{\pi} - \frac{1}{2})E > E \quad (17.41)$$

The input and output current waveform is no longer a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in} \sin \omega t - E) & \alpha \leq \omega t \leq (\pi - \alpha) \\ 0 & (\pi - \alpha) < \omega t < (\pi + \alpha) \end{cases} \quad (17.42)$$

17.4.3 Back EMF Load ($E < 0.5 \sqrt{2}V_{in}$)

A three-phase half-wave diode rectifier with an EMF plus resistor load (a resistor R plus an EMF) is shown in Figure 17.12. The EMF value E is in the condition $E < 0.5 \sqrt{2}V_{in}$. Suppose an auxiliary parameter m :

$$m = E/\sqrt{2}V_{in} < 0.5$$

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.34)$$

$$v_o(t) = \sqrt{2}V_{in} \sin \omega t \quad \left(\frac{2n\pi}{3} + \frac{\pi}{6}\right) \leq \omega t \leq \left(\frac{2n\pi}{3} + \frac{5\pi}{6}\right) \quad (17.35)$$

where $n = 1, 2, 3, \dots$

$$i_m(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in} \sin \omega t - E) & \left(\frac{2n\pi}{3} + \frac{\pi}{6}\right) \leq \omega t \leq \left(\frac{2n\pi}{3} + \frac{5\pi}{6}\right) \\ 0 & \text{other} \end{cases} \quad (17.43)$$

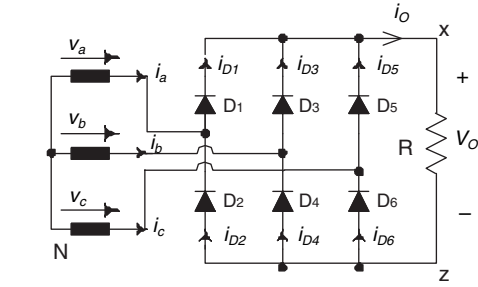
Where V_{in} is the RMS value of the input voltage. The input wave is sinusoidal waveform, the corresponding output is repeating partial sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output is a DC voltage with ripple in the repeating frequency 3ω . After FFT analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only n th ($n = 3k$) harmonics existing.

Where V_{dc} is the DC component of the output voltage, which is the average value, V_n is the n th order harmonic component of the output voltage. The output DC average voltage and current are

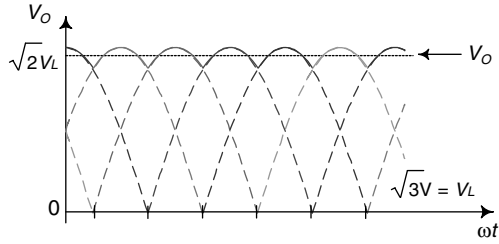
$$V_{O-av} = \frac{3\sqrt{6}}{2\pi} V_{in} = 1.17V_{in} \quad (17.44)$$

17.5 Three-Phase Full-Bridge Diode Rectifier with Resistive Load

A three-phase full-bridge diode rectifier with a purely resistive load is shown in Figure 17.13a, and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 17.13b. The three phase AC suppliers have same RMS value V_{in} with amplitude $\sqrt{2}V_{in}$ and frequency ω , and phase angle shift of 120° each other. The circuit will be analyzed for the



(a) Circuit diagram



(b) Input voltage waveform

FIGURE 17.13

Three-phase full-bridge diode rectifier with a resistor (R).

relationship of the output to input. The AC supply voltage is sinusoidal. Therefore the output voltage and current are sinusoidal half-waveforms

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.34)$$

$$v_O(t) = \sqrt{6}V_{in} \sin \omega t \quad \frac{n\pi}{3} \leq \omega t \leq \frac{(n+1)\pi}{3} \quad (17.45)$$

where $n = 1, 2, 3, \dots$

$$i_{in}(t) = i_O(t) = \frac{\sqrt{6}V_{in}}{R} \sin \omega t \quad \frac{n\pi}{3} \leq \omega t \leq \frac{(n+1)\pi}{3} \quad (17.46)$$

Where V_{in} is the RMS value of the input voltage. The input wave is a sinusoidal waveform, the corresponding output is a repeating partial sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output is a DC voltage with ripple in the repeating frequency 6ω . After FFT analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only n th ($n = 6k$) harmonics existing. The parameter ripple factor RF is defined

$$RF = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{\sum_{n=1}^{\infty} V_n^2}}{V_{dc}} = 0.054 \quad (17.47)$$

where V_{dc} is the DC component of the output voltage, V_n is the n th order harmonic component of the output voltage.

The input voltage is an AC voltage with distortion in the repeating frequency 6ω . After FFT analysis of the supplying waveform, the harmonic components are shown in the frequency spectrum. From the spectrum, there are only n th ($n = 6k \pm 1$) harmonics existing. The parameter total harmonic distortion (THD) is defined

$$THD = \frac{V_{ac}}{V_{fund}} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_{fund}} = 0.046 \quad (17.48)$$

where V_{fund} is the fundamental component of the input voltage, V_n is the n th order harmonic component of the input voltage.

The output DC average voltage and current are

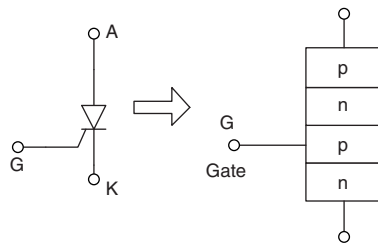
$$V_{O-av} = \frac{3\sqrt{6}}{\pi} V_{in} = 2.34 V_{in} \quad (17.49)$$

$$I_{O-av} = 2.34 \frac{V_{in}}{R} \quad (17.50)$$

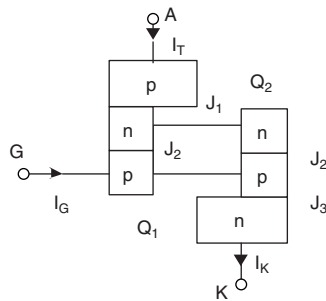
Since the output DC voltage ripple is very small ($RF = 0.054$), the EMF load usually has the condition $E < \sqrt{6} V_{in}$. There is no need to spend time discussing this case.

17.6 Thyristor Rectifiers

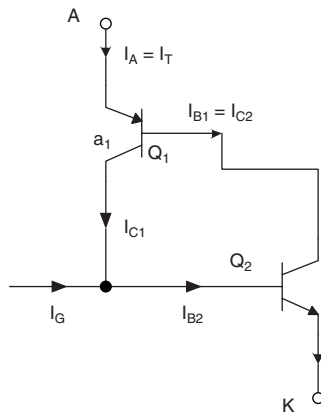
A thyristor is a silicon-controlled rectifier (SCR). It is a four-layer p-n-p-n semiconductor device forming three junctions J1-J2-J3, as shown in [Figure 17.14a](#). It has three external electrodes: anode, cathode, and gate. This structure can be considered as a two-type transistor in a cascade connection shown in [Figure 17.14b and c](#). Its characteristics will be discussed in the next section. It is controlled by a firing pulse with shifting firing angle (α). When $\alpha = 0^\circ$ the characteristics of a thyristor is the same as those of a diode.



(a) Thyristor symbol and structure



(b) Combination by two transistors



(c) Equivalent circuit

FIGURE 17.14
Thyristor.

17.6.1 Single-Phase Half-Wave Rectifier with Resistive Load

A single-phase half-wave thyristor rectifier with resistive load is shown in [Figure 17.15](#). The firing angle α can be set in the range:

$$0 < \alpha < \pi$$

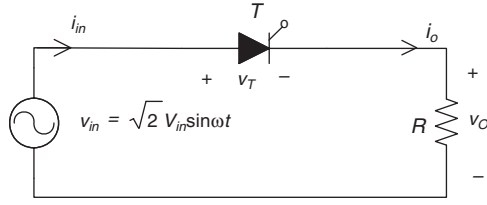


FIGURE 17.15

Single-phase half-wave thyristor rectifier with a resistor (R).

As before, the input voltage is a sinusoidal wave:

$$v_{in}(t) = \sqrt{2} V_{in} \sin \omega t \quad (17.1)$$

The output voltage and current are

$$v_o(t) = \begin{cases} \sqrt{2} V_{in} \sin \omega t & \alpha \leq \omega t \leq \pi \\ 0 & \pi < \omega t < 2\pi + \alpha \end{cases} \quad (17.51)$$

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{\sqrt{2} V_{in}}{R} \sin \omega t & \alpha \leq \omega t \leq \pi \\ 0 & \pi < \omega t < 2\pi + \alpha \end{cases} \quad (17.52)$$

Their average values are

$$V_{O-av} = 0.45 V_{in} (1 + \cos \alpha) \quad (17.53)$$

$$I_{O-av} = 0.45 \frac{V_{in}}{R} (1 + \cos \alpha) \quad (17.54)$$

17.6.2 Single-Phase Half-Wave Thyristor Rectifier with Inductive Load

A single-phase half-wave thyristor rectifier with inductive load ($R + L$) is shown in [Figure 17.16](#). The load time constant is $\tau = L/R$. Hence the load impedance Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi \quad (17.55)$$

where

$$\phi = \tan^{-1} \frac{\omega L}{R}$$

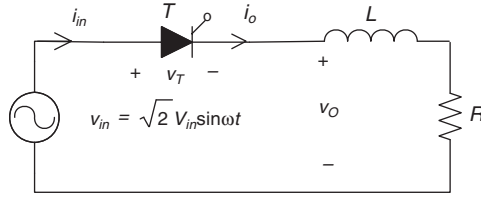


FIGURE 17.16

Single-phase half-wave thyristor rectifier with inductive load ($R + L$).

The output voltage and current are

$$v_O(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq \beta \\ 0 & \beta < \omega t < 2\pi + \alpha \end{cases} \quad (17.56)$$

$$i_{in}(t) = i_O(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{|Z|} \sin(\omega t - \phi) + \sin(\alpha - \phi)e^{-\frac{(\beta - \alpha)/\omega}{L/R}} & \alpha \leq \omega t \leq \beta \\ 0 & \beta < \omega t < 2\pi + \alpha \end{cases} \quad (17.57)$$

where β is the extinction angle and is determined by

$$\sin(\beta - \phi) = \sin(\alpha - \phi)e^{-\frac{\beta - \alpha}{\omega\tau}} \quad (17.58)$$

Their average values are

$$V_{O-av} = 0.45V_{in}(\cos \alpha - \cos \beta) \quad (17.59)$$

$$I_{O-av} = 0.45 \frac{V_{in}}{R}(\cos \alpha - \cos \beta) \quad (17.60)$$

17.6.3 Single-Phase Half-Wave Thyristor Rectifier with Pure Inductive Load

A single-phase half-wave thyristor rectifier with pure inductive load (L) is shown in [Figure 17.17](#). The load is an inductor L only. Therefore,

$$Z = j\omega L = \omega L \angle \phi \quad (17.61)$$

where

$$\phi = \frac{\pi}{2}$$

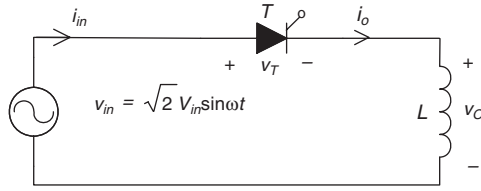


FIGURE 17.17

Single-phase half-wave thyristor rectifier with pure inductive load (L).

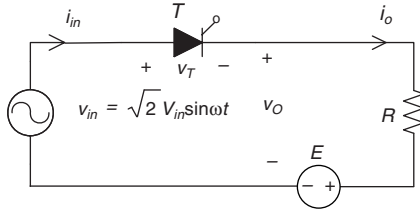


FIGURE 17.18

Single-phase half wave thyristor rectifier with EMF plus resistor ($R + EMF$).

The output voltage and current are

$$v_O(t) = \begin{cases} \sqrt{2} V_{in} \sin \omega t & \alpha \leq \omega t \leq 2\pi - \alpha \\ 0 & 2\pi - \alpha < \omega t < 2\pi + \alpha \end{cases} \quad (17.62)$$

$$i_{in}(t) = i_O(t) = \begin{cases} \frac{\sqrt{2} V_{in}}{|Z|} (\cos \alpha - \cos \omega t) & \alpha \leq \omega t \leq 2\pi - \alpha \\ 0 & 2\pi - \alpha < \omega t < 2\pi + \alpha \end{cases} \quad (17.63)$$

Their average values are

$$V_{O-av} = 0 \quad (17.64)$$

$$I_{O-av} = \frac{\sqrt{2} V_{in}}{\omega L \pi} [(\pi - \alpha) + \sin \alpha] \quad (17.65)$$

17.6.4 Single-Phase Half-Wave Rectifier with Back EMF Plus Resistive Load

A single-phase half wave thyristor rectifier with an EMF plus resistor load (a resistor R plus an EMF) is shown in Figure 17.18. The EMF value is E ,

which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m :

$$m = E/\sqrt{2}V_{in} < 1$$

and

$$\eta = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input voltage is
$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

The thyristor conduction condition requires firing angle $\alpha \geq \eta$. Hence, output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\pi - \eta) \\ E & (\pi - \eta) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.66)$$

The input wave is a sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle. The output DC average voltage is

$$V_{O-av} = \frac{\sqrt{2}V_{in}}{2\pi} (\cos \eta + \cos \alpha) + \frac{E}{2\pi} (\alpha + \pi + \eta) > E \quad (17.67)$$

The input and output current waveform is no longer a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R} (\sqrt{2}V_{in} \sin \omega t - E) & \alpha \leq \omega t \leq (\pi - \eta) \\ 0 & (\pi - \eta) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.68)$$

The input and output current average value is

$$I_{O-av} = \frac{\sqrt{2}V_{in}}{2\pi R} [\cos \eta + \cos \alpha - m(\pi - \eta - \alpha)] \quad (17.69)$$

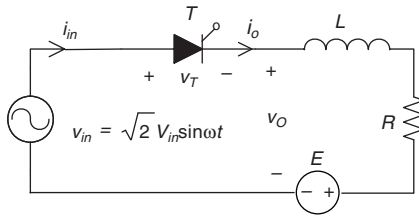


FIGURE 17.19

Single-phase half wave thyristor rectifier with EMF plus resistor and inductor ($EMF + R + L$).

17.6.5 Single-Phase Half-Wave Rectifier with Back EMF Plus Inductive Load

A single-phase half wave thyristor rectifier with an EMF plus inductive load (an EMF plus a resistor R and an inductor L) is shown in Figure 17.19. The EMF value is E , which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m :

$$m = E / \sqrt{2}V_{in} < 1$$

and

$$\eta = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

As before, the load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{\omega L}{R}$$

the load time constant $\tau = L/R$.

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input voltage is (17.1)

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t$$

Since the inductor causes the current continuity, the thyristor conduction angular length is γ , in which usually $\alpha + \gamma \geq \pi$. The thyristor conduction condition requires firing angle $\alpha \geq \eta$. Hence, output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\alpha + \gamma) \\ E & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.70)$$

Where γ is determined by:

$$e^{-\frac{\gamma}{\omega L/R}} = \frac{\frac{m}{\cos \phi} - \sin(\alpha + \gamma - \phi)}{\frac{m}{\cos \phi} - \sin(\alpha - \phi)} \quad (17.71)$$

The input wave is sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle. The output DC average voltage is

$$V_{O-av} = E \quad (17.72)$$

The input and output current waveform is no longer a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \begin{cases} \left(\frac{\sqrt{2}V_{in}}{|Z|} [\sin(\omega t - \phi) - \{\frac{m}{\cos \phi} - [\frac{m}{\cos \phi} - \sin(\alpha - \phi)]e^{-\frac{\gamma}{\omega L/R}}\}] \right) & \alpha \leq \omega t \leq (\alpha + \gamma) \\ 0 & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.73)$$

The input and output current average value is

$$I_{O-av} = \frac{\sqrt{2}V_{in}}{2\pi R} [\cos \alpha - \cos(\alpha + \gamma) - m\gamma] \quad (17.74)$$

17.6.6 Single-Phase Half-Wave Rectifier with Back EMF Plus Pure Inductor

A single-phase half wave thyristor rectifier with an EMF plus a pure inductor L is shown in [Figure 17.20](#). The EMF value is E , which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m :

$$m = E/\sqrt{2}V_{in} < 1$$

and

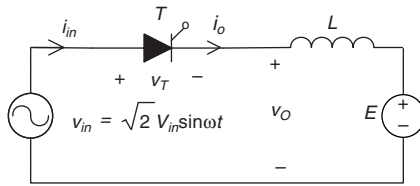


FIGURE 17.20

Single-phase half wave thyristor rectifier with EMF plus inductor ($EMF + L$).

$$\eta = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2} V_{in}}$$

The load Z is

$$Z = j\omega L = \omega L \angle \phi$$

where

$$\phi = \frac{\pi}{2}$$

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input voltage is
$$v_{in}(t) = \sqrt{2} V_{in} \sin \omega t \quad (17.1)$$

Since the inductor causes the current continuity, the thyristor conduction angular length is γ , which is usually $\alpha + \gamma \geq \pi$. The thyristor conduction condition requires firing angle $\alpha \geq \eta$. Hence, output voltage is

$$v_o(t) = \begin{cases} \sqrt{2} V_{in} \sin \omega t & \alpha \leq \omega t \leq (\alpha + \gamma) \\ E & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.75)$$

where γ is determined by:

$$\gamma = \frac{\cos \alpha - \cos(\alpha + \gamma)}{m} \quad (17.76)$$

The input wave is a sinusoidal waveform, the corresponding output is a partial sinusoidal waveform less than half-cycle. The output DC average voltage is

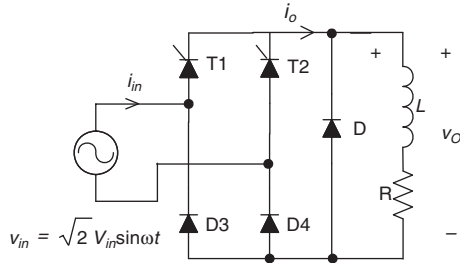


FIGURE 17.21

Single-phase full-wave semicontrolled thyristor rectifier with inductive load ($L + R$) plus a free-wheeling diode D .

$$V_{O-av} = E \quad (17.77)$$

The input and output current waveform is no longer a sinusoidal waveform.

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{\omega L} [\cos \alpha - \cos \omega t - m(\omega t - \alpha)] & \alpha \leq \omega t \leq (\alpha + \gamma) \\ 0 & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \quad (17.78)$$

The input and output current average value is

$$I_{O-av} = \frac{\sqrt{2}V_{in}}{2\pi\omega L} \left[\gamma \cos \alpha + \sin \alpha - \sin(\alpha + \gamma) - \frac{m\gamma^2}{2} + m\alpha\gamma \right] \quad (17.79)$$

17.6.7 Single-Phase Full-Wave Semicontrolled Rectifier with Inductive Load

A single-phase full-wave semicontrolled rectifier with inductive load (an inductor L and a resistor R) plus a free-wheeling diode D , is shown in Figure 17.21. This rectifier is operating in quadrant 1 only because of the free-wheeling diode D . The rectified output waveform is repeating in the frequency 2ω . The load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{\omega L}{R}$$

the load time constant $\tau = L/R$.

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input voltage is
$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

Output voltage is
$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq \pi \\ 0 & \pi < \omega t < (\pi + \alpha) \end{cases} \quad (17.80)$$

The output DC average voltage is

$$V_{O-av} = \frac{\sqrt{2}V_{in}}{\pi} (1 + \cos \alpha) \quad (17.81)$$

If the inductance is large enough and load time constant $\tau = L/R$ is larger than the half-cycle $T/2 = 1/2f$, and the input and output current waveform can be considered constant.

$$i_o(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{(\pi - \alpha)R} (1 + \cos \alpha) & \alpha \leq \omega t \leq \pi \\ 0 & \pi < \omega t < (\pi + \alpha) \end{cases} \quad (17.82)$$

The input and output current average value is

$$I_{O-av} = \frac{\sqrt{2}V_{in}}{\pi R} (1 + \cos \alpha) \quad (17.83)$$

17.6.8 Single-Phase Full-Controlled Rectifier with Inductive Load

A single-phase full-wave semicontrolled thyristor rectifier with inductive load (an inductor L and a resistor R) is shown in [Figure 17.22](#). This rectifier is operating in quadrants I and IV. The rectified output waveform is repeating in the frequency 2ω . If the inductance is large enough, the output current can be constant. The load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{\omega L}{R}$$

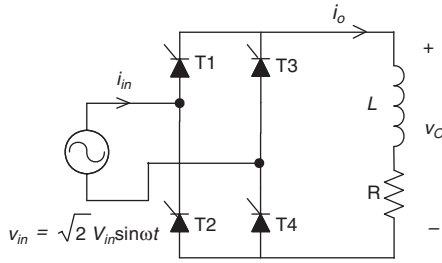


FIGURE 17.22

Single-phase full-wave semicontrolled thyristor rectifier with inductive load ($L + R$).

the load time constant $\tau = L/R \gg T/2 = 1/2f$.

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input voltage is
$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \quad (17.1)$$

Output voltage is
$$v_O(t) = \sqrt{2}V_{in} \sin \omega t \quad \alpha \leq \omega t \leq (\pi + \alpha) \quad (17.84)$$

The output DC average voltage is

$$V_{O-av} = \frac{2\sqrt{2}V_{in}}{\pi} \cos \alpha \quad (17.85)$$

If the inductance is large enough and load time constant $\tau = L/R$ is larger than the half-cycle $T/2 = 1/2f$, the input and output current waveform can be considered constant.

$$i_O(t) = \frac{2\sqrt{2}V_{in}}{\pi R} \cos \alpha \quad (17.86)$$

The input and output current average value is

$$I_{O-av} = \frac{\sqrt{2}V_{in}}{\pi R} (1 + \cos \alpha) \quad (17.87)$$

17.6.9 Three-Phase Half-Wave Rectifier with Resistive Load

A three-phase half-wave thyristor rectifier with a resistor R is shown in [Figure 17.23](#). This rectifier is operating in quadrant I only. The rectified output waveform is repeating in the frequency 3ω . The circuit will be analyzed

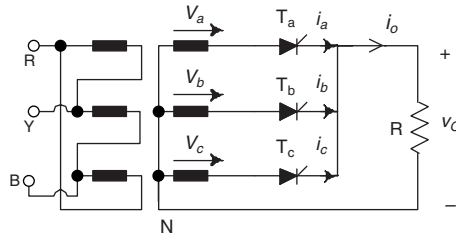


FIGURE 17.23

Three-phase half-wave semicondutor thyristor rectifier with resistor.

for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input line-to-neutral (between phase a to N) voltage is

$$v_{aN}(t) = \sqrt{2}V_{in} \sin(\omega t - \frac{\pi}{6}) \quad (17.88)$$

$$\text{Output voltage is } v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq \frac{2\pi}{3} \\ 0 & \omega t > \frac{2\pi}{3} \end{cases} \quad (17.89)$$

The firing angle α starts from the phase cross point $\omega t = 30^\circ$. Each thyristor's maximum conduction period is 120° . Possible firing angle range is

$$0 \leq \alpha \leq 150^\circ$$

The output DC average voltage is

$$V_{O-av} = \begin{cases} \frac{3\sqrt{6}V_{in} \cos \alpha}{2\pi} & \alpha \leq \frac{\pi}{6} \\ \sqrt{6}V_{in} \sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi} \cos 2\alpha} & \alpha > \frac{\pi}{6} \end{cases} \quad (17.90)$$

The output current waveform is a partial sinusoidal wave.

$$v_o(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{R} \sin \omega t & \alpha \leq \omega t \leq \frac{2\pi}{3} \\ 0 & \omega t > \frac{2\pi}{3} \end{cases} \quad (17.91)$$

The output current average value is

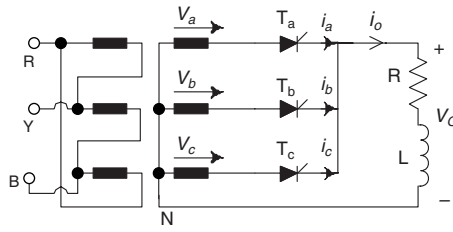


FIGURE 17.24

Three-phase half-wave semicontrolled thyristor rectifier with inductive load ($L + R$).

$$V_{O-av} = \begin{cases} \frac{3\sqrt{6}V_{in} \cos \alpha}{2\pi R} & \alpha \leq \frac{\pi}{6} \\ \frac{\sqrt{6}V_{in}}{R} \sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi} \cos 2\alpha} & \alpha > \frac{\pi}{6} \end{cases} \quad (17.92)$$

17.6.10 Three-Phase Half-Wave Thyristor Rectifier with Inductive Load

A three-phase half-wave thyristor rectifier with inductive load (an inductor L and a resistor R) is shown in Figure 17.24. This rectifier is operating in quadrants I and IV. The rectified output waveform is repeating in the frequency 3ω . If the inductance is large enough, the output current can be constant. The load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{\omega L}{R}$$

the load time constant $\tau = L/R \gg T/3 = 1/3f$.

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input line-to-neutral (between phase a to N) voltage is

$$v_{aN}(t) = \sqrt{2}V_{in} \sin(\omega t - \frac{\pi}{6}) \quad (17.88)$$

$$\text{Output voltage is } v_O(t) = \sqrt{2}V_{in} \sin \omega t \quad \alpha \leq \omega t \leq (\frac{2\pi}{3} + \alpha) \quad (17.93)$$

The firing angle α starts from the phase cross point $\omega t = 30^\circ$. Possible firing angle range is

$$0 \leq \alpha \leq 180^\circ$$

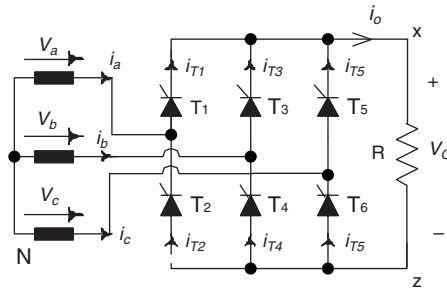


FIGURE 17.25
Three-phase full-wave thyristor rectifier with resister R .

The output DC average voltage is

$$V_{O-av} = \frac{3\sqrt{6}V_{in}}{2\pi} \cos \alpha \quad (17.94)$$

If the inductance is large enough and load time constant $\tau = L/R$ is larger than the half-cycle $T/2 = 1/2f$, the output current waveform can be considered constant.

$$i_O(t) = \frac{3\sqrt{6}V_{in}}{2\pi R} \cos \alpha \quad (17.95)$$

The output current average value is

$$I_{O-av} = \frac{3\sqrt{6}V_{in}}{2\pi R} \cos \alpha \quad (17.96)$$

17.6.11 Three-Phase Full-Wave Thyristor Rectifier with Resistive Load

A three-phase full-wave thyristor rectifier with a resister R is shown in Figure 17.25. This rectifier is operating in quadrant I only. The rectified output waveform is repeating in the frequency 6ω . The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input line-to-line (between phase a to c) voltage is

$$v_{ac}(t) = \sqrt{6}V_{in} \sin(\omega t - \frac{\pi}{6}) \quad (17.88)$$

$$\text{Output voltage is } v_O(t) = \begin{cases} \sqrt{6}V_{in} \sin \omega t & \alpha \leq \omega t \leq \frac{2\pi}{3} \\ 0 & \omega t > \frac{2\pi}{3} \end{cases} \quad (17.97)$$

The firing angle α starts from the phase cross point $\omega t = 30^\circ$. Each thyristor maximum conduction period is 120° . Possible firing angle range is

$$0 \leq \alpha \leq 150^\circ$$

The output DC average voltage is

$$V_{O-av} = \begin{cases} \frac{3\sqrt{6}V_{in} \cos \alpha}{\pi} & \alpha \leq \frac{\pi}{6} \\ 2\sqrt{6}V_{in} \sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi} \cos 2\alpha} & \alpha > \frac{\pi}{6} \end{cases} \quad (17.98)$$

The output current waveform is a partial sinusoidal wave.

$$v_o(t) = \begin{cases} \frac{\sqrt{6}V_{in}}{R} \sin \omega t & \alpha \leq \omega t \leq \frac{2\pi}{3} \\ 0 & \omega t > \frac{2\pi}{3} \end{cases} \quad (17.99)$$

The output current average value is

$$I_{O-av} = \begin{cases} \frac{3\sqrt{6}V_{in} \cos \alpha}{2\pi R} & \alpha \leq \frac{\pi}{6} \\ \frac{\sqrt{6}V_{in}}{R} \sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi} \cos 2\alpha} & \alpha > \frac{\pi}{6} \end{cases} \quad (17.100)$$

17.6.12 Three-Phase Full-Wave Thyristor Rectifier with Inductive Load

A three-phase full-wave thyristor rectifier with inductive load (an inductor L and a resistor R) is shown in [Figure 17.26](#). This rectifier is operating in quadrants I and II. The rectified output waveform is repeating in the frequency 6ω . If the inductance is large enough, the output current can be constant. The load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2} \angle \phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{\omega L}{R}$$

the load time constant $\tau = L/R \gg T/3 = 1/3f$

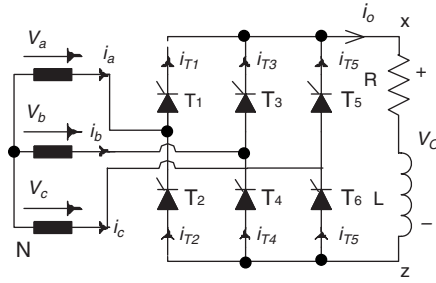


FIGURE 17.26

Three-phase full-wave thyristor rectifier with inductive load ($L + R$).

The circuit will be analyzed for the relationship of the output to input. The AC supply voltage is sinusoidal.

Input line-to-line (between phase a to c) voltage is

$$v_{ac}(t) = \sqrt{6}V_{in} \sin(\omega t - \frac{\pi}{6}) \quad (17.88)$$

$$\text{Output voltage is } v_o(t) = \sqrt{6}V_{in} \sin \omega t \quad \alpha \leq \omega t \leq (\frac{2\pi}{3} + \alpha) \quad (17.101)$$

The firing angle α starts from the phase cross point $\omega t = 30^\circ$. Possible firing angle range is

$$0 \leq \alpha \leq 180^\circ$$

The output DC average voltage is

$$V_{O-av} = \frac{3\sqrt{6}V_{in}}{\pi} \cos \alpha \quad (17.102)$$

If the inductance is large enough and load time constant $\tau = L/R$ is large than the half-cycle $T/6 = 1/6f$, the output current waveform can be considered constant.

$$i_o(t) = \frac{3\sqrt{6}V_{in}}{\pi R} \cos \alpha \quad (17.103)$$

The output current average value is

$$I_{O-av} = \frac{3\sqrt{6}V_{in}}{\pi R} \cos \alpha \quad (17.104)$$

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Control Circuit: EMI and Application Examples of DC/DC Converters

18.1 Introduction

During investigation of DC/DC prototypes and their characteristics, much attention is paid to the circuitry components of the converters. Actually, control components as auxiliary apparatus are important roles for DC/DC converter operation. For example, the PWM pulse train generator is used to yield the switching signal to all switches of DC/DC converters.

EMI, EMS, and EMC have to be considered during DC/DC converter design because they affect the converter and other equipment working operation heavily.

Some particular examples of DC/DC converters are presented in this chapter to demonstrate DC/DC converter application.

18.2 Luo-Resonator

The Luo-resonator is a pulse-width-modulated (PWM) generator, which produces the PWM pulse train switching signal used for DC/DC converters. This resonator consists of only three *operational amplifiers* (OA), and provides a pulse train of the switching signal to control static switch-on or switch-off with adjustable frequency f and conduction duty k . Luo-resonator can be re-integrated into an application specific integrated circuit (ASIC) to produce portable DC/DC converters.

The Luo-resonator is a high efficiency and simple circuit with easily adjusting frequency f and conduction duty k . Its circuit diagram is shown in [Figure 18.1](#). It consists of three OAs named OA1 to 3 and auxiliary. These three 741-type OAs are integrated in a chip TL074 (which contains four OAs). Two potentiometers are applied to adjust the frequency f and conduction duty k .

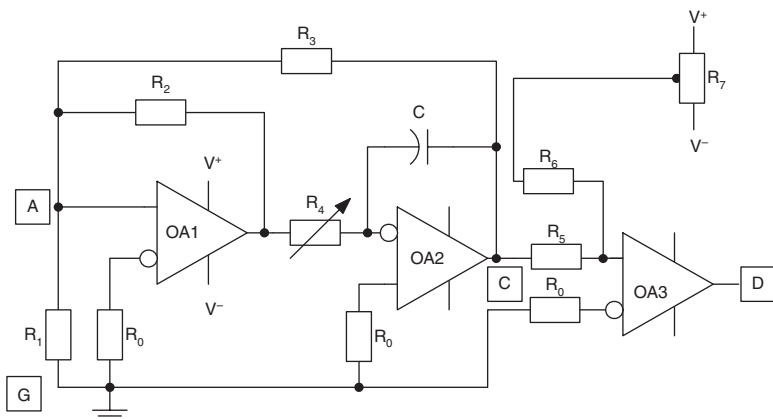


FIGURE 18.1
Luo-resonator.

The analysis of the Luo-resonator is performed under the assumption that the operational amplifier is ideal:

1. Its open-loop gain is infinity
2. Its input impedance is infinity and output impedance is zero
3. Its output voltage positive and negative maximum values are equal to the power supply voltages

18.2.1 Circuit Explanation

Type-741 OA can work with a ± 3 to ± 18 V power supplies, which are marked V_+ , G , and V_- with $|V_-| = V_+$. OA2 in Figure 18.1 acts as the integration operation, its output V_C is a triangle waveform with regulated frequency $f = 1/T$ controlled by potentiometer R_4 . OA1 acts as a resonant operation, its output V_B is a square-waveform with the frequency f . OA3 acts as a comparator, its output V_D is a square-waveform pulse train with regulated conduction duty k controlled by R_7 .

First, the output voltage of OA1 maintained as $V_B = V_+$. In the meantime V_B inputs to OA2 via R_4 . Because of the capacitor C , the output voltage V_C of OA2 decreases toward V_- with the slope $-1/R_4C$. Voltage V_C feeds back to OA1 negatively via R_3 . Voltage V_A at point A changes from $(2mV_+)/ (1 + m)$ downward to 0 in the period of $0 - 2mR_4C$. It then intends toward negative. It causes the OA1's output voltage $V_B = V_-$ at $t = 2mR_4C$ and voltage V_A jumps to

$$\frac{2mV_-}{1 + m} \quad (18.1)$$

Therefore, the output voltage of OA1 jumps to $V_B = V_-$. In the meantime V_B inputs to OA2 via R_4 . Because of the capacitor C , the output voltage V_C of OA2 increases toward V_+ with the slope $1/R_4C$. Voltage V_C feeds back to OA1 negatively via R_3 . Voltage V_A at point A changes from $(2mV_-)/(1 + m)$ upwards to 0 in the period of $2mR_4C - 4mR_4C$. It then intends toward positive. It causes the OA1's output voltage $V_B = V_+$ at $t = 4mR_4C$ and voltage V_A jumps to

$$\frac{2mV_+}{1 + m} \quad (18.2)$$

Voltage V_B takes the two values either V_+ or V_- .

Voltage V_C is a triangle waveform, and inputs to OA3. It compares with shift signal $V_{\text{off-set}}$ regulated by the potentiometer R_7 via R_6 . When $V_{\text{off-set}} = 0$, OA3 yields its output voltage V_D as a pulse train with conduction duty $k = 0.5$. Positive $V_{\text{off-set}}$ shifts the zero-cross point of voltage V_C downward, hence, OA3 yields its output voltage V_D as a pulse train with conduction duty $k > 0.5$. Vice versa, negative $V_{\text{off-set}}$ shifts the zero-cross point of voltage V_C upward, hence, OA3 yields its output voltage V_D as a pulse train with conduction duty $k < 0.5$ as shown in [Figure 18.2](#). Conduction duty k is controlled by $V_{\text{off-set}}$ via the potentiometer R_7 .

18.2.2 Calculation Formulae

The calculation formulas are
Setting,

$$m = \frac{R_3}{R_2} \quad (18.3)$$

We obtain:

$$f = \frac{1}{T} = \frac{1}{4mR_4C} \quad (18.4)$$

and

$$k = 0.5 + \frac{R_5 V_{\text{off-set}}}{2R_6 V_+} \quad (18.5)$$

If the positive and negative maximum values of the shift voltage $V_{\text{off-set}}$ are V_+ and V_- , and $R_5 = R_6$, the value of the conduction duty k is in the range between 0 and 1.0. Considering the resistance tolerance is 5%, we usually choose that resistance R_6 is slightly smaller than resistance R_5 .

This PWM pulse train V_D is applied to the DC/DC converter switch such as a transistor, MOSFET or IGBT via a coupling circuit. The voltage waveforms of $V_A - V_D$ are shown in [Figure 18.2](#).

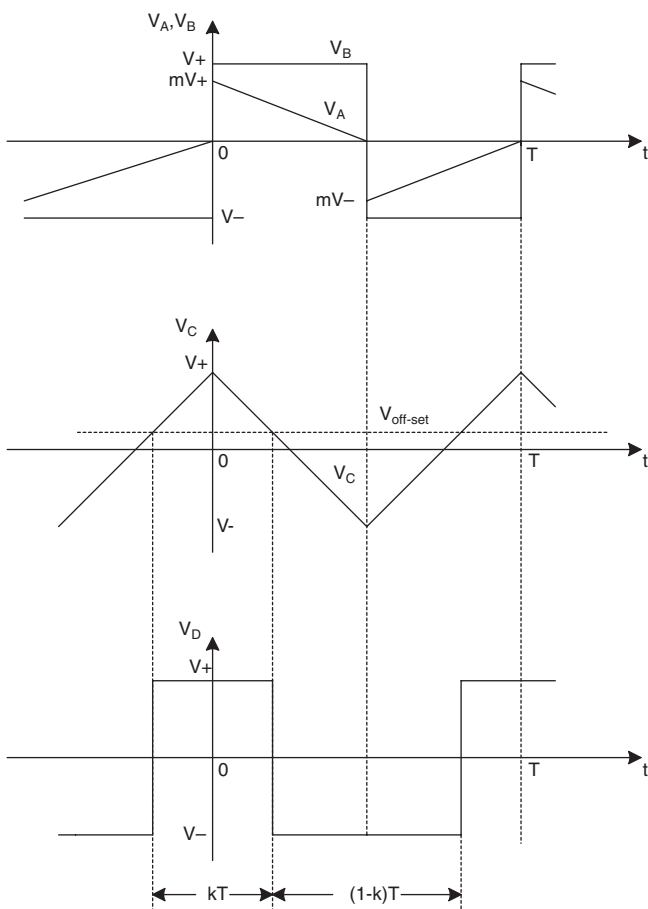


FIGURE 18.2

Voltage waveforms of Luo-resonator.

18.2.3 A Design Example

A Luo-resonator was designed as shown in Figure 18.2 with the component values:

$$R_0 = 10 \text{ k}\Omega; R_1 = R_2 = R_5 = 100 \text{ k}\Omega; R_3 = R_6 = 95 \text{ k}\Omega; \\ R_4 = 510 \text{ }\Omega \text{ to } 5.1 \text{ k}\Omega; R_7 = 20 \text{ k}\Omega \text{ and } C = 5.1 \text{ nF}$$

The results are $m = 0.95$, frequency $f = 10 \text{ kHz}$ to 100 kHz and conduction duty $k = 0$ to 1.0 .

18.2.4 Discussion

Type 741 operational amplifier of chip TL074 has the frequency bandwidth of about 2 MHz . Its open-loop gain is only about 20 when this Luo-resonator

works at $f = 100$ kHz. The waveform of V_c may be deformed slightly. It increases or decreases as an exponential curve, but linearly. However, the frequency f and conduction duty k of the output PWM pulse train are still adjustable.

Although real maximum positive and negative output voltages of all OA are slightly smaller than the power supply voltages V_+ and V_- , experimental results verified that Luo-resonator still works well. When power supply voltages change from ± 5 V to ± 18 V the variations of the frequency f and conduction duty k are less than 2%.

18.3 EMI, EMS and EMC

Electromagnetic interference (EMI) generally exists in all electrical and electronic equipment, especially in all DC/DC converters. Since the switching frequency applied in DC/DC converter is high it causes significant EMI if carelessly designed. For the sake of providing the power quality, two objectives must be achieved. First, limit the high frequency (HF) emissions that can be imposed on the power mains. Second, elaborate the current electromagnetic susceptibility (EMS) test methods with the goal of reducing the EMS of devices on the consumer end of the power grid.

Electromagnetic compatibility (EMC) has come a long way from the “black magic” approach in the early 1960s to an almost exact science today with its analytical methods, measurement techniques, and simulation software. Four decades ago, all existing handbooks on EMC could be counted on the fingers of one hand, but today they could occupy several shelves in a respectable library. This fact is caused by the significant reason that the applied frequency in 200 kHz to 5 MHz is much higher than those (5 kHz to 100 kHz) of 40 years ago. EMI is a serious problem in power electronic circuits because of their fast switching characteristics. Many countries have imposed EMC regulations that must be met before electronic products can be sold legally. Because of this fact, the vital importance of this problem in all equipment including DC/DC converters is recognized.

18.3.1 EMI/EMC Analysis

The recent investigation of international regulations on EMC has prompted active research in the study of EMI emission from switched-mode power converters, which are now indispensable components in modern electronic equipment such as computers. EMI study can be focused on three major elements, namely,

1. The EMI source (EMI emission)
2. The coupling path (EMI transmission)
3. The victim (EMI effect)

It is important to minimize the coupling path and to improve the EMI immunity. An effective solution for EMI suppression is to attack the problem at the EMI source. By studying power electronics circuits, the high dv/dt and di/dt involved in the switching operation of traditional hard-switched power electronics devices are the major source of **EMI emission**. Effectively reducing dv/dt and di/dt in DC/DC converters will largely attenuate the EMI emission in radio frequency (RF) radiation.

In order to improve the energy efficiency and reliability of power converters soft-switching techniques created in 1980s have been proposed to reduce

- The switching power losses across the power devices,
- The switching stress of switched-mode power electronics circuits.

Essentially, soft-switching techniques create a zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) conversion process for the power switched to turn-on and turn-off. Therefore, the instantaneous power losses across the main switches can be reduced or eliminated. Results published recently have confirmed the feasibility of such soft-switched operation.

Coupling path is a complex problem. EMI emission is created by the EMI source and radiated out by certain manner, then EMI reaches the receiver or victim. The EMI transferring process from the source to victim is called coupling path. It relies on the following factors

- The physical structure in both EMI source and victim
- The location and direction between EMI source and victim
- The transmission media (shielded or unshielded) between EMI source and victim
- The difference of the frequency bandwidths between EMI source and victim

Successfully cut, the coupling path can effectively reduce the EMI to other equipment (victim). Unfortunately, no matter how carefully it is done, EMI still affects all victims.

Victim is the equipment to be harmed by the EMI. In order to reduce the interference some effective measures can be taken

- Neat physical structure
- Distance from source
- Shielding equipment
- Large different frequency band from EMI source

We concentrate to reduce the EMI emission that may be created by DC/DC converters in further sub-sections.

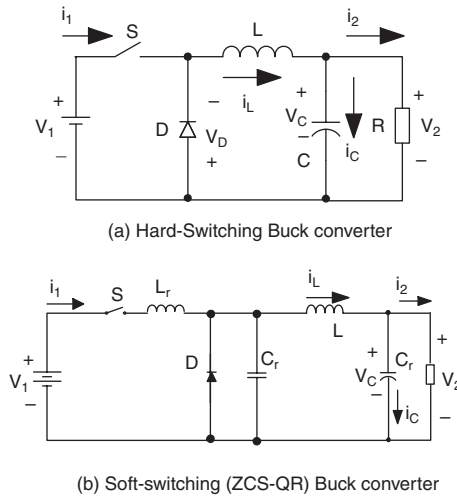


FIGURE 18.3
Hard-switching and soft-switching buck converter.

18.3.2 Comparison with Hard-Switching and Soft-Switching

Hard-switching converters usually have large rates of dv/dt and di/dt . For example, a hard-switching buck converter in Figure 1.23a can be redrawn in Figure 18.3a. Its corresponding soft-switching buck converter is shown in Figure 18.3b. The soft-switching buck converter is similar to its hard-switching circuit, except that it consists of the extra resonant components L_r and C_r . Since the values of the extra resonant components L_r and C_r are usually small, they can be carefully designed in the power devices (switch S and diode D) snubbers. Although a snubber circuit can reduce the EMI, it generally causes additional energy loss. Thus, resonant converters not only produce less EMI, but also exhibit lower energy loss than hard-switching converters with snubber circuit.

The resonant inductor L_r limits the initial current of the main switch S to provide zero-current condition during switch-on. The resonant process can provide another zero-current condition for switch-off operation. The resonant capacitor C_r can discharge through the antiparallel diode of the main switch S (it usually exists in the device), thus clamping the voltage across S to about 1 V for near-zero voltage turn-off of the main switch S .

18.3.3 Measuring Method and Results

An EMC analyzer is usually used to measure the EMI emission conducted and radiated. For example, an EMC analyzer HP 8591EM is widely applied in experiments to measure both conducted and radiated emissions. During

the tests, the detector function was set to the Comité International Spécial des Perturbations Radioélectriques (CISPR) quasi-peak function. With the converter off, the frequency range of interest is swept to survey ambient environmental level. With the converter on, the signals measured are the ambient and the converter emission signals. The actual emission from the converter can be obtained by subtracting the ambient signal from the measured signals.

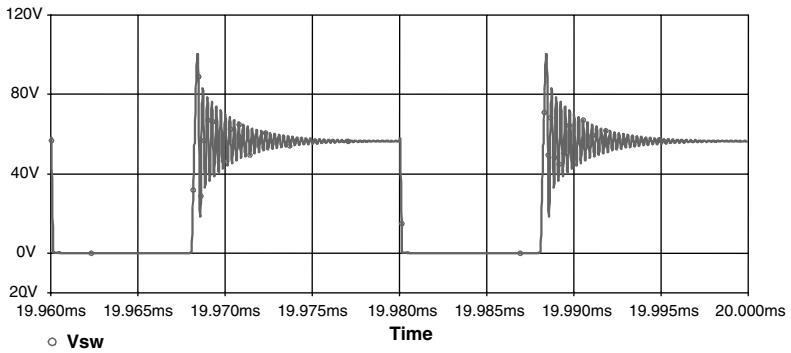
The basic converter components (L and C) in each set of hard-switched and soft-switched converters are identical and the two converters are tested under same load conditions. The magnitude of the inductor current and load current in the two converters of each type are essentially identical. The converters have no EMI filters and are not shielded. In addition, none of the converters has any enclosure. The background EMI was measured just before turning on each converter. Both the conducted EMI (from 50 kHz) and radiated EMI (from 50 kHz to 5 MHz) of the converters were recorded. In the radiated EMI measurement, the results have been corrected with the antenna. All converters were tested with an output power of about 55 W.

For both of the hard-switched and soft-switched buck converters, $V_{in} = 55$ V, $V_o = 20$ V, switching frequency $f = 50$ kHz and duty cycle $k = 0.4$, $L = 2.5$ mH, $C = 20$ μ F and, $R = 7.5$ Ω . For the soft-switched buck converter, $L_r = 4$ μ H and $C_r = 1$ μ F. Figure 18.4 shows the voltage and current waveforms of the main switch S in the hard-switched buck converter. The corresponding current FFT spectrum is shown in Figure 18.5. The switching trajectory in this case is illustrated in Figure 18.6. Figure 18.9 shows the voltage and current waveforms of the main switch S in the soft-switched buck converter. The corresponding current FFT spectrum is shown in Figure 18.8. The switching trajectory in this case is illustrated in Figure 18.9. The L -shape of the trajectory confirms the main switch S in soft-switching state.

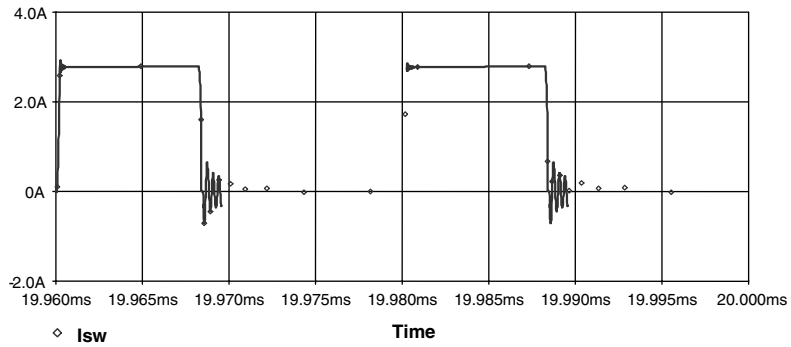
Comparison of Figure 18.4 and Figure 18.7 shows that the soft-switched voltage and current waveforms have very little transient ringing. The reverse recovery current of the diode in the soft-switched converter is also much less than in the hard-switched converter. The significant reduction of the transient ringing in the soft-switched converter results in much reduced dv/dt and di/dt .

Comparison of the FFT spectrums in Figure 18.5 and Figure 18.8 shows that the soft-switched current has much lower total harmonic distortion (THD) than hard-switched current. The FFT spectrum in Figure 18.8 shows the frequency bands are lower than that in Figure 18.5. Otherwise, amplitudes of all harmonics in Figure 18.8 are lower than those in Figure 18.5. From this fact, EMI emission is much lower than that of the corresponding soft-switching converter.

Comparison of the FFT spectrums in Figure 18.6 and Figure 18.9 shows that the switching trajectory shows that the conducted and radiated EMI emission from the hard-switched buck converter (together with the background noise) is larger than that from the soft-switched buck converter. It



(a) Voltage waveform



(b) Current waveform

FIGURE 18.4

Voltage and current waveforms of hard-switching buck converter.

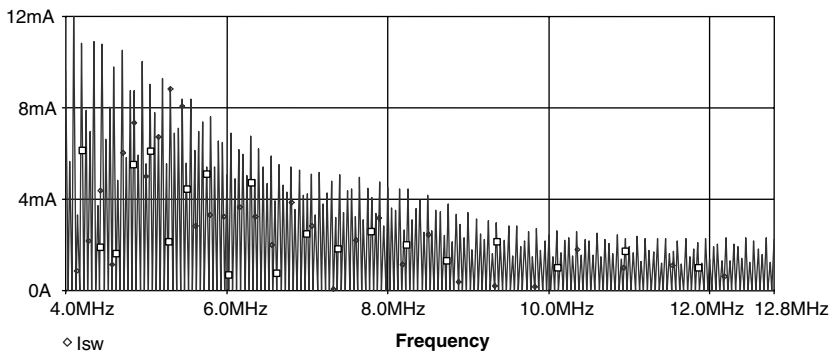


FIGURE 18.5

Current FFT spectrum of hard-switching buck converter.

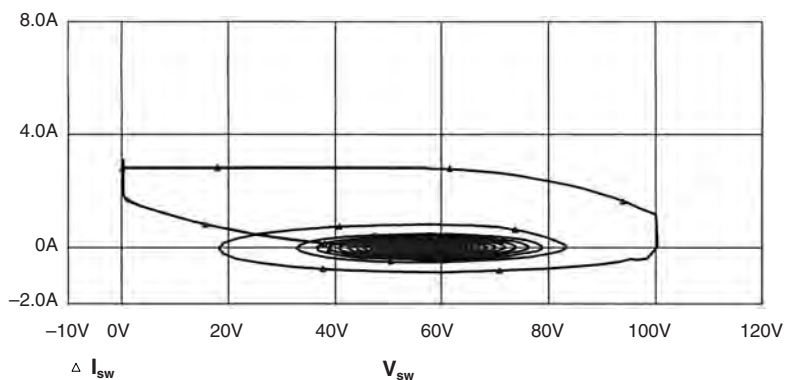
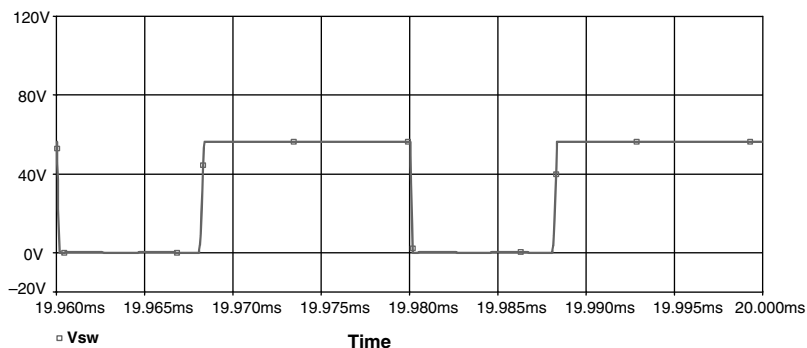
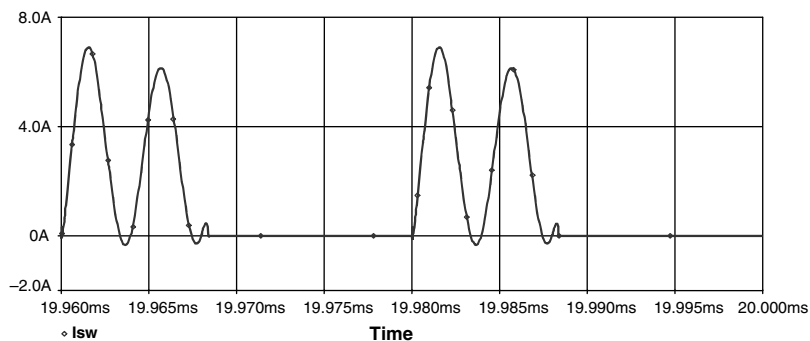


FIGURE 18.6

Switching trajectory of hard-switching buck converter.



(a) Voltage waveform



(b) Current waveform

FIGURE 18.7

Voltage and current waveforms of soft-switching buck converter.

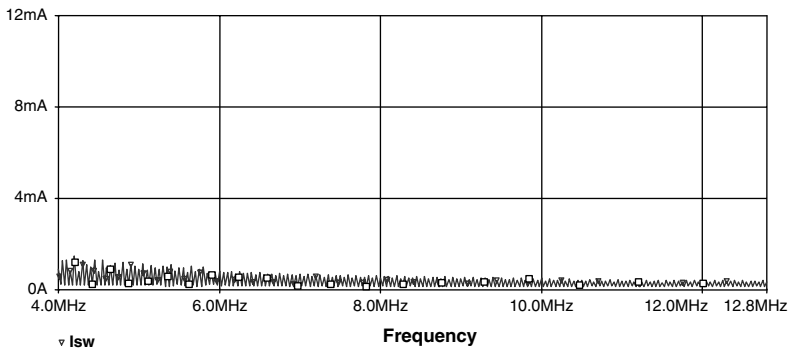


FIGURE 18.8
Current FFT spectrum of soft-switching buck converter.

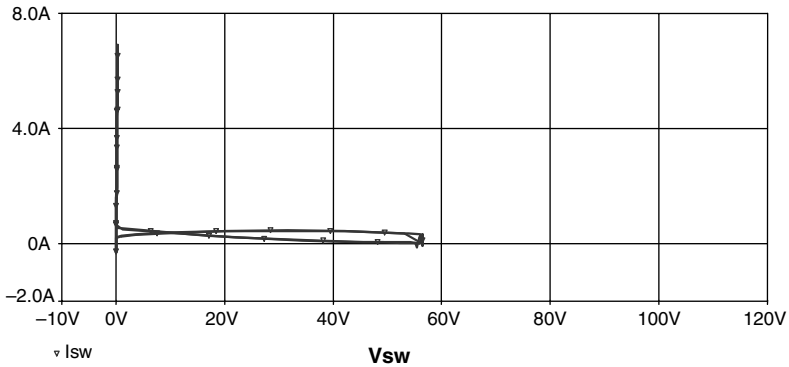


FIGURE 18.9
Switching trajectory of soft-switching buck converter.

can be seen that the soft-switching technique effectively limits the conducted and radiated EMI emission.

18.3.4 Designing Rule to Minimize EMI/EMC

In order to reduce the EMI in certain stage and keep the reasonable EMC, some rules have to be considered during designing a DC/DC converter:

- Take soft-switching techniques ZCS, ZVS, and ZT
- Reduce the switching frequency as low as possible
- Reduce the working power
- Use fewer inductors
- House DC/DC converter in a shielded enclosure

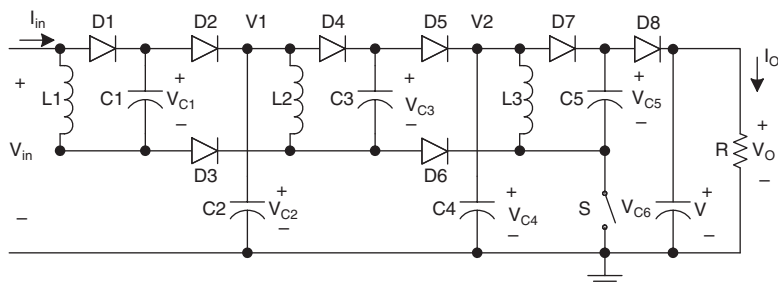


FIGURE 18.10

The 5000 V insulation test bench.

18.4 Some DC/DC Converter Applications

DC/DC conversion technique has been rapidly developed and has been widely applied in industrial applications and communication equipment. Some particular examples of DC/DC converters are presented here to demonstrate DC/DC converter application.

- A 5000 V insulation test bench
- MIT 42 V/14 V 3 kW dual direction DC/DC converter
- IBM 1.8 V/200 A power supply

18.4.1 A 5000 V Insulation Test Bench

Insulation test bench is the necessary equipment for semiconductor manufacturing organizations. An adjustable DC voltage power supply is the heart of this equipment. Traditional method to obtain the adjustable high DC voltage is a diode rectifier via a setting-up transformer. It is costly and large size with poor efficiency.

Using a positive output Luo-converter quadruple-lift circuit plus a general IC-chip TL494, can easily implement the high output voltage (say, 36 V to 1000 V) from a 24 V source, which is shown in Figure 2.57. If higher voltage is required, it is available to implement 192 V to 5184 V, via a positive output super-lift Luo-converter triple-lift circuit, this diagram is shown in Figure 18.10. This circuit is small, effective, and low cost. The output voltage can be determined by

$$V_O = \left(\frac{2-k}{1-k} \right)^3 V_{in} \quad (18.6)$$

TABLE 18.1

The Experimental Results of the 5000 V Test Bench

Conduction duty, k	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.82
Output voltage V_o (V)	192	226	273	244	455	648	1029	1953	5184	6760

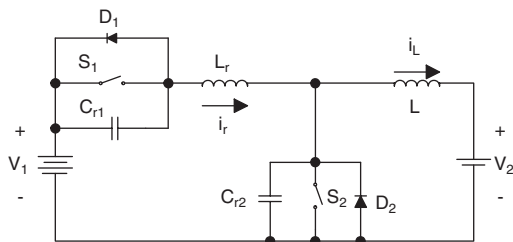


FIGURE 18.11

The MIT 42 V/14 V 3 kW dual direction DC/DC converter.

The conduction duty cycle k is only adjusted in the range 0 to 0.8 to carry out the output voltage in the range of 192 V to 5184 V. The experimental results are listed in Table 18.1. The measured data verified the advantage of this power supply.

18.4.2 MIT 42/14 V 3 KW DC/DC Converter

MIT 42/14 V 3 KW DC/DC converter was required to transfer 3 kW energy between two battery sources with 42 V and 14 V. The circuit diagram is shown in Figure 18.11. This is a two-quadrant zero-voltage-switching (ZVS) quasi-resonant-converter (QRC). The current in low-voltage side can be up to 250 A. This is a typical low-voltage strong-current converter. It is easier to carry out by ZVS-QRC.

This converter consists of two sources V_1 and V_2 , one main inductor L , two main switches S_1 and S_2 , two reverse-paralleled diodes D_1 and D_2 , one resonant inductor L_r and two resonant capacitors C_{r1} and C_{r2} . The working conditions selected:

$$V_1 = 42 \text{ V}$$

$$V_2 = 14 \text{ V}$$

$$L = 470 \text{ } \mu\text{H}$$

$$C_{r1} = C_{r2} = C_r = 1 \text{ } \mu\text{F}$$

$$L_r = \begin{cases} 1 \text{ } \mu\text{H} & \text{normal - operation} \\ 9 \text{ } \mu\text{H} & \text{low - current - operation} \end{cases}$$

Therefore,

$$\omega_O = \frac{1}{\sqrt{L_r C_r}} = 10^6 \text{ rad/s} \quad (18.7)$$

$$Z_O = \sqrt{\frac{L_r}{C_r}} = 1 \quad \Omega \text{ (Normal operation)} \quad (18.8)$$

$$\alpha = \sin^{-1} \frac{V_1}{Z_O I_2} \quad (18.9)$$

It is easy to keep the quasi-resonance when the working current $I_2 > 50 \text{ A}$. If the working current is too low, the resonant inductor will take a large value to guarantee the quasi-resonance state. This converter performs two-quadrant operation:

- Mode A (quadrant I) — Energy transferred from V_1 side to V_2 side
- Mode B (quadrant II) — Energy transferred from V_2 side to V_1 side

Assuming the working current is $I_2 = 100 \text{ A}$ and the converter works in mode A, following calculations are obtained:

$$\omega_O = \frac{1}{\sqrt{L_r C_r}} = 10^6 \text{ rad/s} \quad (18.10)$$

$$Z_O = \sqrt{\frac{L_r}{C_r}} = 1 \quad \Omega \quad (18.11)$$

$$\alpha = \sin^{-1} \frac{V_1}{Z_O I_2} = 24.83^\circ \quad (18.12)$$

$$t_1 = \frac{V_1 C_r}{I_2} = 0.42 \quad \mu\text{s} \quad (18.13)$$

$$t_2 = \frac{\pi + \alpha}{\omega_0} = 3.58 \quad \mu\text{s} \quad (18.14)$$

$$t_3 = \frac{1 + \cos \alpha}{V_1} I_2 L_r = \frac{1 + 0.908}{42} 100 * 10^{-6} = 4.54 \quad \mu\text{s} \quad (18.15)$$

$$t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1} = \frac{0.42 + 3.58 + 4.54}{2} = 4.27 \quad \mu\text{s} \quad (18.16)$$

TABLE 18.2

The Experimental Test Results of MIT 42V/14 Converter

Mode	f (KHz)	I_1 (A)	I_2 (A)	I_L (A)	P_1 (W)	P_2 (W)	η (%)	PD (W/in. ³)
A	78	77.1	220	220	3239	3080	95.1	23.40
A	80	78.3	220	220	3287	3080	93.7	23.58
A	82	81	220	220	3403	3080	90.5	24.01
B	68	220	69.9	220	3080	2939	95.3	22.28
B	70	220	68.3	220	3080	2871	93.2	22.04
B	72	220	66.6	220	3080	2797	90.8	21.77

Note: With the condition: $L_r = 1 \mu\text{H}$, $C_{r1} = C_{r2} = 1 \mu\text{F}$.

$$T = t_1 + t_2 + t_3 + t_4 = 0.42 + 3.58 + 4.54 + 4.27 = 12.81 \mu\text{s} \quad (18.17)$$

$$f = \frac{1}{T} = \frac{1}{12.81} = 78.06 \text{ KHz} \quad (18.18)$$

$$k = \frac{t_3 + t_4}{T} = \frac{4.54 + 4.27}{12.81} = 0.688 \quad (18.19)$$

The volume of this converter is 270 cubic inches. The experimental test results in full power 3 kW are listed in Table 18.2. From the tested data, a high power density 22.85 W/in.³ and a high efficiency 93% are obtained. Because of soft-switching operation, the EMI is low and EMS and EMC are reasonable.

18.4.3 IBM 1.8 V/200 A Power Supply

This equipment is suitable for IBM next-generation computers with power supplies of 1.8 V/200 A. This is a ZCS SR DC/DC Luo-converter, and is shown in [Figure 18.12](#). This converter is based on the double-current synchronous rectifier DC/DC converter plus zero-current-switching technique. It employs a hixaploid-core flat-transformer with the turn ratio $N = 1/12$. It has a six-unit ZCS synchronous rectifier double-current DC/DC converter. The six primary coils are connected in series, and six secondary circuits are connected in parallel. Each unit has particular input voltage V_{in} to be about 33 V, and can offer 1.8 V/35 A individually. Total output current is 210 A. The equivalent primary full current is $I_1 = 17.5$ A and equivalent primary load voltage is $V_2 = 130$ V. The ZCS natural resonant frequency is

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \quad (18.20)$$

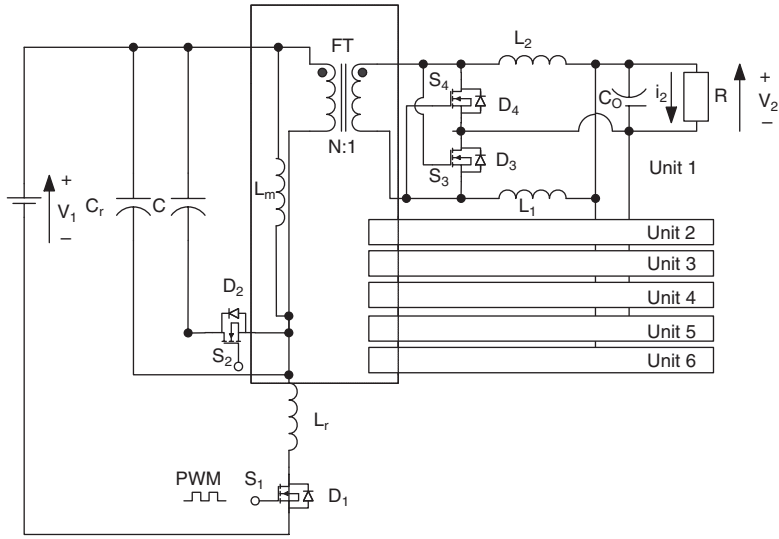


FIGURE 18.12
The IBM 1.8 V/200 A power supply.

$$Z_O = \sqrt{\frac{L_r}{C_r}} \quad (18.21)$$

$$\alpha = \sin^{-1} \frac{Z_O I_1}{V_1} \quad (18.22)$$

The main power supply is from public utility board (PUB) via a diode rectifier. Therefore V_1 is nearly 200 V, and the each unit input voltage V_{in} is about 33 V. Other calculation formulae are

$$t_1 = \frac{I_1 L_r}{V_1} \quad (18.23)$$

$$t_2 = \frac{\pi + \alpha}{\omega_0} \quad (18.24)$$

$$t_3 = \frac{1 + \cos \alpha}{I_1} V_1 C_r \quad (18.25)$$

$$t_4 = \frac{V_1(t_1 + t_2)}{I_1 V_2} \left(I_1 + \frac{V}{Z_0} \frac{\cos \alpha}{\pi / 2 + \alpha} \right) - (t_1 + t_2 + t_3) \quad (18.26)$$

$$T = t_1 + t_2 + t_3 + t_4 \quad (18.27)$$

$$f = \frac{1}{T} \quad (18.28)$$

$$k = \frac{t_1 + t_2}{T} \quad (18.29)$$

Real output voltage and input current are

$$V_O = kNV_1 - (R_L + R_S + \frac{L_m}{T} N^2) I_O \quad (18.30)$$

$$I_{in} = kNI_O \quad (18.31)$$

The power transfer efficiency is

$$\eta = \frac{V_O I_O}{V_{in} I_{in}} = 1 - \frac{R_L + R_S + \frac{L_m}{T} N^2}{kNV_{in}} I_O \quad (18.32)$$

The commercial unit of this power supply works in voltage closed-loop control with inner current closed-loop to keep the output voltage constant. Applying frequency is arranged in the band of 200 kHz to 250 kHz. The volume of the power supply is 14 cubic inches. The transfer efficiency is about 88 to 92% and power density is about 25.7 W/in.³.

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