High Quality Audio J-FET Input Dual Operational Amplifier

■ GENERAL DESCRIPTION

The MUSES8920 is a high quality Audio J-FET input dual operational amplifier. This is a mass production model of MUSES Series. By inheriting MUSES Technology we pursued in the "MUSES series", the MUSES8920 is compatible in high-quality sound and productivity. The MUSES8920 has improved the chip layout and the material, and is developing by thoroughly repeating the listening sound.

The characteristics Low noise (8nV/√Hz), high-SR (25V/μs) and low distortion (0.00004%, Av=1) suitable for audio preamplifiers, active filters, and line amplifiers. In addition, taking advantage of the low input bias current that J-FET has, it is suitable for transimpedance amplifier (I/V converter).

■ PACKAGE OUTLINE

MUSES8920D (DIP8)

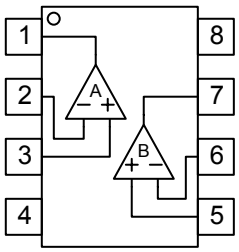
MUSES8920E (EMP8)

■ FEATURES

●Operating Voltage	±3.5V to ±16V
●Low Noise	8nV/√Hz typ.
●THD	0.00004% typ. (Av=1)
●Slew Rate	25V/μs typ.
●Channel Separation	150dB typ.
●High Output Current	100mA typ.(short-circuit current)
●Phase Margin	70 deg typ.
●Input Offset Voltage	0.8mV typ. 5mV max.
●Input Bias Current	5pA typ. 250pA max
●Voltage Gain	135dB typ.
●J-FET technology	
●Package Outline	DIP8, EMP8

■ PIN CONFIGLATION

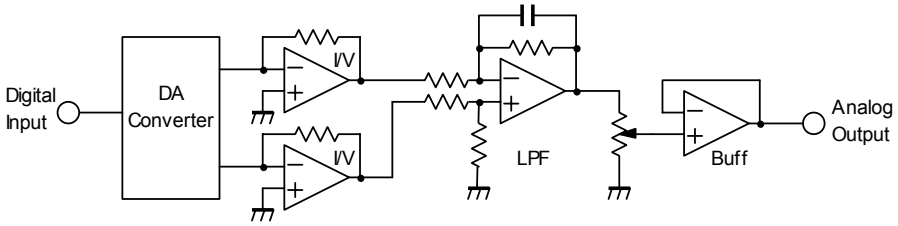
Top View



PIN FUNCTION
1. A OUTPUT
2. A -INPUT
3. A +INPUT
4. V-
5. B +INPUT
6. B -INPUT
7. B OUTPUT
8.V+

■ APPLICATIONS

●Current to Voltage (I/V) Converters
●Hi-end Audio
●Active Filters
●Integrators



DAC Output I/V converter + LPF circuit

■ **ABSOLUTE MAXIMUM RATING** (Ta=25ºC unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	±18	V
Differential Input Voltage Range	V_{ID}	±30(Note1)	V
Common Mode Input Voltage Range	V_{ICM}	±15(Note1)	V
Power Dissipation	P_D	DIP8:870 EMP8:900(Note2)	mW
Operating Temperature Range	Topr	-40~+85	ºC
Storage Temperature Range	Tstg	-50~+150	ºC

(Note1) For supply Voltages less than ±15 V, the maximum input voltage is equal to the Supply Voltage.

(Note2) Mounted on the EIA/JEDEC standard board (114.3×76.2×1.6mm, two layer, FR-4).

(Note3) NJM8920 is ESD (electrostatic discharge) sensitive device.

Therefore, proper ESD precautions are recommended to avoid permanent damage or loss of functionality.

■ **RECOMMENDED OPERATING VOLTAGE** (Ta=25ºC)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+/V^-		±3.5	-	±16	V

■ **ELECTRICAL CHARACTERISTICS**

● **DC CHARACTERISTICS** (V^+/V^-=±15V, Ta=25ºC, Vcm=0V unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Current	Icc	RL=∞, No Signal		-	8	12	mA
Input Offset Voltage	V_{IO}	R_S=50Ω	(Note4)	-	0.8	5	mV
Input Bias Current	I_B		(Note4)	-	5	250	pA
Input Offset Current	I_{IO}		(Note4)	-	2	220	pA
Voltage Gain1	A_{V1}	R_L=10kΩ, Vo=±13V		106	135	-	dB
Voltage Gain2	A_{V2}	R_L=2kΩ, Vo=±12.8V		105	133	-	dB
Voltage Gain3	A_{V3}	R_L=600Ω, Vo=12.5V		105	130	-	dB
Common Mode Rejection Ratio	CMR	V_{ICM}=±12.5V	(Note5)	80	110	-	dB
Supply Voltage Rejection Ratio	SVR	V^+/V^-=±3.5 to ±16V		80	110	-	dB
Maximum Output Voltage1	V_{OM1}	R_L=10kΩ		±13	±14	-	V
Maximum Output Voltage2	V_{OM2}	R_L=2kΩ		±12.8	±13.8	-	V
Maximum Output Voltage3	V_{OM2}	R_L=600Ω		±12.5	±13.5	-	V
Common Mode Input Voltage Range	V_{ICM}	CMR≥80dB		±12.5	±14	-	V

(Note4) Written by absolute ratio.

(Note5) CMR is calculated by specified change in offset voltage. (V_{ICM}=0V to +12.5V, V_{ICM}=0V to -12.5V)

● **AC CHARACTERISTICS** (V^+/V^-=±15V, Ta=25ºC, Vcm=0V unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gain Bandwidth Product	GB	f=10kHz	-	11	-	MHz
Unity Gain Frequency	f_T	A_V=+100, R_S=100Ω, R_L=2kΩ, C_L=10pF	-	10	-	MHz
Phase Margin	Φ_M	A_V=+100, R_S=100Ω, R_L=2kΩ, C_L=10pF	-	70	-	Deg
Equivalent Input Noise Voltage1	V_{NI1}	f=1kHz	-	8	-	nV/√Hz
Equivalent Input Noise Voltage2	V_{NI2}	RIAA, R_S=2.2kΩ, 30kHz, LPF	-	1.1	3.5	μVrms
Total Harmonic Distortion	THD	f=1kHz , A_V=+10, Vo=5Vrms, R_L=2kΩ	-	0.0004	-	%
Channel Separation	CS	f=1kHz , A_V=-100, R_L=2kΩ	-	150	-	dB
Slew Rate	SR	A_V=1, V_{IN}=2Vp-p, R_L=2kΩ, C_L=10pF	-	25	-	V/us

■ Application Notes

●Package Power, Power Dissipation and Output Power

IC is heated by own operation and possibly gets damage when the junction power exceeds the acceptable value called Power Dissipation P_D. The dependence of the MUSES8920 P_D on ambient temperature is shown in Fig 1. The plots are depended on following two points. The first is P_D on ambient temperature 25ºC, which is the maximum power dissipation. The second is 0W, which means that the IC cannot radiate any more. Conforming the maximum junction temperature Tjmax to the storage temperature Tstg derives this point. Fig.1 is drawn by connecting those points and conforming the P_D lower than 25ºC to it on 25ºC. The P_D is shown following formula as a function of the ambient temperature between those points.

$$\text{Dissipation Power} \quad P_D = \frac{Tjmax - Ta}{\theta ja} \text{ [W] (Ta=25ºC to Ta=150ºC)}$$

Where, □ja is heat thermal resistance which depends on parameters such as package material, frame material and so on. Therefore, P_D is different in each package.

While, the actual measurement of dissipation power on MUSES8920 is obtained using following equation.

(Actual Dissipation Power) = (Supply Voltage V_{DD}) X (Supply Current I_{DD}) – (Output Power Po)

The MUSES8920 should be operated in lower than P_D of the actual dissipation power.

To sustain the steady state operation, take account of the Dissipation Power and thermal design.

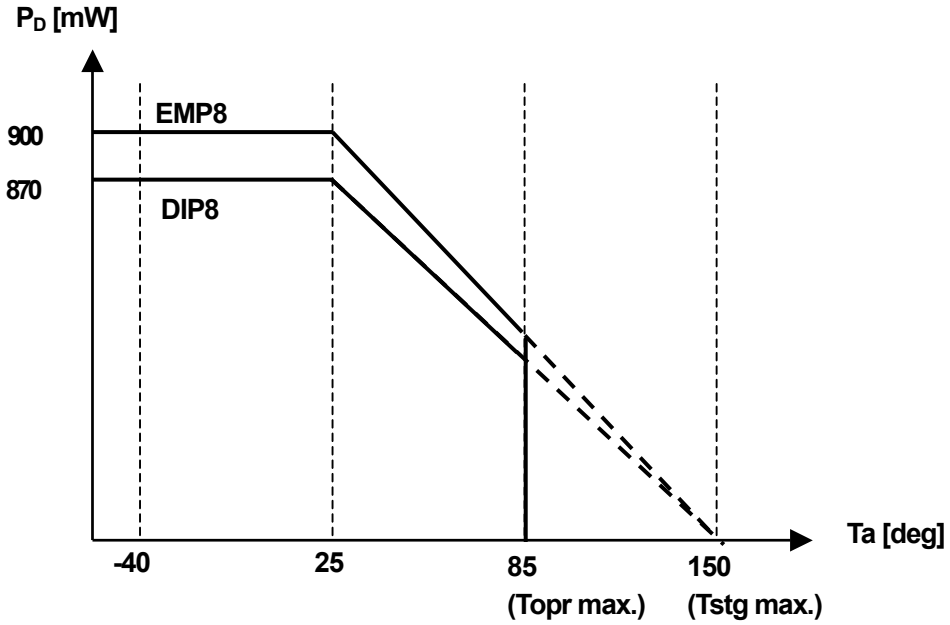
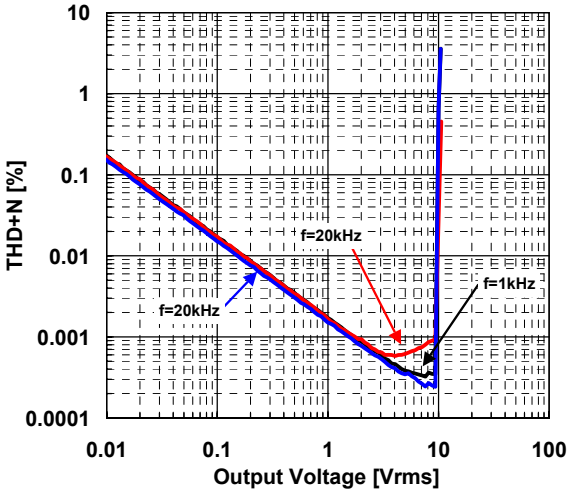


Fig.1 Power Dissipations vs. Ambient Temperature on the MUSE8920

TYPICAL CARACTERISTICS

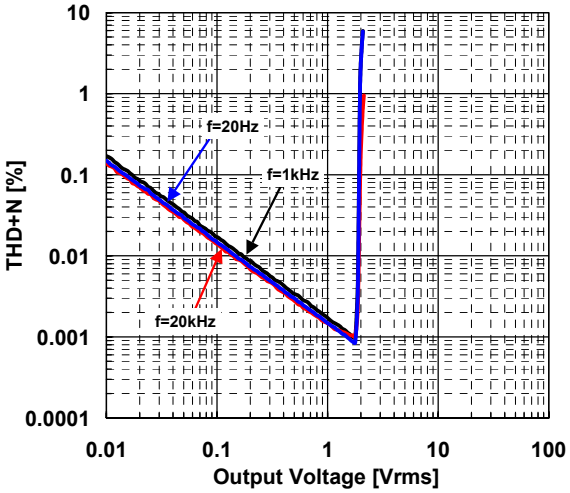
THD+N vs. Output Voltage (Frequency)

V^+/V^-=±15V, A_V=+10, R_L=2k, Ta=25ºC



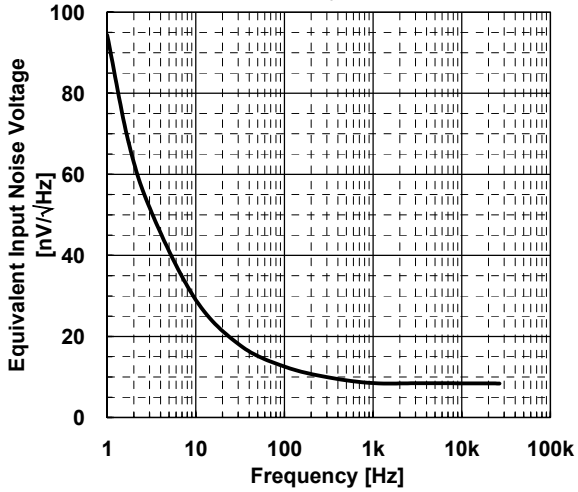
THD+N vs. Output Voltage (Frequency)

V^+/V^-=±3.5V, A_V=+10, R_L=2k, Ta=25ºC



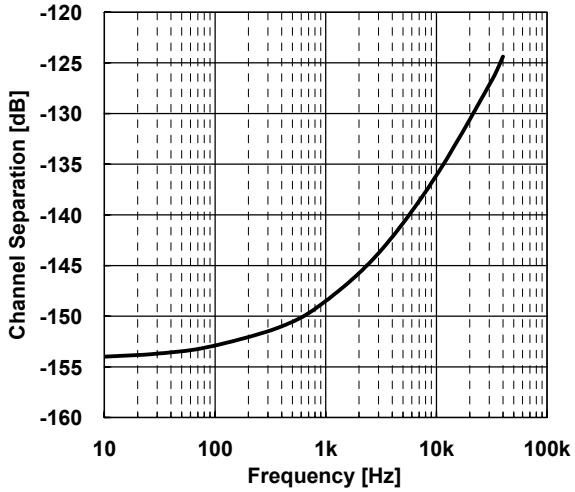
Voltage Noise vs. Frequency

V^+/V^-=±15V, A_V=+100, R_S=100Ω, R_L=∞, Ta=25ºC



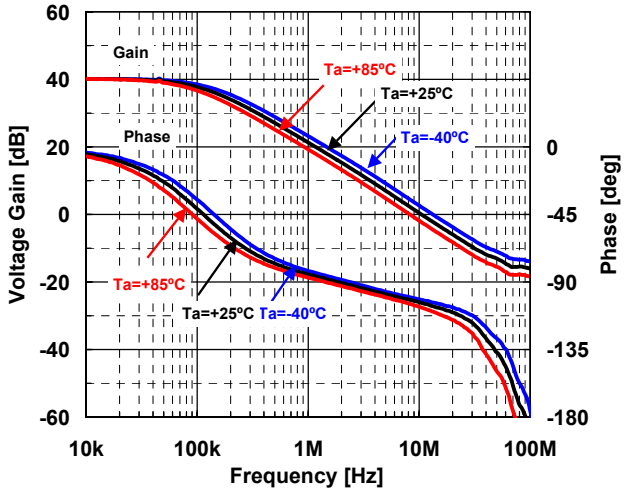
Channel Separation vs. Frequency

V^+/V^-=±15V, A_V=-100, R_L=2kΩ, Ta=25ºC



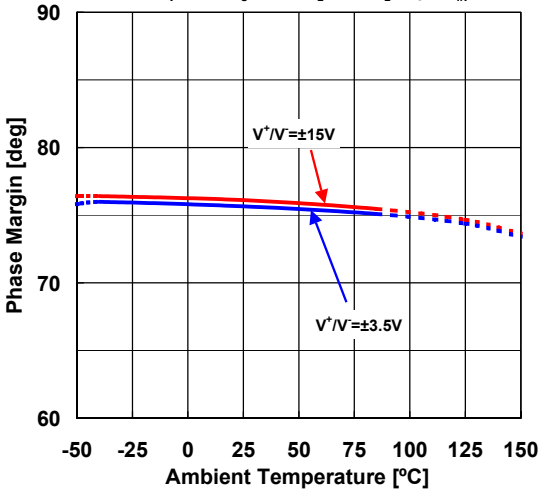
Gain vs. Frequency (Temperature)

V^+/V^-=±15V, A_V=+100, R_L=2kΩ, C_L=10pF



Phase Margin vs. Temperature (Supply Voltage)

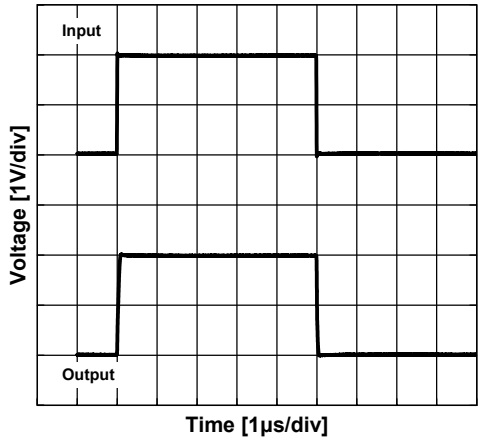
V^+/V^-=±15V, A_V=+100, R_S=100Ω, R_L=2kΩ, C_L=10pF, V_{IN}=-30dBm



■ TYPICAL CARACTERISTICS

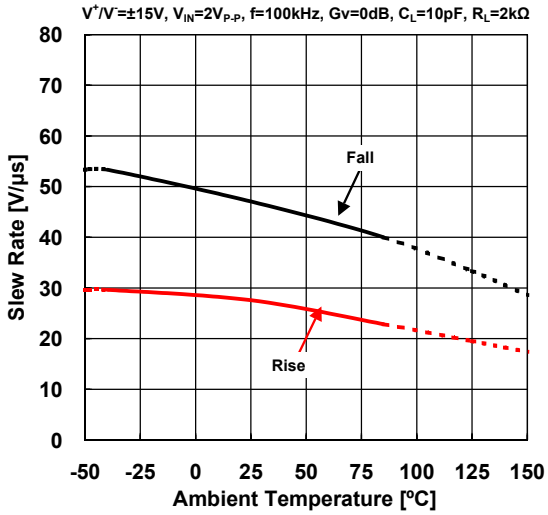
Pulse Response

V^+/V^-=±15V, Gv=0dB, C_L=10pF, R_L=2kΩ, Ta=25ºC



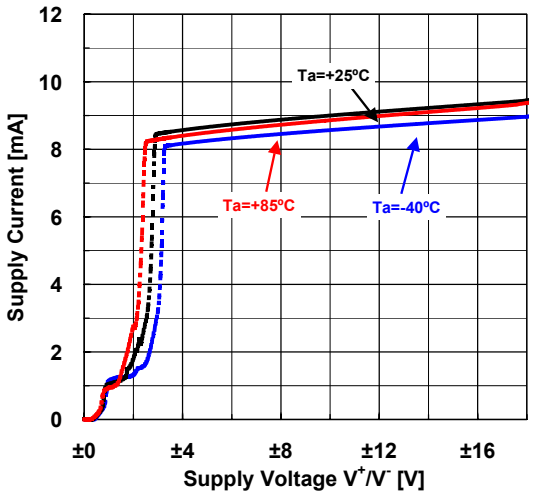
Slew Rate vs. Temperature

V^+/V^-=±15V, V_{IN}=2V_{P-P}, f=100kHz, Gv=0dB, C_L=10pF, R_L=2kΩ



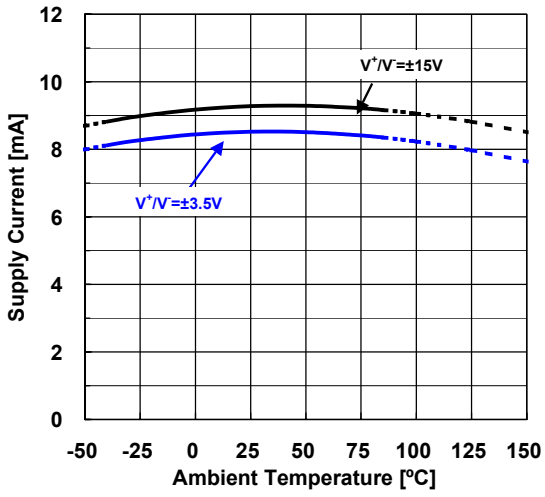
Supply Current vs. Supply Voltage (Temperature)

A_V=0dB



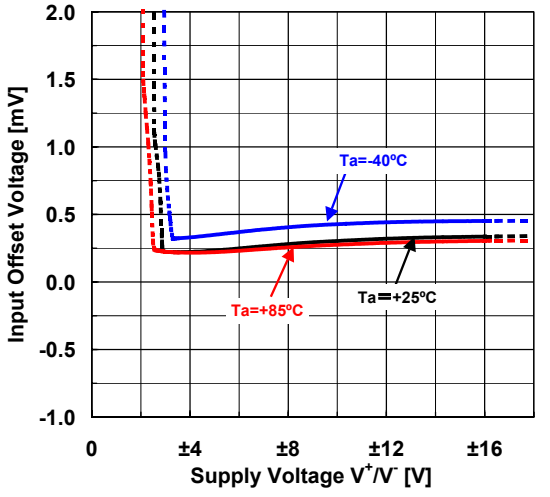
Supply Current vs. Temperature (Supply Voltage)

A_V=0dB



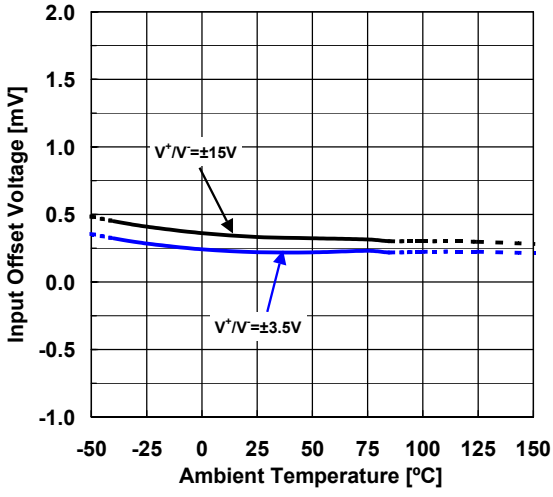
Input Offset Voltage vs. Supply Voltage (Temperature)

V_{ICM}=0V, V_{IN}=0V



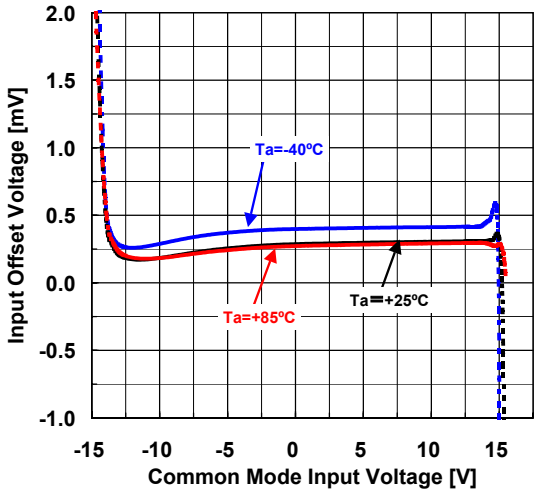
Input Offset Voltage vs. Temperature (Supply Voltage)

V_{ICM}=0V, V_{IN}=0V

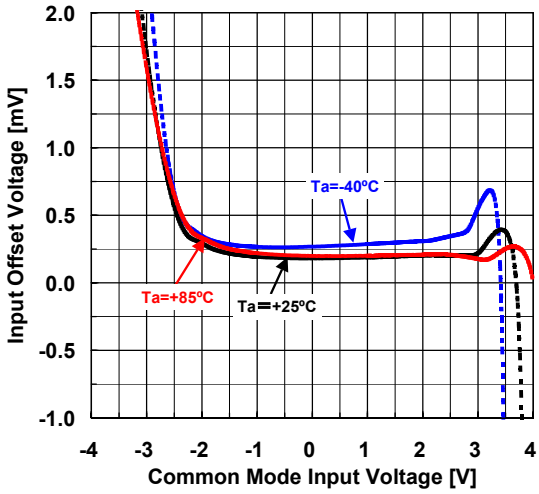


■ TYPICAL CARACTERISTICS

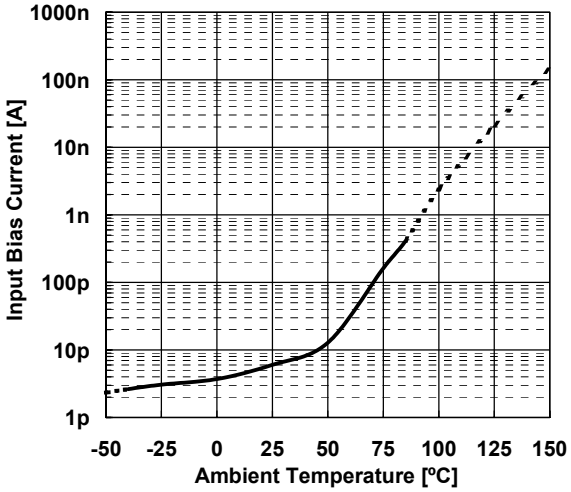
Input Offset Voltage
vs. Common Mode Input Voltage
(Temperature)
V^+/V^-=±15V



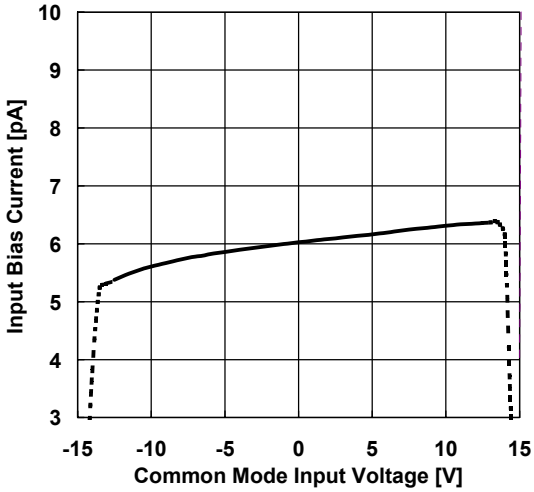
Input Offset Voltage
vs. Common Mode Input Voltage
(Temperature)
V^+/V^-=±3.5V



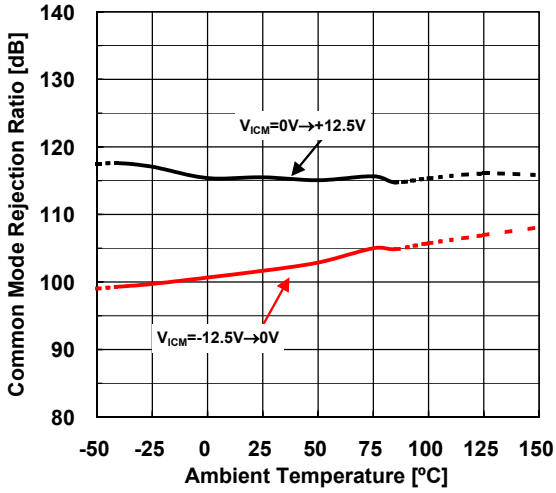
Input Bias Current vs. Temperature (Supply Voltage)
V_{ICM}=0V, V^+/V^-=±15V



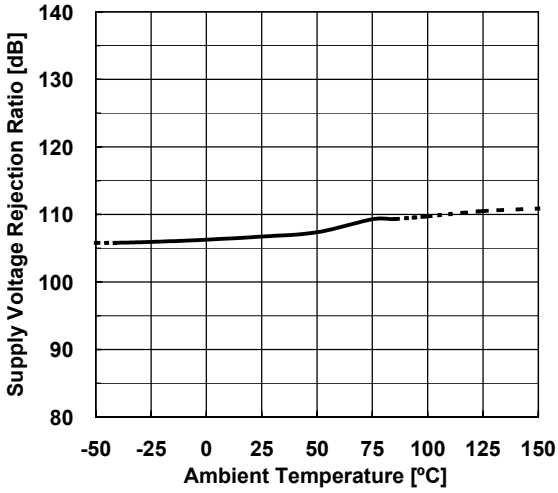
Input Bias Current vs. Common Mode Input Voltage
(Temperature)
V^+/V^-=±15V, Ta=25ºC



CMR vs. Temperature
V^+/V^-=±15V

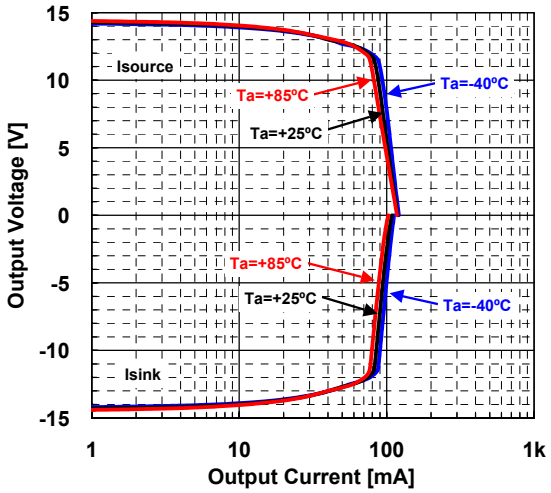


SVR vs. Temperature
V_{ICM}=0V, V^+/V^-=±3.5V→±16V

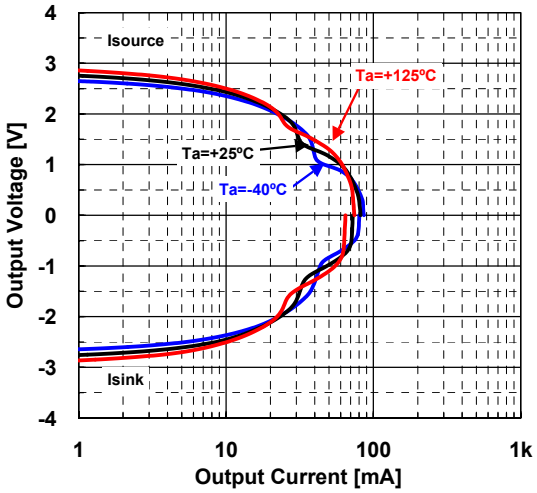


■ TYPICAL CARACTERISTICS

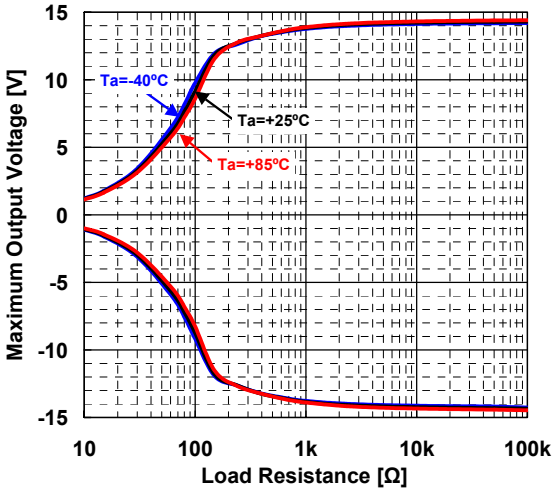
Output Voltage vs. Output Current (Temperature)
V+/V-=±15V



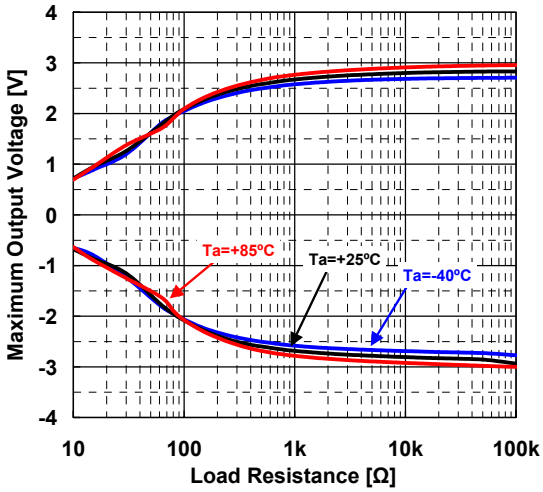
Output Voltage vs. Output Current (Temperature)
V+/V-=±3.5V



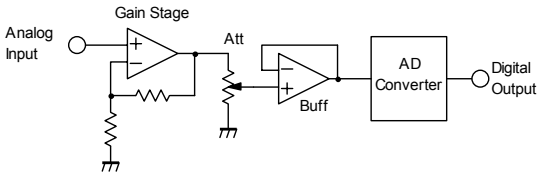
Maximum Output Voltage vs. Load Resistance
(Temperature)
V+/V-=±15V, Gv=open, RL to 0V



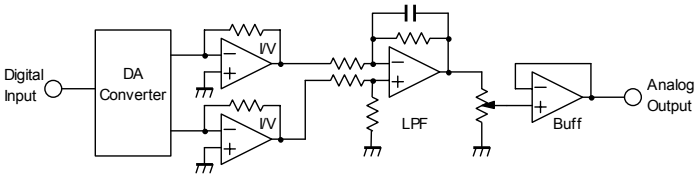
Maximum Output Voltage vs. Load Resistance
(Temperature)
V+/V-=±3.5V, Gv=open, RL to 0V



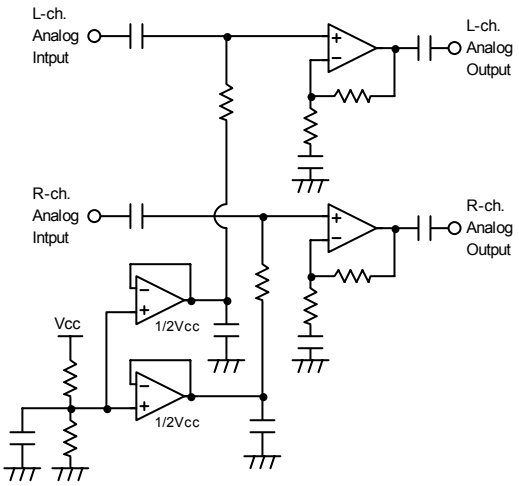
■ APPLICATION CIRCUIT



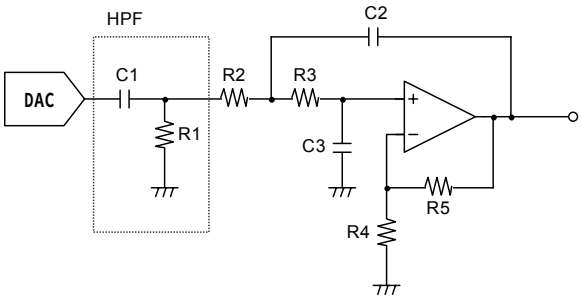
(Fig.1: ADC Input)



(Fig.2:DAC Output)



(Fig.3: Half Vcc Buffer on Single Supply Application)



(Fig.4:DAC LPF Circuit)