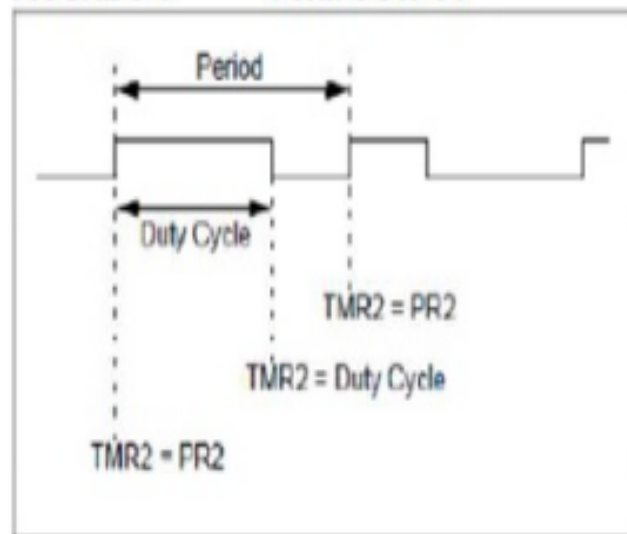# Capture / Compare / PWM (CCP) Modules PWM Signal

FIGURE 8-4:   PWM OUTPUT

If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot \text{Tosc} \cdot (\text{TMR2 Prescale Value})$$

$$\text{PWM frequency} = 1/[\text{PWM period}]$$

$$\text{PWM Duty Cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot \text{Tosc} \cdot (\text{TMR2 Prescale Value})$$

The maximum PWM resolution (bits) for a given PWM frequency is given by the following formula.

EQUATION 8-1:

$$\text{Resolution} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

TABLE 8-3:   EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFFh	0xFFh	0xFFh	0x3Fh	0x1Fh	0x17h
Maximum Resolution (bits)	10	10	10	8	7	5.5