Timer 2 module has period register PR2, at memory location 92_H. The programmer can preset PR2 to a value, which is when the timer is on, continuously compared with the TMR2 register value. If TMR2 reaches PR2 value then TMR2 is cleared to zero on the next increment cycle. Hence, there are PR2+1 cycles between each reset of TMR2 register. This reset is the TMR2 output illustrated in the block diagram, and can be used as a baud rate generator by the synchronous serial port (55P). The resets forms an input to the postscaler, which can be used as an interrupt. The postscaler is controlled by the Timer 2 postscaler bits (TOUTP53, TOUTP52, TOUTP51) of the T2CON control register.

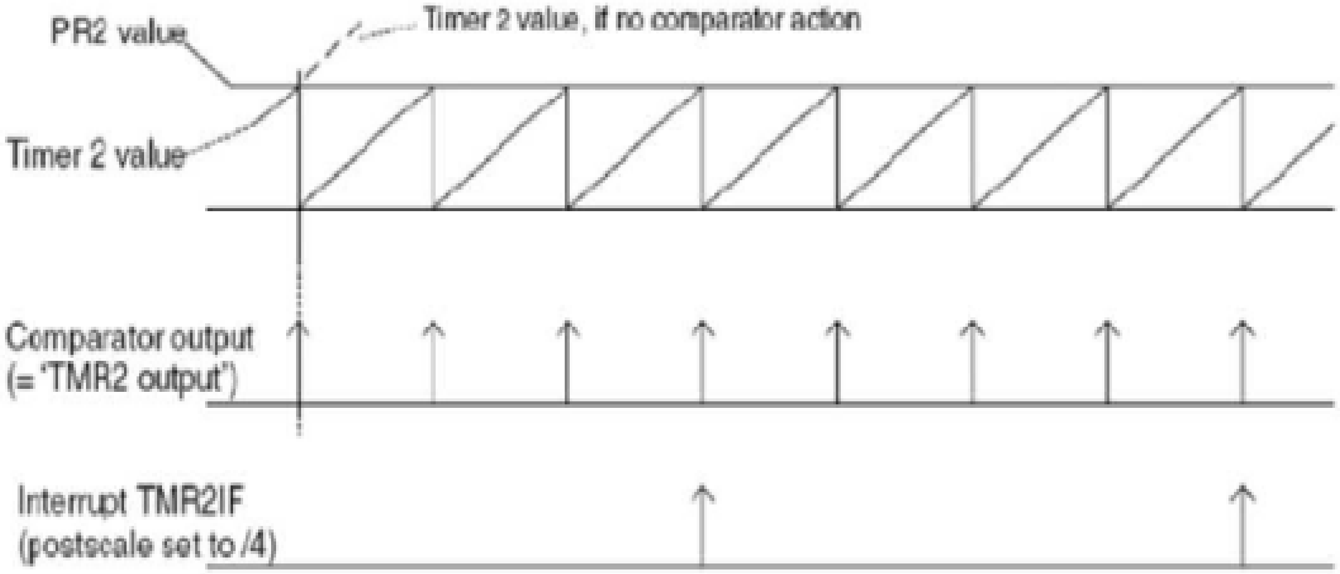

Figure 9.6 PR2 and comparator action

Void setup_timer_2 (mode, period, postscale)

This built-in function is used to configure T/MER 2 module operation. The mode specifies whether the timer is disabled or the prescaler values 1, 4, 16. The timer value may be read and written to using get_timer2() and set_timer2(). Timer 2 is an 8-bit counter/timer.

mode may be one of: T2_D/SABLED, T2_D/V_BY_1, T2_D/V_BY_4, T2_D/V_BY_16 //To dis able Timer 2, and prescaler values period is a int 0-255 that determines when the clock value

//period is PR2

postscale is a number 1-16 that determines how many timer resets before an interrupt: (1 means one reset, 2 means 2, and so on).

Example instructions:

setup_timer_2 (T2_D/V_BY_4, 0xc0, 2);

// At 20mhz, the timer will increment every 800ns: Fosc= 20MHz 3 Fosc/^{4} =5MHz 3

// 5MHz/4=1.25MHz31/(1.25MHz=800ns)

// will overflow every 153.6us: $0xC0_H = 192_D$ 3 192x800ns 3 153.6 microseconds

// and will interrupt every 307.2us: 2x153.6microseconds=307.2microseconds.