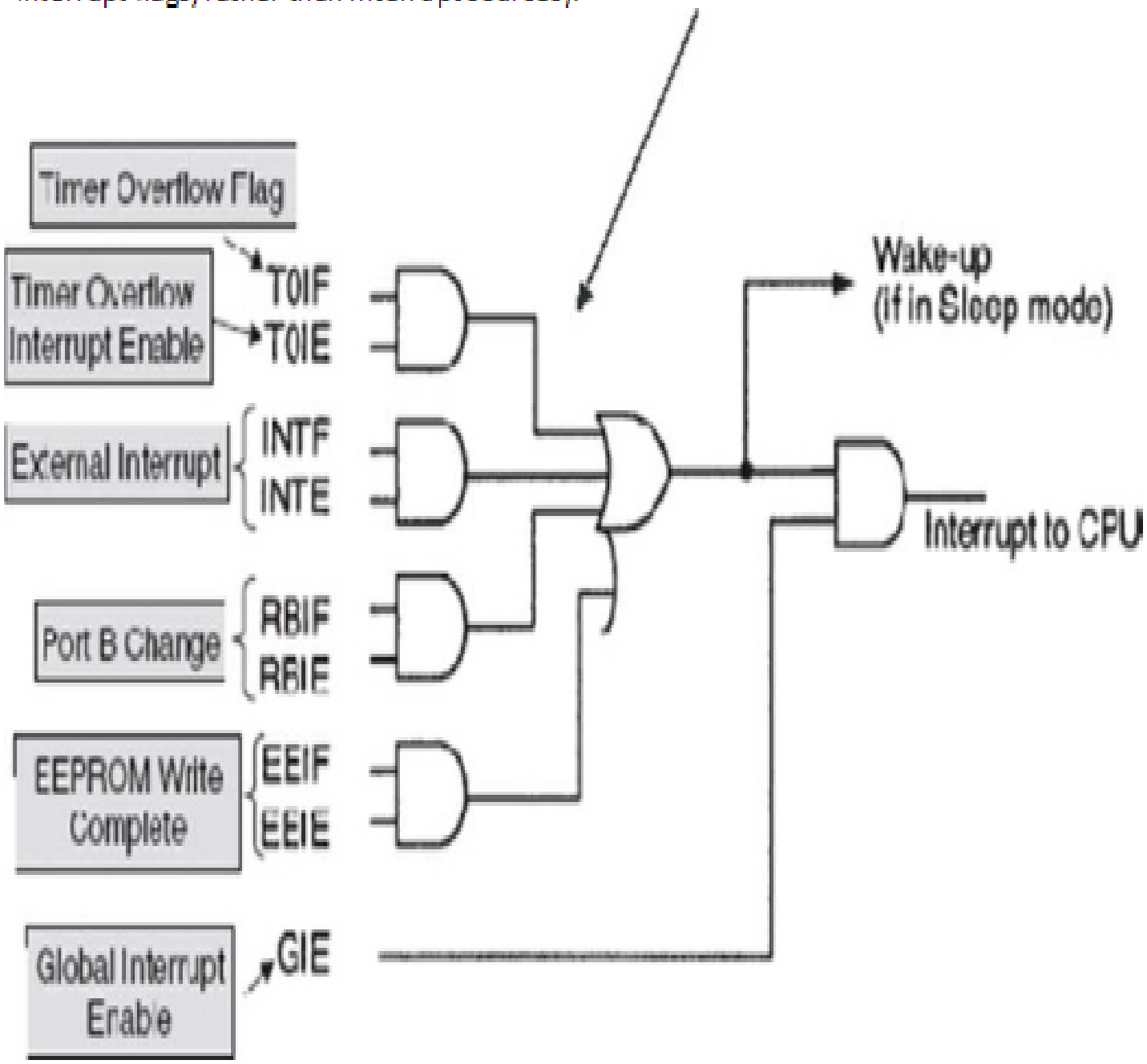
16F84A Interrupt Logic Structure

Interrupt logic structure of 16F84A is shown below. The 5 FR that controls it is the INTCON register and OPTION register. INTCON register contains enable bits of all interrupt sources and OPTION register contain interrupt edge select bit of external interrupt source

Each source has an enable line (labeled by E) and a flag line (labeled by F, actually these are the interrupt flags, rather than interrupt sources).



Note: All four 16 F84A interrupts can be enabled or disabled (maskable). Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit.