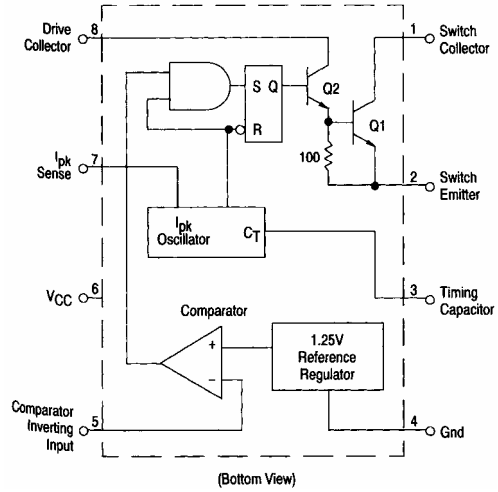
# *DC TO DC CONVERTER CONTROL CIRCUITS* MC34063

The MC34063 is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

## *FEATURES*

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.2 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

## *FUNCTIONAL BLOCK DIAGRAM*



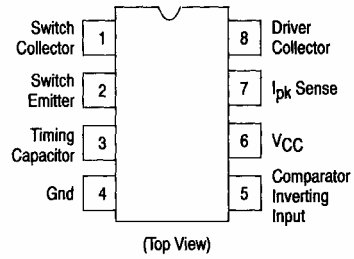

## *MAXIMUM RATINGS*

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 40 | Vdc |
| Comparator Input Voltage Range | $V_{IR}$ | -0.3 to +40 | Vdc |
| Switch Collector Voltage | $V_{C(switch)}$ | 40 | Vdc |
| Switch Emitter Voltage (Vpin 1 = 40 V) | $V_{E(switch)}$ | 40 | Vdc |
| Switch Collector to Emitter Voltage | $V_{CE(switch)}$ | 40 | Vdc |
| Driver Collector Voltage | $I_{C(driver)}$ | 40 | Vdc |
| Driver Collector Current (Note 1) | $I_{C(driver)}$ | 100 | mA |
| Switch Current | $I_{SW}$ | 1.2 | A |
| Power Dissipation and Thermal Characteristics<br>Ceramic Package, U Suffix $T_A$ = +25°C<br>Thermal Resistance<br>Plastic Package, P Suffix $T_A$ = +25°C<br>Thermal Resistance<br>SOIC Package, D Suffix TA = +25°C<br>Thermal Resistance | <br><br>$P_D$<br>$R_{\theta JA}$<br>$P_D$<br>$R_{\theta JA}$<br>$P_D$<br>$R_{\theta JA}$ | <br><br>1.25<br>100<br>1.25<br>100<br>625<br>160 | <br><br>W<br>°C/W<br>W<br>°C/W<br>mW °C/W |
| Operating Junction Temperature | TJ | +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 to +85 | °C |
| Storage Temperature Range | Tstg | -65to+150 | °C |

ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| 34063 | -40° to +85°C | SOP-8 |
| 34063 | | DIP |

Pin connection




## *ELECTRICAL CHARACTERICISTICS*

($V_{CC}$ = 5.0 V, $T_A$= -40 to +85°C unless otherwise specified.)

| **Characteristics** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| ***OSCILLATOR*** | | | | | |
| Frequency ($V_{Pin\ 5}$ = 0 V, $C_T$ = 1.0 nF, $T_A$ = 25°C) | fosc | 24 | 33 | 42 | kHz |
| Charge Current ($V_{CC}$ = 5.0 V to 40 V, $T_A$ = 25°C) | Ichg | 24 | 33 | 42 | μA |
| Discharge Current ($V_{CC}$ = 5.0 V to 40 V, $T_A$ = 25°C) | Idischg | 140 | 200 | 260 | μA |
| Discharge to Charge Current Ratio (Pin7 to Vcc, $T_A$=25°C) | Idischg/Ichg | 5.2 | 6.2 | 7.5 | — |
| Current Limit Sense Voltage (Ichg = Idischg, $T_A$ = 25°C) | Vlpk(sense) | 250 | 300 | 350 | mV |
| ***OUTPUT SWITCH (Note 3)*** | | | | | |
| Saturation Voltage, Darlington Connection ($I_{SW}$ = 1.0 A, Pins 1, 8 connected) | $V_{CE}$(sat) | — | 1.0 | 1.3 | V |
| Saturation Voltage ($I_{SW}$ = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to $V_{CC}$. Forced β = 20) | $V_{CE}$(sat) | — | 0.45 | 0.7 | V |
| DC Current Gain ($I_{SW}$ = 1.0 A, $V_{CE}$ = 5.0 V, $T_A$ = 25°C) | $h_{FE}$ | 50 | 120 | — | — |
| Collector Off-State Current ($V_{CE}$ = 40V) | $I_C$(off) | — | 0.01 | 100 | μA |
| ***COMPARATOR*** | | | | | |
| Threshold Voltage ($T_A$ = 25°C)<br>($T_A$ = $T_{LOW}$ to $T_{HIGH}$) | Vth | 1.225<br>1.21 | 1.25<br>— | 1.275<br>1.29 | V |
| **Threshold Voltage ($T_A$ = 25°C) **** | **Vth** | **1.2375** | **1.25** | **1.2625** | **V** |
| Threshold Voltage Line Regulation ($V_{CC}$ = 3 0 V to 40 V) | Regline | | 1.4 | 5.0 | mV |
| Input Bias Current (Vin=0V) | $I_{IB}$ | — | -40 | -400 | nA |
| ***TOTAL DEVICE*** | | | | | |
| Supply Current ($V_{CC}$ = 5 0 V to 40 V, $C_T$ = 1 0 nF, $V_{pin7}$ = $V_{CC}$. $V_{Pin5}$ > Vth, Pin 2 = Gnd, Remaining pins open) | $I_{CC}$ | | 2.5 | 4.0 | mA |

NOTES:

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain Junction temperature as close to ambient temperature as possible
3. If the output switch is driven into hard saturation (non Darlington configuration) at low switch currents (< 300 mA) and high driver currents (>30 mA), it may take up to 2.0 μs to come out of saturation This condition will shorten the off' time at frequencies > 30 kHz, and is magnified at high temperatures This condition does not occur with a Darlington configuration, since the output switch cannot saturate If a non Darlington configuration is used, the following output drive condition is recommended

Forced β of output switch = $I_C$, output/(Ic, driver -7.0 mA*) > 10

*The 100 Ω. resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts

****Possible version for shipment**

***ELECTRICAL CHARACTERICISTICS***

($V_{CC}$ = 3.3 V, $T_A$= -40 to +85°C unless otherwise specified.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***OSCILLATOR*** | | | | | |
| Frequency ($V_{Pin\ 5}$ = 0 V, $C_T$ = 1.0 nF, $T_A$ = 25°C) | fosc | 24 | 33 | 42 | kHz |
| Charge Current ($V_{CC}$ = 5.0 V to 40 V, $T_A$ = 25°C) | Ichg | 24 | 33 | 42 | μA |
| Discharge Current ($V_{CC}$ = 5.0 V to 40 V, $T_A$ = 25°C) | Idischg | 140 | 200 | 260 | μA |
| Discharge to Charge Current Ratio (Pin7 to Vcc, $T_A$=25°C) | Idischg/Ichg | 5.2 | 6.2 | 7.5 | — |
| Current Limit Sense Voltage (Ichg = Idischg, $T_A$ = 25°C) | Vlpk(sense) | 250 | 300 | 350 | mV |
| ***OUTPUT SWITCH (Note 3)*** | | | | | |
| Saturation Voltage, Darlington Connection ($I_{SW}$ = 1.0 A, Pins 1, 8 connected) | $V_{CE}$(sat) | — | 1.0 | 1.3 | V |
| Saturation Voltage ($I_{SW}$ = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to $V_{CC}$. Forced β = 20) | $V_{CE}$(sat) | — | 0.45 | 0.7 | V |
| DC Current Gain ($I_{SW}$ = 1.0 A, $V_{CE}$ = 5.0 V, $T_A$ = 25°C) | $h_{FE}$ | 50 | 120 | — | — |
| Collector Off-State Current ($V_{CE}$ = 40V) | $I_C$(off) | — | 0.01 | 100 | μA |
| ***COMPARATOR*** | | | | | |
| Threshold Voltage ($T_A$ = 25°C)<br>($T_A$ = $T_{LOW}$ to $T_{HIGH}$) | Vth | 1.225<br>1.21 | 1.25<br>— | 1.275<br>1.29 | V |
| **Threshold Voltage ($T_A$ = 25°C) **** | **Vth** | **1.2375** | **1.25** | **1.2625** | **V** |
| Threshold Voltage Line Regulation ($V_{CC}$ = 3 0 V to 40 V) | Regline | | 1.4 | 5.0 | mV |
| Input Bias Current (Vin=0V) | $I_{IB}$ | — | -40 | -400 | nA |
| ***TOTAL DEVICE*** | | | | | |
| Supply Current ($V_{CC}$ = 5 0 V to 40 V, $C_T$ = 1 0 nF, $V_{pin7}$ = $V_{CC}$. $V_{Pin5}$ > Vth, Pin 2 = Gnd, Remaining pins open) | $I_{CC}$ | | 2.5 | 4.0 | mA |

NOTES:

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain Junction temperature as close to ambient temperature as possible
3. If the output switch is driven into hard saturation (non Darlington configuration) at low switch currents (< 300 mA) and high driver currents (>30 mA), it may take up to 2.0 μs to come out of saturation This condition will shorten the off' time at frequencies > 30 kHz, and is magnified at high temperatures This condition does not occur with a Darlington configuration, since the output switch cannot saturate If a non Darlington configuration is used, the following output drive condition is recommended

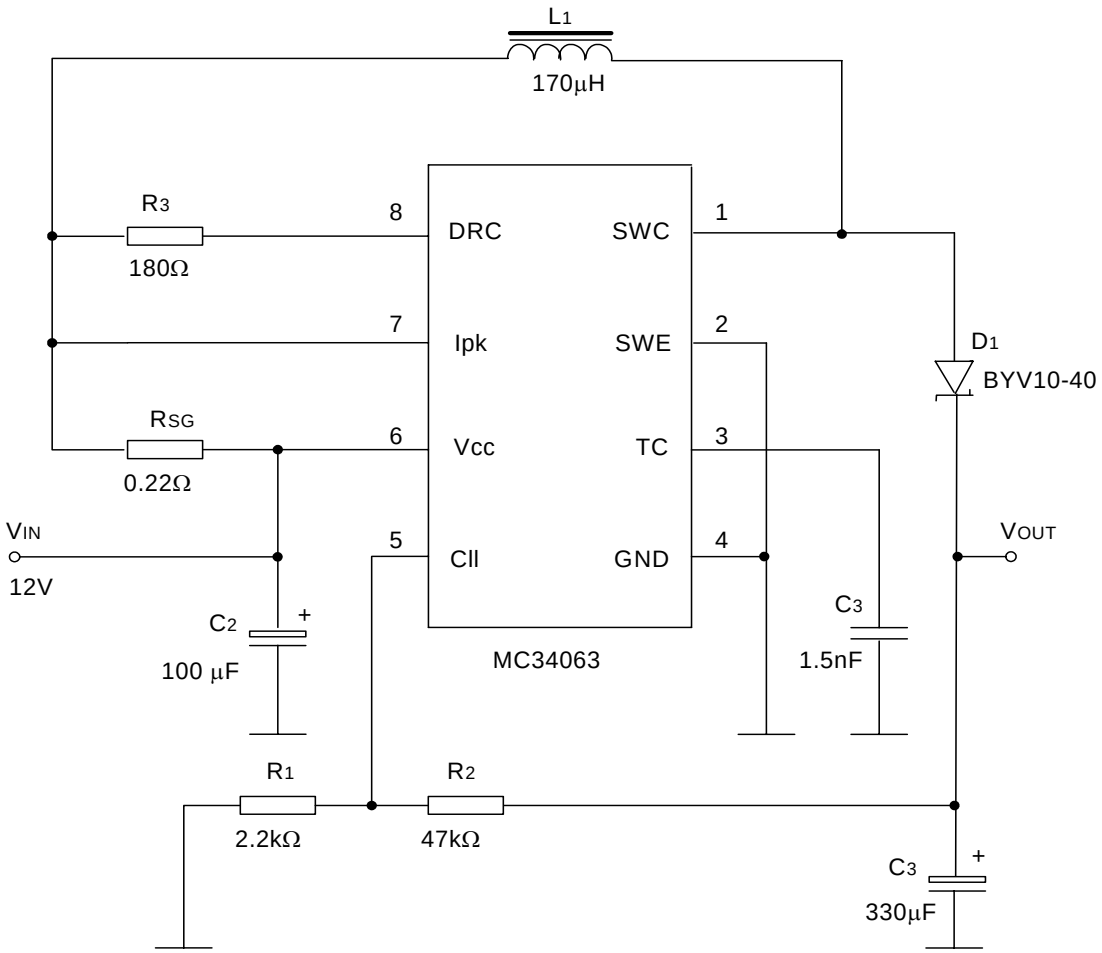
Forced β of output switch = $I_C$, output/(Ic, driver -7.0 mA*) > 10

*The 100 Ω. resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts

****Possible version for shipment**

TYPICAL APPLICATION CIRCUIT

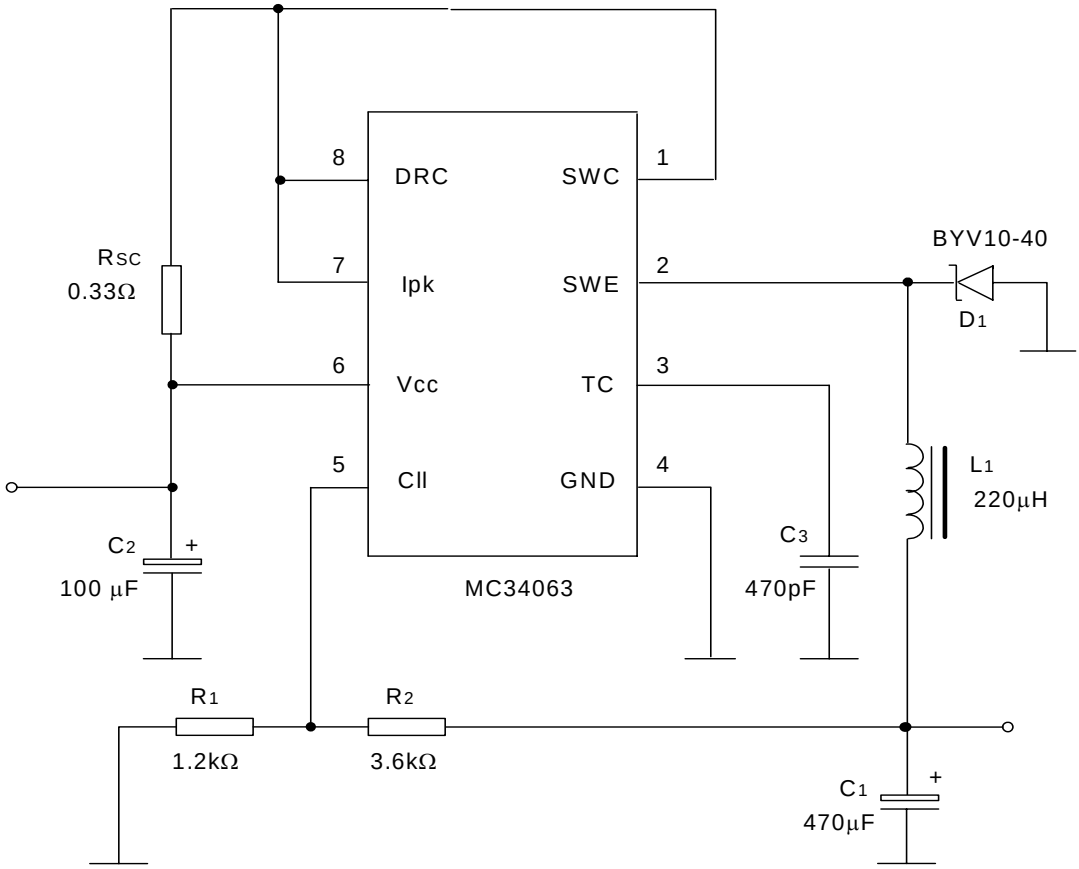
Step-Up Converter




Test Condition ($V_{OUT}$ = 28 V)

| Test | Conditions | Value (Typ) | Unit |
|---|---|---|---|
| Line Regulation | $V_{IN}$ = 8 to 16 V, $I_O$ = 175 mA | 30 | mV |
| Load Regulation | $V_{IN}$ = 12 V, $I_O$ = 75 to 175 mA | 10 | mV |
| Output Ripple | $V_{IN}$ = 12 V, $I_O$ = 175 mA | 300 | mV |
| Efficiency | $V_{IN}$ = 12 V, $I_O$ = 175 mA | 89 | % |

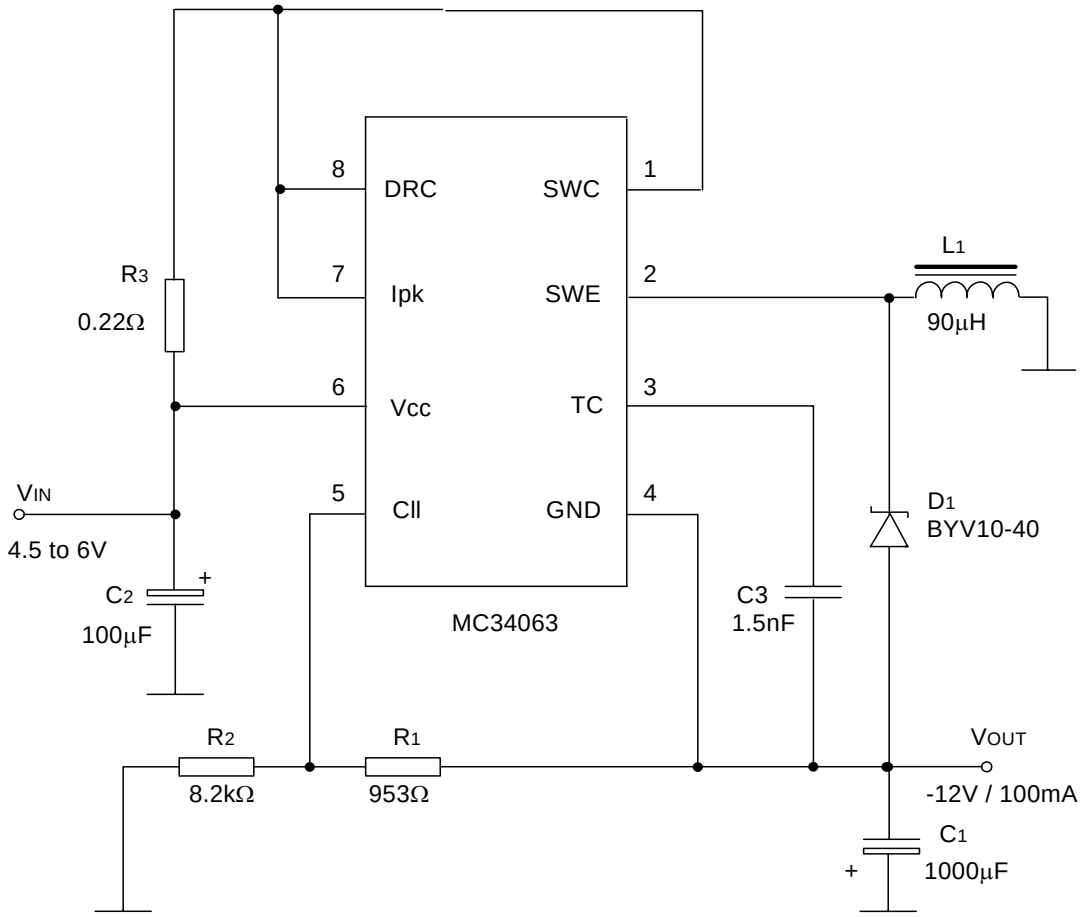
Step-Down Converter




Test Condition ($V_{OUT}$ = 5 V)

| Test | Conditions | Value (Typ) | Unit |
|---|---|---|---|
| Line Regulation | $V_{IN}$ = 15 to 25 V, $I_O$ = 500 mA | 5 | mV |
| Load Regulation | $V_{IN}$ = 25 V, $I_O$ = 50 to 500 mA | 30 | mV |
| Output Ripple | $V_{IN}$ = 25 V, $I_O$ = 500 mA | 100 | mV |
| Efficiency | $V_{IN}$ = 25 V, $I_O$ = 500 mA | 80 | % |
| ISC | $V_{IN}$ = 25 V, RLOAD = 0.1 Ω | 1.2 | A |

Voltage Inverting Converter




Test Condition ($V_{OUT}$ = -12 V)

| Test | Conditions | Value (Typ) | Unit |
|---|---|---|---|
| Line Regulation | $V_{IN}$ = 4.5 to 6 V, $I_O$ = 100 mA | 15 | mV |
| Load Regulation | $V_{IN}$ = 5 V, $I_O$ = 10 to 100 mA | 20 | mV |
| Output Ripple | $V_{IN}$ = 5 V, $I_O$ = 100 mA | 230 | mV |
| Efficiency | $V_{IN}$ = 5 V, $I_O$ = 100 mA | 58 | % |
| ISC | $V_{IN}$ = 5 V, RLOAD = 0.1 Ω | 0.9 | A |

Calculation

| Parameter | Step-Up (Discontinuous mode) | Step-Down (Continuous mode) | Voltage Inverting (Discontinuous mode) |
|---|---|---|---|
| $t_{on}/t_{off}$ | $\frac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$ | $\frac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$ | $\frac{\lvert V_{out}\rvert+V_F}{V_{in}-V_{sat}}$ |
| $(t_{on}+t_{off})max$ | $1/f_{min}$ | $1/f_{min}$ | $1/f_{min}$ |
| $C_T$ | $4.5x10^{-5}t_{on}$ | $4.5x10^{-5}t_{on}$ | $4.5x10^{-5}t_{on}$ |
| $I_{PK(switch)}$ | $2I_{out(max)}[(t_{on}/t_{off})+1]$ | $2I_{out(max)}$ | $2I_{out(max)}[(t_{on}/t_{off})+1]$ |
| $R_{SC}$ | $0.3/I_{PK(switch)}$ | $0.3/I_{PK(switch)}$ | $0.3/I_{PK(switch)}$ |
| $C_O$ | $\equiv \frac{I_{out}t_{on}}{V_{ripple(p-p)}}$ | $\frac{I_{PK(switch)}(t_{on}+t_{off})}{8V_{ripple(p-p)}}$ | $\equiv \frac{I_{out}t_{on}}{V_{ripple(p-p)}}$ |
| L(min) | $\frac{V_{in(min)}-V_{sat}}{I_{PK(switch)}}t_{on(max)}$ | $\frac{V_{in(min)}-V_{sat}-V_{out}}{I_{PK(switch)}}t_{on(max)}$ | $\frac{V_{in(min)}-V_{sat}}{I_{PK(switch)}}t_{on(max)}$ |

NOTES:

$V_{sat}$ = Saturation voltage of the output switch

$V_F$ = Forward voltage drop of the output rectifier

THE FOLLOWING POWER SUPPLY CHARACTERISTICS MUST BE CHOSEN:

$V_{in}$ = Nominal input voltage

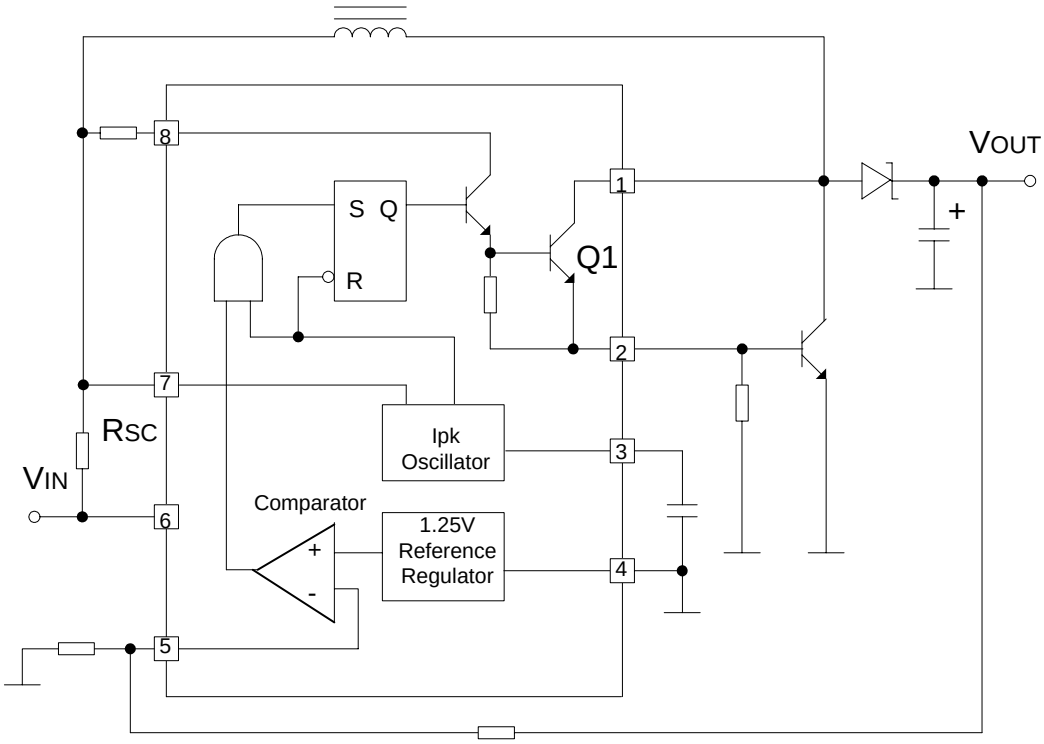
$V_{out}$ = Desired output voltage, $\lvert V_{out}\rvert = 1.25(1+R_2/R_1)$

$I_{out}$ = Desired output current

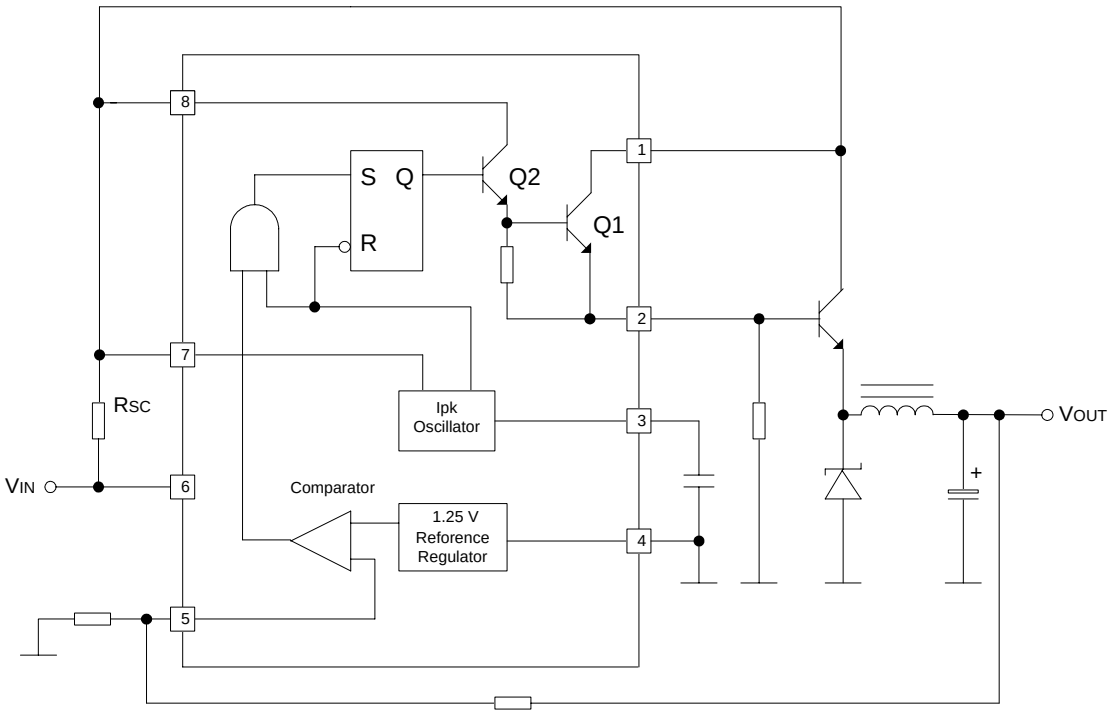
fmin = Minimum desired output switching frequency at the selected values of Vin and lo

$V_{ripple}$ = Desired peak to peak output ripple voltage. In practice, the calculated capacitor value will and to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

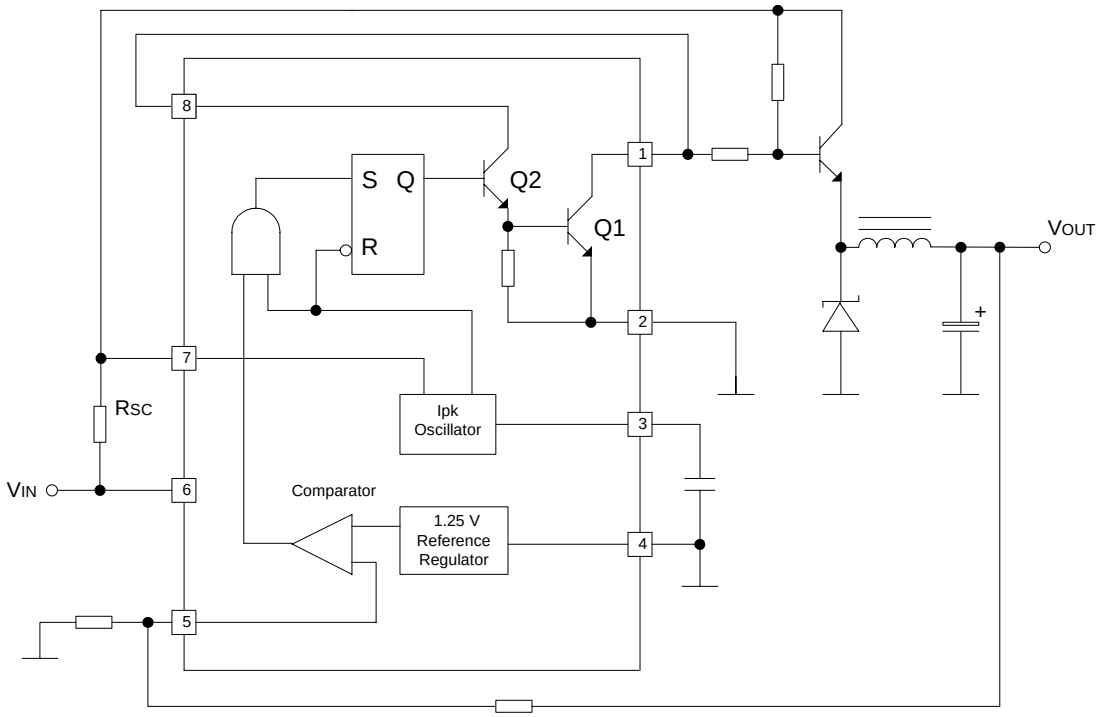
Step-up With External NPN Switch



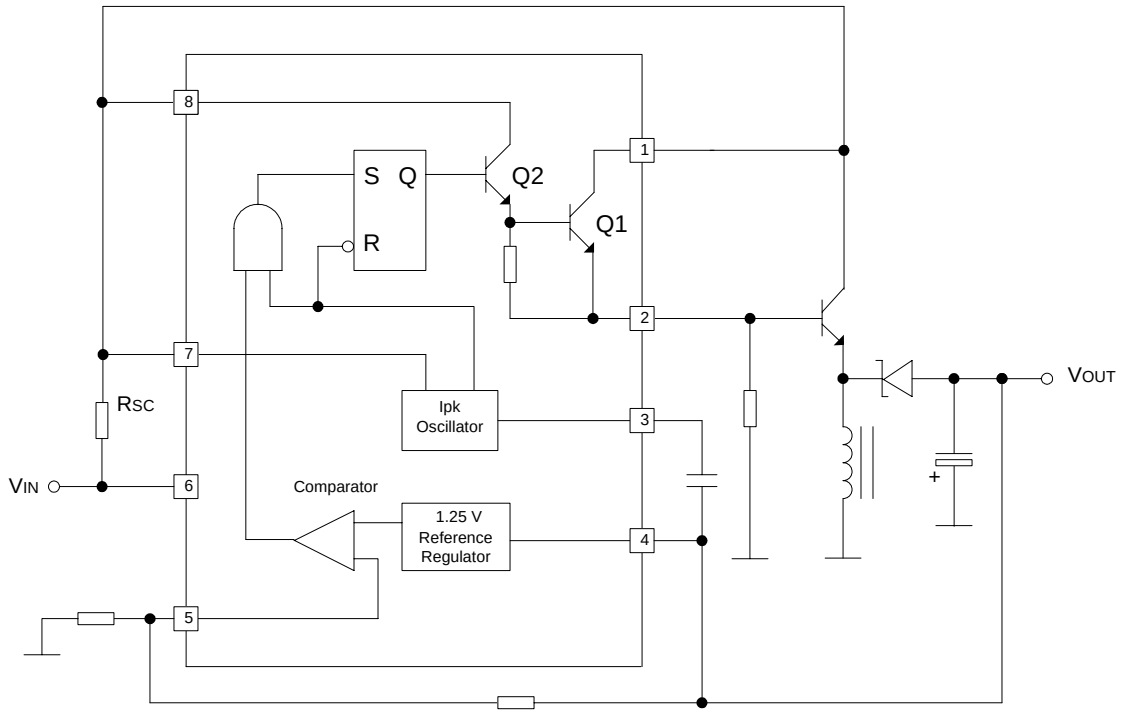
Step-down With External NPN Switch



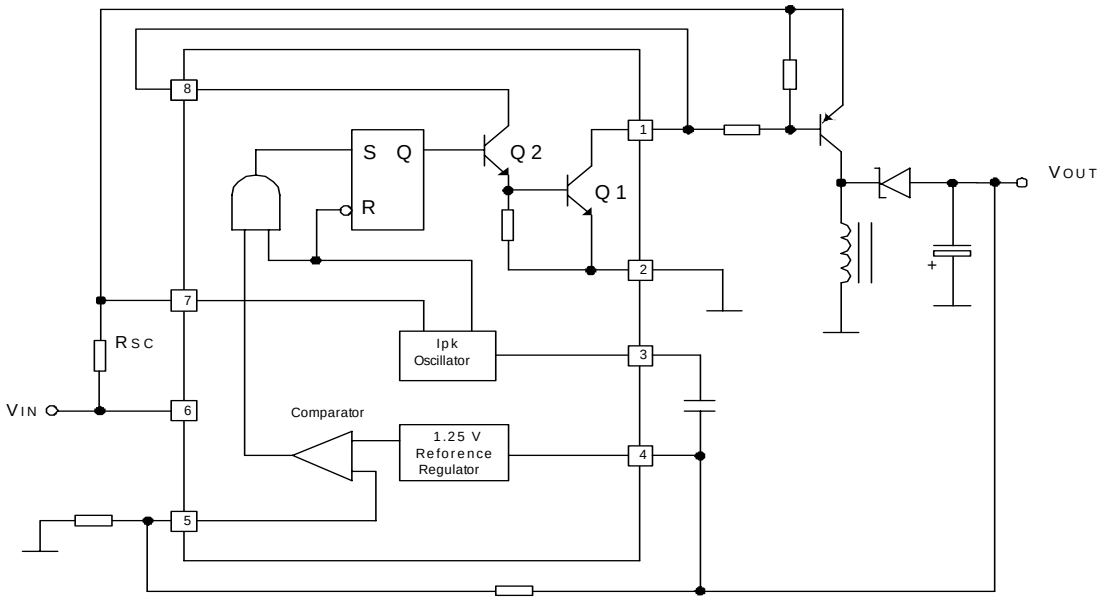

Step-down With External PNP Switch



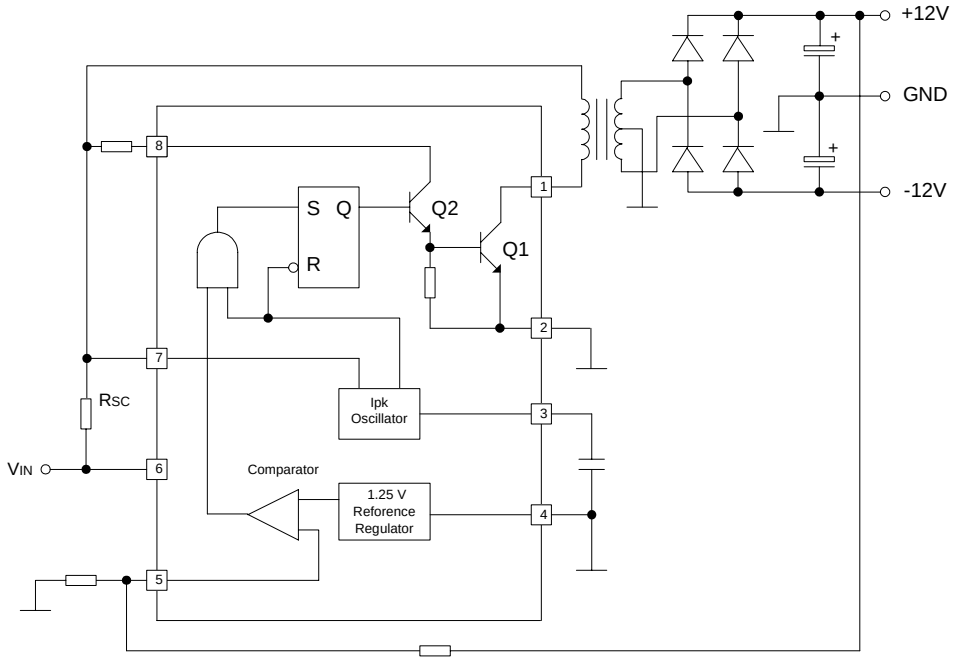
Voltage Inverting With External NPN Switch




Voltage Inverting With External PNP Saturated Switch



Dual Output Voltage




Higher Output Power, Higher Input Voltage