

BIPOLAR DIGITAL ICs

HLL-H 100, H 200 series ☆

TYPE	DESCRIPTION	t_{pd} (ns)	P_D (mW)	f (MHz)	FANOUT	PACKAGE
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Gates

H 102/202	Quad 2-input NAND	105	75	—	25	DIP P/H
H 103/203	Triple 3-input NAND	110	75	—	25	DIP P/H
H 104/204	Expandable dual 4-input NAND	105	75	—	25	DIP P/H
H 105/205	Exp. dual 2-wide 2-input AND-OR-INVERT	110	175	—	25	DIP P/H
H 109/209	Expandable dual 4-input AND power	70	80	—	100 mA	DIP P/H
H 122/222	Quad 2-input (passive pull-up) NAND	120	75	—	10	DIP P/H
H 124/224	Exp. dual 4-input (passive pull-up) NAND	120	75	—	10	DIP P/H
H 167/267	Quad exclusive-OR	—	500	—	25	DIP P/H
H 168/268	Quad exclusive-OR open collector	—	—	—	25	DIP P/H

Flip-flops

H 110/210	Dual JK with separate preset	—	480 ■	1	25	DIP P/H
H 111/211	Dual JK with separate preset and clear	—	480 ■	1	25	DIP Q/K
H 159/259	Quad latch	—	500	—	25	DIP Q/K
H 165/265	Quad Schmitt trigger	—	—	—	—	DIP Q/K
H 166/266	Quad Schmitt trigger open collector	—	—	—	—	DIP Q/K

Other functions

H 112/212	Hex inverter (open collector)	110	55	—	25	DIP P/H
H 113/213	High to low level quad converter (open coll.)	80	60	—	—	DIP P/H
H 114/214	Low to high level quad converter	100	55	—	25	DIP P/H
H 115/215	Hex inverter with strobe (open collector)	110	55	—	25	DIP Q/K
H 117/217	One-shot multivibrator ($T_{pw} \cong 0.83 R_x C_x$)	—	300	—	25	DIP P/H
H 118/218	Hex inverter (active pull-up)	110	60	—	25	DIP P/H
H 119/219	Hex inverter with strobe (active pull-up)	110	60	—	25	DIP Q/K
H 156/256	Binary counter	—	500	1	25	DIP P/H
H 157/257	Decade counter	—	500	1	25	DIP P/H
H 158/258	BCD to decimal decoder Nixie [®] driver	—	460	—	—	DIP Q/K
H 160/260	4-bit shift register	—	500	1.5	25	DIP Q/K

☆ Characteristics of the family: H 100 D1 $V_{CC} = 10.8$ to 20V, temp. range 0 to 75°C, ceramic DIP
 H 100 D6 $V_{CC} = 10.8$ to 16V, temp. range -40 to 85°C, ceramic DIP
 H 100 D2 $V_{CC} = 10.8$ to 16V, temp. range -55 to 125°C, ceramic DIP
 H 200 B1 $V_{CC} = 10.8$ to 16V, temp. range 0 to 75°C, plastic DIP

Noise immunity = 5 V typ @ $V_{CC} = 15V$. HLL can interface directly with COS/MOS, provided $V_{DD} = V_{CC} = 10.8$ to 15 V for HBC/HBF 4000A/4700A series; $V_{DD} = V_{CC} = 10.8$ to 18V for HCC/HCF 4000B/4500B series. No external components or special rules are required.

- Intended as the typical worst case, per gate measured at $V_{CC} = 20 V$ ■ Total P_D for the whole package