AND8490/D

Theory and Applications of the NCP1294, Switching Controller, and Associated Circuits for Lead Acid Battery Charging from a Solar Panel with Maximum Peak Power Tracking (MPPT)

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Introduction

The following paper describes in detail the principle operation of the NCP1294, switching controller, and associated circuits for lead acid battery charging with MPPT. A design example and test data are included.

The NCP1294 solar controller is a flexible solution used in Module Level Power Management (MLPM) solutions.

Background and System Requirements

Most of the solar controller battery chargers on the market today have a large digital content namely to manage maximum power point tracking and battery charging. The manipulation of the power stage, MPPT, and battery management can be controlled with analog circuitry in a cost effective manner. The solar controller parameters for the NCP1294 design are listed below in tabular form.

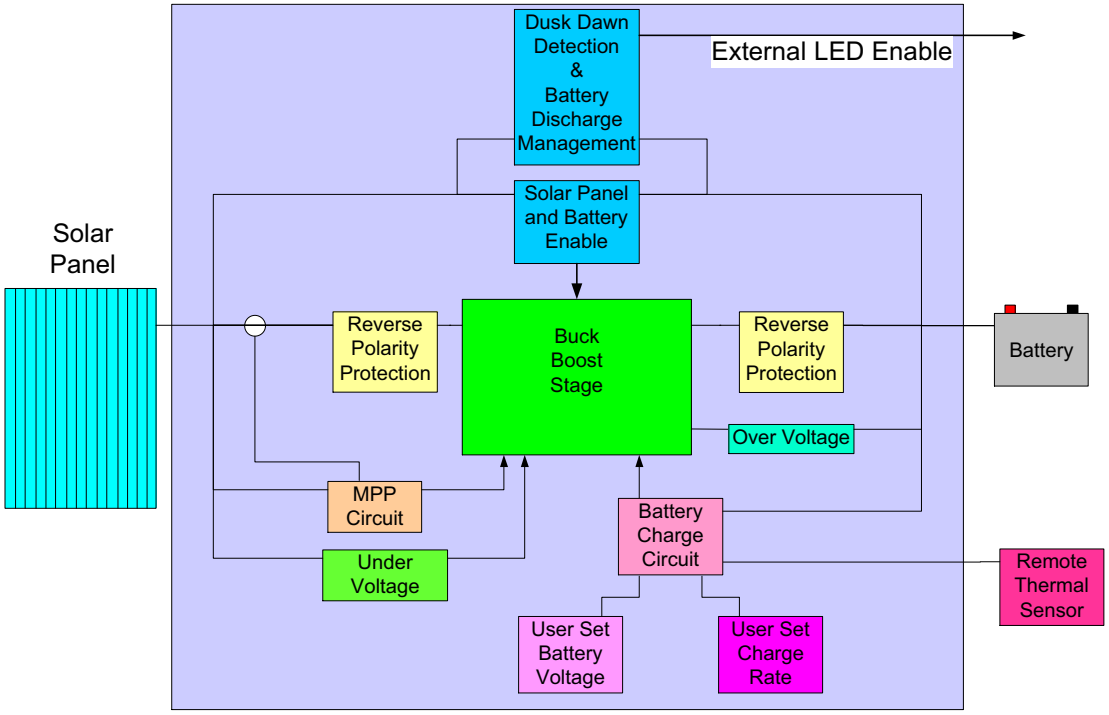


Figure 1. Block Diagram of ON Semiconductor NCP1294 120W Solar Controller

Table 1. ON SEMICONDUCTOR NCP1294 120 W SOLAR CONTROLLER SPECIFICATION

SPECIFICATIONS	Typical Units
Output Current Rating	10 amp maximum (12 V battery controller is limited to 120 W)
Nominal Battery Voltage	12/24/36 VDC
PV Input Voltage	12 V to 60 VDC maximum (Recommended maximum VOC < 50 VDC)
Power Consumption	0.30 W typical standby
Charge Algorithm	3−stage Bulk/Acceptance/Float
Absorption Voltage	14.3 VDC fixed (range 10.0 − 36.0 VDC)
Float Voltage	13.5 VDC fixed (range 10.0 − 36.0 VDC)
Voltage Set Point Limit	17.3 VDC fixed (range 10.0 − 36.0 VDC)
Dusk Dawn Indicator	Positive Logic
Battery Low Indicator	Positive Logic
Temperature Compensation	Optional sensor adjusts charge voltage based on battery temperature
Power Conversion Efficiency	97% Typical 24 V to 14.3 V 8.39 A Output
Physical Configuration and Dimensions	90 mm x 90 mm x 40 mm

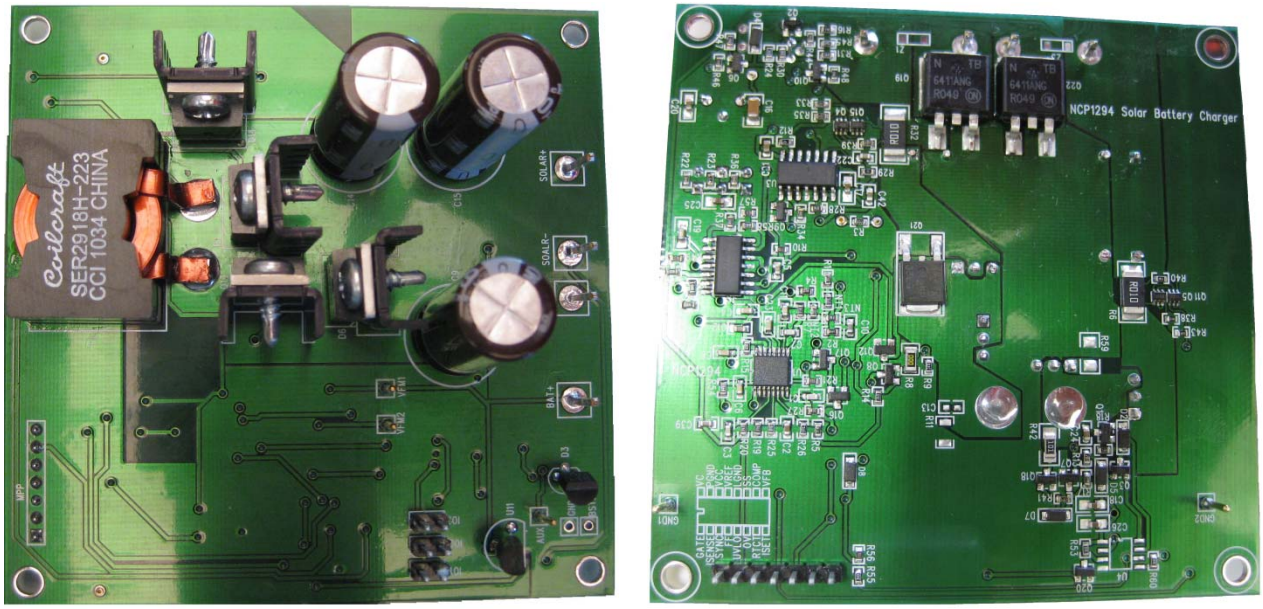


Figure 2.

The specification described above will be configured in a block diagram (Figure 1) to aid the design process and ensure proper understanding of the system. The heart of the system is the power stage which must accept an input voltage of 12 V to 60 V and produce an output of 12 V to 36 V. Since the input voltage range spans the required output voltage, a buck boost topology is required to support the application. The topologies the designer could choose are SEPIC, Non Inverting buck boost, flyback, single switch forward, two switch forward, half bridge, full bridge, or others not listed. The output power for the converter is 120 W, thus the possibility of a flyback converter is eliminated. All of the topologies that are suitable for 120 W or greater have four or more switches and have the added complexity of a transformer with the exception of a four switch buck boost. Future work will include isolated topologies as power demands increase. The output voltage and battery charge rate should be selectable by the installing technician. The battery state of charge must be managed by the proper charge algorithm. Since the controller will be connected to a solar panel, it must have maximum power point tracking (MPPT) to provide a high value to the end customer. The controller should draw no more than 300 mW from either the output or input while not actively converting so all unnecessary circuitry should be turned off unless both the battery and the solar panel are installed. Two positive enable circuits have to be provided to external circuitry. One circuit detects the hours of darkness and another detects the state of charge of the battery so that the external circuit does not discharge the battery to the point of damage. The controller will be installed in the field by technicians and novices with varying degrees of experience, thus it is important to have reverse polarity protection for both the input and output. Since the controller and the batteries may be installed in either a hot or cold location, the controller must accommodate temperature compensation for charging the battery. The design should also include safety features such as battery over voltage detection and solar panel under voltage detection. The resulting block diagram for the system is shown below.

MPPT Methodology

The power source for the controller specified is a solar panel. Solar panels have an IV curve that folds over shortly after the maximum power point where the output voltage falls as the current is increased beyond the maximum power point. Unfortunately the IV curves will change with irradiance, temperature, and age. Irradiance as defined by [3] is “the density of radiation incident on a given surface usually expressed in watts per square centimeter or square meter.” If the solar panel does not have mechanical sun tracking abilities, the irradiance will change as the sun moves approximately ±23° over a year. Further, the irradiance changes daily as the sun moves from horizon to horizon, resulting in a variation of power output throughout the day and year.

The output power increases with decreasing temperature due in large part to the electron and hole mobility of the semiconductor material. Further, as temperature increases, the band gap energy of the semiconductor material also increases. Photons from the sun provide electrons in the valence band of the semiconductor with the energy to leap over the band gap into the semiconductor material. The larger band gap energy means more energy will be required from the photons in the sun to reach the conduction band. As a result, fewer electrons will reach the conduction band resulting in a less efficient solar cell.

To extract the most power out of the variable source, the solar controller specified must employ MPPT. The MPPT must first locate the maximum power point and adjust for environmental conditions in a timely manner to keep the controller close to the maximum power point.

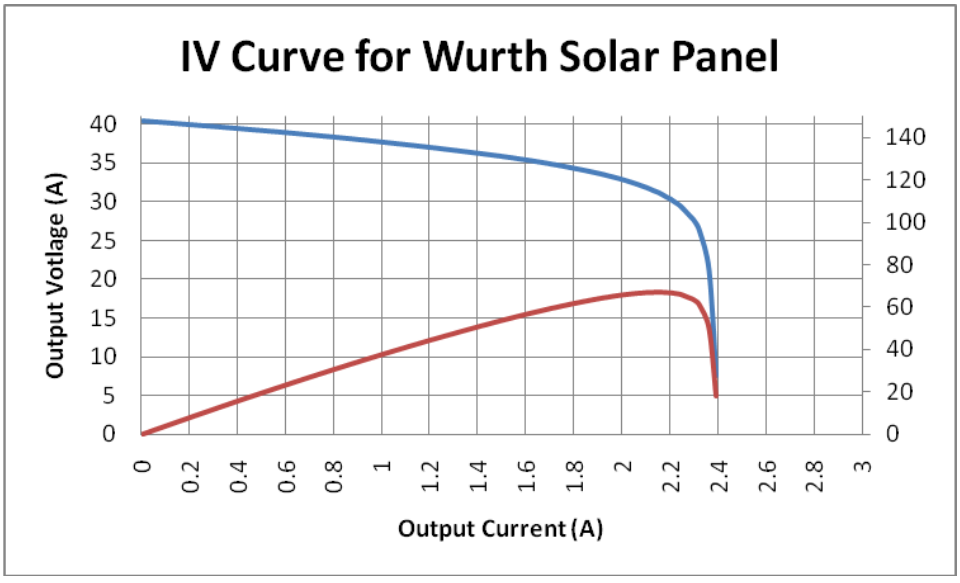


Figure 3. IV Curve GeneCIS Solar Module 70W WSG0036E070

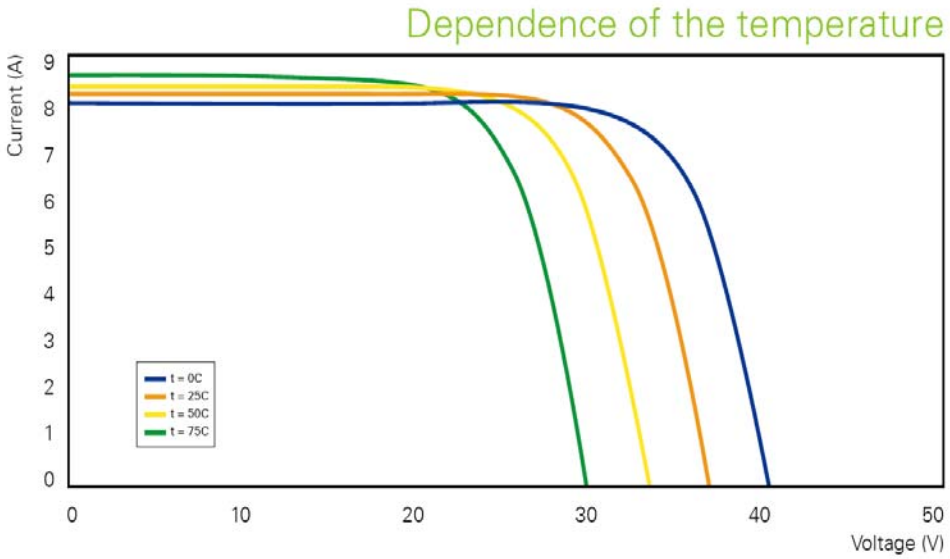


Figure 4. Polycrystalline 6” Silicon Cells BP 3220T Temperature Curves [1]

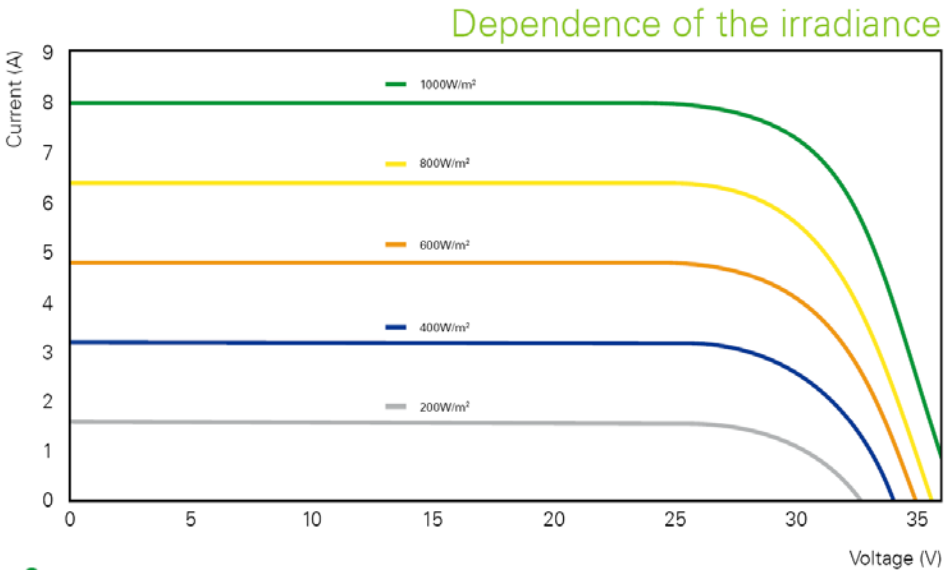


Figure 5. Polycrystalline 6” Silicon Cells BP 3220T Irradiance Curves [1]

Many proven methods exist for MPPT for photo voltaic arrays, but only three will be discussed in this paper for brevity: Fractional Voc, Hill climber/Perturb and observe, and dynamic MPPT.

Fractional Open Circuit Voltage or Voc

Fractional Open Circuit Voltage or Voc relies on the linear relationship between the open circuit voltage of the solar panel and the maximum power point. The method samples the voltage of the solar panel when no load is applied and holds it as a reference for the maximum power point voltage. Figure 5 shows that the maximum power point is between 71% and 78% [2] of the open circuit voltage or about 3/4. Therefore, the following equation can be used to calculate the MPP voltage:

$$VMPP = k * Voc \quad \text{(eq. 1)}$$

The k factor can change with temperature as shown in Figure 4, it is therefore beneficial to temperature compensate the fractional Voc circuit so that it is close to the maximum power point. The advantages to fractional Voc are that it is simple to implement and can be cost effective. The drawback is that the method is not good for a wide variety of solar panels with differing temperature coefficients and open circuit voltages.

Hill Climber/Perturb and Observe

Hill climber involves incrementing the duty cycle and calculating the resulting power change, where “perturb and observe” changes the voltage and observes the power

change. A PWM converter will be used to control the power extracted from the solar array which is a power limited source. Changing the duty cycle also changes the current draw from the array which in turn decreases the voltage in a power limited source. The relationship between duty cycle and voltage is linked so the two concepts will be combined and explained below. The converter starts by drawing very small power from the solar panel, the power is calculated, and the duty cycle is incremented and the power is again calculated. The previous power calculation is compared to the current power calculation and depending on the resulting increase or decrease; the duty cycle is incremented or decremented respectively as shown in Table 2.

Table 2. HILL CLIMBER DECISION TABLE

Change	Change in Power	Next Change
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

The process continues indefinitely finding the maximum power point as fast as the algorithm can move. One drawback to the method is that power is moved from its current point to another point which may not be the maximum power point to see if the maximum power point has changed. The method results in spending half of the time at the maximum power point, while half of the time remains at a suboptimal level. If the algorithm is long, this can mean a significant amount of time is spent not utilizing the maximum power of a solar panel.

Dynamic MPPT

Dynamic MPPT is applied as a change occurs in the system. Since the converter is using PWM, a change is occurring every switching cycle and power drawn from the solar panel is also changing in an observable way every cycle. Dynamic MPPT uses the voltage dip on the solar panel multiplied by the increasing current every switching cycle to determine the error signal that will be produced to regulate the duty cycle. The dynamic response detects the slope of the IV curve, creating a power ramp from which the error signal intersects creating a power representative duty cycle. The cycle ends when the ramp changes slope from positive to negative as shown in Figure 6.

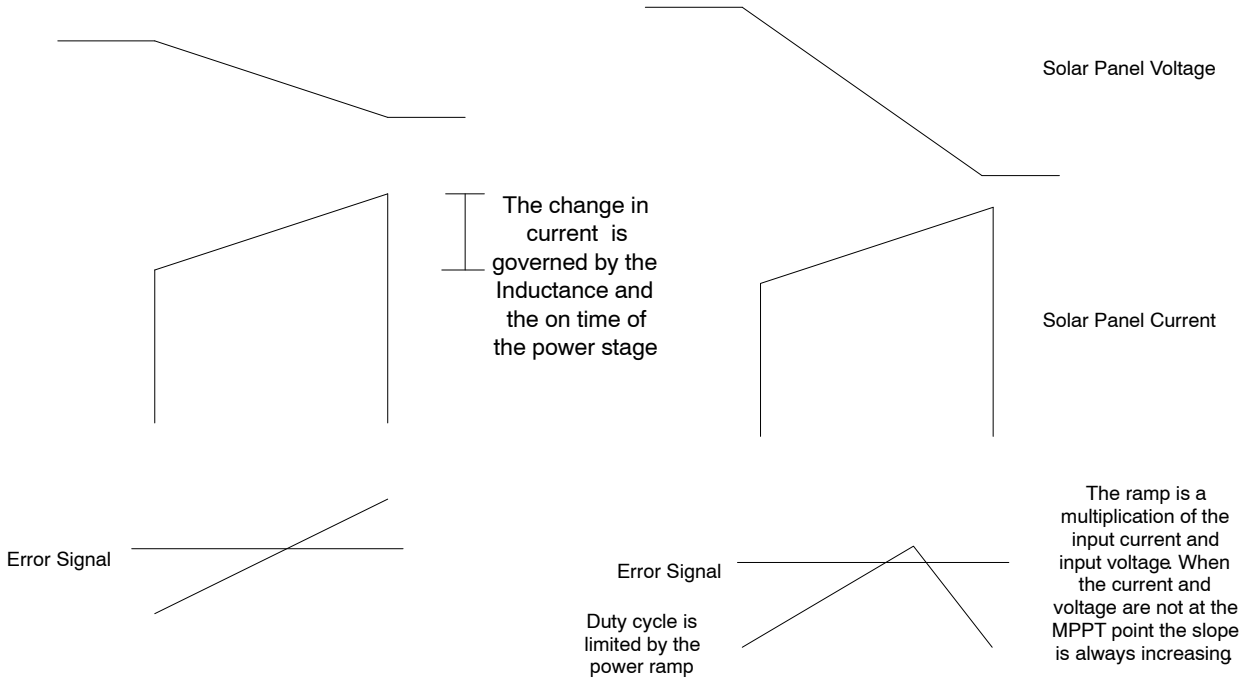


Figure 6. Voltage and Current of a PWM Regulated Converter

NCP1294 Part Description

The NCP1294 fixed frequency feed forward voltage mode PWM controller contains all of the features necessary to be configured in a flyback, boost or forward topology and can be adapted for use in the buck, buck boost, half bridge, and full bridge topologies. The PWM controller has been optimized for high frequency primary side control operation. In addition, the device includes such features as: soft−start, accurate duty cycle limit control, less than 50 μA startup current, over and undervoltage protection, and bidirectional synchronization. [4]

Switch Frequency and Maximum Duty Cycle Calculations

The frequency of the NCP1294 can be set by using an oscillator timing capacitor, CT, which is charged by VREF

through RT and discharged by an internal current source. During the discharge time, the internal clock signal sets the gate output to the low state, thus providing a user selectable maximum duty cycle clamp. Charge and discharge times are determined by following formulas;

$$tc = RT * CT * \ln\left[\frac{V_{ref} - V_{Valley}}{V_{ref} - V_{Peak}}\right] \quad \text{(eq. 2)}$$

$$td = RT * CT * \ln\left[\frac{V_{ref} - V_{Peak} - IdR_T}{V_{ref} - V_{Valley} - IdR_T}\right]$$

tc = charging time
td = discharging time
V_{Peak} = peak voltage of the oscillator
V_{Valley} = valley voltage of the oscillator

For the oscillator to function properly, RT has to be greater than 2.3k.

Feed Forward Voltage Mode Control

In conventional voltage mode control, the ramp signal has a fixed rising and falling slope. The feedback signal is derived solely from the output voltage. Consequently, voltage mode control has inferior line regulation and audio susceptibility. Feed forward voltage mode control derives the ramp signal from the input line. Therefore, the ramp of the slope varies with the input voltage.

At the start of each switch cycle, the capacitor connected to the FF pin is charged through a resistor connected to the input voltage. Meanwhile, the gate output is turned on to drive an external power switching device. When the FF pin voltage reaches the error amplifier output VCOMP, the PWM comparator turns off the gate, which in turn opens the external switch. Simultaneously, the FF capacitor is quickly discharged to 0.3 V.

Overall, the dynamics of the duty cycle are controlled by both input and output voltages. For example, an elevated output voltage reduces VCOMP which in turn causes duty cycle to decrease. However, if the input voltage varies, the slope of the ramp signal will react immediately which provides a much improved line transient response. When the input voltage goes up, the rising edge of the ramp signal increases which reduces duty cycle to counteract the change.

The feed forward feature can also be employed to provide a volt−second clamp, which limits the maximum product of input voltage and turn on time. The clamp is used in circuits, such as forward and flyback converter, to prevent the transformer from saturating. If the line voltage is much greater than the FF pin peak voltage, the charge current can be treated as a constant and is equal to VIN/R. Therefore, the volt−second value is determined by the following equation:

$$V_{IN} * T_{ON} = (VCOMP - VFF(d)) \times R \times C \quad \text{(eq. 3)}$$

VCOMP = COMP pin voltage
VFF(d) = FF pin discharge voltage

As shown in the equation, the volt−second clamp is set by the VCOMP clamp voltage which is equal to 1.8 V. In forward or flyback circuits, the volt−second clamp value is designed to prevent transformers from saturation. In a buck or forward converter, volt−second is equal to:

$$V_{IN} * T_{ON} = \frac{V_{OUT} \times Ts}{n} \quad \text{(eq. 4)}$$

n = transformer turns ratio

The constant, n, is determined by the regulated output voltage, switching period, and transformer turns ratio (use 1.0 for buck converter). As shown in Equations 3 and 4 during steady state, VCOMP doesn't change for input voltage variations, intuitively explaining why FF voltage mode control has superior line regulation and line transient response. Knowing the nominal value of V_{IN} and T_{ON}, one can also select the value of RC to place VCOMP at the center of its dynamic range.

Design Procedure

When selecting a topology for the solar controller, it is important to understand the converters basic operation and its limitations. The topology selected is the non−inverting four switch non−synchronous buck boost topology. The converter operates with a single control signal from the NCP1294, which turns on Q1 and Q2 simultaneously charging L1.

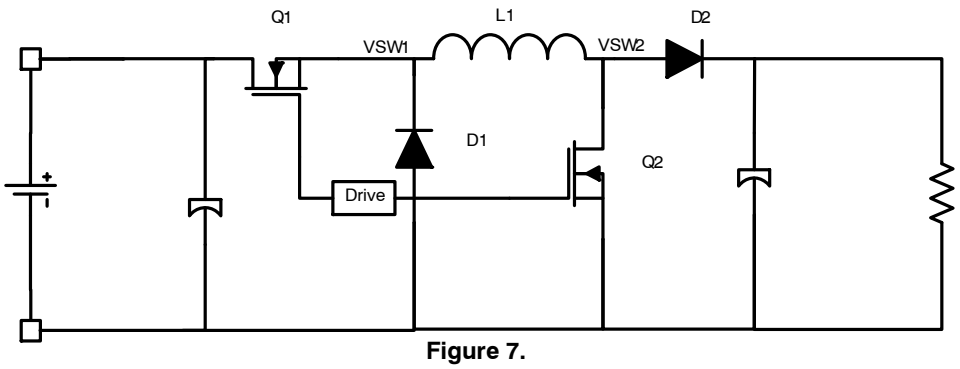


Figure 7.

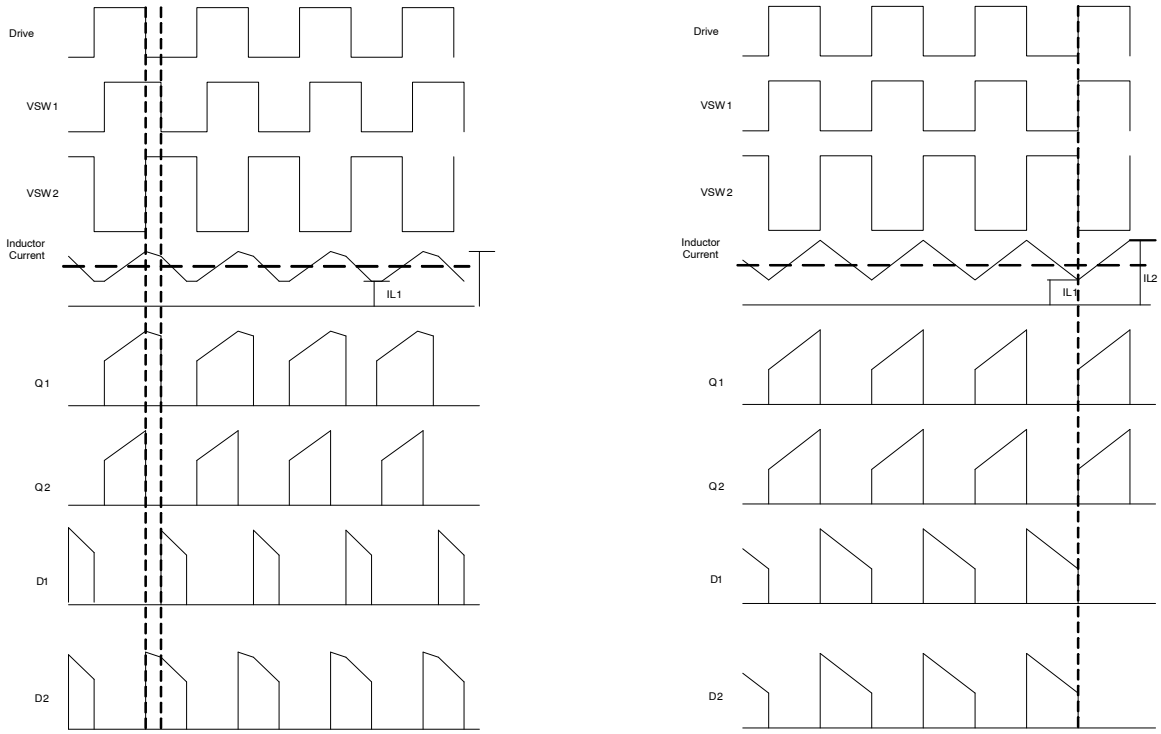


Figure 8. Buck Boost Operation Time Delayed Left, Ideal Right

The four switch buck boost topology is show in Figure 8 where a single inductor is used to control the voltage and current. The four switch non−inverting buck boost has two modes of operation that will be considered the buck mode and the buck boost mode. In the buck mode, the converter produces input voltage pulses that are LC filtered to produce a lower DC output voltage V_{OUT}. The output voltage can be changed by modifying the on time relative to the switching period T or switching frequency. The ratio of high side switch on time to the switching period is called duty ratio D.

$$F_{sw} = \frac{1}{T} \quad \text{(eq. 5)}$$

$$D = \frac{T_{ON}}{T}(1 - D) = \frac{T_{OFF}}{T} \quad \text{(eq. 6)}$$

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}} \rightarrow 56.3\% = \frac{13.5\ V}{24\ V}$$

$$D_{BUCK\_BOOST} = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \rightarrow 36\% = \frac{13.5\ V}{24\ V + 13.5\ V} \quad \text{(eq. 7)}$$

D = Duty cycle
D_{BUCK} = Buck converter duty cycle
D_{BUCK_BOOST} = Buck boost converter duty cycle
F_{SW} = Switching frequency
T = Switching period
T_{OFF} = High side switch off time
T_{ON} = High side switch on time
VIN = Input voltage
V_{OUT} = Output voltage

The solar controller will operate in buck mode if the output voltage can be achieved from 1% to 89%. If the output voltage cannot be reached due to duty cycle limitations, it will switch to buck boost mode where the voltage can be achieved. The duty cycle will change from 89% to a lower duty cycle as show in Figure 9. One thing to note is that when the converters mode switches from buck to buck boost, the error signal will take time to change the duty cycle. The instantaneous change of mode will leave a buck boost converter trying to switch at 89% duty cycle and trying to slew to 47%; this results in the converter trying to output 130 V at the trade over region. The NCP1294 is equipped with a pulse by pulse current limiter and will stop the converter from building energy in the choke to dangerous proportions, easing the transition in duty cycle.

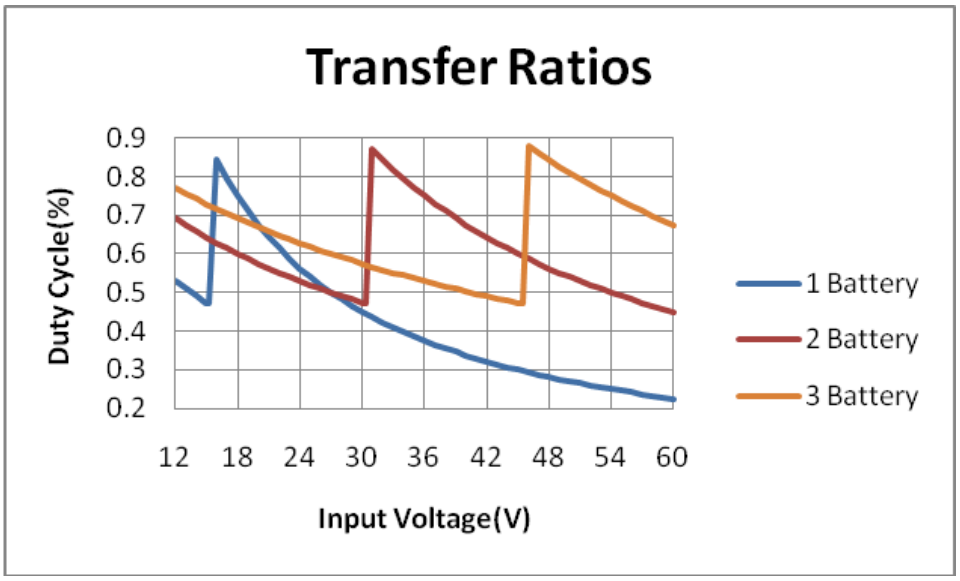


Figure 9. Transfer Ratio Between Buck and Boost Mode for Multiple Batteries

Inductor Selection

When selecting an inductor, the designer may employ a rule of thumb for the design where the percentage of ripple current in the inductor should be between 10% and 40%. The ratio of ripple current to maximum output current is given in Equation 8.

$$ra = \frac{\Delta I}{I_{out}} \quad \text{(eq. 8)}$$

ΔI = Ripple current
I_{out} = Output current
ra = Ripple current ratio

Using the ripple current rule of thumb, the user can establish acceptable values of inductance for a design using Equation 9.

$$L_{OUT\_BUCK} = \frac{V_{IN} * D_{BUCK}}{I_{OUT} \times ra \times F_{SW}} \rightarrow \quad \text{(eq. 9)}$$

$$15.12\ \mu H = \frac{13.5\ V * 56\%}{10\ A \times 25\% \times 200\ kHz}$$

$$L_{OUT\_BUCK\_BOOST} = \frac{V_{IN} * D_{BUCK\_Boost}}{\frac{I_{OUT}}{1 - D_{BUCK\_Boost}} \times ra \times F_{SW}} \rightarrow$$

$$9.68\ \mu H = \frac{13.5 * 36\%}{\frac{10\ A}{1 - 36\%} \times 25\% \times 200\ kHz}$$

D = Duty ratio
D_{BUCK} = Buck converter duty cycle ratio
D_{BUCK_Boost} = Buck boost converter duty cycle ratio
F_{SW} = Switching frequency
I_{OUT} = Output current
L_{OUT_BUCK} = Buck output inductance
$L_{OUT\_BUCK\_BOOST}$ = Buck boost output inductance
ra = Ripple current ratio

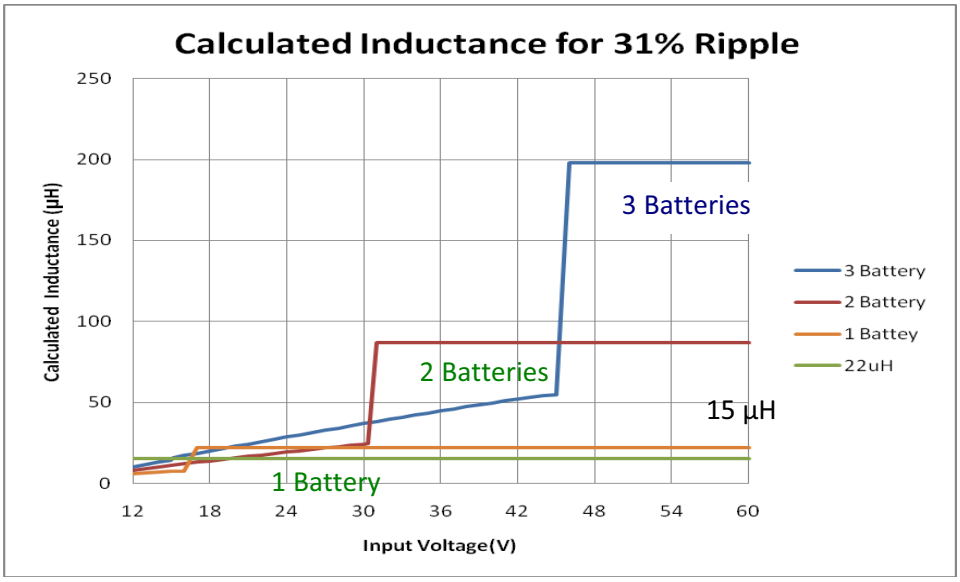


Figure 10. Inductance vs. Current Ripple Ratio

If an inductance of 22 µH is chosen and the converter charges 1 to 3 batteries, the ripple current requirement is satisfied in the buck boost mode; however in the buck mode, the ripple requirement is only met for the case of one battery. The chart below shows the resulting ripple current from the selection of 22 µH.

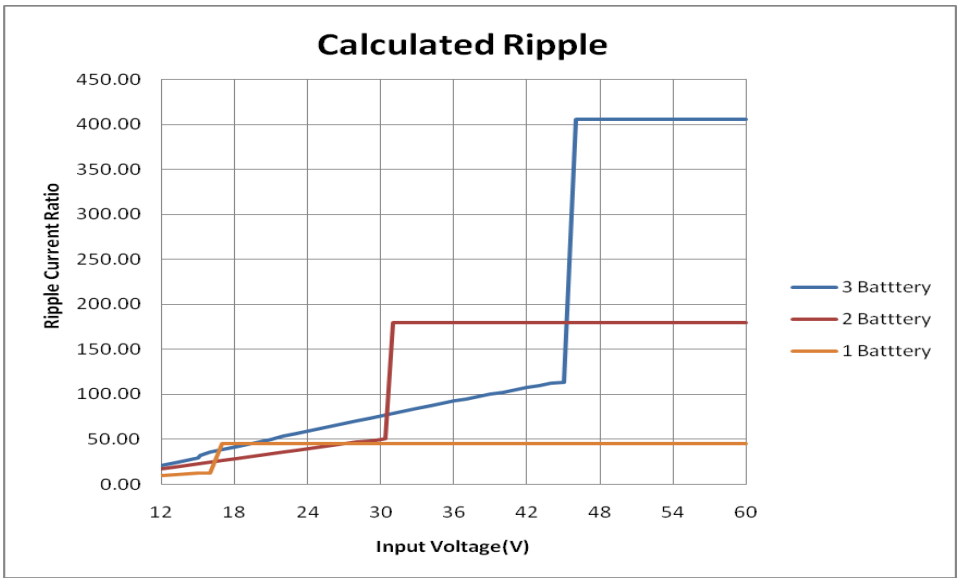


Figure 11. Calculated Ripple Current Ratio with 22□H

When selecting an inductor, the designer must not exceed the current rating of the part. To keep within the bounds of the part's maximum rating, a calculation of the RMS current and peak current are required.

$$I_{DC\_Buck} = I_{OUT} \times \sqrt{1 \times \frac{ra^2}{12}} \rightarrow \quad \text{(eq. 10)}$$

$$10.011\ A = 10\ A \times \sqrt{1 + \frac{30\%^2}{12}}$$

$$I_{DC\_Buck\_Boost} = \frac{I_{OUT}}{1 - D_{BUCK\_Boost}} \rightarrow$$

$$15.63\ A = \frac{10\ A}{1 - 36\%}$$

D_{BUCK_Boost} = Buck boost converter duty cycle ratio
I_{OUT} = Output current
I_{DC_Buck} = Buck converter inductor RMS current

$I_{DC\_Buck\_Boost}$ = Buck boost converter inductor RMS current
ra = Ripple current ratio
D_{BUCK_Boost} = Buck boost converter duty cycle ratio
I_{OUT} = Output current
I_{PK_BUCK} = Buck converter inductor peak current
$I_{PK\_BUCK\_Boost}$ = Buck boost converter inductor peak current
ra = Ripple current ratio

$$I_{PK\_BUCK} = I_{OUT} \times \left(1 + \frac{ra}{2}\right) \rightarrow \quad \text{(eq. 11)}$$

$$11.55\ A = 10\ A \times \left(1 + \frac{31\%}{2}\right)$$

$$I_{PK\_BUCK\_Boost} = \frac{I_{OUT}}{1 - D_{BUCK\_Boost}} \times \left(1 + \frac{ra}{2}\right) \rightarrow$$

$$18.05\ A = \frac{10}{1 - 36\%} \times \left(1 + \frac{31\%}{2}\right)$$

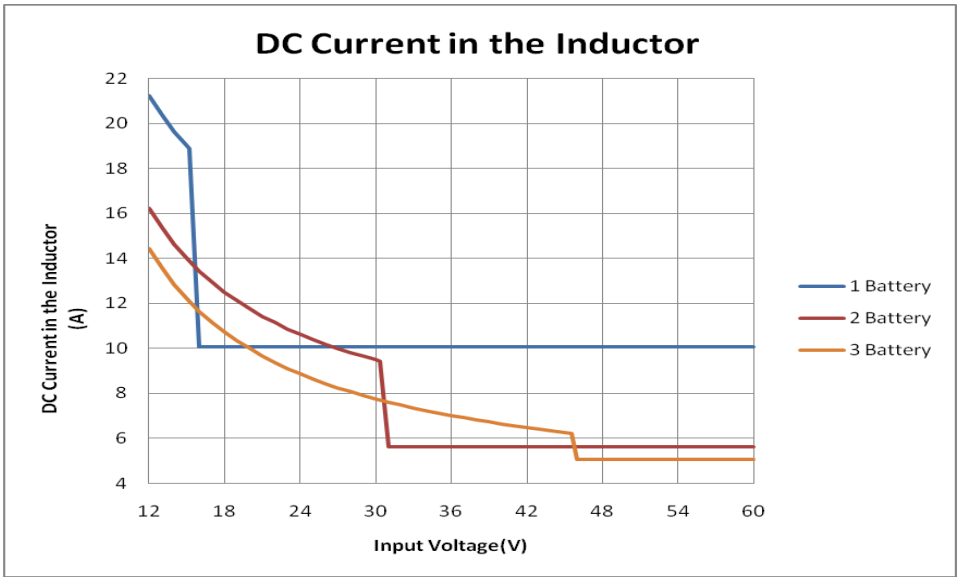


Figure 12. Calculated DC Current in Inductor for Buck Mode and Buck Boost Mode

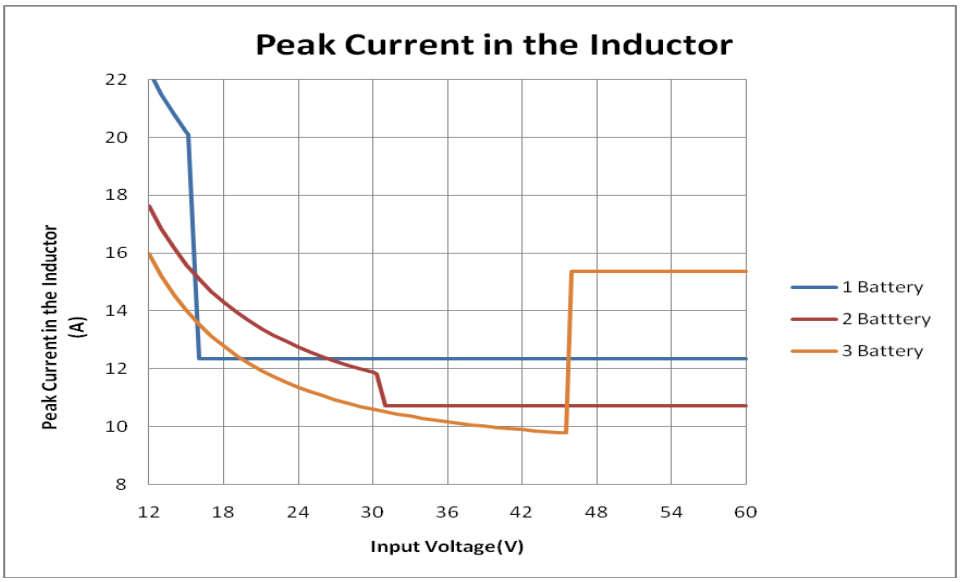


Figure 13. Calculated Peak Current in the Inductor for Buck and Buck Boost Mode

A standard inductor should be found so the inductor will be rounded to 15 μH. The inductor should support an RMS current of 20.5 A and a peak current of 22 A. A good design practice is to select an inductor that has a saturation current that exceeds the maximum current limit with some margin.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space constrained applications. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. The peak−to−peak ripple current for NCP1294 is given by the following equation:

$$I_{pp} = \frac{V_{OUT} \times (1 - D)}{L_{OUT} \times F_{SW}} \rightarrow 1.02\ A = \frac{13.5\ V \times (1 - 56\%)}{22\ \mu H \times 200\ kHz} \quad \text{(eq. 12)}$$

D = Duty ratio
F_{SW} = Switching frequency
I_{pp} = Peak−to−peak current of the inductor
L_{OUT} = Output inductance
V_{OUT} = Output voltage

From Equation 12, it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade−off between dynamic response and ripple current. The power dissipation of an inductor falls into two categories: copper and core losses. Copper losses can be further categorized into DC losses and AC losses. A good first order approximation of the inductor losses can be made using the DC resistance as shown below:

$$LP_{CU\_DCB} = I_{DC\_BUCK}{}^2 \times DCR \rightarrow \quad \text{(eq. 13)}$$
$$260\ mW = 10^2 \times 2.6\ m\Omega$$
$$LP_{CU\_DCB} = I_{DC\_BUCK\_Boost}{}^2 \times DCR \rightarrow$$
$$635.2\ mW = 15.63^2 \times 2.6\ m\Omega$$

DCR = Inductor DC resistance
I_{DC_BUCK} = Buck regulator inductor DC current
$I_{DC\_BUCK\ Boost}$ = Buck boost regulator inductor DC current
LP_{CU_DCB} = Buck inductor DC power dissipation
LP_{CU_DCBB} = Buck boost inductor DC power dissipation

The core losses and AC copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation at which point the total inductor losses can be captured by the equation below:

$$LP_{tot} = LP_{CU\_DC} + LP_{CU\_AC} + LP_{Core} \rightarrow \quad \text{(eq. 14)}$$
$$285\ mW = 260\ mW + 1\ mW + 24\ mW$$

LP_{Core} = Inductor core power dissipation
LP_{CU_AC} = Inductor AC power dissipation
LP_{CU_DC} = Inductor DC power dissipation
LP_{tot} = Total inductor losses

Output Capacitor Selection

The important factors to consider when selecting an output capacitor are DC voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be able to operate properly for the lifetime of a product. When selecting a capacitor, it is important to select a voltage rating that is derated to the guaranteed operating lifetime of a product. Further, it is important to note that when using ceramic capacitors, the capacitance decreases as the voltage applied increases; thus a ceramic capacitor rated at 22 μF 25 V may measure 4.4 μF with an applied voltage of 13.5 V depending on the type of capacitor selected. The output capacitor must be rated to handle the ripple current at full load with proper derating. Since the load is a battery, the question may arise, isn't a battery just like a capacitor? The lead acid battery which is the load is modeled as a voltage source in series with an RC network as shown in Figure 14.

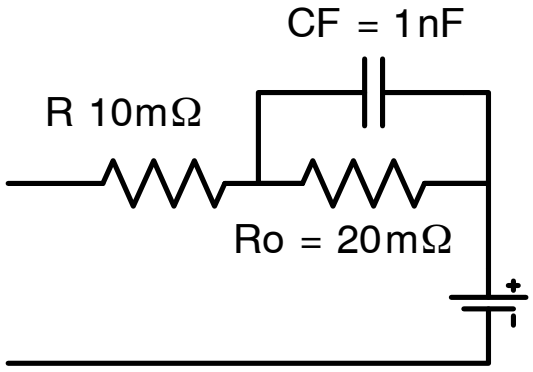


Figure 14. Thevenin Equivalent Battery Model for Lead Acid Battery

The series resistance is very low to begin with; therefore the majority of the pulsed current will go to the battery. The only time the capacitor is needed is when the current flow from the battery decreases towards the end of the absorption stage and in the float stage. Thus a small maintaining capacitance is needed, but ripple voltage and noise are of small concern for this type of battery.

The capacitor RMS ratings given in datasheets are generally for lower switching frequency than used in switch mode power supplies, but a multiplier is given for higher

frequency operation. The RMS current for the output capacitor can be calculated below:

$$CO_{RMS\_BUCK} = I_{OUT}\frac{ra}{\sqrt{12}} \rightarrow 0.294\ A = 10\ A\frac{31\%}{\sqrt{12}} \quad \text{(eq. 15)}$$

$$CO_{RMS-BUCK-Boost} = I_{OUT}\sqrt{\frac{D_{BUCK\_Boost} + \frac{ra^2}{12}}{1 - D_{BUCK\_Boost}}} \rightarrow$$

$$11.54\ A = 10\sqrt{\frac{56\% + \frac{56\%^2}{12}}{1 - 56\%}}$$

Co_{RMS_BUCK} = Buck converter output capacitor RMS current
$Co_{RMS\_BUCK\_Boost}$ = Buck boost converter output capacitor RMS current
D_{BUCK_Boost} = Buck boost converter duty cycle ratio
I_{OUT} = Output current
ra = Ripple current ratio

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize losses and input voltage ripple. The RMS value of the input ripple current is:

$$Iin_{RMS\_Buck} = I_{OUT} \times \sqrt{D_{Buck} \times \left(1 - D_{BUCK}\right)} \rightarrow \quad \text{(eq. 16)}$$

$$1.34\ A = 4.96\ A \times \sqrt{56\% \times (1 - 56\%)}$$

$$Iin_{RMS\_Buck\_Boost} = \frac{I_{OUT}}{1 - D_{Buck\_Boost}}$$

$$\times \sqrt{D_{Buck\_Boost} \times \left[1 - D_{Buck\_Boost} + \frac{ra^2}{12}\right]} \rightarrow$$

$$11.61\ A = \frac{10}{1 - 56\%} \times \sqrt{56\% \times \left[1 - 56\% + \frac{56\%^2}{12}\right]}$$

D = Duty ratio
D_{Buck} = Buck regulator duty cycle ratio
D_{Buck_Boost} = Buck boost regulator duty cycle ratio
Iin_{RMS_Buck} = Buck input capacitance RMS current
$Iin_{RMS\_Buck\_Boost}$ = Buck boost input capacitance RMS current
I_{OUT} = Load current

The equation reaches its maximum value with D = 0.5 at which point the input capacitance RMS current is half the output current. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = CIN_{ESR} \times \left(Iin_{RMS}\right)^2 \rightarrow \quad \text{(eq. 17)}$$

$$246\ mW = 10\ m\Omega \times \left(4.96\ A\right)^2$$

CIN_{ESR} = Input capacitance Equivalent Series Resistance
Iin_{RMS} = Input capacitance RMS current
P_{CIN} = Power loss in the input capacitor

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum capacitor must be used, it must be surge protected, otherwise capacitor failure could occur.

Power MOSFET Dissipation

Power dissipation, package size, and the thermal environment drive power supply design. Once the dissipation is known, the thermal impedance can be calculated to prevent the specified maximum junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The high−side MOSFET will display both switching and conduction losses. The switching losses of the low side MOSFET will not be calculated as it switches into nearly zero voltage and the losses are insignificant. However, the body diode in the low−side MOSFET will suffer diode losses during the non−overlap time of the gate drivers. Starting with the high−side buck and boost MOSFET, the power dissipation can be approximated from the following equation:

$$P_{D\_HS} = P_{COND} + P_{SW\_TOT} \quad \text{(eq. 18)}$$

P_{COND} = Conduction losses
P_{D_HS} = Power losses in the high side MOSFET
P_{SW_TOT} = Total switching losses

Using the ra term from Equation 8, I_{RMS} becomes:

$$I_{RMS\_BUCK} = I_{OUT} \times \sqrt{D \times \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 19)}$$

$$I_{RMS\_BUCK\_Boost} = \frac{I_{OUT}}{1 - D} \times \sqrt{D \times \left(1 + \frac{ra^2}{12}\right)}$$

D_{BUCK} = Buck duty ratio
D_{BUCK_Boost} = Buck boost duty ratio
ra = Ripple current ratio
I_{OUT} = Output current
I_{RMS_BUCK} = Buck high side MOSFET RMS current
$I_{RMS\_BUCK\_Boost}$ = Buck boost high side MOSFET RMS current

The first term in Equation 18 is the conduction loss of the high−side MOSFET while it is on. Since the low side MOSFET is on at the same time as the boost MOSFET the conduction loss can be approximated the same.

$$P_{COND\_BUCK} = \left(I_{RMS\_HS\_BUCK}\right)^2 \times R_{DS(on)} \quad \text{(eq. 20)}$$

$$P_{RMS\_BUCK\_Boost} = \left(I_{RMS\_HS\_BUCK\_Boost}\right)^2 \times R_{DS(on)}$$

$I_{RMS\_HS\_BUCK}$ = Buck RMS current in the high side MOSFET
$I_{RMS\_HS\_BUCK\_Boost}$ = Buck boost RMS current in the high side MOSFET
P_{COND_BUCK} = Buck conduction power losses
$P_{COND\_BUCK\_Boost}$ = Buck boost conduction power losses
$R_{DS(ON)}$ = On resistance of the high side MOSFET

The second term from Equation 18 is the total switching loss and can be approximated from the following equations.

$$P_{SW\_TOT} = P_{SW} + P_{DS} + P_{RR} \quad \text{(eq. 21)}$$

P_{DS} = High side MOSFET drain to source losses
P_{RR} = High side MOSFET reverse recovery losses
P_{SW} = High side MOSFET switching losses
P_{SW_TOT} = High side MOSFET total switching losses

The first term for total switching losses from Equation 21 are the losses associated with turning the high−side MOSFET on and off and the corresponding overlap in drain voltage and current.

$$P_{SW\_BUCK} = P_{TON} + P_{TOFF} = \frac{1}{2} \times \left(I_{OUT} \times V_{IN} \times F_{SW}\right) \times \left(t_{RISE} + t_{FALL}\right) \quad \text{(eq. 22)}$$

$$P_{SW\_BUCK\_Boost} = P_{TON} + P_{TOFF} = \frac{1}{2} \times \left(\frac{I_{OUT}}{1 - D} \times V_{IN} \times F_{SW}\right) \times \left(t_{RISE} + t_{FALL}\right)$$

F_{SW} = Switching frequency
I_{OUT} = Load current
P_{SW_BUCK} = Buck high side MOSFET switching losses
$P_{SW\_BUCK\_Boost}$ = Buck boost high side MOSFET switching losses
P_{TON} = Turn on power losses
P_{TOFF} = Turn off power losses
t_{FALL} = MOSFET fall time
t_{RISE} = MOSFET rise time
V_{IN} = Input voltage

When calculating the rise time and fall time of the high side MOSFET it is important to know the charge characteristic shown in Figure 15.

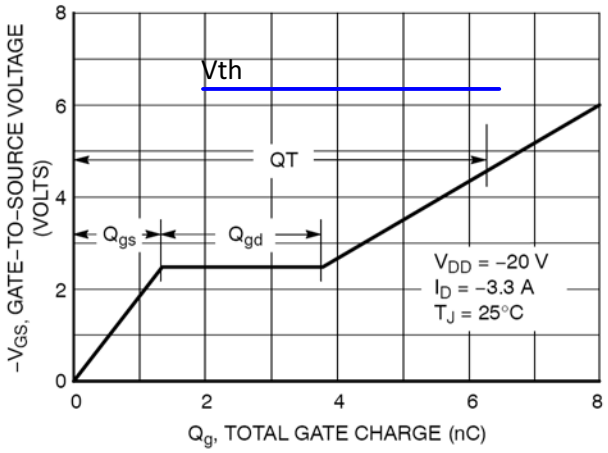


Figure 15. High Side MOSFET Total Charge

$$t_{RISE} = \frac{Q_{GD}}{I_{G1}} = \frac{Q_{GD}}{\left(V_{BST} - V_{TH}\right)/\left(R_{HSPU} + R_G\right)} \quad \text{(eq. 23)}$$

I_{G1} = Output current from the high−side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_{HSPU} = Drive pull up resistance
R_G = MOSFET gate resistance
t_{RISE} = MOSFET rise time
V_{BST} = Boost voltage
V_{TH} = MOSFET gate threshold voltage

$$t_{FALL} = \frac{Q_{GD}}{I_{G2}} = \frac{Q_{GD}}{\left(V_{BST} - V_{TH}\right)/\left(R_{HSPD} + R_G\right)} \quad \text{(eq. 24)}$$

I_{G12} = Output current from the low−side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_G = MOSFET gate resistance
R_{HSPD} = Drive pull down resistance
t_{FALL} = MOSFET fall time
V_{BST} = Boost voltage
V_{TH} = MOSFET gate threshold voltage

Next, the MOSFET output capacitance losses are caused by both the high−side and low−side MOSFETs, but are dissipated only in the high−side MOSFET.

$$P_{DS} = \frac{1}{2} \cdot C_{OSS} \times V_{IN}{}^2 \times F_{SW} \quad \text{(eq. 25)}$$

C_{OSS} = MOSFET output capacitance at 0 V
F_{SW} = Switching frequency
P_{DS} = MOSFET drain to source charge losses
V_{IN} = Input voltage

Finally, the loss due to the reverse recovery time of the body diode in the low−side MOSFET is calculated as follows:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot F_{SW} \quad \text{(eq. 26)}$$

F_{SW} = Switching frequency
P_{RR} = High side MOSFET reverse recovery losses
Q_{RR} = Reverse recovery charge
V_{IN} = Input voltage

The NCP1294 demonstration board is setup to use either a non synchronous or synchronous buck stage depending on the user's needs. If a synchronous buck is required, the calculations and explanation for the dissipation are as follows. The low−side MOSFET turns on into small negative voltages so switching losses are negligible. The low−side MOSFET's power dissipation only consists of conduction loss due to $R_{DS(on)}$ and body diode loss during non−overlap periods. If a non synchronous design is used P conduction goes to zero and P_{BODY} becomes P_{DIODE}.

$$P_{D\_LS} = P_{COND} + P_{BODY} \quad \text{(eq. 27)}$$

P_{BODY} = Low side MOSFET body diode losses
P_{COND} = Low side MOSFET conduction losses
P_{D_LS} = Low side MOSFET losses

Conduction loss in the low−side MOSFET is calculated as follows:

$$P_{COND} = \left(I_{RMS\_LS}\right)^2 \times R_{DS(on)\_LS} \quad \text{(eq. 28)}$$

I_{RMS_LS} = RMS current in the low side
$R_{DS(ON)\_LS}$ = Low−side MOSFET on resistance
P_{COND} = High side MOSFET conduction losses

$$I_{RMS\_LS} = I_{OUT} \cdot \sqrt{\left(1 - D_{BUCK}\right) \times \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 29)}$$

D_{BUCK} = Buck duty ratio
I_{OUT} = Load current
I_{RMS_LS} = RMS current in the low side
ra = Ripple current ratio

The body diode losses can be approximated as:

$$P_{BODY} = V_{FD} \times I_{OUT} \times F_{SW} \times \left(NOL_{LH} + NOL_{HL}\right) \quad \text{(eq. 30)}$$

F_{SW} = Switching frequency
I_{OUT} = Load current
NOL_{HL} = Dead time between the high−side MOSFET turning off and the low−side MOSFET turning on
NOL_{LH} = Dead time between the low−side MOSFET turning off and the high−side MOSFET turning on
P_{BODY} = Low−side MOSFET body diode losses
V_{FD} = Body diode forward voltage drop

Compensation Network

To create a stable power supply, the compensation network around the error amplifier must be used in conjunction with the PWM generator and the power stage. Since the power stage design criteria is set by the application, the compensation network must correct the overall output to ensure stability. The NCP1294 is a voltage mode voltage feed forward part and as such there exists a voltage loop with an input voltage modified ramp. The output inductor and capacitor of the power stage form a double pole and the loop must compensate for that.

The ESR of the output capacitor creates a "zero" at the frequency as shown in Equation 31:

$$FZ_{ESR} = \frac{1}{2\pi \times CO_{ESR} \times C_{OUT}} \rightarrow$$
$$24.87\ kHz = \frac{1}{2\pi \times 0.010\ m\Omega \times 640\ \mu F} \rightarrow \quad \text{(eq. 31)}$$

CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitor
FZ_{ESR} = Output capacitor zero ESR frequency

The frequency of the double pole varies for both a buck and a buck boost, they can be calculated as shown below:

$$FZ_{P\_BUCK} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \rightarrow$$
$$1.34\ kHz = \frac{1}{2\pi \times \sqrt{22\ \mu H \times 640\ \mu F}} \rightarrow \quad \text{(eq. 32)}$$

$$FZ_{P\_BUCK} = \frac{1 - D_{BUCK\_Boost}}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \rightarrow$$
$$590\ Hz = \frac{1 - 47\%}{2\pi \times \sqrt{22\ \mu H \times 640\ \mu F}} \rightarrow$$

C_{OUT} = Output capacitor
D_{BUCK_Boost} = Buck boost duty ratio
F_{P_BUCK} = Buck double pole frequency
$F_{P\_BUCK\_Boost}$ = Buck boost double pole frequency
L_{OUT} = Output inductance

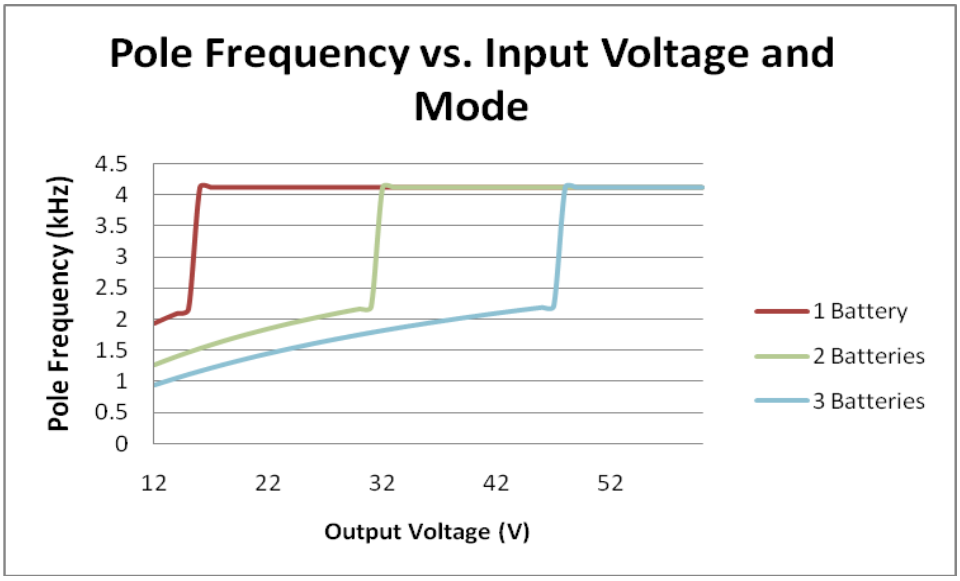


Figure 16. Pole Frequency vs. Input Voltage and Mode

The right half plane zero for the buck boost converter can be calculated with the following equation.

$$FZ_{RHPZ\_BUCK\_Boost} = \frac{V_{IN}^{\ 2}}{2\pi \times (V_{OUT} + V_{IN}) \times L_{OUT} \times I_{OUT}} \rightarrow$$

$$7.71\ kHz = \frac{13.5\ V^2}{2\pi \times (13.5\ V + 17) \times 22\ \mu H \times 8.89\ A} \quad \text{(eq. 33)}$$

$F_{RHPZ\_BUCK\_Boost}$ = Right half plane zero
I_{OUT} = Output current
L_{OUT} = Output inductance
V_{IN} = Input Voltage
V_{OUT} = Output Voltage

The key is to compensating a combination buck and buck boost converter is to know where the RHPZ is and how it changes with load as is defined by the equation above. The RHPZ is at its lowest point when the load is the highest, for this application that occurs with one battery and when the output voltage is at its lowest, as it is a squared term. The input voltage at its highest voltage will also yield the lowest RHPZ as shown in the figure below. Note that when the converter switches to buck mode, RHPZ does not exist, thus in the figure, buck mode is shown as 1 MHz RHPZ although it is understood that it does not exist.

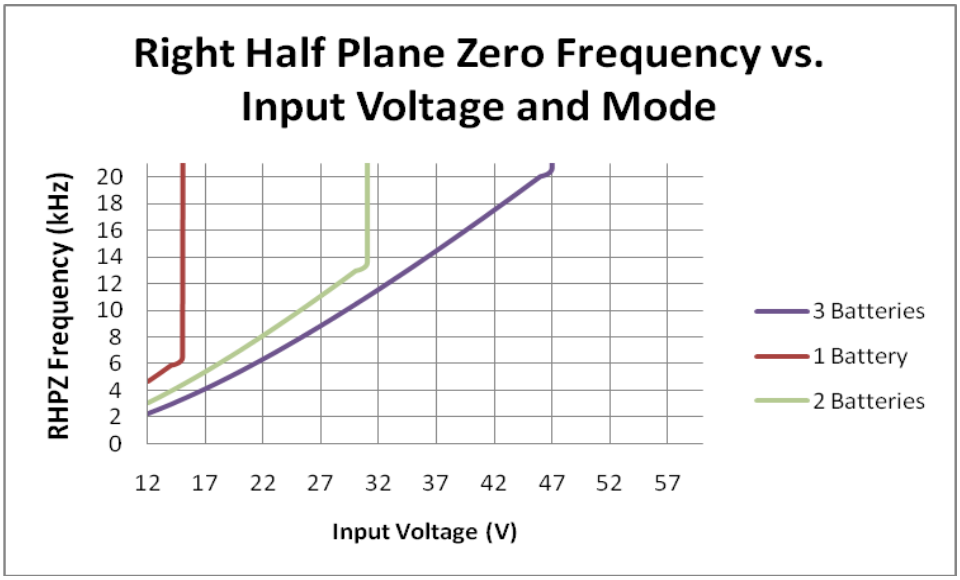


Figure 17. Right Half Plane Zero Frequency

The three equations above define the bode plot that the power stage has created or open loop response of the system. The next step is to close the loop by considering the feedback values. The closed loop crossover frequency should be less than 1/10 of the switching frequency. The designer must balance a high crossover frequency with crossing over a decade before the RHPZ, thus the designer must determine which frequency is lower. In this application the lowest RHPZ is at 6.721 kHz, therefore the crossover frequency will be set to 1.5 kHz. Figure 18 shows type III error amplifier compensation to make the loop stable. Only the type III compensation is shown as type II and type I are a subset.

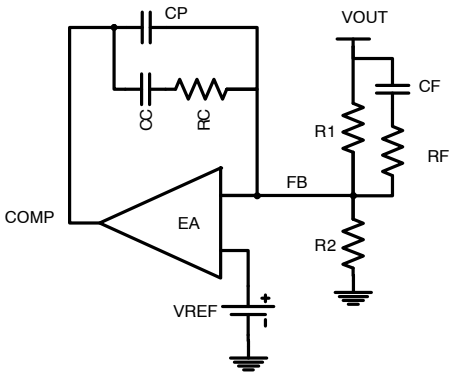


Figure 18. Type III Error Amplifier Configuration

The compensation network consists of the internal error amplifier and the impedance networks. The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response and the highest gain in DC conditions to minimize load regulation issues. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst−case component variations when determining phase margin. To start the design, a resistor value should be chosen for R1 from which all other components can be chosen. A good starting value is 100 kΩ.

The NCP1294 allows the output of the DC−DC regulator to be adjusted down to 1.263 V via an external resistor divider network. The regulator will maintain 1.263 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the regulator will regulate the output voltage proportional to the resistor divider network in order to maintain 1.263 V at the FB pin.

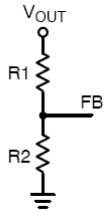


Figure 19. Feedback Resistor Divider

The relationship between the resistor divider network above and the output voltage is shown in Equation 34:

$$R_2 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right) \quad \text{(eq. 34)}$$

R1 = Top resistor divider
R2 = Bottom resistor divider
V_{OUT} = Output voltage
V_{REF} = Regulator reference voltage

The most frequently used output voltages and their associated standard R_1 and R_2 values are listed in Table 3.

Table 3. OUTPUT VOLTAGE SETTINGS

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
13.5	100	10.2
27	100	4.87
40.5	100	3.24

The compensation components for the Type III error amplifier can be calculated using the method described below. The method serves to provide a good starting place for compensation of a power supply. The values can be adjusted in real time using the compensation tool CompCalc for the buck portion of the converter but must be checked in the application
http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP

The integrator for the operation amplifier is set as follows. The designer should set the voltage feed forward resistor to the same value as R1 so that the two values cancel out:

$$C1 = \frac{V_{IN}}{2\pi * Vramp * Fcross} \rightarrow \frac{V_{IN} * R * C * F_{sw}}{2\pi * V_{IN} * D * Fcross * R1} \rightarrow \frac{R * C * F_{sw}}{2\pi * D * Fcross * R1} \quad \text{(eq. 35)}$$

$$41.2\ nF = \frac{100\ k\Omega * 1.5\ nF * 200\ kHz}{2\pi * 89\% * 1.3\ kHz * 100\ k\Omega}$$

C = Feed forward capacitor
C1 = Compensation capacitor
D = Maximum duty cycle of the converter
F_{SW} = Switching frequency
Fcross = Crossover frequency
R = Feed forward resistor
R1 = Upper resistor divider
V_{IN} = Input Voltage
Vramp = Ramp Voltage

The pole frequency for C1 and R1 should now be calculated.

$$FPO = \frac{1}{2\pi * C1 * R1} \quad \text{(eq. 36)}$$

$$38.56\ Hz = \frac{1}{2\pi * 41.26\ nF * 100\ k\Omega}$$

C1 = Compensation capacitor
FPO = Pole frequency
R1 = Upper resistor divider

The zero should be placed at the double pole of the plant.

$$C2 = \frac{1}{4\pi R1}\left(\frac{1}{FP_{\_BUCK}} - \frac{1}{FZ_{ESR}}\right) \rightarrow \quad \text{(eq. 37)}$$

$$2.175\ nF = \frac{1}{2\pi * 100\ k\Omega}\left(\frac{1}{20\ Hz} - \frac{1}{24.87\ kHz}\right)$$

C2 = Compensation capacitor
$F_{P\_BUCK\_Boost}$ = Double pole frequency of buck boost converter
FZ_{ESR} = ESR frequency
R1 = Upper resistor divider

$$R2 = R1\frac{FPO}{F_{P\_BUCK\_Boost}} \rightarrow 5.425\ k\Omega = 100\ k\Omega\frac{38.567\ Hz}{710.9\ Hz} \quad \text{(eq. 38)}$$

F_{P_BUCK} = Double pole frequency of buck converter
$F_{P\_BUCK\_Boost}$ = Double pole frequency of buck boost converter

FPO = Pole frequency of R1 and C1
R1 = Upper resistor divider
R2 = Resistor

$$C_3 = \frac{1}{2\pi \times (R2 * Fcross - R1 * FPO)}$$

$$49.796\ nF = \frac{1}{2\pi \times (5.425\ k\Omega * 1.3\ kHz - 100\ k\Omega * 38.567\ Hz)} \quad \text{(eq. 39)}$$

C_3 = Compensation pole capacitor
Fcross = Crossover frequency
FPO = Pole frequency of R1 and C1
R1 = Upper resistor divider
R2 = Resistor

If the ESR frequency is greater than the switching frequency, a CF compensation capacitor may be needed for stability as the output LC filter is considered high Q and thus will not give the phase boost at the crossover frequency.

$$R3 = \frac{R1 * F_{BUCK\_Boost}}{FZ_{ESR} - F_{P\_BUCK\_Boost}} \rightarrow$$

$$2.943\ k\Omega = \frac{100\ k\Omega * 710\ Hz}{24.87\ kHz - 710\ Hz} \quad \text{(eq. 40)}$$

C_P = Compensation pole capacitor
F_{cross} = Cross over frequency
$F_{P\_BUCK\_Boost}$ = Double pole frequency of buck boost converter
FZ_{ESR} = ESR frequency

System Turn On and Battery Current Draw

The system being created is connected to two finite sources that will supply power to the load at different times of the day and will more than likely not work at the same time except for brief periods. The system is not complete without both the battery and the solar panel installed therefore, detection of the presence of the battery load and the solar panel source are advantageous. For instance it would not be good to dissipate solar panel energy in providing battery voltage if no battery is connected. If a solar panel is connected, the battery would be drained looking for a solar panel to be connected. A simple solution for checking that both the solar panel is connected and the battery is connected is a low current draw comparator. Q1 serves as the comparator and checks to determine if there is a voltage greater than the base−emitter saturation voltage. If the resistor divided solar panel voltage is greater than the VBE(sat) of the NPN transistor, then Q1 becomes saturated and opens Q2, allowing voltage into power the other circuits. If a battery is not provided, none of the circuitry turns on. If a battery is detected and no solar panel is installed, Q2 remains off as does the circuitry. The solar panel detection circuit should be set low so it does not interfere with the operation of the MPPT.

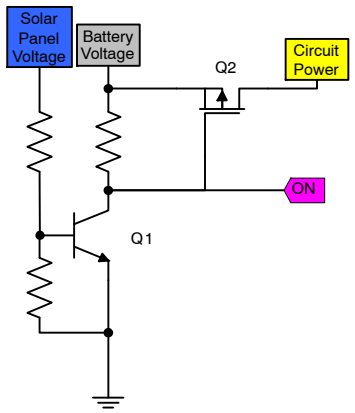


Figure 20. Dual Solar Panel Battery Detection Circuit

The circuit power comes directly from the output battery and the intention of system is to be easily adaptable to a single battery 12 V, dual battery 24 V, or triple battery 36 V system. Therefore it is necessary to provide a dependable voltage to the measurement and switching circuitry. In this application the MC78L08 is used and will provide a steady 8 V supply while handling as much as 40 V.

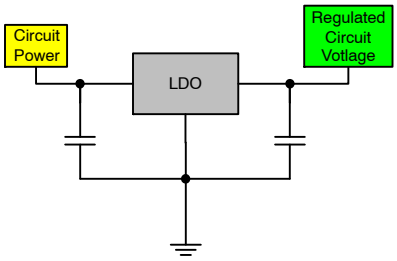


Figure 21. LDO Circuit

The system charges batteries during the day time and discharges them during the night to illuminate a defined space. The input energy is not guaranteed, but the output energy remains constant over a long period of time. If a system is not sized properly, the discharge of the battery can result in damage. To stop the battery from being damaged, the LED circuit must be inhibited from operation if the battery is depleted. The circuit below uses a TL431 to monitor the battery voltage and provides an enable disable signal to the LEDs when the battery is below the cutoff voltage. If the R1 and R2 battery divided voltage is less than 2.5 V, D1 does not pull down on R3. R3 provides greater than the MOSFET threshold voltage to Q1 giving the LED a disable signal. Conversely, if the R1 and R2 battery divided voltage is greater than 2.5 V, D2 pulls down on R3 and Q1 is turned off, pulling up on the LED enable signal. Further, the circuit in the figure below is linked to the battery and solar panel detection circuit. The ON node connection detects daylight and disables the LED string to prevent operation of the LEDs while the solar panel is charging the batteries.

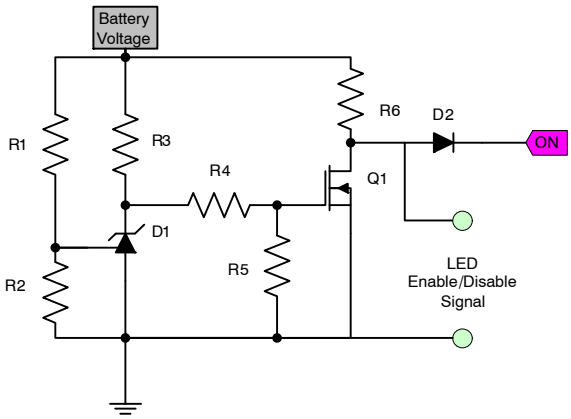


Figure 22. Battery Discharge and Daylight Detection Circuit

Input and Output Current Measurements

To implement battery charging and MPPT it is important to sense the input output currents to control the power into and out of the charger. The simplest method of current sense is low side sensing where the current running in the return path is sensed by an amplifier as shown in Figure 23.

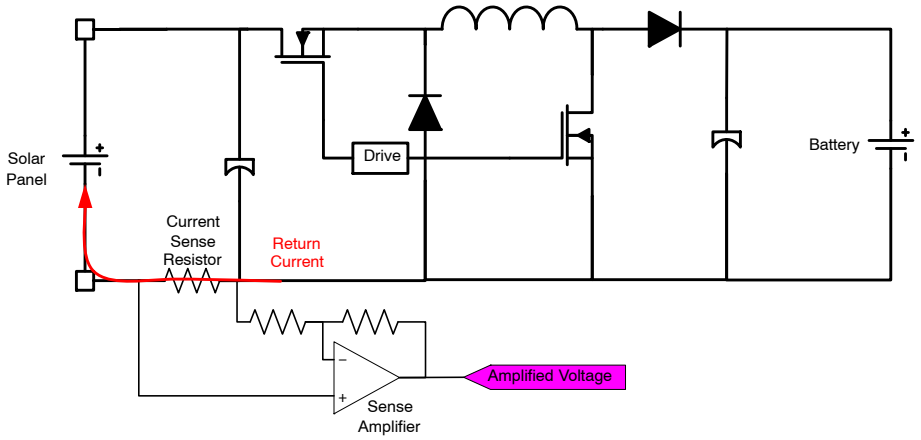


Figure 23. Low Side Amplifier Current Sensing

The issue with low side sensing is that the solar controller being produced may be configured in a system with many other solar controllers and the installer may want to employ central grounding which will defeat the current sense employed by diverting the current from the sense resistor in part or in full. The current sensed by the amplifier then becomes small in comparison with the actual current being drawn from the device. While low side current sense is easy to implement and can be executed inexpensively, it may not provide a positive user experience as the controller will cease to function properly when installed by different users. Figure 24 shows central grounding and how it can affect the sensed current in low side sensing.

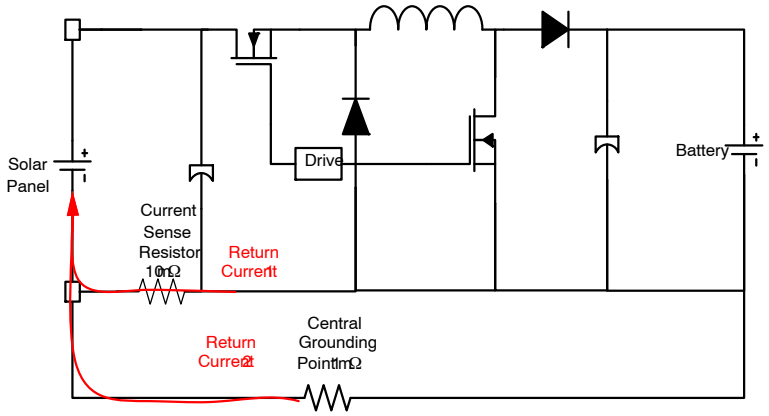


Figure 24. Central Grounding Diagram

Implementing high side current sensing allows common point grounding as the ground path current does not affect this sensing. Unfortunately the operation amplifier chosen must have a wide common mode input range. The amplifier chosen must work at high input voltages and the complexity of the circuit increases.

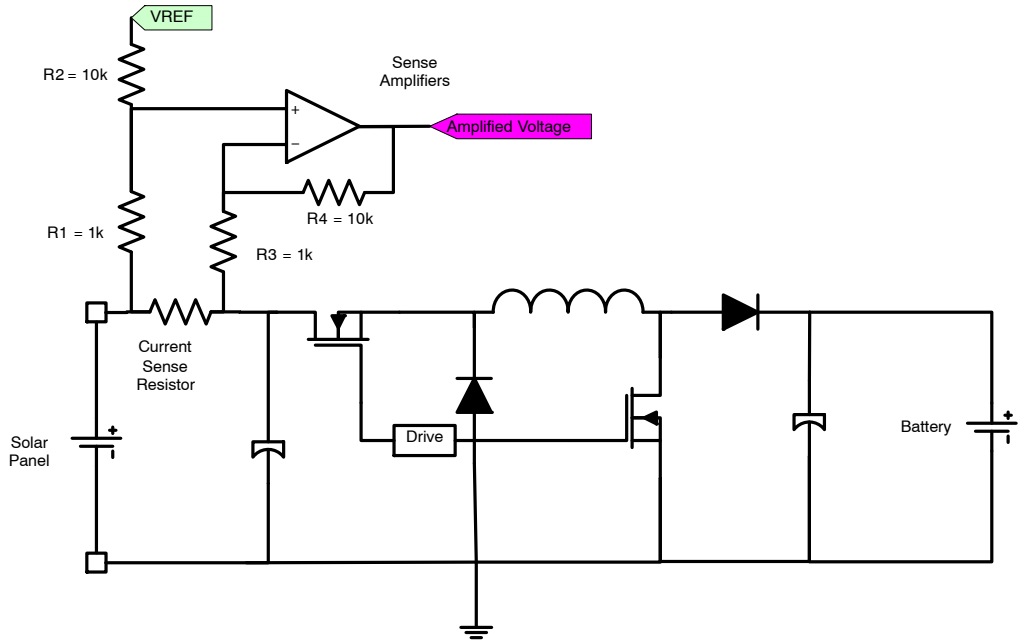


Figure 25. Amplifier High Side Current Sensing

Since the primary aim of the system is making a cost effective solution, the designer should aim to implement the solution minimizing current consumption and maximizing accuracy. One cost effective way to sense high side current is to use current mirrors to mirror the voltage to ground level. The simplest current mirror to use is a Windlar, which is handicapped by the Early effect and the current differs by a multiple of 2 of the base current. The next current mirror considered is the Wilson current mirror, which has relatively good current parity. The only problem with the Wilson current mirror is that the number of transistors doubles from 4 to 8, making it unattractive from a cost and circuit management perspective.

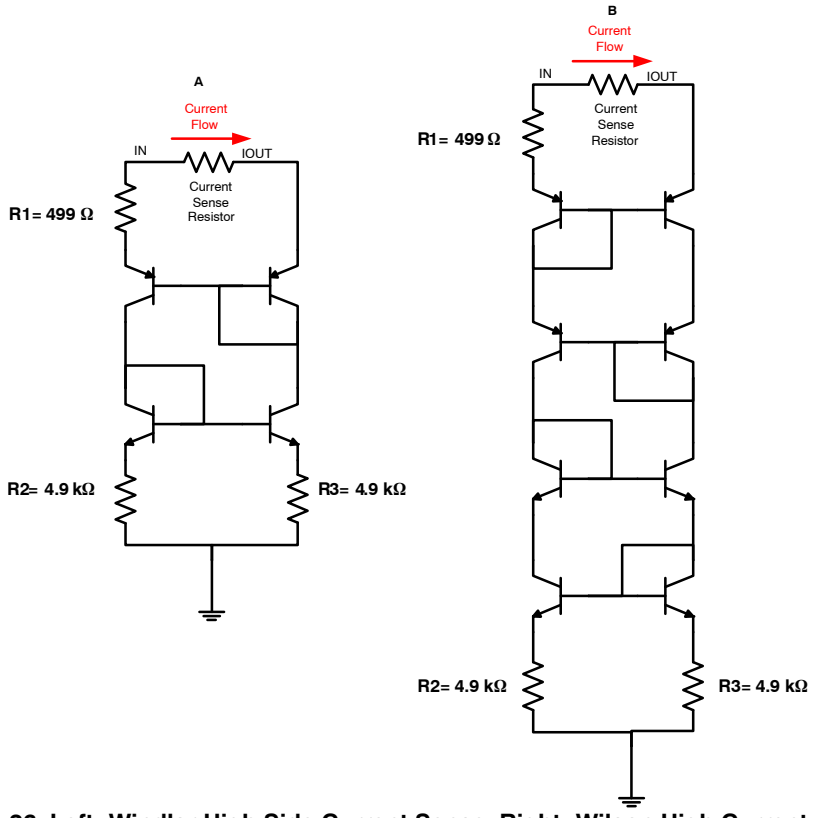


Figure 26. Left: Windlar High Side Current Sense, Right: Wilson High Current Sense

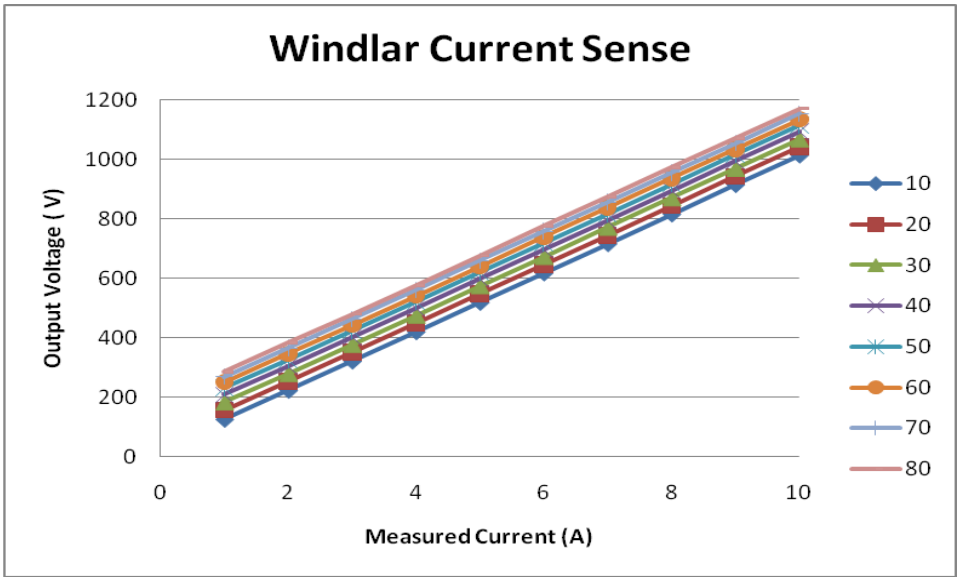


Figure 27. Simulated Accuracy of the Windlar Current Sense

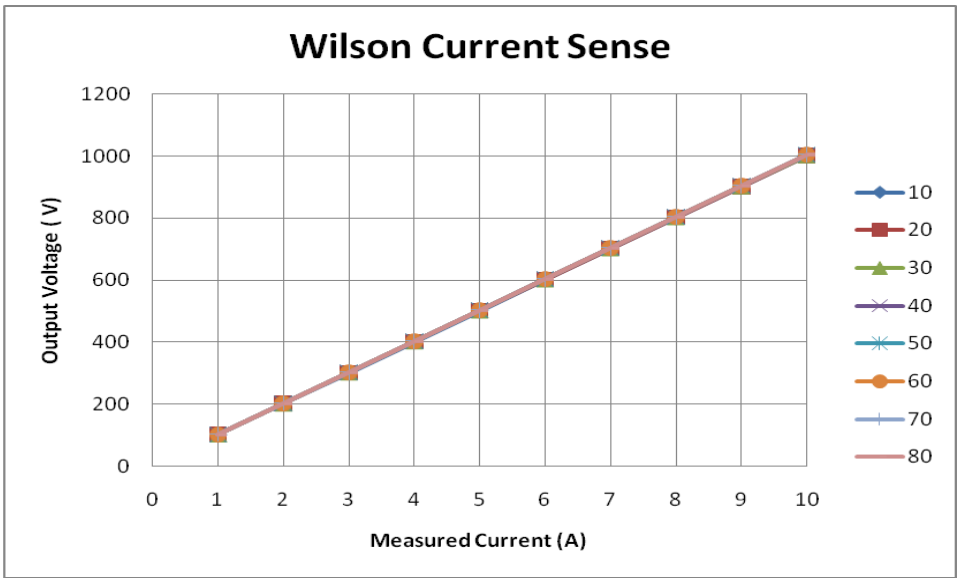


Figure 28. Simulated Accuracy of the Wilson Current Sense

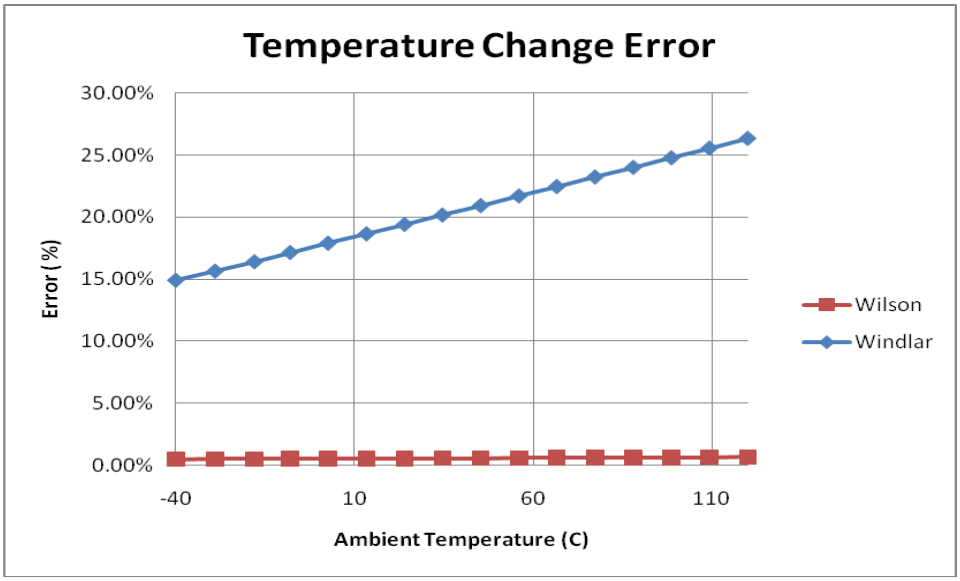


Figure 29. Temperature Error of Windlar and Wilson Current Senses

With the error introduced by the Windlar current sense, it may first appear that this current sense is not useful, but if a relative current level is desired, the circuit may still be useful. For most MPPT algorithms the maxima of a voltage multiplied by a current is desired. If the current measurement changes with voltage, the maximum is found but perhaps not the optimal maximum depending on how the algorithm is setup. While not the best solution, it may be good enough for the cost target. If a small output voltage range is considered, such as the one to a single battery which varies from 10 V to 15 V, the variation of the Windlar may be fine but the designer must decide if cost or precision is more important. The designer must also consider the speed at which the answer is required. The Wilson current mirror while accurate had a delay from 500 ns to 2 μs depending on bias currents where the Windlar had less than 200 ns.

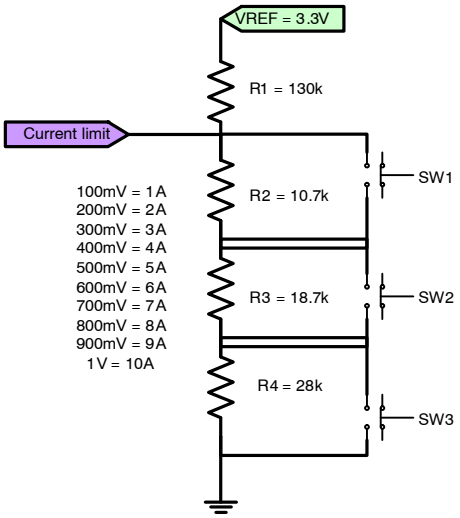


Figure 30. Output Charge Rate Programming

Input and Output Current Balancing

When building an ideal solar controller, the controller should protect the batteries or load while extracting the maximum energy from the solar panels. Unfortunately in the real world a customer or installer may purchase a large solar panel and a small battery. If the solar controller were to charge at the peak power, the battery would charge too fast and the lifetime of the battery would degrade or an explosion could occur. What the controller should do is to manage the needs of the battery and balance them with the peak power supplied from the solar panel. Thus a maximum battery charge rate programming as well as a voting scheme is needed to determine what is limiting the current out of the system. The programming of the current is accomplished via a 3.3 V reference provided by the NCP1294 and a resistor divider network. The shorting of one or multiple headers will result in a different current limit shown below where 100 mV is 1 A.

1		Short	
0		Open	
s1	s2	s3	Programmed Current
1	1	1	0.00
0	1	1	2.51
1	0	1	4.15
1	1	0	5.85
0	0	1	6.09
0	1	0	7.57
1	0	0	8.72
0	0	0	10.11

The user programmed set current is compared to the measured output current of the system and an error signal is produced. The error signal results in the voltage level set of the pulse by pulse current limiter. Likewise, the MPPT finds the maximum power point and sets the pulse by pulse current limiter for achieving the maximum power point. The lowest current set point should govern the system and the two signals will fight for dominance. If the two designs are merged into series regulators they can coexist. If a regulator is not able to achieve its intended higher current, it will keep opening the pass MOSFET until it is fully on and the other MOSFET will regulate the current.

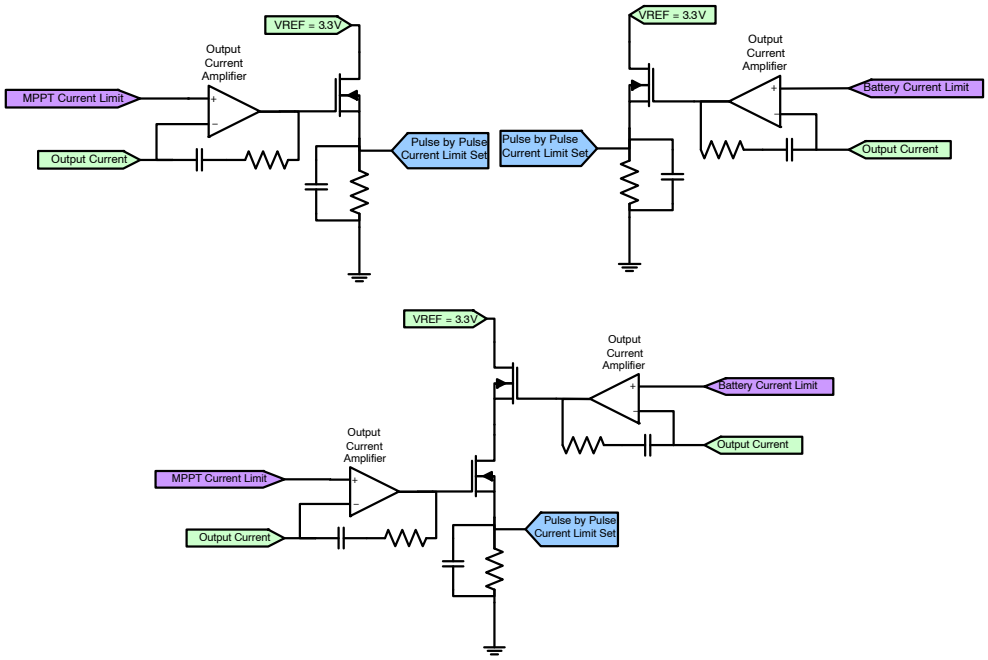


Figure 31. Voting Scheme

The operation of the circuit is shown graphically below where the maximum charge rate of the battery is set below the MPPT of the solar panel and the system tradeoff between charging at the maximum battery charge rate and the maximum power point is achieved.

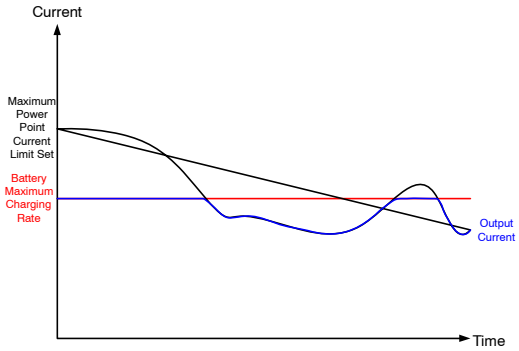


Figure 32. Battery Charging Between MPPT and Maximum Charge Rate

Solar Panel Connection Transients

When connecting a solar panel to a solar controller, load voltage transient can occur and a designer must take action to protect the power supply from large transients. The voltage transients shown below for the panel described are about 14% above Voc.

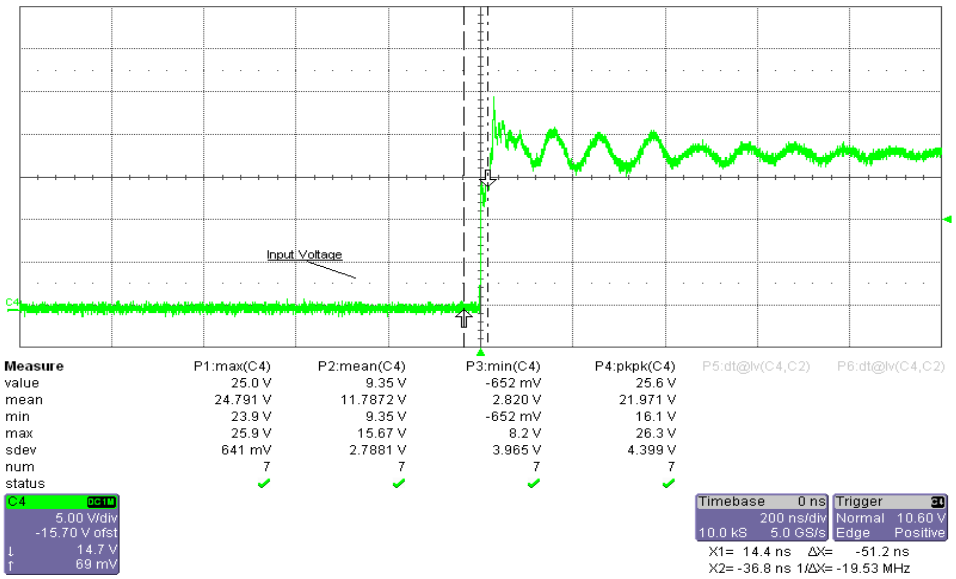


Figure 33. Crystal Solar Panel Connection to a 10 kΩ Resistive Load Positive Terminal Connected Last

Voltage transients can be minimized in some of the following ways: suppression, filtering, or tolerating. If the designer chooses to suppress the transients, the power dissipated to suppress the transient must be calculated. The inductance of the connection wires can be calculated for a pair of wires as long d > 5*a using the following equation:

$$L = \frac{\mu_O * l}{4\pi} * \left(1 + 4 * \ln\left(\frac{d - a}{a}\right)\right) \qquad \text{(eq. 41)}$$

$$3.95\ \mu H = \frac{4\pi * 10^{-7}\frac{H}{m} * 9m}{4\pi} * \left(1 + 4 * \ln\left(\frac{7.5\ mm - 1.5\ mm}{1.5\ mm}\right)\right)$$

a = Wire radius
d = Wire (center) distance
l = Length of wire
L = Wire inductance
μ_o = 4πx10−7

The energy delivered to the load from the wire inductance is 1/2LI^2. The current delivered to the load will be at maximum short circuit current or Isc. From the scope capture shown in Figure 34, the transients do not last longer than 1 μs, thus the power dissipation needed for the transient voltage suppressor can be calculated as shown below:

$$E = \frac{\frac{1}{2} * L * Isc^2}{TR_{Time}} \rightarrow 34.8\ W = \frac{\frac{1}{2} * 3.95\ \mu H * (4\ A)^2}{1\ \mu s} \qquad \text{(eq. 42)}$$

E = Energy
Isc = Short circuit current
L = Wire inductance
TR_{Time} = Transient rise time

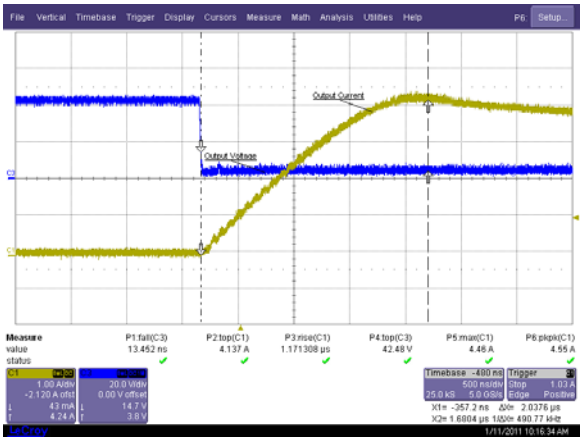


Figure 34. Short Circuit Response of the Wurth Solar panel

The proper part can be selected by looking at the pulse rating curve for the voltage suppressor. An example pulse rating curve is shown in Figure 35.

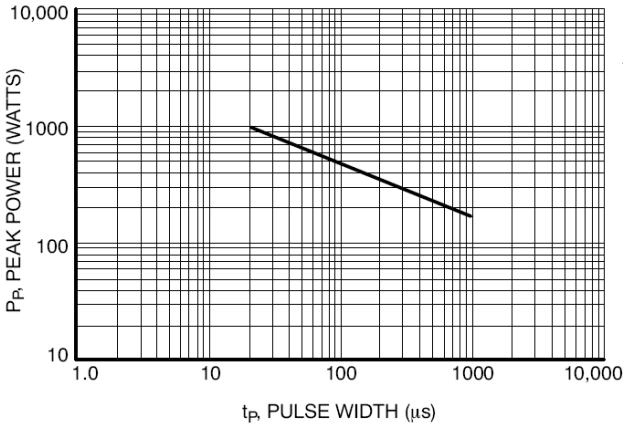


Figure 35. Pulse Rating Curve for the SMF5.0AT1 Series [5]

The amplitude of the voltage spike can be estimated by using v = l*di/dt. Assuming the inductance calculated above and the current is Isc, the remaining value to be obtained is the dt. The rise time of the current will vary with the technology, irradiance, and temperature of the solar panel and the wire inductance, but the reaction time of the Wurth solar panel with nine meters of wire connected is shown in Figure 34 and is less than 2 μs.

$$V_{Spike} = \frac{L * \Delta I}{\Delta t} \rightarrow 8.3\ V = \frac{3.95\ \mu H * 4.2\ A - 0\ A}{2\ \mu s} \quad \text{(eq. 43)}$$

ΔI = Change in current
L = Wire inductance
Δt = Time
V_{Spike} = Resulting line spike

Since the transients seen on the input are short in duration, a filter can be used to reduce the amplitude of the voltage that the rest of the system will see. The worst case scenario is that the input system is charged up to the open circuit voltage of the solar panel with no load applied when the transient pulses are applied. According to [6] the voltage the system will be subjected to can be approximated by using the diagram shown in Figure 36 and equations below.

$$a = \frac{1}{2} * \frac{R1}{L_{Filter}} + \frac{1}{R2 * C_{Filter}}$$

$$\beta = \sqrt{\frac{R1 + R2}{R2 * L_{Filter} * C_{Filter}} - a^2}$$

$$\theta = a\tan\left(\frac{\beta}{a}\right) \quad \text{(eq. 44)}$$

$$V2(t) = \frac{V_{Spike} * R2}{R1 + R2} \times \left(1 - \frac{\sqrt{\frac{R1+R2}{R2}}}{\beta * \sqrt{L_{Filter} * C_{Filter}}} * e^{-a*t} * \sin(\beta * t + \theta)\right)$$

a = Exponential time constant
C_{Filter} = Input capacitance
L_{Filter} = Input inductance
R1 = DCR of the input inductor
R2 = Load resistance
V_{Spike} = Resulting line spike

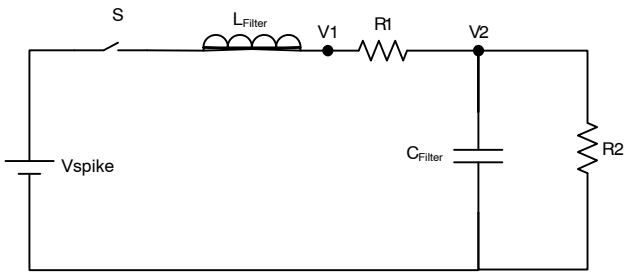


Figure 36. Simplified Input Diagram

If a reasonable filter is chosen where the inductance is 1 μH, capacitance is 10 μF, R1 is 1 mΩ and R2 is 1 MΩ the time base result of the filter can be calculated as shown in Figure 37.

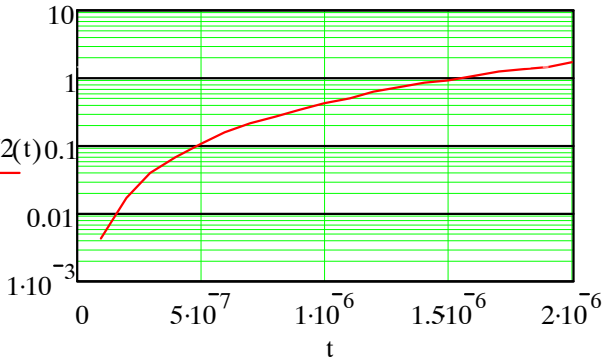


Figure 37. Change in Voltage Over Time at V2

Reverse Polarity Protection

Aside from normal solar panel transients there also exists the possibility of four different input to output connections.

Table 4. INPUT TO OUTPUT CONNECTION POSSIBILITIES

Case	Output Voltage	Input Voltage
1	Correct	Correct
2	Correct	Reverse
3	Reverse	Correct
4	Reverse	Reverse

In case 1 there is no need for protection as the input and output are connected correctly. In case 2, the input voltage is connected in reverse. If current is allowed to flow in this case, then all but the output diode will have the possibility of being damaged. However, by placing a diode in series with the input either as shown in B or C in Figure 38 all devices can be protected. One drawback to the series diode is that it dissipates power continuously in a system. If the

diode is placed in for reverse polarity protection in a high current system, the losses can be significant. An alternative way to implement reverse polarity protection is to place a diode such that it opens a fuse when a reverse voltage is applied as shown in D in Figure 38. The fuse chosen can be a user replaceable or a polley thermal fuse. The fuse provides the necessary protection but can lead to an unfavorable user experience. A low loss way to implement the diode reverse polarity protection is to use a MOSFET that turns on when the voltage is applied in the proper polarity and turns off when it is not. One example of the appropriate circuit is shown in E in Figure 38.

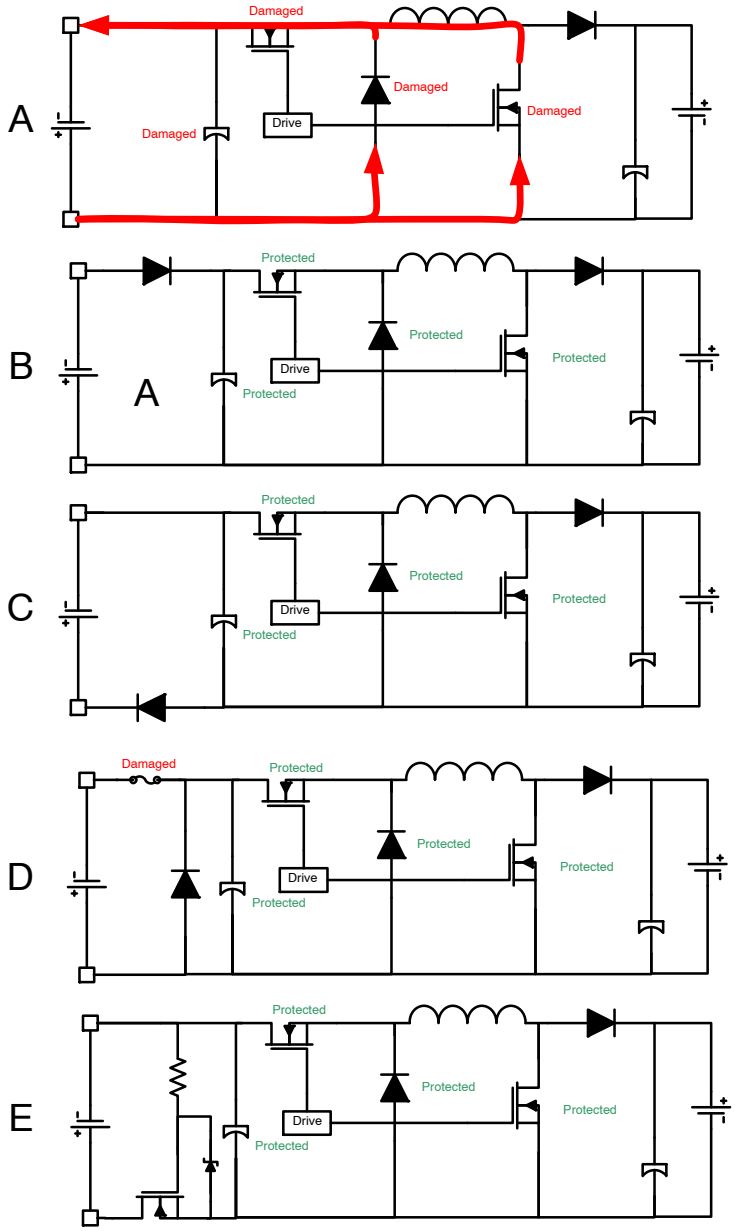


Figure 38. Input Connected in Reverse Polarity

In case 3 where the output is connected in reverse polarity and the input is connected correctly, three of the power components could be damaged. Since the source is assumed to be a lead acid battery, the protection is critical as damaged components could be ignited from the large amount of energy. Figure 39 B shows one way to protect from reverse output voltage.

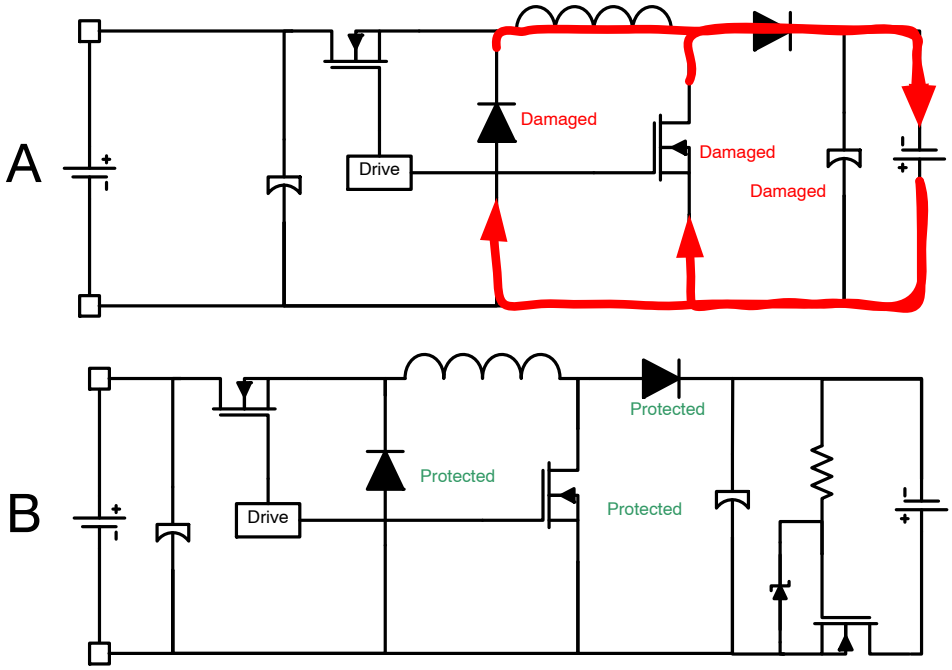


Figure 39. Output Connected in Reverse Polarity

The final case is one in which both the input and output are connected incorrectly. In case 4, if the designer implemented both protections from case 2 and case 3 the input and output would be protected. The designer should not overlook the voltage suppressors that are installed on the input at the transient voltages which can be presented in either the proper polarity or reverse polarity. Therefore it is important to have bi−directional transient suppressors that can withstand the normal reverse polarity voltage without damage.

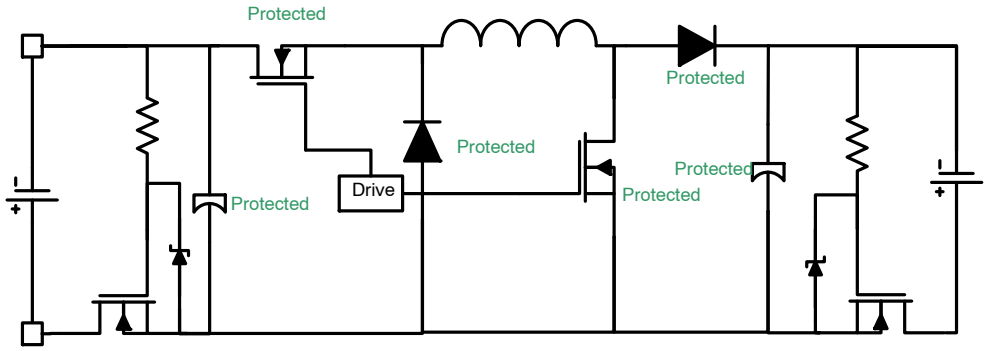


Figure 40. Input and Output Connected in Reverse Polarity

Although the above methods serve as electrical means of preventing damage to the power supply, a system designer should not overlook a mechanical means of preventing damage such as a keyed connector or dissimilar connections. One may wonder if the central grounding will affect the protection in place for reverse polarity protection and the answer is no. The topology implemented for protection in the design opens the path even with central grounding.

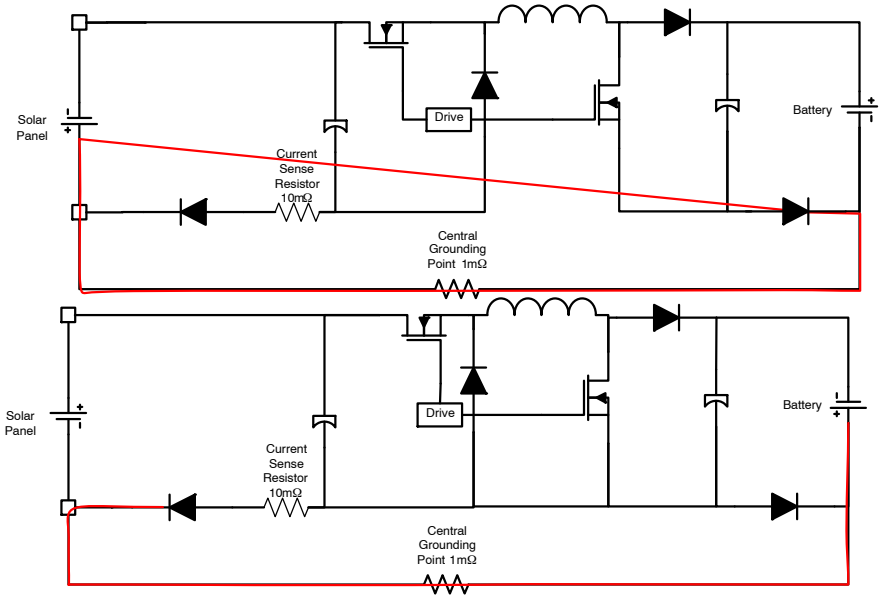


Figure 41. Reverse Polarity Protection with Central Grounding Scheme

Drive Scheme for Main Switches

The basic four switch buck boost converter is shown in Figure 42 but, Q1 and Q2 must be driven with the appropriate drive scheme to ensure good switching waveforms.

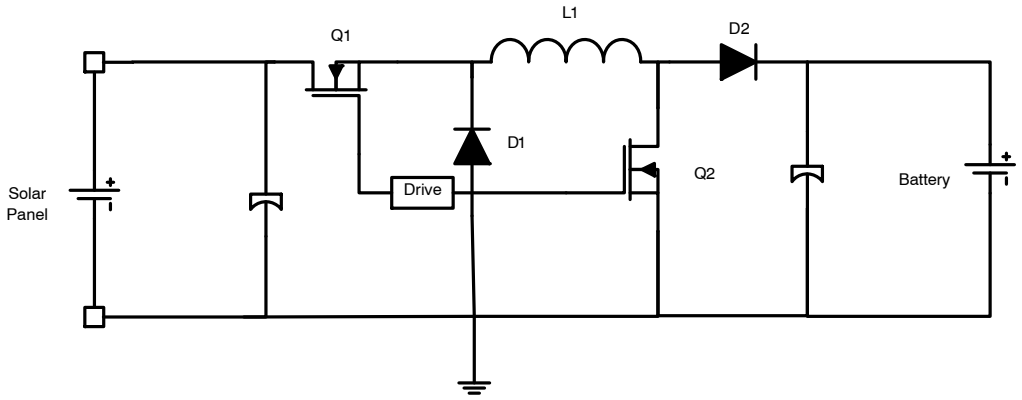


Figure 42. General Schematic for Buck Boost

The next decision one would have to make is should Q1 be a PMOSFET or an NMOSFET. When making the Q1 design decision one must consider input voltage range, efficiency, price, and second sources. First, the input voltage range is 10 V to 60 V so the MOSFET must be able to handle a minimum of 60 V but keeping with good design practice, the break down voltage will need to be derated. In order to have a product with a long lifetime a part that is rated for 100V needs to be found. The converter should have the best possible efficiency as solar panels are currently expensive and the energy derived from them is precious. The MOSFET that should be selected has a low Rd_{son} and low gate charge as the converter should switch as fast as possible to reduce the size of L1 which can be the largest part of a controller design. The price of a PMOSFET can be 2 to 4 times higher and the gate charge is usually double that of an NMOSFET with the same Rd_{son}. Further, if the designer decides to change from a non−synchronous discrete driver to an integrated synchronous driver there are very few PMOSFET synchronous integrated drivers. If the designer manages to find a PMOSFET that is at cost parity with an NMOSFET and has the same gate charge, the chances are not good that there will be many second sources. Therefore, the choice of a PMOSFET may put the solar controller in a line down situation after production has started. For all of the aforementioned reasons, the high side MOSFET will be an NMOSFET but both a PMOSFET drive scheme and NMOSFET drive scheme are shown in the Figures 43 and 44 below. In the NMOSFET drive scheme shown in Figure 43, a drive signal is sent to the gate of Q1, in this case a 2N7002. When the drive signal from the NCP1294 is high, it pulls down on the R1 R2 resistor divider. The resistor divider in turn pulls down on the gate of Q3, turning it on and allowing C1 pre−charged 8 V to flow through the switching

diode, D2, to the gate of Q2, turning it on and allowing the switch node to rise. As the switch node rises, so does the voltage at the gate of Q2 until the solar panel voltage is presented to the switch node and the solar panel voltage plus 8 V is presented at the gate of Q2. Once the gate signal goes low, the current ceases to flow through R1 and R2 and the gate of Q3 is pulled to VSW plus the bias voltage. R3 discharges to the switch node potential and Q4 discharges the gate of Q2 to the switch node. Upon completion of Q2 discharge the switch node falls and C1 charges up to 9 V through D1. In this type of drive scenario, there may be a startup into pre−bias issue where the converter never gets started. If the battery is connected first to the output, then the solar panel is connected, there will be 12 V at the switch node and 8 V on the VC node which will not allow capacitor C1 to charge properly. Since C1 is not charged properly, Q2 can only turn on linearly and will not start switching. The purpose of the pink highlighted area is to solve this issue by pulling down on VSW during Q2s off time to ensure C1 is properly charged. D3 and R5 can be used to change the nonoverlap time of the synchronous C1 charging. In looking at the drive scheme for the PMOSFETs, only 3 transistors are required versus the 7 needed for the N drive, but each transistor is approximately 0.03 USD in medium quantities, so quantitatively the P drive is 0.09 USD vs 0.21 USD for the N drive. The question one must ask is: is the PMOSFET for the application less than the cost difference of the drivers and will the efficiency be degraded? Another question is can a synchronous driver be used for the same cost as it will also improve efficiency? The answer is no because a driver that will work at 60 V will cost 0.71 USD and trading a diode for a MOSFET would double the cost for the switch. The main design will not be a synchronous design, but if the designer holds efficiency above cost, a driver has been made available so that the designer can prototype both circuits to weigh cost and efficiency.

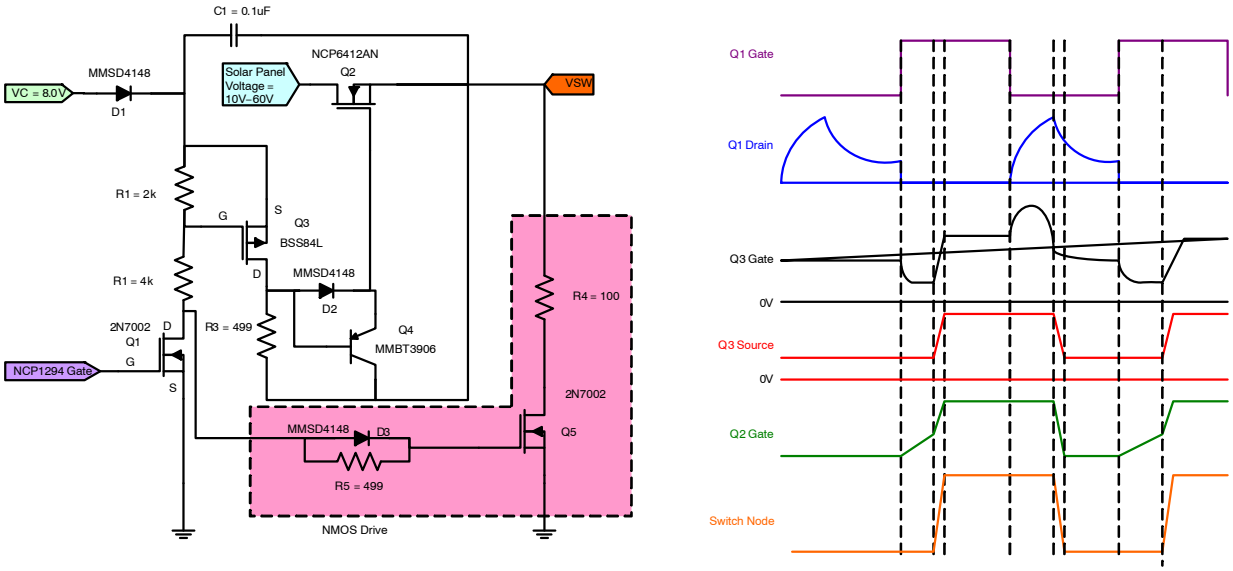


Figure 43. NMOSFET Drive Scheme

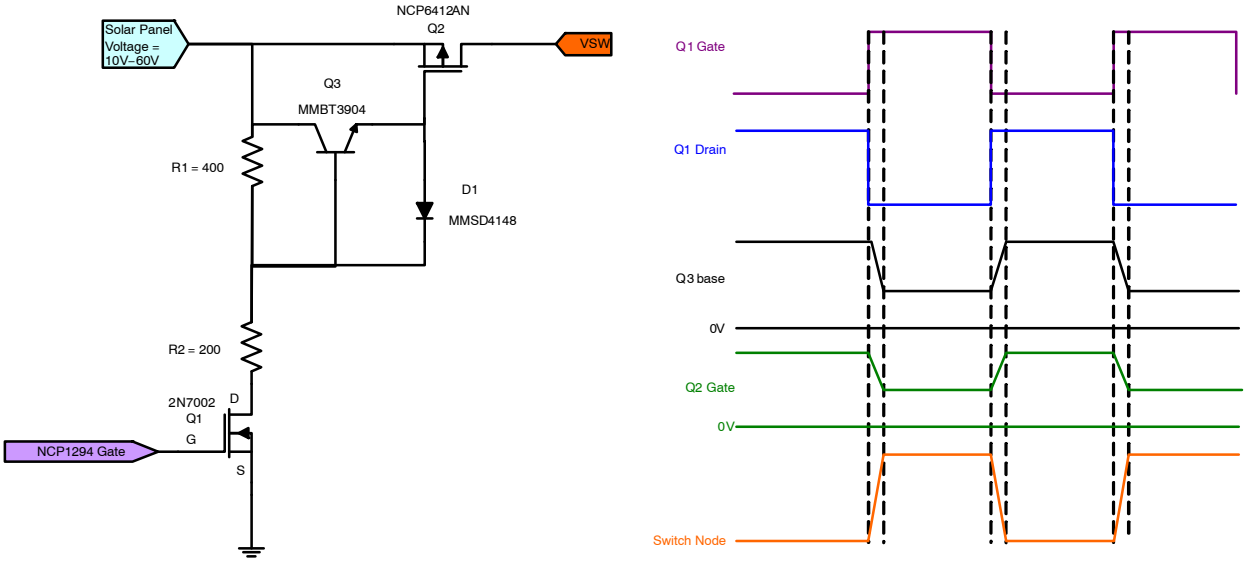
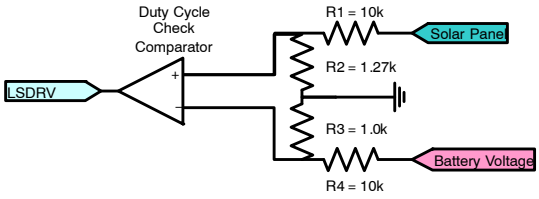
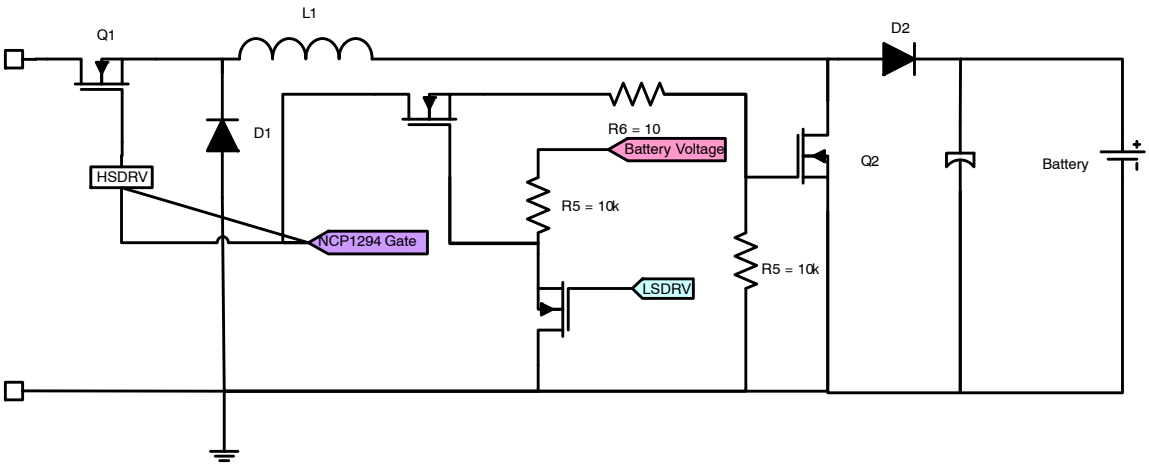


Figure 44. PMOSFET Drive Scheme

Q2 is only turned on during buck boost operation unlike Q1 which is driven continuously during both buck and buck boost operation. The solar controller should turn on the buck boost portion (Q2) of the circuit only when the input voltage falls too far to maintain regulation and that is determined by the choice of components and allowable max duty cycle. Therefore, a circuit is needed to determine at what duty cycle the full four switch buck boost will be engaged. The circuit in Figure 45 looks at the solar panel voltage and the battery charge voltage and determines when they have hit the predetermined duty cycle threshold. Once they have passed the 85% duty cycle, the full buck boost state will begin to operate.





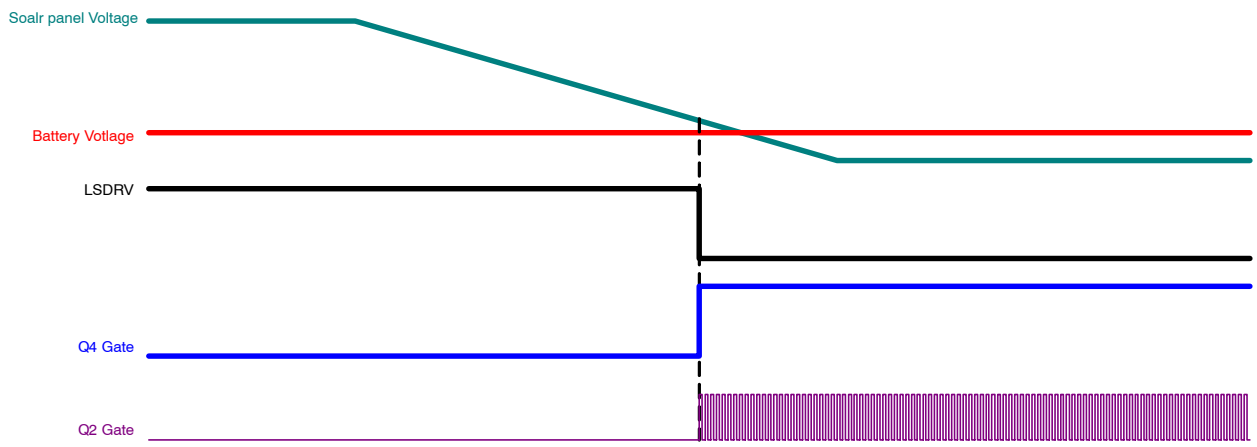


Figure 45. Buck Boost Mode Detector

Buck Mode Power Saving Option

During buck mode, Q2 remains off and D2 is always forward conducting. In buck mode it is advantageous to short D2 since it does not serve a constructive purpose in this mode and the tradeoff made is one of efficiency for cost. The power dissipation of D2 is contained in the following equations.

$$P_{diode} = Vf * I_{OUT} \rightarrow 7\ W = 0.7 * 10\ A \quad \text{(eq. 45)}$$

I_{OUT} = Output current
P_{diode} = Power dissipation of a diode
Vf = Forward voltage of a diode

$$P_{MOSFET} = I_{OUT}{}^2 R_{DS(on)} \rightarrow \frac{P_{MOSFET}}{I_{OUT}{}^2} = R_{DS(on)} \rightarrow 70\ m\Omega = \frac{7\ W}{10\ A^2} \quad \text{(eq. 46)}$$

I_{OUT} = Output current
P_{MOSFET} = Power dissipation of the P_{MOSFET}
$R_{DS(on)}$ = On resistance of the P_{MOSFET}

The trade off is a good one as long as the Rd_{son} is lower than 70 mΩ as shown graphically in the Figure 46 below, where the diode has a constant efficiency drop and the MOSFET losses have a linear loss factor.

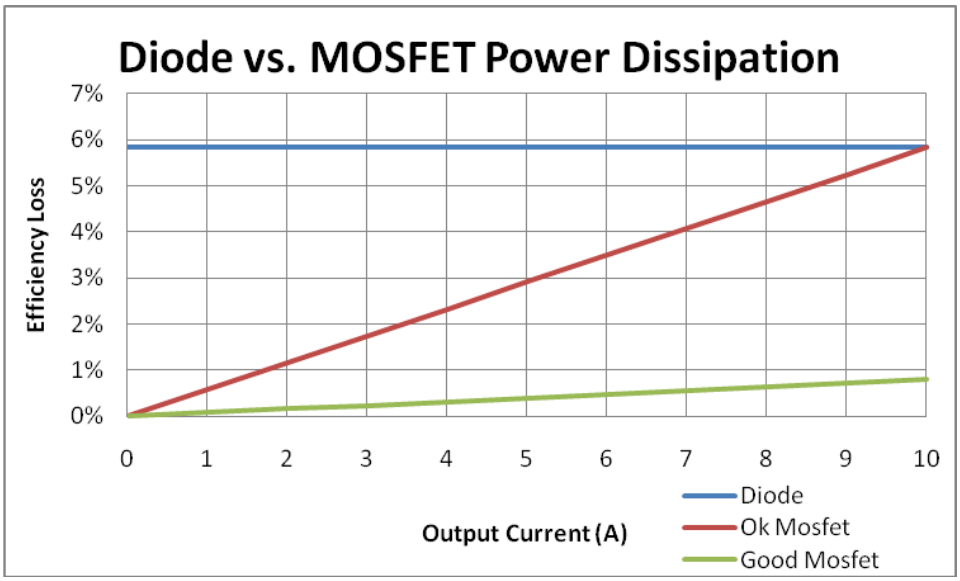


Figure 46. Efficiency Loss of Diode vs. MOSFET

Battery Charging

There are three stages to charging a lead acid battery: constant current or bulk charge, absorption or constant voltage mode, and float. During the bulk charge, the current is to be held constant which is accomplished with the NCP1294 pulse by pulse current limiting and the current set circuit. The current will maintain the set charge rate configured by the designer or user unless the maximum power point falls below that level, at which time it will charge to the max power point adjusted rate.

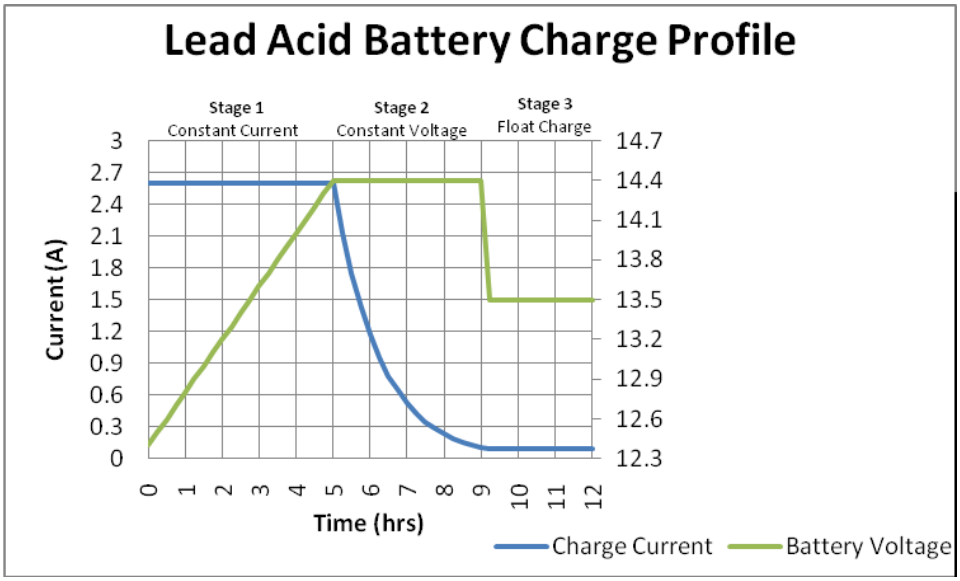


Figure 47. Lead Acid Battery Charge Profile

Since the NCP1294 has pulse by pulse current limiting, nothing needs to change between Stage 1 and Stage 2 as the output voltage can be set to 14.5 V for both stages. In Stage 1, the outer voltage loop is never satisfied and the inner current loop maintains the required current. In Stage 2, the outer voltage loop takes over functionality and the inner current loop is not used except to maintain the maximum power point. The result of the voltage loop taking over is that a constant voltage of 14.5 V is maintained, while the current drops to 5% of the amp hour rating. When the current drops to 5%, the solar controller will change to float state and the outer voltage loop will decrease to 13.5 V where it remains indefinitely or until the current need changes. Many types of lead acid batteries are suitable for solar powered street lights, they are: flooded, Valve Regulated Lead Acid (VRLA), Absorbed Gas Mat (AGM), and gel. A table of appropriate absorption, float and over voltage levels are shown in Table 5.

Table 5. CHARGING VOLTAGES OF LEAD ACID BATTERIES

Charging Mode	Voltage Range (V)							
	Flooded		Sealed VRLA		AGM		GEL	
	Min	Max	Min	Max	Min	Max	Min	Max
Absorption	14.2	14.8	14.2	14.5	14.4	15	14.4	14.7
Float	13.2	13.5	13.2	13.5	13.2	13.8	13.5	13.8
Over Voltage	15.1		14.9		15.3		15.4	

While the output voltage is set to 14.5 V for absorption and 13.5 V for float charge, the designer can place a potentiometer to dial in the voltage they would like for their particular battery. The voltage change circuitry is shown in Figure 48 below.

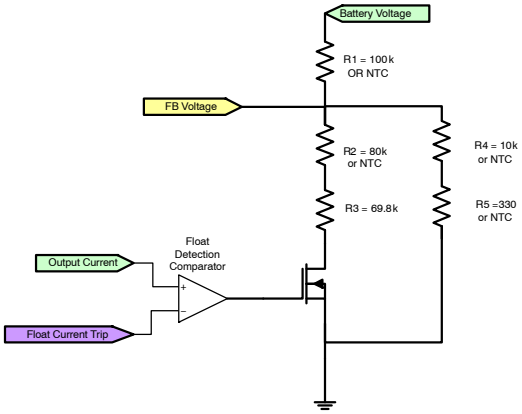


Figure 48. Battery State Control and Internal Temperature Compensation

One important thing to know is the affect temperature will have on battery charge voltage as most solar installations are not in sheltered environmental conditions. Typical lead acid battery voltage moves as an exponential. Some variation exists in the upper and lower battery tolerance at a specific temperature, the equations to define upper and lower battery voltages for the standard six cells configuration is shown below.

$$Bat_{UPPER} = 15.928617e^{-0.002479T} \quad \text{(eq. 47)}$$

$$Bat_{LOWER} = 15.327247e^{-0.002582T} \quad \text{(eq. 48)}$$

Bat_{UPPER} = Lower battery tolerance
Bat_{LOWER} = Upper battery tolerance
T = Battery Temperature in degrees C

To compensate for the battery change with temperature, the output set point of the solar controller must change with temperature. If remote sensing is not used, one idea for compensation is to use a negative temperature coefficient resistor or NTC as the voltage of the battery decreases as temperature increases. The NCP1294 regulates voltage at the FB node to be 1.263 V, therefore the resistance of R1 must be decreased or a temperature compensated current should be injected into the FB node. To determine how the NTC value changes over temperature, the following equation is used.

$$R = Ro \times e^{\beta \times \left(\frac{1}{T} - \frac{1}{To}\right)} \quad \text{(eq. 49)}$$

β = Thermistor Constant
R = Resistance at specified temperature
Ro = Resistance at To
To = 298.15 K (25°C)
T = Current temperature in K

If a NTC is placed in series with R1, the resulting battery voltage falls within the upper and lower battery limits established in Equations 47 and 48, except when it gets extremely cold. However, if a NTC replaces R2, the resulting curve does no harm in cold temperatures, but would destroy the battery when hot. When the two curves are put together, the resulting curve fits between the rails as shown below in Figures 49 and 50.

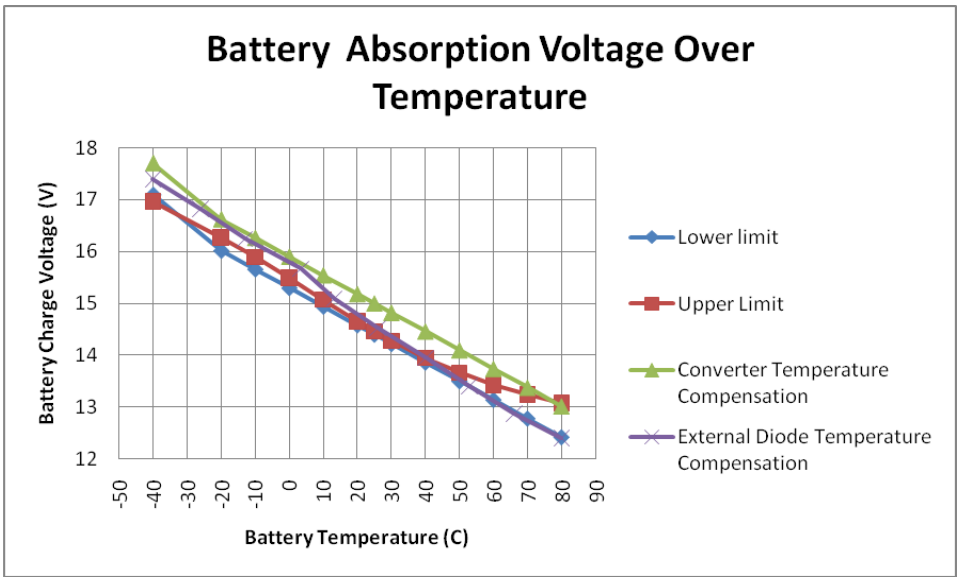


Figure 49. Temperature Compensated Battery Charged Voltage

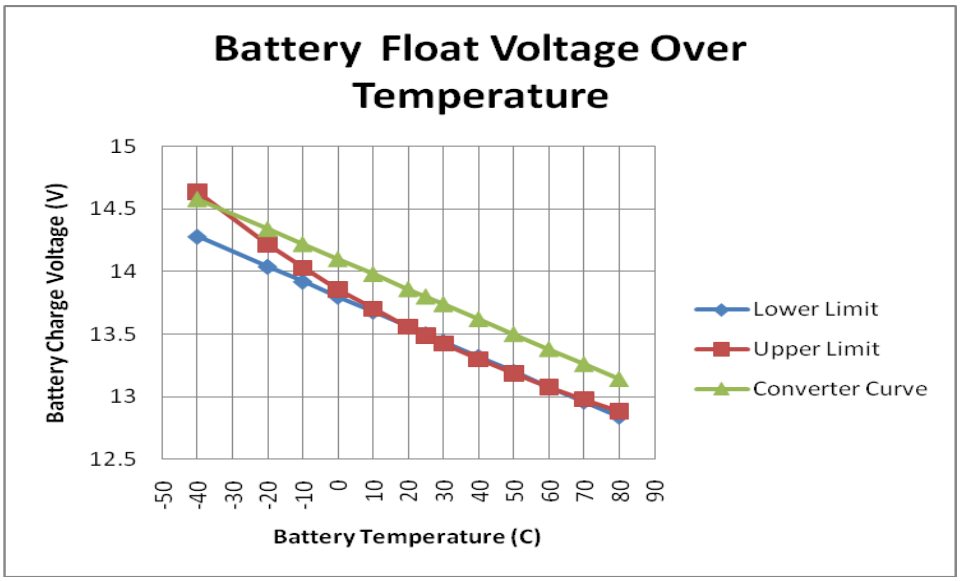


Figure 50. Temperature Compensated Battery Float Voltage

The NCT loop should be placed as far away from the converter heat sources as possible. If the designer does not want to use an internal NTC, an external diode sense can be used in conjunction with the NCP1294 3.3 V reference. When using diodes to monitor the temperature as shown in Figures 49 and 51, it is important to buffer the 3.3 V reference voltage as the diode configuration can be remotely located on the battery or outside the case, where it will be exposed to ambient temperatures as well as ambient noise. Buffering the reference will isolate other circuitry which may be using the reference from the external noise contamination.

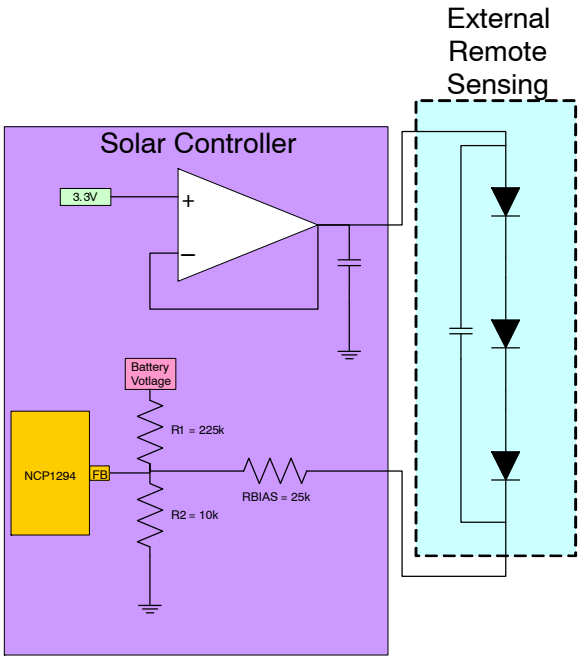


Figure 51. External Diode Temperature Monitoring

OOV

The output battery voltage should be monitored to determine if the feedback mechanisms have been damaged or the remote sensing has influenced the battery voltage beyond the battery temperature compensation. The NCP1294 is equipped with a OOV comparator, when tripped the OOV shuts off the system. The comparator can be used on the input of the system or the output of the system, but is recommended to be used on the output as a failsafe mechanism. When using a single battery system, a single trip point of 18 V can be used or trip points can be set based on the state of charge. If using the float voltage state, a trip voltage of 15 V needs to be set. If using the absorption phase of charge, an 18 V level should be set. If a completely safe system were to be setup, a trip level could be set to 10% greater than the battery voltage adjusted for temperature and state of charge.

OUV

The converter input voltage should be monitored to determine if the input voltage level will cause a thermal issue. The NCP1294 is equipped with an under voltage lockout independent of V_{IN} monitoring to ensure the input voltage is at the desired level for providing full output power.

OTP

Since the solar controller can be used in an inappropriate way, it is suggested that the temperature of the buck main switch be monitored to determine if it has exceed maximum temperature levels. If the temperature of the main MOSFET has exceeded appropriate levels, the current can be throttled back to reduce the power dissipation of the system.

Thermal Management

The NCP1294 is a small source of power dissipation in the system for which the equations above detailed the loss mechanisms. The control portion of the IC power dissipation is determined by the formula below:

$$P_C = I_{CC} \times V_{IN} \quad \text{(eq. 50)}$$

I_{CC} = Control circuitry current draw
P_C = Control power dissipation
V_{IN} = Input voltage

Once the IC power dissipations are determined, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient temperature. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D \times R_{\theta JA} \quad \text{(eq. 51)}$$

P_D = Power dissipation of the IC
$R_{\theta JA}$ = Thermal resistance junction to ambient of the regulator package
T_A = Ambient temperature
T_J = Junction temperature

Thermal performance of the solar controller is strongly affected by the PCB layout. Extra care should be taken by users during the design process to ensure that the IC and power switches will operate under the recommended environmental conditions. As with any power design, proper laboratory testing should be performed to ensure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET RDS_{ON}). Several layout tips are listed below for the best electric and thermal performance.

The Solar Panel

The solar panel supported by the NCP1294 evaluation board is between 5 W and 120 W. The industry standard types of solar panels were considered for this development. Most common types of solar cells are crystalline silicon in which there are two primary types: monocrystaline and polycrystalline silicon. Monacrystalline is the most efficient, but also more expensive to produce and is usually limited to commercial and residential applications. Amorphous solar panels consist of a thin film made from molten silicon that is spread across a large plate of stainless steel or similar material. The crystalline structures are very fragile and usually sandwiched between two sheets of glass for protection.

- Monocrystalline 18% efficiency
- Polycrystalline 15% efficiency
- Amorphous 10% efficiency

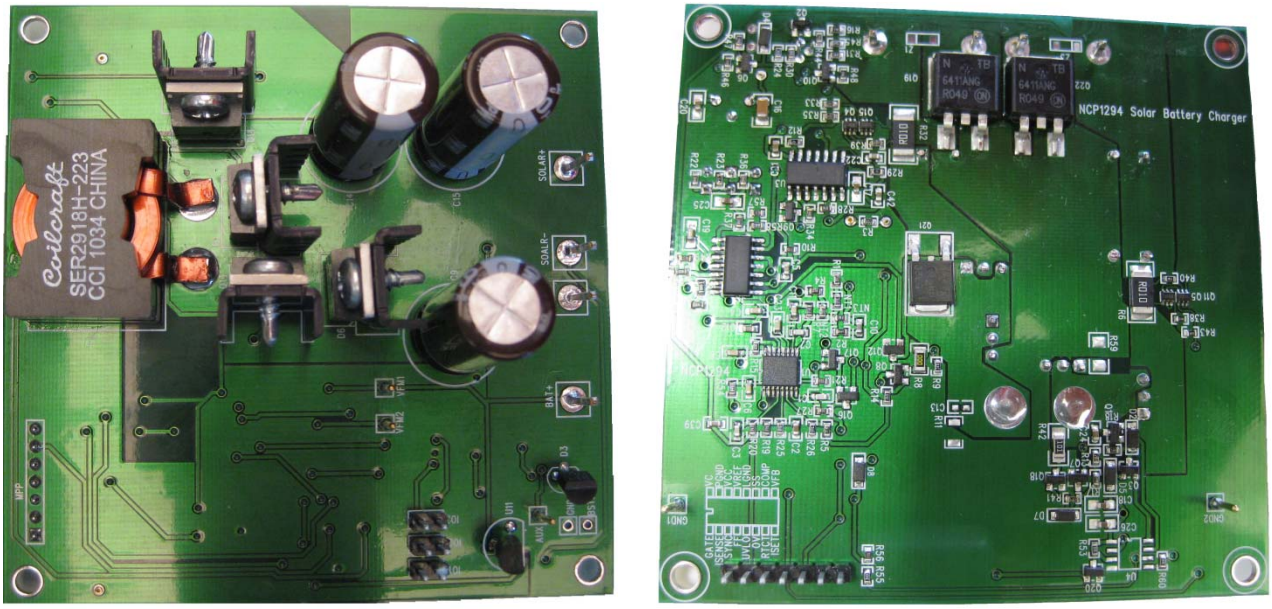


Figure 52. Solar Controller PCB

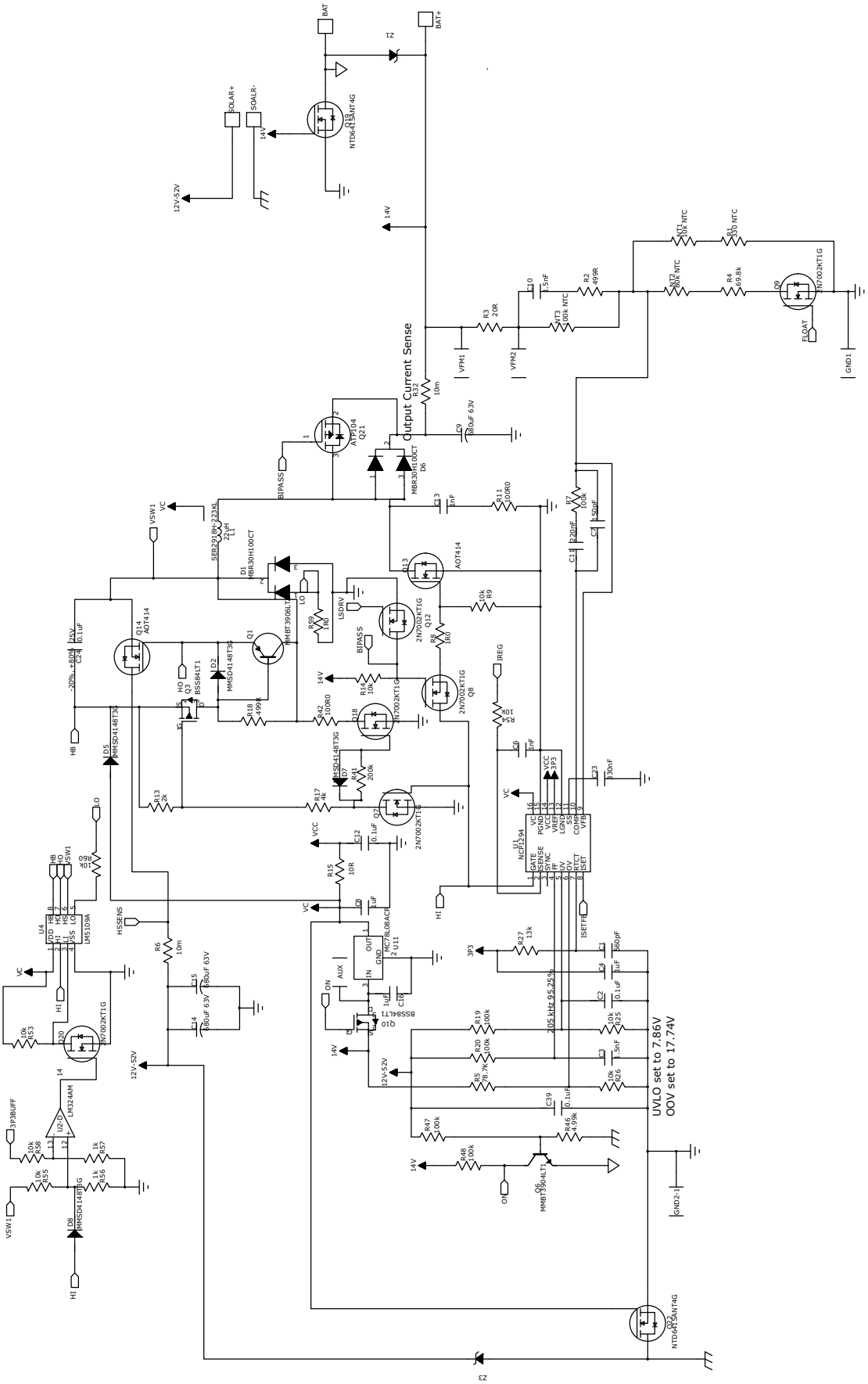


Figure 53. Schematic 1Z

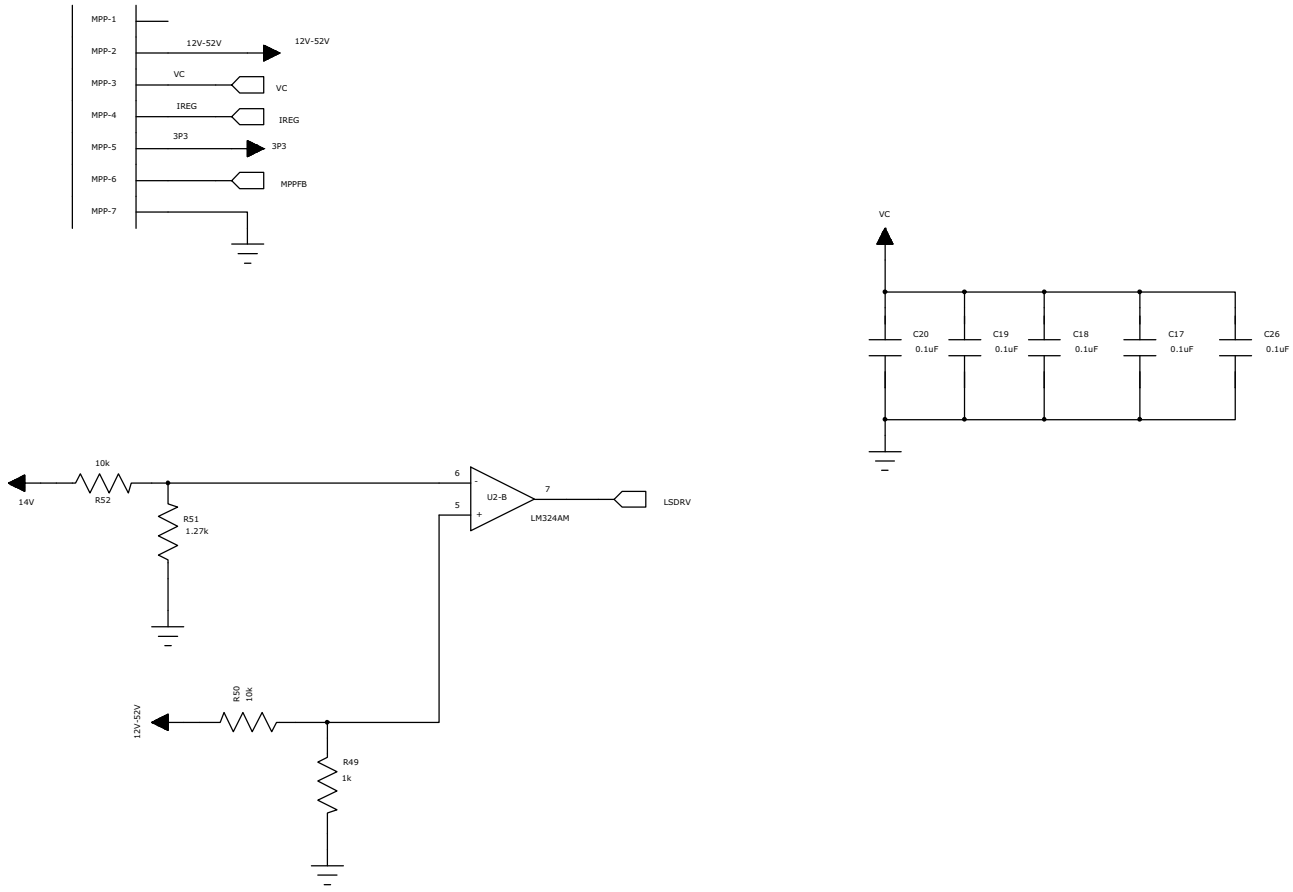
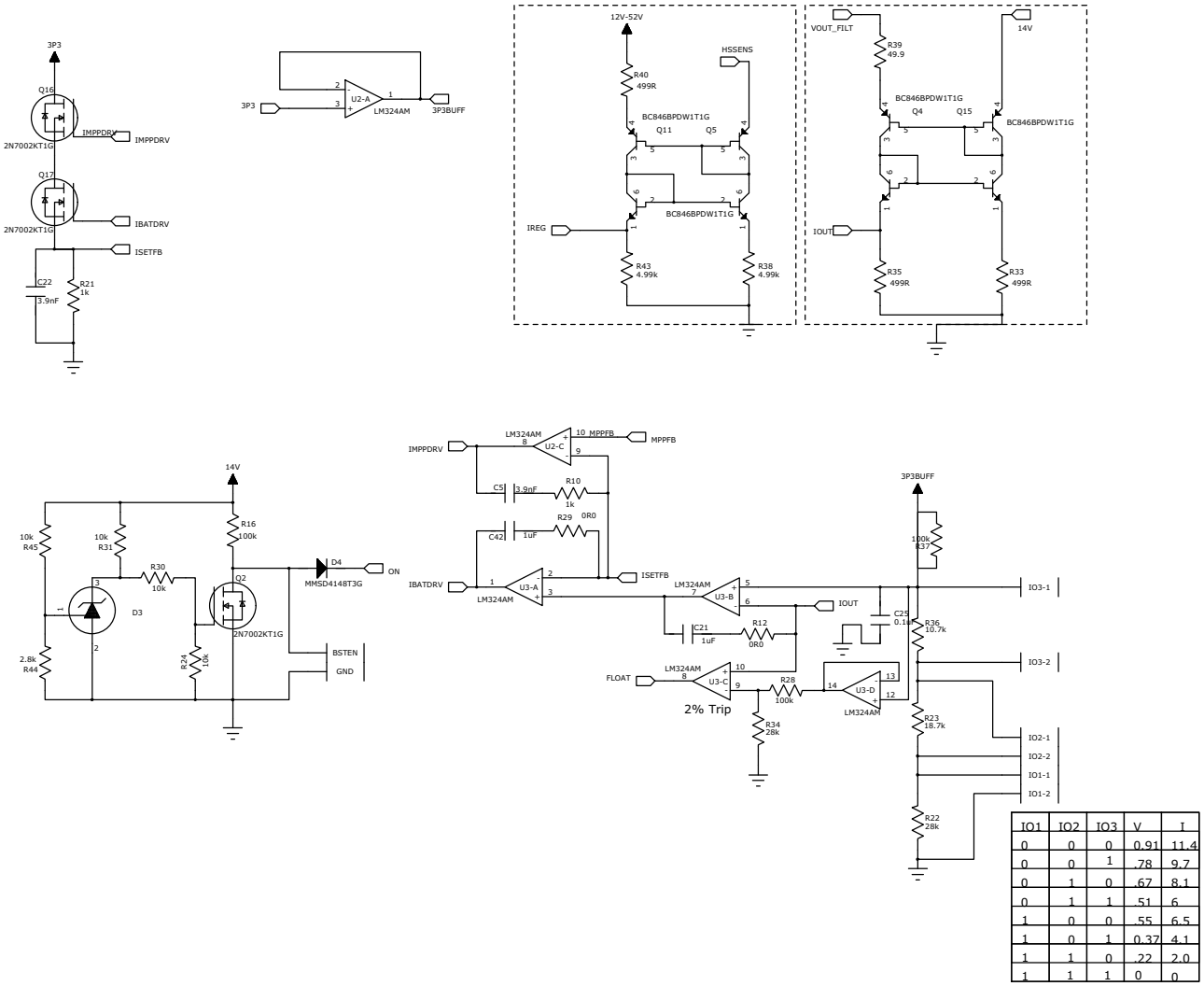


Figure 54. Schematic 2



IO1	IO2	IO3	V	I
0	0	0	0.91	11.4
0	0	1	.78	9.7
0	1	0	.67	8.1
0	1	1	.51	6
1	0	0	.55	6.5
1	0	1	0.37	4.1
1	1	0	.22	2.0
1	1	1	0	0

Figure 55. Schematic 3

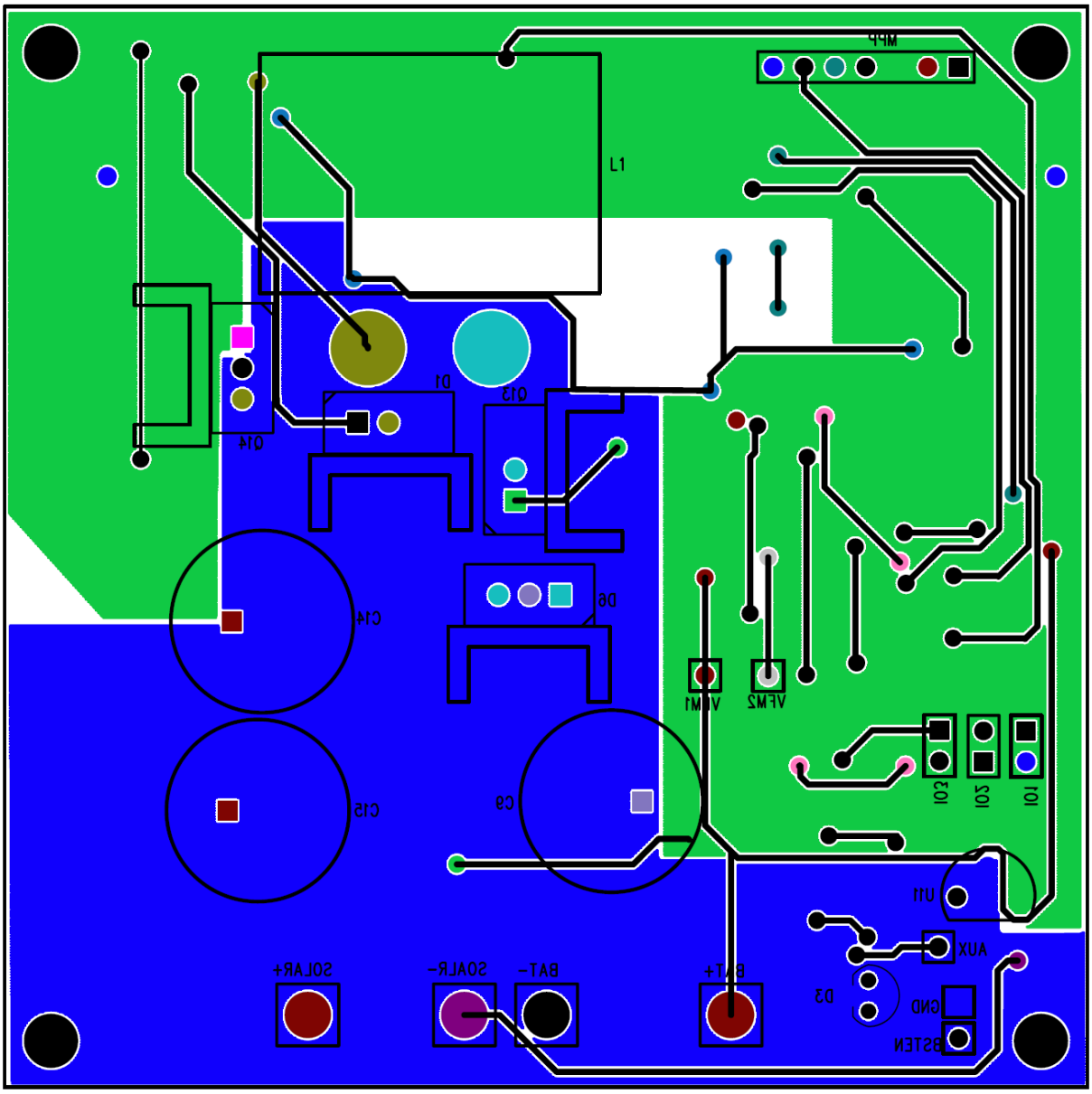


Figure 56. Layout Bottom

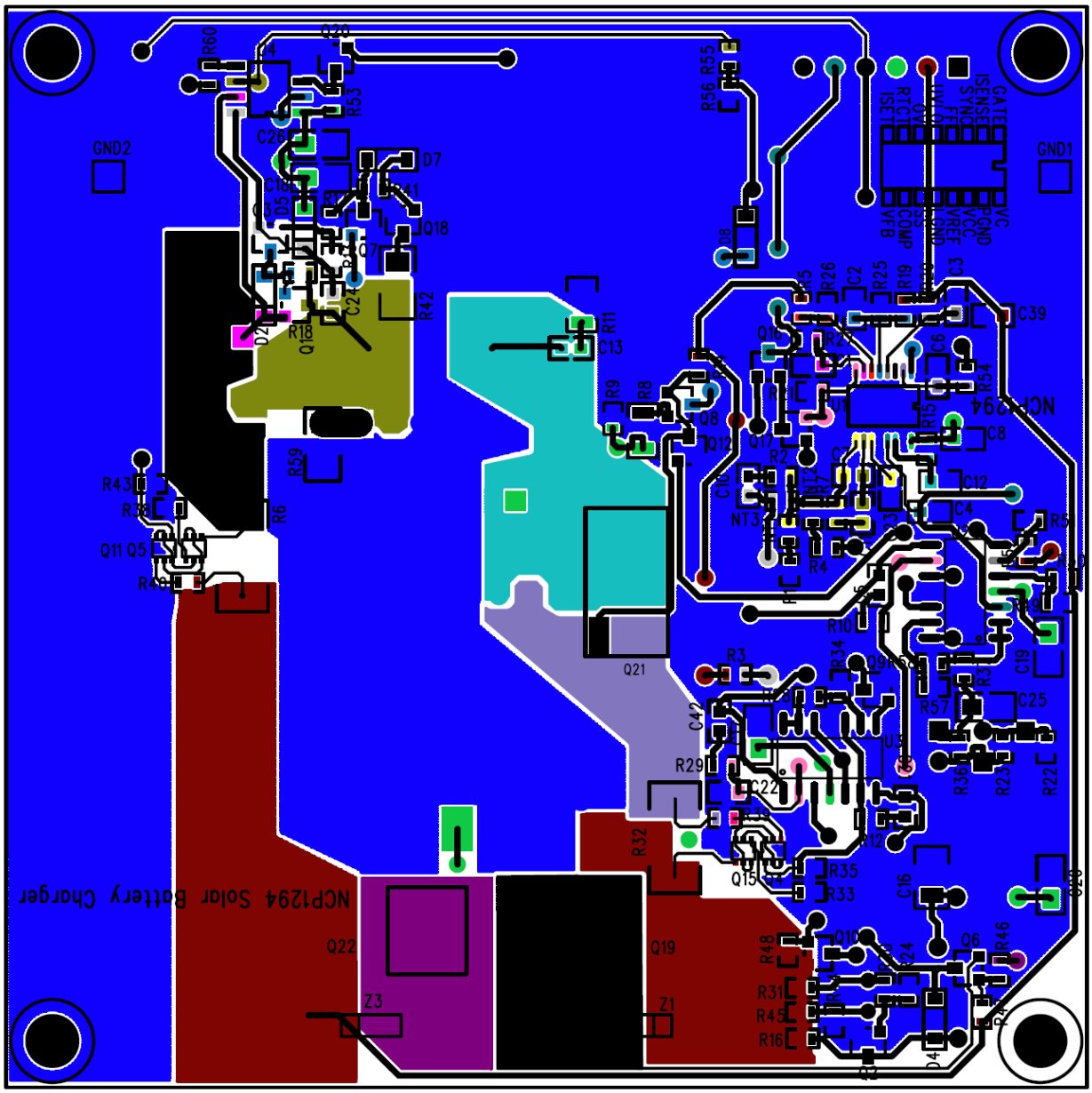


Figure 57. Layout Top

Table 6. BOM

Reference	Qty	Description	Part Name	Manufacturer	Footprint	Manufacturer	Manufacturer Part #
Q2, Q7 – 9, Q12, Q16 – 18, Q20	9	Small Signal N MOSFET	60 V 380 mA	NA	SOT−23	ON Semiconductor	2N7002KT1G
Q21	1	30 V, 72 A, Single P−Channel MOSFET	8.4 mΩ	NA	ATPAK (2leads + tab)	SANYO	ATP104−TL−H
D2, D4 – 5, D7−8	5	Switching Diodes	1 V	NA	SOD123	ON Semiconductor	MMSD4148T3G
Q4 – 5, Q11, Q15	4	NPN Dual	65 V 100 mA	NA	SC−88	ON Semiconductor	BC846BPDW1T1G
Q3, Q10	2	NFET	10R 50 V	NA	SOT−23	ON Semiconductor	BSS84LT1
C1	1	SMT Ceramic Capacitor	560 pF	±5%	603	TDK Corporation	C1608C0G1H561J
C3, C10	2	SMT Ceramic Capacitor	1.5 nF	±10%	603	TDK Corporation	C1608X7R2A152K

Table 6. BOM

Reference	Qty	Description	Part Name	Manufacturer	Footprint	Manufacturer	Manufacturer Part #
C6, C13	2	SMT Ceramic Capacitor	1 nF	10%	603	TDK	C1608X7R2A102K
C4, C8	2	SMT Ceramic Capacitor	1 μF	−20%, +80%	603	Taiyo Yuden	EMK107B7105KA−T
C23	1	SMT Ceramic Capacitor	330 nF	±10%	603	TDK Corporation	C1608X7R1A334K
C17−20, C25−26	6	SMT Capacitor	0.1 μF	±20%	805	AVX Corporation	08055C104MAT2A
C2, C12, C24	3	Ceramic Chip Capacitor	0.1 μF	−20%, +80%	603	AVX	06033G104ZAT2A
C11	1	Ceramic Chip Capacitor	220 nF	10%	603	TDK Corporation	C1608X7R1C224K
C5, C22	2	Ceramic Chip Capacitor	3.9 nF	10%	603	Murata	GRM188R71H392KA01D
C21, C42	2	Ceramic Chip Capacitor	1 μF	10%	603	Murata	GRM188R71H392KA01D
C39	1	Ceramic Chip Capacitor	0.1 μF	±20%	603	TDK Corporation	C1608X7S2A104M
C7	1	Ceramic Chip Capacitor	150 pF	5%	603	TDK Corporation	C1608C0G1H151J
C16	1	Ceramic Chip Capacitor	1 μF	±10%	1206	Murata	GRM31MF51E105ZA01L
U1	1	Enhanced Voltage Mode PWM Controller	3 V Reference	NA	SOIC 16	ON Semiconductor	NCP1294
C9, C14−15	3	Electrolytic Capacitor	680 μF 63 V	20%	16X25	Nichicon	UPW1J471MHD6
U2−3	2	QUAD, LOW POWER OP AMP	1 MHz	NA	14−SOIC	ON Semiconductor	LM324ADR2G
U4	1	Half Bridge Driver	1 A 108 V	NA	8−WDFN	National Semiconductor	LM5109AMA
D1, D6	2	Schottky Rectifier	100 V 30 A	NA	TO−220	ON Semiconductor	MBR30H100CTG
U11	1	8.0 V Regulator		4%	TO−92−3	ON Semiconductor	MC78L08ACPRE
Q6	1	General Purpose NPN Transistor	40 V 200 mA	NA	SOT−23	ON Semiconductor	MMBT3904LT1G
Q1	1	General Purpose PNP Transistor	PNP	NA	SOT−23	ON Semiconductor	MMBT3906LT1G
Z1, Z3	2						NI
Q13−14	2	N−MOSFET	100 V 18.2m	NA	TO−220	Alpha & Omega	AOT414
Q19, Q22	2	N MOSFET	100 V 50m	NA	Dpak	ON Semiconductor	NTD6415ANT4G
NT1	1	Resistor	10k NTC	±1.0%	603	EPCOS Inc	B57331V2103J60
NT2	1	Resistor	80k NTC	±1.0%	603	Vishay / Dale	NTHS0603N01N8002JE
NT3	1	Resistor	100k NTC	±1.0%	603	TDK	NTCG164KF104FT1
R1	1	Resistor	330 NTC	±1.0%	603	Murata	NCP18XM331J03RB
R2, R18, R33, R35, R40	5	Resistor	499R	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT499R
R9, R14, R24−26, R30−31, R45, R50, R52 − 55, R58, R60	15	Resistor	10k	±1.0%	603	Panasonic	ERJ−3EKF1002V
R13	1	Resistor	2k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT2K00
R10, R49, R21	3	Resistor	1k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT1K00
R29, R12	2	Resistor	0R0	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT499R
R16, R37, R7, R47 − 48, R19 − 20, R28	8	Resistor	100k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT100K
R34, R22	2	Resistor	28k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT28K0
R43, R46, R38	3	Resistor	4.99k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT4K99
R44	1	Resistor	2.8k	±1.0%	603	Vishay / Dale	RMCF0603FT2k80
R5	1	Resistor	78.7k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT78K7

Table 6. BOM

Reference	Qty	Description	Part Name	Manufacturer	Footprint	Manufacturer	Manufacturer Part #
R36	1	Resistor	10.7k	±1.0%	603	STACKPOLE	RMCF0603FT10K7
R27	1	Resistor	13k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT13K0
R3	1	Resistor	20R	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT20R0
R51	1	Resistor	1.27k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT1K27
R4	1	Resistor	69.8k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT69K8
R17	1	Resistor	4k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT4K99
R39	1	Resistor	49.9	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT49R9
R41	1	Resistor	200k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT4K99
R56−57	2	Resistor	1k	±1.0%	603	Panasonic	ERJ−3EKF1002V
R23	1	Resistor	18.7k	±1.0%	603	Stackpole Electronics Inc	RMCF0603FT15K0
R15	1	Resistor	10R	±5.0%	603	Stackpole Electronics Inc	RMCF0603JT10R0
R8, R59	2	Resistor	1R0	±5.0%	1206	Stackpole Electronics Inc	RMCF1206JT1R00
R42, R11	2	Resistor	100R0	±5.0%	1206	Stackpole Electronics Inc	RMCF1206JT100R
R6, R32	2	Resistor	10m	±1.0%	2512	Bourns Inc.	CRA2512−FZ−R010ELF
L1	1	Inductor	22 μH	±10%	SMT	Coilcraft	SER2918H−223KL
D3	1	Shunt Reference		±1.0%		ON Semiconductor	TL431ACLPRAG

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