

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input (AUIRS2123) or out of Phase with input (AUIRS2124)
- Leadfree, RoHS compliant
- Automotive qualified*

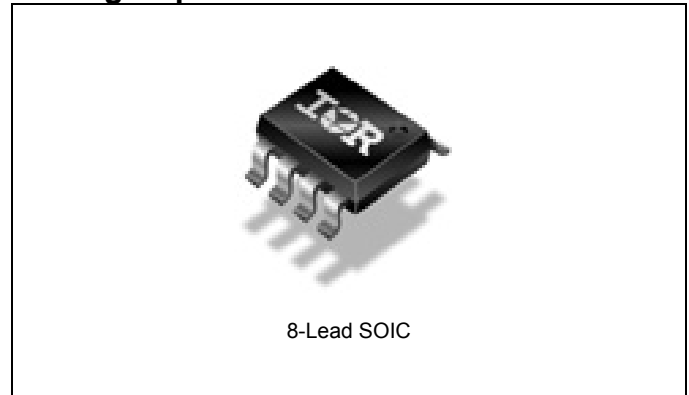
Typical Applications

- General purpose single high side inverters

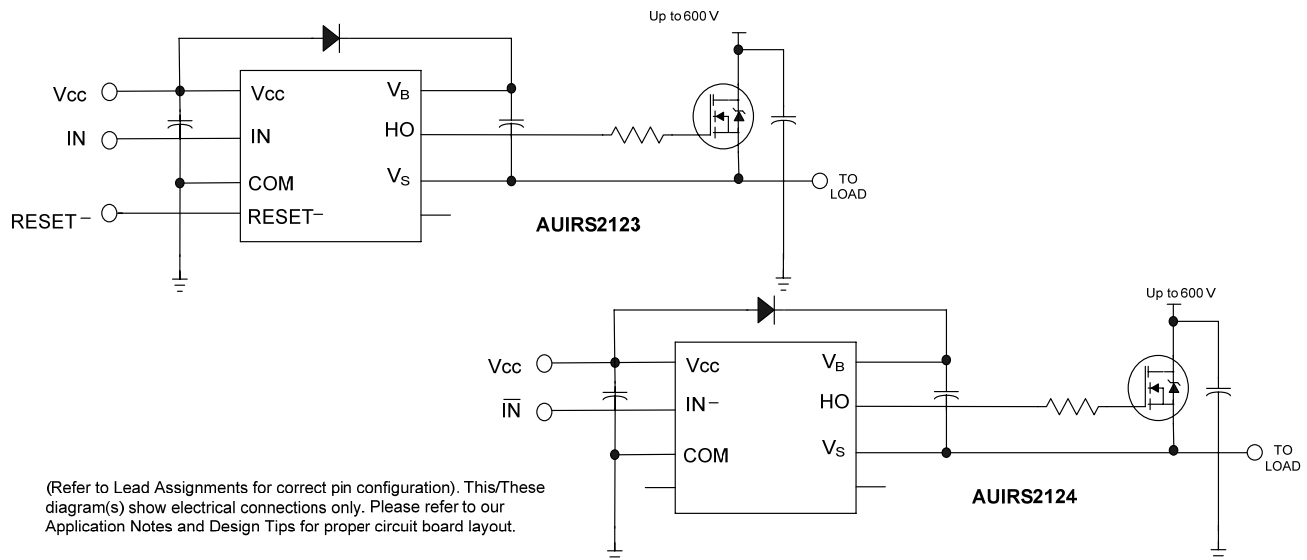
Product Summary

| | |
|---|----------------------|
| Topology | Single highside |
| V_{OFFSET} | $\leq 600 \text{ V}$ |
| V_{OUT} | 10 V – 20 V |
| $I_{\text{O+}} \& I_{\text{O-}}$ (typical) | 500 mA |
| $t_{\text{ON}} \& t_{\text{OFF}}$ (typical) | 140 ns & 140 ns |

Package Options



Typical Connection Diagram



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Description

The AUIRS2123S/AUIRS2124S are high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Qualification Information[†]

| | | | |
|-----------------------------------|----------------------|---|--|
| Qualification Level | | Automotive (per AEC-Q100 ^{††}) | |
| | | Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | SOIC8 | MSL3 ^{†††} 260°C (per IPC/JEDEC J-STD-020) |
| ESD | Machine Model | Class M3 (per AEC-Q100-003) | |
| | Human Body Model | Class H2 (per AEC-Q100-002) | |
| | Charged Device Model | Class C5 (per AEC-Q100-011) | |
| IC Latch-Up Test | | Class II, Level A (per AEC-Q100-004) | |
| RoHS Compliant | | Yes | |

[†] Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

^{††} Exceptions to AEC-Q100 requirements are noted in the qualification report.

^{†††} Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. This is a stress only rating and operation of the device at these or any conditions exceeding those indicated in the operational sections of this specification is not implied

| Symbol | Definition | Min. | Max. | Units |
|-----------|--|-------------|----------------|--------|
| V_{BS} | High Side Floating Supply Voltage | -0.3 | 25 | V |
| V_B | High Side Driver Output Stage Voltage | -0.3 | 625 | V |
| V_S | High Side Floating Supply Offset Voltage | $V_B - 25$ | $V_B + 0.3$ | V |
| V_{Ho} | Output Voltage Gate Connection | $V_S - 0.3$ | $V_B + 0.3$ | V |
| V_{CC} | Supply Voltage | -0.3 | 25 | V |
| V_{IN} | Input Voltage | -0.3 | $V_{CC} + 0.3$ | V |
| V_{RES} | Reset Input Voltage | -0.3 | $V_{CC} + 0.3$ | V |
| dV/dt | Allowable Offset Voltage Slew Rate | -50 | 50 | V/nsec |
| T_J | Junction Temperature | -55 | 150 | °C |
| T_S | Storage Temperature | -55 | 150 | |

Recommended Operating Conditions

For proper operations the device should be used within the recommended conditions.

| Symbol | Definition | Min. | Max. | Units |
|-----------|--|------------|------------|-------|
| V_B | High Side Driver Output Stage Voltage -10V Transient 0.4 us | $V_S + 10$ | $V_S + 20$ | V |
| V_S | High Side Floating Supply Offset Voltage -25V Transient 0.4 μ s | † | 600 | V |
| V_{Ho} | Output Voltage Gate Connection | V_S | V_B | V |
| V_{CC} | Supply Voltage | 10 | 20 | V |
| V_{IN} | Input Voltage | 0 | V_{CC} | V |
| V_{RES} | Reset Input Voltage | 0 | V_{CC} | V |
| T_A | Ambient Temperature ($f_s < 60\text{kHz}$, $V_{BS} = 14\text{V}$, $C_{load} = 2.5\text{nF}$, $R = 50\text{Ohm}$) | -40 | 125 | °C |

† Logic operational for V_S of -5 to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$.
 (Please refer to the Design Tip DT97-3 for more details).

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

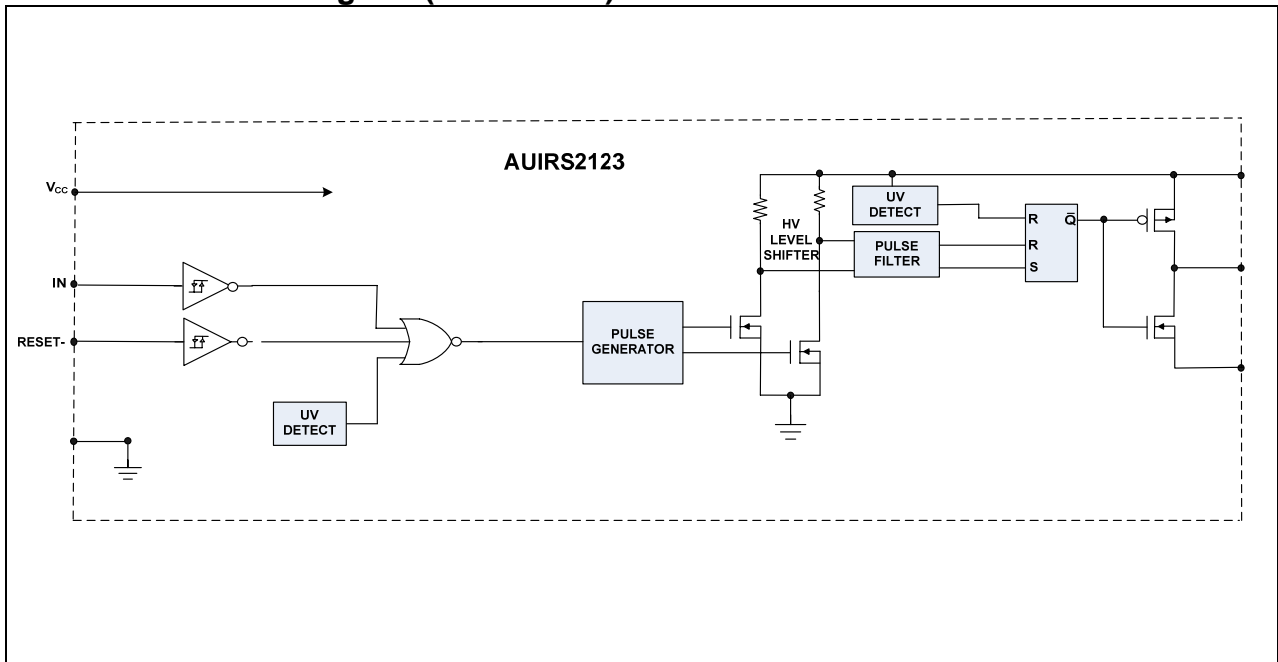
| Symbol | Definition | Min | Typ | Max | Units | Test Conditions | |
|-------------|---|-----------|------------|-----|---------------|---|-------------------|
| V_{IH} | Logic "1" input voltage | AUIRS2123 | 0.70 | — | — | V | |
| | Logic "0" input voltage | AUIRS2124 | * V_{CC} | — | — | | |
| V_{IL} | Logic "0" input voltage | AUIRS2123 | — | — | 0.35 | | |
| | Logic "1" input voltage | AUIRS2124 | — | — | * V_{CC} | | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | — | — | 2 | $I_O = 10$ mA | | |
| V_{OL} | Low level output voltage, V_O | — | 0.1 | 0.2 | | | |
| I_{LK} | Offset supply leakage current | — | — | 50 | μ A | $V_B = V_S = 600$ V | |
| I_{QBS} | Quiescent V_{BS} supply current | — | — | 240 | | $V_{IN} = 0$ V or V_{CC} | |
| I_{QCC} | Quiescent V_{CC} supply current | — | — | 500 | | $V_{IN} = V_{CC}$ | |
| I_{IN+} | Logic "1" input bias current | AUIRS2123 | — | — | | 5.0 | $V_{IN} = 0$ V |
| | | AUIRS2124 | — | — | | | $V_{IN} = V_{CC}$ |
| I_{IN-} | Logic "0" input bias current | AUIRS2123 | — | — | | 5.0 | $V_{IN} = V_{CC}$ |
| | | AUIRS2124 | — | — | | | |
| V_{BSUV+} | V_{BS} supply undervoltage positive going threshold | 7.2 | 8.6 | 9.6 | V | | |
| V_{BSUV-} | V_{BS} supply undervoltage negative going threshold | 6.6 | 8.0 | 9.0 | | | |
| V_{CCUV+} | V_{CC} supply undervoltage positive going threshold | 7.2 | 8.6 | 9.6 | | | |
| V_{CCUV-} | V_{CC} supply undervoltage negative going threshold | 6.6 | 8.0 | 9.0 | | | |
| I_{O+} | Output high short circuit pulsed current | 250 | 500 | — | mA | $V_O = 0$ V, $V_{IN} =$ Logic "1" $PW \leq 10$ μ s | |
| I_{O-} | Output low short circuit pulsed current | 250 | 500 | — | | $V_O = 15$ V, $V_{IN} =$ Logic "0" $PW \leq 10$ μ s | |

Dynamic Electrical Characteristics

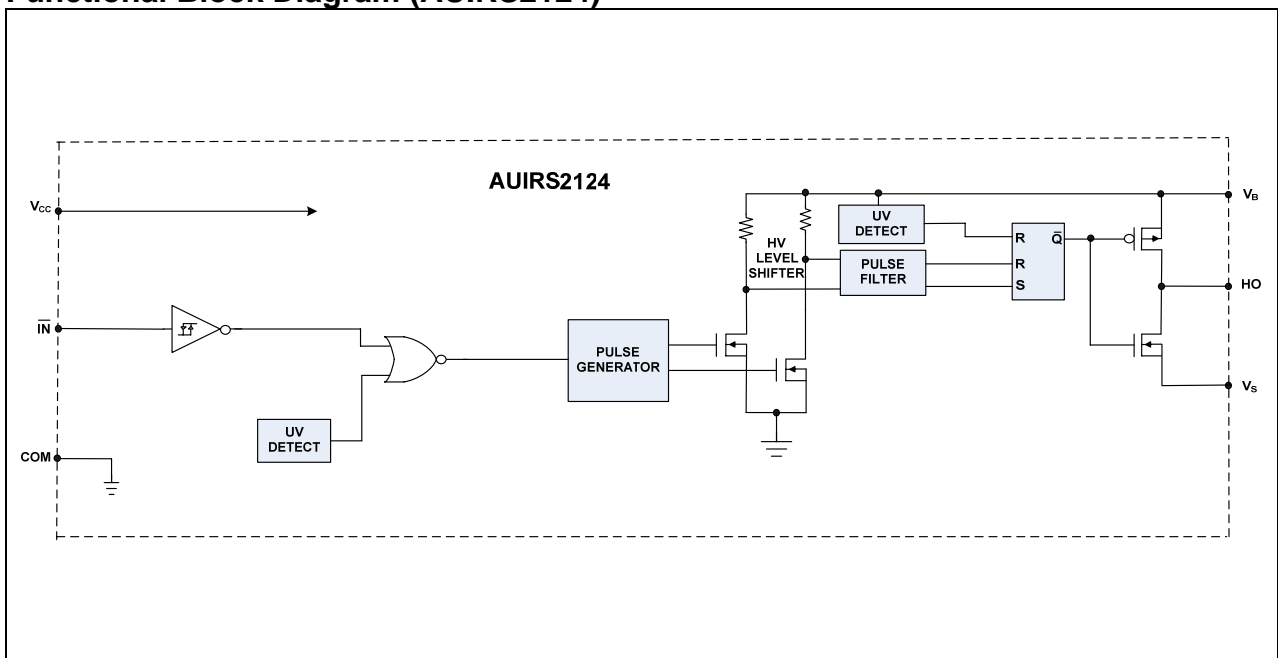
V_{BIAS} (V_{CC} , V_{BS}) = 15 V, C_L = 1000 pF, T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|-----------|---|-----|-----|-----|-------|-----------------|
| t_{on} | Turn-on propagation delay | — | 140 | 240 | ns | $V_S = 0$ V |
| t_{off} | Turn-off propagation delay | — | 140 | 240 | | $V_S = 600$ V |
| t_r | Turn-on rise time | — | 80 | 200 | | |
| t_f | Turn-off fall time | — | 80 | 200 | | |
| t_{RES} | RESET to output turn off propagation delay (AUIRS2123 only) | — | 170 | 300 | | |

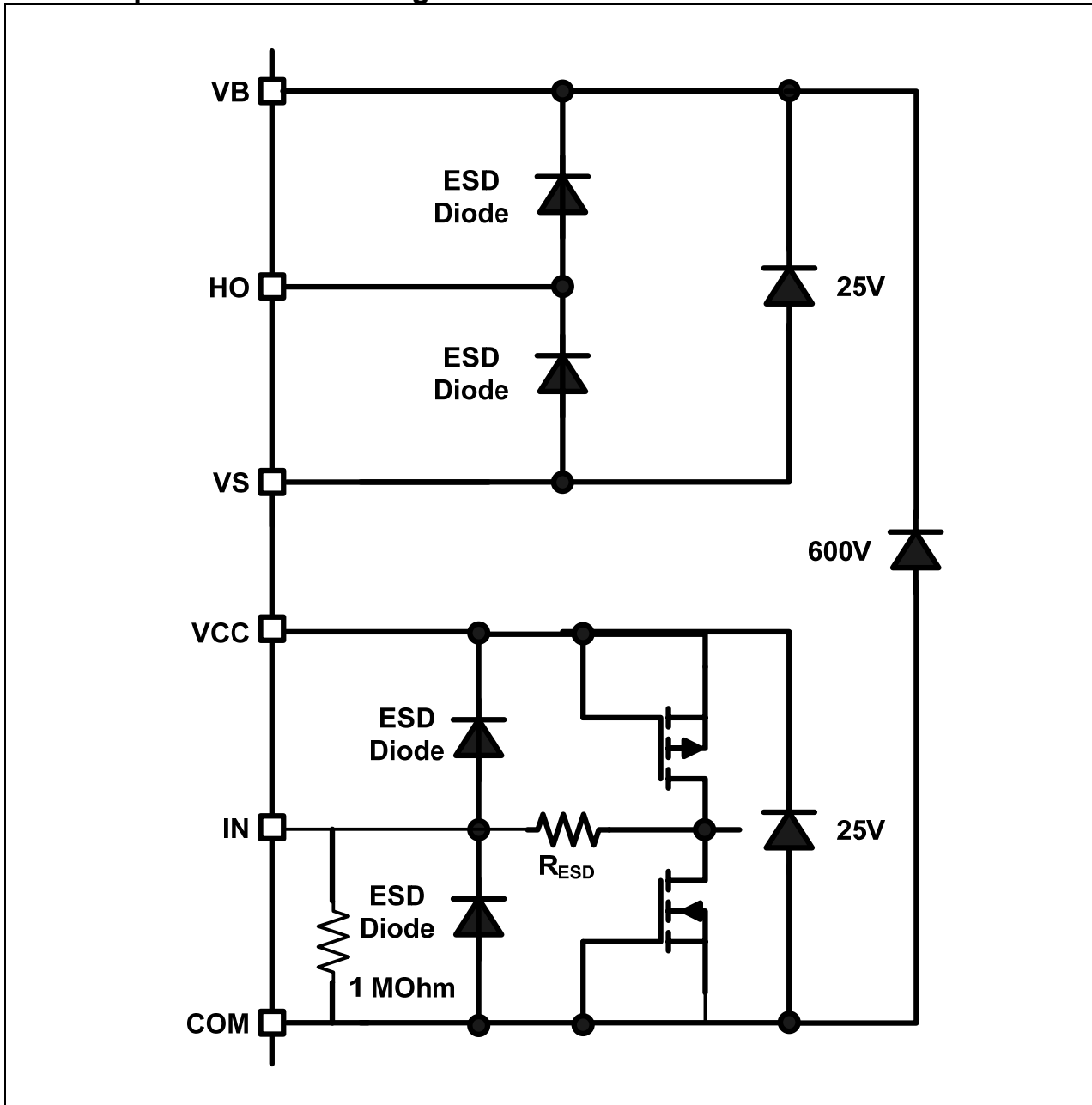
Functional Block Diagram (AUIRS2123)



Functional Block Diagram (AUIRS2124)

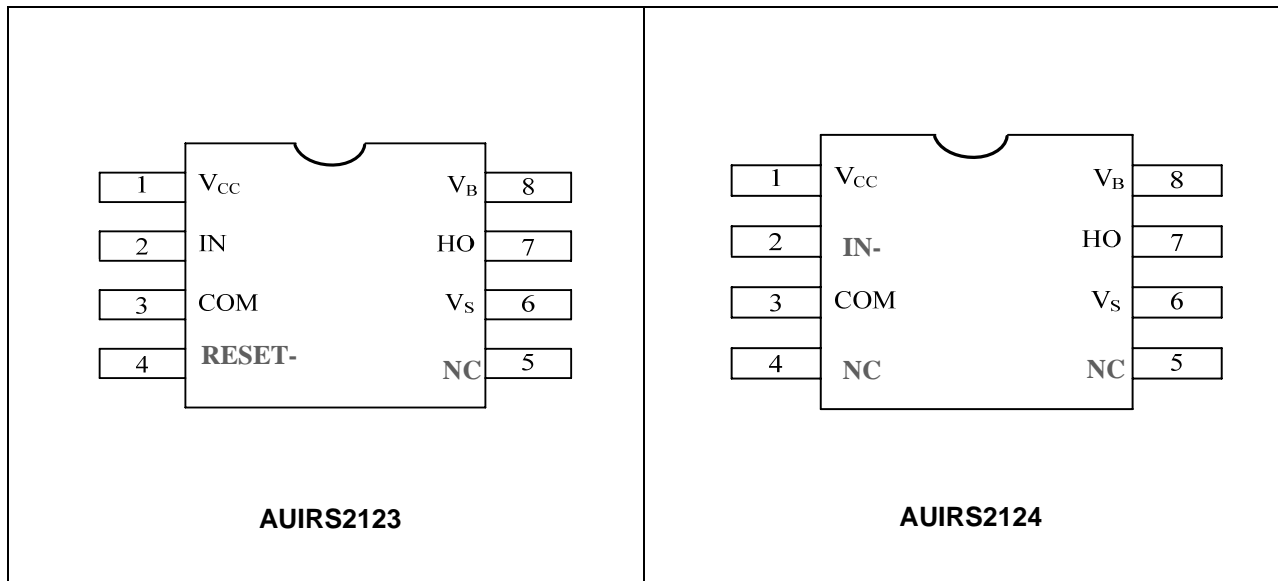


I/O Pin Equivalent Circuit Diagram



Lead Definitions

| Pin | Symbol | Pin description |
|-----|-----------------|--|
| 1 | V _{CC} | Low side and logic fixed supply |
| 2 | IN IN- | Logic input for gate driver output (HO), in phase with HO (AUIRS2123) Logic input for gate driver output (HO), out of phase with HO (AUIRS2124) |
| 3 | COM | Logic Ground |
| 4 | RESET- NC | Driver Enable Signal Input (negative logic) (AUIRS2123) No connection (AUIRS2124) |
| 5 | NC | No connection |
| 6 | V _S | High-side floating supply return |
| 7 | H _O | High-side gate drive output |
| 8 | V _B | High-side floating supply |



Application Information and Additional Details

AUIRS2123 logic table for V_{CC} , V_{BS} , RESET, IN, and H_o

| V_{CC} | V_{BS} | RESET- | IN | H_o |
|-----------------|-----------------|--------|------|-------|
| X | X | X | LOW | OFF |
| X | X | LOW | X | OFF |
| < $V_{CCUVLO-}$ | X | X | X | OFF |
| X | < $V_{BSUVLO-}$ | X | X | OFF |
| > $V_{CCUVLO+}$ | > $V_{BSUVLO+}$ | HIGH | HIGH | ON |

RESET = HIGH indicates that high side NMOS is allowed to be turned on.

RESET = LOW indicates that high side NMOS is OFF.

IN = HIGH indicates that high side NMOS is on.

IN = LOW indicates that high side NMOS is off.

X = independent

AUIRS2124 logic table for V_{CC} , V_{BS} , RESET, IN, and H_o

| V_{CC} | V_{BS} | IN- | H_o |
|-----------------|-----------------|------|-------|
| X | X | HIGH | OFF |
| < $V_{CCUVLO-}$ | X | X | OFF |
| X | < $V_{BSUVLO-}$ | X | OFF |
| > $V_{CCUVLO+}$ | > $V_{BSUVLO+}$ | LOW | ON |

IN- = HIGH indicates that high side NMOS is on.

IN- = LOW indicates that high side NMOS is off.

X = independent

Parameter Temperature Trends

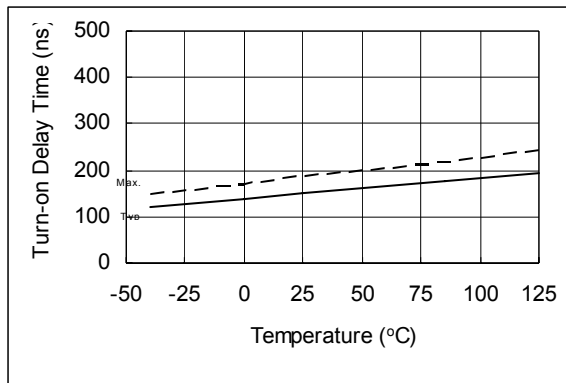


Figure 1A. Turn-on Delay Time vs. Temperature

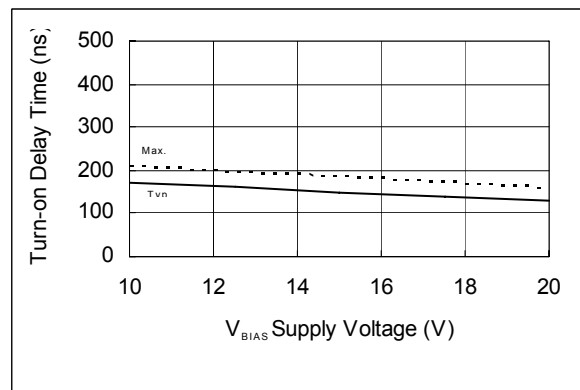


Figure 1B. Turn-on Delay Time vs. Supply Voltage

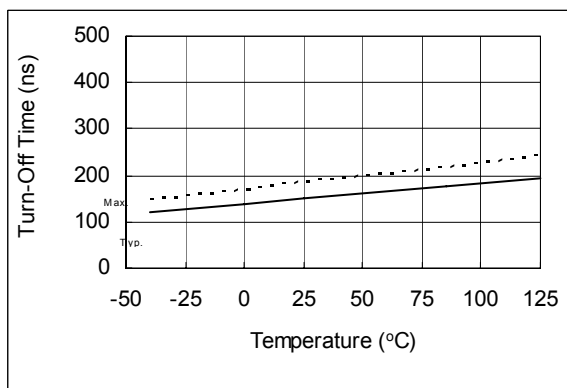


Figure 2A. Turn-Off Time vs. Temperature

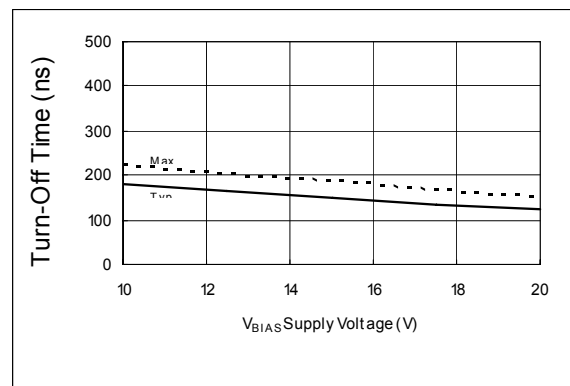


Figure 2B. Turn-Off Time vs. Supply Voltage

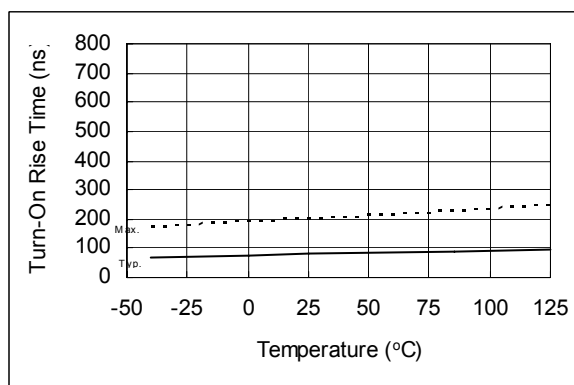


Figure 3A. Turn-On Rise Time (VBS=17V) vs. Temperature

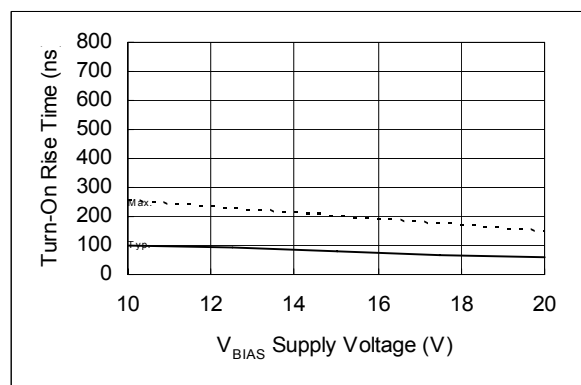


Figure 3B. Turn-On Rise Time (VBS=17V)

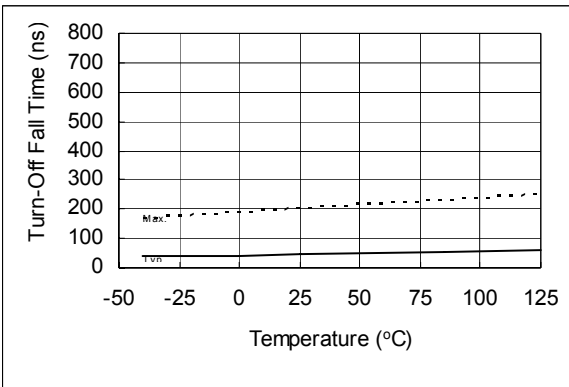


Figure 4A. Turn-Off Fall Time (V_{BS}=17V) vs. Temperature

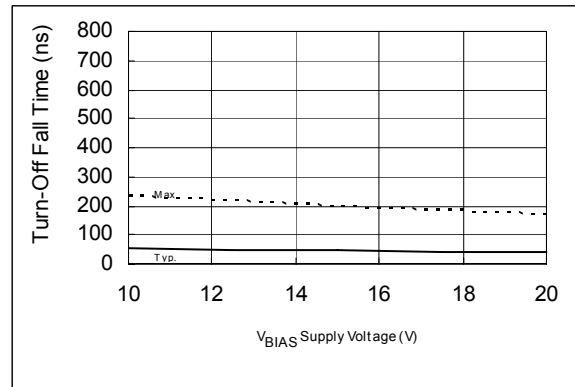


Figure 4B. Turn-Off Fall Time (V_{BS}=17V) vs. Supply Voltage

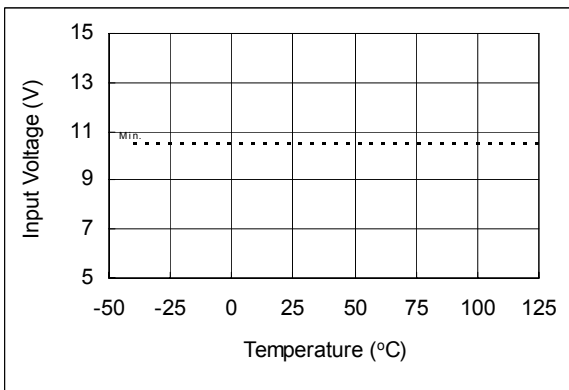


Figure 5A. Logic "1" Input Voltage vs. Temperature

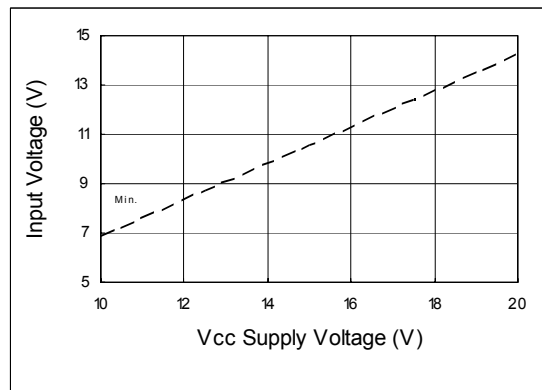


Figure 5B. Logic "1" Input Voltage vs. Supply Voltage

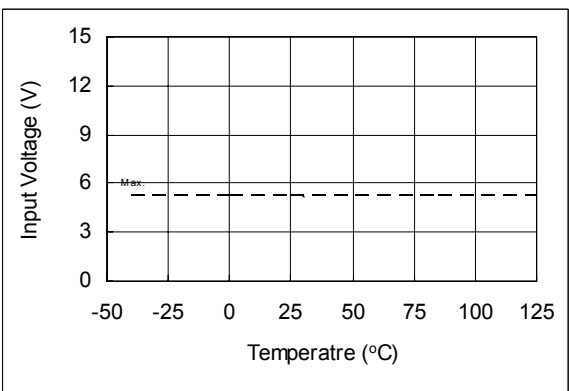


Figure 6A. Logic "0" Input Voltage vs. Temperature

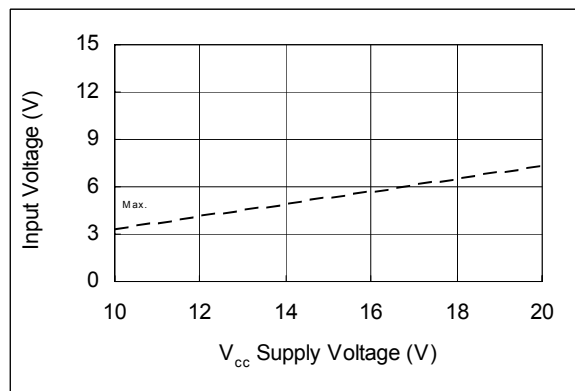


Figure 6B. Logic "0" Input Voltage vs. Supply Voltage

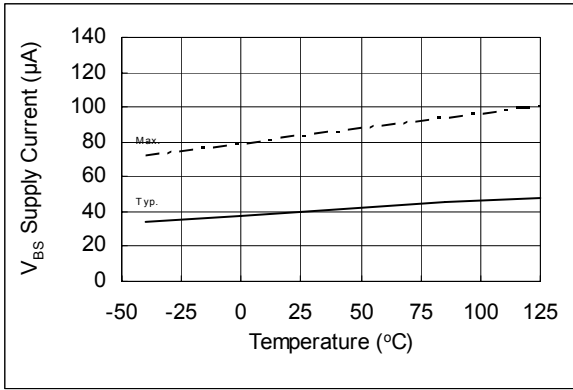


Figure 7A. VBS Supply Current vs. Temperature

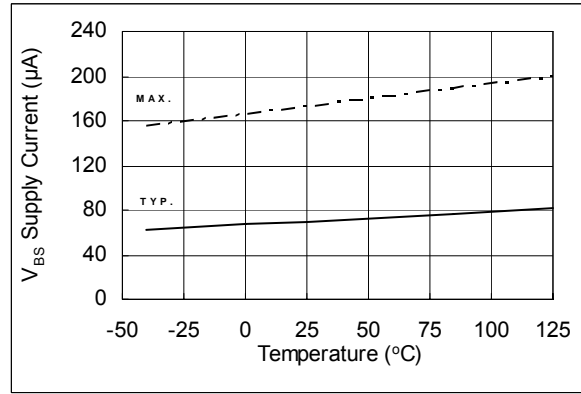


Figure 8A. VBS Supply Current vs. Temperature

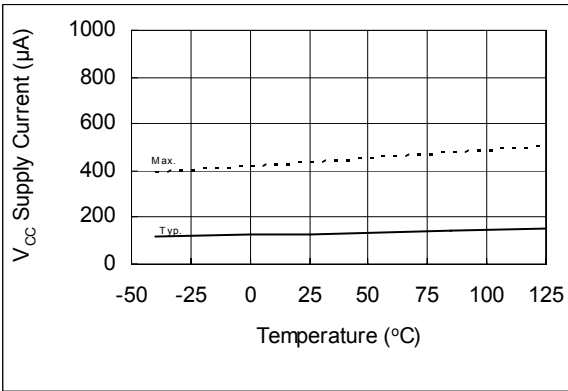


Figure 9A. Vcc Supply Current vs. Temperature

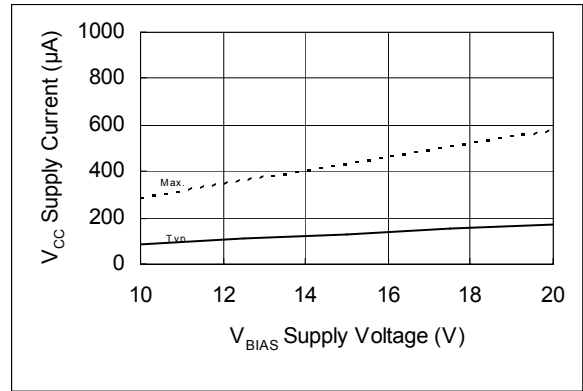


Figure 9B. Vcc Supply Current vs. Supply Voltage

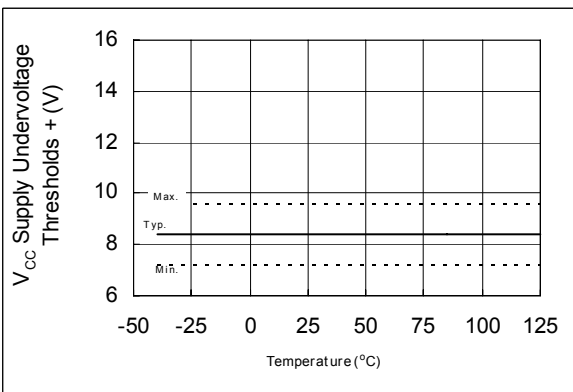


Figure 10A. Vcc Supply Undervoltage Threshold (+) vs. Temperature

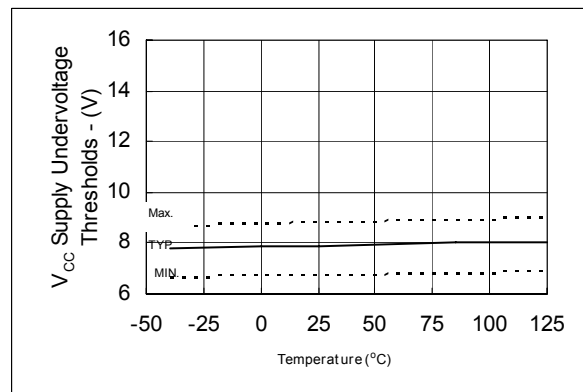


Figure 10B. Vcc Supply Undervoltage Threshold (-) vs. Temperature

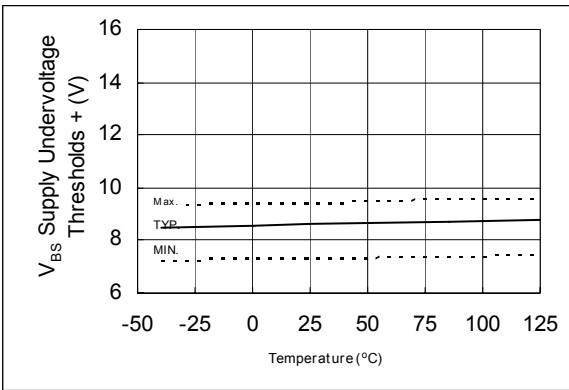


Figure 11A. VBS Supply Undervoltage Threshold (+) vs. Temperature

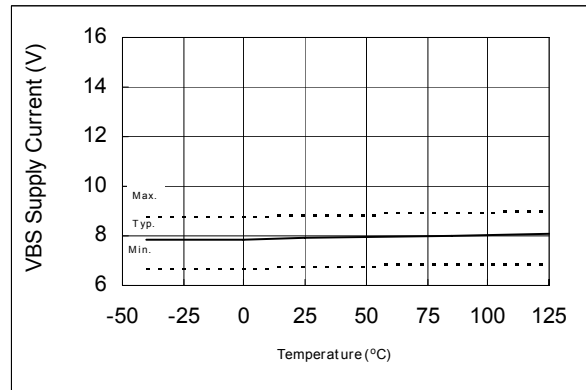


Figure 11B. VBS Supply Undervoltage Threshold (-) vs. Temperature

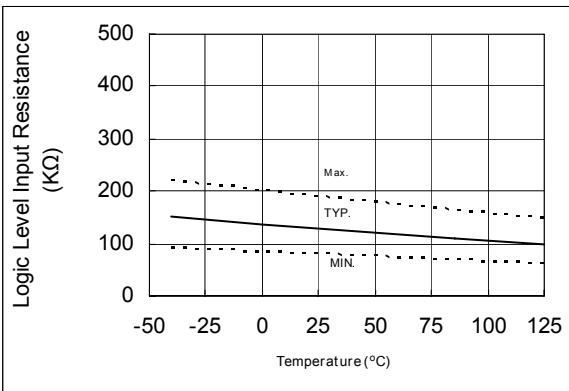


Figure 12. Logic Level Input Resistance vs. Temperature

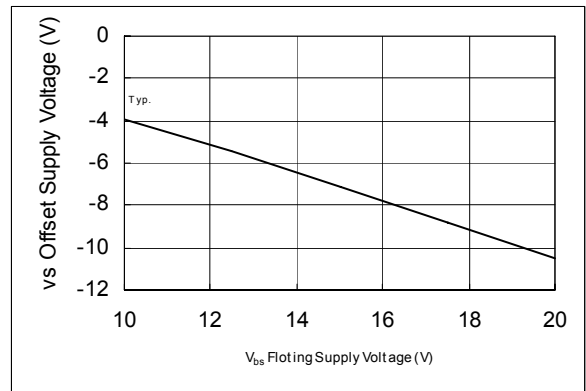
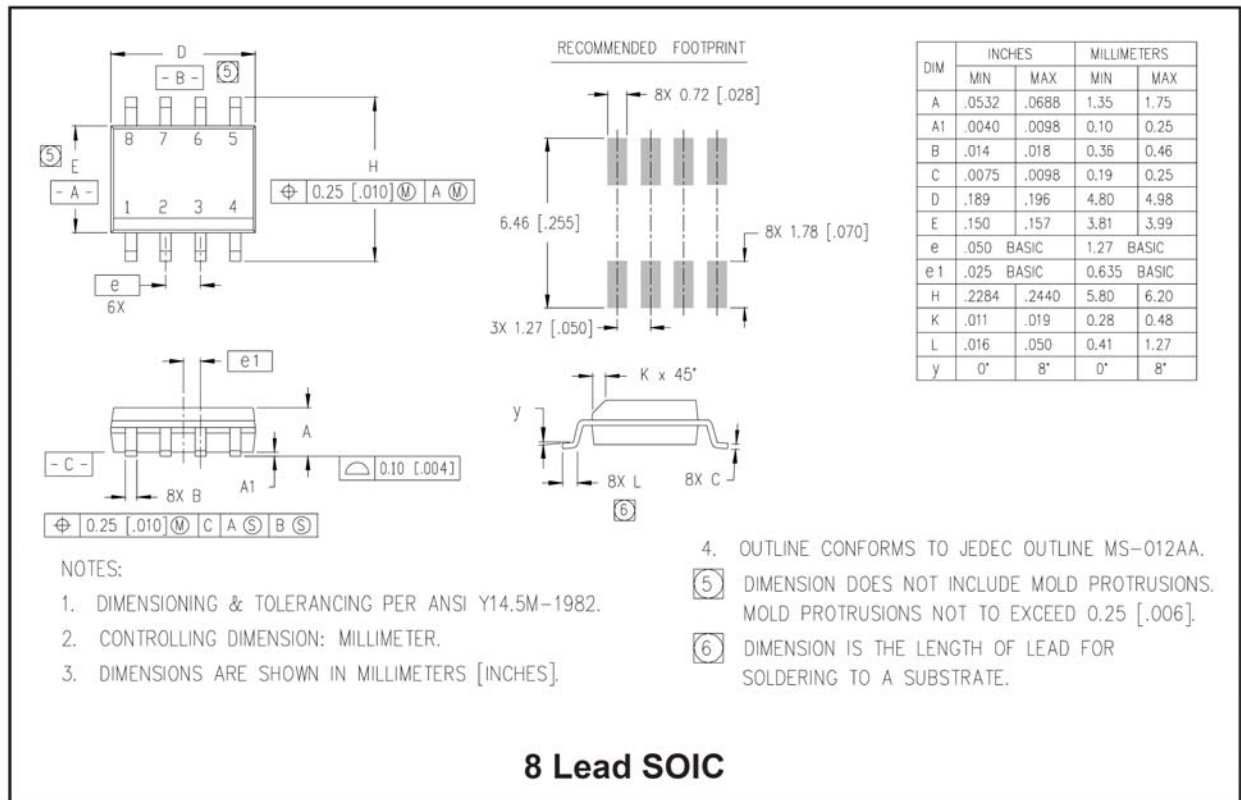
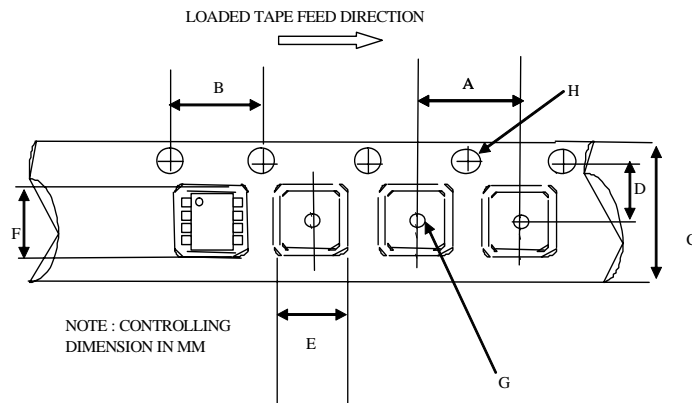


Figure 13. Maximum VS Negative Offset vs. Supply Voltage

Package Details

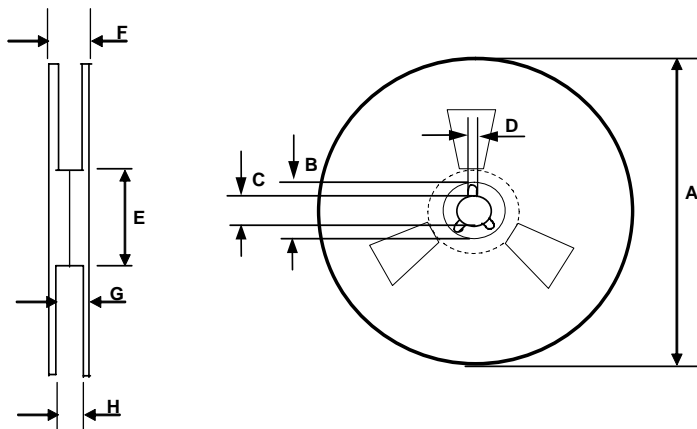


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

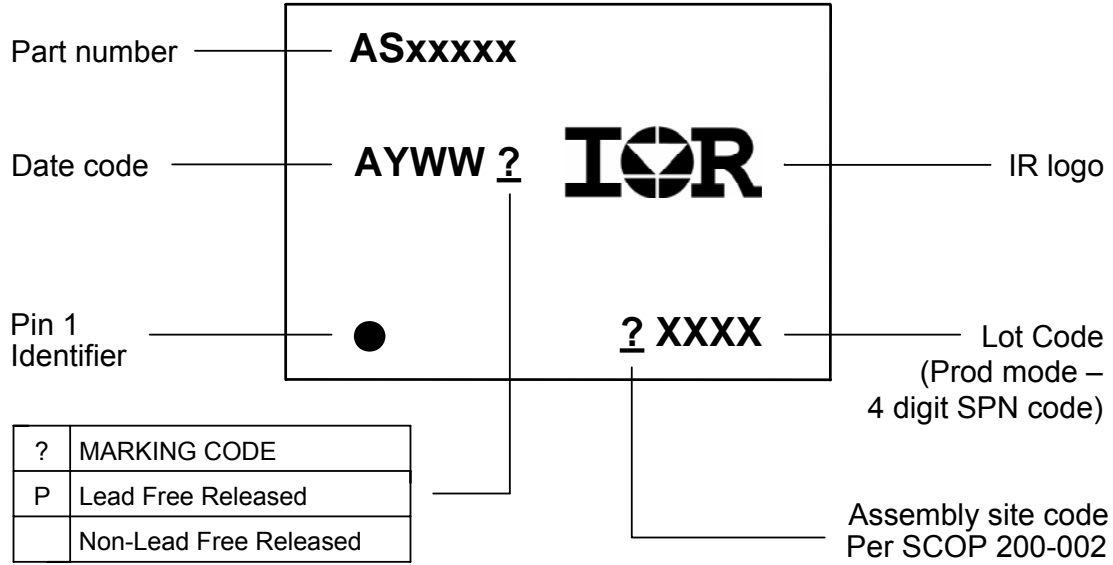
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 8SOICN

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

Part Marking Information



Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
| | | Form | Quantity | |
| AUIRS2123S | SOIC8 | Tube/Bulk | 95 | AUIRS2123S |
| | | Tape and Reel | 2500 | AUIRS2123STR |
| AUIRS2124S | SOIC8 | Tube/Bulk | 95 | AUIRS2124S |
| | | Tape and Reel | 2500 | AUIRS2124STR |

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Revision History

| Date | Comment |
|------|---------|
|------|---------|