Bridgeless SEPIC-derived LED Driver without Electrolytic Capacitor for Multistring Application

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Abstract— The widely used multi-stage cascade structure and the employed low-frequency diode rectified bridge in the front-end PFC rectifier, result in the low efficiency of LED drivers. Meanwhile, the electrolytic capacitor with large capacitance is used as decoupling capacitors is also an obstacle to the overall long-term reliability of the LED lighting product. To overcome these limitations, a bridgeless SEPIC-derived AC/DC converter without electrolytic capacitors is proposed in this paper. Furthermore its isolation type is easy to couple with our studied twin-bus configuration for increasing the overall efficiency of LED drivers. A 50-W hardware prototype has been designed, fabricated and tested in the laboratory to verify the converter validity under universal input voltage condition.

1. INTRODUCTION

Due to the rapid progress of in the semiconductor manufacture and package technology, LEDs have been considered for the general-purpose lighting [1]. Compared with conventional artificial light- sources, high power LEDs have numerous advantage, such as higher efficacy, a maximum of 100,000 h of lifetime, and so on [2]. Currently, to obtain sufficient luminance, many LEDs have to be connected and arranged in parallel LED strings. Driving multiple LED stings in parallel from an offline power source poses challenges in many aspects of power supply design. First of all, high power factor, and low-input-current harmonics are becoming the mandatory design criteria for LED drivers. In general lighting application, ballasts with input power exceeding 25-W are required to comply with stricter requirements as stated in IEC 61000-3-2-Class C [3] and Energy Star [4]. State-of-the-art LED driver shows that long lifetime and high efficiency are also the main design consideration of LED power supply for matching LED virtues. Additionally, the PWM dimming is also desired to further power saving.

A lot of work has been directed toward power factor correction (PFC) topologies and control schemes in LED application over the past decades [5–7]. These topologies are suitable for different power levels and customer requirements. However, these topologies have several common drawbacks. First of all, electrolytic capacitors with large capacitance are usually used as the storage capacitor in the previously mentioned LED lighting drivers. However, the lifetime of electrolytic capacitors is much shorter than the potential lifetime of LEDs. Hereafter, a low frequency diode rectified bridge is inserted between the EMI filter and the PFC stage, which degrade the overall system efficiency. Furthermore, the typical solution for LED drivers is employing the multi-stages cascade structure. Such a cascade configuration can help LEDs achieving good operating performance. However too many power handle stages results in the lower efficiency and relatively high cost.

This paper proposed a novel bridgeless SEPIC-derived AC/DC converter for LED lighting application. Though this topology appears similar to the presented bridgeless SEPIC circuit in [8], the operational characteristics are quite different. In the proposed circuit, the special DCM is employed to make the bus capacitor decouple the pulsating input power and constant output power. By allowing a relatively voltage ripple, the proposed AC/DC converter is able to eliminate electrolytic capacitors while maintaining desired the performances such as high power factor, low output ripple et al.. Additionally, this proposed circuit is not difficult to match our presented Twin-Bus configuration in [9]. The detailed operating principle and design consideration are described in the following sections. A laboratory prototype with 50-W power level has been built and tested to verify the presented topology.

2. PROPOSED BRIDGELESS AC/DC CONVERTER

Figure 1(a) shows the proposed bridgeless SEPIC-derived AC/DC converter. Though this topology appears similar to the presented bridgeless SEPIC circuit in [20], the operational characteristics

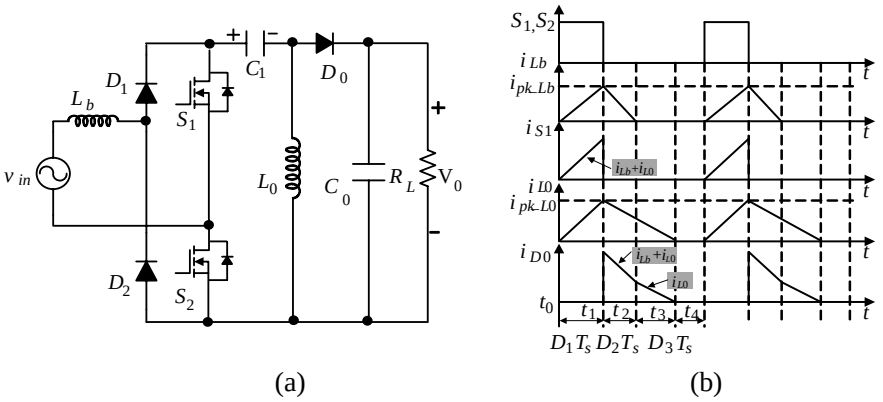

Figure 1: Proposed circuit and its main current waveforms in a switch cycle for positive half-line cycle. (a) Proposed bridgeless AC/DC Converter. (b) Theoretical waveforms in a switch cycle.

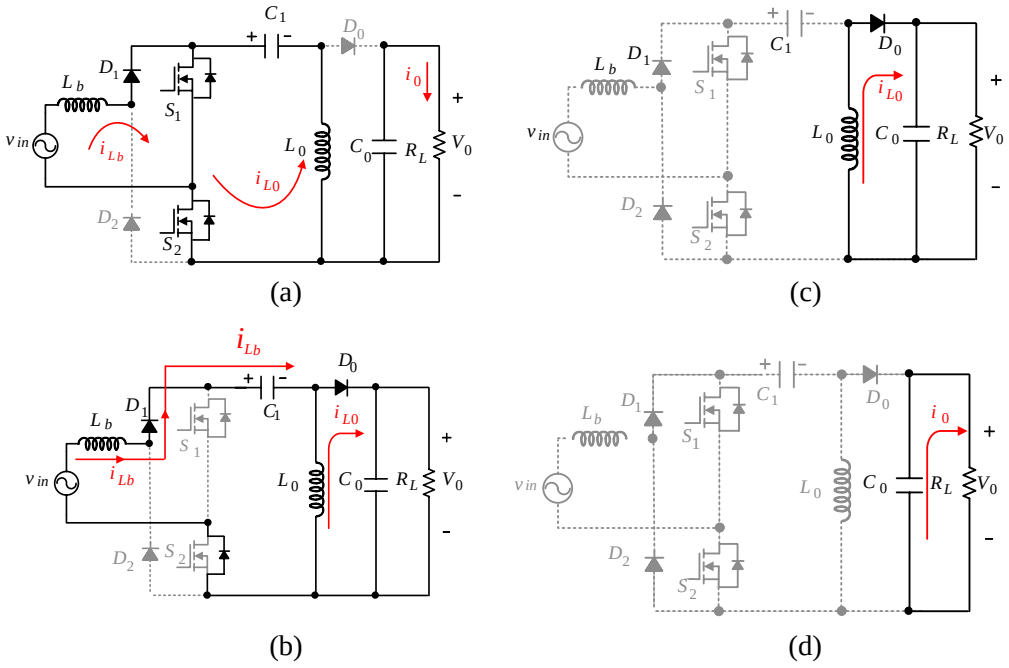

Figure 2: Equivalent circuit during the different interval. (a) Interval $[t_0, t_1]$. (b) Interval $[t_1, t_2]$. (c) Interval $[t_2, t_3]$. (d) Interval $[t_3, t_4]$.

are quite different. Before describing the operation principle, the following assumptions are made: (1) The input voltage v_{in} is ideal sinusoidal. (2) The switching frequency (f_s) is much higher than the ac line frequency (f_l). (3) The voltages V_{C1}, and V_0 can be considered constant during switching period T_s.

The operation of this converter is symmetrical in two half line cycles of input voltage. Therefore the converter operation is explained during one switching period in the positive half line cycle of the input voltage. The schematics operations during one switching cycle can be divided into four distinct intervals as shown by the equivalent circuits in Figure 2. The theoretical waveforms during a switching period are plotted in Figure 1(b). The converter analysis starts at the instant t_0.

Interval 1: $[t_0, t_1]$: Prior to this interval, the currents through L_b and L_0 are at zero level. This mode starts by turning S_1 and S_2 on. When the switch S_1 and S_2 is turned on at t_0 simultaneously, the diodes D_0 is reverse biased. Therefore, capacitor C_1 is as the charging power supply of inductance L_0. The corresponding equivalent circuit is shown in Figure 2(a). Hence, the currents i_{Lb} and i_{L0} begin to increase linearly by slope of v_{in}/L_b and V_{C1}/L_0 as shown as Figure 1(b), respectively. This interval ends by turning off the switch S_1 and S_2. Based on the aforementioned operation,

the following equations can be derived:

$$i_{L_b}(t) = \frac{v_{in}}{L_b}t \tag{1}$$

$$i_{L_0}(t) = \frac{V_{C_1}}{L_0}t \tag{2}$$

$$i_{S_1} = i_{L_b}(t) + i_{L_0}(t) = \left(\frac{v_{in}}{L_b} + \frac{V_{C_1}}{L_0}\right)t \tag{3}$$

Interval 2: $[t_1, t_2]$: When the switch S_1 and S_2 are turned off, capacitor C_1 is as the discharging power supply of inductance L_b. Meanwhile the output diode D_0 begins to conduct carrying the sum of i_{Lb} and i_{L0}. Thus, currents i_{Lb} and i_{L0} decrease linearly at rates proportional to $(V_{C1} + V_0 - v_{in})$ and V_0, respectively. The corresponding current waveforms are shown in D_2T_S of Figure 1(b). Figure 2(b) shows the equivalent circuit at this interval. This interval is not ends until the current i_{Lb} reaches zero level. Similarly, the current of inductor L_b and L_0 (i_{Lb} and i_{L0}) and diode current i_{D0} can be described approximately as:

$$i_{L_b}(t) = \frac{v_{in}}{L_b}D_1T_s + \frac{V_{in} - V_{C1} - V_0}{L_b}t \tag{4}$$

$$i_{L_0}(t) = \frac{V_{C_1}}{L_0}D_1T_s - \frac{V_0}{L_0}t \tag{5}$$

$$i_{D_0}(t) = \left(\frac{v_{in}}{L_b} + \frac{V_{C_1}}{L_0}\right)D_1T_s + \frac{v_{in} - V_{C1}}{L_b}t - \left(\frac{V_0}{L_0} + \frac{V_0}{L_b}\right)t \tag{6}$$

Interval 3: $[t_2, t_3]$: In this interval, the current i_{L0} continues to decrease through the output diode D_0. This interval ends when the current of D_0 reaches zero. The corresponding equivalent circuit is plotted in Figure 2(c).

Interval 4: $[t_3, t_4]$: This interval is a freewheeling stage where all semi-conductors are off and all branch currents are zero. The converter stays in this state until the switch S_1 and S_2 are turned on again.

3. CONTROL STRATEGY

It needs to note that the switches S_1 and S_2 can be driven in the following two ways: (1) as shown in Figure 3(b), the switch S_1 and S_2 are driven by the same signal with switching frequency f_s; (2) the switch S_2 keep turning on at the positive half line cycle, the switch S_1 is turned on and off with switching frequency f_s. Accordingly, the switch S_1 keeps turning on at the negative half line cycle. In this paper, to make the control circuit be simply, the driven way (1) is employed.

From the operation principle descripted in Section 2, the voltage control mode only is good enough to adjust constant output voltage. Figure 3 shows the detailed implemented circuit of the aforementioned control strategy. Driver IC IR2110s is used to drive switch S_1 and S_2 with same control signal. Although control IC UCC38C44 is designed based on peak current mode, it is not difficult to modify as voltage control mode by adding resister R_{S1}, R_{S2} and bipolar transistor Q_1. In addition, FOD2742 is 8-PIN SOIC error amplifier optocoupler consisting of the popular KA431 precision programmable shunt reference and an optocoupler, which is employed to implement isolation and output feedback regulation.

4. EXPERIMENTAL VERIFICATION

To verify the presented bridgeless SEPIC-derived AC/DC converter, a laboratory prototype with the following specifications was designed and tested. The prototype is arranged with Twin-Bus output stage to comply with the Twin-Bus configuration. Universal input voltage: $v_{in} = 90v_{ac}$, 60 Hz. Twin-bus output voltage: $V_{01} = 50V_{dc}$, $V_{02} = 45V_{dc}$. Rated output power: $P_0 = 50$ W. Switching frequency: $f_s = 53$ kHz.

The schematic diagram of the laboratory prototype is shown in Figure 4, which was used to convert the universal ac line voltage into the twin-bus voltage V_{01} and V_{02}, and provides a high power factor and low harmonics to meet the standard such as IEC 61000-3-2 Class C. The PFC inductor L_b is split into two smaller ones (L_{b1} and L_{b2}) integrated in same core to reduce the common-mode EMI.

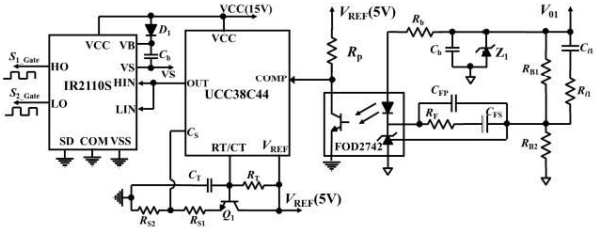

Figure 3: Control strategy and implemented circuit.

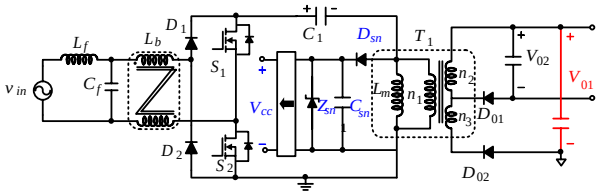

Figure 4: Bridgeless SEPIC-derived AC/DC converter with twin-bus output.

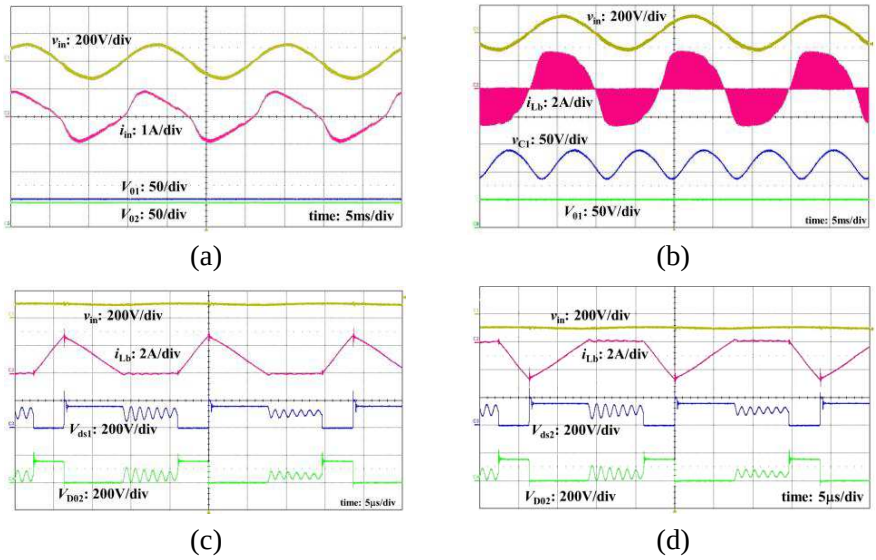

Figure 5: Experimental results under 90 V input voltage condition. (a) Measured v_{in}, i_{in}, V_{01} and V_{02}. (b) Measured v_{in}, i_{Lb}, v_{C1} and V_{01}. (c) Experimental waveform at peak value of the positive half cycle. (d) Experimental waveform at peak value of the negative half cycle.

Figure 5 shows the experimental waveform at 90 V input voltage and full load. In Figure 5(a), the input current i_{in} have a near-sinusoidal waveform and is in phase with the input voltage v_{in}. Thus the high PF with 0.96 can be achieved. The third and fourth channel in Figure 5(a) shows the measured waveform of output voltage V_{01} and V_{02}. As can be seen, the output voltage is regulated well with small voltage ripple. Figure 5(b) is the experimental waveforms of inductor current i_{Lb} and bus voltage v_{C1}. It can be observed that the capacitor voltage v_{C1} bhas the relatively large double line-frequency (120 Hz) ripple Δv_{C1}. Meanwhile, the waveforms of V_{ds1}, V_{ds2}, V_{D02} during the switching period T_s are provided for the positive and negative half line cycle of the input voltage v_{in}, respectively.

5. CONCLUSION

A bridgeless SEPIC-derived AC/DC topology without electrolytic capacitors is studied in this paper. The basic circuit operating principle and design consideration are described in detail to achieve the desired performance. Its isolation type is easy to couple with our proposed twin-bus configuration for increasing the total efficiency of LED drivers.

Additionally, it is noteworthy that the way (2) can be employed to further improve the efficiency. Future work is to improve the efficiency by this operation mode.

ACKNOWLEDGMENT

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