microID™ 13.56 MHz RFID System Design Guide

NEW CUSTOMER NOTIFICATION SYSTEM

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

DATA SHEET MARKINGS

Microchip uses various data sheet markings to designate each document phase as it relates to the product development stage. The markings appear at the bottom of the data sheet, between the copyright and document and page numbers. The definitions for each marking are provided below for your use.

Marking	Description
Advance Information	The information is on products in the design phase. Your designs should not be finalized with this information as revised information will be published when the product becomes available.
Preliminary	This is preliminary information on new products in production but not yet fully characterized. The specifications in these data sheets are subject to change without notice. Before you finalize your design, please ensure that you have the most current revision of the data sheet by contacting your Microchip sales office.
No Marking	Information contained in the data sheet is on products in full production.

Trademarks

DNV Certification, Inc. USA — ANSI-RAB QMS ACCREDITED — DNV MSC The Netherlands Accredited by the RvA — DNV — ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

Table of Contents

Table of Contents

AN680

Passive RFID Basics

Author: *Youbok Lee and Pete Sorrells*
Microchip Technology Inc.

INTRODUCTION

Radio Frequency Identification (RFID) systems use radio frequency to identify, locate and track people, assets and animals. Passive RFID systems are composed of three components – a reader (interrogator), passive tag and host computer. The tag is composed of an antenna coil and a silicon chip that includes basic modulation circuitry and non-volatile memory. The tag is energized by a time-varying electromagnetic radio frequency (RF) wave that is transmitted by the reader. This RF signal is called a *carrier signal*. When the RF field passes through an antenna coil, there is an AC voltage generated across the coil. This voltage is rectified to result in a DC voltage for the device operation. The device becomes functional when the DC voltage reaches a certain level. The information stored in the device is transmitted back to the reader. This is often called backscattering. By detecting the backscattering signal, the information stored in the device can be fully identified.

There are two classes of RFID device depending on type of memory cell : (a) read only device and (b) read and write device. The memory cell can be made of EEPROM or FRAM. EEPROM is based on CMOS silicon and FRAM is based on ferroelectric memory. Since CMOS process technology has been matured, the EEPROM can be produced relatively at lower cost than the FRAM device. However, FRAM based RFID device consumes less power which is desirable for low power device. Therefore, it is known as a good candidate for the future RFID device, if its manufacturing cost becomes compatible to that of the CMOS technology.

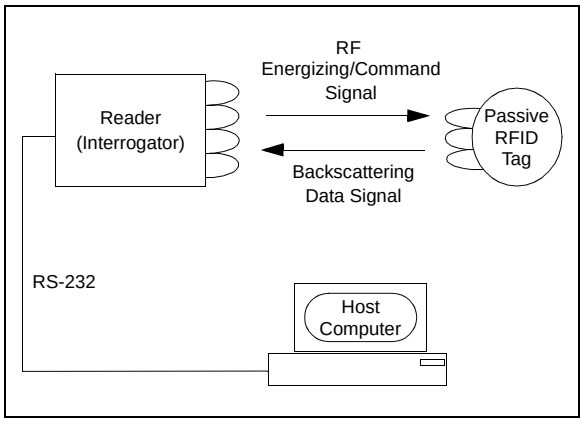
Because of its simplicity for use, the passive RFID system has been used for many years in various RF remote sensing applications. Specifically in access control and animal tracking applications.

In recent years, there have been dramatic increases in application demands. In most cases, each applications uses a unique packaging form factor, communication protocol, frequency, etc. Because the passive tag is remotely powered by reader's RF signal, it deals with very small power (~ μw). Thus, the read range (communication distance between reader and tag) is typically limited within a proximity distance. The read range varies with design parameters such as frequency, RF power level, reader's receiving sensitivity, size of antenna, data rate, communication protocol, current consumptions of the silicon device, etc.

Low frequency bands (125 kHz – 400 kHz) were traditionally used in RFID applications. This was because of the availability of silicon devices. Typical carrier frequency (reader's transmitting frequency) in today's applications range from 125 kHz – 2.4 GHz.

In recent years, the applications with high frequency (4 – 20 MHz) and microwave (2.45 GHz) bands have risen with the advent of new silicon devices. Each frequency band has advantages and disadvantages. The 4 – 20 MHz frequency bands offer the advantages of low (125 kHz) frequency and microwave (2.4 GHz) bands. Therefore, this frequency band becomes the most dominant frequency band in passive RFID applications.

FIGURE 1: SIMPLE CONFIGURATION OF RFID SYSTEMS



DEFINITIONS

READER, INTERROGATOR

RFID reader is used to activate passive tag with RF energy and to extract information from the tag.

For this function, the reader includes RF transmission, receiving and data decoding sections. In addition, the reader includes a serial communication (RS-232) capability to communicate with the host computer. Depend-

ing on the complexity and purpose of applications, the reader's price range can vary from ten dollars to a few thousand dollar worth of components and packaging.

The RF transmission section includes an RF carrier generator, antenna and a tuning circuit. The antenna and its tuning circuit must be properly designed and tuned for the best performance. See Application Note AN710 (DS00710) for the antenna circuit design.

Data decoding for the received signal is accomplished using a microcontroller. The firmware algorithm in the microcontroller is written in such a way to transmit the RF signal, decode the incoming data and communicate with the host computer.

Typicall, reader is a read only device, while the reader for read and write device is often called interrogator. Unlike the reader for read only device, the interrogator uses command pulses to communicate with tag for reading and writing data.

TAG

Tag consists of a silicon device and antenna circuit.

The purpose of the antenna circuit is to induce an energizing signal and to send a modulated RF signal. The read range of tag largely depends upon the antenna circuit and size.

The antenna circuit of tag is made of LC resonant circuit or E-field dipole antenna, depending on the carrier frequency. The LC resonant circuit is used for the frequency of less than 100 MHz. In this frequency band, the communication between the reader and tag takes place with magnetic coupling between the two antennas through the magnetic field. The antenna utilizing the inductive coupling is often called magnetic dipole antenna.

The antenna circuit must be designed such a way to maximize the magnetic coupling between them. This can be achieved with the following parameters:

a) LC circuit must be tuned to the carrier frequency of the reader
b) Maximize Q of the tuned circuit
c) Maximize antenna size within physical limit of application requirement.

See Application Note AN710 for more details.

When the frequency goes above 100 MHz, the requirement of LC values for its resonant frequency becomes too small to realize with discrete L and C components. As frequency increases, the wavelength is getting shorter. In this case, a true E-field antenna can be made of a simple conductor that has linear dimension less than or equivalent to half (½) the wavelength of the signal. The antenna that is made of a simple conductor is called electric dipole antenna. The electric dipole antenna utilizes surface current that is generated by an electric field (E-Field). The surface current on the conductor produces voltage at load. This voltage is used to energize the silicon device. Relatively simple antenna structure is formed for the higher frequency compared to the lower frequency.

READ ONLY DEVICE, READ/WRITE DEVICE:

For the read only device, the information that is in the memory can't be changed by RF command once it has been written.

Read only devices are programmed as follows: (a) in the factory as a part of manufacturing process, (b) contactlessly programmed one time after the manufacturing (MCRF200 and MCRF250) or (c) can be programmed and also reprogrammed in contact mode (MCRF355 and MCRF360).

A device with memory cells that can be reprogrammed by RF commands is called read/write device. The information in the memory can be reprogrammed by Interrogator command.

Memory in today's RFID device is made of (a) CMOS or (b) FRAM array. The CMOS memory cell needs higher voltage for writing than reading. In the passive read/write device, the programming voltage is generated by multiplying the rectified voltage. The voltage multiplier circuit is often called a charge pumper. In addition to the programming voltage, the read/write device needs command decoder and other controller logics. As a result, the read/write device needs more circuit building blocks than that of the read only device. Therefore, the device size is larger and cost more than a read only device. The FRAM device needs the same voltage for reading and writing. However, its manufacturing cost is much higher than CMOS technology. Most of RFID device available today's market place are CMOS based device.

READ/WRITE RANGE

Read/write range is a communication distance between the reader (Interrogator) and tag. Specifically, the read range is a maximum distance to read data out from the tag and write range is a maximum distance to write data from interrogator to tag.

The read/write range is related to:

(1) Electromagnetic coupling of the reader (interrogator) and tag antennas, (2) RF Output power level of reader (interrogator), (3) Carrier frequency bands, (4) Power consumption of device, etc.

The electromagnetic coupling of reader and tag antennas increases using similar size of antenna with higher Q in both sides. The read range is improved by increasing the carrier frequency. This is due to the gain in the radiation efficiency of the antenna as the frequency increases. However, the disadvantage of high frequency (900 MHz - 2.4 GHz) application are shallow skin depth and narrower antenna beam width. These cause less penetration and more directional problem,

respectively. Low frequency application, on the other hand, has advantage in the penetration and directional, but a disadvantage in the antenna performance.

The read range increases by reducing the current consumptions in the silicon device. This is because additional radiating power is available by reducing the power dissipation in the silicon device.

MODULATION PROTOCOL

The passive RFID tag uses backscattering of the carrier frequency for sending data from the tag to reader. The amplitude of backscattering signal is modulated with modulation data of the tag device. The modulation data can be encoded in the form of ASK (NRZ or Manchester), FSK or PSK. Therefore, the modulation signal from the tag is Amplitude-Amplitude, Amplitude-FSK and Amplitude-PSK. See MicroID 125 kHz Design Guide for Amplitude, Amplitude-FSK and Amplitude-PSK reader.

CARRIER

Carrier is the transmitting radio frequency of reader (interrogator). This RF carrier provides energy to the tag device, and is used to detect modulation data from the tag using backscattering. In read/write device, the carrier is also used to deliver interrogator's command and data to the tag.

Typical passive RFID carrier frequencies are:

a) 125 kHz - 400 kHz
b) 4 MHz - 24 MHz
c) 900 MHz - 2.45 GHz.

The frequency bands must be selected carefully for applications because each one has its own advantages and disadvantages. Table 1 shows the characteristic of each frequency bands.

TABLE 1:

Frequency Bands	Antenna Components	Read Range (typical)	Penertration (skin depth)	Orientation (Directionality)	Usability in metal or humid environment	Applications (typical)
Low Frequency (125 - 400) kHz	Coil (> 100 turns) and capacitor	Proximity (8")	Best	Least	Possible	Proximity
Medium Frequency (4 MHz - 24 MHz)	Coil (< 10 turns) and capacitor	Medium (15")	Good	Not much	Possible	Low cost and high volume
High Frequency (>900 MHz)	E-field dipole (a piece of conductor)	Long (> 1 m)	Poor	Very high	Difficult	Line of sight with long range

SYSTEM HANDSHAKE

Typical handshake of a tag and reader (interrogator) is as follows:

A. Read Only Tag

1. The reader continuously transmits an RF signal and watches always for modulated backscattering signal.
2. Once the tag has received sufficient energy to operate correctly, it begins clocking its data to a modulation transistor, which is connected across the antenna circuit.
3. The tag's modulation transistor shorts the antenna circuit, sequentially corresponding to the data which is being clocked out of the memory array.
4. Shorting and releasing the antenna circuit accordingly to the modulation data causes amplitude fluctuation of antenna voltage across the antenna circuit.
5. The reader detects the amplitude variation of the tag and uses a peak-detector to extract the modulation data.

B. Read and Write Tag

(Example: MCRF45X devices with FRR and Reader Talks First mode)

1. The interrogator sends a command to initiate communication with tags in the fields. This command signal is also used for energizing the passive device.
2. Once the tag has received sufficient energy and command, it responses back with its ID for acknowledgment.
3. The interrogator now knows which tag is in the field. The interrogator sends a command to the identified tag for what to do next: processing (read or write) or sleep.
4. If the tag receive processing and reading commands, it transmits a specified block data and waits for the next command.
5. If the tag receives processing and writing commands along with block data, it writes the block data into the specified memory block, and transmits the written block data for verification.
6. After the processing, the interrogator sends an "end" command to send the tag into the sleep ("silent") mode.
7. If the device receives "end" command after processing, it sends an acknowledgement (8-bit preamble) and stays in sleep mode. During the sleep mode, the device remains in non-modulating (detuned) condition as long as it remains in the power-up. This time the handshake is over.
8. The interrogator is now looking for the next tag for processing, establishes an handshake and repeats the processing.
9. See Figure 4-1 in MCRF45X data sheet for more details.

BACKSCATTER MODULATION

This terminology refers to the communication method used by a passive RFID tag to send data to the reader using the same reader's carrier signal. The incoming RF carrier signal to the tag is transmitted back to the reader with tag's data.

The RF voltage induced in the tag's antenna is amplitude-modulated by the modulation signal (data) of tag device. This amplitude-modulation can be achieved by using a modulation transistor across the LC resonant circuit or partially across the resonant circuit.

The changes in the voltage amplitude of tag's antenna can affect on the voltage of the reader antenna. By monitoring the changes in the reader antenna voltage (due to the tag's modulation data), the data in the tag can be reconstructed.

The RF voltage link between reader and tag antennas are often compared to a weakly coupled transformer coils; as the secondary winding (tag coil) is momentarily shunted, the primary winding (reader coil) experiences a momentary voltage drop.

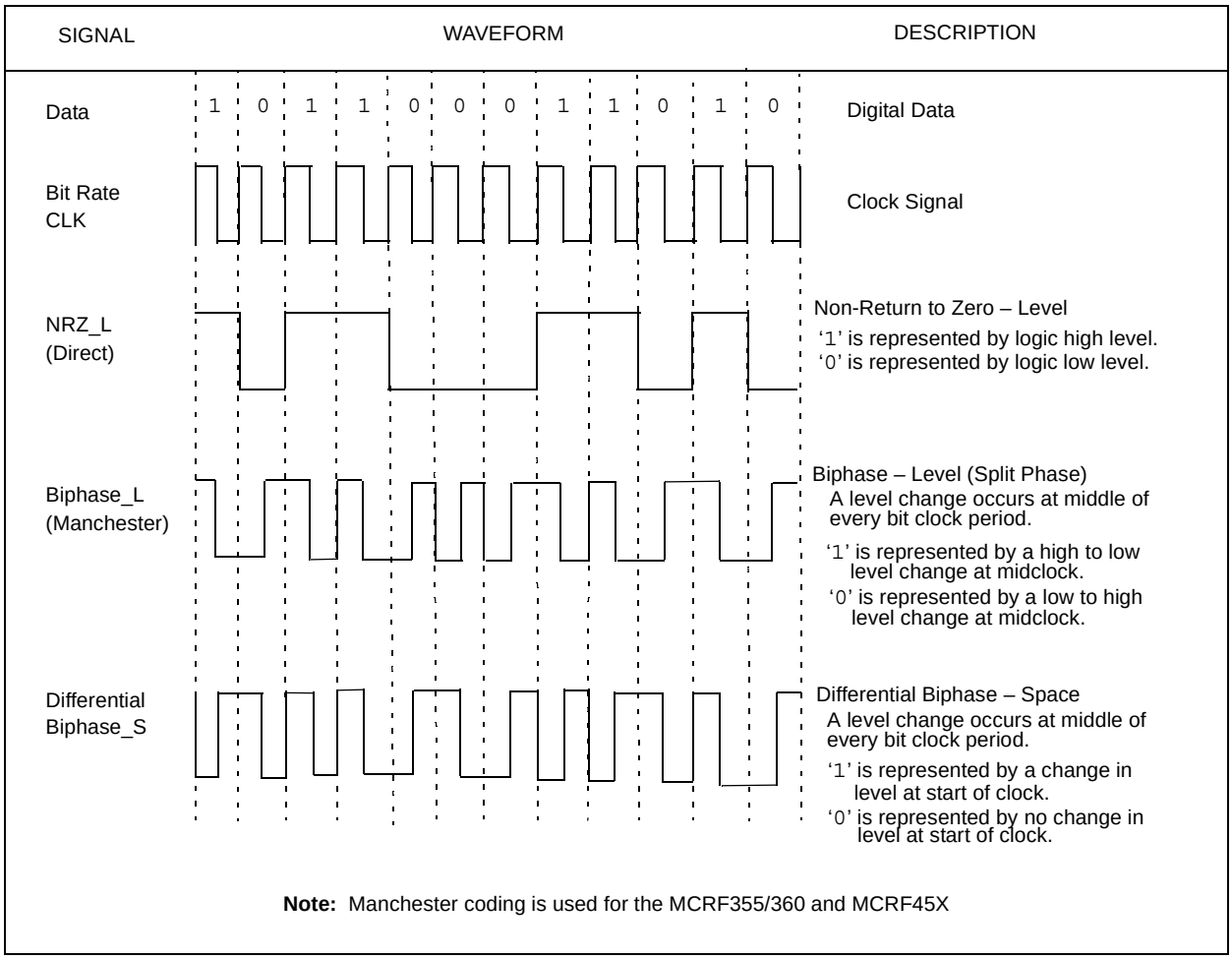
DATA ENCODING

Data encoding refers to processing or altering the data bitstream in-between the time it is retrieved from the RFID chip's data array and its transmission back to the reader. The various encoding algorithms affect error recovery, cost of implementation, bandwidth, synchronization capability and other aspects of the system design. Entire textbooks are written on the subject, but there are several popular methods used in RFID tagging today:

1. **NRZ (Non-Return to Zero) Direct.** In this method no data encoding is done at all; the 1's and 0's are clocked from the data array directly to the output transistor. A low in the peak-detected modulation is a '0' and a high is a '1'.
2. **Differential Biphase.** Several different forms of differential biphase are used, but in general the bitstream being clocked out of the data array is modified so that a transition always occurs on every clock edge, and 1's and 0's are distinguished by the transitions within the middle of the clock period. This method is used to embed clocking information to help synchronize the reader to the bitstream. Because it always has a transition at a clock edge, it inherently provides some error correction capability. Any clock edge that does not contain a transition in the data stream is in error and can be used to reconstruct the data.

3. **Biphase_L (Manchester).** This is a variation of biphase encoding in which there is not always a transition at the clock edge. **The MCRF355/360 and MCRF45X devices use this encoding method.**

FIGURE 2: VARIOUS DATA CODING WAVEFORMS



Note: Manchester coding is used for the MCRF355/360 and MCRF45X

DATA MODULATION FOR 125 kHZ DEVICES (MCRF2XX)

Although all the data is transferred to the host by amplitude-modulating the carrier (backscatter modulation), the actual modulation of 1's and 0's is accomplished with three additional modulation methods:

1. Direct. In direct modulation, the Amplitude Modulation of the backscatter approach is the only modulation used. A high in the envelope is a '1' and a low is a '0'. Direct modulation can provide a high data rate but low noise immunity.
2. **FSK (Frequency Shift Keying).** This form of modulation uses two different frequencies for data transfer; the most common FSK mode is FC/8/10. In other words, a '0' is transmitted as an amplitude-modulated clock cycle with period corresponding to the carrier frequency divided by 8, and a '1' is transmitted as an amplitude-modulated clock cycle period corresponding to the carrier frequency divided by 10. The amplitude modulation of the carrier thus switches from FC/8 to FC/10 corresponding to 0's and 1's in the bitstream, and the reader has only to count cycles between the peak-detected clock edges to decode the data. FSK allows for a simple reader design, provides very strong noise immunity, but suffers from a lower data rate than some other forms of data modulation. In Figure 3, FSK data modulation is used with NRZ encoding.
3. **PSK (Phase Shift Keying).** This method of data modulation is similar to FSK, except only one frequency is used, and the shift between 1's and 0's is accomplished by shifting the phase of the backscatter clock by 180 degrees. Two common types of PSK are:
   - Change phase at any '0', or
   - Change phase at any data change (0 to 1 or 1 to 0).

   PSK provides fairly good noise immunity, a moderately simple reader design, and a faster data rate than FSK. Typical applications utilize a backscatter clock of FC/2, as shown in Figure 4.

FIGURE 3: FSK MODULATED SIGNAL, FC/8 = 0, FC/10 = 1

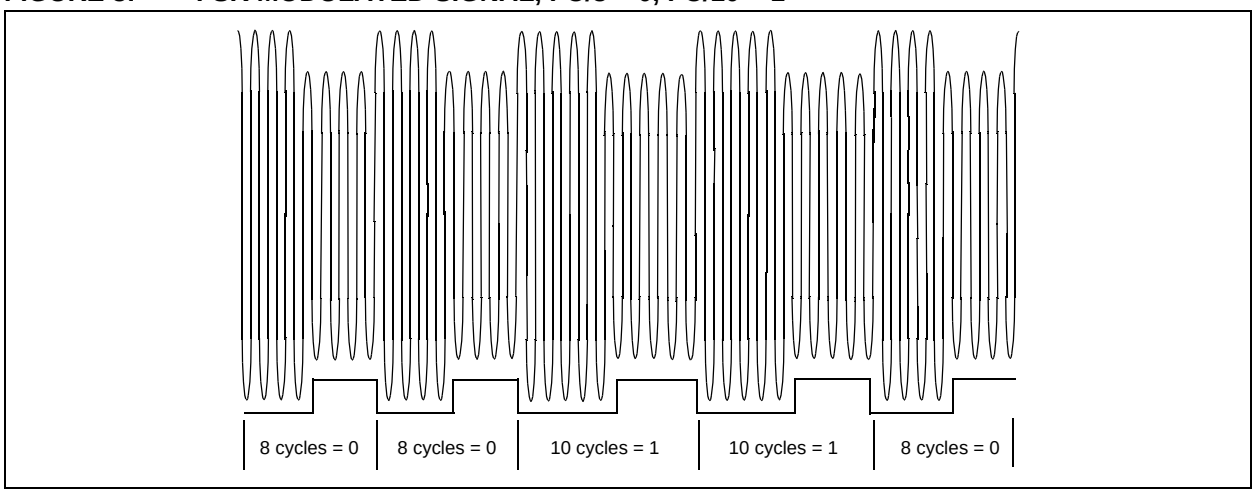
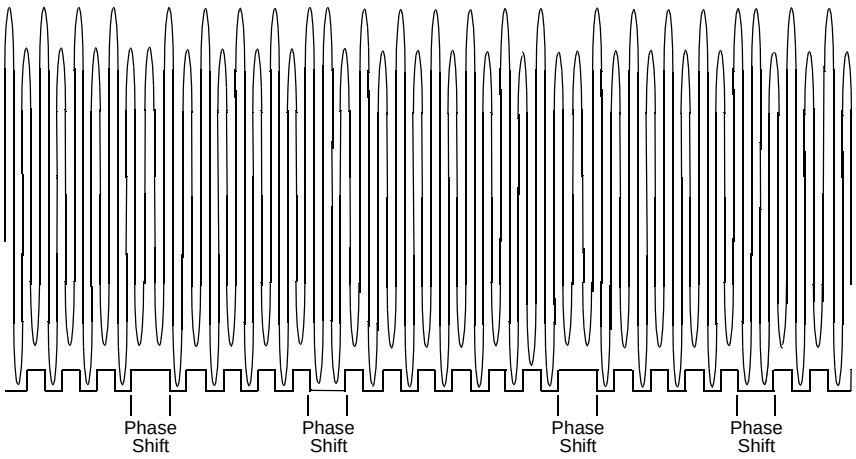


FIGURE 4: PSK MODULATED SIGNAL



ANTI-COLLISION

In many existing applications, a single-read RFID tag is sufficient and even necessary: animal tagging and access control are examples. However, in a growing number of new applications, the simultaneous reading of several tags in the same RF field is absolutely critical: library books, airline baggage, garment and retail applications are a few.

In order to read multiple tags simultaneously, the tag and reader must be designed to detect the condition that more than one tag is active. Otherwise, the tags will all backscatter the carrier at the same time and the amplitude-modulated waveforms shown in Figure 3 and Figure 4 would be garbled. This is referred to as a *collision*. No data would be transferred to the reader. The tag/reader interface is similar to a serial bus, even though the “bus” travels through the air. In a wired serial bus application, arbitration is necessary to prevent bus contention. The RFID interface also requires arbitration so that only one tag transmits data over the “bus” at one time.

A number of different methods are in use and in development today for preventing collisions; most are patented or patent pending. Yet, all are related to making sure that only one tag “talks” (backscatters) at any one time. See the *MCRF250* (DS21267), *MCRF355/360* (DS21287) and *MCRF45X* (DS40232) data sheets for various anti-collision algorithms.

NOTES:

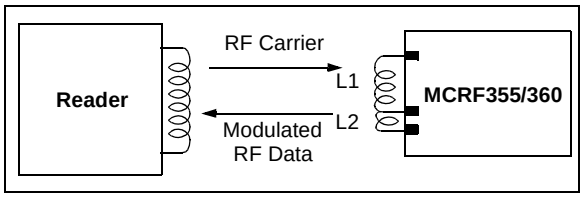
MCRF355/360

MCRF355/360 Data Sheet

FEATURES

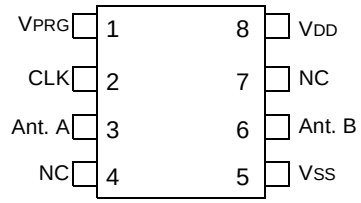
- Carrier frequency: 13.56 MHz
- Data modulation frequency: 70 kHz
- Manchester coding protocol
- 154 bits of user-reprogrammable memory
- On-board 100 ms sleep timer
- Built-in anti-collision algorithm for reading up to 50 tags in the same RF field
- “Cloaking” feature minimizes the detuning effects of adjacent tags
- Internal 100 pF resonant capacitor (MCRF360)
- Read-only device in RF field
- Rewritable with contact programmer or factory-programmed options
- Very low power CMOS design
- Die, wafer, PDIP or SOIC package options

APPLICATION



PACKAGE TYPE

PDIP/SOIC



DESCRIPTION

The MCRF355 and MCRF360 are Microchip’s 13.56 MHz microID™ family of RFID tagging devices. They are uniquely designed read-only passive Radio Frequency Identification (RFID) devices with an advanced anti-collision feature. The device is powered remotely by rectifying RF magnetic fields that are transmitted from the reader.

The device has a total of six pads (see Figure 1-1). Three (ant. A, B, VSS) are used to connect the external resonant circuit elements. The additional three pads (VPRG, CLK, VDD) are used for programming and testing of the device.

The device needs an external resonant circuit between antenna A, B, and VSS pads. The resonant frequency of the circuit is determined by the circuit elements between the antenna A and VSS pads. The resonant circuit must be tuned to the carrier frequency of the reader for maximum performance. The circuit element between the antenna B and VSS pads is used for data modulation. See Application Note AN707 (DS00707) for further operational details.

The MCRF360 includes a 100 pF internal resonant capacitor (100 pF). By utilizing this internal resonant capacitor, the device needs external coils only for the resonant circuit. Examples of the resonant circuit configuration for both the MCRF355 and MCRF360 are shown in Section 3.

When a tag (device with the external LC resonant circuit) is brought to the reader’s RF field, it induces an RF voltage across the LC resonant circuit. The device rectifies the RF voltage and develops a DC voltage. The device becomes functional as soon as VDD reaches the operating voltage level.

The device includes a modulation transistor that is located between antenna B and VSS pads. The transistor has high turn-off (a few MΩ) and low turn-on (3 Ω) resistance. The turn-on resistance is called modulation resistance (RM). When the transistor turns off, the resonant circuit is tuned to the carrier frequency of the reader. This condition is called uncloaking. When the modulation transistor turns on, its low turn-on resistance shorts the external circuit element between the antenna B and VSS. As a result, the resonant circuit no longer resonates at the carrier frequency. This is called cloaking.

The induced voltage amplitude (on the resonant circuit) changes with the modulation data: higher amplitude during uncloaking (tuned), and lower amplitude during cloaking (detuned). This is called “amplitude modulation” signal. The receiver channel in the reader detects this amplitude modulation signal and reconstructs the modulation data.

The occurrence of the cloaking and uncloaking of the device is controlled by the modulation signal that turns the modulation transistor on and off, resulting in communication from the device to the reader.

The data stream consists of 154 bits of Manchester-encoded data at a 70 KHz rate. The Manchester code waveform is shown in Figure 2-2. After completion of the data transmission, the device goes into sleep mode for about 100 ms. The device repeats the transmitting and sleep cycles as long as it is energized. During the sleep time the device remains in an uncloaked state.

Sleep time is determined by a built-in low-current timer. There is a wide variation of the sleep time between each device. This wide variation of sleep time results in a randomness of the time slot. Each device wakes up and transmits its data in a different time slot with respect to each other. Based on this scenario, the reader is able to read many tags that are in the same RF field.

The device has a total of 154 bits of reprogrammable memory. All bits are reprogrammable by a contact programmer. A contact programmer (part number PG103003) is available from Microchip Technology Inc. Factory programming prior to shipment, known as Serialized Quick Turn Programming^{SM} (SQTP^{SM}), is also available. The device is available in die form or packaged in SOIC or PDIP.

Note:	Information provided herein is preliminary and subject to change without notice.

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1-1: ABSOLUTE MAXIMUM/MINIMUM RATINGS

Parameters	Symbol	Min.	Max.	Units	Conditions
Coil Current	I_{PP_AC}	—	40	mA	Peak-to-Peak coil current
Assembly temperature	T_{ASM}	—	300	°C	< 10 sec
Storage temperature	T_{STORE}	-65	150	°C	—

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	**Commercial (C): T_{AMB} = -20°C to 70°C**					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Reading voltage	V_{DDR}	2.4	—	—	V	V_{DD} voltage for reading
Hysteresis voltage	V_{HYST}	—	TBD	—	TBD	—
Operating current	I_{DDR}	—	7	10	µA	V_{DD} = 2.4V during reading at 25°C
Testing voltage	V_{DDT}	—	4	—	V	—
Programming voltage: High level input voltage Low level input voltage High voltage	 V_{IH} V_{IL} V_{HH}	 0.7 * V_{DDT} — —	 — — 20	 — 0.3 * V_{DDT} —	 V V V	External DC voltage for programming and testing
Current leakage during sleep time	I_{DD_OFF}	—	10	—	nA	**(Note 1)**
Modulation resistance	R_M	—	3	4	Ω	DC resistance between Drain and Source gates of the modulation transistor (when it is turned on)
Pull-Down resistor	R_{PDW}	5	8	—	KΩ	CLK and V_{PRG} internal pull-down resistor

Note 1: This parameter is not tested in production.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	**Commercial (C): T_{AMB} = -20°C to 70°C**					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Carrier frequency	F_C		13.56		MHz	Reader's transmitting frequency
Modulation frequency	F_M	58	70	82	kHz	Manchester coding
Coil voltage during reading	V_{PP_AC}	4	—	—	V_{PP}	Peak-to-Peak AC voltage across the coil during reading
Coil clamp voltage	V_{CLMP_AC}	—	32	—	V_{PP}	Peak -to-Peak coil clamp voltage
Test mode clock frequency	F_{CLK}		115	500	kHz	25°C
Sleep time	T_{OFF}	50	100	150	ms	Off time for anti-collision feature, at 25°C
Internal resonant capacitor (MCRF360)	C_{RES}	85	100	115	pF	Internal resonant capacitor between Antenna A and V_{SS}, at 13.56 MHz
Resonant frequency (MCRF360)	F_R	12.65	13.56	14.711	MHz	with L = 1.377 µH
Write/Erase pulse width	T_{WC}	—	2	10	ms	Time to program bit, at 25°C
Clock high time	T_{HIGH}	—	4.4	—	µs	25°C
Clock low time	T_{LOW}	—	4.4	—	µs	25°C
Stop condition pulse width	$T_{PW:STO}$	—	1000	—	ns	25°C
Stop condition setup time	$T_{SU:STO}$	—	200	—	ns	25°C
Setup time for high voltage	$T_{SU:HH}$	—	800	—	ns	25°C
High voltage delay time	$T_{DL:HH}$	—	800	—	ns	Delay time before the next clock, at 25°C
Data input setup time	$T_{SU:DAT}$	—	450	—	ns	25°C
Data input hold time	$T_{HD:DAT}$	—	1.2	—	µs	25°C
Output valid from clock	T_{AA}	—	200	—	ns	25°C
Data retention	—	200		—	Years	For T < 120°C

TABLE 1-4: PAD COORDINATES (MICRONS)

Pad Name	Lower Left X	Lower Left Y	Upper Right X	Upper Right Y	Passivation Openings		Pad Center X	Pad Center Y
					Pad Width	Pad Height		
Ant. A	-610.0	489.2	-521.0	578.2	89	89	-565.5	533.7
Ant. B	-605.0	-579.8	-516.0	-490.8	89	89	-560.5	-535.3
VSS	-605.0	-58.2	-516.0	30.8	89	89	-560.5	-13.7
VDD	463.4	-181.4	552.4	-92.4	89	89	507.9	-136.9
CLK	463.4	496.8	552.4	585.8	89	89	507.9	541.3
VPRG	463.4	157.6	552.4	246.6	89	89	507.9	202.1

Note 1: All coordinates are referenced from the center of the die. The minimum distance between pads (edge to edge) is 10 mil.

2: Die Size = 1.417 mm x 1.513 mm = 1417 µm x 1513 µm = 55.79 mil x 59.57 mil

FIGURE 1-1: MCRF355/360 DIE LAYOUT

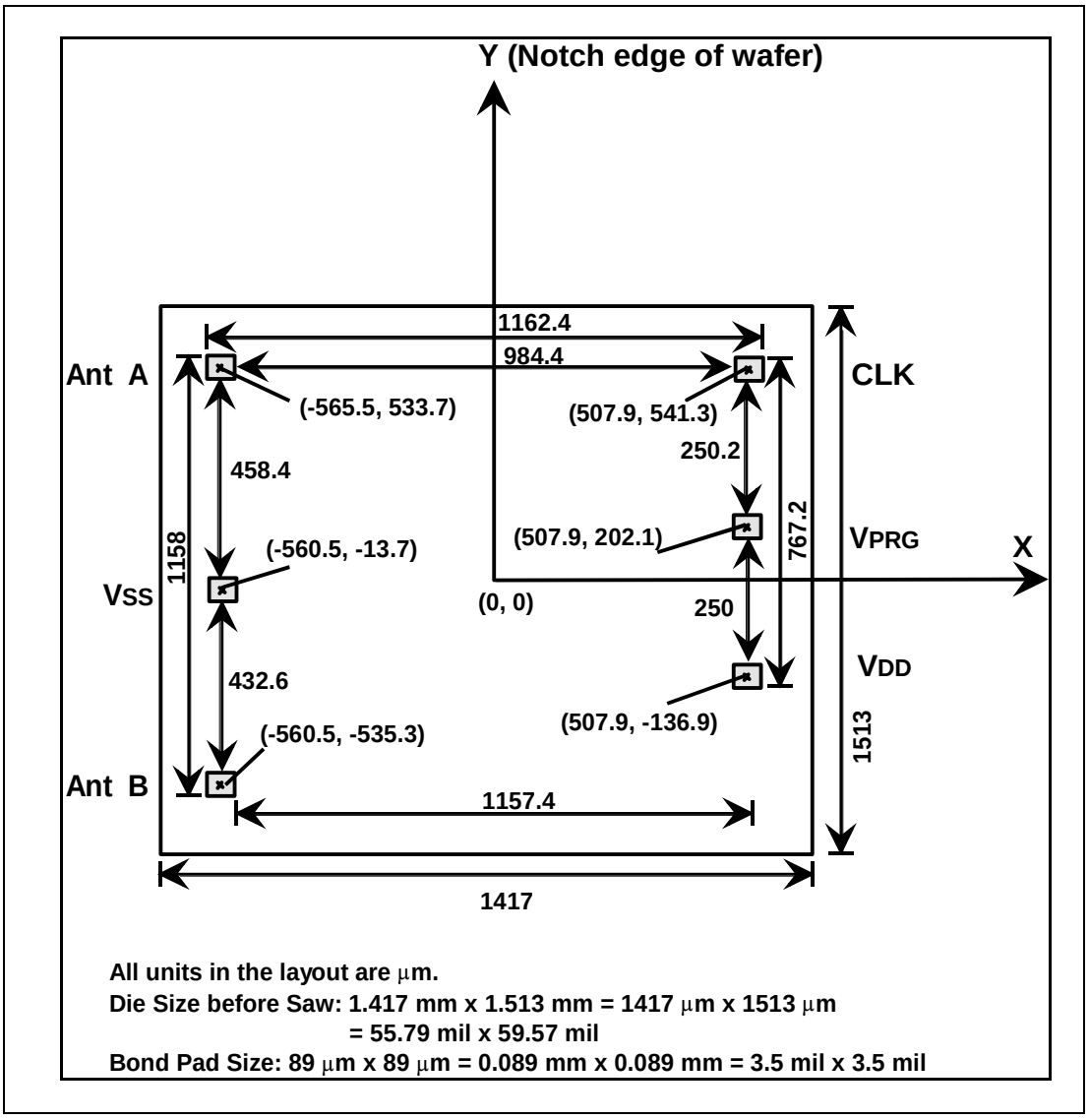


TABLE 1-5: DIE MECHANICAL DIMENSIONS

Specifications	Min.	Typ.	Max.	Unit	Comments
Bond pad opening	— —	3.5 x 3.5 89 x 89	— —	mil µm	**(Note 1, Note 2)**
Die backgrind thickness	— —	8 177.8	— —	mil µm	Sawed 8” wafer on frame (option = WF) **(Note 3)**
	— —	11 279.4	— —	mil µm	• Bumped, sawed 8” wafer on frame (option = WFB) • Unsawed wafer (option = W) • Unsawed 8” bumped wafer (option = WB), **(Note 3)**
Die backgrind thickness tolerance	— —	— —	±1 ±25.4	mil µm	**(Note 4)**
Die passivation thickness (multilayer)	—	0.9050	—	µm	**(Note 5)**
Die Size: Die size X*Y before saw (step size) Die size X*Y after saw	 — —	 55.79 x 59.57 54.22 x 58	 — —	 mil mil	 — —

Note 1: The bond pad size is that of the passivation opening. The metal overlaps the bond pad passivation by at least 0.1 mil.
2: Metal Pad Composition is 98.5% Aluminum with 1% Si and 0.5% Cu.
3: As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow.
4: This specification is not tested. For design guidance only.
5: The Die Passivation thickness can vary by device depending on the mask set used.
6: The conversion rate is 25.4 µm/mil.

Notice: Extreme care is urged in the handling and assembly of die products since they are susceptible to mechanical and electrostatic damage.

TABLE 1-6: PAD FUNCTION TABLE

Name	Function
Ant. A	Connected to external resonant circuit, **(Note)**
Ant. B	Connected to external resonant circuit, **(Note)**
VSS	Connected to external resonant circuit. Device ground during test mode, **(Note)**
VDD	DC voltage supply for programming
CLK	Main clock pulse for device
VPRG	Input/Output for programming and read test

Note: See Figure 3-1 for the connection with external resonant circuit.

2.0 FUNCTIONAL DESCRIPTION

The device contains three major sections: (1) Analog Front-End, (2) Controller Logic and (3) Memory. Figure 2-1 shows the block diagram of the device.

2.1 Analog Front-End Section

This section includes power supply, power-on-reset, and data modulation circuits.

2.1.1 POWER SUPPLY

The power supply circuit generates DC voltage (V_{DD}) by rectifying induced RF coil voltage. The power supply circuit includes high-voltage clamping diodes to prevent excessive voltage development across the antenna coil.

2.1.2 POWER-ON-RESET (POR)

This circuit generates a power-on-reset when the tag first enters the reader field. The reset releases when sufficient power has developed on the V_{DD} regulator to allow for correct operation.

2.1.3 DATA MODULATION

The data modulation circuit consists of a modulation transistor and an external LC resonant circuit. The external circuit must be tuned to the carrier frequency of the reader (i.e., 13.56 MHz) for maximum performance.

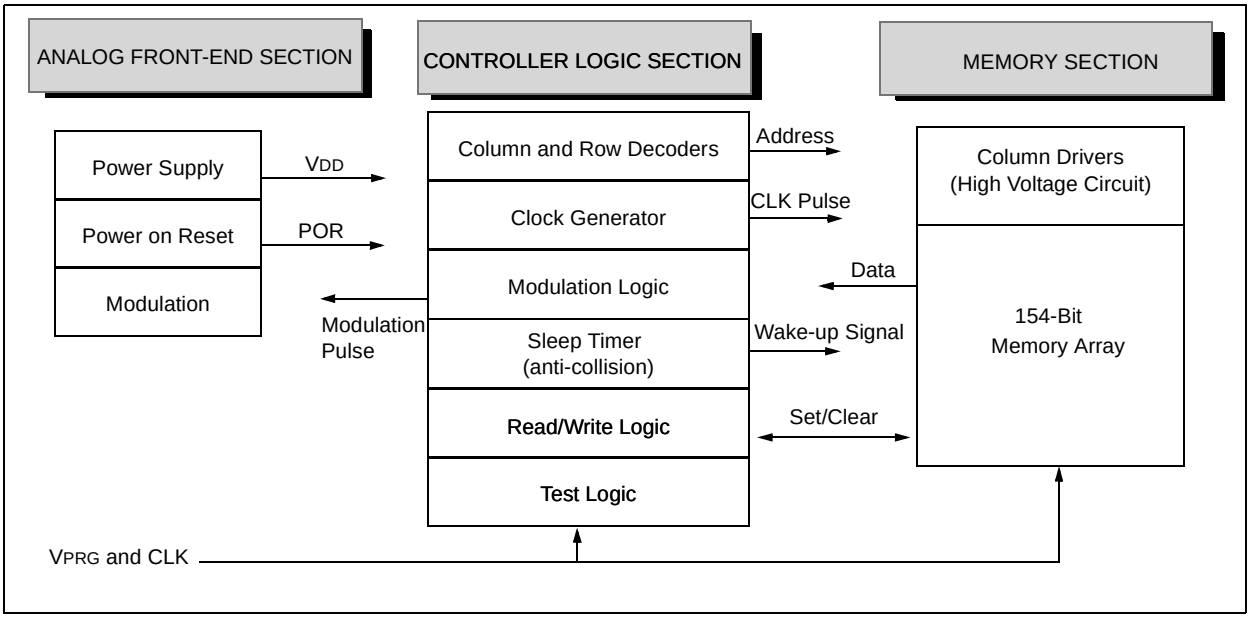
The modulation transistor is placed between antenna B and Vss pads and has small turn-on resistance (R_M). This small turn-on resistance shorts the external circuit between the antenna B and Vss pads as it turns on.

The transistor turns on during the “High” period of the modulation data and turns off during the “Low” period.

When the transistor is turned off, the resonant circuit resonates at the carrier frequency. Therefore, the external circuit develops maximum voltage across it. This condition is called uncloaking (tuned). When the transistor is turned on, its low turn-on resistance shorts the external circuit, and therefore the circuit no longer resonates at the carrier frequency. The voltage across the external circuit is minimized. This condition is called cloaking (detuned).

The device transmits data by cloaking and uncloaking based on the on/off condition of the modulation transistor. Therefore, with the 70 kHz - Manchester format, the data bit “0” will be sent by cloaking (detuned) and uncloaking (tuned) the device for 7 ms each. Similarly, the data bit “1” will be sent by uncloaking (tuned) and cloaking (tuned) the device for 7 ms each. See Figure 2-2 for the Manchester waveform.

FIGURE 2-1: BLOCK DIAGRAM



2.2 Controller Logic Section

2.2.1 CLOCK PULSE GENERATOR

This circuit generates a clock pulse (CLK). The clock pulse is generated by an on-board time-base oscillator. The clock pulse is used for baud rate timing, data modulation rate, etc.

2.2.2 MODULATION LOGIC

This logic acts upon the serial data (154 bits) being read from the memory array. The data is then encoded into Manchester format. The encoded data is then fed to the modulation transistor in the Analog Front-End section. The Manchester code waveform is shown in Figure 2-2.

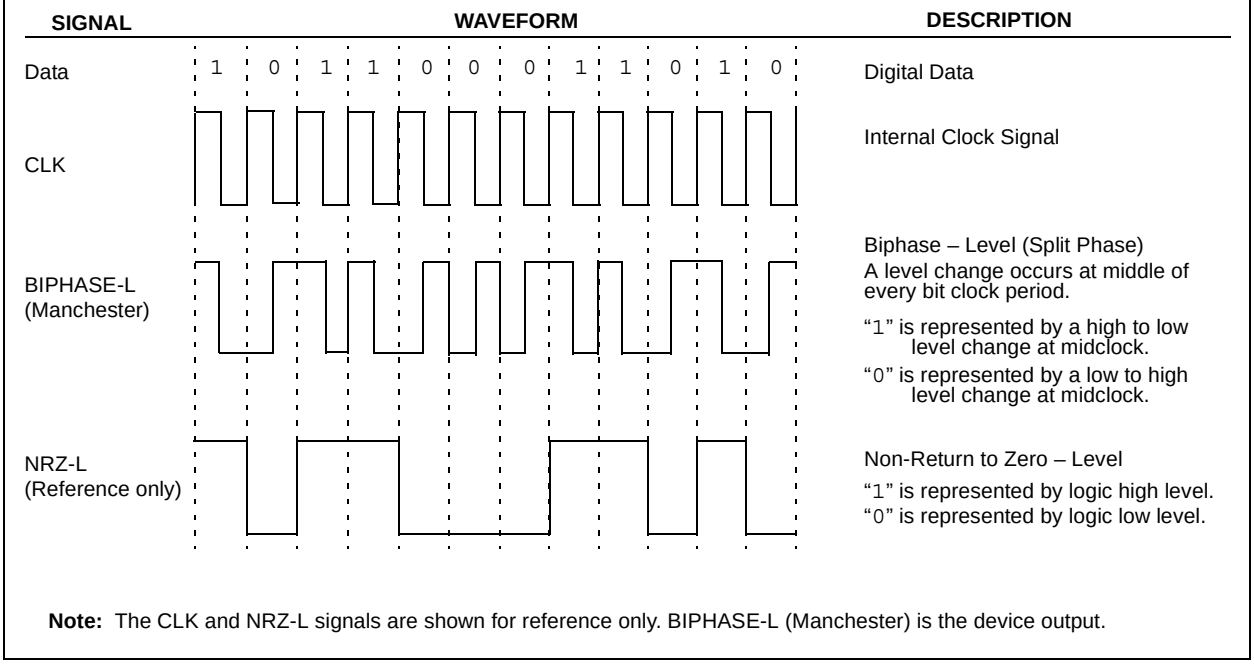
2.2.3 SLEEP TIMER

This circuit generates a sleep time (100 ms ± 50%) for the anti-collision feature. During this sleep time (TOFF), the modulation transistor remains in a turned-on condition (cloaked) which detunes the LC resonant circuit.

2.2.4 READ/WRITE LOGIC

This logic controls the reading and programming of the memory array.

FIGURE 2-2: CODE WAVEFORMS



Note: The CLK and NRZ-L signals are shown for reference only. BIPHASE-L (Manchester) is the device output.

3.0 RESONANT CIRCUIT

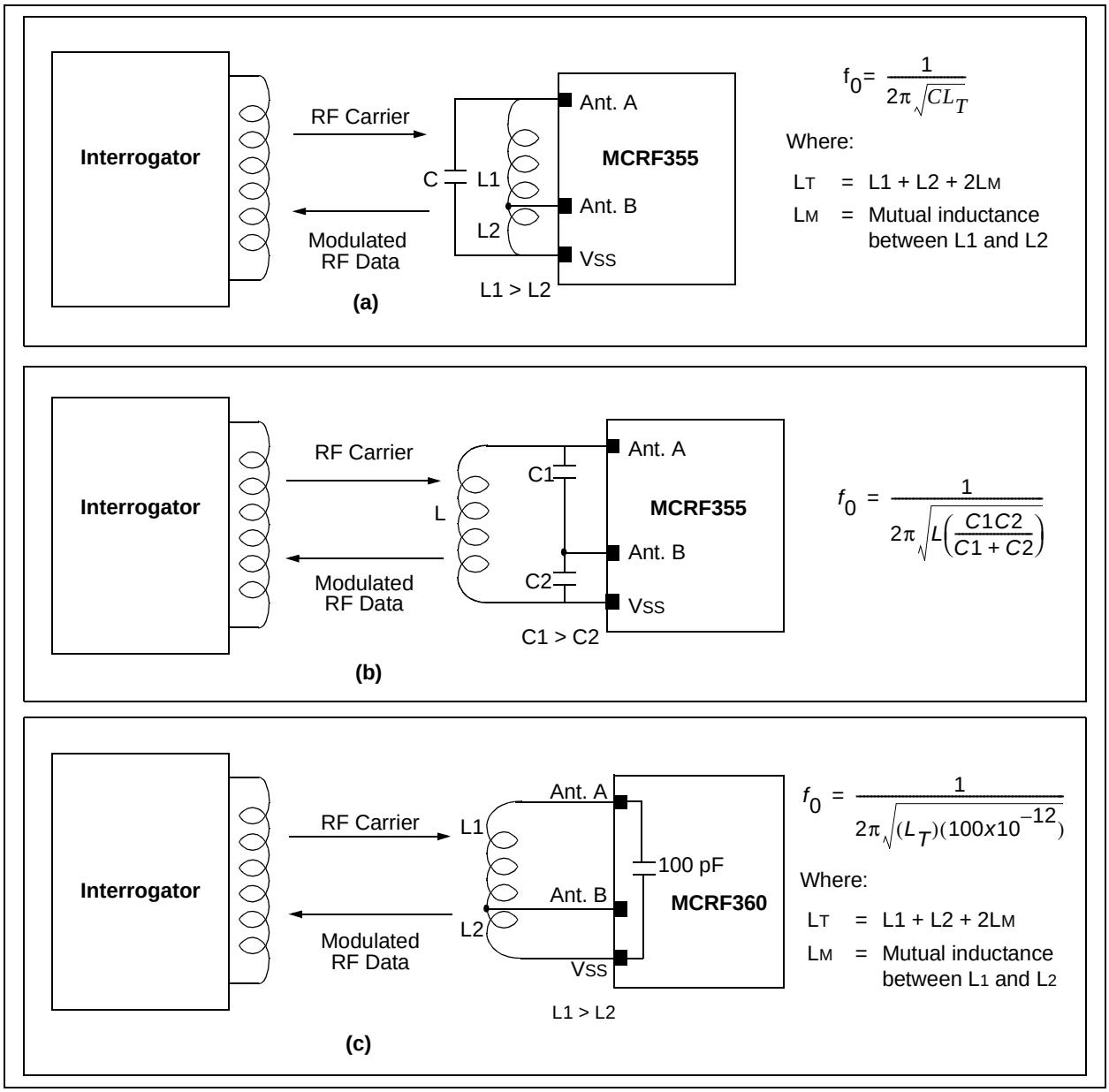
The MCRF355 requires external coils and capacitor in order to resonate at the carrier frequency of the reader. About one-fourth (¼) of the turns of the coil should be connected between antenna B and VSS; remaining turns should be connected between antenna A and B pads. The MCRF360 includes a 100 pF internal resonant capacitor. Therefore, the device needs only external coils for the resonant circuit. For example, the device needs 1.377 µH of inductance for the carrier frequency = 13.56 MHz.

Figures 3-1 (a) and (b) show possible configurations of the external circuits for the MCRF355. In Figure 3-1 (a), two external antenna coils (L1 and L2) in series and a capacitor that is connected across the two inductors form a parallel resonant circuit to pick up incoming RF signals and also to send modulated signals to the reader. The first coil (L1) is connected between antenna A and B pads. The second coil (L2) is connected between antenna B and VSS pads. The capacitor is connected between antenna A and VSS pads.

Figure 3-1(b) shows the resonant circuit formed by two capacitors (C1 and C2) and one inductor.

Figure 3-1(c) shows a configuration of an external circuit for the MCRF360. By utilizing the 100 pF internal resonant capacitor, only L1 and L2 are needed for the external circuit.

FIGURE 3-1: CONFIGURATION OF EXTERNAL RESONANT CIRCUITS



4.0 DEVICE PROGRAMMING

MCRF355/360 is a reprogrammable device in contact mode. The device has 154 bits of reprogrammable memory. It can be programmed in the following procedure. (A programmer, part number PG103003, is also available from Microchip.)

4.1 Programming Logic

Programming logic is enabled by applying power to the device and clocking the device via the CLK pad while loading the mode code via the VPRG pad (See Examples 4-1 through 4-4 for test definitions). Both the CLK and the VPRG pads have internal pull-down resistors.

4.2 Pin Configuration

Connect antenna A, B, and VSS pads to ground.

4.3 Pin Timing

1. Apply VDDT voltage to VDD. Leave VSS, CLK, and VPRG at ground.
2. Load mode code into the VPRG pad. The VPRG is sampled at CLK low to high edge.
3. The above mode function (3.2.2) will be executed when the last bit of code is entered.
4. Power the device off (VDD = VSS) to exit programming mode.
5. An alternative method to exit the programming mode is to bring CLK logic "High" before VPRG to VHH (high voltage).
6. Any programming mode can be entered after exiting the current function.

4.4 Programming Mode

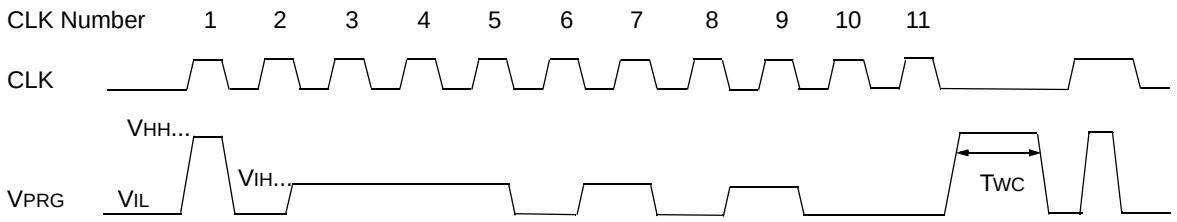
1. Erase EE Code: 0111010100
2. Program EE Code: 0111010010
3. Read EE Code: 0111010110

Note: '0' means logic "Low" (VIL) and '1' means logic "High" (VIH).

4.5 Signal Timing

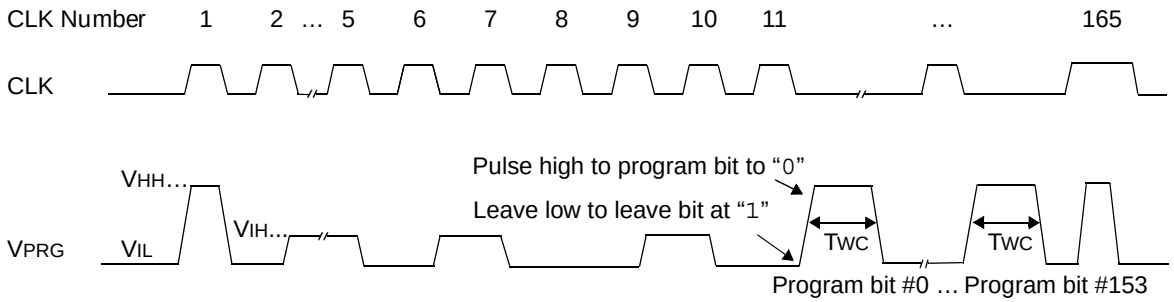
Examples 4-1 through 4-4 show the timing sequence for programming and reading of the device.

EXAMPLE 4-1: PROGRAMMING MODE 1: ERASE EE



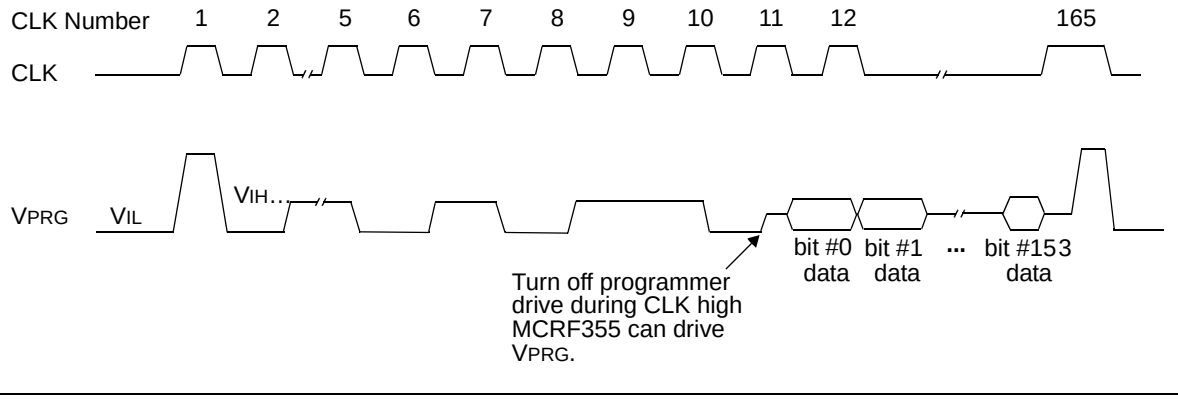
Note: Erases entire array to a '1' state between CLK and Number 11 and 12.

EXAMPLE 4-2: PROGRAMMING MODE 2: PROGRAM EE

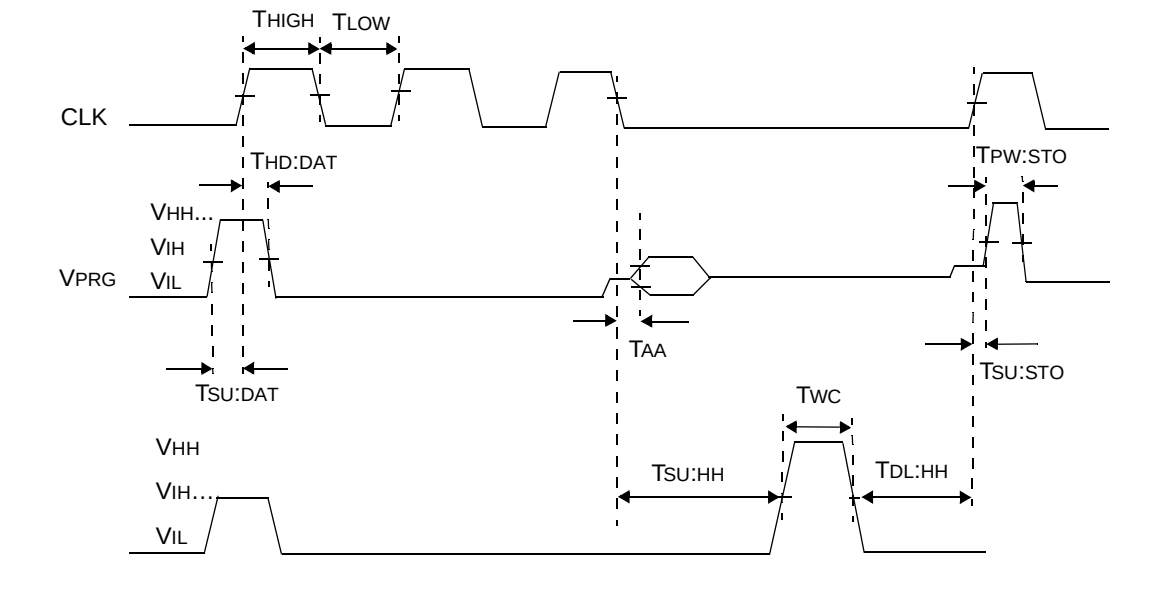


Note: Pulsing VPRG to VHH for the bit programming time while holding the CLK low programs the bit to a '0'.

EXAMPLE 4-3: PROGRAMMING MODE 3: READ EE



EXAMPLE 4-4: TIMING DATA



MCRF355/360 GUIDE PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, (e.g., on pricing or delivery), please refer to the factory or the listed sales office.

MCRF355 – /WF

Package:		WF	= Sawed wafer on frame (8 mil backgrind)
		WFB	= Bumped, sawed wafer on frame (8 mil backgrind)
		W	= Wafer (11 mil backgrind)
		WB	= Bumped wafer (11 mil backgrind)
		S	= Dice in waffle pack
		SB	= Bumped die in waffle pack
		SN	= 150 mil SOIC
		P	= PDIP
Temperature Range:			= -20°C to +70°C
Part Number:	MCRF355		= 13.56 MHz Anti-Collision device
	MCRF360		= 13.56 MHz Anti-Collision device with 100 pF of on-chip resonance capacitance

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

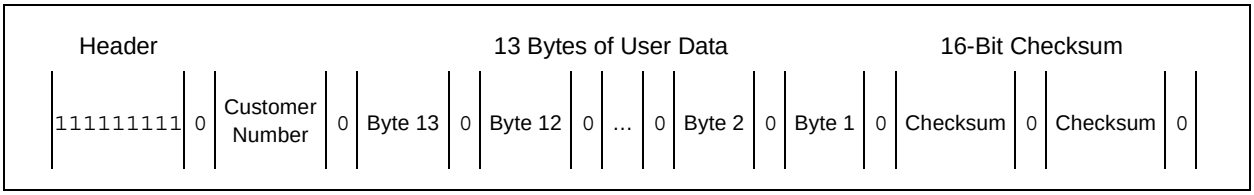
1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

Microchip Development Kit Sample Format for the MCRF355/360 Devices



9	bit header
8	bit customer number
104	bits (13 x 8) of user data
17	bits of zeros between each byte, header, and checksum
16	bits of checksum
Total:	154 bits

Notes:

- Users can program all 154 bits of the MCRF355/360. The array can be programmed in any custom format and with any combination of bits.
- The format presented here is used for Microchip microID™ Development System (DV103003) and can be ordered as production material with a unique customer number.
- See TB032 for information on ordering custom programmed production material.
- The Microchip Development System (DV103003) uses nine 1's (111111111) as header.
- The preprogrammed tag samples in the development kit have hex 11(= 0001 0001) as the customer number.
- For the development system, users can program the customer number (1 byte) plus the 13 bytes of user data, or they can deselect the "Microchip Format" option in the MicroID™ RFLAB and program all 154 bits in any format.
- When users program the samples using the MicroID™ RFLAB, the RFLAB calculates the checksum (2 bytes) automatically by adding up all 14 bytes (customer number + 13 bytes of user data), and put into the checksum field in the device memory. See Example 1 for details.
- When the programmed tag is energized by the reader field, the tag outputs all 154 bits of data.
- When the demo reader detects data from the tag, it reports the 14 bytes of the data (customer number plus 13 bytes of user data) to the host computer if the header and checksum are correct. The reader does not send the header and checksum to the host computer.
- The "MicroID™ RFLab" or a simple terminal program such as "terminal.exe" can be used to read the reader's output (28 hex digits) on the host computer.
- When the demo reader is used in the terminal mode (terminal.exe), the tag's data appear after the first two dummy ASCII characters (GG). See Example 2 for details.

EXAMPLE-2: CHECKSUM

Checksum (XXXXXXXX XXXXXXXX) = Byte 1 + Byte 2 + ...+ Byte 13 + Customer Number (1 byte)

EXAMPLE-3: READER'S OUTPUT IN TERMINAL MODE ("TERMINAL.EXE")

The demo reader outputs GG+28 hex digits, i.e., GG 12345678901234567890ABCDEFGF.

The first two ASCII characters (GG) are dummy characters.

The tag's data are the next 28 hex digits (112 bits) after the first two ASCII characters (GG).

NOTES:

Factory Programming Support (SQTP^{SM})

INTRODUCTION

The MCRF355 and MCRF360 are 13.56 MHz RF tags which can be contact programmed. The contact programming of the device can be performed by the user or factory-programmed by Microchip Technology, Inc. upon customer request. All 154 bits of data may be programmed in any format or pattern defined by the customer.

For factory programming, ID codes and series numbers must be supplied by the customer or an algorithm may be specified by the customer. This technical brief describes only the case in which identification codes (ID) and series numbers are supplied. The customer may supply the ID codes and series numbers on floppy disk or via email. The codes must conform to the Serialized Quick Turn Programming^{SM} (SQTP^{SM}) format below:

FILE SPECIFICATION

SQTP codes supplied to Microchip must comply with the following format:

The ID code file is a plain ASCII text file from floppy disk or email (no headers).

If code files are compressed, they should be self-extracting files.

The code files are used in alphabetical order of their file names (including letters and numbers).

Used (i.e., programmed) code files are discarded by Microchip after use.

Each line of the code file must contain one ID code for one IC.

The code is in hexadecimal format.

The code line is exactly 154 bits (39 hex characters, where the last 2 bits of the last character are don't cares).

Each line must end with a carriage return.

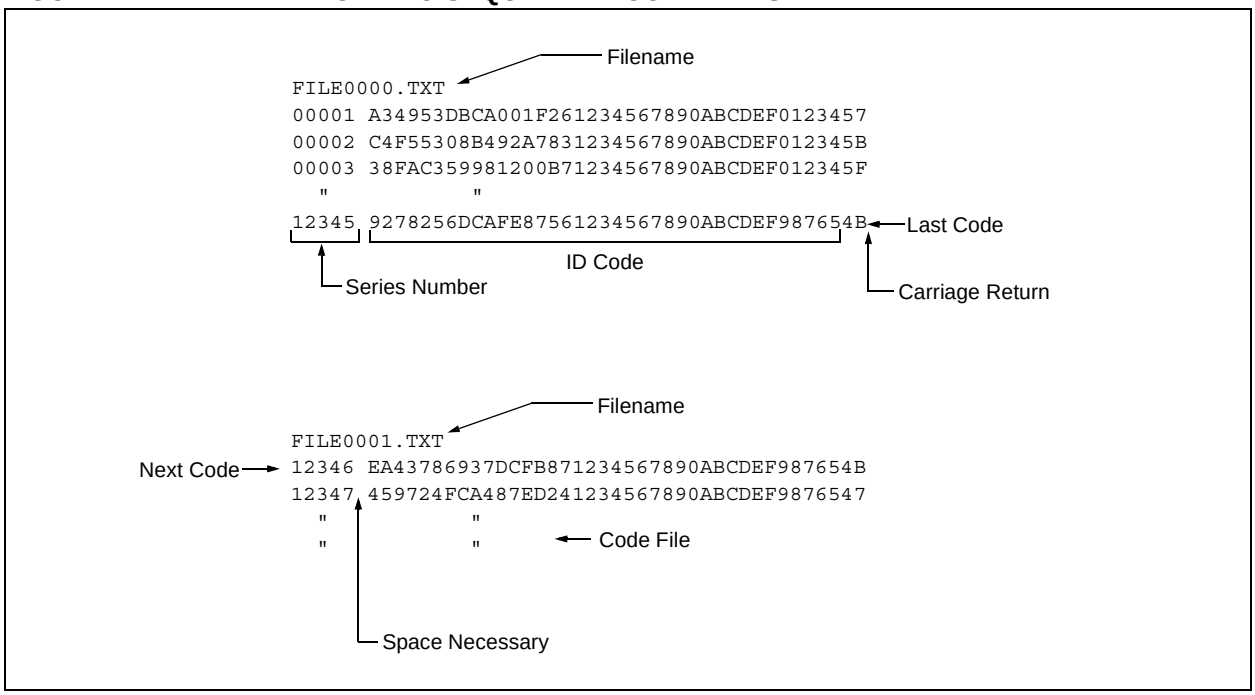
Each hexadecimal ID code must be preceded by a decimal series number.

Series number and ID code must be separated by a space.

The series number must be unique and ascending to avoid double programming.

The series numbers of two consecutive files must also count up for proper linking.

FIGURE 1: EXAMPLE OF TWO SEQUENTIAL CODE FILES



NOTES:

MCRF450/451/452/455

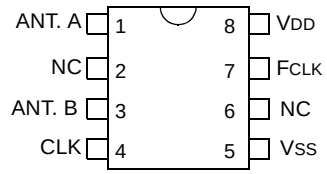
MCRF450/451/452/455 Data Sheet

FEATURES

- Contactless read and write
- 1024 bits (32 blocks) of total memory
- 928 bits of user programmable memory
- User controlled write-protection of each block
- Manchester coding protocol with CRC for reading
- 70 kHz data rate
- RF field gaps and 1-of-16 PPM with CRC for writing
- High speed deterministic anti-collision algorithm for reading and writing virtually any number of tags in the same RF field
- Three pads for external antenna circuit (MCRF450, 451, 455)
- Two pads for external antenna (MCRF452)
- Internal resonance capacitors (MCRF451, 452, 455)
- Factory programmed unique 32-bit tag ID
- Interrogator talks first (ITF) or tag talks first (TTF) operation
- Fast and normal modes for data transmission
- Anti-tearing feature for secure write transactions
- Full 32-bit EAS support
- Very low power CMOS design
- Die, wafer, bumped wafer, PDIP or SOIC package options
- Asynchronous operation for low power/extended read range

PACKAGE TYPES

PDIP/SOIC

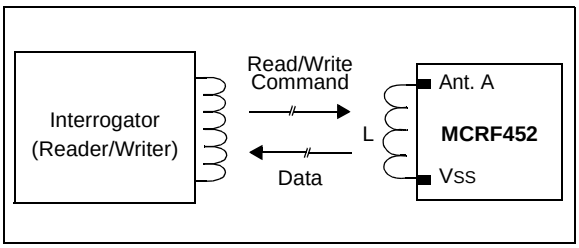


DESCRIPTION

The MCRF45X is a contactless read/write passive RFID device that is optimized for 13.56 MHz RF carrier signal. The device needs an external LC resonant circuit to communicate with interrogator wirelessly. The device is powered remotely by rectifying an RF signal that is transmitted from the interrogator, and transmits or updates its contents of memory based on commands from the interrogator.

The device is engineered to be used effectively for item level tagging applications such as retail and inventory management, where a large volume of tags are read and written in the same interrogator field.

APPLICATION



The device contains 32 blocks of EEPROM memory. Each block consists of 32 bits. The first three blocks (B0 - B2: 96 bits) are allocated for device operation, the remaining 29 blocks (B3 - B29: 928 bits) are for user data. The 928 (B3 - B31) user bits are contactlessly writable block-wise by interrogator commands. All blocks except bits 30 and 31 in block 0 are write-protectable.

The device has two operational modes depending on the conditions of talk first (TF) and fast read (FR) bits. These modes are: “tag talks first” (TTF) and “interrogator talks first” (ITF) modes. The device operates in TTF mode if both TF and FR bits are set. In this mode, the device transmits its fast read response data (96 bits in default) as soon as it is energized, and waits for the next commands. The device operates in the “interrogator talks first” mode, if the TF bit is cleared. In this mode, the device requires an interrogator command before it sends any data.

The device uses an internal oscillator for data timing of the read operation. The data rate for reading is 70 kHz and uses Manchester format. The communication between the interrogator and the device takes place asynchronously.

The interrogator sends commands to the device by amplitude modulating its RF carrier signal. 1-of-16 Pulse Position Modulation (PPM) and specially timed gap pulses are used for the modulation of the carrier signal. The device includes a detection circuit to detect these interrogator commands.

To enhance the detection accuracy in the device, the interrogator sends a time reference signal (time calibration pulse) to the device followed by the command and programming data. The time reference signal is used to calibrate timing of the internal decoder of the device.

Depending on the metal mask options, the device includes internal resonant capacitor between antenna A and VSS pads: (a) no internal resonant capacitor for the MCRF450, (b) 100 pF for the MCRF451, (c) two 50 pF in series (25 pF in total) for the MCRF452 and (d) 50 pF for the MCRF455. The internal resonant capacitor for each metal mask option is shown in Figures 1-2 through 1-5.

The MCRF450 needs an external LC resonant circuit that is connected between antenna A, antenna B, and VSS pads. See Figure 1-2 for the external circuit configuration. The MCRF452 needs a single external antenna coil only between antenna A and VSS pads as shown in Figure 1-4.

This external circuit along with the internal resonant capacitor must be tuned to the carrier frequency of the interrogator for maximum performance.

When a tag (device with the external LC resonant circuit) is brought to the interrogator’s RF field, it develops an RF voltage across the external circuit. The device rectifies the RF voltage and develops a DC voltage (VDD). The device becomes functional as soon as VDD reaches the operating voltage level.

The device sends data to the interrogator by turning on/off the internal modulation transistor. This internal modulation transistor is located between antenna B and VSS. The modulation transistor has very small turn-on resistance between Drain (antenna B) and Source (VSS) terminals during its turn-on time.

When the modulation transistor turns-on, the resonant circuit component between antenna B and VSS, that is in parallel with the modulation transistor, is shorted due to the low turn-on resistance. This results in a change of the LC value of the circuit. As a result, the circuit no longer resonates at the carrier frequency of the interrogator. Therefore, the voltage across the circuit is minimized. This condition is called cloaking.

When the modulation transistor turns-off, the circuit resonates at the carrier frequency of the interrogator, and develops maximum voltage. This condition is called uncloaking. Therefore, the data is sent to the interrogator by turning-on (cloaking) and off (uncloaking) the modulation transistor.

Therefore, the voltage amplitude of the carrier signal across the LC resonant circuit changes depending on the amplitude of modulation data (cloaking for logic “High” level and uncloaking for logic “Low” level). This is called amplitude modulation signal. The receiver channel in the Interrogator detects this amplitude modulation signal and reconstructs the modulation data for decoding.

The device includes a unique anti-collision algorithm to be read or written effectively in multiple tag environments. To minimize data collision, the algorithm utilizes time division multiplexing of the device response. Therefore, each device can communicate with the interrogator in a different time slot. The devices in the interrogator’s RF field remain in a non-modulating condition if they are not in the given time slot. This enables the interrogator to communicate with the multiple devices one at a time without data collision. The details of the algorithm are described in Section 4.0.

To enhance data integrity for writing, the device includes an anti-tearing feature. This anti-tearing feature provides verification of data integrity for incomplete write cycles due to failed communication from the interrogator to the device during the write sequences.

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1-1: ABSOLUTE RATINGS

Parameters	Symbol	Min.	Max.	Units	Conditions
Coil current into coil pad	I_{PP_AC}	—	40	mA	Peak-to-Peak coil current
Maximum power dissipation	P_{MPD}	—	0.5	W	—
Ambient temperature with power applied	T_{AMB}	-40	125	°C	—
Assembly temperature	T_{ASM}	—	300	°C	< 10 Sec
Storage temperature	T_{STORE}	-65	150	°C	—

Note: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	**Commercial (C): T_{AMB} = -20°C to 70°C**					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Reading voltage	V_{DDR}	2.8	—	—	V	V_{DD} voltage for reading at 25°C
Operating current in normal mode	I_{OPER_N}	—	20	—	µA	V_{DD} = 2.8V during reading at 25°C
Operating current in fast mode	I_{OPER_F}	—	45	—	µA	V_{DD} = 2.8V during reading at 25°C
Writing current	I_{WRITE}	—	130	—	µA	At 25°C, V_{DD} = 2.8V
Writing voltage	V_{WRITE}	2.8	—	—	V_{DC}	At 25 °C
Modulation resistance	R_M	—	3	5	Ω	DC turn-on resistance between Drain and Source terminals of the modulation transistor at V_{DD} = 2.8V

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	**Commercial (C): T_{AMB} = -20°C to 70°C**					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Carrier frequency	F_C	2	13.56	35	MHz	**(Note 1)**
Coil voltage during reading	V_{PP_AC}	4	—	—	V_{PP}	Peak-to-Peak AC voltage across the coil during reading **(Note 1)**
Internal Resonant Capacitor	C_{RES_100}	85	100	115	pF	Between Ant. A and V_{SS} pads at 13.56 MHz and at 25°C, MCRF451
Internal Resonant Capacitor	$C_{RES\_2\_50A}$	42.5	50	57.5	pF	Between Ant. A and B pads at 13.56 MHz and at 25°C, MCRF452
Internal Resonant Capacitor	$C_{RES\_2\_50B}$	42.5	50	57.5	pF	Between Ant. B and V_{SS} pads at 13.56 MHz and at 25°C, MCRF452
Internal Resonant Capacitor	C_{RES_50}	42.5	50	57.5	pF	Between Ant. A and V_{SS} pads at 13.56 MHz and at 25°C, MCRF455
Coil detuning voltage	V_{DETUNE}	—	TBD	—	V_{PP}	Coil voltage at which the limiting circuit becomes active
Interrogator data (ITD) rate_normal	F_{ITD_NORM}	—	1.4286	—	kHz	—
Interrogator data (ITD) rate_fast	F_{ITD_FAST}	—	25	—	kHz	—
Device data rate	F_{DVD}	58	70	82	kHz	Both normal and fast modes
Modulation depth of 1-of-16 PPM	M_{DEPTH_PPM}	—	—	100	%	—
Pulse width of 1-of-16 PPM for normal mode	PW_{PPM_N}	—	175	—	µs	See Figure 4-2 and Table 4-7 for details.
Pulse width of 1-of-16 PPM for fast mode	PW_{PPM_F}	—	10	—	µs	See Figure 4-2 and Table 4-7 for details.
Symbol width of 1-of-16 PPM for normal mode	SW_{PPM_N}	—	2.8	—	ms	—
Symbol width of 1-of-16 PPM for fast mode	SW_{PPM_F}	—	160	—	µs	—
Gap pulse width of Fast Read command	GPW_FR	—	175	—	µs	See Figure 4-3 and Table 4-7 for details.
EEPROM (Memory) Writing Time	T_{WRITE}	—	5	—	ms	Write time for a 32-bit block.
Command Decode Time	T_{DECODE}	—	TBD	—	µs	Time delay between end of command symbol and start of the device response.
Time slot	T_{SLOT}		2.5	2.925	ms	—
Listening Window	T_{LW}	TBD	1	TBD	ms	—
Modulation depth of Fast Read command	M_{DEPTH_FRR}	—	—	100	%	—
Command Duration of Fast Read command (FRR and FRB)	T_CMD_FRR	—	1.575	—	ms	175 µs/pulse position x 9 pulse positions = 1.575 ms

Note 1: Not tested in production.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	**Commercial (C): T_{AMB} = -20°C to 70°C**					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input impedance A	Zin_A	—	TBD	—	Ω	Input impedance between antenna pad A and VSS, at 13.56 MHz with modulation transistor off (no external coils)
Input impedance B	Zin_B	—	TBD	—	Ω	Input impedance between antenna pad B and VSS, at 13.56 MHz with modulation transistor off (no external coils)
Data retention	—	200	—	—	Years	For T < 120°C
Endurance	—	1	—	—	Million Cycles	At 25°C

Note 1: Not tested in production

TABLE 1-4: PAD COORDINATES (MICRONS)

Pad Name	**Lower Left X**	**Lower Left Y**	**Upper Right X**	**Upper Right Y**	**Passivation Openings**		**Pad Center X**	**Pad Center Y**
					Pad Width	**Pad Height**		
Ant. Pad A	-853.50	-953.90	-764.50	-864.90	89.00	89.00	-809.00	-909.40
Ant. Pad B	759.50	-955.50	848.50	-866.50	89.00	89.00	804.00	-911.00
VSS	769.10	939.70	858.10	1028.70	89.00	89.00	813.60	984.20
VDD	-839.50	83.70	-750.50	172.70	89.00	89.00	-795.00	128.20
CLK	721.10	116.00	810.10	205.00	89.00	89.00	765.60	160.50
FCLK	-821.50	872.50	-732.50	961.50	89.00	89.00	-777.00	917.00

Note 1: All coordinates are referenced from the center of the die. The minimum distance between pads (edge to edge) is 10 mil.

2: Unsawed die size = 74.96 mil x 89.15 mil.

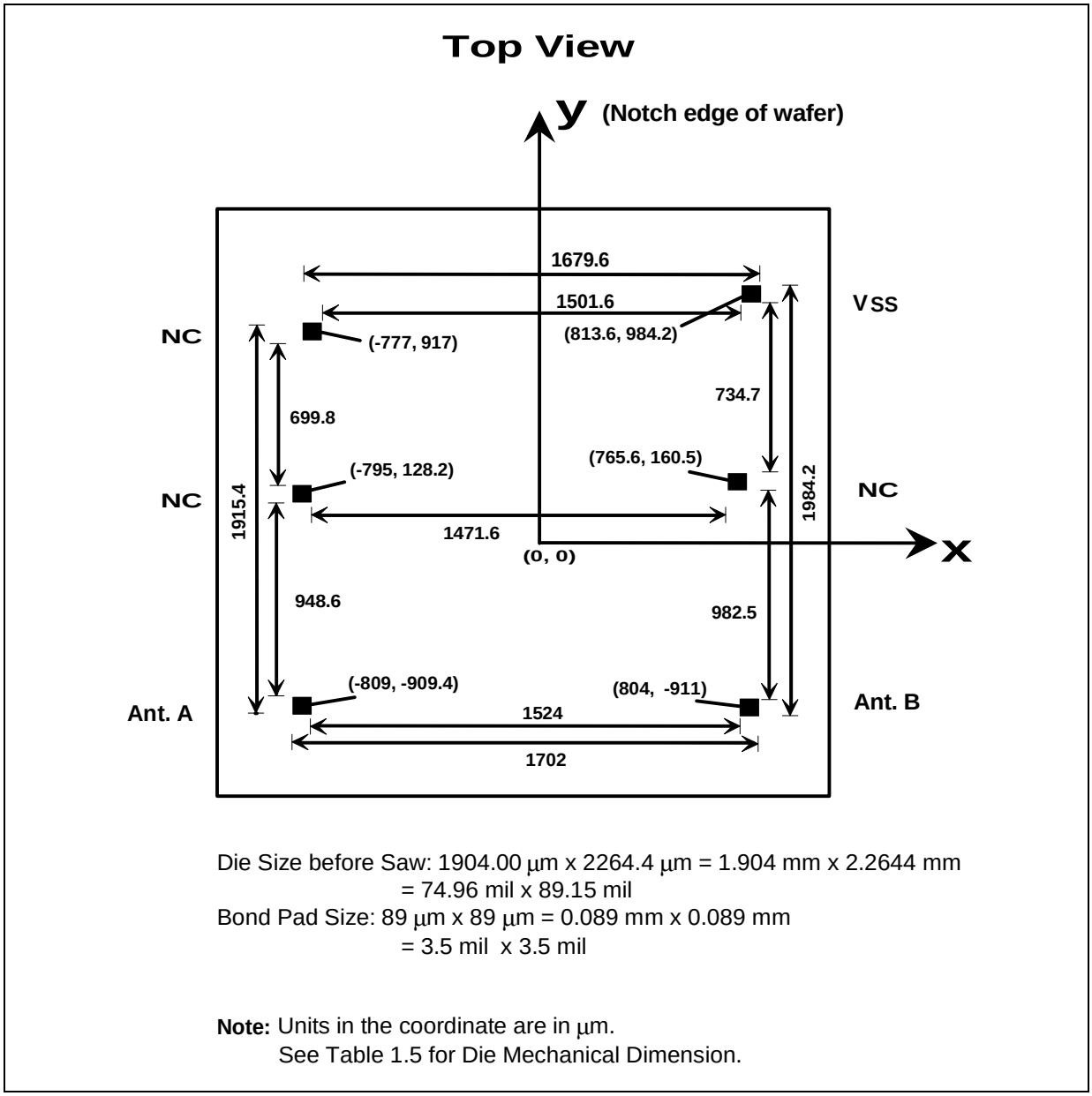
TABLE 1-5: DIE MECHANICAL DIMENSIONS

Specifications	Min.	Typ.	Max.	Unit	Comments
Bond pad opening	— —	3.5 x 3.5 89 x 89	— —	mil µm	**Note 1, Note 2**
Die backgrind thickness	— —	8 177.8	— —	mil µm	Sawed 8” wafer on frame (option = WF) **(Note 3)**
	— —	11 279.4	— —	mil µm	• Bumped, sawed 8” wafer on frame (option = WFB) • Unsawed wafer (option = W) • Unsawed 8” bumped wafer (option = WB), **(Note 3)**
Die backgrind thickness tolerance	— —	— —	±1 ±25.4	mil µm	**Note 4**
Die passivation thickness (multilayer)	—	0.9050	—	µm	**Note 5**
Die Size: Die size X*Y before saw (step size) Die size X*Y after saw	 — —	 74.96 x 89.15 73.39 x 87.58	 — —	 mil mil	 — —

Note 1: The bond pad size is that of the passivation opening. The metal overlaps the bond pad passivation by at least 0.1 mil.
2: Metal Pad Composition is 98.5% Aluminum with 1% Si and 0.5% Cu.
3: As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow.
4: This specification is not tested. For design guidance only.
5: The Die Passivation thickness can vary by device depending on the mask set used.
6: The conversion rate is 25.4 µm/mil.

Notice: Extreme care is urged in the handling and assembly of die products since they are susceptible to mechanical and electrostatic damage.

FIGURE 1-1: MCRF450/451/452/455 DIE LAYOUT



Die Size before Saw: 1904.00 μm x 2264.4 μm = 1.904 mm x 2.2644 mm
= 74.96 mil x 89.15 mil
Bond Pad Size: 89 μm x 89 μm = 0.089 mm x 0.089 mm
= 3.5 mil x 3.5 mil

Note: Units in the coordinate are in μm.
See Table 1.5 for Die Mechanical Dimension.

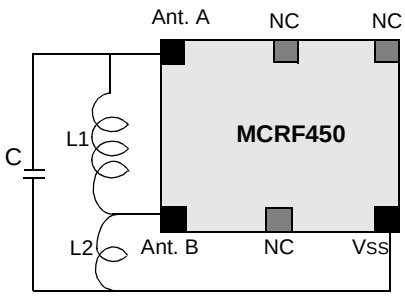
TABLE 1-6: PAD FUNCTION TABLE

Name	Function
Ant. Pad A	Connected to antenna coil L1
Ant. Pad B	Connected to antenna coils L1 and L2 (450/451/455), NC for 452
VSS	Connected to antenna coil L2 Device ground during test mode, **(Note 1)**
NC	Not connected, **(Note 2)**

Note 1: Substrate = VSS

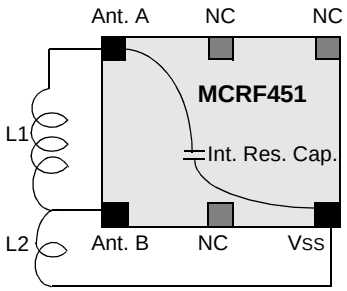
2: Leave floating or connect to VSS

FIGURE 1-2: MCRF450



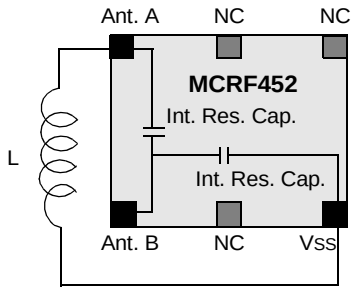
L1: External Antenna Coil A
L2: External Antenna Coil B
C: External Capacitor
NC: Not connected
Note: Substrate = VSS

FIGURE 1-3: MCRF451



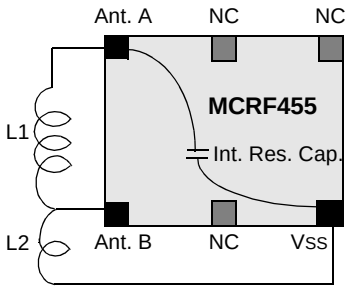
Internal Resonant Capacitor (CRES_100) = 100 pF
L1: External Antenna Coil A
L2: External Antenna Coil B
NC: Not connected
Note: Substrate = VSS

FIGURE 1-4: MCRF452



Internal Resonant Capacitor between Ant. A and Ant. B pads (CRES_2_50A) = 50 pF
Internal Resonant Capacitor between Ant. B and Vss pads (CRES_2_50B) = 50 pF
NC: Not connected
L: External Antenna Coil
Note: Substrate = VSS
Total Internal Resonant Capacitance = 25pF

FIGURE 1-5: MCRF455



Internal Resonant Capacitor (CRES_50) = 50 pF
L1: External Antenna Coil A
L2: External Antenna Coil B
NC: Not connected
Note: Substrate = VSS

2.0 BLOCK DIAGRAM

The device contains four major sections. They are: Analog Front-End, Detection/Encoding, Read/Write Anti-collision, and Memory sections. Figure 2-1 shows the block diagram of the device.

2.1 Analog Front-End Section

This section includes high and low voltage regulators, power-on-reset, 70 kHz clock generator, and modulation circuits.

2.1.1 HIGH AND LOW VOLTAGE REGULATOR

The high voltage circuit generates the programming voltage for the memory section. The low voltage circuit generates DC voltage (V_{DD}) to operate the device.

2.1.2 POWER ON RESET (POR)

This circuit generates a power-on-reset voltage. The reset releases when sufficient power has been developed by the voltage regulator to allow for correct operation.

2.1.3 CLOCK GENERATOR

This circuit generates a clock (CLK). The main clock is generated by an on-board 70 kHz time base oscillator. This clock is used for all timing in the device except for the fast mode PPM decoding.

2.1.4 DATA MODULATION

The data modulation circuit consists of a modulation transistor and an resonant LC resonant circuit. The resonant circuit must be tuned to the carrier frequency of the interrogator (i.e., 13.56 MHz) for maximum performance.

The modulation transistor is placed between antenna B and Vss pads, and is designed to result in the turn-on resistance of less than four ohms (R_M). This small turn-on resistance shorts the resonant circuit component between the antenna B and V_{SS} pads as it turns on. This results in a change of the resonant frequency of the resonant circuit. As a result, the resonant circuit becomes detuned to the carrier frequency of the interrogator. The voltage across the resonant circuit is minimized during this time. This condition is called “cloaking”.

The transistor, however releases the resonant circuit as it turns off. Therefore, the resonant circuit tunes to the carrier frequency of the interrogator again, and develops maximum voltage. This condition is called “uncloaking”.

The device transmits data by cloaking and uncloaking based on the on/off condition of the modulation transistor. Therefore, with the 70 kHz - Manchester format, the data bit “0” will be sent by cloaking and uncloaking the device for 7 µs each. Similarly, the data bit “1” will be sent by uncloaking and cloaking the device for 7 µs each. See Figure 4-1 for the Manchester waveform.

2.1.5 DETUNING CIRCUIT

The purpose of this circuit is to prevent excessive RF voltage across the resonant circuit.

This circuit monitors V_{DD} and detunes the resonant circuit if the RF coil voltage exceeds the threshold limit (V_{DETUNE}) which is above the operating voltage of the device.

FIGURE 2-1: BLOCK DIAGRAM

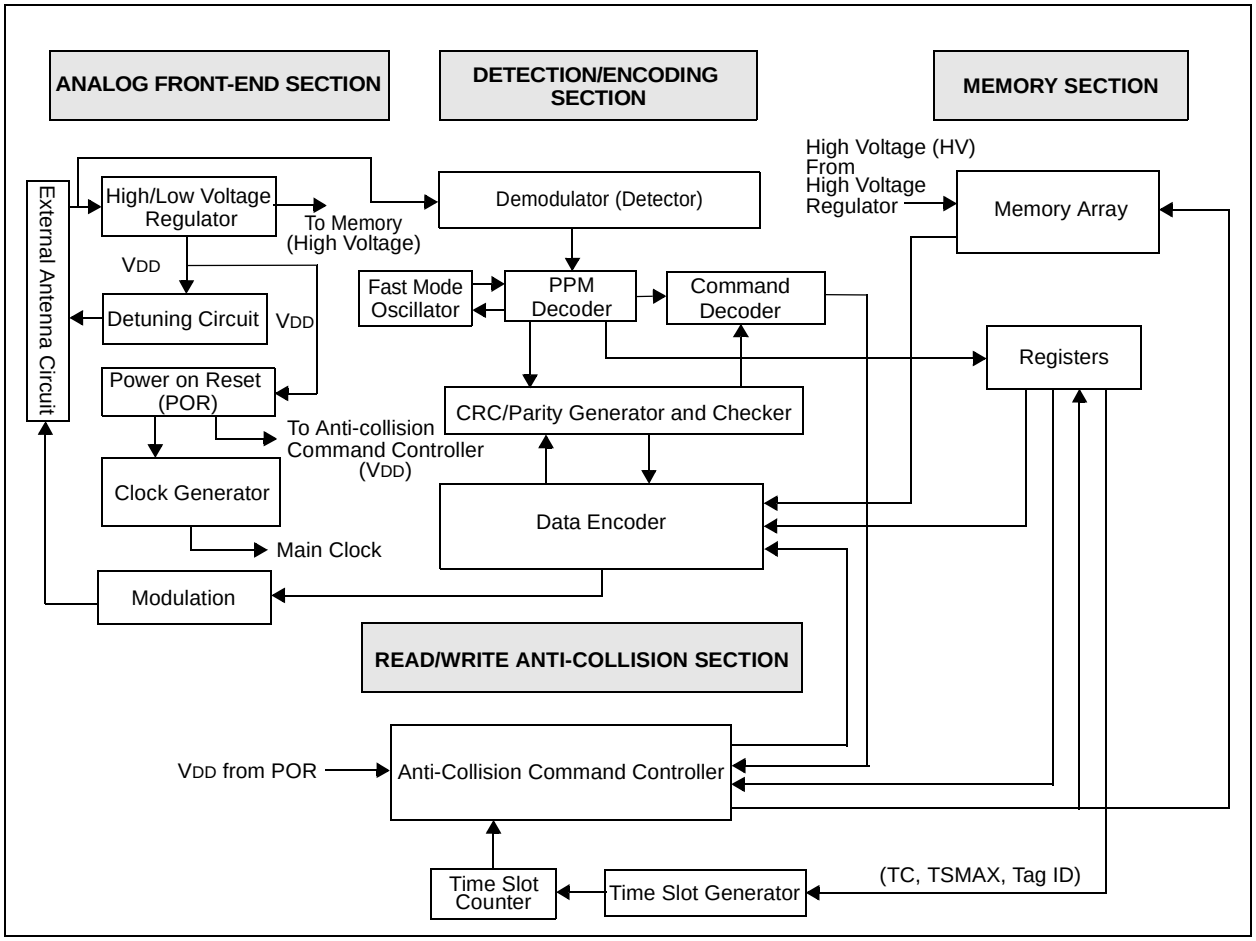
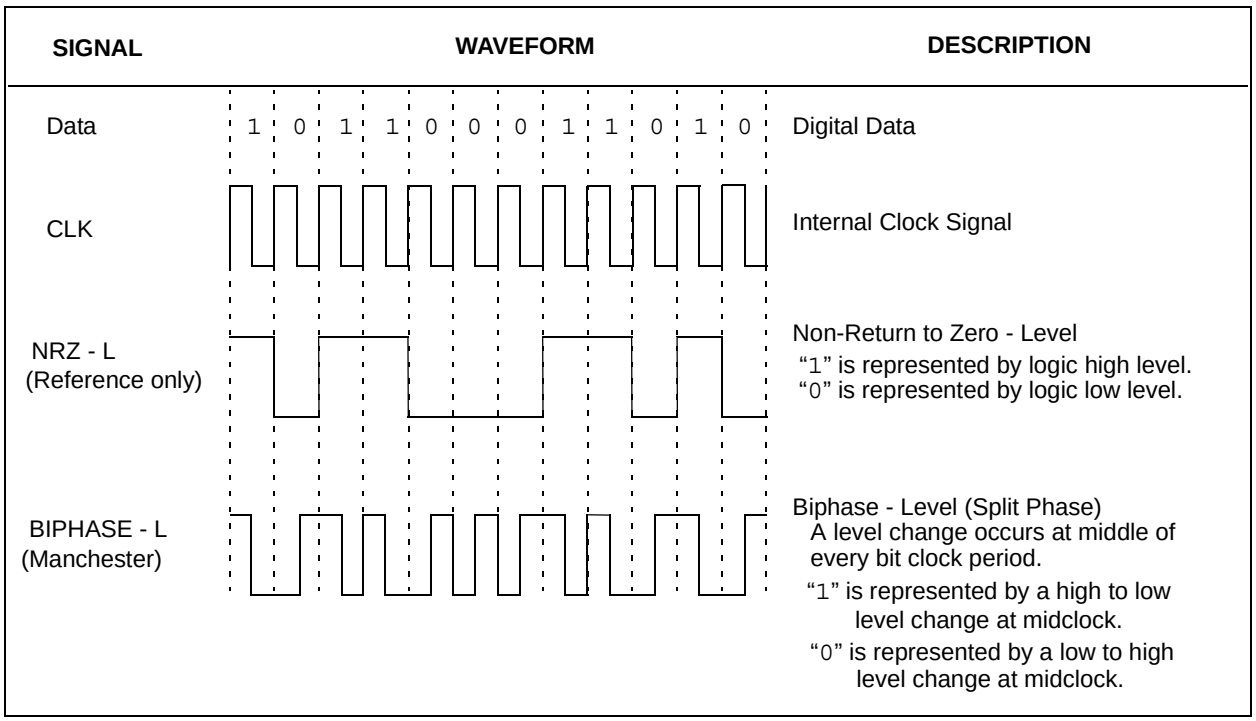


FIGURE 2-2: DATA WAVEFORM OF DEVICE



3.0 DETECTION AND ENCODING SECTION

This section encodes data with the Manchester format and also detects commands from the interrogator.

3.1 Demodulator (Detector)

This circuit demodulates the interrogator commands, and sends them to the Pulse Position Modulation (PPM) decoder.

3.2 Fast Mode Oscillator

This oscillator generates a clock that is used for decoding fast mode commands.

3.3 PPM Signal Decoder

This section decodes the PPM signals, and sends the results to both the command decoder and CRC/parity checker.

3.4 Command Decoder

This section decodes the interrogator commands and sends the results to the anti-collision/command controller.

3.5 CRC/Parity Generator and Checker

This section generates CRC and parity bits for transmitting and receiving data. The device utilizes a 16-bit cyclic redundancy code (CRC) for error detection. Its polynomial and initial values are:

CRC Polynomial: $X^{16}+X^{12}+X^5+X^0$

Initial Value: $FFFF

This polynomial is also known as CRC CCITT (Consultative Committee for International Telegraph and Telephone). The interrogator also uses the same CRC for data processing. The device uses the CRC in the following ways:

1. **Normal case:** The interrogator will send a write command with CRC. When the device receives the command, it checks the CRC prior to any processing. If it is a correct CRC, the device programs the block data and also stores the CRC in the EEPROM. As soon as the data is written in the memory, both the programmed data and stored CRC (SCRC) are sent back to the interrogator as a verification. The device also sends both the programmed data and stored CRC (SCRC) when as a response to the read command.

   If the CRC is incorrect, the device ignores the incoming message (does not respond to the interrogator) and waits for the next command with a correct CRC.

2. **Special Case 1:** When reading block 0 or 2, a calculated CRC (CCRC) is sent. This is because both the TF and FR bits in the block 0 are non-write-protectable while the rest of the bits in the block are write-protectable. This means the stored CRC (SCRC) in the block no longer represents the CRC of the block data if only the TF or the FR bit is reprogrammed. This is also true for block 2 which is a write-protection block: The write-protected bit can not be reprogrammed once it has been written. Therefore, the stored CRC in these blocks (0 and 2) are not used. Instead, the device calculates the current CRC of the block and sends it to the interrogator.
3. **Special Case 2:** For the Fast Read (FR) response (this is the device response to an FRR command), bits 0-15 (FRR_CRC) in block 0 are sent as the CRC of the fast read field (FRF: blocks 3-5). See Table 4-3 for device responses.

3.6 Data Encoder

This section multiplexes serial data, encodes it into Manchester format, and sends it to the modulation circuit. See Figure 2-2 for the Manchester waveform.

4.0 READ/WRITE ANTI-COLLISION LOGIC

This section includes the anti-collision algorithm of the device, and consists of the anti-collision/command controller, the time slot counter, and the time slot generator.

4.1 Description of Algorithm

The read and write anti-collision algorithm is based on time division multiplexing of tag responses. Each device is allowed to communicate with the interrogator in its time slot only. When not in its assigned time slot, the device remains in a non-modulating condition. This enables the interrogator to communicate with other devices in the same interrogator field with fewer chances of data collision.

Figure 4-1 shows the anti-collision algorithm flowchart, which consists of four control loops. They are: Detection, Processing, Sleeping, and Reactivation loops. All devices in the interrogator's RF field are controlled by five different commands and internal control flags.

The interrogator commands are:

1. **Fast Read Request (FRR):** If the TF bit of the device is cleared, then it will respond to only this command from the interrogator. This command consists of five specially timed gap pulses. See Figs. 4-3 to 4-8. The position of the five gap pulses in the given time span (1.575 ms) determines the parameters of the command. The command has three parameters: TCMAX, TSMAX, and Data transmission speed. The details of these parameters will be discussed in the following sections. If the device receives the FRR command, it sends the fast read (FR) response (96 bits in default) and then listens for 1 ms (TLW) for a matching code from the interrogator.
2. **Fast Read Bypass (FRB):** This command is used in the Reactivation loop. This command is only applicable to a device with the fast read bit (FR bit: bit 31 in block 0) cleared. The device responds with 64 bits of data which includes block 1 data (32-bit Tag ID), and then listens for 1 ms (TLW) for a matching code from the interrogator. The command structure is the same as the FRR command: Five specially timed gap pulses (1.575 ms). The command parameter (see Figure 4-8) determines the data rate (normal speed or fast speed) of subsequent interrogator commands.
3. **Matching Code 1 (MC1):** This command consists of time calibration pulses (TCP) followed by 1-of-16 PPM signals. It is used when the device does not need any further processing. This MC1 command causes a device which is in the Detection loop to enter the Sleeping loop.
4. **Matching Code 2 (MC2):** The command structure is the same as MC1: TCP followed by 1-of-16 PPM signals. The command is used when the device needs further processing (read/write). The device enters the Processing Loop if it receives this command in the Detection Loop.

   The matching code (MC1 and MC2) command consists of 12 bits (or 3 symbols). The first 8 bits (or the first two symbols) are selected from the 32-bit Tag ID. The next 4 bits (or the 3rd symbol) determine the matching code type (3 bits) and a parity bit (see Section 4.2.3.6). The command lasts for about 11.2 ms including the time calibration pulses.
5. **End Process (EP):** This command consists of the time reference pulses followed by 1-of-16 PPM signals. The EP command causes a device to exit the Processing loop and enter the Sleeping loop.

4.1.1 DETECTION LOOP

The device can enter this loop in two ways if the fast read (FR: bit 31 of block 0) bit is set. The two ways depend on the condition of the talk-first (TF: bit 30 of block 0) bit. They are: (1) If the TF bit is cleared, the device enters this loop and waits for a fast read request (FRR) command. This is called "interrogator talks first" (ITF) mode. (2) If the TF bit is set, the device enters this loop by transmitting the fast read (FR) response without waiting for an FRR command. This case (2) is called "tag talks first" (TTF) mode.

For case (1) above, the parameters of the FRR are:

(a). Maximum number of time slots (TSMAX=1, 16, or 64),

(b). Maximum transmission counter (TCMAX = 1, 2, or 4), and

(c). Data transmission speed (normal or fast mode).

The purpose of the TCMAX and TSMAX parameters is to acknowledge the device in the Detection loop as fast as possible. TSMAX represents the maximum number of time slots between the end of the FRR command and the beginning of the fast read (FR) response. One time slot (TSLOT) represents 2.5 ms. For example, TSMAX = 64 represents a maximum of 160 ms of time delay before sending the FR response. See Section 4.2.4 for the calculation of actual time delay. TCMAX represents the maximum number of fast read (FR) responses a device can send after an FRR command. For example, TCMAX = 4 means the device can send its FR response four times (after the FRR command) for acknowledgment (matching code).

The TSMAX and TCMAX values are determined by the interrogator's decision on how many tags are in the field. The interrogator may assign TSMAX = 1 and TCMAX = 1 assuming there is only one tag in the field. The efficiency of the detection will increase in multiple

tag environments by assigning a higher number to both the TSMAX and TCMAX. If the device receives the FRR, it clears the Position 1 flag, waits for its time slot and replies with the fast read (FR) response and then listens for 1 ms. The FR response consists of a maximum of 160 manchester data bits (default: 96 bits, see Table 4-3 and Example 7-1) which includes the 32-bit Tag ID and the fast read field data (blocks 3-5).

To acknowledge the FR response, the interrogator can start to send a matching code (MC) during the device's 1 ms listening window (T_{LW}). The MC is encoded with 1-of-16 PPM signal. See Figure 4-9 for the 1-of-16 PPM signal. The MC1 is given to the device if the device does not need any further processing. If the device receives the MC1, it enters the Sleeping loop and stays in the loop in a non-modulating condition. The MC2 command is given to the device if further processing (read/write) is required. If the device receives the MC2 command, it enters the Processing loop.

If the device misses the MC within the listening window, it sends the FR response again after its time slot if two conditions are met: (1) Position 1 flag is cleared and (2) TCMAX has not elapsed. The device checks the condition (elapsed or not elapsed) of TCMAX using an internal transmission counter (TC). The transmission counter (TC) consists of 3 bits. If the Position 1 flag is cleared, the device increments the TC by 1 each time it does not receive a MC during its listening window. See the flow chart in Figure 4-1 for the conditional increment of the transmission counter. Table 4-1 shows an example of detecting the elapsed TCMAX using a rolling modulo-8 transmission counter.

For the TTF case, the device repeats its FR response according to the TCMAX and TSMAX parameters as specified in Table 5-5. Even though the device is operating in TTF mode, it will respond to its correct MC during its listening window. If TCMAX = 1, 2 or 4, it will also respond to FRR commands just as in the ITF case (see Section 4.1.1.1).

4.1.1.1 Matching Code Queuing

Once the device receives the FRR command, it sends the FR response and waits for a matching code (MC) during its listening window. If the device does not receive its correct MC code before its TCMAX has elapsed (see Table 4-1), it goes back to the beginning of the Detection loop (position 1 in the loop), and waits for either a new FRR command or matching code (MC1 or MC2). This is called "matching code queuing". In this queuing, the device stays in the Detection loop waiting for an interrogator command (FRR or MC). This queuing takes place within the Detection loop and is controlled by the conditions of Set Position 1 Flag and TCMAX.

This queuing allows the interrogator to communicate with a device outside its listening window. The result is enhanced and accelerated processing of individual devices in a multiple tag environment.

TABLE 4-1: CONDITIONS FOR TCMAX = ELAPSED FOR ITF MODE

Rolling Modulo -8 TC			TCMAX = 1	TCMAX = 2	TCMAX = 4
0	0	1	elapsed	—	—
0	1	0	elapsed	elapsed	—
0	1	1	elapsed	—	—
1	0	0	elapsed	elapsed	elapsed
1	0	1	elapsed	—	—
1	1	0	elapsed	elapsed	—
1	1	1	elapsed	—	elapsed
0	0	0	elapsed	elapsed	—

4.1.2 PROCESSING LOOP

The reading and writing processes take place in this loop. Devices in this loop are waiting for commands for processing. In order to read from or write to the device, its "Processing Flag" (PF) must be set. Any device entering this loop with its PF cleared is called a follow-along tag. This follow-along tag in the loop is not processed for reading or writing.

If the device with PF set receives the End process (EP) command, it exits this loop and enters the Sleeping loop. However, the same EP command sends the follow-along tag back to the Detection loop.

If the device receives the FRR or FRB command in this loop, it sees the command as invalid, resets itself, and goes back to the initial power up state.

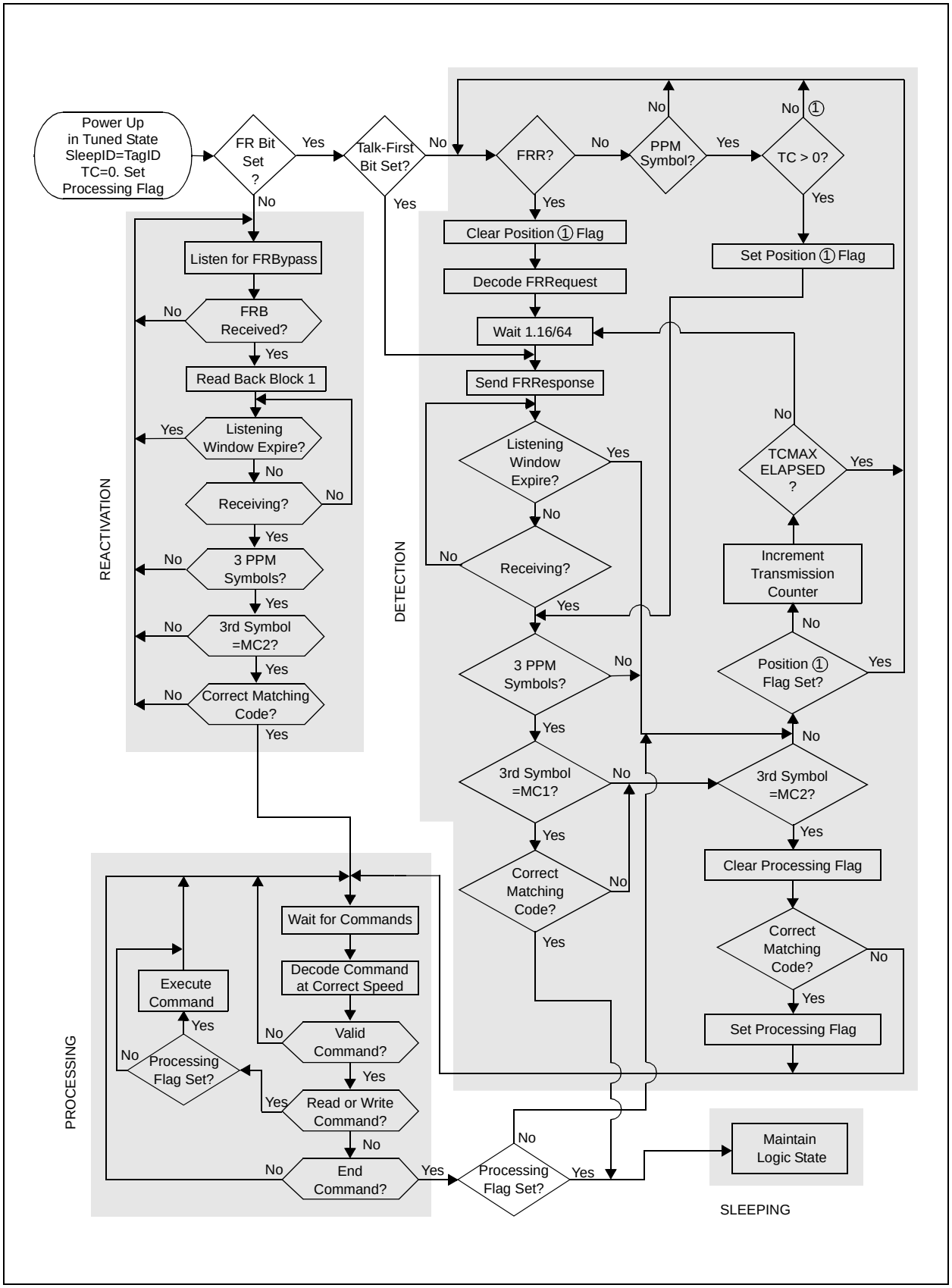
4.1.3 SLEEPING LOOP

This loop is used to keep all processed devices in a "silent" condition. The devices stay in this loop in a non-modulating condition as long as they remain in the field.

4.1.4 REACTIVATION LOOP

This loop is used to process a device with its fast read (FR) bit cleared. A device in this loop waits for the fast read bypass (FRB) command. If a device receives the FRB, it transmits the contents of block 1 (Tag ID) in its memory and waits for matching code 2 (MC2) in its listening window. If the device in this loop receives matching code 2 (MC2), it leaves this loop and enters the Processing loop. This reactivation loop has no anti-collision capability; it is designed for reactivation of single devices. This loop can be effectively used in retail store applications to process returning items from customers.

FIGURE 4-1: ANTI-COLLISION FLOW CHART



4.2 Anti-Collision Command Controller

This section manages the anti-collision algorithm and establishes the communications between the interrogator and device.

4.2.1 STRUCTURE OF READ/ WRITE COMMAND SIGNALS

The interrogator's read/write commands have the following structure:

Read/Write command = Command + Address + Data + Parity (or CRC)

The commands are summarized in the table below:

TABLE 4-2: READ/WRITE COMMANDS FROM INTERROGATOR TO DEVICE

Interrogator Command	Command Code	Address	Data	Parity or CRC	Symbol Length
Unused	00x	xxxxx	—	—	—
Read 32-bit block	110	aaaaa	—	Parity	3 symbols
Unused	111	00xxx	—	—	—
Unused	111	0100x	—	—	—
End Process	111	01010	—	Parity	3 symbols
Unused	111	01011	—	—	—
Unused	111	011xx	—	—	—
Unused	111	1000x	—	—	—
Set Talk First Bit	111	10010	—	Parity	3 symbols
Set FR Bit	111	10011	—	Parity	3 symbols
Clear Talk First Bit	111	10100	—	Parity	3 symbols
Clear FR Bit	111	10101	—	Parity	3 symbols
Unused	111	1011x	—	—	—
Unused	111	11xxx	—	—	—
Unused	100	xxxxx	—	—	—
Write 32-bit block	101	aaaaa	32 bits	CRC-16	14 symbols
Unused	01x	xxxxx	—	—	—

Legend: aaaaa = Block address
x = don't care
Command and address are sent MSN (most significant nibble) first
Data and parity/CRC are sent LSN (least significant nibble) first.

4.2.2 STRUCTURE OF DEVICE RESPONSE

When the device receives the interrogator command, it responds with 70 kHz - Manchester encoded data having the following structures:

For blocks 0 and 2:

Device Response = Preamble (8 bits) + Block Number (5 bits) + "000" + Block Data (32 bits) + Calculated CRC (CCRC: 16 bits)

For all other blocks:

Device Response = Preamble (8 bits) + Block Number (5 bits) + "000" + Block Data (32 bits) + Stored CRC (SCRC: 16 bits)

TABLE 4-3: INTERROGATOR COMMANDS AND DEVICE RESPONSES

Interrogator Command	Delay	Device Response
Read 32-bit block for block 0 and block 2	TDECODE	Preamble, block #, "000", block data, CCRC
Read 32-bit block except for block 0 and block 2	TDECODE	Preamble, block #,"000", block data, SCRC
Write 32-bit block	TWRITE	For blocks 0 and 2: Preamble, block #, "000",block data, CCRC For all others: Preamble, block #, "000", block data, SCRC
Set Fast Read (FR) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
Clear Fast Read (FR) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
Set Talk First (TF) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
Clear Talk First (TF) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
End Process (EP)	TDECODE	Preamble
FRR	f(TSMAX, TCMAX, 8-bit Tag ID)	Preamble,TC, TP, "0", Tag ID, FRF, FRR_CRC (bits 0-15 in block 0) (maximum of 160 data bits)
FRB	TDECODE	Preamble, address of block #1(00001),"000", Tag ID (32 bits), SCRC (64 data bits)

References used in this table. Examples are given in Section 7.0.

Preamble =	11111110 (8 bits)."0" is transmitted last.
Block # =	5 bit addressed block, transmits LSB (least significant bit) first.
Block data =	32-bit data of the addressed block, transmits LSB first.
CCRC =	Calculated CRC of the preceding block number and block data. Transmits LSB first.
SCRC =	Stored CRC. This SCRC is the CRC of the write command, address, and data from the interrogator, LSB first. The device stores the CRC of the command for each block. See Section 5.2 for details.
TP =	Tag parameters (4 bits: "0", DF0, DF1, parity). where DF0 and DF1 determine the FR field length (see Table 5-6).
TC =	Transmission counter (3 bits), transmits LSB first.
Parity =	Even parity bit of TC and TP.
Tag ID =	32 bits of unique identification code of the device, transmits LSB first. This Tag ID is pre-programmed in the factory prior to shipping.
8-bit Tag ID =	8 bits of Tag ID selected from the 32 bits of the unique tag identification code. Transmits LSB first (see Section 4.2.3.6 for selecting the 8 bits from the Tag ID).
FRF =	Fast Read Field (blocks 3-5), transmits LSB first (see Section 5.0).
f(TSMAX, TCMAX, 8-bit Tag ID =	Delay is a function of the TSMAX, TCMAX and 8-bit Tag ID.
TWRITE =	Writing time for EEPROM (see Table 1-3).
FRR_CRC =	CRC of 32-bit Tag ID first followed by fast read field (FRF) data.
TDECODE =	Time requirement for command decoding (see Table 1-3).

4.2.3 DETECTION OF INTERROGATOR COMMANDS

The interrogator sends commands to the device by amplituding modulating the carrier signal (gap pulse). The interrogator uses two classes of encoding signals for modulation. They are (a) 1-of-16 PPM for data transmission, and (b) specially timed gap pulse sequence for the fast read commands (FRR and FRB). The fast read commands consist of five gap pulses within nine possible gap pulse positions (1.575 ms). The combination of the possible gap positions determines the command type and parameters of the fast read command.

The interrogator also sends time calibration pulses (TCP) prior to the 1-of-16 PPM. The TCP is used to calibrate the time base of the decoder in the device. The specifics of the two encoding methods and the TCP are described in the following sections.

4.2.3.1 FAST READ COMMANDS

The fast read commands are composed of five 175 µs-wide gap pulses (see Figure 4-2) whose spacing within 1.575 ms determines the command type and its parameters. Table 4-4 shows the specification of the gap signal for the fast read commands. Two commands are used for the fast read. They are: (1) Fast Read Request (FRR) in the Detection loop, and (2) Fast Read Bypass (FRB) in the Reactivation loop. See Tables 4-5 and 4-6 for the FRR gap pulse positions and also Figures 4-3 to 4-8 for the gap modulation patterns.

The parameters of FRR are (1) number of time slots (TSMAX = 1,16,or 64), (2) max transmission counter (TCMAX), and (3) data transmission speed. The FRB has only a data transmission speed parameter (normal or fast speed mode). The device extracts these parameters based on the positions of the five gap pulses within the 1.575 ms time span as shown in Figures 4-3 to 4-8.

TSMAX=1 is given if there is only one device in the field. This is called “conveyor mode” or “single tag environment”. In this mode, the device responds with the FR response signal in every time slot until it receives a correct matching code, or until TCMAX is elapsed.

4.2.3.2 DATA TRANSMISSION SPEED

The interrogator can send data with two different data rates: (1) Normal and (2) Fast speed modes. The normal speed uses 2.8 ms/symbol, and the fast speed uses 160 µs/symbol. One symbol represents one 4-bit data packet (see Section 4.2.3.4 for 1-of-16 PPM). The data transmission speed is a parameter of the fast read commands (FRR and FRB). This parameter indicates the data speed of subsequent interrogator commands. The data rate of the device output (70 kHz) is not affected by this parameter.

TABLE 4-4: SPECIFICATION OF GAP SIGNAL FOR FAST READ COMMANDS (FRR AND FRB)

Number of gaps for one command	5
Total available number of gap positions within the command time span	9
Command time span	1.575 ms
Gap pulse width	175 µs

TABLE 4-5: SPECIFICATION OF MODULATION SEQUENCE FOR FAST READ REQUEST (FRR)

Maximum Time Slot (TSMAX)	TCMAX	Gap Pulse Position	Data Transmission Mode
1	1	(1,2,3,4,6)	Normal Speed
		(1,3,5,6,8)	Fast Speed
	2	(1,2,3,4,5)	Normal Speed
		(1,3,5,6,7)	Fast Speed
	4	(1,2,3,5,6)	Normal Speed
		(1,3,5,7,8)	Fast Speed
16	1	(1,2,4,6,8)	Normal Speed
		(1,3,4,6,8)	Fast Speed
	2	(1,2,4,6,7)	Normal Speed
		(1,3,4,6,7)	Fast Speed
	4	(1,2,4,5,6)	Normal Speed
		(1,3,4,5,6)	Fast Speed
64	1	(1,2,4,5,7)	Normal Speed
		(1,3,4,5,7)	Fast Speed

TABLE 4-6: SPECIFICATION OF MODULATION SEQUENCE FOR FRB COMMAND

Symbol	Gap Pulse Position	Data Transmission Mode
FRB_N	(1,2,3,5,7)	Normal Speed
FRB_F	(1,3,5,7,9)	Fast Speed

FIGURE 4-2: PULSE WAVEFORM OF GAP AND 1-OF-16 PPM SIGNALS

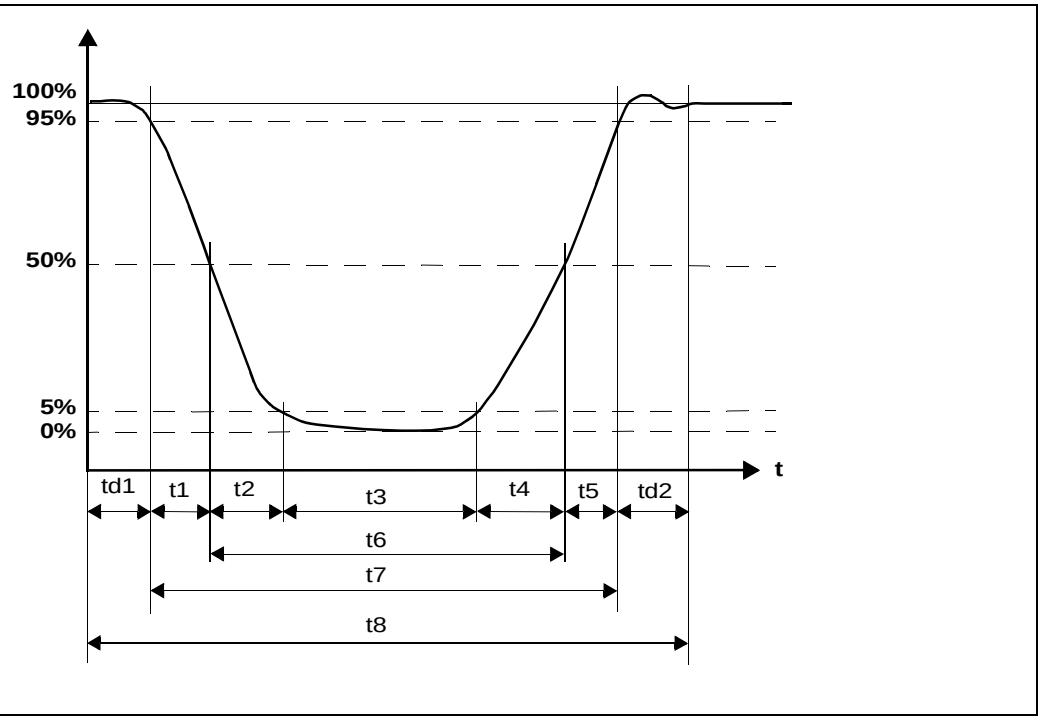


TABLE 4-7: WAVEFORM CHARACTERISTICS OF GAP AND 1-OF-16 PPM SIGNALS

Signal	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gap signal and 1-of-16 PPM for normal mode	td1	—	25	—	µs	—
	td2	—	25	—	µs	—
	t1	0	12.5	—	µs	—
	t2	0	12.5	—	µs	—
	t3	—	75	—	µs	—
	t4	0	12.5	—	µs	—
	t5	0	12.5	—	µs	—
	t6	—	100	—	µs	PW_{PPM_N}
	t7	—	125	—	µs	—
	t8	—	175	—	µs	—
1-of-16 PPM for fast mode	td1	—	1.25	—	µs	—
	td2	—	1.25	—	µs	—
	t1	0	0.75	—	µs	—
	t2	0	0.75	—	µs	—
	t3	—	4.5	—	µs	—
	t4	0	0.75	—	µs	—
	t5	0	0.75	—	µs	—
	t6	—	6	—	µs	PW_{PPM_F}
	t7	—	7.5	—	µs	—
	t8	—	10	—	µs	—

The following figures show the various modulation patterns of the fast read commands (FRR and FRB). Each command consists of a combination of five gap pulses within nine possible gap positions. The pulse width of each gap is 175 µs and the total time span of each command for the nine possible positions is 1.575 ms (175 µs x 9 = 1.575 ms).

In the figures, P*mn* represents *m*th gap pulse at *n*th gap position in the given data packet (symbol).

FIGURE 4-3: GAP MODULATION PATTERNS FOR FRR, NORMAL SPEED, TSMAX = 1

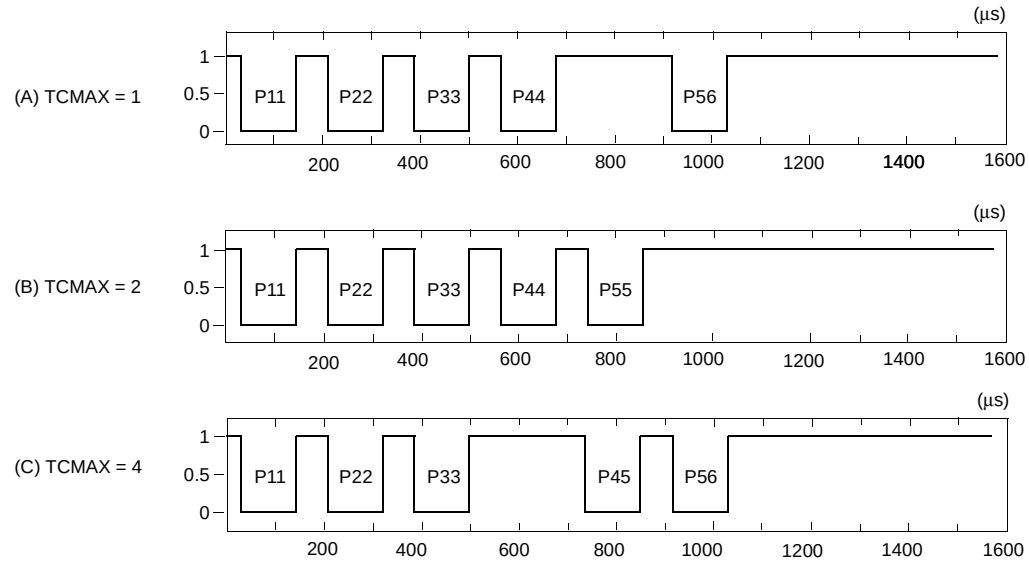


FIGURE 4-4: GAP MODULATION PATTERNS FOR FRR, FAST SPEED, TSMAX = 1

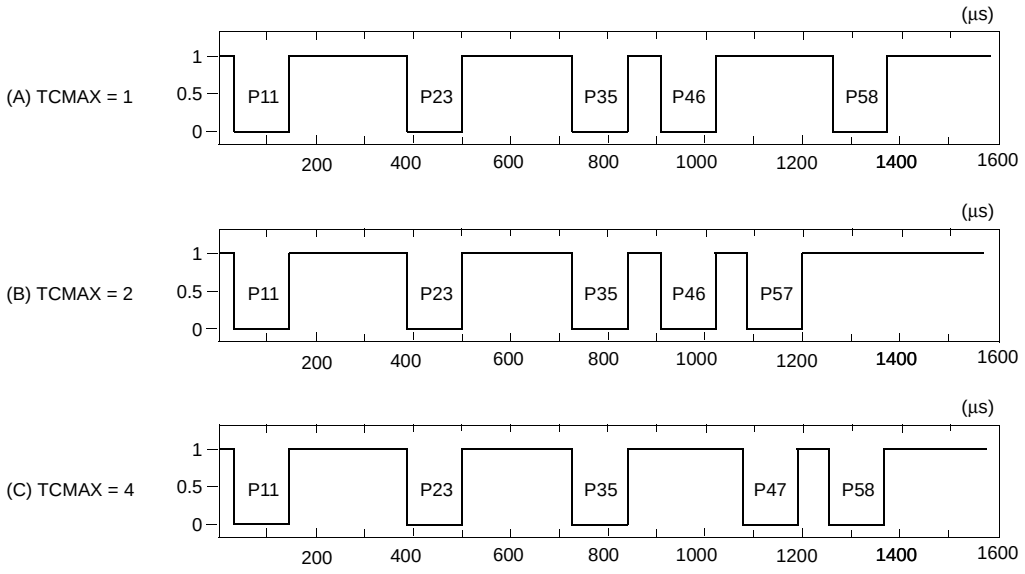


FIGURE 4-5: GAP MODULATION PATTERNS FOR FRR, NORMAL SPEED, TSMAX = 16

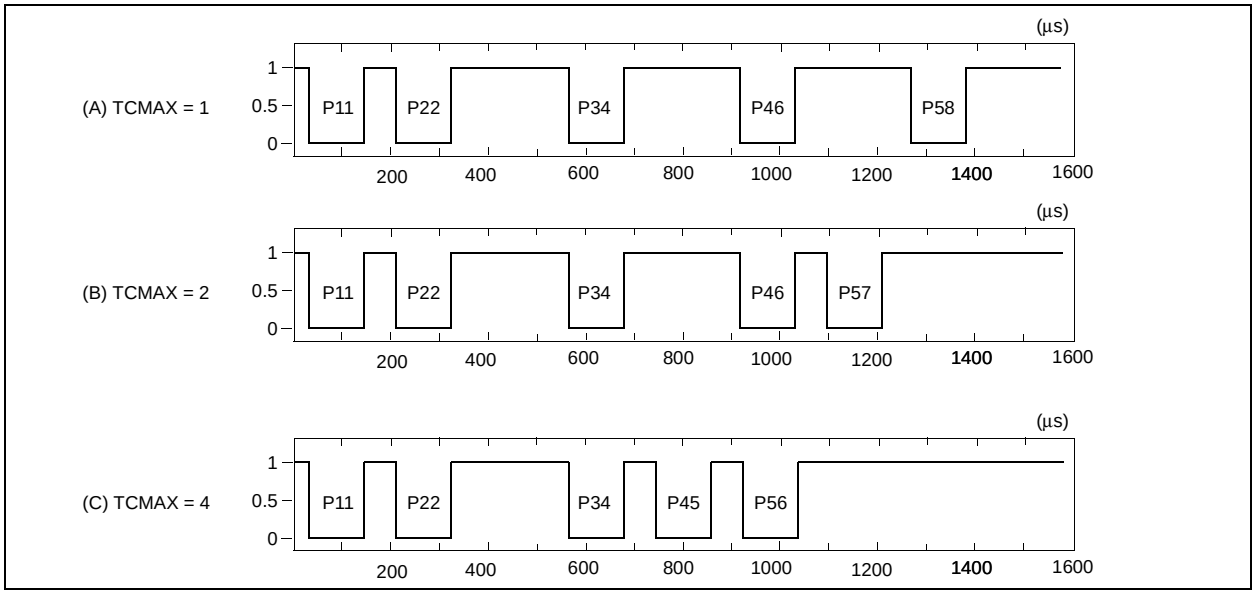


FIGURE 4-6: GAP MODULATION PATTERNS FOR FRR, FAST SPEED, TSMAX = 16

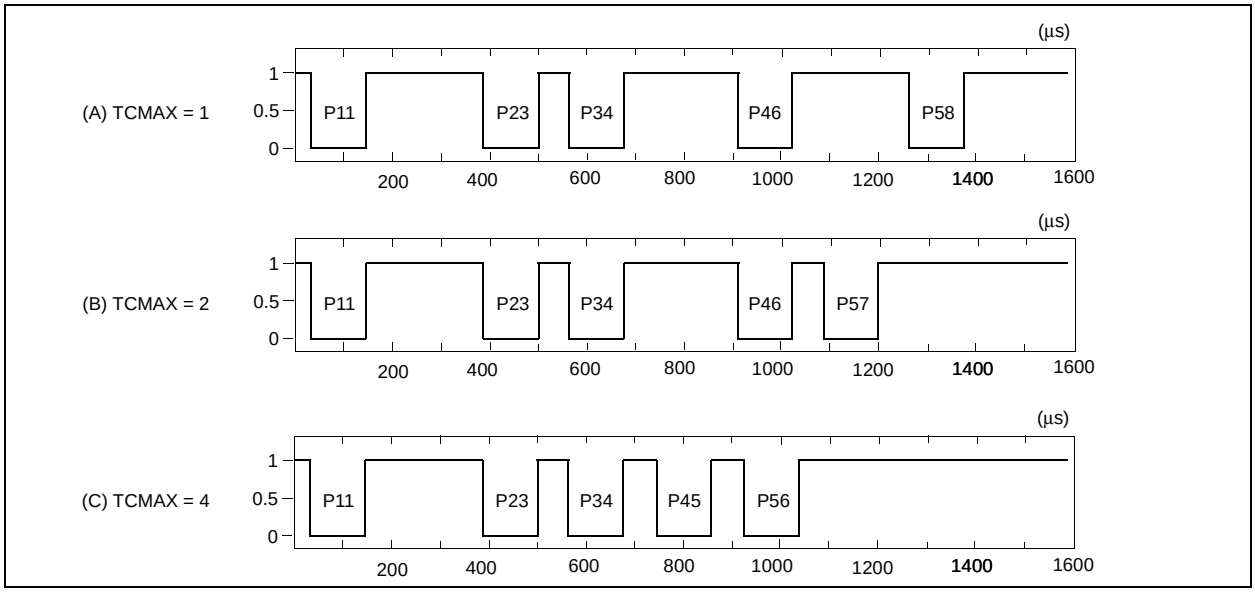


FIGURE 4-7: GAP MODULATION PATTERNS FOR FRR, TSMAX = 64, TCMAX = 1

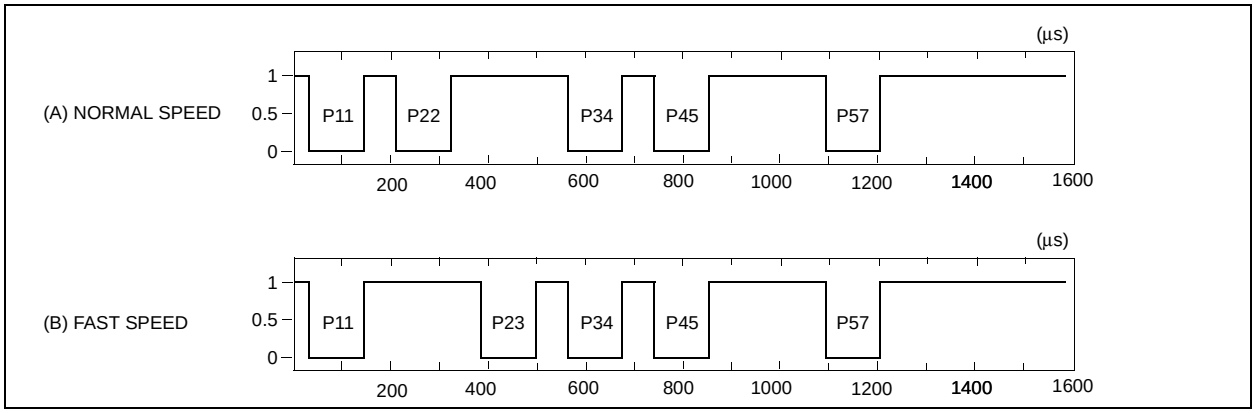
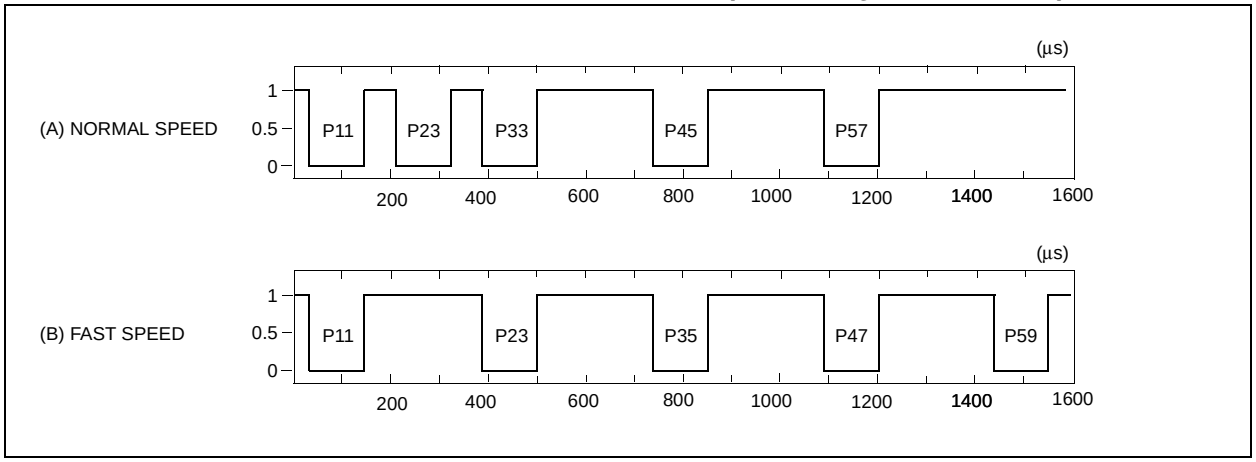


FIGURE 4-8: GAP MODULATION PATTERNS FOR FRB (FAST REQUEST BYPASS)



4.2.3.3 USAGE OF TSMAX AND TCMAX

The parameters of the TSMAX and TCMAX are determined by an expected number of tags in the Detection Loop. The following table shows the recommended FRR command repeat time for each of the 7 possible combinations of TSMAX and TCMAX. The command repeat time in Table 4-8 is calculated by:

Command Repeat Time = TSMAX x TCMAX x 2.5ms x 1.17

where:

1.17 is related to the tolerance of the baud rate.

TABLE 4-8: FRR COMMAND REPEAT TIME VS. (TSMAX, TCMAX)

(TSMAX,TCMAX)	(1,1)	(1,2)	(1,4)	(16,1)	(16,2)	(16,4)	(64,1)
Command Repeat Time	2.925 ms	5.85 ms	11.7 ms	46.8 ms	93.6 ms	187.2 ms	187.2 ms

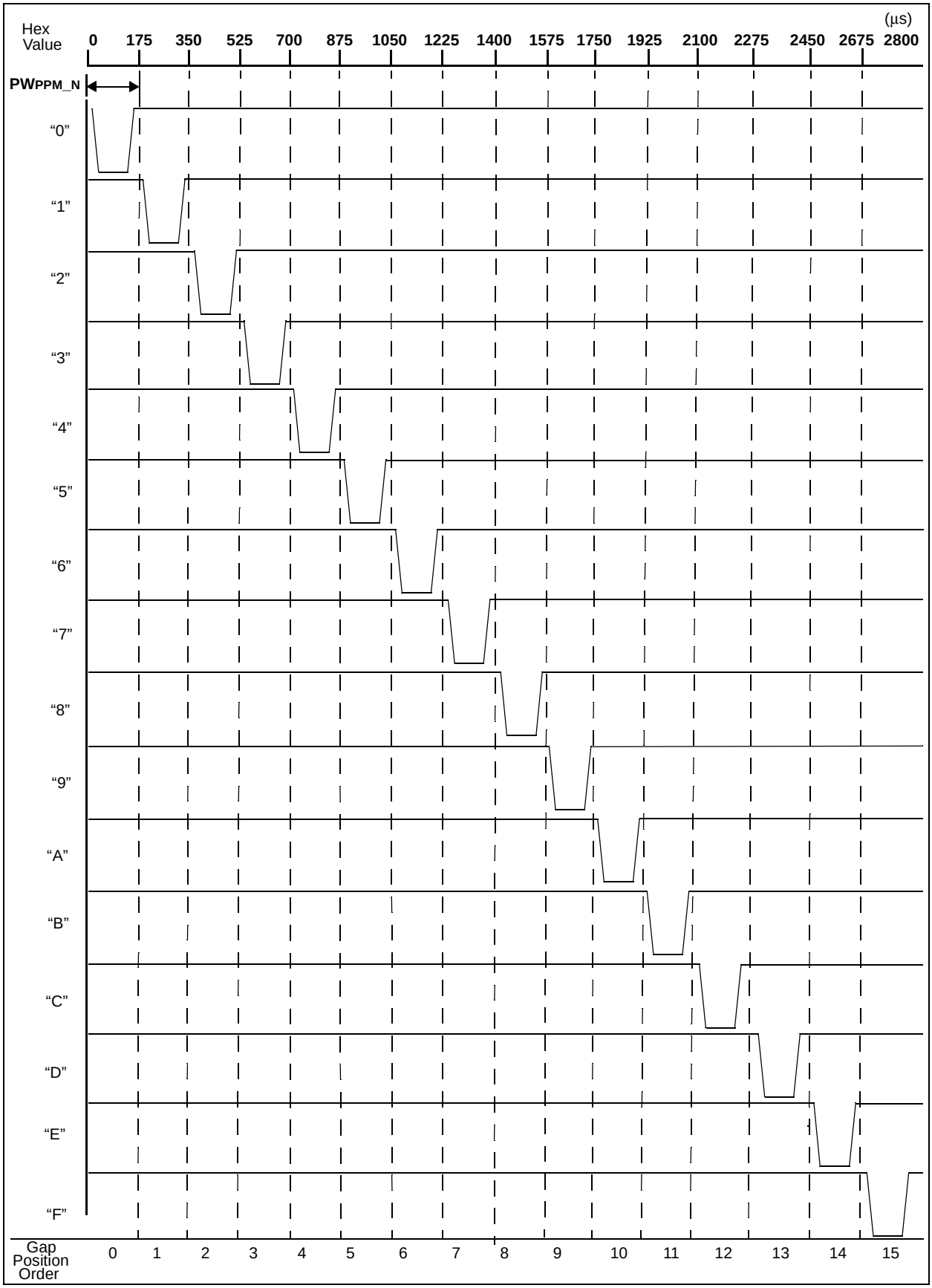
4.2.3.4 1-OF-16 PPM

The interrogator uses 1-of-16 Pulse Position Modulation (PPM) for matching codes (MC1 and MC2), End Process (EP), and also commands in Table 4-2. 1-of-16 PPM uses only one gap pulse in one of sixteen possible pulse positions for sending 4-bit symbols (2^4=16). This means one symbol (one data packet) represents 4 bits of binary data. One symbol lasts for 2.8 ms and 160 µs for normal speed and fast speed mode, respectively. All communications begin with time calibration pulses (TCP) composed of three pulses in positions zero, six and fourteen of a 1-of-16 PPM symbol as shown in Figure 4-10.

TABLE 4-9: 1-OF-16 PPM PULSE SPECIFICATIONS

	Normal Mode	**Fast Mode**
Modulation depth	100%	100%
Pulse width	175 µs	10 µs
Gap width	100 µs	6 µs
Pulse positions per symbol	16	16
Symbol width	2.8 ms	160 µs
Calibration sequence	Pulses in positions 0,6,14	Pulses in positions 0,6,14

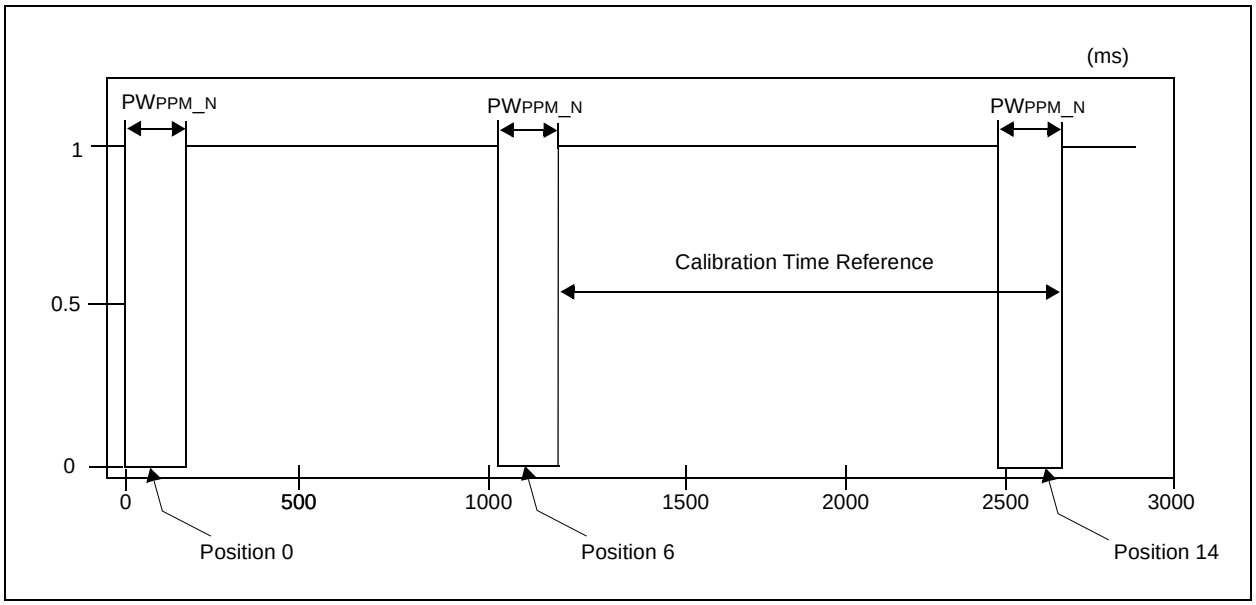
FIGURE 4-9: 1-OF-16 PPM REPRESENTATION FOR HEX VALUES FOR NORMAL SPEED MODE



4.2.3.5 CALIBRATION OF TIME REFERENCE FOR DECODING

The device uses time calibration pulses (TCP) to match its internal decoder timing to the interrogator timing. The interrogator transmits the timing pulses at the start of all commands and at least every 17 symbols. The TCP uses a code violation of the 1-of-16 PPM signal consisting of three gap pulses within one symbol. The first gap pulse is located at position 0, the second gap pulse at position 6, and the third at position 14 of the symbol. The time period between the last two gap pulses is used to calibrate the device's timing for decoding. Figure 4-10 shows the calibration pulses for normal speed mode. The waveform of the gap pulses is the same as the 1-of-16 PPM signal as shown in Figure 4-2. For the fast speed mode, the gap positions are the same. PW_{PPM_F} is the gap pulse width and SW_{PPM_F} is the symbol width of the fast mode.

FIGURE 4-10: CALIBRATION PULSES FOR NORMAL SPEED MODE



4.2.3.6 CALCULATION OF MATCHING CODE

When the interrogator receives the FR response from a device, it sends a matching code (MC) to select the device. The MC is sent during the device's listening window. There are two different types of matching codes. They are MC1 and MC2. Both MC1 and MC2 are used in the Detection loop and MC2 is used in the Reactivation loop as detailed in Figure 4-1. The MC1 command is used to send the device to the Sleeping loop, and MC2 is used to send the device to the Processing loop.

The MC is an 8-bit "match" of tag ID followed by 4-bit matching code type and parity bit such that:

> Matching code (12 bits) = "match (8 bits of tag ID)" + matching code type (3 bits)+ parity (1 bit)

The matching code type and parity bit is bit-wise structured as follows:

- MC1: 010P
- MC2: 100P

where P represents the parity bit of all match bits (8 bits) plus the MC type (3 bits).

The "match" part of the MC is eight bits of the 32-bit Tag ID. The interrogator selects the 8 bits from the 32-bit Tag ID by calculating the bit range of the Tag ID. Equation 4-1 shows the equation for selecting the bit range using the transmission counter (TC). Both the 32-bit Tag ID and TC are included in the FR response. An example for the calculation of the matching code is given in Section 7-2.

EQUATION 4-1: BIT-WISE EQUATION FOR "MATCH"

"Match" = Tag ID bit range a: b
{4*TC} modulo 32: {4 (TC +1) + 3} modulo 32

where {} modulo 32 means the remainder of {} divided by 32. For example, {28} modulo 32 and {35} modulo 32 are 28 and 3, respectively.

4.2.4 TIME SLOT GENERATOR

This block generates time slots for the device. The time slot represents the time delay between the end of the FRR command and the beginning of the FR response. The available time slots are 1, 16 or 64. One time slot represents 2.5 ms. The device calculates the actual time slot based on the TSMAX, TC and Tag ID. The maximum time slot (TSMAX) is assigned to the device by the FRR command (see Figs. 4-3 to 4-7), or set to 16 if the talk first (TF) bit is set.

Four or six bits of the Tag ID are used at a time to calculate the time slot, with TC being the shift parameter to choose which portion of the 32-bit Tag ID is used as shown in Equation 4-2.

EQUATION 4-2: EQUATION FOR TIME SLOT CALCULATION

TSMAX	Time Slot = Tag ID bit range a:b
64	{[4(TC+1)+1] modulo 32: [4 TC] modulo 32} XOR TC LSB
16	{[4(TC+1)-1] modulo 32: [4 TC] modulo 32} XOR TC LSB
1	0

Note: The exclusive-or (XOR) in the above equation in Equation 4-2. This is called "semi-inverting" that randomizes worst case tag IDs, e.g. a Tag ID of '77777777' or '00000000'. Table 4-10 shows examples of the calculation.

TABLE 4-10: EXAMPLE: TAG ID = H'825FE1A0'

TC	Relevant Tag ID		Selected Tag ID before XOR with LSB of TC		Calculated Time Slot (TS) (after XOR with LSB of TC)			
	Hexadecimal	Binary	TSMAX=16	TSMAX=64	TSMAX=16		TSMAX=64	
0	h'825FE1(A0)'	b'1010 0000'	h'0'	h'20'	h'0'	d'0'	h'20'	d'32'
1	h'825FE(1A)0'	b'0001 1010'	h'A'	h'1A'	h'5'	d'5'	h'25'	d'37'
2	h'825F(E1)A0'	b'1110 0001'	h'1'	h'21'	h'1'	d'1'	h'21'	d'33'
3	h'825(FE)1A0'	b'1111 1110'	h'E'	h'3E'	h'1'	d'1'	h'01'	d'1'
4	h'82(5F)E1A0'	b'0101 1111'	h'F'	h'1F'	h'F'	d'15'	h'1F'	d'31'
5	h'8(25)FE1A0'	b'0010 0101'	h'5'	h'25'	h'A'	d'10'	h'1A'	d'26'
6	h'(82)5FE1A0'	b'1000 0010'	h'2'	h'02'	h'2'	d'2'	h'02'	d'2'
7	h'(08)25FE1A'	b'0000 1000'	h'8'	h'08'	h'7'	d'7'	h'37'	d'55'

In Table 4-10, h'x..x' represents hexadecimal number, d'x..x' represents decimal number, and b'x..x' represents binary number.

Table 4-10 shows the calculated time slot (TS) is 5 for TC = 1 and TSMAX = 16 with Tag ID = h'825FE1A0'. This means the device waits for 12.5 ms (5 x 2.5 ms = 12.5 ms) in a non-modulating condition between the end of FRR and the start of the FR response.

Also the TS is 37 for TC = 1 and TSMAX = 64. This means the device waits for 92.5 ms (37 x 2.5 ms = 92.5 ms) between the end of FRR and the start of the FR response in a non-modulating condition.

4.2.5 TIME SLOT COUNTER

This section generates the sleep time (2.5 ms x TS) of the device. During the sleep time, the device remains in a non-modulating condition.

5.0 MEMORY SECTION

The memory section is organized into two groups: (1) Main Memory Section and (2) Stored CRC Memory Section.

5.1 Main Memory Section

The main section is organized into 32 blocks as shown in Table 5-1. Each block has 32 bits. The first 3 blocks (0 - 2) are used for predefined parameters and device operation. The next three blocks (3 - 5) are used as the fast read fields. The blocks from 6 to 31 (26 blocks) are used for user data memory. The memory is read or written in 32-bit selectable units, with the exception of the fast read (FR) bit and the talk first (TF) bit, which are individually selectable.

5.2 Stored CRC (SCRC) Memory Section

This memory section is used to store the CRC of the main memory section, and organized into 32 blocks. Each block has 16 bits. Each block contains the CRC in the corresponding block of the main memory section. The stored CRC (SCRC) corresponds to the interrogator command (write 32-bit block) and data.

TABLE 5-1: MEMORY ORGANIZATION

Main Memory Section (32 blocks x 32 bits)	Stored CRC (SCRC) Section (32 blocks x 16 bits)	Comments
MSB ... LSB	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
FR | TF | Tag Parameters | FR Response CRC		Block 0 (Tag Parameters/FR)
SNR 3 | SNR 2 | SNR 1 | SNR 0		Block 1 (Tag ID = Serial Number)
31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0		Block 2 (Write-Protect 1st kb)
Fast | Read | Field | (LS Block)		Block 3 (FR Field Least Significant Block)
		Block 4 (FR Field)
Fast | Read | Field | (MS Block)		Block 5 (FR Field Most Significant Block)
		Block 6 (User Data)
		Block 7 (User Data)
		Block 8 (User Data)
		Block 9 (User Data)
		Block 10 (User Data)
		Block 11 (User Data)
. . . . .	. . . . .	. . . . .
		Block 29 (User Data)
		Block 30 (User Data)
		Block 31 (User Data)

5.3 BIT LAYOUT

5.3.1 BLOCK 0

The bit layout in block 0 is given in the following table. FR and TF bits are not write-protectable.

TABLE 5-2: BIT LAYOUT OF BLOCK 0

B0:31	B0:30	B0:29	B0:28	B0:27	B0:26	B0:25	B0:24
FR	TF	TFT1	TFT0	DF1	DF0	MT1*	MT0*
B0:23	B0:22	B0:21	B0:20	B0:19	B0:18	B0:17	B0:16
TM2*	TM1*	TM0*					
B0:15	B0:14	B0:13	B0:12	B0:11	B0:10	B0:9	B0:8
FRR CRC 15	FRR CRC 14	FRR CRC 13	FRR CRC 12	FRR CRC 11	FRR CRC 10	FRR CRC 9	FRR CRC 8
B0:7	B0:6	B0:5	B0:4	B0:3	B0:2	B0:1	B0:0
FRR CRC 7	FRR CRC 6	FRR CRC 5	FRR CRC 4	FRR CRC 3	FRR CRC 2	FRR CRC 1	FRR CRC 0

Note: * These are 'hardwired' bits, not EEPROM bits.

5.3.1.1 DESCRIPTION OF BITS

TABLE 5-3: FR BIT (B0:31)

FR	Answer to Fast Read Request signal
1	Yes (e.g. "Item" is unpaid in retail EAS applications)
0	No (e.g. "Item" has been purchased in retail EAS applications)

Note: FR bit is not write-protectable.

TABLE 5-4: TF BIT (B0:30)

TF	Talk first
0	Wait for FRR command
1	Send Fast Read Response without waiting for FRR command

Note: TF bit is not write-protectable.

TABLE 5-5: TFT BITS (B0:29 - B0:28)

TFT1	TFT0	Talk First TCMAX [1]
0	0	1
0	1	2
1	0	4
1	1	Never Elapses (Default) [2]

Note 1: Only applicable in tag talks first (TTF) mode. If FRR, TCMAX in command applies. Maximum time slot (TSMAX) parameter is set to 64 for TTF mode.

2: The device continuously sends its FR response until it receives its correct matching code. On average, the device will send its FR response every 80 ms.

TABLE 5-6: DF BITS (B0:27 - B0:26)

DF1	DF0	FR Data Field Length
0	0	32 bits (Default)
0	1	48 bits
1	0	64 bits
1	1	96 bits

TABLE 5-7: MT BITS (B0:25 - B0:24)

MT1	MT0	Memory type
0	0	Single level EEPROM (Default)
0	1	Reserved for future uses (e.g.; multi level EEPROM)
1	0	Reserved for future uses (e.g.; FRAM)
1	1	Reserved for future uses

Note: The MT bits are "hardwired".

TABLE 5-8: TM BITS (B0:23 - B0:21)

TM2	TM1	TM0	Total memory size
0	0	0	512 bits
0	0	1	1 Kbit (Default)
0	1	0	TBD
0	1	1	TBD
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

Note: The TM bits are “hardwired”.

TABLE 5-9: B0: (20-16) AND B0: (15-0)

B0:(20-16)	Available for user
B0:(15-0)	CRC for the Fast Read Response

5.3.2 BLOCK 1: UNIQUE 32-BIT TAG ID

Block 1 contains 32 bits of unique Tag ID with stored CRC (SCRC). The ID is uniquely serialized.

5.3.3 BLOCK 2: WRITE-PROTECT FOR THE FIRST KBITS

Each bit corresponds to a 32-bit block, i.e. bit 0 to block 0, bit 1 to block 1, etc. Write-protection is a one way process, i.e. once a block is write-protected, it cannot be modified. It should be noted that the write-protect block itself can be write-protected. TF and FR bits in block 0 are not write-protectable even if the write-protection bit in the block is set.

TABLE 5-10: WRITE-PROTECT

Block X Write Status	Bit X of Write-Protect Block
Block X writable	1
Block X write-protected	0

5.3.4 BLOCKS 3-5: FAST READ FIELDS

These blocks contain data bits for the FR response. The state of the DF bits (see Table 5-6) in block 0 determines the actual number of bits to be sent. This block can be used as a customer ID or also as additional tag ID numbers.

6.0 DEVICE TESTING

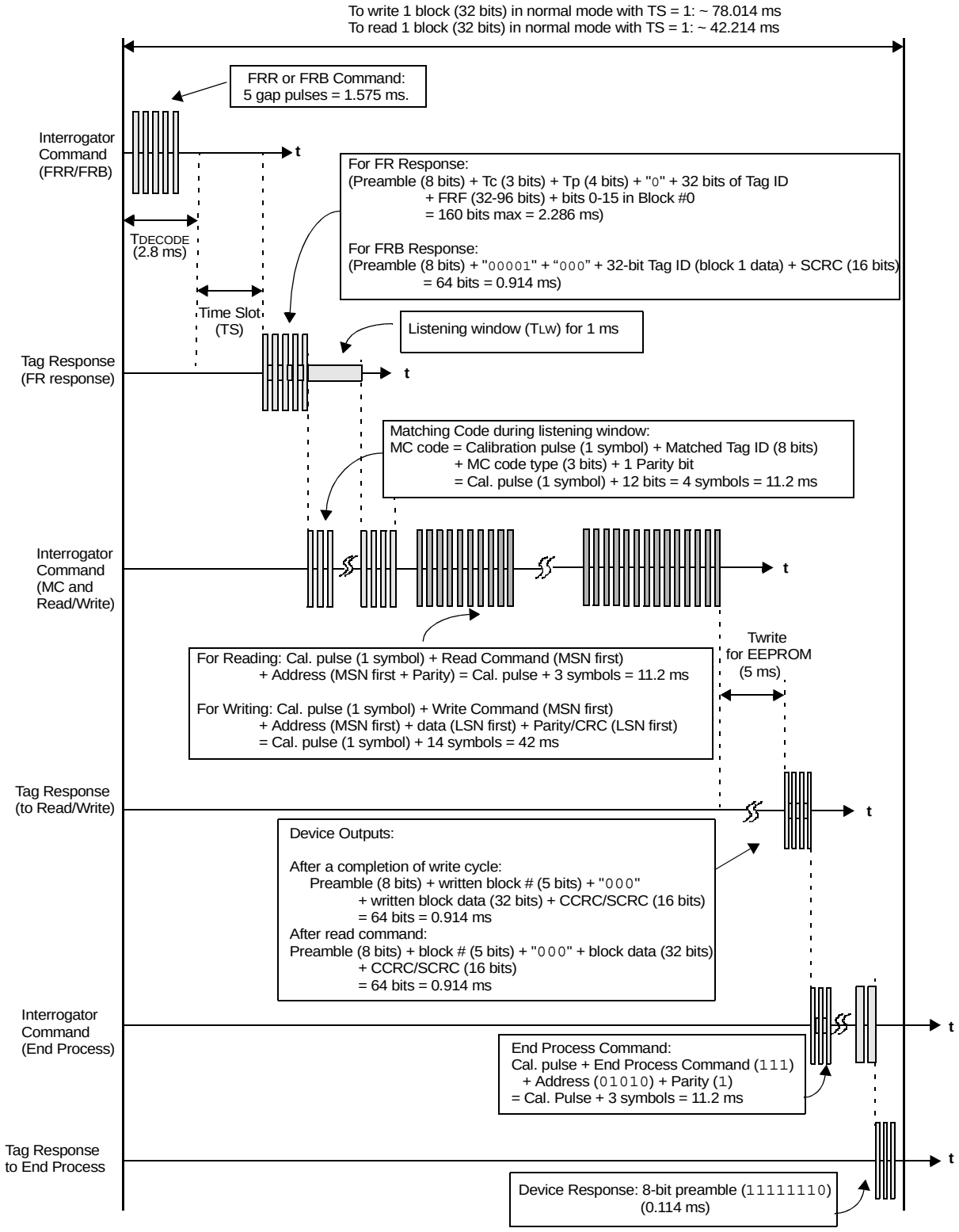
The device will be shipped to customers with the Fast Read (FR) bit set, and with block 1 write-protected.

The following bits are factory programmed prior to shipping:

1. DF0(B0:26) and DF1(B0:27) are set to “0”.
2. TFT0(B0:28) and TFT1(B0:29) bits are set to “1”.
3. All bits in the FR field (blocks 3-5) are programmed to “1”s.
4. The FRR_CRC(B0:0 - B0:15) bits are also programmed according to the Tag ID and item (3) above.

7.0 EXAMPLES

EXAMPLE 7-1: READ/WRITE PULSE SEQUENCE



EXAMPLE 7-2: CALCULATION OF MATCHING CODE FOR TAG ID = 825FE1A0 (HEX, MSB FIRST)

The “match” part of the matching code is calculated by the Bit-Wise Equation in Equation 4-1:

“Match (8 bits)” = Tag ID bit range a:b = {4(TC)}modulo 32: {4(TC + 1) + 3}modulo 32

For TC = 2, the above equation gives a = 8, and b = 15.

The “Match (8 bits)” is chosen from (8th 9th 10th 11th) and (12th 13th 14th 15th) bits of the Tag ID.

Therefore, for the Tag ID = 825FE1A0 (hex) = b/1000 0010 0101 1111 1110 0001 1010 0000/,

“Match (8 bits)” = b/1110 0001/ = 1E (hex).

Using this “Match” part, a complete set of matching code is assembled as:

1E5 for MC1, and

1E9 for MC2

where: 5 in the MC1 was from b/0101/ (010 for MC1 and the last “1” is a parity bit),
and 9 in the MC2 was from b/1001/ (100 for MC2 and the last “1” is a parity bit).

Gap position in the 1-of-16 PPM signal for the calculated MC codes:

The gap position numbers in the 1-of-16 PPM for the calculated MC codes are (see Figure 4-9 for 1-of-16 PPM):

Positions 1, 14, and 5 for 1E5 for MC1 code

Positions 1, 14, and 9 for 1E9 for MC2 code.

The “Match” part of the matching code for various TCs are given in Table 7-1.

TABLE 7-1: CALCULATED “MATCH” FOR TAG ID = 825FE1A0 (HEX)

TC	“Match (8 bits) in hex”
0	0A
1	A1
2	1E
3	EF
4	F5
5	52
6	28
7	80

EXAMPLE 7-3: TO WRITE DATA INTO THE DEVICE

The interrogator command structure for writing (see Section 4.2.1) is:

Calibration pulse + Writing Command (MSN first) + Address (MSN first) + Data (LSN first) + Parity/CRC (LSN first)

If the interrogator wants to write data “0123cdef (Hex, MSB to LSB)” to block 5, the following message will be sent:

Calibration pulse + Write Command (MSN first) + Address (MSN first) + Data (LSN first) + Parity/CRC (LSN first)

= 101 (write command) + 00101 (address) + f e d c 3 2 1 0 (data, hex) + CRC

= Calibration pulse + a 5 f e d c 3 2 1 0 6 0 2 e (hex string)

The hex string above is encoded with the 1-of-16 PPM signals. See Figure 4-10 for the 1-of-16 PPM representation of hex values.

Referring to Figure 4-10, the gap positions in the 1-of-16 PPM for the above hex string are:

Positions 10 (a), 5 (5), 15 (f), 14 (e), 13 (d), 12 (c), 3 (3), 2 (2), 1 (1), 0 (0), 6 (6), 0 (0), 2 (2), e (14).

EXAMPLE 7-4: TO READ DATA FROM THE DEVICE

To read the content of block 5 that has been programmed in the previous example, the interrogator sends the following command:

Calibration pulse + Read Command (110) + Address (00101) + Parity (0)

= Calibration pulse + C50 (hex)

The gap positions in the 1-of-16 PPM signal for the above hex string are:

12 (C), 5 (5), 0 (0).

Device Response:

When the device receives the above interrogator command, the device outputs the following 70 kHz Manchester encoded data string (see Section 4.2.2 for the structure of device response):

Preamble (8 bits) + Block number (5 bits, LSB first) + ‘000’ + Block Data (32 bits, LSB first) + SCRC (16 bits)
= 1-1-1-1-1-1-1-0 (f7) + 1-0-1-0-0-0-0-0 (5 0) + 1-1-1-1 0-1-1-1 1-0-1-1... 1-0-0-0 0-0-0-0 (f e d c 3 2 1 0) + 0-1-1-0 0-0-0-0 0-1-0-0 0-1-1-1 (602e).

EXAMPLE 7-5: TO SEND THE “END PROCESS” COMMAND

The interrogator command structure (see Section 4.2) for the End Process is:

Calibration pulse + End Process Command (111) + Address (01010) + Parity (1) = Calibration pulse + EA1 (hex)

The gap positions in the 1-of-16 PPM signal for the above hex string are:

14 (E), 10 (A), 1 (1).

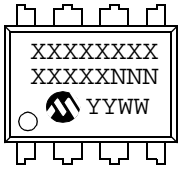
Device Response:

The device outputs the 8-bit preamble (“11111110”) when it receives the End Process command, and enters the Sleeping Loop.

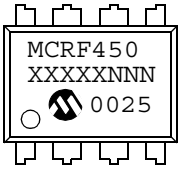
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

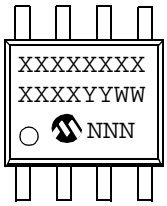
8-Lead PDIP (300 mil)



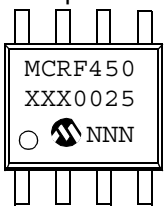
Example:



8-Lead SOIC (150 mil)



Example:

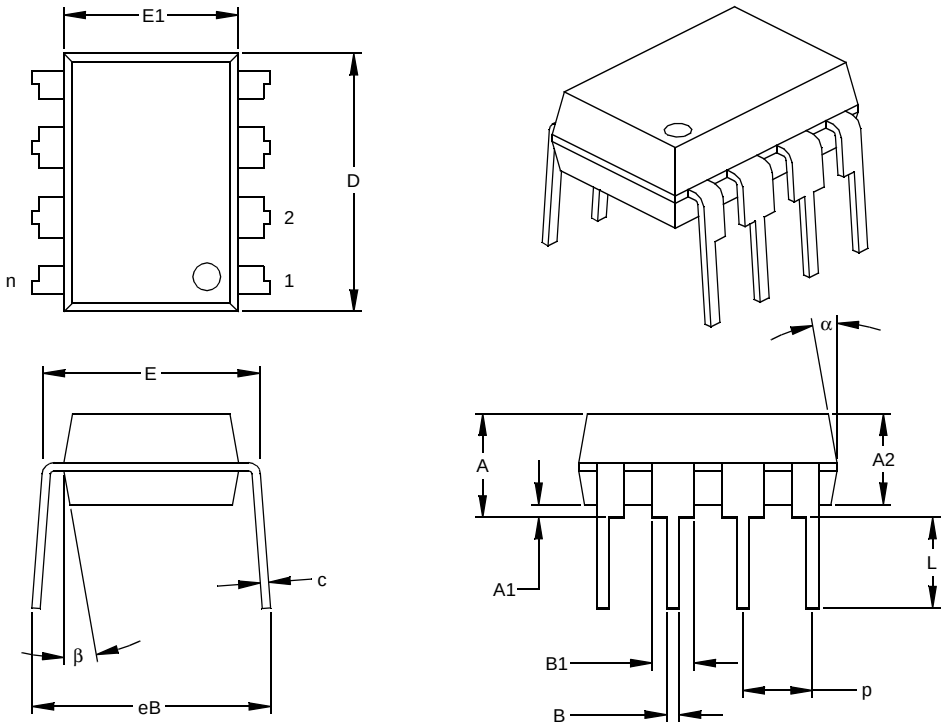


Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard device marking consists of Microchip part number, year code, week code, and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

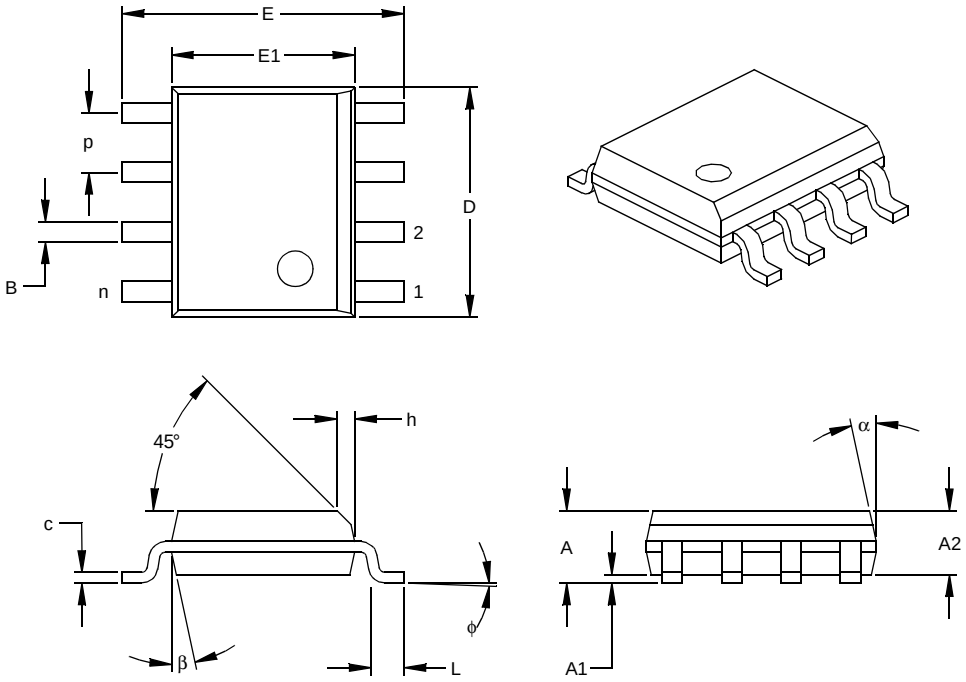


UNITS		INCHES*			MILLIMETERS		
DIMENSION LIMITS		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



UNITS		INCHES*			MILLIMETERS		
DIMENSION LIMITS		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	.10	.18	.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	.25	.38	.51
Foot Length	L	.019	.025	.030	.48	.62	.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	.20	.23	.25
Lead Width	B	.013	.017	.020	.33	.42	.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-7578.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager Total Pages Sent

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: **MCRF450/451/452/455** Literature Number: **DS40232C**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

MCRF450/451/452/455 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

MCRF450/451/452/455 **/X**

Package:	WF	=	Sawed 8” wafer on frame (8 mil backgrind)
	WFB	=	Bumped, sawed 8” wafer on frame (11 mil backgrind)
	W	=	8” wafer (11 mil backgrind)
	WB	=	Bumped 8” wafer (11 mil backgrind)
	S	=	Dice in waffle pack (11 mil backgrind)
	SB	=	Bumped die in waffle pack (11 mil backgrind)
	SN	=	SOIC, 8-lead, 300 mil body
	P	=	PDIP, 8-lead, 150 mil body
Device:	MCRF450/451/452/455	=	13.56 MHz Read/Write Anti-collision device

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see last page)
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip’s Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

AN752

CRC Algorithm for MCRF45X Read/Write Device

Author: Youbok Lee, Ph.D.
Microchip Technology Inc.

INTRODUCTION

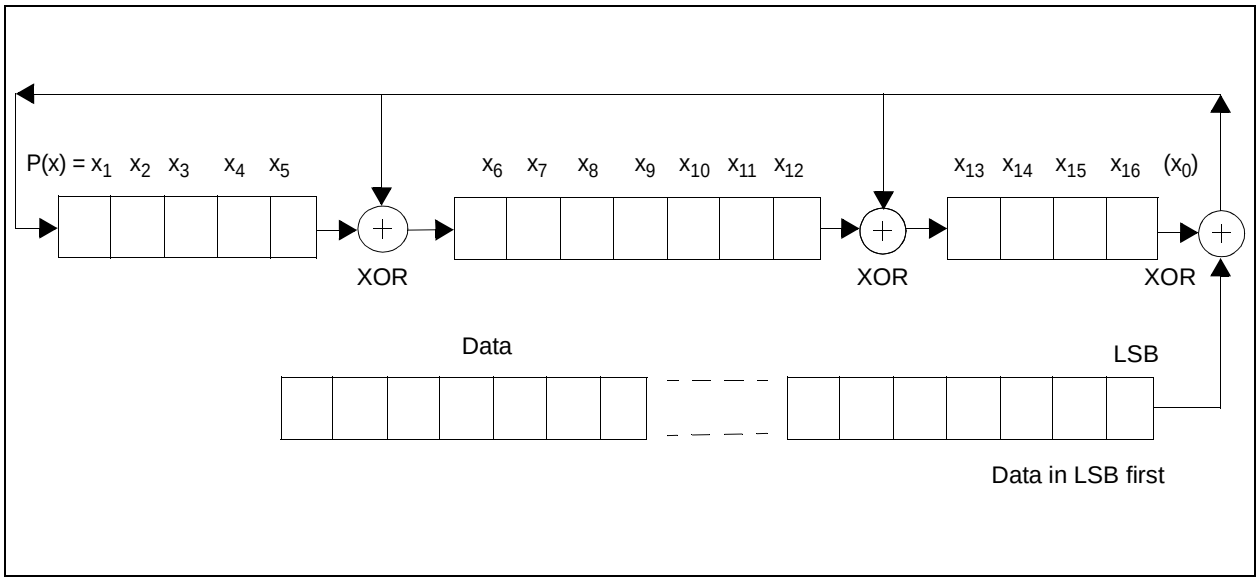
The 13.56 MHz read/write devices (MCRF4XX) use a 16-bit Cyclic Redundancy Code (CRC) to ensure the integrity of data. Its polynomial and initial values are:

CRC Polynomial: $X^0+X^5+X^{12}+X^{16}$ = 1000-0100-0000-1000-(1) = 8408 (hex)

Initial Value: $FFFF

This polynomial is also known as CRC CCITT-16. The interrogator applies the same polynomial to the incoming and transmitting data.

FIGURE 1: CCITT-16 CRC ENCODER



COMPUTATION ALGORITHM

Figure 1 shows the CCITT-16 CRC encoder. Figure 2 is the computational flow chart for computer programming.

The encoder consists of 16 shift registers and 3 exclusive-OR gates. The registers start with 1111-1111-1111-1111 (or FFFF in hex). The encoder performs XOR and shifts its content until the last bit is entered. The final register's content after the last data bit is the calculated CRC value of the data set.

Example: The following procedure shows a workout example of the CRC calculation using the encoder.

Data: 8552F189 (hex): 0001-1010-1010-0100-1111-1000-1001 (binary, LSB first for each nibble).

Table 1 shows each step of the calculation. The content of the register after the last bit is 07F1. This 07F1 is the calculated CRC of the data.

When transmitting data, this calculated CRC is attached to the data. The interrogator sends the data and CRC with LSN (Least Significant Nibble) first. Therefore, the hex string to be sent will be: 981F25581F70 and for data = 8552F189.

FIGURE 2: FLOW-CHART OF CRC COMPUTATION

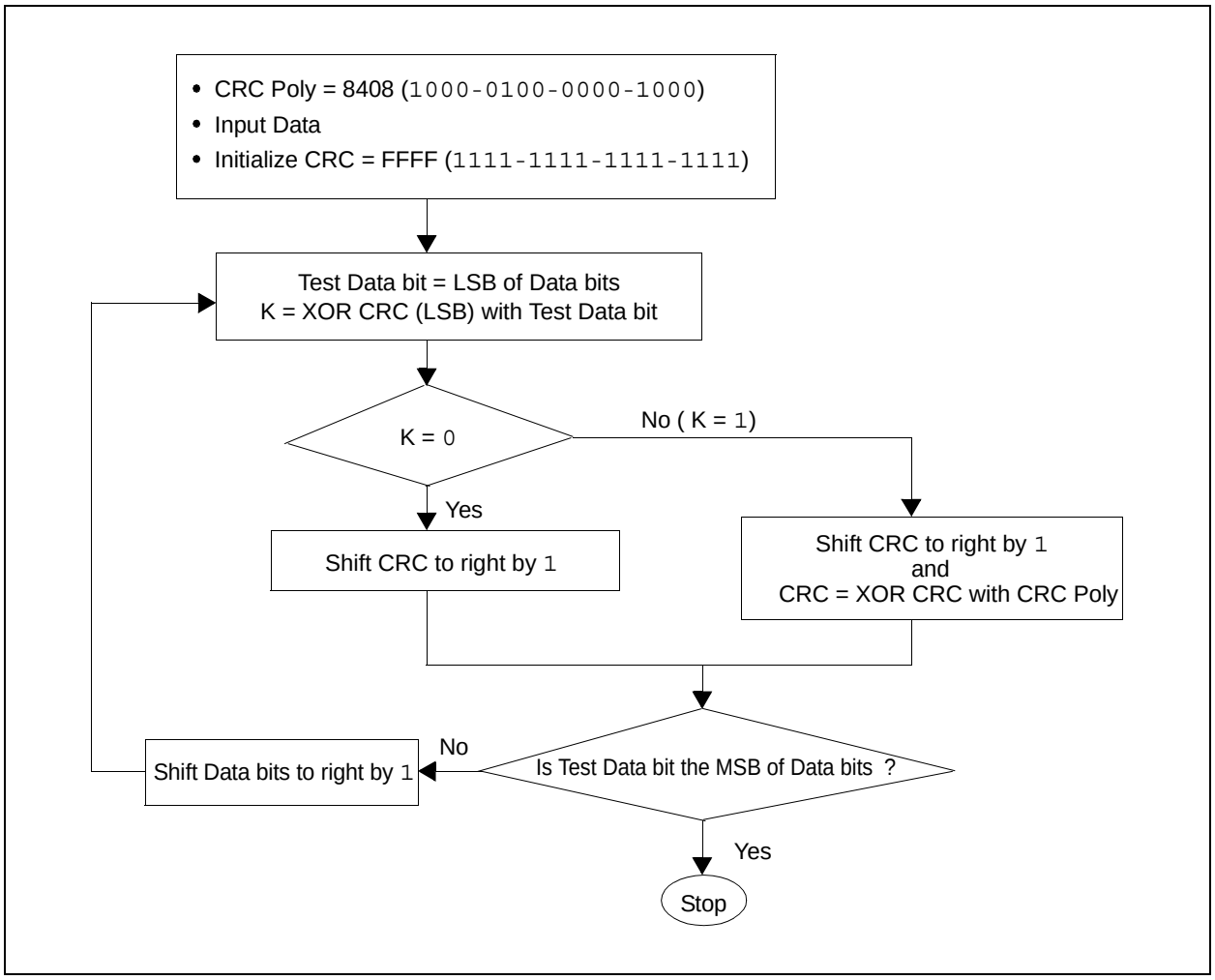


TABLE 1: CRC WORKOUT EXAMPLE FOR DATA = 8552F189 (HEX)

Bit No.	Input Data	Register Contents																	Hex Value
		X_1	X_2	X_3	X_4	X_5	-	X_6	X_7	X_8	X_9	X_{10}	X_{11}	X_{12}	-	X_{13}	X_{14}	X_{15}	X_{16}	
Initial		1	1	1	1	1	-	1	1	1	1	1	1	1	-	1	1	1	1	FFFF
1	0	1	1	1	1	1	-	0	1	1	1	1	1	1	-	0	1	1	1	FBF7
2	0	1	1	1	1	1	-	0	0	1	1	1	1	1	-	0	0	1	1	F9F3
3	0	1	1	1	1	1	-	0	0	0	1	1	1	1	-	0	0	0	1	F8F1
4	1	0	1	1	1	1	-	1	0	0	0	1	1	1	-	1	0	0	0	7C78
5	1	1	0	1	1	1	-	0	1	0	0	0	1	1	-	0	1	0	0	BA34
6	0	0	1	0	1	1	-	1	0	1	0	0	0	1	-	1	0	1	0	5D1A
7	1	1	0	1	0	1	-	0	1	0	1	0	0	0	-	0	1	0	1	AA85
8	0	1	1	0	1	0	-	0	0	1	0	1	0	0	-	1	0	1	0	D14A
9	1	1	1	1	0	1	-	1	0	0	1	0	1	0	-	1	1	0	1	ECAD
10	0	1	1	1	1	0	-	0	1	0	0	1	0	1	-	1	1	1	0	F25E
11	1	1	1	1	1	1	-	1	0	1	0	0	1	0	-	0	1	1	1	FD27
12	0	1	1	1	1	1	-	0	1	0	1	0	0	1	-	1	0	1	1	FA9B
13	0	1	1	1	1	1	-	0	0	1	0	1	0	0	-	0	1	0	1	F945
14	1	0	1	1	1	1	-	1	0	0	1	0	1	0	-	0	0	1	0	7CA2
15	1	0	0	1	1	1	-	1	1	0	0	1	0	1	-	0	0	0	1	3E51
16	0	1	0	0	1	1	-	0	1	1	0	0	1	0	-	0	0	0	0	9B20
17	1	1	1	0	0	1	-	0	0	1	1	0	0	1	-	1	0	0	0	C998
18	1	1	1	1	0	0	-	0	0	0	1	1	0	0	-	0	1	0	0	E0C4
19	1	1	1	1	1	0	-	1	0	0	0	1	1	0	-	1	0	1	0	F46A
20	1	1	1	1	1	1	-	1	1	0	0	0	1	1	-	1	1	0	1	FE3D
21	1	0	1	1	1	1	-	1	1	1	0	0	0	1	-	1	1	1	0	7F1E
22	0	0	0	1	1	1	-	1	1	1	1	0	0	0	-	1	1	1	1	3F8F
23	0	1	0	0	1	1	-	0	1	1	1	1	0	0	-	1	1	1	1	9BCF
24	0	1	1	0	0	1	-	0	0	1	1	1	1	0	-	1	1	1	1	C9EF
25	0	1	1	1	0	0	-	0	0	0	1	1	1	1	-	1	1	1	1	E0FF
26	0	1	1	1	1	0	-	1	0	0	0	1	1	1	-	0	1	1	1	F477
27	0	1	1	1	1	1	-	1	1	0	0	0	1	1	-	0	0	1	1	FE33
28	1	0	1	1	1	1	-	1	1	1	0	0	0	1	-	1	0	0	1	7F19
29	1	0	0	1	1	1	-	1	1	1	1	0	0	0	-	1	1	0	0	3F8C
30	0	0	0	0	1	1	-	1	1	1	1	1	0	0	-	0	1	1	0	1FC6
31	0	0	0	0	0	1	-	1	1	1	1	1	1	0	-	0	0	1	1	0FE3
32	1	0	0	0	0	0	-	1	1	1	1	1	1	1	-	0	0	0	1	**07F1 (CRC Value)**

APPENDIX A: EXAMPLE WITH C-SOURCE CODE FOR CRC CALCULATION

```
# include  <stdio.h>
# include <stdlib.h>
# include "onescnt.h"
# define NULL 0
# define true 1
# define false 0
void main (int argc, char *argv[ ])
{
int i, j, k, message[40], num_bits, bitcount, bytecount, crc, next_bit, crc_temp, message_temp;
int maskreg[8] = {1, 2, 4, 8, 16, 32, 64, 128};
int crc_nibble[4];
char ch
FILE *fin;
if (argc != 2)
{ printf ("proper usage is CCITT {indata file with data in hex}\n"); abort (); }
if ( (fin =fopen(argv[1], "r")) ==NULL)
                {printf("Can't open %s\n", argv[1]; abort();}
i = 0;
while ( (ch=fgetc(fin)) !=EOF)
{
message_temp = 0;
//retrieve the input data field and convert to an integer message field
if ((ch >= 'a') && (ch <= 'f')) ch = ch - 0x20
if ((ch >= 'A') && (ch <= 'F')) ch = ch - 0x70
if ((ch >= '0') && (ch <= '?'))
{
message_temp = ch - '0';
 message[i++] = message_temp;
}
}
// At this point, message[ ] holds data with nibbles (4 bits on each array). This will be used for
CRC calculation
message[ i ] = -1;
k = i
// The above is used for array checking and k value is the total number of nibbles.
printf ("Read in %d nibbles. \n", k);
printf ("Original data in hex read in from data file: \n");
 for (i = 0; i < k; i++)
printf("%x ", message[ i ]);
printf("\n\n");

// Now computing the CRC of data
//----------- Initialization ------------------------------
crc = 0xffff; //initial CRC value
crc_poly = 0x8408; //1000-0100-0000-1000
//-------------------------------------------------------
printf ("Initial  CRC value in hex: %x ... \n", crc);
num_bits = k*4;
for ( i = 0; i < num_bits; i++)
{
bitcount = i % 4;
bytecount = i/4;
next_bit = (message[bytecount] & maskreg[bitcount]); //This will find the next data bit to apply
next_bit = ((next_bit >> bitcount) & 1); //This will move the current data bit to LSB of next_bit
// and make all bits except LSB bit to zero
crc_temp = crc^next_bit; //xor the last nibble of crc (actually the last bit of CRC) with next_bit
if (crc_temp & 1)
{
printf ("xor = 1\n");
crc = crc >> 1; //Shift the crc by 1 to right
crc = crc^crc_poly ; //xor current crc with crc_poly
```

```
crc = crc|0x8000; //this may not be necessary
}
// if it is zero, just shift crc by 1
if (!(crc_temp &1))
{
printf ("xor = 0\n");
crc = crc >> 1;
crc = crc & 0x7fff;// this may not be necessary
}
printf("Temp CRC after iteration %d: ", i);
for (j = i; j<num_bits; j++)
printf("  ");
}
printf("%d\n", crc);
}
crc_nibble [0] = crc & x000f;
crc_nibble [1] = (crc & x000f >> 4;
crc_nibble [2] = (crc & x000f >> 8;
crc_nibble [3] = (crc & x000f >> 12;
printf("Bit order for shifting in nibbles in LSB first. \n");
printf ("\n CRC at end: %x  ", crc);
printf ("Send %x %x %x %x \n", crc_nibble[0], crc_nibble[1],crc_nibble[2],crc_nibble[3],);
printf("\n\n");
fclose(fin);
}
```

NOTES:

AN707

MCRF 355/360 Application Note: Mode of Operation and External Resonant Circuit

Author: Youbok Lee, Ph.D.
Microchip Technology Inc.

INTRODUCTION

The MCRF355 passive RFID device is designed for low cost, multiple reading, and various high volume tagging applications using a frequency band of 13.56 MHz. The device has a total of 154 memory bits that can be reprogrammed by a contact programmer. The device operates with a 70 kHz data rate, and asynchronously with respect to the reader's carrier. The device turns on when the coil voltage reaches 4 V_{PP} and outputs data with a Manchester format (see Figure 2-3 in the data sheet). With the given data rate (70 kHz), it takes about 2.2 ms to transmit all 154 bits of the data. After transmitting all data, the device goes into a sleep mode for 100 ms +/- 50%.

The MCRF355 needs only an external parallel LC resonant circuit that consists of an antenna coil and a capacitor for operation. The external LC components must be connected between antenna A, B, and ground pads. The circuit formed between Antenna Pad A and the ground pad must be tuned to the operating frequency of the reader antenna.

MODE OF OPERATION

The device transmits data by tuning and detuning the resonant frequency of the external circuit. This process is accomplished by using an internal modulation gate (CMOS), that has a very low turn-on resistance (2 ~ 4 ohms) between Drain and Source. This gate turns on during a logic "High" period of the modulation signal and off otherwise. When the gate turns on, its low turn-on resistance shorts the external circuit between Antenna Pad B and the ground pad. Therefore, the resonant frequency of the circuit changes. This is called *detuned* or *cloaking.* Since the detuned tag is out of the frequency band of the reader, the reader can't see it.

The modulation gate turns off as the modulation signal goes to a logic "Low." This turn-off condition again tunes the resonant circuit to the frequency of the reader antenna. Therefore the reader sees the tag again. This is called *tuned* or *uncloaking.*

The tag coil induces maximum voltage during "uncloaking (tuned)" and minimum voltage during cloaking (detuned). Therefore, the cloaking and uncloaking events develop an amplitude modulation signal in the tag coil.

This amplitude modulated signal in the tag coil perturbs the voltage envelope in the reader coil. The reader coil has maximum voltage during cloaking (detuned) and minimum voltage during uncloaking (tuned). By detecting the voltage envelope, the data signal from the tag can be readily reconstructed.

Once the device transmits all 154 bits of data, it goes into "sleep mode" for about 100 ms. The tag wakes up from sleep time (100 ms) and transmits the data package for 2.2 ms and goes into sleep mode again. The device repeats the transmitting and sleep cycles as long as it is energized.

FIGURE 3: VOLTAGE ENVELOPE IN READER COIL

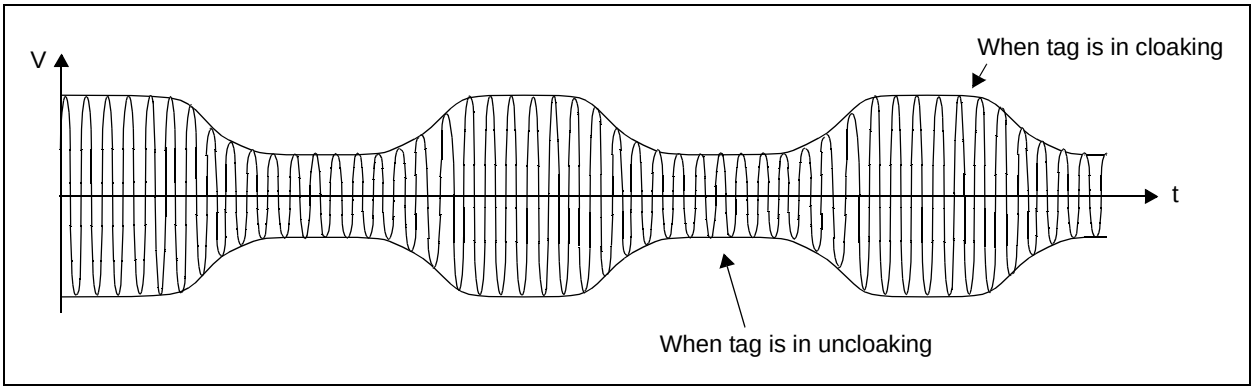
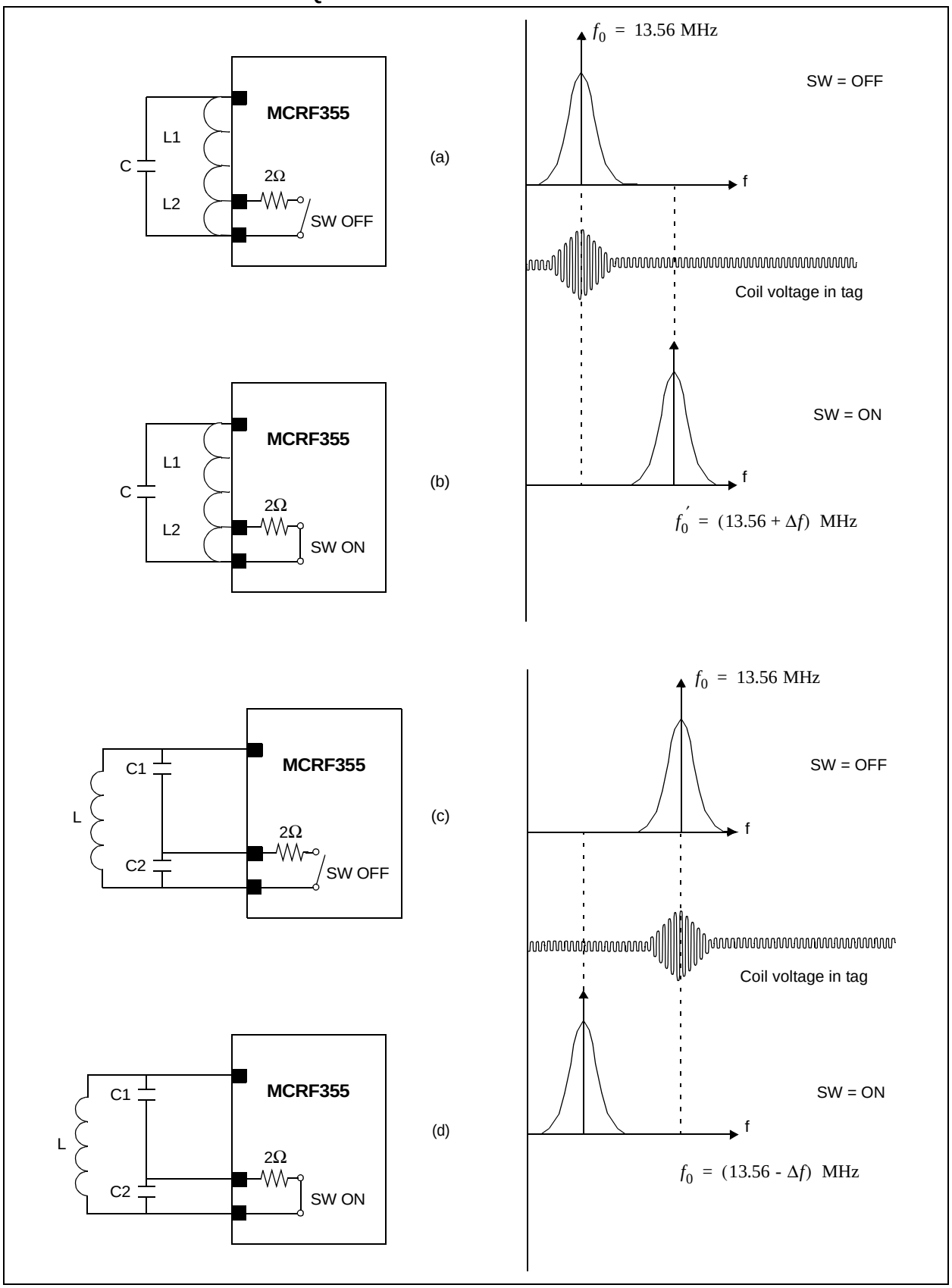


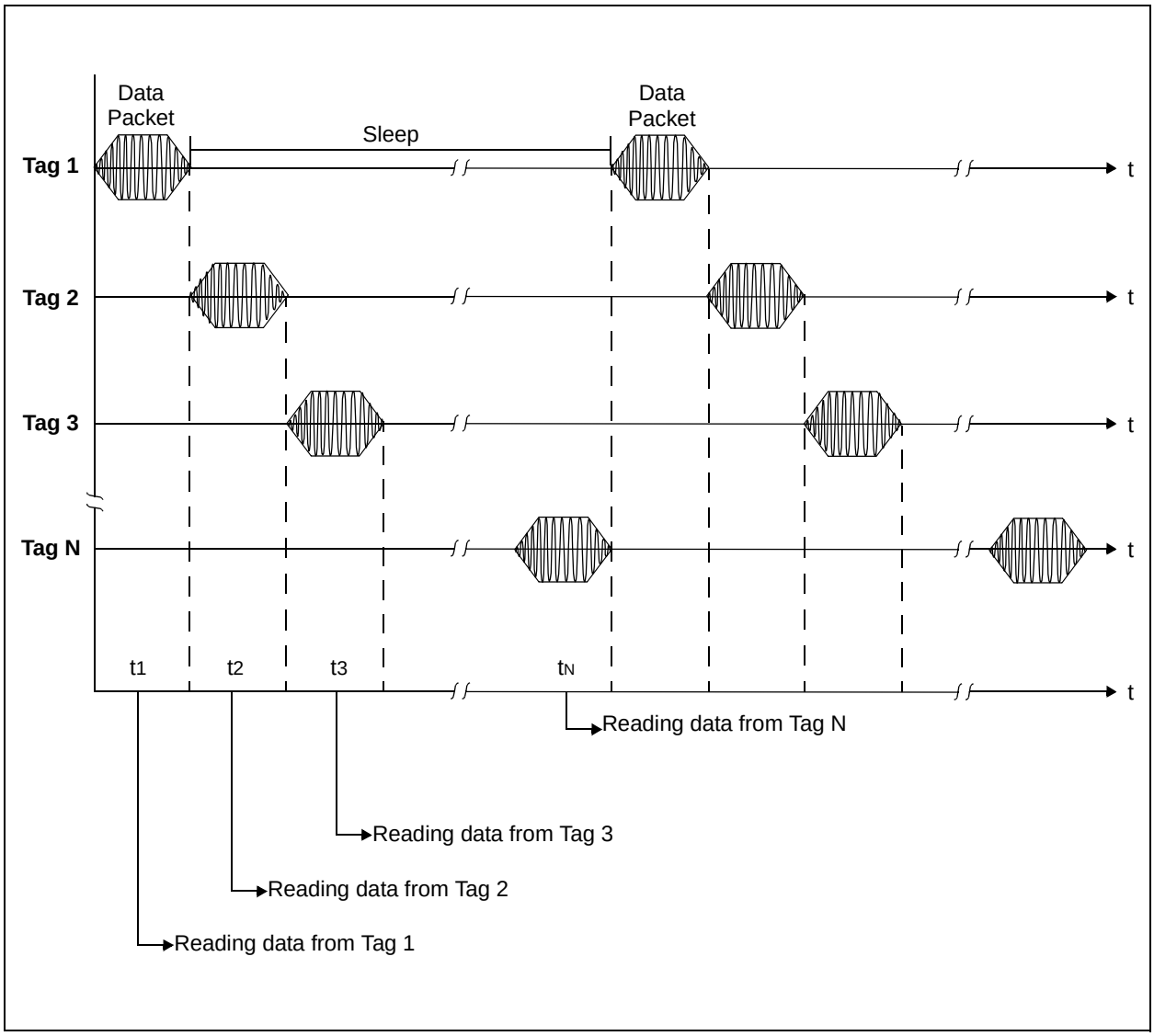
FIGURE 4: (A) UNCLOAKING (TUNED) AND (B) CLOAKING (DETUNED) MODES AND THEIR RESONANT FREQUENCIES



ANTI-COLLISION FEATURES

During sleep mode, the device remains in a cloaked state where the circuit is detuned. Therefore, the reader can't see the tag during sleep time. While one tag is in sleep mode, the reader can receive data from other tags. This enables the reader to receive clean data from many tags without any data collision. This ability to read multiple tags in the same RF field is called a*nti-collision.* Theoretically, more than 50 tags can be read in the same RF field. However, it is affected by distance from the tag to the reader, angular orientation, movement of the tags, and spacial distribution of the tags.

FIGURE 5: EXAMPLE OF READING MULTIPLE TAGS



EXTERNAL CIRCUIT CONFIGURATION

Since the device transmits data by tuning and detuning the antenna circuit, caution must be given in the external circuit configuration. For a better modulation index, the differences between the tuned and detuned frequencies must be wide enough (about 3 ~ 6 MHz).

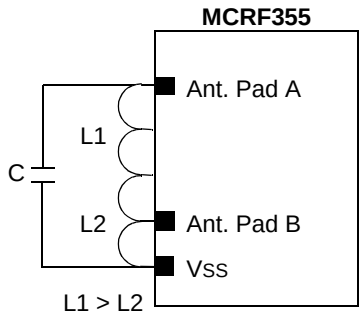
Figure 6 shows various configurations of the external circuit. The choice of the configuration must be chosen depending on the form-factor of the tag. For example, (a) is a better choice for printed circuit tags while, (b) is a better candidate for coil-wound tags. Both (a) and (b) relate to the MCRF355.

In configuration (a), the tuned resonance frequency is determined by a total capacitance and inductance from Antenna Pad A to VSS. During cloaking, the internal switch (modulation gate) shorts Antenna Pad B and VSS. Therefore, the inductance L2 is shorted out. As a result, the detuned frequency is determined by the total capacitance and inductance L1. When shorting the inductance between Antenna Pad B and VSS, the detuned (cloak) frequency is higher than the tuned (uncloak) frequency

In configuration (b), the tuned frequency (uncloak) is determined by the inductance L and the total capacitance between Antenna Pad A and VSS. The circuit detunes (cloak) when C2 is shorted. This detuned frequency (cloak) is lower than the tuned (uncloak) frequency.

The MCRF360 includes a 100 pF internal capacitor. This device needs only an external inductor for operation. The explanation on tuning and detuning is the same as for configuration (a).

FIGURE 6: VARIOUS EXTERNAL CIRCUIT CONFIGURATIONS



(a) Two inductors and one capacitor

$$f_{tuned} = \frac{1}{2\pi\sqrt{L_T C}}$$

$$f_{detuned} = \frac{1}{2\pi\sqrt{L_1 C}}$$

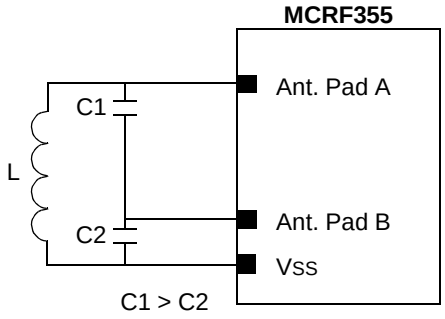
$$L_T = L_1 + L_2 + 2L_m$$

where:

L_m = mutual inductance

= $K\sqrt{L_1 L_2}$

K = coupling coefficient of two inductors $0 \le K \le 1$

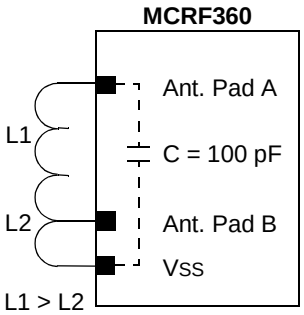


(b) Two capacitors and one inductor

$$f_{tuned} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$f_{detuned} = \frac{1}{2\pi\sqrt{LC_1}}$$

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$



(c) Two inductors with one internal capacitor

$$f_{tuned} = \frac{1}{2\pi\sqrt{L_T C}}$$

$$f_{detuned} = \frac{1}{2\pi\sqrt{L_1 C}}$$

$$L_T = L_1 + L_2 + 2L_m$$

PROGRAMMING OF DEVICE

All of the memory bits in the are reprogrammable by a contact programmer or by factory programming prior to shipment, known as Serialized Quick Turn Programming^{SM} (SQTP^{SM}). For more information about contact programming, see the *microID™ 13.56 MHz System Design Guide* (DS21299). For information about SQTP programming, please see *TB032* (DS91032), of the design guide.

AN710

Antenna Circuit Design for RFID Applications

Author: *Youbok Lee, Ph.D.*
Microchip Technology Inc.

INTRODUCTION

Passive RFID tags utilize an induced antenna coil voltage for operation. This induced AC voltage is rectified to provide a voltage source for the device. As the DC voltage reaches a certain level, the device starts operating. By providing an energizing RF signal, a reader can communicate with a remotely located device that has no external power source such as a battery. Since the energizing and communication between the reader and tag is accomplished through antenna coils, it is important that the device must be equipped with a proper antenna circuit for successful RFID applications.

An RF signal can be radiated effectively if the linear dimension of the antenna is comparable with the wavelength of the operating frequency. However, the wavelength at 13.56 MHz is 22.12 meters. Therefore, it is difficult to form a true antenna for most RFID applications. Alternatively, a small loop antenna circuit that is resonating at the frequency is used. A current flowing into the coil radiates a near-field magnetic field that falls off with r^{-3}. This type of antenna is called a *magnetic dipole antenna.*

For 13.56 MHz passive tag applications, a few microhenries of inductance and a few hundred pF of resonant capacitor are typically used. The voltage transfer between the reader and tag coils is accomplished through inductive coupling between the two coils. As in a typical transformer, where a voltage in the primary coil transfers to the secondary coil, the voltage in the reader antenna coil is transferred to the tag antenna coil and vice versa. The efficiency of the voltage transfer can be increased significantly with high *Q* circuits.

This section is written for RF coil designers and RFID system engineers. It reviews basic electromagnetic theories on antenna coils, a procedure for coil design, calculation and measurement of inductance, an antenna tuning method, and read range in RFID applications.

REVIEW OF A BASIC THEORY FOR RFID ANTENNA DESIGN

Current and Magnetic Fields

Ampere's law states that current flowing in a conductor produces a magnetic field around the conductor. The magnetic field produced by a current element, as shown in Figure 7, on a round conductor (wire) with a finite length is given by:

EQUATION 1:

$$B_\phi = \frac{\mu_o I}{4\pi r}(\cos\alpha_2 - \cos\alpha_1) \qquad (\text{Weber}/m^2)$$

where:

I = current
r = distance from the center of wire
μ_0 = permeability of free space and given as $4\pi \times 10^{-7}$ (Henry/meter)

In a special case with an infinitely long wire where:

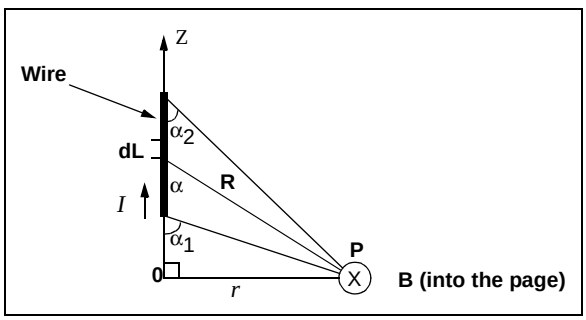
α_1 = -180°
α_2 = 0°

Equation 1 can be rewritten as:

EQUATION 2:

$$B_\phi = \frac{\mu_o I}{2\pi r} \qquad (\text{Weber}/m^2)$$

FIGURE 7: CALCULATION OF MAGNETIC FIELD B AT LOCATION P DUE TO CURRENT I ON A STRAIGHT CONDUCTING WIRE



The magnetic field produced by a circular loop antenna is given by:

EQUATION 3:

$$B_z = \frac{\mu_o I N a^2}{2(a^2 + r^2)^{3/2}}$$

$$= \frac{\mu_o I N a^2}{2} \left(\frac{1}{r^3}\right) \quad \text{for} \quad r^2 >> a^2$$

where

I = current

a = radius of loop

r = distance from the center of wire

μ_0 = permeability of free space and given as $\mu_0 = 4\pi \times 10^{-7}$ (Henry/meter)

The above equation indicates that the magnetic field strength decays with $1/r^3$. A graphical demonstration is shown in Figure 9. It has maximum amplitude in the plane of the loop and directly proportional to both the current and the number of turns, N.

Equation 3 is often used to calculate the ampere-turn requirement for read range. A few examples that calculate the ampere-turns and the field intensity necessary to power the tag will be given in the following sections.

FIGURE 8: CALCULATION OF MAGNETIC FIELD B AT LOCATION P DUE TO CURRENT I ON THE LOOP

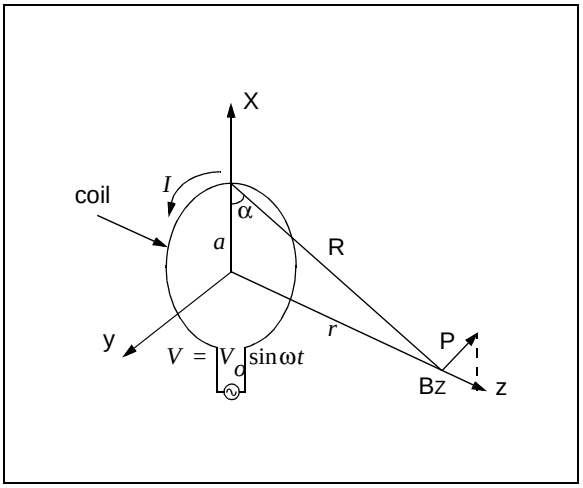
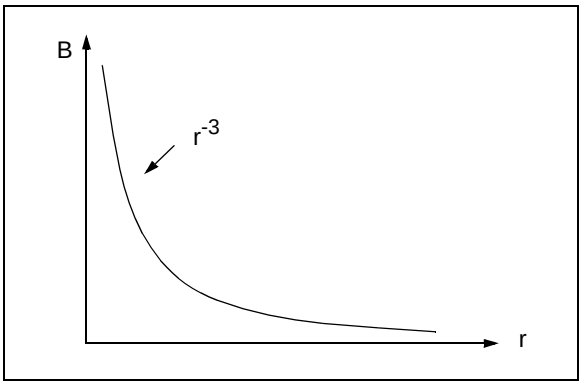


FIGURE 9: DECAYING OF THE MAGNETIC FIELD B VS. DISTANCE *r*



INDUCED VOLTAGE IN AN ANTENNA COIL

Faraday's law states that a time-varying magnetic field through a surface bounded by a closed path induces a voltage around the loop.

Figure 10 shows a simple geometry of an RFID application. When the tag and reader antennas are in close proximity, the time-varying magnetic field B that is produced by a reader antenna coil induces a voltage (called electromotive force or simply EMF) in the closed tag antenna coil. The induced voltage in the coil causes a flow of current on the coil. This is called Faraday's law. The induced voltage on the tag antenna coil is equal to the time rate of change of the magnetic flux Ψ.

EQUATION 4:

$$V = -N\frac{d\psi}{dt}$$

where:

N = number of turns in the antenna coil

Ψ = magnetic flux through each turn

The negative sign shows that the induced voltage acts in such a way as to oppose the magnetic flux producing it. This is known as Lenz's Law and it emphasizes the fact that the direction of current flow in the circuit is such that the induced magnetic field produced by the induced current will oppose the original magnetic field.

The magnetic flux Ψ in Equation 4 is the total magnetic field B that is passing through the entire surface of the antenna coil, and found by:

EQUATION 5:

$$\psi = \int B \cdot dS$$

where:

B = magnetic field given in Equation 2

S = surface area of the coil

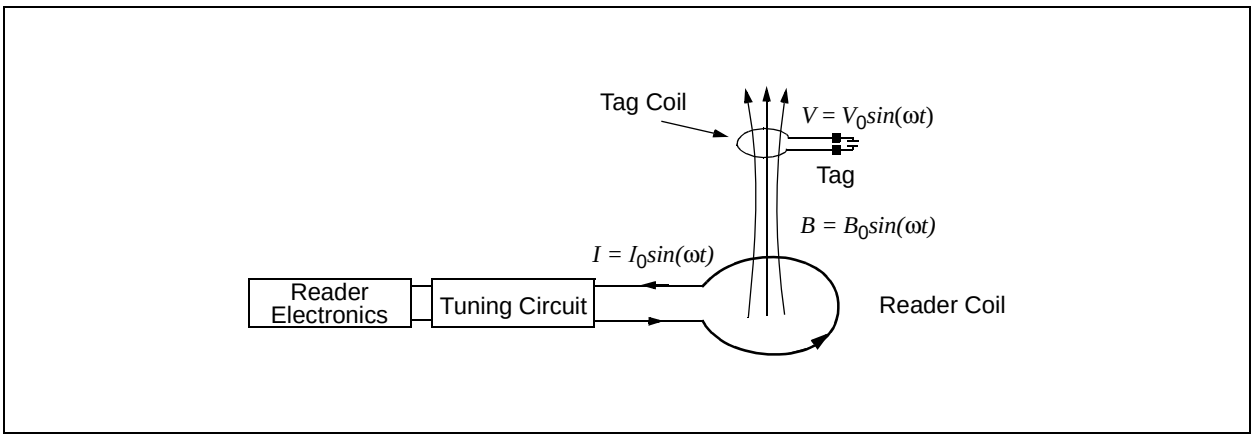
• = inner product (*cosine angle between two vectors*) of vectors B and surface area S

Note:	Both magnetic field B and surface S are vector quantities.

The presentation of inner product of two vectors in Equation 5 suggests that the total magnetic flux ψ that is passing through the antenna coil is affected by an orientation of the antenna coils. The inner product of two vectors becomes minimized when the cosine angle between the two are 90 degrees, or the two (B field and the surface of coil) are perpendicular to each other and maximized when the cosine angle is 0 degrees.

The maximum magnetic flux that is passing through the tag coil is obtained when the two coils (reader coil and tag coil) are placed in parallel with respect to each other. This condition results in maximum induced voltage in the tag coil and also maximum read range. The inner product expression in Equation 5 also can be expressed in terms of a mutual coupling between the reader and tag coils. The mutual coupling between the two coils is maximized in the above condition.

FIGURE 10: A BASIC CONFIGURATION OF READER AND TAG ANTENNAS IN RFID APPLICATIONS



Using Equations 3 and 5, Equation 4 can be rewritten as:

EQUATION 6:

$$V = - N_2 \frac{d\Psi_{21}}{dt} = - N_2 \frac{d}{dt}\left(\int B \cdot dS\right)$$

$$= - N_2 \frac{d}{dt}\left[\int \frac{\mu_o i_1 N_1 a^2}{2(a^2 + r^2)^{3/2}} \cdot dS\right]$$

$$= - \left[\frac{\mu_o N_1 N_2 a^2 (\pi b^2)}{2(a^2 + r^2)^{3/2}}\right] \frac{di_1}{dt}$$

$$= - M \frac{di_1}{dt}$$

where:

- V = voltage in the tag coil
- i_1 = current on the reader coil
- a = radius of the reader coil
- b = radius of tag coil
- r = distance between the two coils
- M = mutual inductance between the tag and reader coils, and given by:

EQUATION 7:

$$M = \left[\frac{\mu_o \pi N_1 N_2 (ab)^2}{2(a^2 + r^2)^{3/2}}\right]$$

The above equation is equivalent to a voltage transformation in typical transformer applications. The current flow in the primary coil produces a magnetic flux that causes a voltage induction at the secondary coil.

As shown in Equation 6, the tag coil voltage is largely dependent on the mutual inductance between the two coils. The mutual inductance is a function of coil geometry and the spacing between them. The induced voltage in the tag coil decreases with r^{-3}. Therefore, the read range also decreases in the same way.

From Equations 4 and 5, a generalized expression for induced voltage V_o in a tuned loop coil is given by:

EQUATION 8:

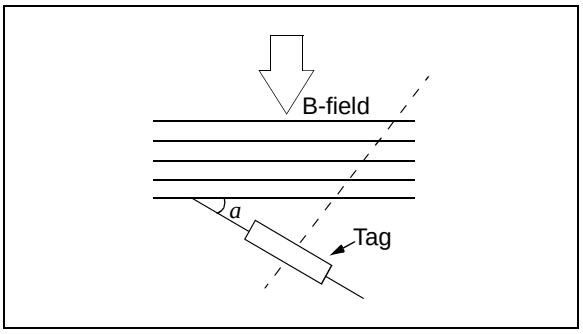
$$V_0 = 2\pi f N S Q B_o \cos\alpha$$

where:

- f = frequency of the arrival signal
- N = number of turns of coil in the loop
- S = area of the loop in square meters (m^2)
- Q = quality factor of circuit
- B_0 = strength of the arrival signal
- α = angle of arrival of the signal

In the above equation, the quality factor Q is a measure of the selectivity of the frequency of the interest. The Q will be defined in Equations 31 through 47.

FIGURE 11: ORIENTATION DEPENDENCY OF THE TAG ANTENNA



The induced voltage developed across the loop antenna coil is a function of the angle of the arrival signal. The induced voltage is maximized when the antenna coil is placed in parallel with the incoming signal where $\alpha = 0$.

EXAMPLE 2: CALCULATION OF B-FIELD IN A TAG COIL

The MCRF355 device turns on when the antenna coil develops 4 VPP across it. This voltage is rectified and the device starts to operate when it reaches 2.4 VDC. The B-field to induce a 4 VPP coil voltage with an ISO standard 7810 card size (85.6 x 54 x 0.76 mm) is calculated from the coil voltage equation using Equation 8.

EQUATION 9:

$$V_o = 2\pi fNSQB_o\cos\alpha = 4$$

and

$$B_o = \frac{4/(\sqrt{2})}{2\pi fNSQ\cos\alpha} = 0.0449 \qquad (\mu wbm^{-2})$$

where the following parameters are used in the above calculation:

Tag coil size	=	(85.6 x 54) mm^2 (ISO card size) = 0.0046224 m^2
Frequency	=	13.56 MHz
Number of turns	=	4
Q of tag antenna coil	=	40
AC coil voltage to turn on the tag	=	4 VPP
cos α	=	1 (normal direction, $\alpha = 0$).

EXAMPLE 3: NUMBER OF TURNS AND CURRENT (AMPERE-TURNS)

Assuming that the reader should provide a read range of 15 inches (38.1 cm) for the tag given in the previous example, the current and number of turns of a reader antenna coil is calculated from Equation 3:

EQUATION 10:

$$(NI)_{rms} = \frac{2B_z(a^2 + r^2)^{3/2}}{\mu a^2}$$

$$= \frac{2(0.0449 \times 10^{-6})(0.1^2 + (0.38)^2)^{3/2}}{(4\pi \times 10^{-7})(0.1^2)}$$

$$= 0.43(\text{ampere - turns})$$

The above result indicates that it needs a 430 mA for 1 turn coil, and 215 mA for 2-turn coil.

EXAMPLE 4: OPTIMUM COIL DIAMETER OF THE READER COIL

An optimum coil diameter that requires the minimum number of ampere-turns for a particular read range can be found from Equation 3 such as:

EQUATION 11:

$$NI = K\frac{(a^2 + r^2)^{\frac{3}{2}}}{a^2}$$

where: $K = \frac{2B_z}{\mu_o}$

By taking derivative with respect to the radius α,

$$\frac{d(NI)}{da} = K\frac{3/2(a^2 + r^2)^{1/2}(2a^3) - 2a(a^2 + r^2)^{3/2}}{a^4}$$

$$= K\frac{(a^2 - 2r^2)(a^2 + r^2)^{1/2}}{a^3}$$

The above equation becomes minimized when:

$$a^2 - 2r^2 = 0$$

The above result shows a relationship between the read range versus optimum coil diameter. The optimum coil diameter is found as:

EQUATION 12:

$$a = \sqrt{2}r$$

where:

a	=	radius of coil
r	=	read range.

The result indicates that the optimum loop radius, a, is 1.414 times the demanded read range r.

WIRE TYPES AND OHMIC LOSSES

Wire Size and DC Resistance

The diameter of electrical wire is expressed as the American Wire Gauge (AWG) number. The gauge number is inversely proportional to diameter, and the diameter is roughly doubled every six wire gauges. The wire with a smaller diameter has a higher DC resistance. The DC resistance for a conductor with a uniform cross-sectional area is found by:

EQUATION 13:

$$R_{DC} = \frac{l}{\sigma S} \qquad (\Omega)$$

where:

l = total length of the wire
σ = conductivity
S = cross-sectional area

Table 6 shows the diameter for bare and enamel-coated wires, and DC resistance.

AC Resistance of Wire

At DC, charge carriers are evenly distributed through the entire cross section of a wire. As the frequency increases, the reactance near the center of the wire increases. This results in higher impedance to the current density in the region. Therefore, the charge moves away from the center of the wire and towards the edge of the wire. As a result, the current density decreases in the center of the wire and increases near the edge of the wire. This is called a *skin effect*. The depth into the conductor at which the current density falls to 1/e, or 37% of its value along the surface, is known as the *skin depth* and is a function of the frequency and the permeability and conductivity of the medium. The skin depth is given by:

EQUATION 14:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

where:

f = frequency
μ = permeability of material
σ = conductivity of the material

EXAMPLE 5:

The skin depth for a copper wire at 13.56 MHz can be calculated as:

EQUATION 15:

$$\delta = \frac{1}{\sqrt{\pi f (4\pi \times 10^{-7})(5.8 \times 10^{-7})}}$$

$$= \frac{0.0179}{\sqrt{f}} \qquad (m)$$

$$= 0.187 \qquad (mm)$$

The wire resistance increases with frequency, and the resistance due to the skin depth is called an AC resistance. An approximated formula for the AC resistance is given by:

EQUATION 16:

$$R_{ac} \approx \frac{1}{2\sigma\pi\delta} = (R_{DC})\frac{a}{2\delta} \qquad (\Omega)$$

where:

a = coil radius

TABLE 6: AWG WIRE CHART

Wire Size (AWG)	Dia. in Mils (bare)	Dia. in Mils (coated)	Ohms/ 1000 ft.	Cross Section (mils)
1	289.3	—	0.126	83690
2	287.6	—	0.156	66360
3	229.4	—	0.197	52620
4	204.3	—	0.249	41740
5	181.9	—	0.313	33090
6	162.0	—	0.395	26240
7	166.3	—	0.498	20820
8	128.5	131.6	0.628	16510
9	114.4	116.3	0.793	13090
10	101.9	106.2	0.999	10380
11	90.7	93.5	1.26	8230
12	80.8	83.3	1.59	6530
13	72.0	74.1	2.00	5180
14	64.1	66.7	2.52	4110
15	57.1	59.5	3.18	3260
16	50.8	52.9	4.02	2580
17	45.3	47.2	5.05	2060
18	40.3	42.4	6.39	1620
19	35.9	37.9	8.05	1290
20	32.0	34.0	10.1	1020
21	28.5	30.2	12.8	812
22	25.3	28.0	16.2	640
23	22.6	24.2	20.3	511
24	20.1	21.6	25.7	404
25	17.9	19.3	32.4	320
26	15.9	17.2	41.0	253
27	14.2	15.4	51.4	202
28	12.6	13.8	65.3	159
29	11.3	12.3	81.2	123
30	10.0	11.0	106.0	100
31	8.9	9.9	131	79.2
32	8.0	8.8	162	64.0
33	7.1	7.9	206	50.4
34	6.3	7.0	261	39.7
35	5.6	6.3	331	31.4
36	5.0	5.7	415	25.0
37	4.5	5.1	512	20.2
38	4.0	4.5	648	16.0
39	3.5	4.0	847	12.2
40	3.1	3.5	1080	9.61
41	2.8	3.1	1320	7.84
42	2.5	2.8	1660	6.25
43	2.2	2.5	2140	4.84
44	2.0	2.3	2590	4.00
45	1.76	1.9	3350	3.10
46	1.57	1.7	4210	2.46
47	1.40	1.6	5290	1.96
48	1.24	1.4	6750	1.54
49	1.11	1.3	8420	1.23
50	0.99	1.1	10600	0.98

Note: mil = 2.54×10^{-3} cm

INDUCTANCE OF VARIOUS ANTENNA COILS

An electric current element that flows through a conductor produces a magnetic field. This time-varying magnetic field is capable of producing a flow of current through another conductor – this is called *inductance*. The inductance L depends on the physical characteristics of the conductor. A coil has more inductance than a straight wire of the same material, and a coil with more turns has more inductance than a coil with fewer turns. The inductance L of inductor is defined as the ratio of the total magnetic flux linkage to the current I through the inductor:

EQUATION 17:

$$L = \frac{N\Psi}{I} \qquad \text{(Henry)}$$

where:

N = number of turns
I = current
Ψ = the magnetic flux

For a coil with multiple turns, the inductance is greater as the spacing between turns becomes smaller. Therefore, the tag antenna coil that has to be formed in a limited space often needs a multilayer winding to reduce the number of turns.

Calculation of Inductance

Inductance of the coil can be calculated in many different ways. Some are readily available from references[1-4]. It must be remembered that for RF coils the actual resulting inductance may differ from the calculated true result because of distributed capacitance. For that reason, inductance calculations are generally used only for a starting point in the final design.

INDUCTANCE OF A STRAIGHT WOUND WIRE

The inductance of a straight wound wire shown in Figure 7 is given by:

EQUATION 18:

$$L = 0.002l\left[\log_e\frac{2l}{a} - \frac{3}{4}\right] \qquad (\mu H)$$

where:

l and a = length and radius of wire in cm, respectively.

EXAMPLE 7: INDUCTANCE CALCULATION FOR A STRAIGHT WIRE:

The inductance of a wire with 10 feet (304.8cm) long and 2 mm in diameter is calculated as follows:

EQUATION 19:

$$L = 0.002(304.8)\left[\ln\left(\frac{2(304.8)}{0.1}\right) - \frac{3}{4}\right]$$

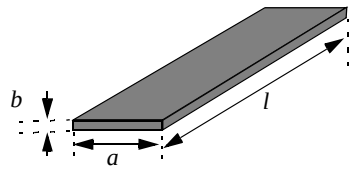
$$= 0.60967(7.965)$$

$$= 4.855(\mu H)$$

INDUCTANCE OF THIN FILM INDUCTOR WITH A RECTANGULAR CROSS SECTION

Inductance of a conductor with rectangular cross section as shown in Figure 12 is calculated as:

FIGURE 12: A STRAIGHT THIN FILM INDUCTOR



EQUATION 20:

$$L = 0.002l\left\{\ln\left(\frac{2l}{a+b}\right) + 0.50049 + \frac{a+b}{3l}\right\} \qquad (\mu H)$$

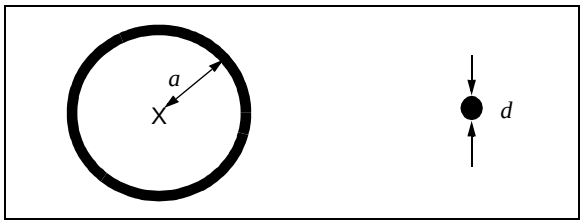
where:

a = width in cm
b = thickness in cm
l = length of conductor in cm

INDUCTANCE OF A CIRCULAR COIL WITH SINGLE TURN

The inductance of a circular coil shown in Figure 13 can be calculated by:

FIGURE 13: A CIRCULAR COIL WITH SINGLE TURN



EQUATION 21:

$$L = 0.01257(a)\left[2.303\log_{10}\left(\frac{16a}{d} - 2\right)\right] \qquad (\mu H)$$

where:

a = mean radius of loop in (cm)
d = diameter of wire in (cm)

INDUCTANCE OF AN N-TURN CIRCULAR COIL WITH SINGLE LAYER

The inductance of a circular coil with single layer is calculated as:

EQUATION 22:

$$L = \frac{(aN)^2}{22.9l + 25.4a} \qquad (\mu H)$$

where:

N = number of turns
l = length
a = the radius of coil in cm

INDUCTANCE OF N-TURN CIRCULAR COIL WITH MULTILAYER

FIGURE 14: N-TURN CIRCULAR COIL WITH SINGLE LAYER

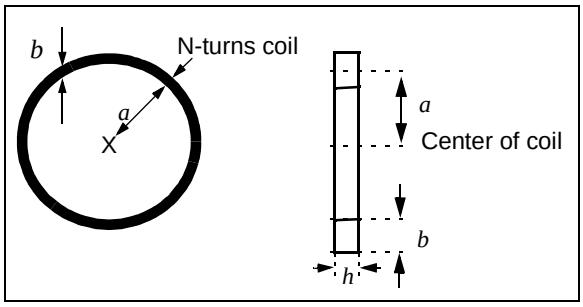


Figure 14 shows an N-turn inductor of circular coil with multilayer. Its inductance is calculated by:

EQUATION 23:

$$L = \frac{0.31(aN)^2}{6a + 9h + 10b} \qquad (\mu H)$$

where:

a = average radius of the coil in cm
N = number of turns
b = winding thickness in cm
h = winding height in cm

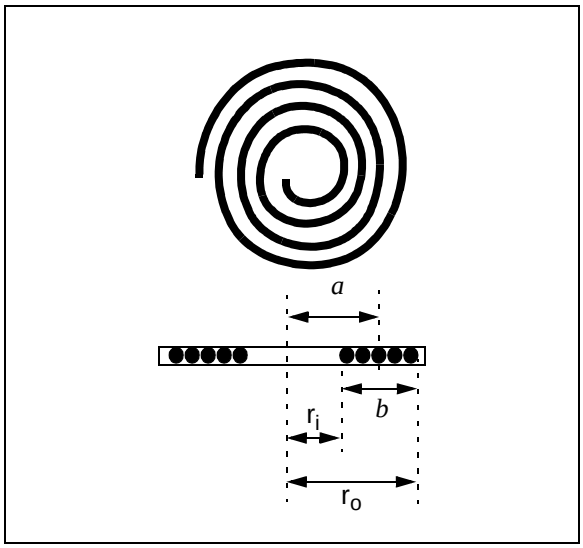
INDUCTANCE OF SPIRAL WOUND COIL WITH SINGLE LAYER

The inductance of a spiral inductor is calculated by:

EQUATION 24:

$$L = \frac{(aN)^2}{8a + 11b} \qquad (\mu H)$$

FIGURE 15: A SPIRAL COIL



where:

a = $(r_i + r_o)/2$
b = $r_o - r_i$
r_i = Inner radius of the spiral
r_o = Outer radius of the spiral

Note: All dimensions are in cm

INDUCTANCE OF N-TURN SQUARE LOOP COIL WITH MULTILAYER

Inductance of a multilayer square loop coil is calculated by:

EQUATION 25:

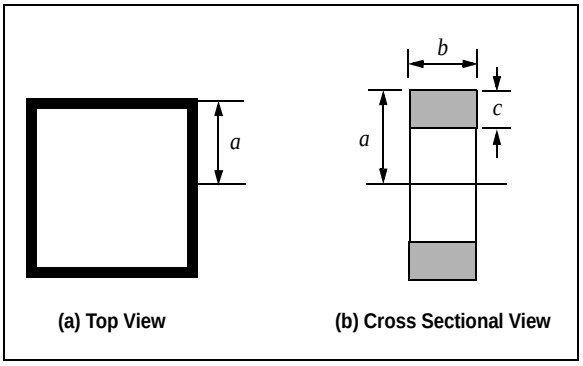
$$L = 0.008aN^2\left\{2.303\log_{10}\left(\frac{a}{b+c}\right) + 0.2235\frac{b+c}{a} + 0.726\right\}(\mu H)$$

where:

N = number of turns
a = side of square measured to the center of the rectangular cross section of winding
b = winding length
c = winding depth as shown in Figure 16

Note: All dimensions are in cm

FIGURE 16: N-TURN SQUARE LOOP COIL WITH MULTILAYER



INDUCTANCE OF A FLAT SQUARE COIL

Inductance of a flat square coil of rectangular cross section with N turns is calculated by[4]:

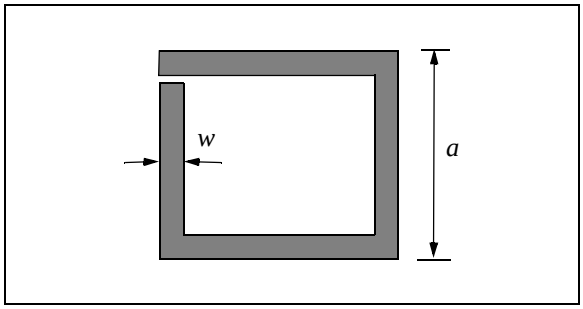
EQUATION 26:

$$L = 0.0467aN^2\left\{\log_{10}\left(2\frac{a^2}{t+w}\right) - \log_{10}(2.414a)\right\} + 0.02032aN^2\left\{0.914 + \left[\frac{0.2235}{a}(t+w)\right]\right\}$$

where:

L = in µH
a = side length in inches
t = thickness in inches
w = width in inches

FIGURE 17: SQUARE LOOP INDUCTOR WITH A RECTANGULAR CROSS SECTION



The formulas for inductance are widely published and provide a reasonable approximation for the relationship between inductance and the number of turns for a given physical size[1–4]. When building prototype coils, it is wise to exceed the number of calculated turns by about 10% and then remove turns to achieve a right value. For production coils, it is best to specify an inductance and tolerance rather than a specific number of turns.

CONFIGURATION OF ANTENNA CIRCUITS

Reader Antenna Circuits

The inductance for the reader antenna coil for 13.56 MHz is typically in the range of a few microhenries (μH). The antenna can be formed by aircore or ferrite core inductors. The antenna can also be formed by a metallic or conductive trace on PCB board or on flexible substrate.

The reader antenna can be made of either a single coil, that is typically forming a series or a parallel resonant circuit, or a double loop (transformer) antenna coil. Figure 18 shows various configurations of reader antenna circuit. The coil circuit must be tuned to the operating frequency to maximize power efficiency. The tuned LC resonant circuit is the same as the bandpass filter that passes only a selected frequency. The *Q* of the tuned circuit is related to both read range and bandwidth of the circuit. More on this subject will be discussed in the following section.

Choosing the size and type of antenna circuit depends on the system design topology. The series resonant circuit results in minimum impedance at the resonance frequency. Therefore, it draws a maximum current at the resonance frequency. Because of its simple circuit topology and relatively low cost, this type of antenna circuit is suitable for proximity reader antenna.

On the other hand, a parallel resonant circuit results in maximum impedance at the resonance frequency. Therefore, maximum voltage is available at the resonance frequency. Although it has a minimum resonant current, it still has a strong circulating current that is proportional to *Q* of the circuit. The double loop antenna coil that is formed by two parallel antenna circuits can also be used.

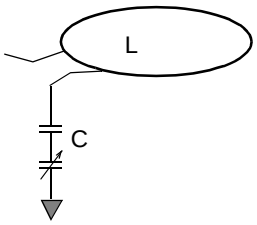
The frequency tolerance of the carrier frequency and output power level from the read antenna is regulated by government regulations (e.g., FCC in the USA).

FCC limits for 13.56 MHz frequency band are as follows:

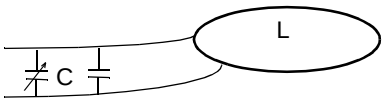
1. Tolerance of the carrier frequency: 13.56 MHz +/- 0.01% = +/- 1.356 kHz.
2. Frequency bandwidth: +/- 7 kHz.
3. Power level of fundamental frequency: 10 mv/m at 30 meters from the transmitter.
4. Power level for harmonics: -50.45 dB down from the fundamental signal.

The transmission circuit including the antenna coil must be designed to meet the FCC limits.

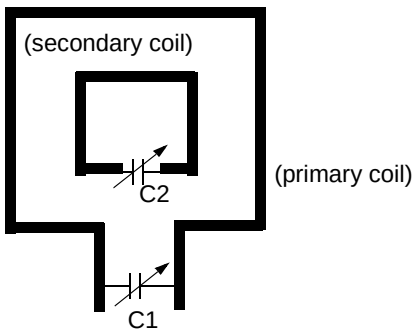
FIGURE 18: VARIOUS READER ANTENNA CIRCUITS



(a) Series Resonant Circuit



(b) Parallel Resonant Circuit



(c) Transformer Loop Antenna

Tag Antenna Circuits

The MCRF355 device communicates data by tuning and detuning the antenna circuit (see AN707). Figure 19 shows examples of the external circuit arrangement.

The external circuit must be tuned to the resonant frequency of the reader antenna. In a detuned condition, a circuit element between the antenna B and VSS pads is shorted. The frequency difference (delta frequency) between tuned and detuned frequencies must be adjusted properly for optimum operation. It has been found that maximum modulation index and maximum read range occur when the tuned and detuned frequencies are separated by 3 to 6 MHz.

The tuned frequency is formed from the circuit elements between the antenna A and VSS pads without shorting the antenna B pad. The detuned frequency is found when the antenna B pad is shorted. This detuned frequency is calculated from the circuit between antenna A and VSS pads excluding the circuit element between antenna B and VSS pads.

In Figure 19 (a), the tuned resonant frequency is:

EQUATION 27:

$$f_o = \frac{1}{2\pi\sqrt{L_T C}}$$

where:

L_T = $L_1 + L_2 + 2L_M$ = Total inductance between antenna A and VSS pads

L_1 = inductance between antenna A and antenna B pads

L_2 = inductance between ant. B and VSS pads

M = mutual inductance between coil 1 and coil 2

= $k\sqrt{L_1 L_2}$

k = coupling coefficient between the two coils

C = tuning capacitance

and detuned frequency is:

EQUATION 28:

$$f_{detuned} = \frac{1}{2\pi\sqrt{L_1 C}}$$

In this case, $f_{detuned}$ is higher than f_{tuned}.

Figure 19(b) shows another example of the external circuit arrangement. This configuration controls C_2 for tuned and detuned frequencies. The tuned and untuned frequencies are

EQUATION 29:

$$f_{tuned} = \frac{1}{2\pi\sqrt{\left(\frac{C_1 C_2}{C_1 + C_2}\right)L}}$$

and

EQUATION 30:

$$f_{detuned} = \frac{1}{2\pi\sqrt{LC_1}}$$

A typical inductance of the coil is about a few microhenry with a few turns. Once the inductance is determined, the resonant capacitance is calculated from the above equations. For example, if a coil has an inductance of 1.3 µH, then it needs a 106 pF of capacitance to resonate at 13.56 MHz.

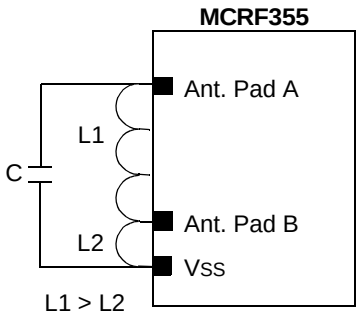
CONSIDERATION ON QUALITY FACTOR *Q* AND BANDWIDTH OF TUNING CIRCUIT

The voltage across the coil is a product of quality factor *Q* of the circuit and input voltage. Therefore, for a given input voltage signal, the coil voltage is directly proportional to the *Q* of the circuit. In general, a higher *Q* results in longer read range. However, the *Q* is also related to the bandwidth of the circuit as shown in the following equation.

EQUATION 31:

$$Q = \frac{f_o}{B}$$

FIGURE 19: VARIOUS EXTERNAL CIRCUIT CONFIGURATIONS



(a) Two inductors and one capacitor

$$f_{tuned} = \frac{1}{2\pi\sqrt{L_T C}}$$

$$f_{detuned} = \frac{1}{2\pi\sqrt{L_1 C}}$$

$$L_T = L_1 + L_2 + 2L_m$$

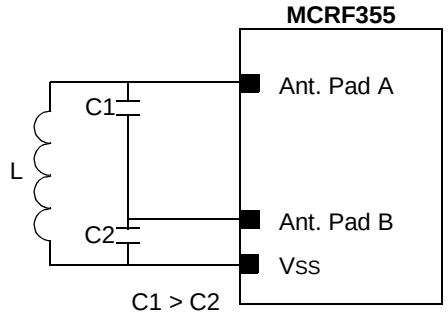
where:

L_m = mutual inductance

= $K\sqrt{L_1 L_2}$

K = coupling coefficient of two inductors

$0 \le K \le 1$

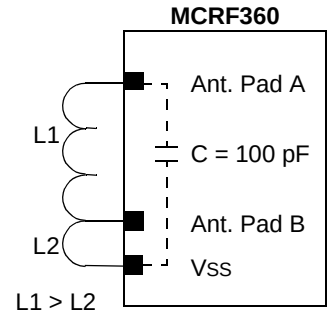


(b) Two capacitors and one inductor

$$f_{tuned} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$f_{detuned} = \frac{1}{2\pi\sqrt{LC_1}}$$

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$



(c) Two inductors with one internal capacitor

$$f_{tuned} = \frac{1}{2\pi\sqrt{L_T C}}$$

$$f_{detuned} = \frac{1}{2\pi\sqrt{L_1 C}}$$

$$L_T = L_1 + L_2 + 2L_m$$

Bandwidth requirement and limit on circuit *Q* for MCRF355

Since the MCRF355 operates with a data rate of 70 kHz, the reader antenna circuit needs a bandwidth of at least twice of the data rate. Therefore, it needs:

EQUATION 32:

$$B_{minimum} = 140 \text{ kHz}$$

Assuming the circuit is turned at 13.56 MHz, the maximum attainable Q is obtained from Equations 31 and 32:

EQUATION 33:

$$Q_{max} = \frac{f_o}{B} = 96.8$$

In a practical LC resonant circuit, the range of Q for 13.56 MHz band is about 40. However, the Q can be significantly increased with a ferrite core inductor. The system designer must consider the above limits for optimum operation.

RESONANT CIRCUITS

Once the frequency and the inductance of the coil are determined, the resonant capacitance can be calculated from:

EQUATION 34:

$$C = \frac{1}{L(2\pi f_o)^2}$$

In practical applications, parasitic (distributed) capacitance is present between turns. The parasitic capacitance in a typical tag antenna coil is a few (pF). This parasitic capacitance increases with operating frequency of the device.

There are two different resonant circuits: parallel and series. The parallel resonant circuit has maximum impedance at the resonance frequency. It has a minimum current and maximum voltage at the resonance frequency. Although the current in the circuit is minimum at the resonant frequency, there are a circulation current that is proportional to Q of the circuit. The parallel resonant circuit is used in both the tag and the high-power reader antenna circuit.

On the other hand, the series resonant circuit has a minimum impedance at the resonance frequency. As a result, maximum current is available in the circuit. Because of its simplicity and the availability of the high current into the antenna element, the series resonant circuit is often used for a simple proximity reader.

Parallel Resonant Circuit

Figure 20 shows a simple parallel resonant circuit. The total impedance of the circuit is given by:

EQUATION 35:

$$Z(j\omega) = \frac{j\omega L}{(1-\omega^2 LC) + j\frac{\omega L}{R}} \quad (\Omega)$$

where ω is an angular frequency given as $\omega = 2\pi f$.

The maximum impedance occurs when the denominator in the above equation is minimized. This condition occurs when:

EQUATION 36:

$$\omega^2 LC = 1$$

This is called a resonance condition, and the resonance frequency is given by:

EQUATION 37:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

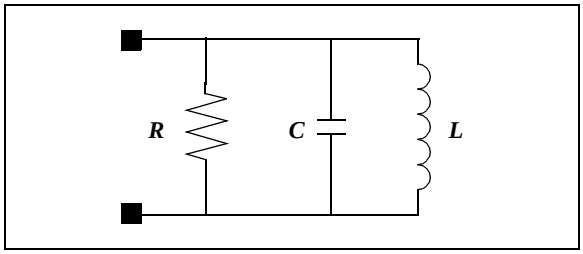
By applying Equation 36 into Equation 35, the impedance at the resonance frequency becomes:

EQUATION 38:

$$Z = R$$

where R is the load resistance.

FIGURE 20: PARALLEL RESONANT CIRCUIT



The R and C in the parallel resonant circuit determine the bandwidth, B, of the circuit.

EQUATION 39:

$$B = \frac{1}{2\pi RC} \quad (Hz)$$

The quality factor, Q, is defined by various ways such as

EQUATION 40:

$$Q = \frac{\text{Energy Stored in the System per One Cycle}}{\text{Energy Dissipated in the System per One Cycle}}$$

$$= \frac{reactance}{resistance}$$

$$= \frac{\omega L}{r} \qquad \text{For inductance}$$

$$= \frac{1}{\omega c r} \qquad \text{For capacitance}$$

$$= \frac{f_0}{B}$$

where:

$\omega = 2\pi f$ = angular frequency
f_0 = resonant frequency
B = bandwidth
r = ohmic losses

By applying Equation 37 and Equation 39 into Equation 40, the Q in the parallel resonant circuit is:

EQUATION 41:

$$Q = R\sqrt{\frac{C}{L}}$$

The Q in a parallel resonant circuit is proportional to the load resistance R and also to the ratio of capacitance and inductance in the circuit.

When this parallel resonant circuit is used for the tag antenna circuit, the voltage drop across the circuit can be obtained by combining Equations 8 and 41:

EQUATION 42: .

$$V_o = 2\pi f_o NQSB_o \cos\alpha$$

$$= 2\pi f_0 N\left(R\sqrt{\frac{C}{L}}\right)SB_0 \cos\alpha$$

The above equation indicates that the induced voltage in the tag coil is inversely proportional to the square root of the coil inductance, but proportional to the number of turns and surface area of the coil.

Series Resonant Circuit

A simple series resonant circuit is shown in Figure 21. The expression for the impedance of the circuit is:

EQUATION 43:

$$Z(j\omega) = r + j(X_L - X_C) \qquad (\Omega)$$

where:

r = a DC ohmic resistance of coil and capacitor
X_L *and* X_C = the reactance of the coil and capacitor, respectively, such that:

EQUATION 44:

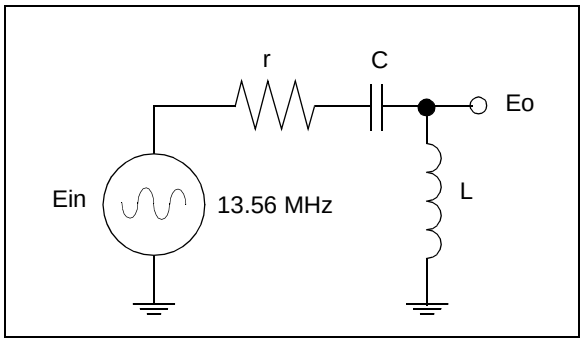
$$X_L = 2\pi f_o L \qquad (\Omega)$$

EQUATION 45:

$$X_c = \frac{1}{2\pi f_o C} \qquad (\Omega)$$

The impedance in Equation 43 becomes minimized when the reactance component cancelled out each other such that $X_L = X_C$. This is called a resonance condition. The resonance frequency is same as the parallel resonant frequency given in Equation 37.

FIGURE 21: SERIES RESONANCE CIRCUIT



The half power frequency bandwidth is determined by r and L, and given by:

EQUATION 46:

$$B = \frac{r}{2\pi L} \qquad (Hz)$$

The quality factor, Q, in the series resonant circuit is given by:

$$Q = \frac{f_0}{B} = \frac{\omega L}{r} = \frac{1}{r\omega C}$$

The series circuit forms a voltage divider, the voltage drops in the coil is given by:

EQUATION 47:

$$V_o = \frac{jX_L}{r + jX_L - jX_c} V_{in}$$

When the circuit is tuned to a resonant frequency such as $X_L = X_C$, the voltage across the coil becomes:

EQUATION 48:

$$V_o = \frac{jX_L}{r} V_{in}$$

$$= jQV_{in}$$

The above equation indicates that the coil voltage is a product of input voltage and Q of the circuit. For example, a circuit with Q of 40 can have a coil voltage that is 40 times higher than input signal. This is because all energy in the input signal spectrum becomes squeezed into a single frequency band.

EXAMPLE 8: CIRCUIT PARAMETERS

If the DC ohmic resistance r is 5 Ω, then the L and C values for 13.56 MHz resonant circuit with Q = 40 are:

EQUATION 49:

$$X_L = Qr_s = 200\Omega$$

$$L = \frac{X_L}{2\pi f} = \frac{200}{2\pi(13.56MHz)} = 2.347 \qquad (\mu H)$$

$$C = \frac{1}{2\pi f X_L} = \frac{1}{2\pi(13.56\ \text{MHz})(200)} = 58.7\ \text{(pF)}$$

TUNING METHOD

The circuit must be tuned to the resonance frequency for a maximum performance (read range) of the device. Two examples of tuning the circuit are as follows:

- **Voltage Measurement Method:**
  a) Set up a voltage signal source at the resonance frequency.
  b) Connect a voltage signal source across the resonant circuit.
  c) Connect an Oscilloscope across the resonant circuit.
  d) Tune the capacitor or the coil while observing the signal amplitude on the Oscilloscope.
  e) Stop the tuning at the maximum voltage.

- **S-parameter or Impedance Measurement Method using Network Analyzer:**
  a) Set up an S-Parameter Test Set (Network Analyzer) for S11 measurement, and do a calibration.
  b) Measure the S11 for the resonant circuit.
  c) Reflection impedance or reflection admittance can be measured instead of the S11.
  d) Tune the capacitor or the coil until a maximum null (S11) occurs at the resonance frequency, f_0. For the impedance measurement, the maximum peak will occur for the parallel resonant circuit, and minimum peak for the series resonant circuit.

FIGURE 22: VOLTAGE VS. FREQUENCY FOR RESONANT CIRCUIT

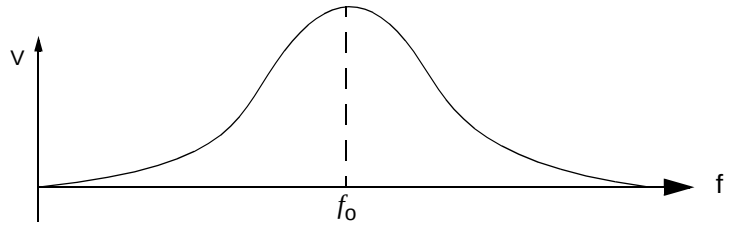
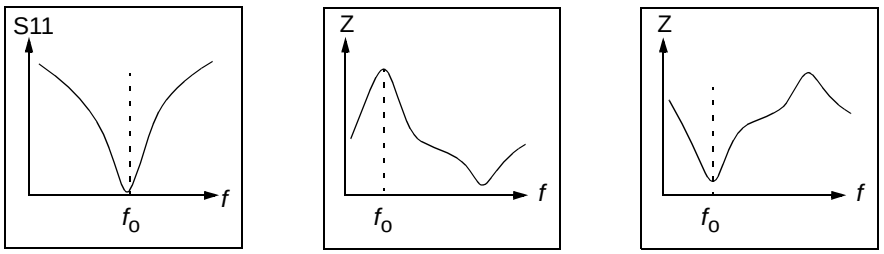


FIGURE 23: FREQUENCY RESPONSES FOR RESONANT CIRCUIT



(a) (b) (c)

Note 1: (a) S11 Response, (b) Impedance Response for a Parallel Resonant Circuit, and (c) Impedance Response for a Series Resonant Circuit.

2: In (a), the null at the resonance frequency represents a minimum input reflection at the resonance frequency. This means the circuit absorbs the signal at the frequency while other frequencies are reflected back. In (b), the impedance curve has a peak at the resonance frequency. This is because the parallel resonant circuit has a maximum impedance at the resonance frequency. (c) shows a response for the series resonant circuit. Since the series resonant circuit has a minimum impedance at the resonance frequency, a minimum peak occurs at the resonance frequency.

READ RANGE OF RFID DEVICES

Read range is defined as a maximum communication distance between the reader and tag. In general, the read range of passive RFID products varies, depending on system configuration and is affected by the following parameters:

a) Operating frequency and performance of antenna coils
b) Q of antenna and tuning circuit
c) Antenna orientation
d) Excitation current
e) Sensitivity of receiver
f) Coding (or modulation) and decoding (or demodulation) algorithm
g) Number of data bits and detection (interpretation) algorithm
h) Condition of operating environment (electrical noise), etc.

The read range of 13.56 MHz is relatively longer than that of 125 kHz device. This is because the antenna efficiency increases as the frequency increases. With a given operating frequency, the conditions (a – c) are related to the antenna configuration and tuning circuit. The conditions (d – e) are determined by a circuit topology of reader. The condition (f) is a communication protocol of the device, and (g) is related to a firmware software program for data detection.

Assuming the device is operating under a given condition, the read range of the device is largely affected by the performance of the antenna coil. It is always true that a longer read range is expected with the larger size of the antenna with a proper antenna design. Figures 24 and 25 show typical examples of the read range of various passive RFID devices.

FIGURE 24: READ RANGE VS. TAG SIZE FOR TYPICAL PROXIMITY APPLICATIONS*

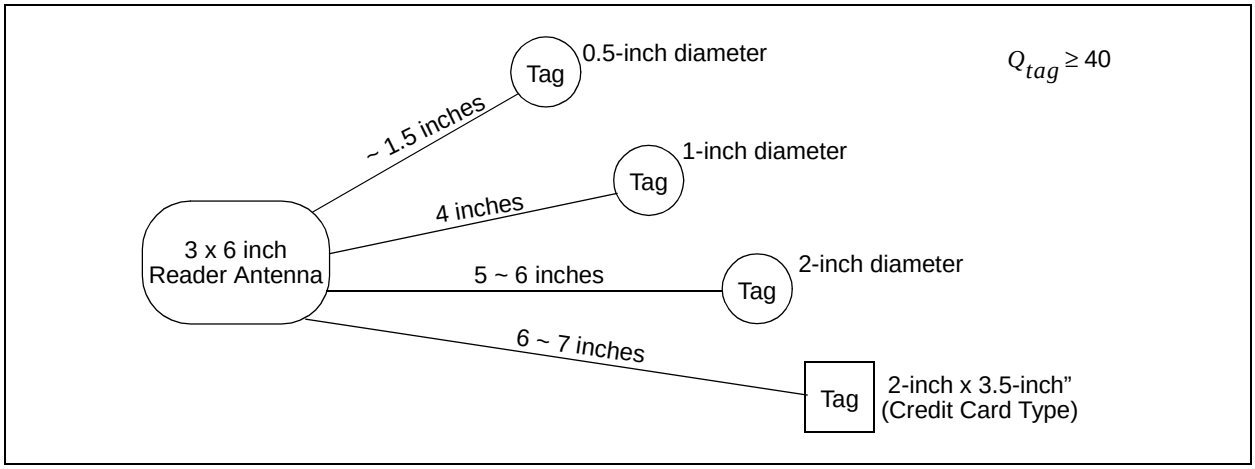
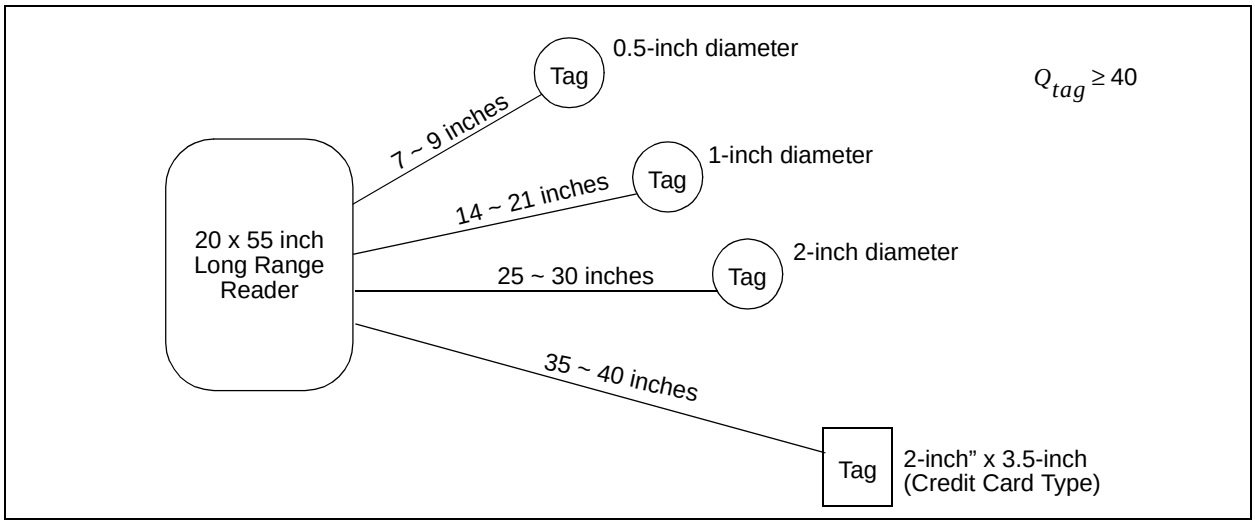


FIGURE 25: READ RANGE VS. TAG SIZE FOR TYPICAL LONG RANGE APPLICATIONS*



Note: Actual results may be shorter or longer than the range shown, depending upon factors discussed above.

REFERENCES

[1] V. G. Welsby, The Theory and Design of Inductance Coils, John Wiley and Sons, Inc., 1960.

[2] Frederick W. Grover, Inductance Calculations Working Formulas and Tables, Dover Publications, Inc., New York, NY., 1946.

[3] Keith Henry, Editor, Radio Engineering Handbook, McGraw-Hill Book Company, New York, NY., 1963.

[4] James K. Hardy, High Frequency Circuit Design, Reston Publishing Company, Inc.Reston, Virginia, 1975.

MCRF355/360 Reader Reference Design

1.0 INTRODUCTION

This chapter provides a reference guide for the 13.56 MHz reader designer. The schematic included in this chapter is for the 13.56 MHz Reference Reader included in the DV103003 microID™ Developer's Kit. The circuit is designed for short read-range applications. The basic design can be modified for long-range or other applications with MCRF355/360 devices. An electronic copy of the PICmicro® microcontroller source code is available upon request.

2.0 READER CIRCUITS

The RFID reader consists of transmitting and receiving sections. It transmits a carrier signal (13.56 MHz), receives the backscattered signal from the tag, and performs data processing. The reader also communicates with an external host computer. A basic block diagram of a typical RFID reader is shown in Figure 2-1.

The transmitting section contains a 13.56 MHz signal oscillator (74HC04), power amplifier (Q2), and RF tuning circuits. The tuning circuit matches impedance between the antenna coil circuit and the power driver at 13.56 MHz. The radiating signal strength from the antenna must comply with government regulations. For best performance, the antenna coil circuit must be tuned to the same frequency of the tag. The design for antenna circuits is given in Application Note AN710 (DS00710).

The receiving section contains an envelope detector (D6), hi-pass filters, and amplifiers (U2 and U3). When the tag is energized, it transmits 154 bits of data that is encoded in Biphase-L (Manchester). In the Manchester encoding, data '1' is represented by a logic high-to-low level change at midclock, and data '0' is represented by a low-to-high level change at midclock. There is always a level change at middle of every bit clock.

FIGURE 2-1: FUNCTIONAL BLOCK DIAGRAM OF TYPICAL RFID READER

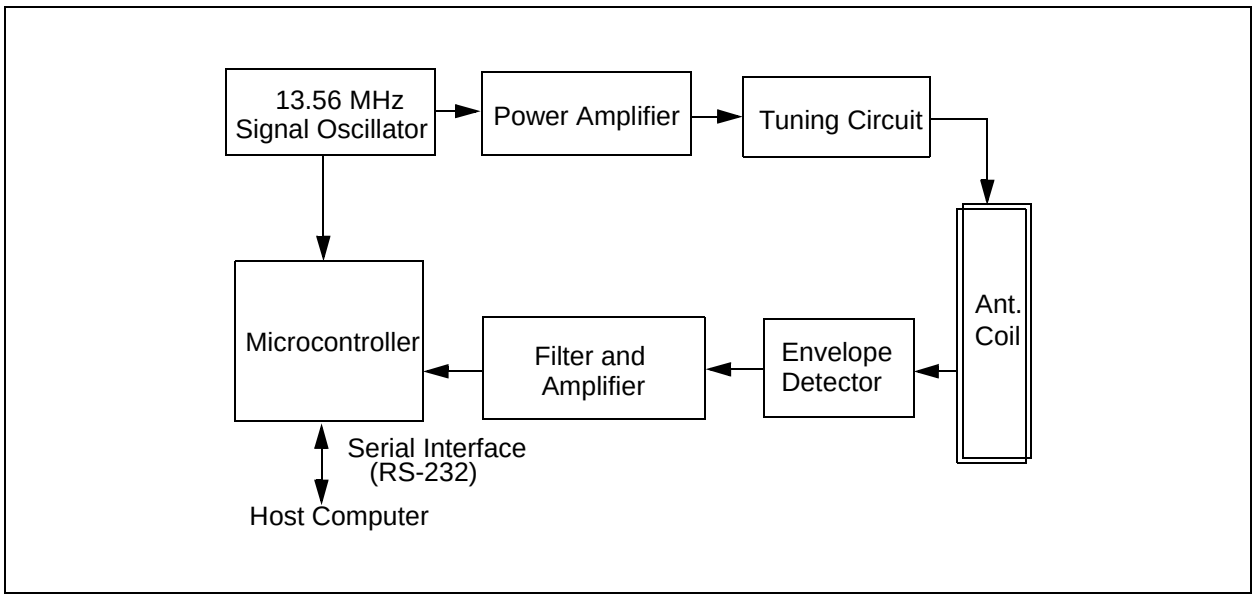


FIGURE 2-2: SIGNAL WAVEFORMS

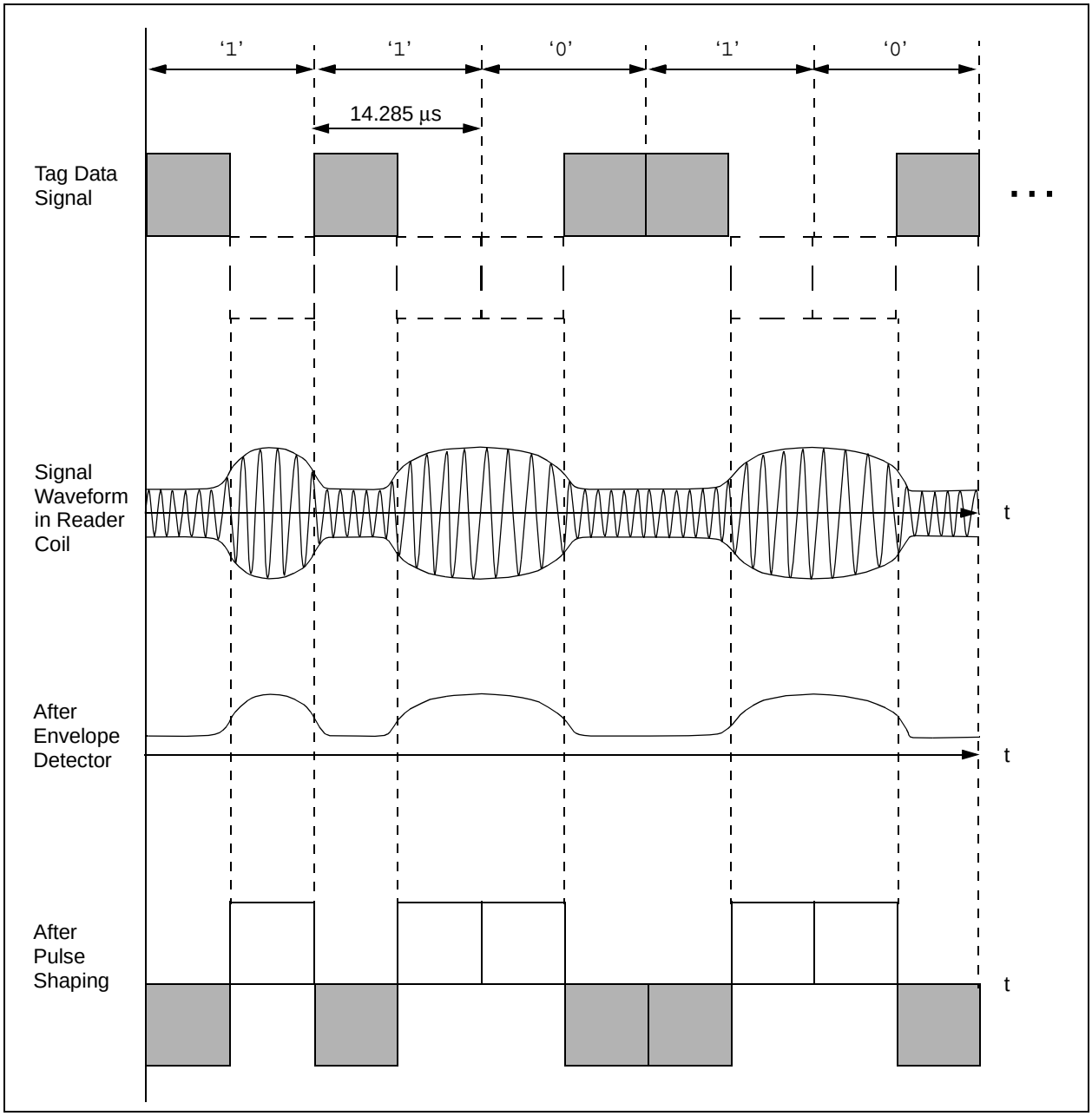
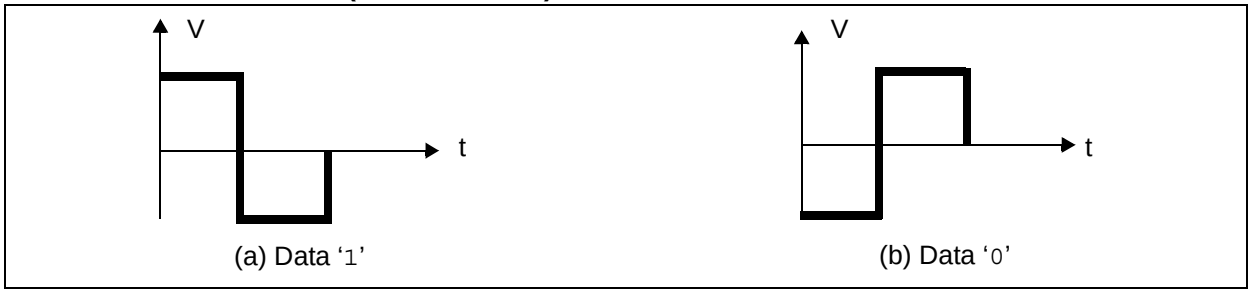


FIGURE 2-3: BIPHASE-L (MANCHESTER) SIGNAL



(a) Data '1' (b) Data '0'

When the tag is energized by the reader's carrier signal, it transmits back with an amplitude modulated signal. This results in a perturbation in the voltage amplitude across the reader antenna coil. The envelope detector detects the changes in the voltage amplitude and passes it into an RC filter (R7, C11). The charged signal in the capacitor passes through active filters and amplifiers. The signal that is passing through this receiving section is the data signal. This filtered-shaped data signal is fed into Pin 10 of the microcontroller for data processing.

2.1 FCC Specifications on Transmitting Signal

Each country limits the signal strength of the radio frequency signal that is intentionally radiated from the device. In the USA, the maximum signal strength that is radiated from the device is regulated by Federal Communication Commission (FCC). Any device operating at 13.56 MHz frequency band must comply with the FCC Part 15.225 of the federal regulation. FCC limits for 13.56 MHz frequency band are al follows:

1. Tolerance of the carrier frequency: 13.56 MHz +/- 0.01% = +/- 7 kHz.
2. Frequency bandwidth: +/- 7 kHz.
3. Power level of fundamental frequency: 10 mv/m at 30 meters from the transmitter.
4. Power level for harmonics: -50.45 dB down from the fundamental signal.

The transmission circuit including the antenna coil must be designed to meet the FCC limits.

3.0 OPTIMIZATION FOR LONG-RANGE APPLICATIONS

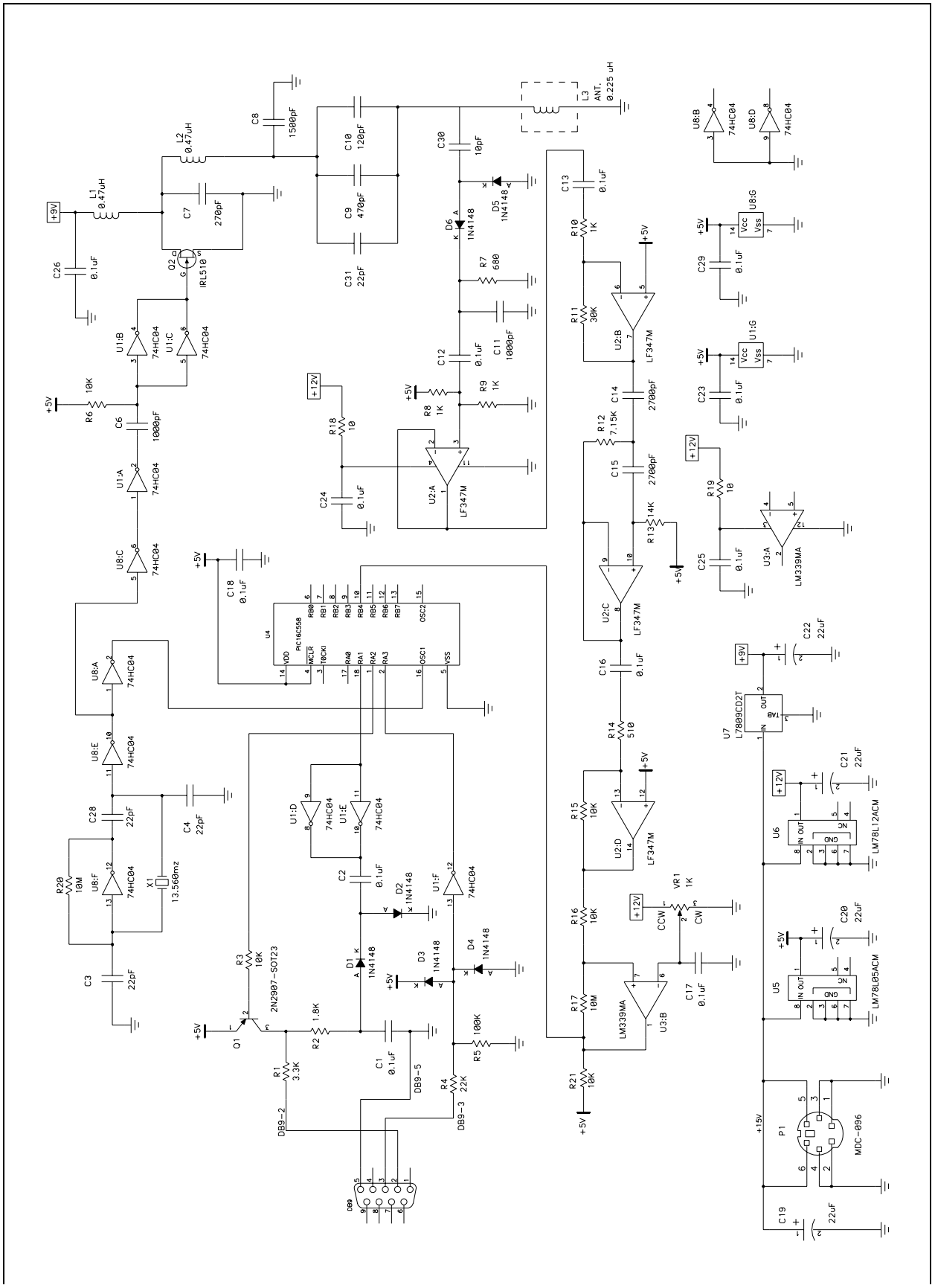
The reader circuit provided is designed for about a 5-inch read-range, using a 2-inch by 2-inch tag coil that is printed on PCB with the MCRF355. The read-range can be increased by increasing the reader power, sensitivity, and antenna size. A read-range of more than 30-inches can be achieved with the MCRF355 and an optimized reader. In order to optimize the reader circuit for long-range applications, the following aspects may be considered:

1. **Optimize the output power level within FCC limits.** The reader should provide a sufficient signal level to the tag. The tag needs about 4 V_{PP} across the coil circuit for operation. The power level radiating from the reader antenna must comply to the government regulations such as FCC specifications in the USA. The FCC limits for 13.56 MHz band are described in Section 2.1. For long-range applications, the designer may start with about 50 V_{PP} of antenna voltage and optimize the signal strength for a read-range within the government regulations.
2. **Increase the size of the antenna.** The read-range, in general, is proportional to the size of the reader coil (see Equation 12 in Application Note 710). An optimum radius of antenna is 1.414 times of the read-range.
3. **Increase the *Q* of the antenna circuit.** The read-range increases with Q of the antenna circuit. This is because the induced voltage is directly proportional to Q of the circuit. The recommended Q for long-range applications is as follows:

   $40 < Q < 96$ for reader
   $40 < Q$ for tag

4. **Optimize the input sensitivity of the reader.** The sensitivity is a measure of how weak a signal can be and still be satisfactorily received. The sensitivity is proportional to the carrier power and square of the modulation index (1 for 100% modulation such as MCRF355). It is inversely proportional to the noise signal. The limit to the sensitivity of the receiving section of the reader is noise, both external and internal. The external noises may come from various sources such as computers, televisions, appliances, motors, power lines, transformers, etc. The internal noise is mostly due to a thermal noise of components. To reduce noise, the reader should be operated a distance away from the noise sources. The receiving section may have a 70 kHz bandpass filter to reduce the noises. The 70 kHz bandpass filter will pass only the 70 kHz data signal for processing. The receiving section should have sensitivity of about -120 dBm for long-range applications.
5. **Optimize the amplitude gain circuit.** The receiving circuit amplifies the modulated signals before data processing. The input signal contains both real data and noise. Typically, op amplifiers are used for both as a gain amplifier and filter. The gain must be optimized within the circuit to obtain gains only at the real data signal.

4.0 READER SCHEMATIC



5.0 READER BILL OF MATERIALS

Assembly #	Line #	Qty	Part #	Part Description	Reference Designator
02-01523	1	1	02-01523-D	PCB ASSY DWG, MCRF355 microID READER	—
02-01523	2	1	03-01523	SCHEMATIC, MCRF355 microID READER	—
02-01523	3	1	04-01523	PCB FABRICATION, MCRF355 microID READER	—
02-01523	4	2	MM74HC04M	IC, SMT, CMOS HEX INVERTER, 14P SOIC	U1, U8
02-01523	5	1	LF347M	IC, SMT, QUAD BI-FET OP AMP, 14P SOIC	U2
02-01523	6	1	LM339M	IC, SMT, LOW POWER LOW OFFSET VOLT QUAD COMPARATORS,14P SOIC	U3
02-01523	7	1	PIC16C558-20/SO	IC, PIC16C558-20/SO EPROM-BASED 8-BIT CMOS MICROCONTROLLER	U4
02-01523	8	1	LM78L05ACM	IC, REG, +5V 100 mA REGULATOR	U5
02-01523	9	1	LM78L12ACM	IC, REG, +12V 100 mA REGULATOR	U6
02-01523	10	1	L7809CD2T	IC, +9V, REG 1.5A TO-263	U7
02-01523	11	1	MMBT2907ALT1	TRANSISTOR, PNP, 2N2907A, SOT-23	Q1 Flip upside and bend legs toward the PCB
02-01523	12	1	IRL510	TRANSISTOR, N-CHANNEL HEX FET, TO220AB	Q2
02-01523	13	6	RLS4148TE11C	DIODE SMT, ROHM DIODE LL-34 SIG DIODE	D1-D6
02-01523	14	1	ERJ-3GSYJ332V	RES SMT, 3.3K OHM, 1/16W, 5%, 0603	R1
02-01523	15	1	ERJ-3GSYJ182V	RES SMT, 1.8K OHM, 1/16W, 5%, 0603	R2
02-01523	16	5	ERJ-3GSYJ103V	RES SMT, 10K OHM, 1/16 W, 5%, 0603	R3, R6, R15, R16, R21
02-01523	17	1	ERJ-3GSYJ223V	RES SMT, 22K OHM, 5% 0603	R4
02-01523	18	1	ERJ-3GSYJ104V	RES SMT, 100K OHM 1/16W 5% TYPE 0603	R5
02-01523	19	1	ERJ-3GSYJ681V	RES SMT, 680 OHM 1/16W 5% 0603	R7
02-01523	20	3	ERJ-3GSYJ102V	RES SMT, 1K OHM 1/16W 5% 0603	R8-R10
02-01523	21	1	ERJ-3GSYJ303V	RES SMT, 30K OHM 1/16W 5% 0603	R11
02-01523	22	1	ERJ-3EKF7151V	RES SMT, 7.15K OHM 1/16W 1% 0603	R12
02-01523	23	1	MFR-25FRF 14K0	RES, 14K OHM 1/4W 1% MF	R13, connected from U2 pin 12 to top pad of R13
02-01523	24	2	RM73B1JT106J	RES SMT, 10M OHM 1/16W 5% 0603	R17, R20
02-01523	25	2	ERJ-3GSYJ100V	RES SMT, 10 OHM 1/16W 5% 0603	R18, R19
02-01523	26	1	EVM-7JSX30B13	RES SMT, POT, 1K OHM 3MM SEALED, 3 TT	VR1
02-01523	27	12	ECU-V1H104KBW	CAP SMT, 0.1uF 50V 10%, X7R CER 1206	C1, C2, C12, C13, C16-18, C23-C26, C29
02-01523	28	3	ECU-V1H220JCV	CAP SMT, 22 pF CERAMIC 5% 50V 0603 NPO	C3, C4, C28
02-01523	29	2	ECU-V1H102KBV	CAP SMT, 1000 pF 50V CERAMIC 10% 0603 X7R	C6, C11

Assembly #	Line #	Qty	Part #	Part Description	Reference Designator
02-01523	30	1	ECU-V1H271JCV	CAP SMT, 270 pF 50V CERAMIC 5% 0603 NPO	C7
02-01523	31	1	ECU-V1H152KBV	CAP SMT, 1500 pF 50V CERAMIC 10% 0603 X7R	C8
02-01523	32	1	GRM42-6C0G471G500AL	CAP SMT, 470 pF 500V 2% 1206 C0G”	C9
02-01523	33	1	GRM42-6C0G121J500AL	CAP SMT, 120 pF 500V 5% 1206 C0G”	C10
02-01523	34	2	ECU-V1H272KBV	CAP SMT, 2700PF 50V CERAMIC 10% 0603 XR7	C14, C15
02-01523	35	4	ECE-A1EU220	CAP, 22UF 25V RADIAL ELECTROLYTIC 20%	C19-C22
02-01523	36	1	GRM42-6C0G100J500AL	CAP SMT, 10 pF 500V 5% 1206 C0G	C30
02-01523	37	1	GRM42-6C0G220J500AL	CAP SMT, 22 pF 500V 5% 1206 C0G	C31 (AS NEEDED)
02-01523	38	2	43LS477	INDUCTOR, 0.47 µH	L1, L2
02-01523	39	1	MCX0001	OSCILLATOR, CUSTOM 13.560 MHz, PARALLEL MODE, 22 pF LOAD, HC49 CASE, 30 PPM	X1
02-01523	40	1	MDC-096	CONN, MINI-DIN, 6-PIN	P1
02-01523	41	1	KF22-E9S-NJ	CONN, D-SUB 9P RECPT RT ANGLE WITH JACK SCREWS	DB9
02-01523	42	1	08-00170	LABEL, MCRF355 READER FIRM-WARE, 355READ.HEX, 1/25/99, U4	@ U4
02-01523	43	1	ERJ-3GSYJ511V	RES SMT, 510 OHM 1/16W 5% 0603	R14

6.0 READER SOURCE CODE FOR THE PICmicro® MCU

```
;receiver.asm



;Processor: PIC16C558 operating at 13.56 MHz
;           Ti= 295 nsec

        processor 16c558
        #include "P16c558.inc"
        __config h'3ff2'  ;protection off,PWRT enabled,watchdog disabled,HS oscillator


#define _CARRY          STATUS,0
#define _ZERO           STATUS,2

#define _125KHZ         PORTA,1
#define _RS232TX        PORTA,2
#define _RS232RX        PORTA,3
#define _RS232          PORTA
#define SIGNAL          PORTB,4
invmask               = h'2'
;.............................................................
;Define variables and constants here--
delay       =h'20'
wait        =h'21'
acctime     =h'22' ;accumulated sync interval sum--also used as halfbit interval threshold
#define     halfthr     acctime  ;halfbit interval threshold
halfthr     =acctime ;halfbit interval threshold
recv_csumhi =h'23' ;2 bytes for storing received checksum
recv_csumlo =h'24'
bitcnt      =h'25' ;RS232 bit counter
cycle_cnt   =h'26'
halfthr     =h'27' ;threshold value between halfbit and fullbit intervals
ptr1        =h'28' ;temporary FSR storage
ptr2        =h'29' ;temporary FSR storage
TXchar      =h'2a' ;character to transmit over RS232
temp        =h'2b' ;temporary storage
shiftcnt    =h'2c' ;used to strip the framing '0' bits from the rec'd data array
letters    =h'2d' ;storage area for next character to send
charcnt     =h'2e'
lastbit     =h'2f' ;the LSb stores the last rec'd bit--flip it by complementing f

;;;!!!!!!!!!!!!!!!!!!!!bit storage area--16 bytes of storage, indirectly addressed
;;;Note that s/w tests for MSb to detect end of area--be careful if move to different
;;;processor or relocate this storage area
recvbits    =h'40'  ;32 bytes set aside for storing the received bits--actual number of bytes
                    ;in transmission is 18
;;Note that main loop uses bit tests to determine bit receive or runaway condition (to limit
;;processing time). Keep this in mind if recvbits storage area changed in the future.
```

```
;;40h-60h is reserved for received bits--actual bit receiving area 40h-51h, rest is overrun area

;;52h-73h set aside for ASCII conversion of received bytes before RS232 transmission. Note that
;;52h-60h contains no useful information from the use during receive of demodulated bits. Also,
;;        bits are not being received while the ASCII conversion and serial transmission are
;;        taking place.
;;        'G' 1st character: "go"
;;        Character 2-37:    ASCII representation of received 18 bytes (until checksum used)
;;        Character 38:      '\n' newline

sendascii   =h'52'  ;begin of storage area for ASCII conversion of received bytes
xfercnt     =d'14'  ;defines number of received bytes to convert to ASCII & transmit

;.....................................................................

;.....................................................................................
;Overall function- To recover Manchester encoded RFID message after AM demodulation and
;                  comparator decision. The comparator input trips the interrupt on PORTB change.
;The steps are:
;
;     1- Initialize registers to seek synch field.
;     2- Determine bit width from synch field by averaging the periods between transitions
;        over the synch field. TMR0 is cleared at each edge. If the timer overflows before
;          the next edge, synch seek starts over. The synch field is composed of 9 bits.
;     3- Use the measured bit width to establish a threshold period between repeat bits and
;          complement of previous bit. This is due to the Manchester encoding method. Since there
;          is always a transition in the middle of each bit interval transmitted, a repeated bit
;          will appear as a pair of edges that occur with a halfbit interval period. A bit that
;          is the complement of the last received bit will appear as an interval between edges
;          of a full bit interval period.
;     4- Shift in bits as they are received into the storage array. When the timer overflows,
;          consider the data field over. The received data format is MSb to LSb, where the MSb
;          is the first bit received.
;     5- There are 16 bytes in the message, followed by a 16 bit checksum of the message
;          contents. The remaining bit is unused.
;       6- Compute the checksum of the received 16 byte message and compare to the received
;          checksum.
;       7- If checksums match, convert the message and the checksum into ASCII form and transmit
;          over the RS232 serial link. The message format is:
;                 "GG" :the go characters (start of message)
;                 36 bytes which are the ASCII representation of the 18 bytes received
;                 "\n" : closing newline character
;          The serial data rate is 9600 bps, 8 data bits, 1 stop, no parity
;.....................................................................


        org h'000'          ;RESET vector location
        goto   init
        org h'004'          ;interrupt vector location

;=============================================================================================
;;isr(): interrupt service routine
;        interrupts enabled for transition on PORTB
;
;        1- BEWARE! To minimize interrupt response time, the w & status register are NOT
;           archived.
;      2- The isr execution path is determined by w register and uses calculated goto's.
;           The w for next isr is set at end of current isr execution and is dependent on
;           signal context (i.e. sync start, w/in sync, w/in data, etc.)
;         Be very cautious here--must stay w/in 255 instructions for this to work!
;      3- Sync field processed as follows:
;            -Ignore the first 4 transitions, they may be in response to tag power on reset
;            -Accumulate the sum of next 8 intervals
;            -Establish half bit width from full bit width threshold value based on
;             average interval measured above. Due to Manchester encoding, repeat of previous
```

```
;             bit will be a series of 2 halfbit width intervals, complement of previous bit
;             will be a fullbit width interval. halfbit defined as 1.5x(average sync).
;               -wait for interval over the fullbit threshold. This is end of sync. In accordance
;             w/ Manchester encoding, the sync field will be: 1 1 1 1 1 1 1 1 0
;=============================================================================================
isr
      addwf  PCL,f       ;4 calculated goto
;first sync edge is calculated goto here
      clrf   TMR0        ;5
      movf   PORTB,f     ;6 must read PORTB before clearing RBIF
      bcf    INTCON,RBIF ;7 just in case timer interrupt happened just at 1st edge
      bcf    INTCON,T0IF ;8
      movlw  (first_cycle - isr-d'1') ;9 next isr calculated goto offset
      clrf   lastbit     ;10  lastbit @ end of sync = 0
      retfie             ;12
;end of first cycle here. Note that first 4 transitions are ignored, because sync start is
;corrupted by tag power on reset.
first_cycle
      clrf   TMR0        ;5
      movf   PORTB,f     ;6 must read PORTB before clearing RBIF
      bcf    INTCON,RBIF ;7
      movlw  (second_cycle - isr-d'1') ;8 next isr calculated goto offset
      retfie             ;10
;end of 2nd cycle here. Note that first 4 transitions are ignored, because sync start is
;corrupted by tag power on reset.
second_cycle
      clrf   TMR0        ;5
      movf   PORTB,f     ;6 must read PORTB before clearing RBIF
      bcf    INTCON,RBIF ;7
      movlw  recvbits    ;8
      movwf  FSR         ;9 set up to store data bits
      movlw  (third_cycle - isr-d'1') ;10 next isr calculated goto offset
      retfie             ;12
;end of 3rd cycle here. Note that first 4 transitions are ignored, because sync start is
;corrupted by tag power on reset. The 3rd cycle is the 4th transition, so from here we measure
;the longest interval in sync field.
third_cycle
      clrf   TMR0        ;5
      movf   PORTB,f     ;6 must read PORTB before clearing RBIF
      bcf    INTCON,RBIF ;7
      clrf   acctime     ;8  reset accumulated sync interval for average
      movlw  (fourth_cycle - isr-d'1') ;9 next isr calculated goto offset
      retfie             ;11
;end of 4th cycle here. Start looking for longest sync interval here.
fourth_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9  first measured sync cycle, must be the largest
      movlw  (fifth_cycle - isr-d'1') ;10
      retfie             ;12
;end of 5th cycle here.
fifth_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (sixth_cycle - isr-d'1') ;10
      retfie             ;12
;end of 6th cycle here.
sixth_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
```

```
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (seventh_cycle - isr-d'1') ;10
      retfie             ;12
;end of 7th cycle here.
seventh_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (eighth_cycle - isr-d'1') ;10
      retfie             ;12
;end of 8th cycle here.
eighth_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (nineth_cycle - isr-d'1') ;10
      retfie             ;12
;end of 9th cycle here.
nineth_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (tenth_cycle - isr-d'1') ;10
      retfie             ;12
;end of 10th cycle here.
tenth_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (eleventh_cycle - isr-d'1') ;10
      retfie             ;12
;end of 11th cycle here. --this is last of sync cycles to be accumulated. Average the result
;and determine halfbit threshold in remaining sync cycles.
eleventh_cycle
      movf   TMR0,w      ;5
      clrf   TMR0        ;6
      movf   PORTB,f     ;7
      bcf    INTCON,RBIF ;8
      addwf  acctime,f   ;9   acctime = acctime + TMR0
      movlw  (twelfth_cycle - isr-d'1') ;10
      retfie             ;12
;end of 12th cycle here. Start averaging the sync interval accumulated time
twelfth_cycle
      movf   PORTB,f     ;5
      bcf    INTCON,RBIF ;6
      rrf    acctime,f   ;7 acctime/2
      rrf    acctime,f   ;8 acctime/4
      rrf    acctime,f   ;9 avg interval = acctime/8
      movlw  h'1f'       ;10   clear 3 MSbs that may have been set by carry
      andwf  acctime,f   ;11
      movlw  (cycle13 - isr-d'1') ;12
      retfie             ;14
;end of 13th cycle here. Calculate the halfbit threshold = 1.5(sync interval avg) Note that
;that the threshold value will be kept in acctime (=halfthr)
cycle13
```

```
      clrf   TMR0        ;5
      movf   PORTB,f     ;6
      bcf    INTCON,RBIF ;7
      rrf    acctime,w   ;8 half the sync interval avg
      addwf  acctime,f   ;9 halfthr = 1+1.5x(sync interval avg)
      incf   acctime,f   ;10
      movlw  (sync_end - h'100'-h'1'-isr) ;11
      bsf    PCLATH,0    ;12  adjust for origin @ 100h
      retfie             ;14

      org   h'100'
;sync end wait. End of sync is distinguished by a fullbit interval. ( T > halfthr )
sync_end
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9    Test interval to detect end of sync field (halfthr - w)
      movlw (sync_end - h'100'-isr-d'1') ;10
      btfss STATUS,C     ;12   Carry set for halfthr >= w
      movlw (bit1 - h'100'-isr-h'1');12   If T > halfbit, end of sync detected. Proceed to data
processing
      retfie             ;14
;rec'd bit processing here --bit1 is 1st bit of 8 bit block
bit1
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit1    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit2 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit1
;repeated bit (1 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half21-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half21       ;2nd half, bit1
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit2-h'100'-isr-h'1');8
      retfie             ;10

;rec'd bit processing here --bit2 is 2nd bit of 8 bit block
bit2
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit2    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
```

```
      movlw (bit3 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit2
;repeated bit (2 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half22-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half22       ;2nd half, bit2
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit3-h'100'-isr-h'1');8
      retfie             ;10
;rec'd bit processing here --bit3 is 3rd bit of 8 bit block
bit3
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit3    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit4 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit3
;repeated bit (3 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half23-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half23       ;2nd half, bit3
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit4-h'100'-isr-h'1');8
      retfie             ;10
;rec'd bit processing here --bit4 is 4th bit of 8 bit block
bit4
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit4    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit5 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit4
;repeated bit (4 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half24-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
```

```
half24       ;2nd half, bit4
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit5-h'100'-isr-h'1');8
      retfie             ;10
;rec'd bit processing here --bit5 is 5th bit of 8 bit block
bit5
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit5    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit6 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit5
;repeated bit (5 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half25-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half25       ;2nd half, bit5
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit6-h'100'-isr-h'1')   ;8
      retfie             ;10

;rec'd bit processing here --bit6 is 6th bit of 8 bit block
bit6
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit6    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit7 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit6
;repeated bit (6 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half26-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half26       ;2nd half, bit6
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit7-h'100'-isr-h'1') ;8
      retfie             ;10
;rec'd bit processing here --bit7 is 7th bit of 8 bit block
bit7
```

```
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit7    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit8 - h'100'-isr-h'1') ;15
      retfie             ;17
halfabit7
;repeated bit (7 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half27-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half27       ;2nd half, bit7
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit8-h'100'-isr-h'1') ;8
      retfie             ;10
;rec'd bit processing here --bit8 is 8th bit of 8 bit block
bit8
      movf  TMR0,w       ;5
      clrf  TMR0         ;6
      movf  PORTB,f      ;7
      bcf   INTCON,RBIF  ;8
      subwf halfthr,w    ;9   Test interval to determine bit. C = 1 for repeated bit
      btfsc STATUS,C     ;11
      goto  halfabit8    ;12
;fullbit processing here
      comf  lastbit,f    ;12  Complement lastbit for fullbit measurement
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14  shift in the new bit
      movlw (bit1 - h'100'-isr-h'1') ;15
      incf  FSR,f        ;16
      retfie             ;18
halfabit8
;repeated bit (8 of 8)
      rrf   lastbit,w    ;13
      rlf   INDF,f       ;14
      movlw (half28-h'100'-isr-h'1') ;15
      retfie             ;17
;2nd half of bit interval processing
half28       ;2nd half, bit8
      clrf  TMR0         ;5
      movf  PORTB,f      ;6
      bcf   INTCON,RBIF  ;7
      movlw (bit1-h'100'-isr-h'1') ;8
      incf  FSR,f        ;9   advance to next byte in recvbits storage array
      retfie             ;11



;The negative RS232 supply is generated by an inverter clocked at ~125 KHz by port pin RA1.
        ;first pump up the -5V, i.e. generate 125 KHz clock (T=8 usec, ~27 Ti)
        ;run for a total of 128 cycles before sending data
       ;put line at stop bit level

alphabet
```

```
        clrwdt
      bcf   INTCON,GIE  ;make sure interrupts are off
      movlw  sendascii
      movwf  FSR

      movlw  xfercnt    ;# of ASCII represented received bytes to xfer
      addlw  xfercnt    ;x2
      addlw  h'3'       ;plus 2 start character "G" and newline character at end
      movwf  charcnt
;;set up registers in bank 1
        bsf    STATUS,RP0  ;point to bank 1
        movlw  h'8'
        movwf  TRISA       ;RA3 input, RA2-0 output
        movlw  h'10'
        movwf  TRISB       ;RB7-5,3-0 output, RB4 input
        movlw  b'00001100' ;set up timer option for internal clock, prescale-->watchdog/16
        movwf  OPTION_REG  ;port B pullups enabled
        bcf    STATUS,RP0  ;point back to bank 0
;;done setting up registers in bank 1, back to bank 0
        bsf    _RS232TX  ;default is mark mode
        call   gen125khz

;start the test transmission
sendA
        movf   INDF,w
        movwf  TXchar
        movlw  d'8'
        movwf  bitcnt
       ;stop bit last
        bsf    _RS232TX
        call   TX_RS232    ;stop bit = 3Ti


        call   ti17        ;burn 17Ti (includes the 2Ti for the call)
        ;start bit first
        bcf    _RS232TX
        call   TX_RS232
        call   ti17       ;burn 17Ti (includes the 2Ti for the call, adjusts the bit timing)
sendchar
        btfsc  TXchar,0    ;1Ti
        goto   setbit      ;3Ti
        bcf    _RS232TX
        goto   nextbit
setbit
        bsf    _RS232TX    ;4Ti
nextbit
        call   TX_RS232    ;6Ti
        rrf    TXchar,f    ;7Ti
        call   ti10        ;17Ti
        decfsz bitcnt,f    ;18Ti
        goto   sendchar    ;20Ti
       ;stop bit last
        bsf    _RS232TX
        call   TX_RS232    ;stop bit = 3Ti


      incf   FSR,f      ;1
      decfsz charcnt,f  ;2
      goto   inalpha    ;4
      movlw  d'255'
      movwf  charcnt
      movlw  d'10'
      movwf  bitcnt
waiting
      call   ti17
```

```
      decfsz charcnt,f
      goto   waiting
      decfsz bitcnt,f
      goto   waiting
      goto   seekinit
inalpha
      call   ti10
      goto   sendA


;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;subroutine--RS232 bit timing & 125 KHz voltage inverter maintenance
;;            baud rate set to 9600 bps--this is a bit time of 104 usec
;;            Timing for this subroutine: to104 loop is 5.605 usec, additional setup
;;                                        overhead is 1.77 usec. If do 17 to104 loops,
;;                                        that leaves 5.844 usec to make up in the calling
;;                                        routine to meet 104 usec target. 5.844= 19.8 Ti
;;                                        (20 Ti)
;;                                        Note that 5.844 is not evenly divisible by the
;;                                        instruction cycle time. Need to save one
;;                                        instruction every 5th bit sent--w/ the stop & start
;;                                        bit overhead, easier to save 2 extra instructions
;;                                        every character sent (10 bits)
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;
TX_RS232
        movlw  d'17'    ;time out 104 usec, Ti=295 nsec
        movwf  wait
to104
        movlw  invmask   ;flip voltage inverter bit
        xorwf  _RS232,f
        movlw  d'4'
        movwf  delay
wait4usec
        decfsz delay,f     ;4 usec is half inverter clock period
        goto   wait4usec
        decfsz wait,f
        goto   to104
        movlw  invmask
        xorwf  _RS232,f
        nop
        nop
        nop
        return


;;=============================================================================


;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;subroutine--generates 128 cycles at ~125 KHz for the RS232 voltage inverter
gen125khz
        movlw  d'128'
        movwf  cycle_cnt
next125
        bsf    _125KHZ
        movlw  d'4'
        movwf  delay
highside
        decfsz delay,f
        goto   highside
        bcf    _125KHZ
        movlw  d'4'
```

```
        movwf  delay
lowside
        decfsz delay,f
        goto   lowside
        decfsz cycle_cnt,f
        goto   next125
        return
;;end gen125khz
subroutine;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;subroutine-ti17: burn 17 Ti--includes the 2Ti to call this subroutine
;;           ti15: burn 15 Ti, including call
;;           ti10: burn 10 Ti, including call
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
ti17
        movlw  d'3'     ;1
        movwf  delay    ;2
burn9
        decfsz delay,f
        goto   burn9    ;11
        clrwdt          ;12
        nop             ;13
        return          ;15+2 for call ti17=17Ti

ti15
        movlw  d'3'     ;1
        movwf  delay    ;2
burn9Ti
        decfsz delay,f
        goto   burn9Ti  ;11
        return          ;13+2 for call ti15=15Ti

ti12
      nop
      clrwdt
ti10
        goto   dly1      ;2Ti
dly1
        goto   dly2      ;4Ti
dly2
        goto   leaveti10 ;6Ti
leaveti10
        return           ;8Ti+2Ti=10Ti



;=================
;;initialization
;=================
init
        ;1st set up the I/O configuration--note that setting PORTB 7,6,5,4,0 as outputs disables
        ;them as external interrupt sources. In this application PORTB-4 is utilized as an
        ;external interrupt source upon change of state. All other external interrupt sources are
        ;set as outputs to disable them as interrupts.

;;set up registers in bank 1
        bsf    STATUS,RP0  ;point to bank 1
        movlw  h'8'
        movwf  TRISA       ;RA3 input, RA2-0 output
        movlw  h'10'
        movwf  TRISB       ;RB7-5,3-0 output, RB4 input
        movlw  b'00001000' ;set up timer option for internal clock, no prescaler
```

```
        movwf  OPTION_REG  ;port B pullups enabled
        bcf    STATUS,RP0  ;point back to bank 0
;;done setting up registers in bank 1, back to bank 0
      movlw  HIGH isr
      movwf  PCLATH      ;setup for calculated goto's dependent on context when entering
                              ;isr
;=====================================================
;;initialization for sync field search- done @ turn on & after data recovery complete (or failed)
;=====================================================
seekinit
        clrwdt
      movlw  d'19'
      movwf  bitcnt    ;clear the bit storage field
      movlw  recvbits
      movwf  FSR
clrbits
      clrf   INDF
      incf   FSR,f
      decfsz bitcnt,f
      goto   clrbits


        movlw  recvbits
        movwf  FSR        ;start of the received bits field
      movf   PORTB,w ;read PORTB before clearing INTCON to be sure RBIF=0
      clrf   INTCON
      clrf   TMR0
;================================================================================
; From here on, the w register represents the PCL offset when answering the isr.
; It is to be used for no other purpose until interrupts are disabled.
;================================================================================
      movlw  d'0'
      clrf   PCLATH
      bsf    INTCON,RBIE  ;enable portB change interrupt enable
      bsf    INTCON,GIE   ;global interrupts are now enabled.


;====================
;;tag word search
;====================
;The main loop monitors the T0IF flag to detect successfully received word (subject to
;checksum test). Tag word processing is isr driven. A calculated goto method is used for
;position context in tag word for speed. FOR THIS REASON, THE W REGISTER CANNOT BE USED
;BY THE MAIN LOOP! If the main loop detects a timer overflow, the w register is cleared to
;return processing to first sync edge search.
;Also, expect recvbits area to be @ 40h-52h while receiving data. The ptr will be tested to
;determine this bitwise (because w can't be used in the main loop).
;============================================================================================
seeksync
      bcf     INTCON,RBIE
      movlw   d'0'    ;calculated goto offset for 1st sync edge processing
      clrf    PCLATH
      clrf    FSR     ;FSR = 0 to indicate not gathering bits
      bsf     INTCON,RBIE
      bcf     INTCON,T0IF
main
        clrwdt
      btfsc   FSR,6
      goto    datamain   ;receiving data, monitor progress
      btfsc   INTCON,T0IF
      goto    seeksync   ;if TMR0 overflows w/o receiving bits, seeksync
        goto    main
;check for done receiving bits using TMR0 overflow as indicator. Also test for overflow from
;proper bit storage area for runaway condition (non tag noise tripping comparator)
datamain
```

```
      clrwdt
      btfsc   INTCON,T0IF
      goto    calc_checksum ;if timer overflows, calculate checksum of received data
      btfsc   FSR,5         ;if bit 5 set, FSR > 5fh and has overrun its proper area.
      goto    seeksync      ;search for sync.
      goto    datamain
;Data received at this point. Two processing tasks remain:
;1- the framing '0' bits must be removed from the received 14 data bytes and 16 bit checksum
;2- the checksum of the 14 data bytes must be calculated and compared to the received
;   16 bit checksum
;If checksums match, transmit data over RS232 link.

calc_checksum
      clrf    INTCON
clrgie
      bcf     INTCON,GIE
        btfsc   INTCON,GIE   ;make sure it's clear before proceeding
      goto    clrgie
      movf    PORTB,f
      clrf    INTCON       ;disable all interrupts while processing received data
;remove the framing '0' bits by bit shifting the data array left until all framing 0s are
;shifted out

      movlw   d'17'
      movwf   bitcnt
      movwf   shiftcnt
shiftout
      movlw   recvbits+d'17'
      movwf   FSR
roll_left
      rlf     INDF,f
      decf    FSR,f
      decfsz  shiftcnt,f
      goto    roll_left     ;rotate left shiftcnt # of bytes
      decfsz  bitcnt,f
      goto    next_RL
      goto    framestripped
;bit shift left through the array (successively 1 byte less each time)
next_RL
      movf    bitcnt,w
      movwf   shiftcnt
      goto    shiftout
framestripped

;1st check for all 0s in data--This is an illegal combination
      movlw   recvbits
      movwf   FSR
      movlw   d'14'
      movwf   bitcnt
zerotest
      movf    INDF,w
      btfss   STATUS,Z
      goto    nonzero
      decfsz  bitcnt,f
      goto    zerotest
      goto    seekinit     ;all zeros received. Ignore the message
nonzero
;do 16 bit checksum of first 14 bytes received. It should match the last 2 bytes received.
      movlw   recvbits
      movwf   FSR
      movlw   d'14'
      movwf   bitcnt
      clrf    recv_csumlo
      clrf    recv_csumhi
sumbytes
```

```
      movf    INDF,w
      addwf   recv_csumlo,f
      btfsc   STATUS,C
      incf    recv_csumhi,f  ;carry into high byte as necessary
      incf    FSR,f          ;point to next data byte
      decfsz  bitcnt,f
      goto    sumbytes
;now compare the received checksum w/ the calculated checksum. Transmit data if they match.
      movf    recv_csumhi,w
      subwf   INDF,f
      btfss   STATUS,Z
      goto    seekinit
      incf    FSR,f         ;point to received checksum LSB
      movf    recv_csumlo,w
      subwf   INDF,f
      btfss   STATUS,Z
      goto    seekinit
;message passes checksum. Convert to ASCII and transmit.
;now convert to ASCII form
      movlw    recvbits
      movwf    ptr1       ;keep track of where in conversion
      movlw    sendascii
      movwf    ptr2
      movwf    FSR
      movlw    "G"
      movwf    INDF
      incf     ptr2,f
      incf     FSR,f
      movwf    INDF      ;double "G" to indicate start
      incf     ptr2,f    ;next ascii character
      movlw    xfercnt  ;how many bytes to convert to ASCII
      movwf    bitcnt
      movlw    h'4'
      movwf    PCLATH   ;set up PCLATH for lookup table
asciiconv
      movf     ptr1,w
      movwf    FSR
      swapf    INDF,w
      andlw    h'f'       ;isolate the MSN
      call     hex2ascii
      movwf    temp       ;hold the ASCII character
      movf     ptr2,w
      movwf    FSR
      movf     temp,w     ;store ASCII representation of received byte MSN
      movwf    INDF
      incf     ptr2,f     ;advance ASCII ptr
      movf     ptr1,w     ;back to received bytes
      movwf    FSR
      movf     INDF,w
      andlw    h'f'       ;isolate the LSN
      call     hex2ascii
      movwf    temp
      movf     ptr2,w
      movwf    FSR
      movf     temp,w     ;store ASCII representation of received byte LSN
      movwf    INDF
      incf     ptr2,f     ;advance ASCII ptr
      incf     ptr1,f     ;advance received byte ptr
      decfsz   bitcnt,f
      goto     asciiconv
;done data conversion, now indicate newline before sending
      movlw    "\n"       ;newline character
      incf     FSR,f
      movwf    INDF
```

```
;cleared for RS232 transmission
      goto     alphabet

;hexadecimal to ASCII conversion table
      org      h'3ff'
hex2ascii
      addwf    PCL,f
      retlw    "0"   ;ascii 0
      retlw    "1"   ;ascii 1
      retlw    "2"   ;ascii 2
      retlw    "3"   ;ascii 3
      retlw    "4"   ;ascii 4
      retlw    "5"   ;ascii 5
      retlw    "6"   ;ascii 6
      retlw    "7"   ;ascii 7
      retlw    "8"   ;ascii 8
      retlw    "9"   ;ascii 9
      retlw    "A"   ;ascii A
      retlw    "B"   ;ascii B
      retlw    "C"   ;ascii C
      retlw    "D"   ;ascii D
      retlw    "E"   ;ascii E
      retlw    "F"   ;ascii F

        end
```

13.56 MHz Reader Reference Design for the MCRF 450/451/452/455 Read/Write Devices

1.0 INTRODUCTION

The anti-collision interrogator in the DV103005 Development Kit is for Microchip Technology Inc.'s 13.56 MHz RFID devices (MCRF35X/360 and MCRF45X devices). The interrogator is used in conjunction with the RFLab 3.2 or above. User must select device type in the RFLab Menu Bar for either MCRF35X/360 or MCRF45X device.

In the MCRF35X/360 mode, the interrogator transmits 13.56 MHz carrier signal continuously and receives tag's responses. This is often called "tag talks first" (TTF). The interrogator is working as the reader in the DV103003 kit that is for read only device (MCRF35X and MCRF360).

In the MCRF45X mode, the interrogator sends commands for reading or writing block data. Interrogator uses amplitude modulation for the commands. To initiate communications, the interrogator sends specially timed gap pulses: FRR (fast read request) and FRB (fast read bypass). These pulses consist of 5 gaps within 1.575 ms time span. Each gap pulse is 175 µs wide with 100% modulation depth. Gap means an absence of RF field. See Figures 4-3 thru 4-8 in the MCRF45X data sheet for details.

1-of -16 PPM (pulse position modulation) is used for data and commands such as read/write command for block data, command to set/clear TF (tag talks first) and FR (fast read) bits, and command for end process. The 1-of-16 PPM signal consists of one gap pulse within 2.8 ms time span for a normal mode and 160 µs for a fast mode. The gap's position within 16 possible locations determines its representation for hex value. See Figure 4-9 in the MCRF45X data sheet (DS40232) for details.

The interrogator also sends a time reference pulse before the commands and data. This time reference signal consists of three gap pulses within 2.8 ms time span for a normal mode and 160 µs for a fast mode. See Figure 4-10 in the MCRF45X data sheet for details. Figure 1-1 shows the read/write pulse sequence between the interrogator and device.

The demo interrogator communicates with the device in conjunction with the RFLab.

The RFLab is a menu driven software package. Once the "MCRF450" - "Continuous" - "Run" menus are selected, the interrogator transmits FRR command continuously. Tags responds to the FRR command with a maximum of 160 bits of data including its unique ID number (32 bits). To read or write a specific memory block, users must select the tag ID and block number.

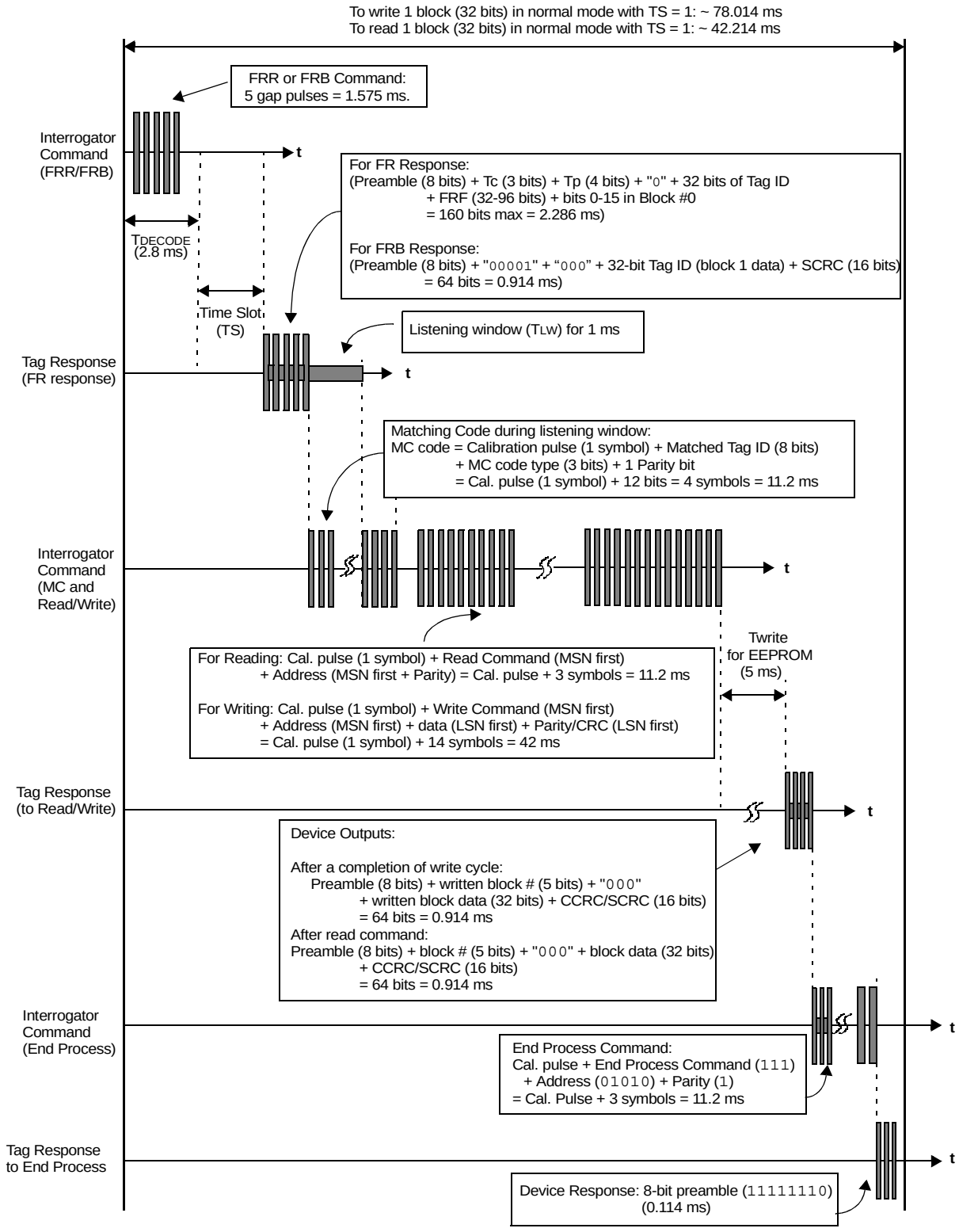
The demo interrogator along with the RFLab included in the DV103005 kit is made as a reference material for various applications. The demo interrogator is designed for a general purpose utilizing all possible features shown in the data sheet. Both firmware and schematics can be modified for each individual applications.

The interrogator uses two PICmicro® microcontrollers (MCUs) to communicate with a host computer, to send commands and data to the tag, and to receive and process the data from the tag.

The U17 includes the anti-collision algorithm shown in Figure 4-1 of the MCRF45X data sheet. It controls all functions of the interrogator except decoding the received Manchester data which is done by the U14.

The circuit is designed for medium read/write range applications (about 15" with 2" x 2" tag). The circuit can be optimized for lower cost, or modified for long-range applications. Electronic copies of the PICmicro MCU source codes, schematics and Bill of Material (BOM) are included in the CD.

FIGURE 1-1: READ/WRITE PULSE SEQUENCE



2.0 INTERROGATOR CIRCUITS

The interrogator circuit consists of (1) transmitting, (2) receiving and (3) command control/data processing sections.

2.1 RF Transmission Section

U6:A and 13.56 MHz crystal form a crystal oscillator and output a 13.56 MHz signal. The output signal is fed into pin 1 of U7. The input signal on pin 2 of U7 is coming from U17 (Master Microcontroller). The following is the output of U17 for pin 2 of U7.

- MCRF45X mode: Modulation signal for commands and block data for writing.
- Stand by mode: Logic "HIGH".
- MCRF35X/360 mode: Logic "HIGH".

Therefore, U7 outputs (a) a modulated RF signal (for command or write data) or (b) continuous RF signals during the stand by and MCRF35X/360 operation. The output signal of the U7 is fed into the gate of RF power amplifier U8 through U6:D, E and F. Splitting the output of U6:C using U6:D, E and F is helpful for preventing excessive heat on U6.

U4 is an adjustable voltage regulator and supplies the DC power supply voltage for U8. The U4 is controlled by U17 through U16 (DAC) and U3. The main idea of using the adjustable voltage regulator is to adjust the RF output signal level of U8. The power level is adjusted by the following procedure in the RFLab menu:

"Configure" -> "Carrier Strength"

User can select the "Carrier Strength" from 0% – 100% (from the above menu). Default is set to 100%. The interrogator outputs the maximum power level at this setting.

RFLab sends the Carrier Strength information to U17 which adjusts U4's output voltage through U16 and U3.

This corresponds to about 12.37 VDC at pin 2 of U4 for the 15 VDC input voltage.

The purpose of adjusting the carrier signal level is to reduce a possible near-field problem which may result in an irregular clock rate of the RFID device. This is due to an excessive input voltage to the device when the tag is placed too close to the reader antenna. In this case, the output power level from the interrogator should be decreased. However, for a longer read range, it is often necessary to output higher power level so that it can detect tags in the far range.

Adjusting the carrier signal level is an optional choice. Therefore, the circuit components (U16, U3 and U4) associated with this feature can be easily removal. In this case, +15 VDC or 9 VDC should be directly applied to L9 for U8.

The RF output voltage from U8 is fed into antenna circuit formed by C1, C2, C3, C4, C5 and antenna coil L.

The demo unit has three different sizes of antenna. Each one has one turn inductor along the edge of the PCB board. The metal trace is embedded inside the PCB.

Figure 2-1 shows the antenna circuit. The impedance of LC circuit is given by:

EQUATION 2-1:

$$Z(\omega) = \frac{\frac{1}{C_4}\left(j\omega L + \frac{1}{j\omega C_S}\right)}{-\omega^2 L + \left(\frac{1}{C_S} + \frac{1}{C_4}\right)}$$

where

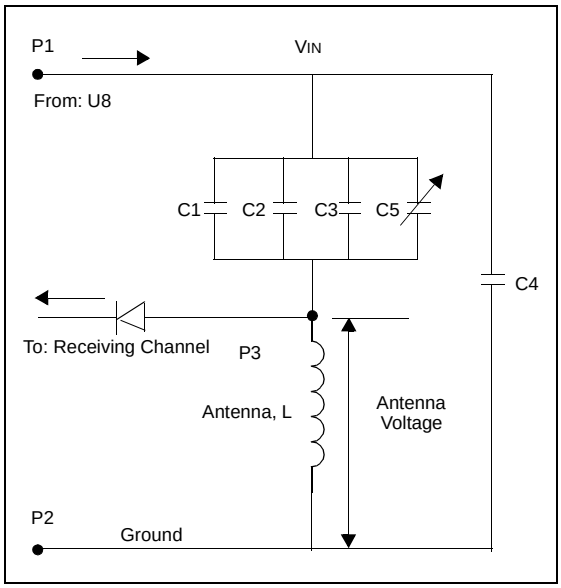
$C_S = C_1 + C_2 + C_3 + C_5$

$\omega = 2\,\pi\,f$

f = output carrier frequency

The resonant frequency of the antenna circuit in the interrogator is given by solving the impedance equation in Equation 2-1. In Equation 2-1, the impedance Z(ω) has poles and zeroes. The poles are found at the condition when the denumerator goes to zero and the zeroes are found when the numerator goes to zero. The poles result in a maximum impedance, since the denumerate goes to zero. Therefore, the frequencies at the poles are the parallel resonant frequencies. The zeroes result in a minimum impedance since the number goes to zero. Thus, the frequencies at the zeroes are series resonant frequencies.

FIGURE 2-1: ANTENNA CIRCUIT



The resonant frequencies by solving the poles and zeroes are:

EQUATION 2-2:

$$f_{series} = \frac{1}{2\pi\sqrt{LC_S}} = \frac{1}{2\pi\sqrt{L(C_1 + C_2 + C_3 + C_5)}}$$

and

EQUATION 2-3:

$$f_{parallel} = \frac{1}{2\pi\sqrt{L\left(C_S\left(1 + \frac{C_S}{C_4}\right)\right)}}$$

where

$C_S = C_1 + C_2 + C_3 + C_5$

Equation 2-3 is used for the antenna circuit of the interrogator in the DEV103005 kit.

The antenna voltage across the L is given:

EQUATION 2-4:

$$V_{Ant} = \frac{jX_L}{r + j(X_L - X_{C_S})} V_{in}$$

where

r = Ohmic resistance of L and C

$X_L = 2\ \pi\ f\ L\ (\Omega)$

$X_{C_S} = (2\ \pi\ f\ C_S)^{-1}\ (\Omega)$

V_{IN} = AC voltage at points between P1 and P2.

The antenna voltage measured between P3 and P2 contributes the radiating RF field from the antenna. The voltage is about 60 V_{PP} – 80 V_{PP}. C5 can be adjusted to get the maximum voltage across the antenna. The current that flows along antenna L generates magnetic fields.

Each interrogator unit may have a slightly different output parasitic capacitor. As a result, there will be a chance of tuning variation when the antenna is attached to the unit. This results in shorter read range. In this case, C5 in the circuit should be adjusted properly.

2.2 Receiving Section

The receiving section receives 70 kHz Manchester data from tag in the field. D1, C4 and R3 collectively form an envelope detector.

L1 and C3 forms a 70 kHz band pass filter. D4 and D2 are used to limit signal amplitude level which prevents U1:A going into a saturation condition. L3, C33 and C47 form a 13.56 MHz notch filter and by-pass the induced carrier signal into ground. FB1 is an RF choker that gives high attenuation to high frequency signal. U1:A is a gain amplifier that gives about 26 dB voltage gain. U1: B is a unit gain second-order high-pass filter. U1:C is a gain amplifier with about 29 dB voltage gain. U1:D is a unit gain second-order low-pass filter. U1:B and D result in a band-pass filter for the 70 kHz Manchester data.

U11:A, B, T1 and T2 circuits are used to find a midpoint of the input data voltage. The resulting average voltage, (V_P^+ + V_P^-)/2, is used as a reference voltage for the voltage comparator U2. The output of U2 is fed into the
PICmicro micrcontroller U17 for data decoding.

2.3 Command Control and Data Decoding Section

The interrogator uses two PICmicro MCUs (PIC16F876-20/SP) for the command controls, data decoding and communication with a host computer.

The U17 includes PIC-code routines to follow the device's read/write anti-collision algorithm as shown in Figure 4-1 in the data sheet. The U14 performs bit timing calculation for the received Manchester code.

The U17 does the following tasks:

a) Communicate with a host computer
b) Encode and transmit:
   FRR and FRB Commands
   Calculate/Send MC1 and MC2
   Read/Write/End Commands
   Calibration Pulse
   Data and CRC
c) Decode receiving data
d) Calculate CRC for transmitting data and receiving data. CRC look-up table is used for the calculation.
e) Give a received data stream to U14 for decoding of the Manchester data.

The flow charts of the PICmicro microcontroller routines for U14 and U17 are shown in AN760 (DS00760). The source codes are included in the CD.

Figure 2-2 shows the functional block diagram of the interrogator.

FIGURE 2-2: FUNCTIONAL BLOCK DIAGRAM OF DEMO INTERROGATOR

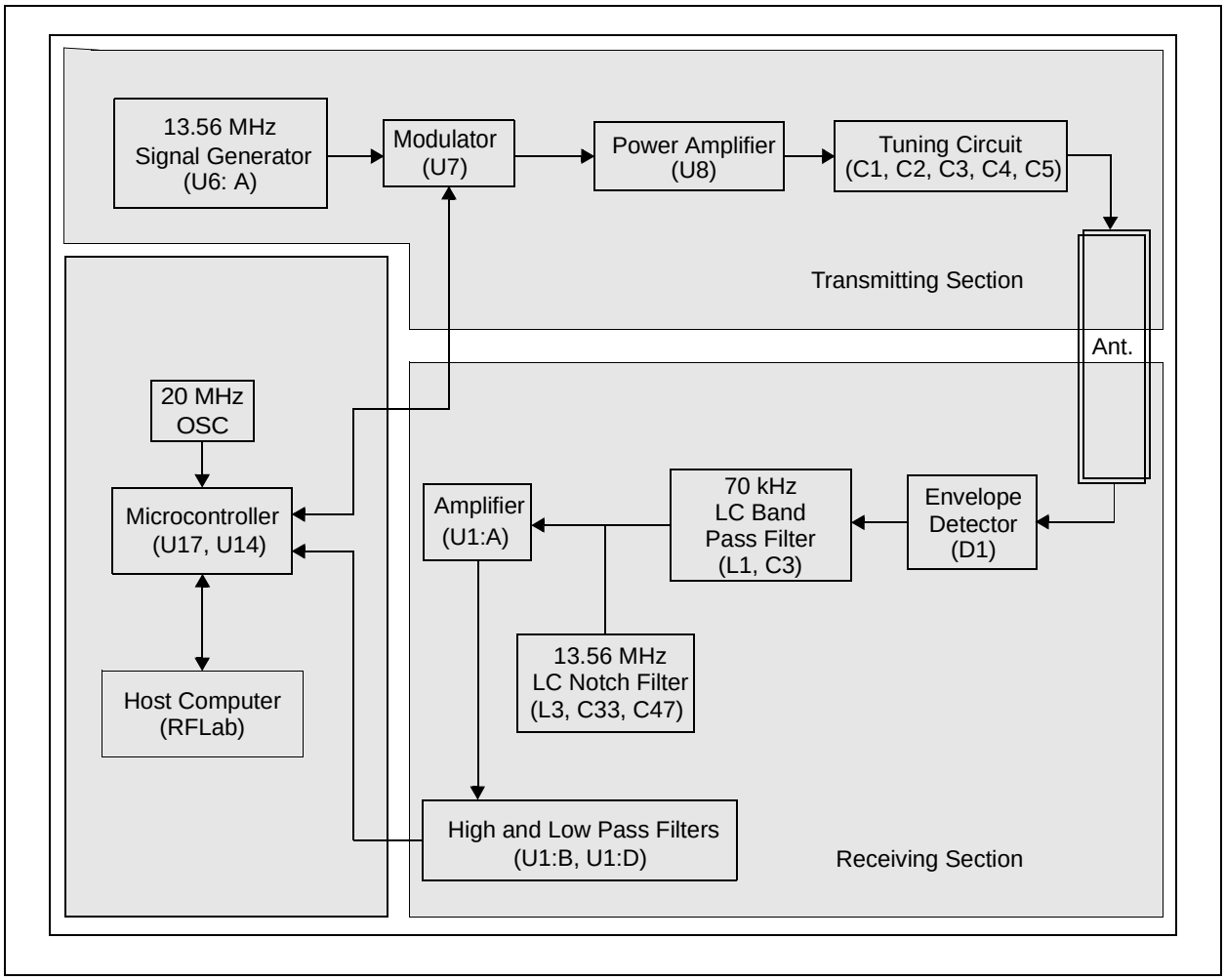


FIGURE 2-3: DATA SIGNAL WAVEFORMS FROM TAG

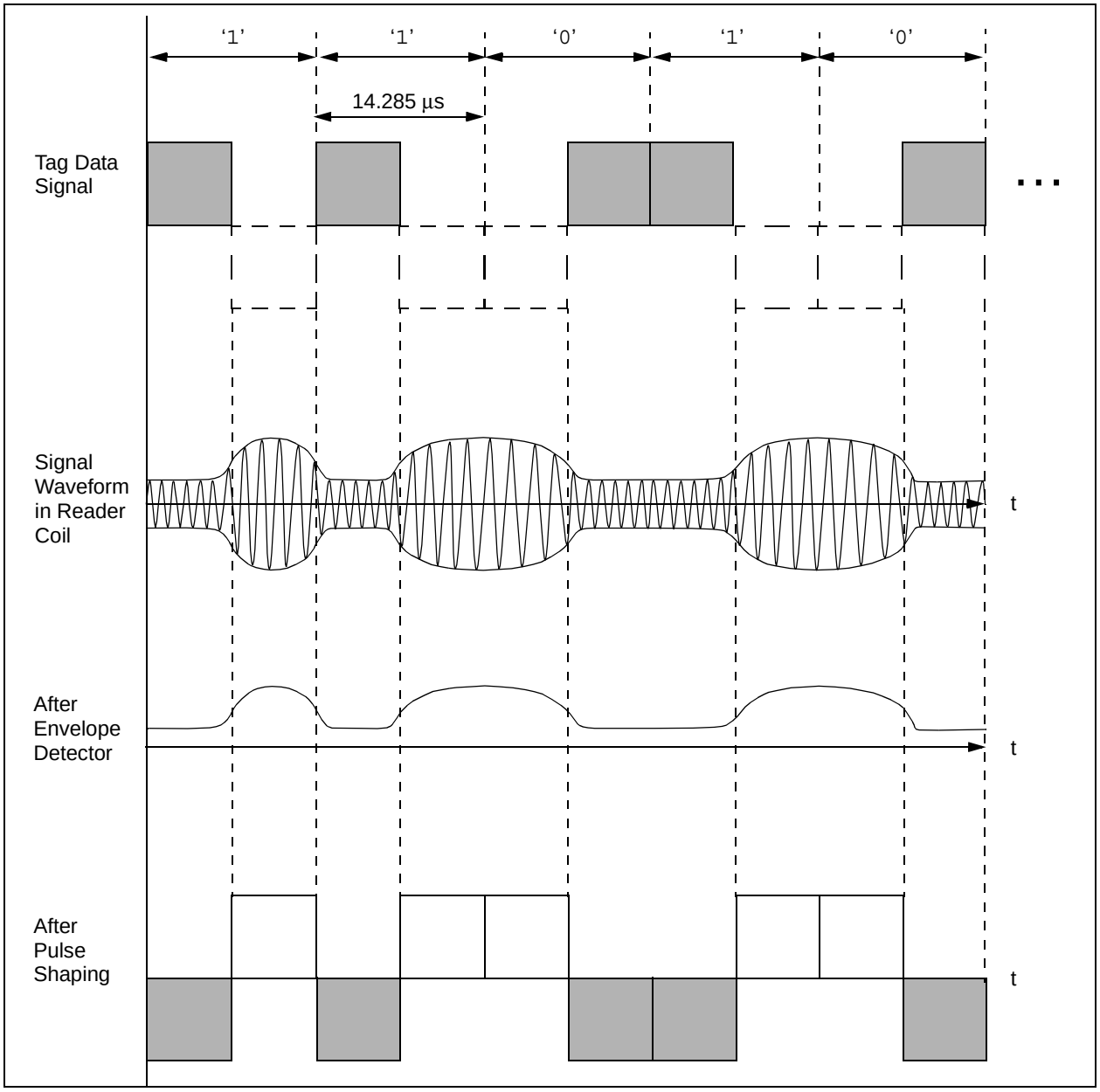
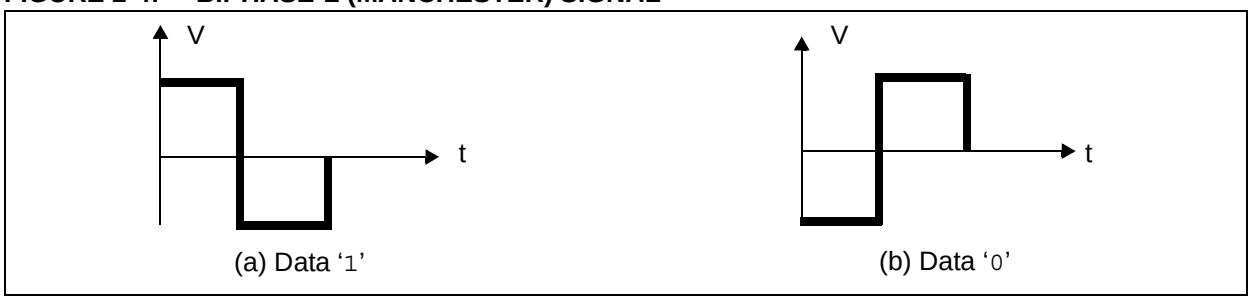
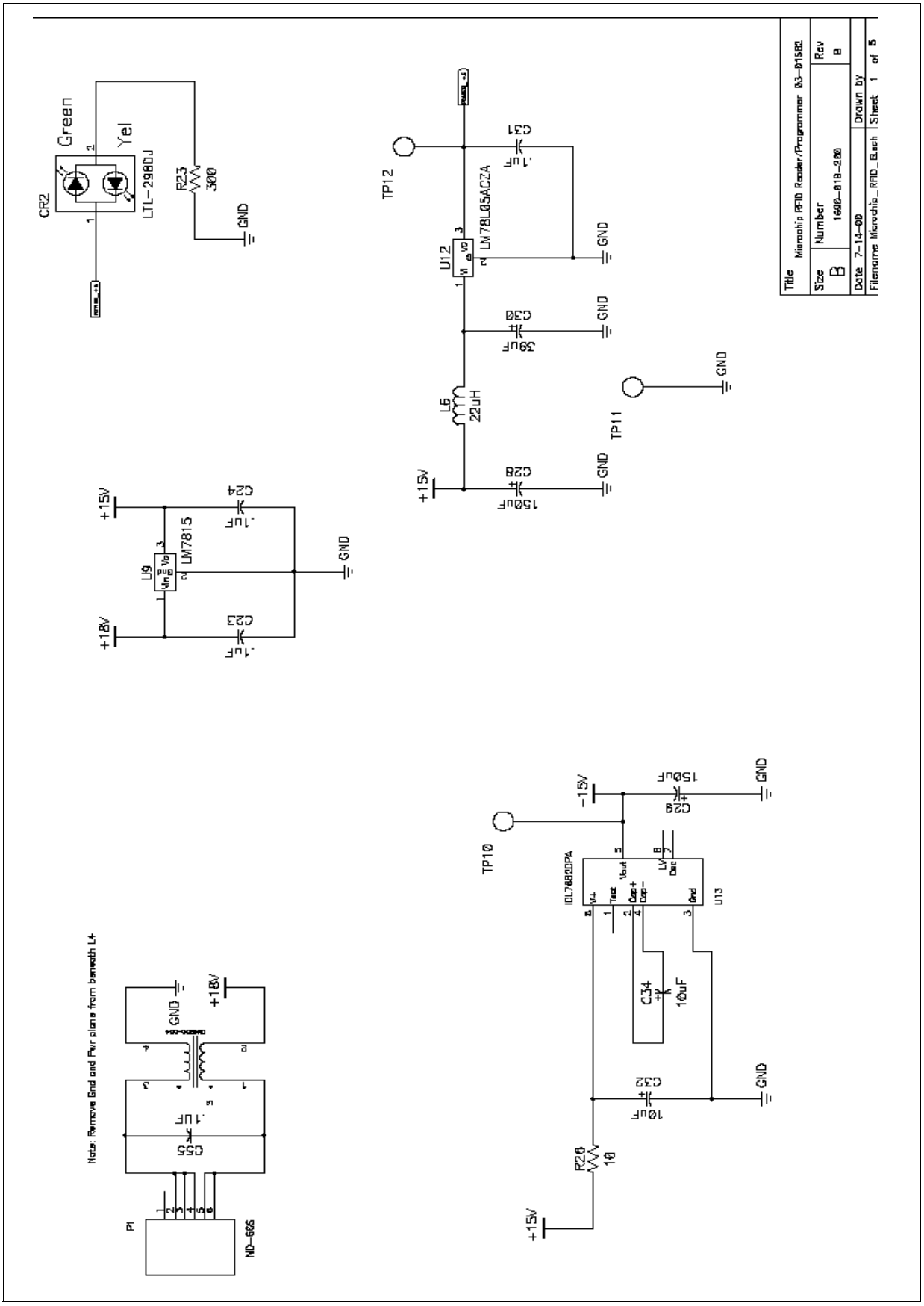
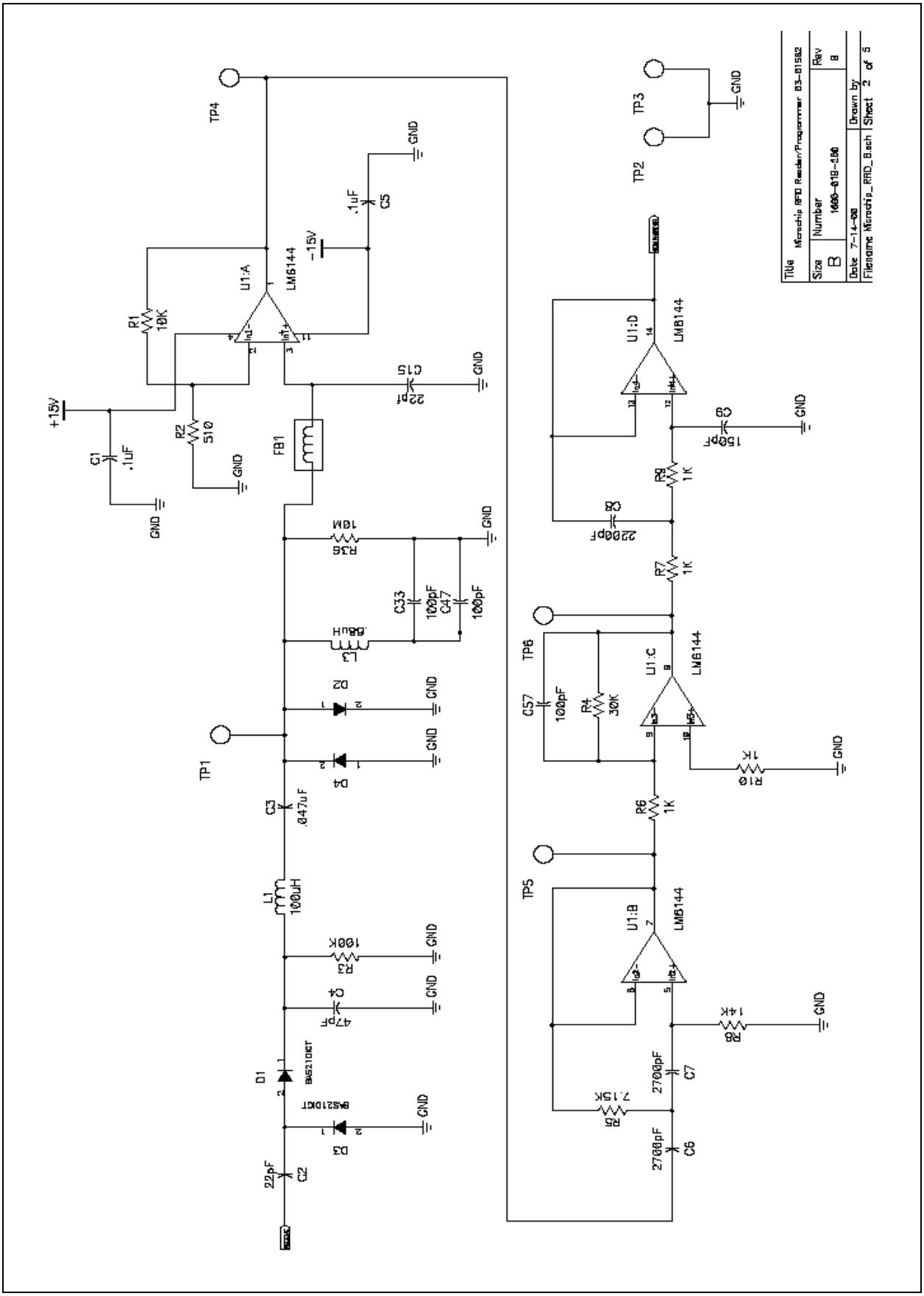
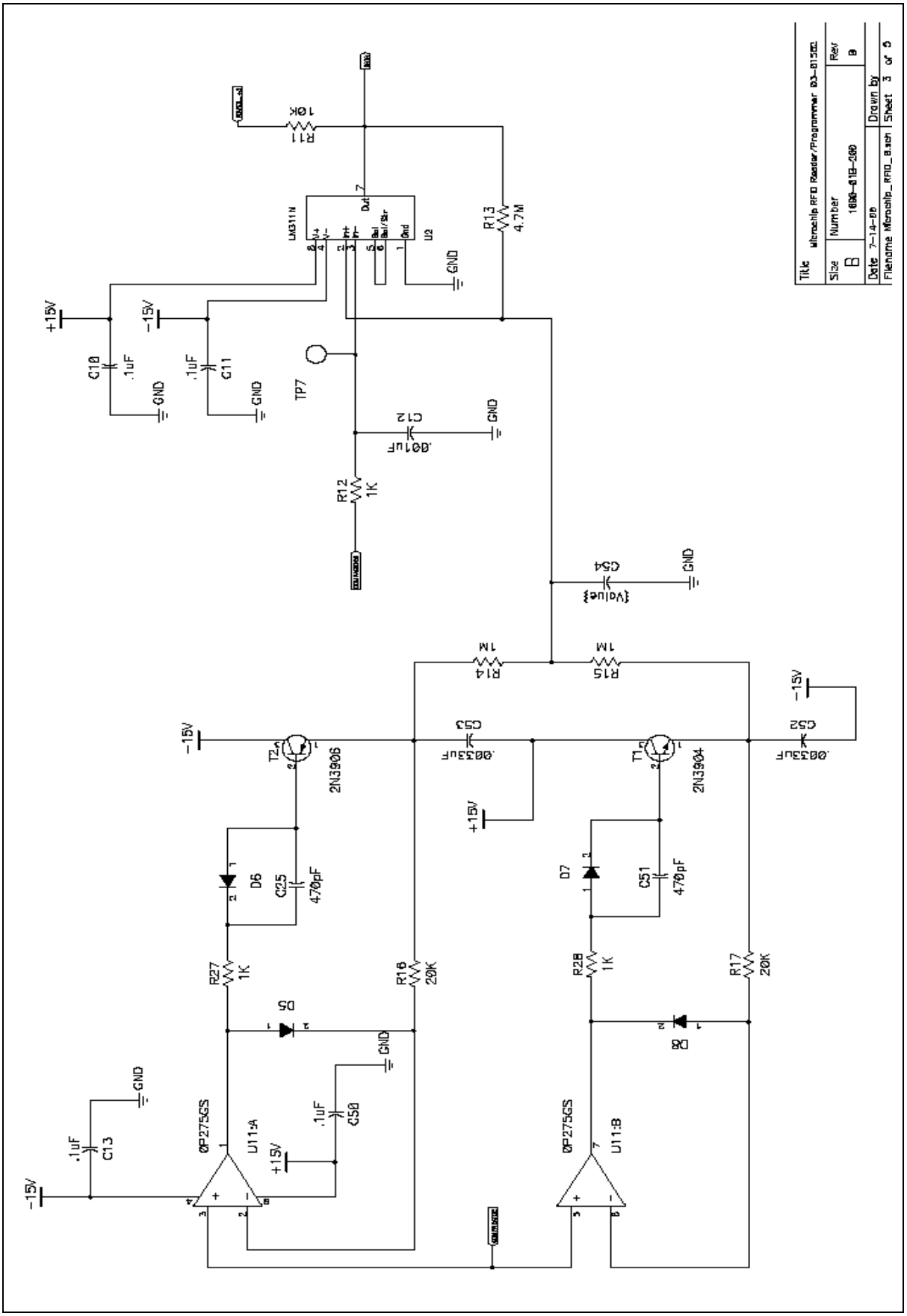


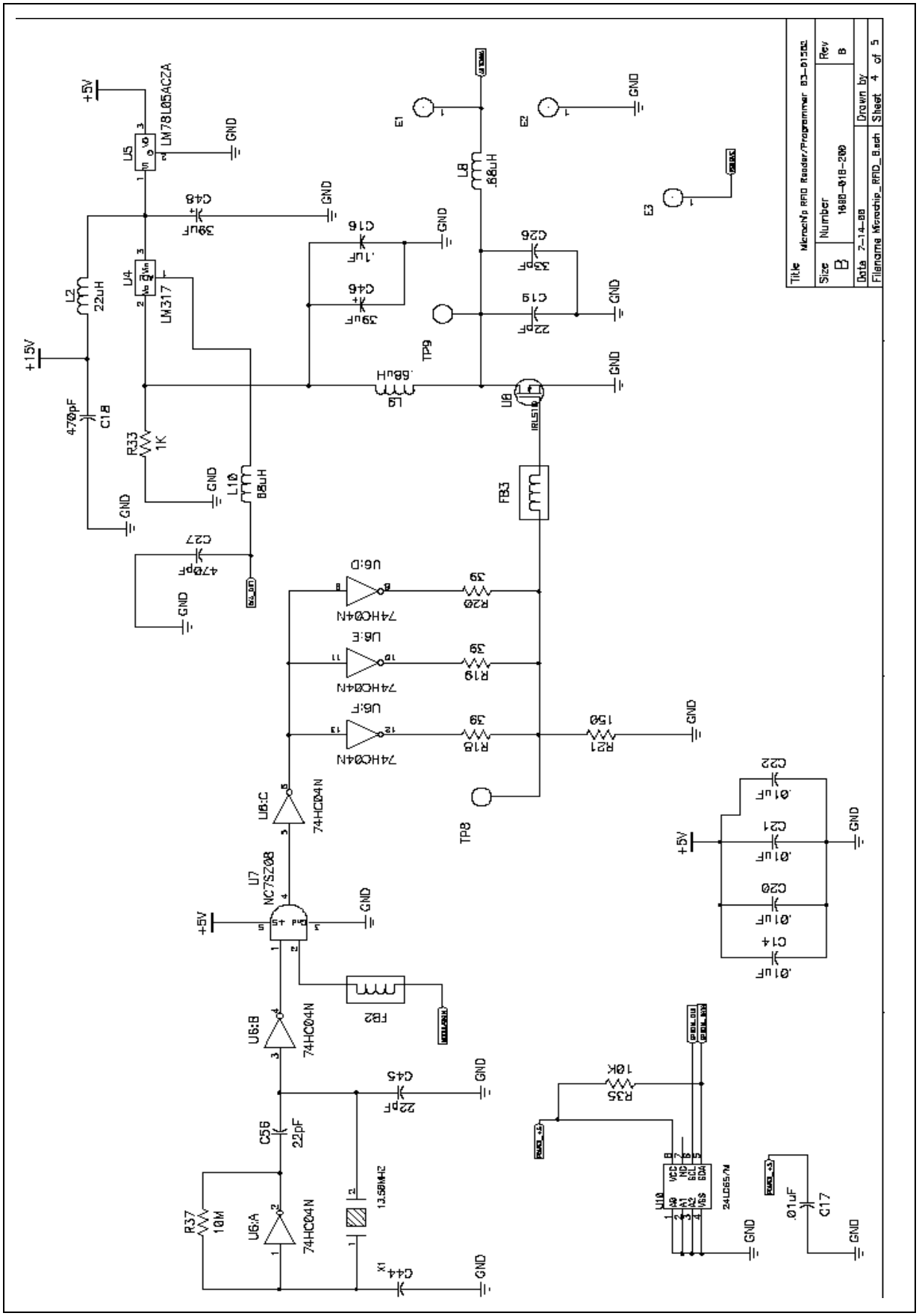
FIGURE 2-4: BIPHASE-L (MANCHESTER) SIGNAL

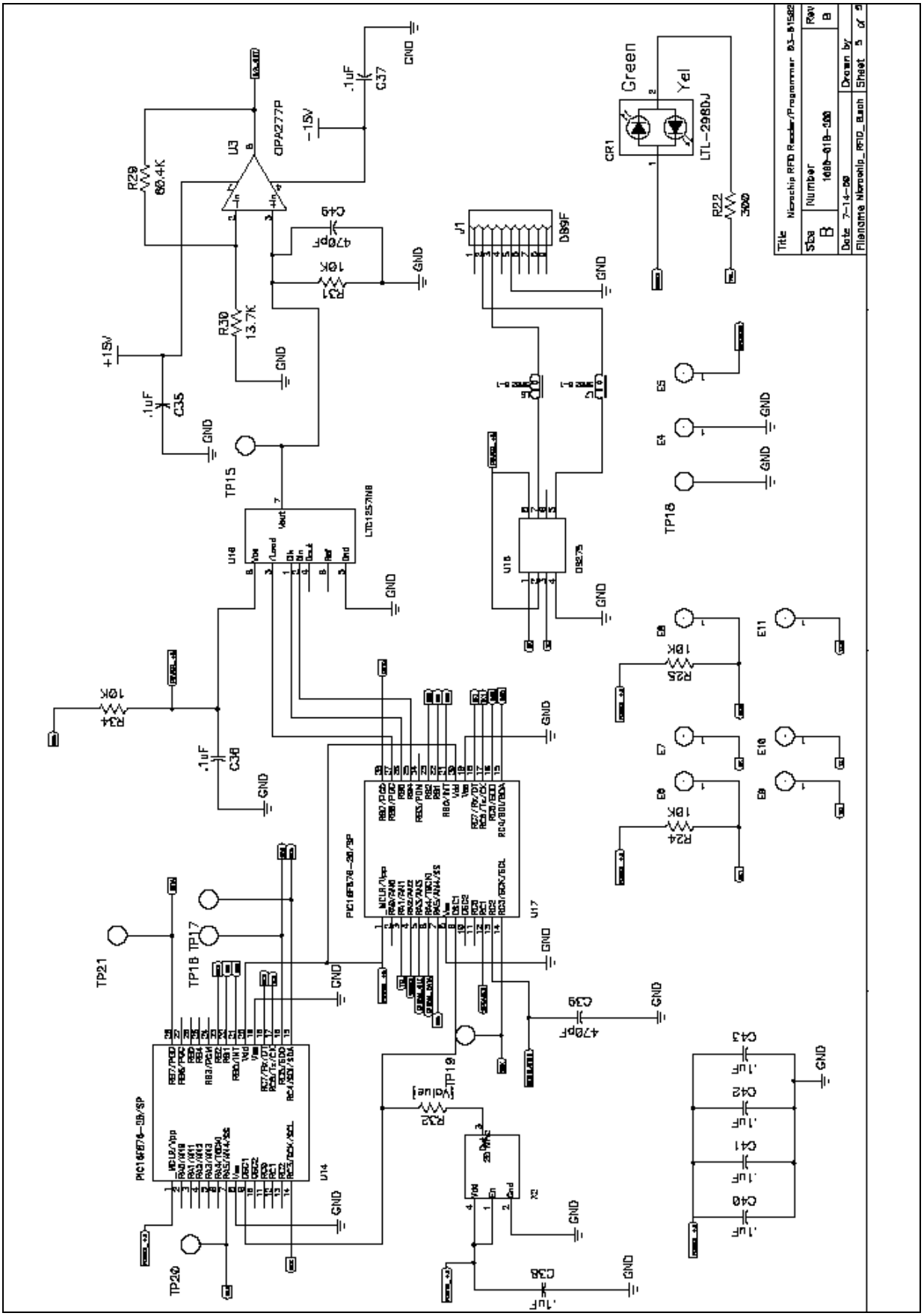


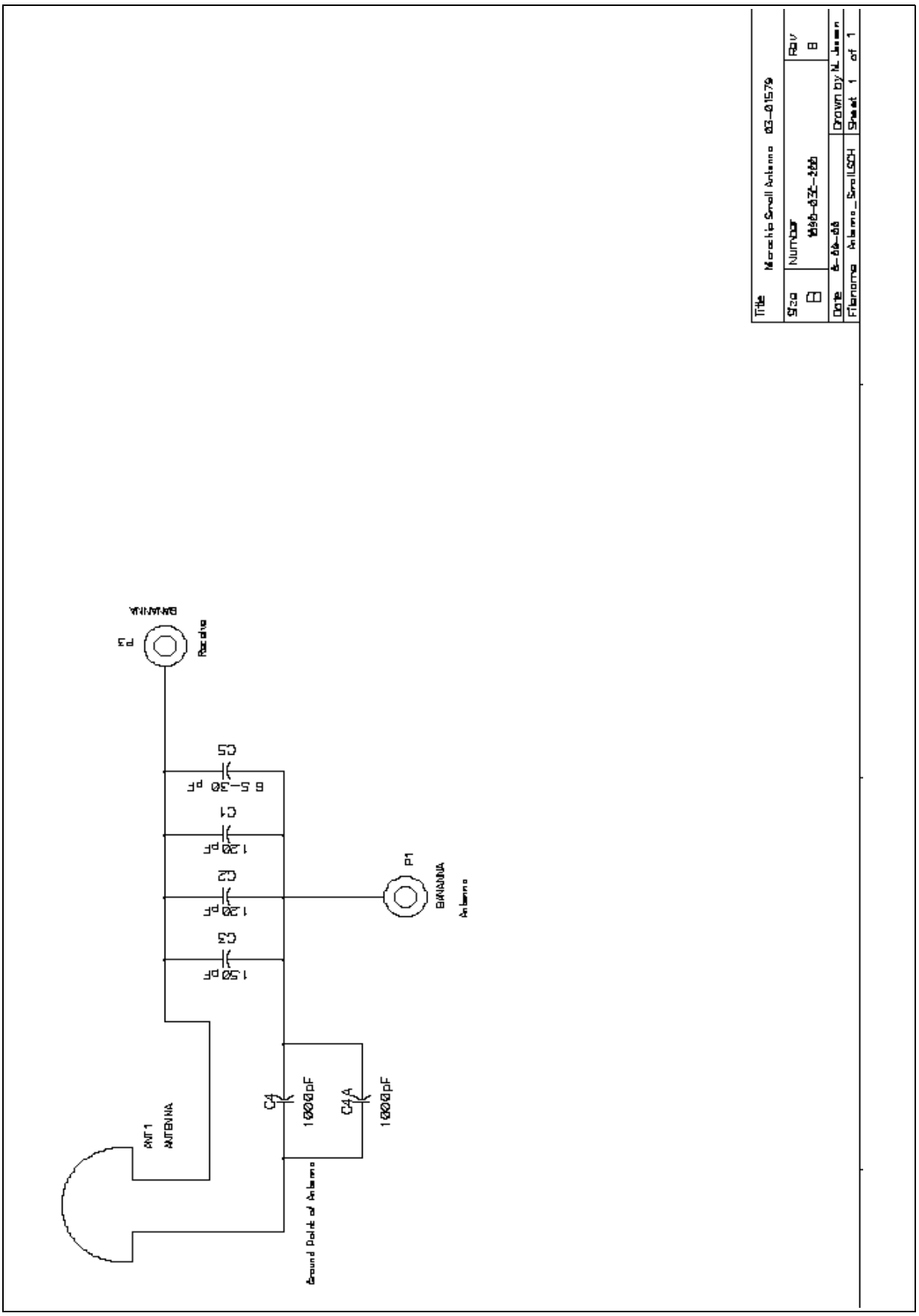

Green
Yel
CR2
LTL-298DJ
R23
300
GND
TP12
C31
.1uF
U12
LM78L05ACZA
C30
39uF
L5
22uH
TP11
C28
150uF
+15V
+18V
C24
.1uF
U9
LM7815
C23
.1uF
Title
Microchip RFID Reader/Programmer 03-01582
Size
B
Number
1600-018-200
Rev
B
Date
7-14-00
Drawn by
Filename Microchip_RFID_Flash
Sheet 1 of 5
TP10
-15V
C29
150uF
U13
IDL7680PA
C34
10uF
C32
10uF
R26
10
C35
.1uF
P1
ND-606
Note: Remove Gnd and Pwr plans from beneath L4

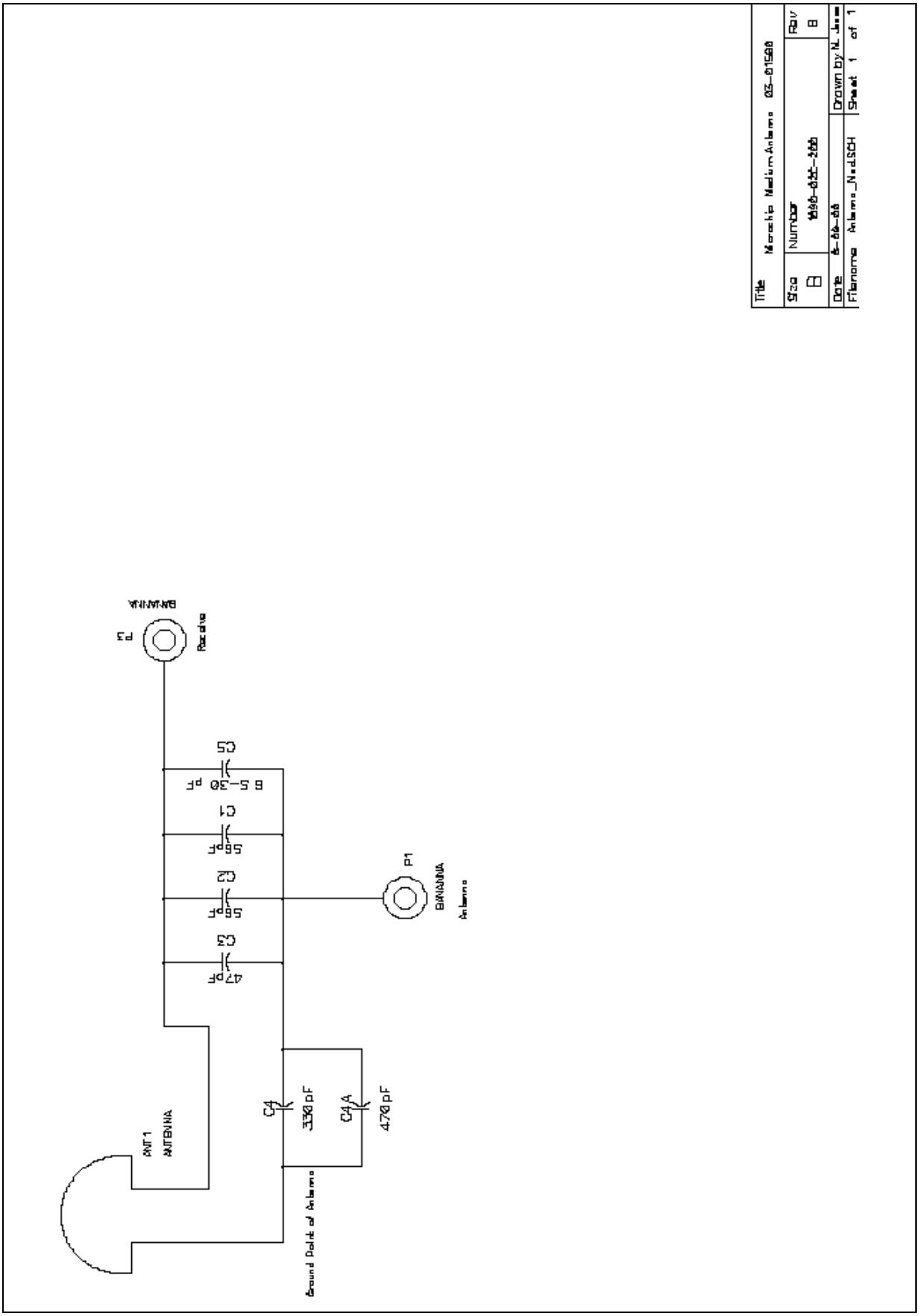


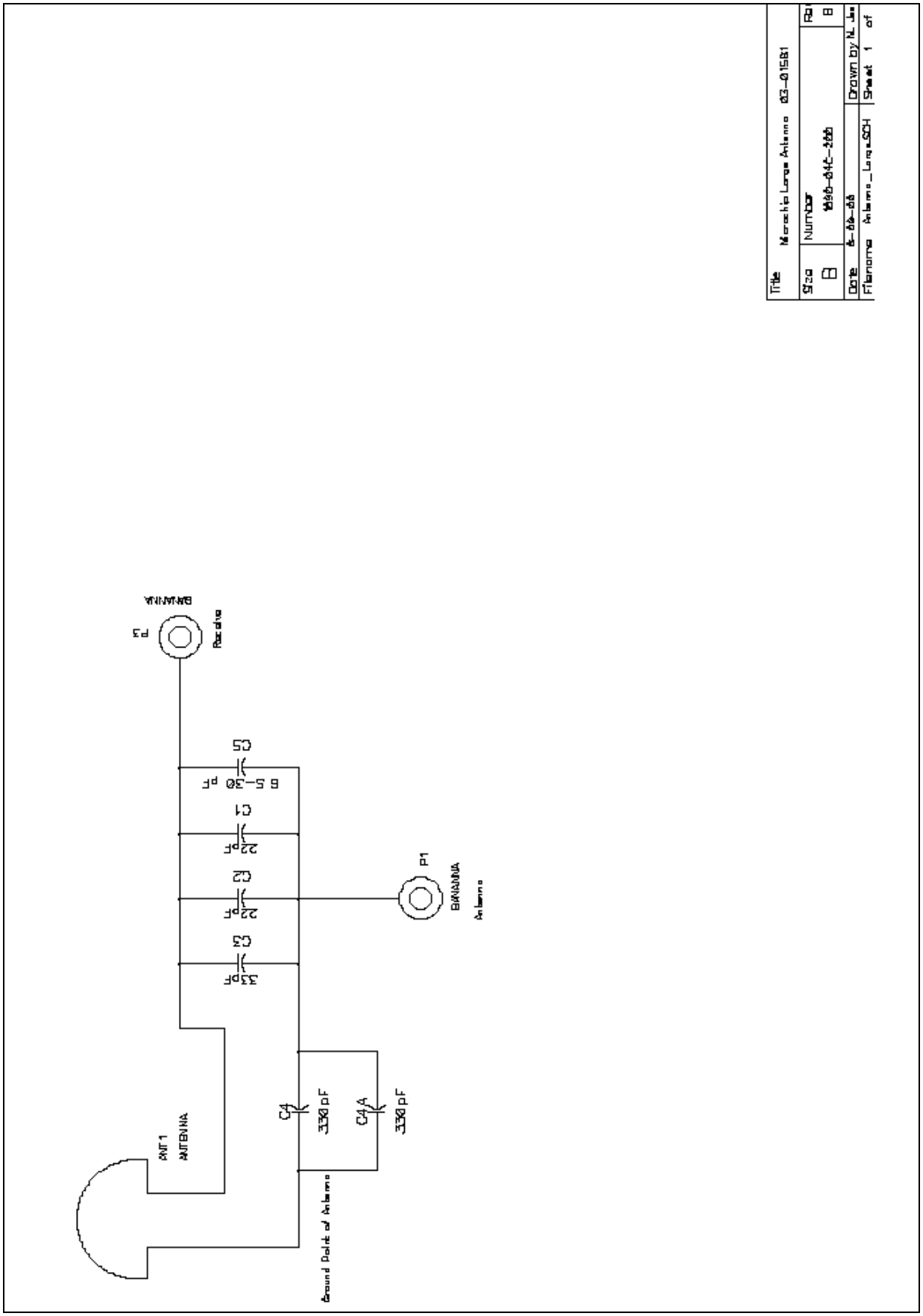

Title Microchip RFID Reader/Programmer 03-01502
Size B
Number 1060-010-000
Rev B
Date 7-14-00
Drawn by
Filename Microchip_RFID_B.sch
Sheet 3 of 5
10K
R11
LM311N
U2
R13
4.7M
GND
+15V
-15V
C10
.1uF
C11
TP7
C12
.001uF
R12
1K
C54
{Value}
1M
R14
R15
C53
.0033uF
C52
T2
2N3906
T1
2N3904
D6
C25
470pF
D7
C51
R27
1K
R16
20K
R28
R17
D5
D8
C13
C50
U11:A
U11:B
OP275GS




Title Microchip RFID Reader/Programmer
Size B
Number 1089-018-500
Rev B
Date 7-14-00
Drawn by
Filename Microchip_RFID_Bash
Sheet 5 of 5
U3
OPA277P
R29
80.4K
R30
13.7K
R31
10K
C49
470pF
C37
.1uF
-15V
+15V
C35
.1uF
GND
TP15
U18
LTC1257IN8
CR1
Green
Yel
LTL-2980J
R22
390
J1
D89F
U16
DS275
E5
E4
TP16
R25
10K
R24
10K
R34
10K
C36
.1uF
E8
E11
E7
E10
E9
E6
TP21
TP18
TP17
TP19
TP20
U17
PIC16F876-08/SP
U14
PIC16F876-08/SP
C39
470pF
R33
10K
X2
C38
.1uF
C43
.1uF
C42
.1uF
C41
.1uF
C40
.1uF




Title Microchip Medium Antenna 03-01508
Size B
Number 100-0XX-XXX
Rev B
Date 6-06-00
Drawn by N. Jones
Filename Antenna_Med.SCH
Sheet 1 of 1
P3
Receive
C5
8.5-30 pF
C1
56pF
C2
56pF
C3
47pF
P1
BANANNA
Antenna
C4
330 pF
C4A
470 pF
ANT1
ANTENNA
Ground Point of Antenna



Interface Control Document for the 13.56 MHz MCRF450/451/452/455 Anti-Collision Interrogator

SCOPE

This document specifies the external interface requirements for the MCRF45X and MCRF355/360 Reader/Writer. A description of the RS232 interface messages, their bit fields and meanings are described in this document.

Identification

This interface control document is applicable to the Microchip's 13.56 MHz RFID Reader/Writer.

System Overview

The RFID Reader/Writer will support both reading and writing of the MCRF355/360 and MCRF45X RFID devices. The RFID Reader/Writer will support communication for command and data via an RS232 interface using standard protocol settings.

Document Organization

This document is organized as follows:

- SCOPE: Identifies the scope of this document
- REFERENCE DOCUMENTS: Identifies any documents referenced by this specification by document number, revision and date
- EXTERNAL INTERFACES: Identifies the specific external electrical and mechanical interfaces for the Support Electronics for the PDE

REFERENCED DOCUMENTS

The following references are used for this document:

[1] EIA Standard RS-232-C

[2] RS-232A Specification

EXTERNAL INTERFACES

Electrical Interfaces

SERIAL COMPUTER INTERFACE

The RFID Reader/Writer will communicate with the external host computer via RS232 interface. The interface settings will be 19.2 Kbaud, 8 bits, no parity and one stop bit. All characters transmitted will be within the ASCII character set, ASCII value less than 127.

TEST INTERFACE

The RFID Reader/Writer will provide discrete LEDs that will provide simple status of the RFID Reader/Writer independent of attached PC.

Communication Protocol/Messages

The packet protocol for the RFID Reader/Writer is described in the following paragraphs. The protocol provides a robust, easily managed interface that supports debugging on a simple ASCII terminal in addition to providing a checksum for message validation.

The general message format is as follows:

Sync Char	Command	Data	Checksum	CR LF

General Message Format

Sync Char	Single byte character '@' denoting the beginning of a message
Command	Single byte character defining the command this message represents. See Table 1 for a list of commands
Data	A variable length field containing additional information support the command
Checksum	The two-byte checksum used for the message includes the Sync Char through the end of the Data field. See the following paragraph for more information on the checksum used
CR LF	This two-byte field is the standard ASCII carriage return '0x0D' and the line feed '0x0A'

TABLE 1:

Command Char	From	To	Description
'2'	R/W	PC	Data field contains MCRF355 data (14 bytes)
'3'	R/W	PC	Data field contains MCRF355 data (18 bytes)
'4'	R/W	PC	Data field contains MCRF450 data blocks (Read)
'5'	R/W	PC	Data field contains MCRF450 data blocks (Write)
'6'	R/W	PC	Data field contains MCRF450 FRB response data
'7'	R/W	PC	Data field contains MCRF450 FRR response data
'F'	R/W	PC	Firmware version
'R'	R/W	PC	Response message
'R'	PC	R/W	Reset request command
'M'	PC	R/W	Mode select command
'N'	PC	R/W	No operation
'V'	PC	R/W	Verbose read command
'W'	PC	R/W	Write command
'C'	PC	R/W	Configuration message
'L'	PC	R/W	Load command

COMMAND OVERVIEW

CHECKSUM

The checksum is a two-character field. Adding the fields Sync Char through Data into an unsigned byte type and ignoring any overflow generated determines this value. The resultant value is then negated to provide a 2's complement checksum value. This 8-bit result is then converted to two hex characters to represent the checksum in the message (e.g. checksum byte value 00101100 results in a checksum of two ASCII bytes '2C' represented in the message).

MESSAGE FORMATS

The following paragraphs detail the individual commands and messages.

LOAD MESSAGE

The load command provides a method to update the PIC 16F876 firmware in the field via the RS-232 interface. The Data Field length is zero. When the load command is received, the RFID Reader/Writer will transition to a 'loader', which will then accept hex record lines to be written to program memory. The format of the hex record will be the format generated by the Microchip assembler/linker. Each hex record line will be validated before writing to program memory. The RFID Reader/Writer will respond with 'Ready' response message upon successful write or an error message if unsuccessful. After the final line of the .HEX file is sent, the newly loaded program is entered using the POR vector at address 0000. See Response Message paragraphs.

0x40	'L'	Data	Checksum	CR LF

LOAD MESSAGE FORMAT

RESPONSE MESSAGE

The response message is used to provide acknowledge and status response from the R/W to the external PC. The data field contains the specific response encoded as a 2-digit hexadecimal number. The responses supported are listed below.

0x40	'R'	Response Number	Checksum	CR LF

RESPONSE MESSAGE FORMAT

Response Number	Equivalent Text	Description
00	"Ready"	Ready for the next message
01	"EEPROM Burn Failed"	Previous write was read back and validated unsuccessfully
02	"No Entry Point Specified"	No processor instructions were given for ROM locations 0-3
03	"Invalid Address"	A write to Program ROM was outside valid range
04	"Invalid Hex Data"	The characters representing hex data were not in the range 0-9, A-F
05	"RS-232 Error"	Characters were lost or garbled. Message should be repeated.
06	"Invalid Checksum"	Checksum did not verify
07	"Undefined Command"	Command byte sent is not a known command
08	"Invalid Paramter"	Contents of a command string are invalid
09	"Bad Processor"	The Slave processor fails to communicate

RESPONSE MESSAGES

RESET MESSAGE

The reset message is sent from the external PC to the Reader/Writer. It instructs the R/W to reset itself, and return to the just-powered-up state. In this state, the carrier is off, and the R/W is sending 'A' characters over the RS-232 line at a 50 Hz rate, looking for a PC-based application to communicate with. See the paragraph "Auto Detect Support" for a more complete description. The data field length is zero.

0x40	'R'	Data Field	Checksum	CR LF

RESET MESSAGE FORMAT

NOP MESSAGE

The NOP message is a no operation message. It can be used as a 'heart-beat' message to maintain communication if needed. The Data Field length is zero. This command returns the "Ready" Response Message ('R'). Note that this and every command causes the Reader/Writer to stop its current operations to process the new command. After this command, the Reader/Writer remains in the idle loop, waiting for the next command.

0x40	'N'	Data Field	Checksum	CR LF

NOP MESSAGE

MODE SELECT MESSAGE

The mode select message is used to put the RFID Reader/Writer in a specific read mode as defined below.

0x40	'M'	Data Field	Checksum	CR LF

MODE SELECT MESSAGE

The mode field contains a one-byte character that defines the specific mode to place the reader into. This byte is defined below.

Mode Char	Description
'0'	Read MCRF355/360 tags, returning the data in Microchip format. No anti-aliasing – all tag reads are reported
'1'	Read MCRF355/360 tags, returning raw tag data. No anti-aliasing – all tag reads are reported
'2'	Read MCRF355/360 tags, returning the data in Microchip format. Anti-aliasing enabled -- subsequent reads of the same tag are ignored.
'3'	Read MCRF355/360 tags, returning raw tag data. Anti-aliasing enabled -- subsequent reads of the same tag are ignored.
'I'	Inventory read mode. (FRR & FRB: tags are put to sleep after being identified)
'C'	Continuous read mode. (FRR & FRB)
'A'	Alarm mode. (FRR only)
'S'	Stop reading mode. (Leave carrier on)
'F'	Reader/writer off. (Turn carrier off)

MODE SELECT CHARACTERS

355 DATA BLOCKS MESSAGE – MICROCHIP FORMAT

This message contains the entire data block from the MCRF355/360 represented in ASCII hex format. It assumes the tag was written in Microchip format, which is: 10-bit header (9 ones, and 1 zero), followed by 14 8-bit bytes and a 2-byte checksum, with each byte separated by a zero bit, and written MSb first. The checksum of the block is verified before transmission.

0x40	'2'	Data Block	Checksum	CR LF

355/360 DATA BLOCKS MESSAGE

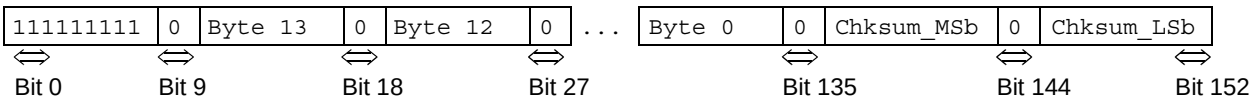
The format of the data block is as follows:

```
T<time stamp>, <data>
```

Where:

Field name	Description
Time stamp	The time stamp of when the device was read. This value consists of 2 bytes (4 ASCII hex characters), with the LSb = 819.2 µS. The clock is a free-running counter with a rollover period of 53.7 seconds. The bytes are sent MSb first.
Data	The 14 data bytes represented in ASCII hex characters. Byte 13 is first; byte 0 is last. The checksum bytes are not transferred.
355/360 DATA BLOCKS MESSAGE DETAIL	

"Microchip Format" is defined by the MCRF 355/360 Contact Programmer, and is shown graphically below. Of the 154 bits in the tag, the first 9 are the preamble, and fixed as '1' bits. Following the preamble, and separating each byte, are spacer bits (zeros). All bytes are Most Significant bit (MSb) first. This format allows 14 data bytes followed by a 16-bit checksum (simple summation of all 14 bytes).



355 DATA BLOCKS MESSAGE – RAW FORMAT

This message contains the data block from the MCRF355/360 represented in ASCII hex format. It assumes the tag was written in Microchip format, however the spacer bits which exist between every byte are not removed. Internally, the data is converted to Microchip format so that the block checksum can be calculated and verified before transmission.

0x40	'3'	Data Block	Checksum	CR LF

355/360 Data Blocks Message

The format of the Data Block is as follows:

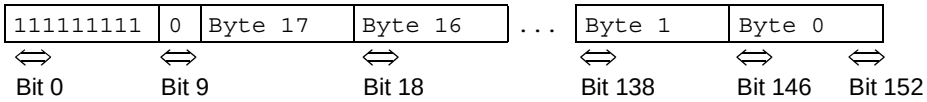
```
T<time stamp>, <data>
```

Where:

Field name	Description
Time stamp	The time stamp of when the device was read. This value consists of 2 bytes (4 ASCII hex characters), with the LSb = 819.2 µS. The clock is a free-running counter with a rollover period of 53.7 seconds. The bytes are sent MSb first.
Data	The 18 data bytes represented in ASCII hex characters. Byte 17 is sent first.
355/360 DATA BLOCKS MESSAGE DETAIL	

The tag data is assumed to be as shown graphically below for purposes of displaying it in 'Raw Format'. It is similar to Microchip Format in that all bytes are Most Significant bit (MSb) first, and the first 10 bits are the fixed preamble (9 one-bits followed by a zero bit). The remaining 143 bits make up the 18 8-bit bytes.

Note:	The last byte has one missing bit. Its Least Significant bit (LSb) is fixed at zero.



MCRF45X DATA BLOCKS MESSAGE

0x40	'4'	Data Block	Checksum	CR LF

45X DATA BLOCKS MESSAGE

This message contains the data blocks returned from the MCRF450 in response to a Verbose Read command. All 32 blocks of the MCRF450 tag are included. The message elements are defined below. The format of the Data Block is:

```
I<id>,<block>:<data>,<block>:<data>,...<block>:<data>
```

Where:

Field name	Description
I<id>	The ASCII hex representation of the 4-byte tag ID. LSb first.
Block	Block number, represented by 2 ASCII hex characters. Its value ranges from 00 to 1F (31 decimal). Block numbers are followed by a colon.
Data	One data block (4 bytes) from the tag, represented in ASCII hex characters. Data blocks are separated by commas. A block which is unreadable (invalid CRC) will return "XXXX" for the data. In this case, it will be 4 characters instead of 8. The data is LSb first.
45X DATA BLOCKS MESSAGE DETAIL	

MCRF45X DATA BLOCKS WRITTEN MESSAGE

0x40	'5'	Data Block	Checksum	CR LF

45X DATA BLOCKS MESSAGE

This message contains the data blocks returned from the MCRF45X in response to a Verbose Write command. One message is returned per tag written. The message elements are defined below. The format of the Data Block is:

```
I<id>,<block>:<data>,<block>:<data>,...<block>:<data>
```

Where:

Field name	Description
I<id>	The ASCII hex representation of the 4-byte tag ID. LSb first.
Block	Block number, represented by 2 ASCII hex characters. Its value ranges from 00 to 1F (31 decimal). Block numbers are followed by a colon.
Data	One data block (4 bytes) from the tag, represented in ASCII hex characters. This data is what the tag returned following the write to this block. A block which is write-protected will return to "RO" for the data. In this case, it will be 2 characters instead of 8. A block which is unreadable (invalid CRC) will return "XXXX" for the data. The data is LSb first.
45X DATA BLOCKS MESSAGE DETAIL	

450 FRB RESPONSE MESSAGE

0x40	'6'	Data Block	Checksum	CR LF

45X FRB RESPONSE MESSAGE

This message This message contains the data returned from the MCRF45X in response to an FRB command. The message elements are defined below. The format of the Data Block is:

```
T<time stamp>,<TC/TP>,<ID>,<FRF>
```

Where:

Field name	Description
Time stamp	The time stamp of when the device was read. This value consists of 2 bytes (4 ASCII hex characters), with the LSb = 819.2 µS. The clock is a free-running counter with a rollover period of 53.7 seconds. The bytes are sent MSb first.
ID	One data block (4 bytes) represented in ASCII hex characters. The data is from Block #1, the tag's ID. The data is sent LSb first.
45X FRB RESPONSE MESSAGE DETAIL	

MCRF45X FRR RESPONSE MESSAGE

0x40	'7'	Data Block	Checksum	CR LF

45X FRR RESPONSE MESSAGE

This message contains the data returned from the MCRF450 in response to an FRR command. The message elements are defined below. The format of the Data Block is:

```
T<time stamp>,<TC/TP>,<ID>,<FRF>
```

Where:

Field name	Description
Time stamp	The time stamp of when the device was read. This value consists of 2 bytes (4 ASCII hex characters), with the LSb = 819.2 µS. The clock is a free-running counter with a rollover period of 53.7 seconds. The bytes are sent MSb first.
TC/TP	One byte containing the TC and TP values from the tag, represented in ASCII hex characters. Bits 0-2 are the TC value; bits 3-7 are the TP (tag parameters) value. See the MCRF45X Data Sheet on the format of the TP field.
ID	One data block (4 bytes) represented in ASCII hex characters. The data is from Block #1, the tag's ID. The data is sent LSb first.
FRF	The Fast Read Field, represented in ASCII hex characters. The data is from Blocks #3-5. The exact number of bytes in the FRF depends upon the 2 DF bits within the TP field, and can be 4, 6, 8 or 12. The LSb is sent first.
45X FRR RESPONSE MESSAGE DETAIL	

FIRMWARE VERSION RESPONSE MESSAGE

0x40	'F'	Data Block	Checksum	CR LF

FIRMWARE VERSION RESPONSE MESSAGE

This message is sent once, immediately following connection establishment. The format of the Data Block is 2 ASCII digits indicating the major and minor revision numbers. The range of revision numbers supported is 1.0 thru 9.9.

VERBOSE READ MESSAGE

This message will terminate continuous read mode and initiate a read of a specific ID tag in the field. The response to this message will be a 450 Data Blocks message ('4').

0x40	'V'	Data Block	Checksum	CR LF

VERBOSE READ MESSAGE

The tag ID field contains the 4 tag ID bytes represented in ASCII hex format.

WRITE MESSAGE

The write message provides the capability to program one or all MCRF45X devices with one to 16 blocks of data. If write-all-tags is selected, the Reader/Writer will look for all FRR and FRB parts in the field, writing them as soon as they are found, until the user places the Reader/Writer into another mode (or idle state). If one-tag-write is selected, the carrier is turned off after the selected tag is found and written. The response to this message will be one or more 45X Data Blocks Written message ('5') - one per tag.

Block 1 (the tag ID) should not be written.

If the starting block number is 0 or 2, the number of data blocks to be written is limited to 1 block.

In order to prevent an FRR part from becoming inaccessible in case of a failed write to blocks 0, 3, 4 or 5, the Reader/Writer will turn an FRR part into an FRB part prior to writing these blocks, then return it into an FRR part only if all blocks were written correctly. When writing to block 0, bit 31 should be kept clear to keep from flagging a special case, described next.

Two special cases of the Write Command exist: converting FRR tags into FRBs, and converting FRB tags into FRRs.

To turn devices into FRR parts, issue the Write Message for data block 0, with the two most-significant bits of the data (Fast Read and Talk First bits) set to '1'. The remaining 30 data bits are don't care. When the Reader/Writer sees this situation, it will calculate the correct FRR response CRC for the tag and write it to the low 16 bits of block 0. After successful write, it then sets the FR bit. A 45X Data Blocks Written message ('5') is returned for each tag which is changed from an FRB part to an FRR part.

To turn devices into FRB parts, issue the Write Message for data block 0, with bit 31 of the data (Fast Read) set to '1', and bit 30 (Talk First) set to '0'. The remaining 30 data bits are don't care. The Reader/Writer will clear the FR bit (bit 31 of block 0) without affecting any other tag memory bits. A 450 Data Blocks Written message ('5') is returned for each tag which is changed from an FRR part to an FRB part.

The format of the message is as follows.

0x40	'W'	Data Block	Checksum	CR LF

WRITE MESSAGE

The Data Block has the following format when writing to one selected tag. All characters not between braces ('<' '>') are necessary for a valid message. The total number of <data> fields must be 16 or less.

```
I<id>,<block number>,<data>,...,<data>
```

Where:

Field name	Description
I<id>	The ASCII hex representation of the 4-byte tag ID. (LSb first)
<block number>	The beginning block number to write, represented in ASCII hex.
<data>	A 4-byte block of data, LSB first, in ASCII hex representation.

The Data Block has the following format to write to all devices in the R/W field. The total number of <data> fields must be 16 or less.

```
*,<block number>,<data>,<data>,....,<data>
```

Where:

Field name	Description
*	Replacing the I<id> field with a star character denotes all tags.
<block number>	The beginning block number to write, represented in ASCII hex.
<data>	A 4-byte block of data, LSB first, in ASCII hex representation.

CONFIGURATION MESSAGE

The configuration message provides a method to set specific attributes within the RFID Reader/Writer firmware. The format of the message is as follows.

0x40	'C'	Data Block	Checksum	CR LF

CONFIGURATION MESSAGE

The Data Block consists of up to 7 parameters that may be set. The parameters are separated by commas and begin with an identifying character. Any parameter not included in the command retains the value it had before the Configuration Message. The order of the parameters is not important.

```
T<ts>,M<tcmax>,S<speed>,P<ppm timing>,G<gap timing>,V<vpp>,I<audio>
```

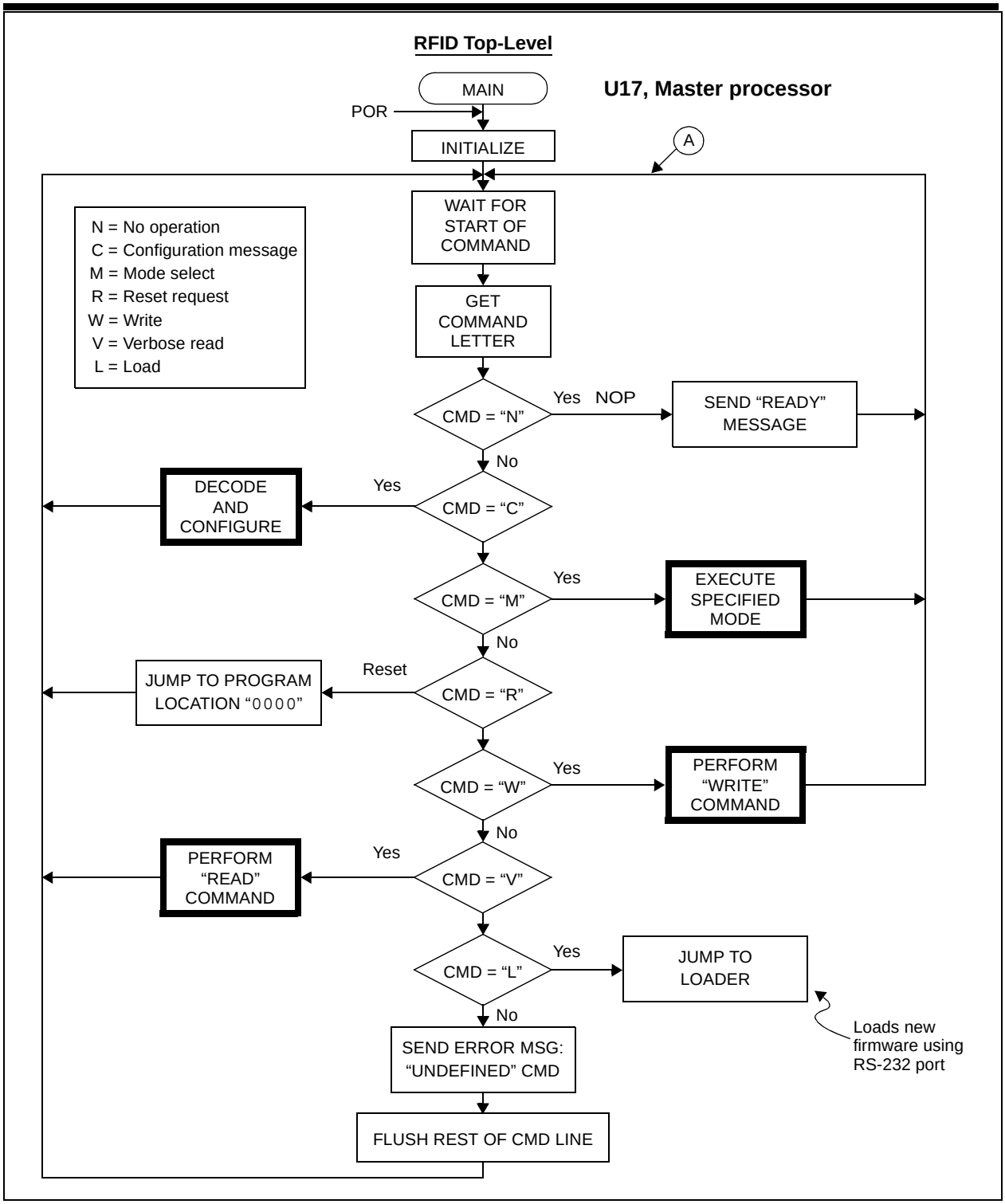
Where:

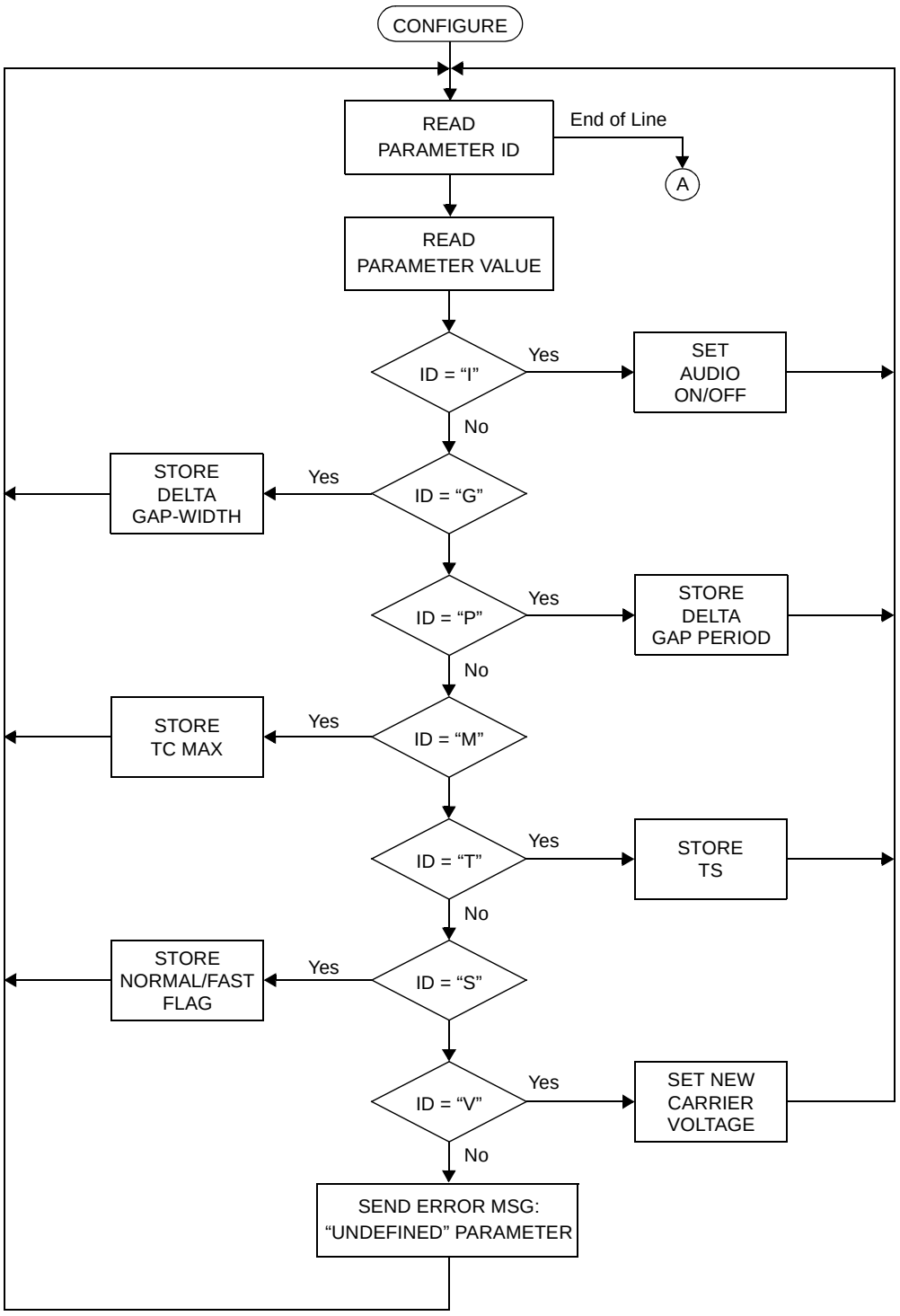
Field	POR Value	Description
T<ts>	16	The ASCII hex representation of 1 byte: The number of Time Slots used in the tag's FRR command. Valid values are: 1, 16, 64.
M<tcmax>	1	The ASCII hex representation of 1 byte: The TCMAX value to use in the tag's FRR command. Valid values are: 1, 2, 4. If TS = 64, then TCMAX must be 1.
S<speed>	0	The ASCII hex representation of 1 byte: Whether to modulate the carrier at Normal Speed or Fast Speed for the PPM symbols. A value of 0 sets Normal Speed; a value of 1 sets Fast Speed.
P<ppm timing>	0	The ASCII hex representation of an 8-bit signed integer: The relative timing to use for gap periods. Valid range is -6 to +6, with 0 being nominal (175 µS Normal Speed/10 µS Fast Speed). -6 corresponds to 20% reduction in time, and +6 corresponds to 20% increase in time. +/- 3 corresponds to +/-10%, etc.
G<gap timing>	0	The ASCII hex representation of an 8-bit signed integer: The relative timing to use for gap widths. Valid range is -6 to +6, with 0 being nominal (100 µS Normal Speed/6 µS Fast Speed). -6 corresponds to 20% reduction in time, and +6 corresponds to 20% increase in time. +/- 3 corresponds to +/-10%, etc.
V<vpp>	FFh	The ASCII hex representation of 1 byte: The relative strength of the carrier signal. A value of 0 sets no carrier; a value of FFh sets maximum carrier field strength.
I<audio>	1	The ASCII hex representation of 1 byte: A value of 1 enables beeps when each tag is detected. A value of 0 disables audible indication.

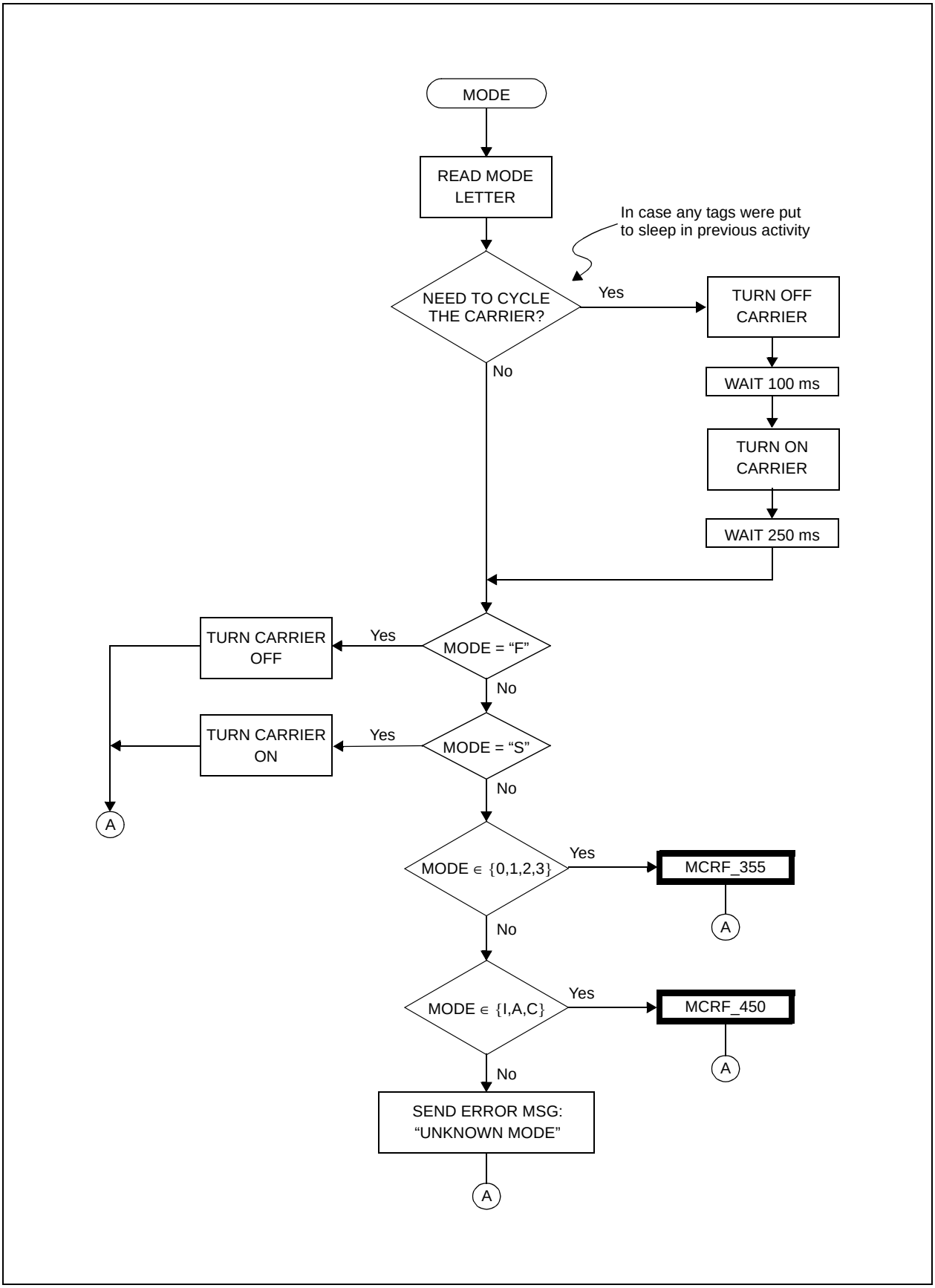
AUTO DETECT SUPPORT

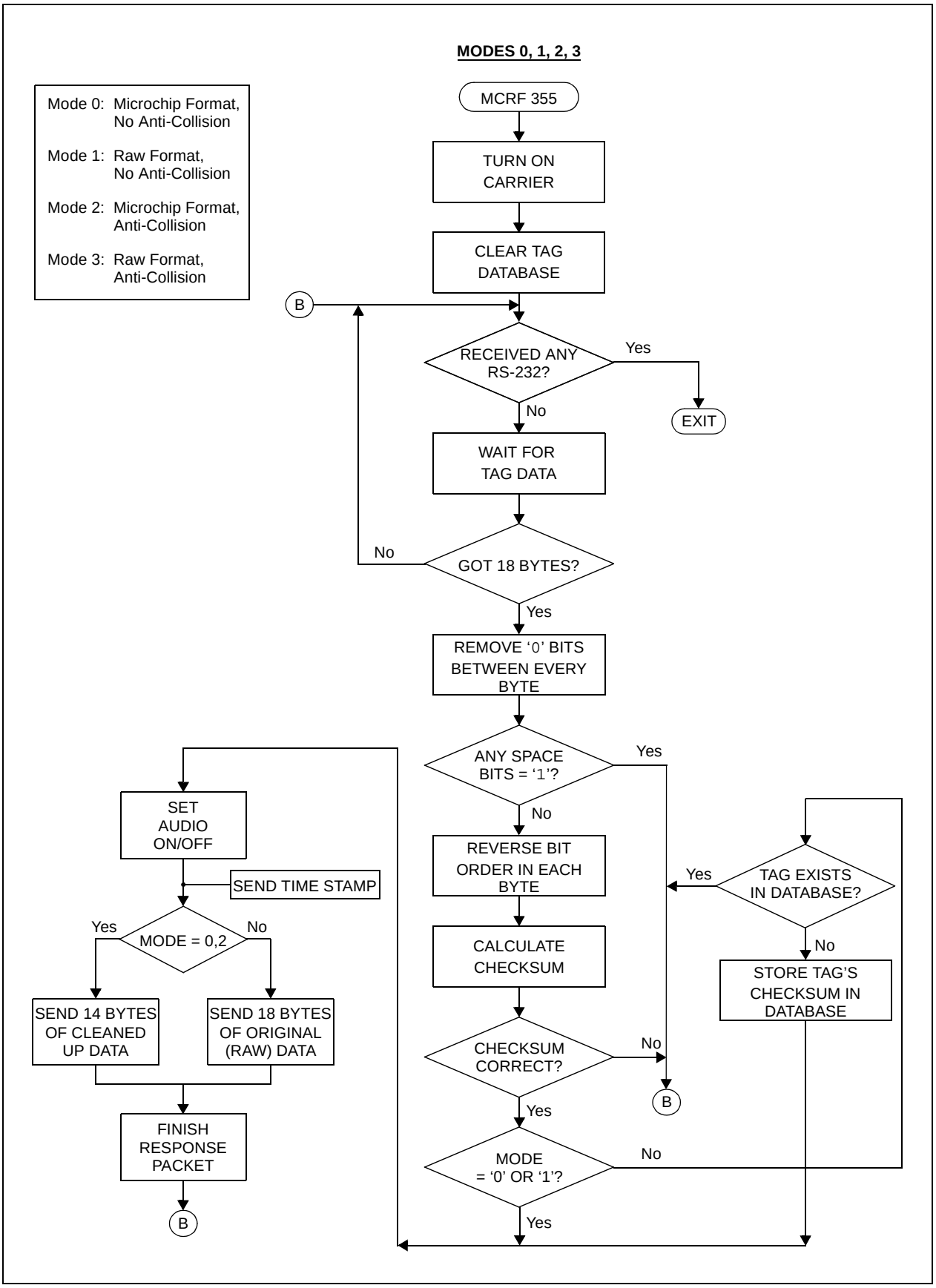
At power-up of the RFID Reader/Writer, the character 'A' will be continuously transmitted at a 50 Hz rate over the serial port. This provides a serial stream to support auto-detection of the device by a PC. When the Reader/Writer receives a 'B' character from the PC, it will cease transmission of the 'A' characters, and return a type 'F' Response Message (Firmware Version), thus establishing a positive confirmation of communication. The RS-232 parameters are: 19.2 Kbaud, 8 bits, no parity, and 1 stop bit.

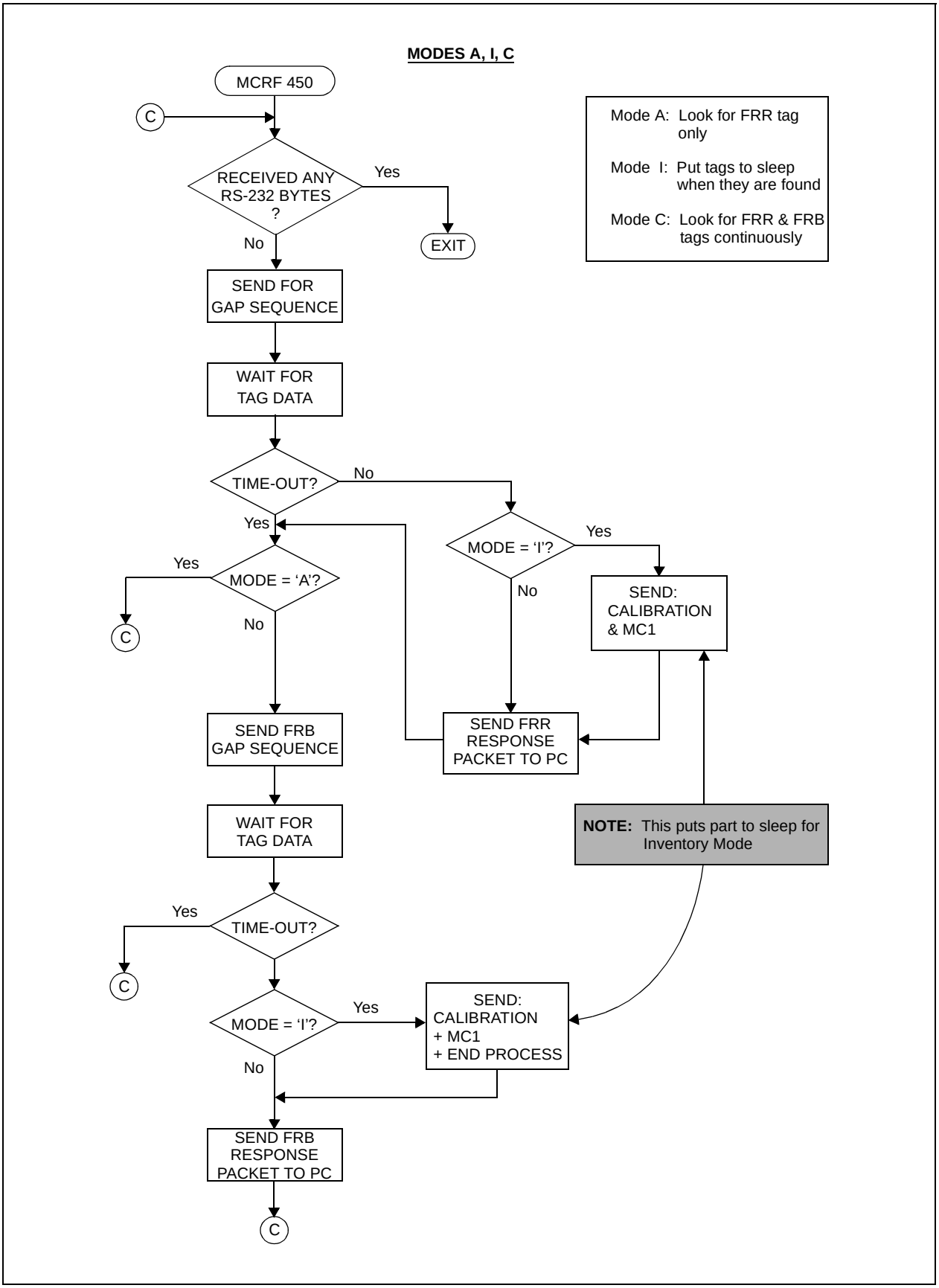
PICmicro® Microcontroller Firmware Flow Chart of MCRF45X Demo Reader

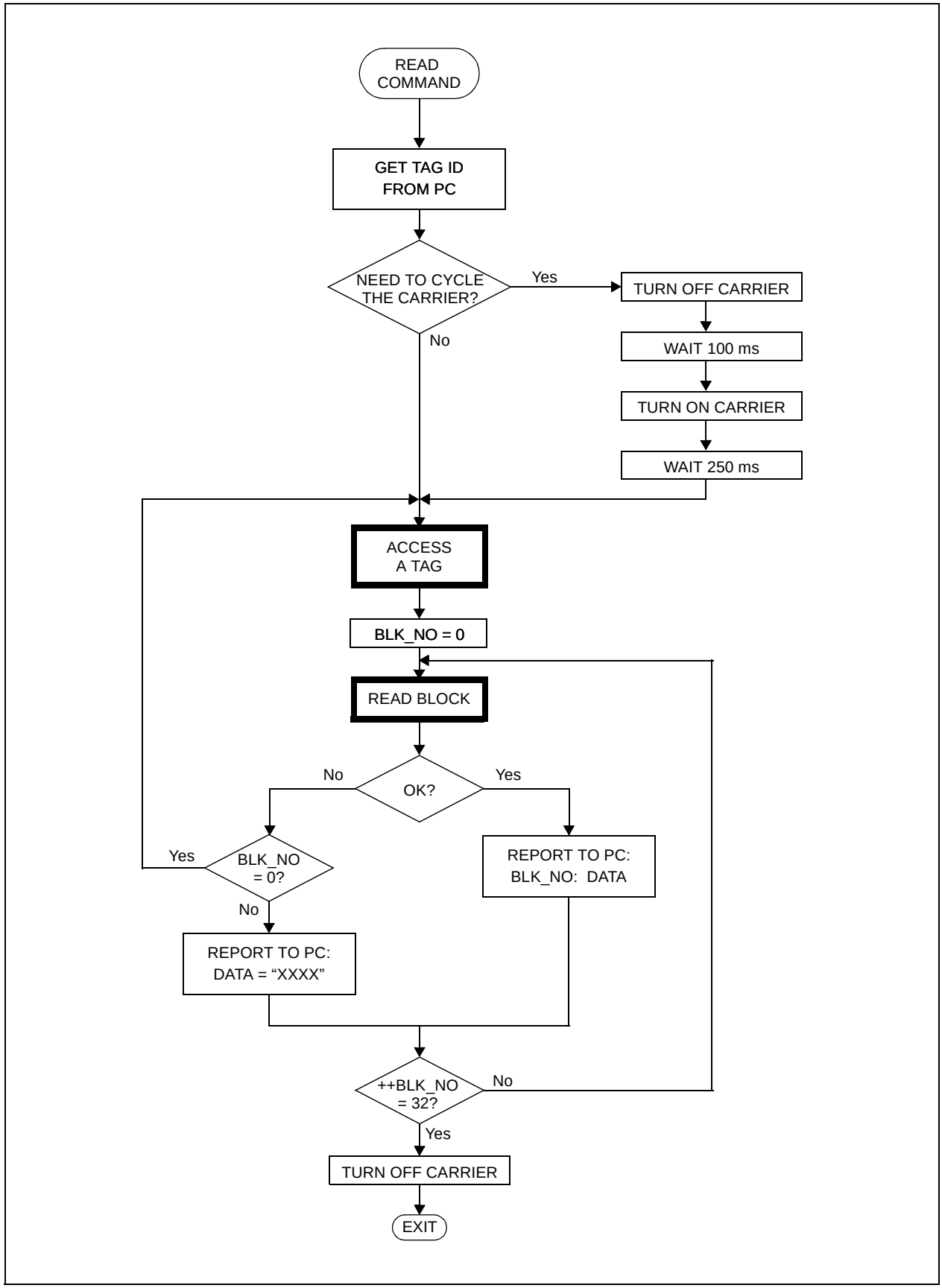


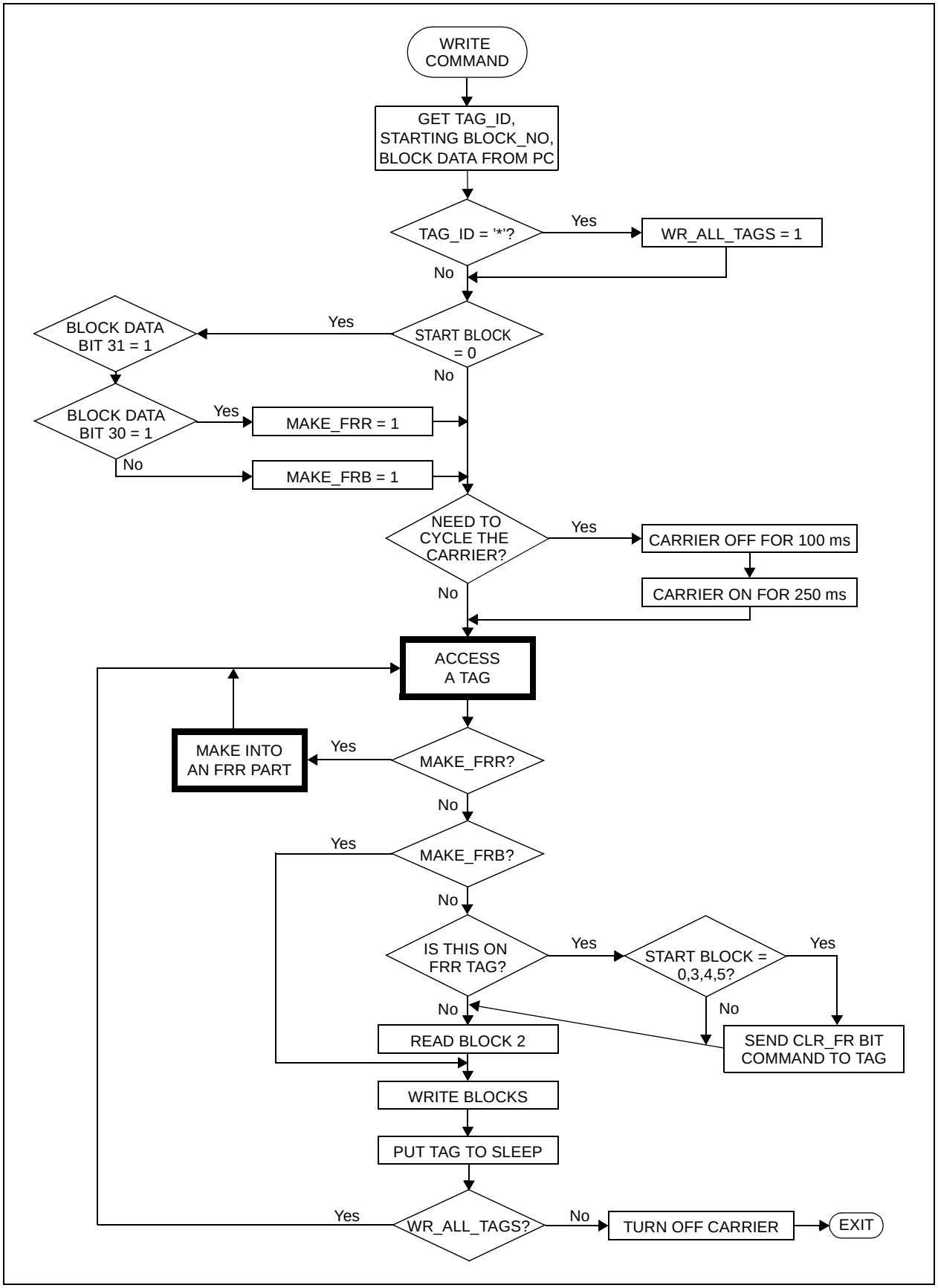


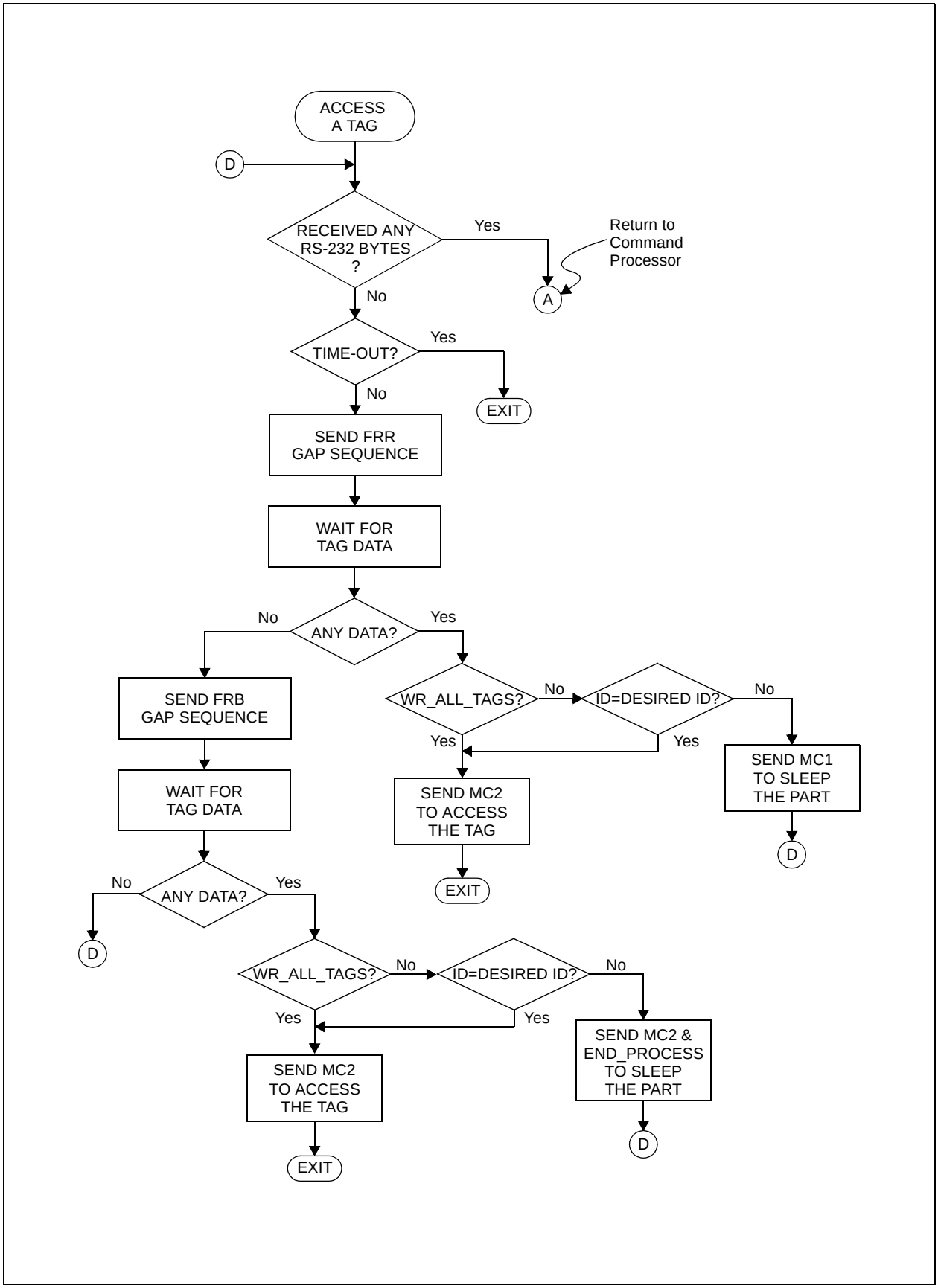

MODE
READ MODE LETTER
In case any tags were put to sleep in previous activity
NEED TO CYCLE THE CARRIER?
Yes
TURN OFF CARRIER
WAIT 100 ms
TURN ON CARRIER
WAIT 250 ms
No
MODE = “F”
Yes
TURN CARRIER OFF
No
MODE = “S”
Yes
TURN CARRIER ON
No
A
MODE ∈ {0,1,2,3}
Yes
MCRF_355
A
No
MODE ∈ {I,A,C}
Yes
MCRF_450
A
No
SEND ERROR MSG: “UNKNOWN MODE”
A

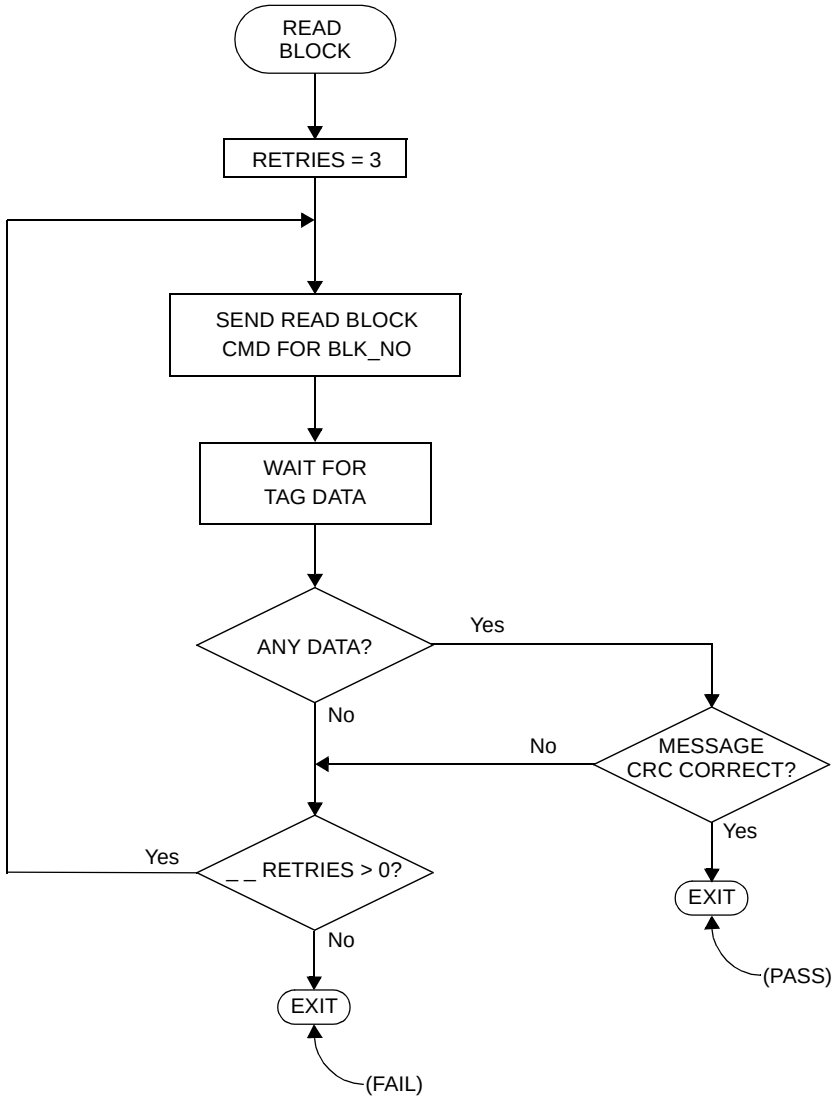


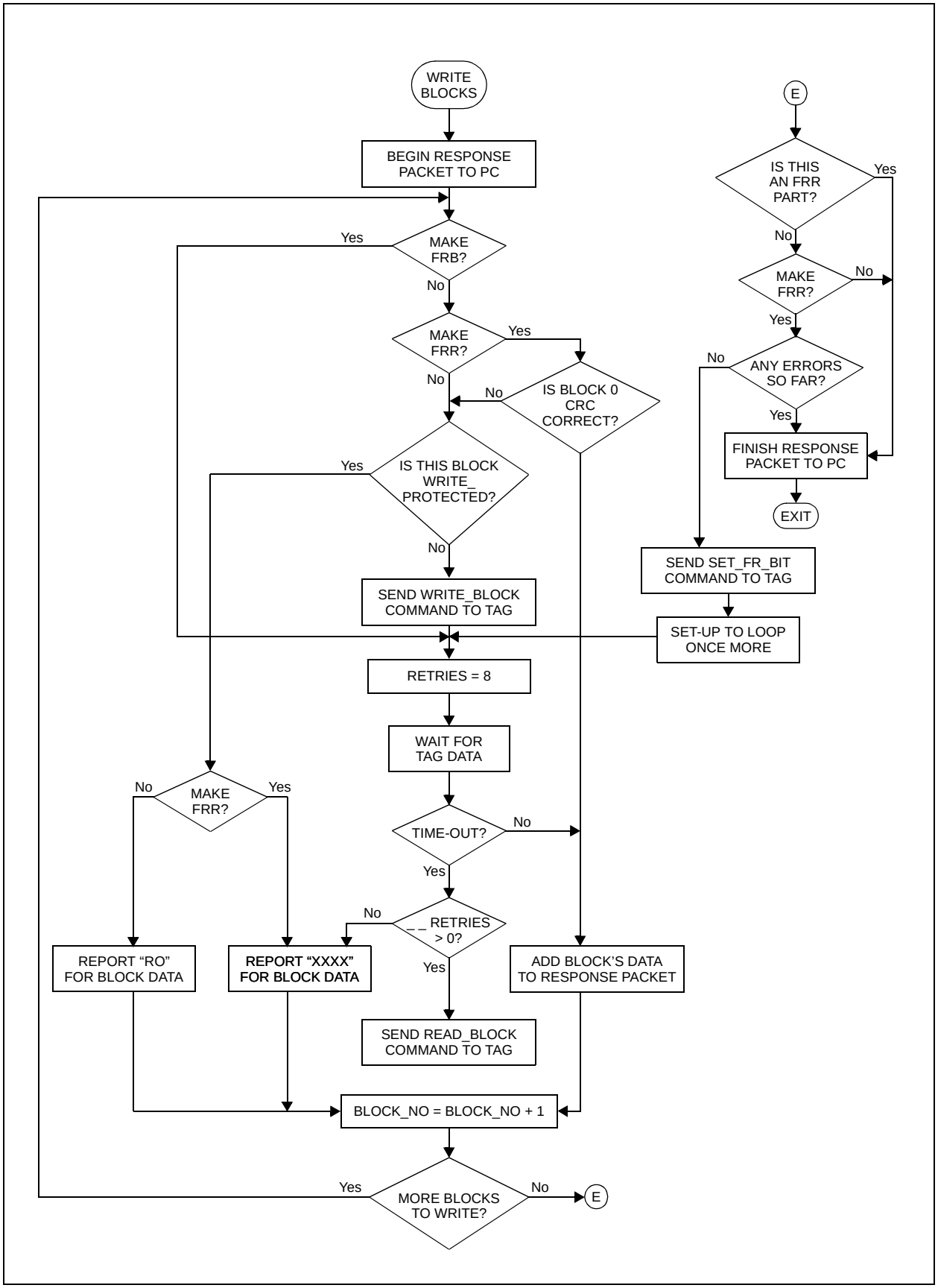

MODES A, I, C
MCRF 450
C
RECEIVED ANY RS-232 BYTES ?
Yes
EXIT
No
SEND FOR GAP SEQUENCE
WAIT FOR TAG DATA
TIME-OUT?
No
Yes
MODE = 'I'?
Yes
No
SEND: CALIBRATION & MC1
MODE = 'A'?
Yes
C
No
SEND FRB GAP SEQUENCE
SEND FRR RESPONSE PACKET TO PC
WAIT FOR TAG DATA
NOTE: This puts part to sleep for Inventory Mode
TIME-OUT?
Yes
C
MODE = 'I'?
Yes
SEND: CALIBRATION + MC1 + END PROCESS
No
SEND FRB RESPONSE PACKET TO PC
C
Mode A: Look for FRR tag only
Mode I: Put tags to sleep when they are found
Mode C: Look for FRR & FRB tags continuously

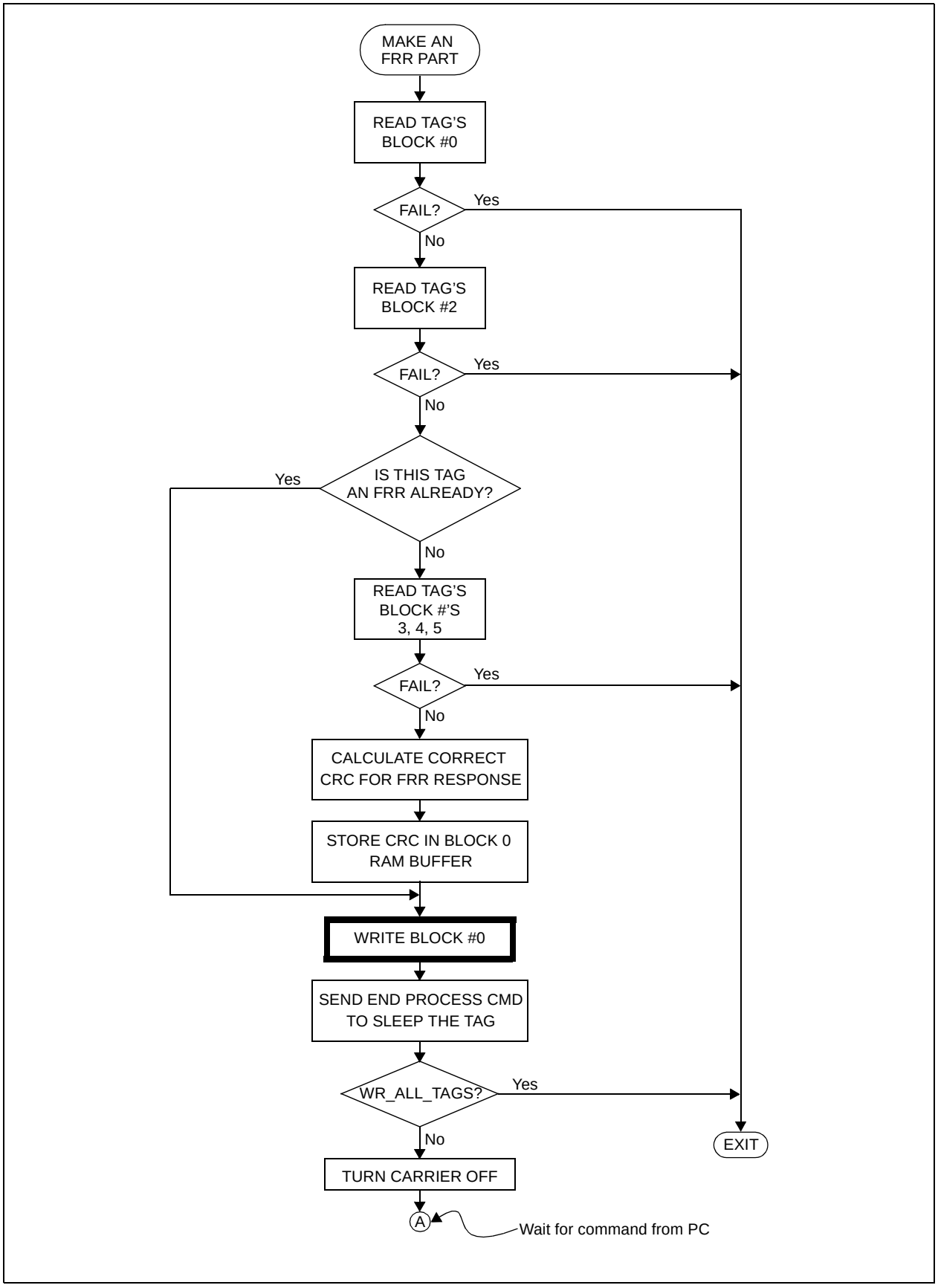


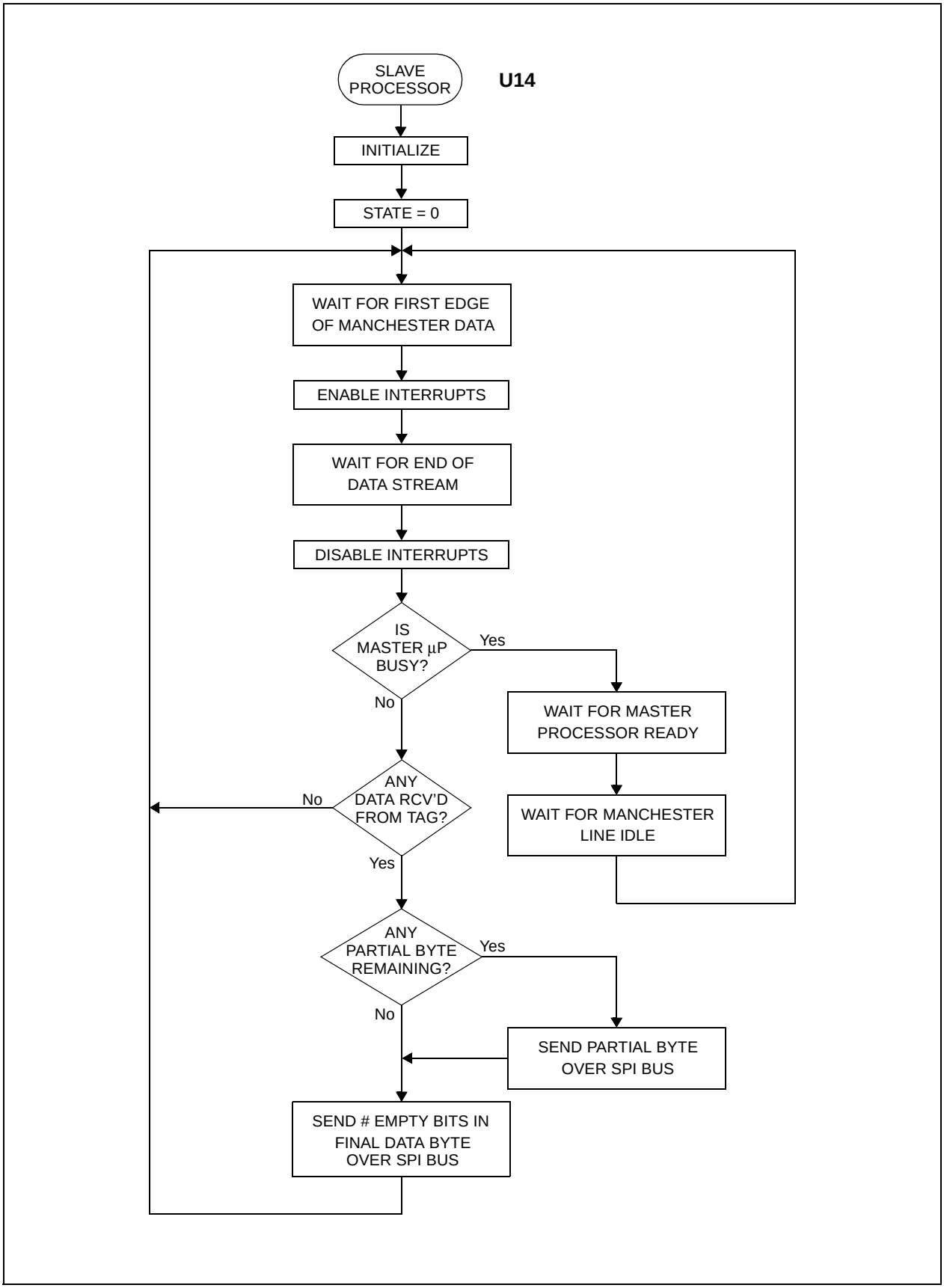

WRITE COMMAND
GET TAG_ID, STARTING BLOCK_NO, BLOCK DATA FROM PC
TAG_ID = '*'?
Yes
WR_ALL_TAGS = 1
No
START BLOCK = 0
Yes
BLOCK DATA BIT 31 = 1
No
BLOCK DATA BIT 30 = 1
Yes
MAKE_FRR = 1
No
MAKE_FRB = 1
NEED TO CYCLE THE CARRIER?
Yes
CARRIER OFF FOR 100 ms
CARRIER ON FOR 250 ms
No
ACCESS A TAG
MAKE_FRR?
Yes
MAKE INTO AN FRR PART
No
MAKE_FRB?
Yes
No
IS THIS ON FRR TAG?
Yes
START BLOCK = 0,3,4,5?
Yes
No
No
READ BLOCK 2
SEND CLR_FR BIT COMMAND TO TAG
WRITE BLOCKS
PUT TAG TO SLEEP
WR_ALL_TAGS?
Yes
No
TURN OFF CARRIER
EXIT

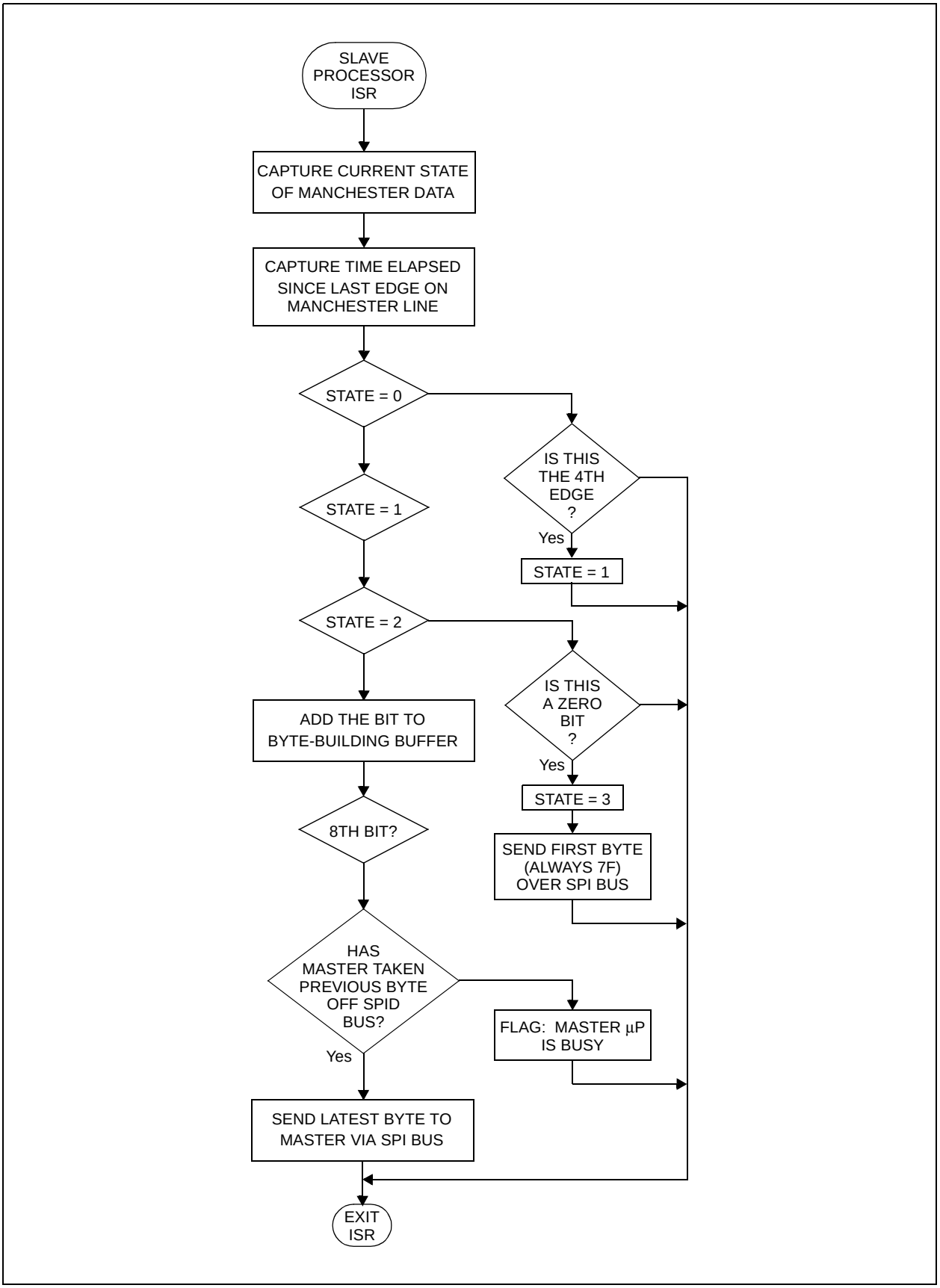



READ BLOCK
RETRIES = 3
SEND READ BLOCK CMD FOR BLK_NO
WAIT FOR TAG DATA
ANY DATA?
Yes
No
MESSAGE CRC CORRECT?
No
Yes
EXIT
(PASS)
Yes
_ _ RETRIES > 0?
No
EXIT
(FAIL)




MAKE AN FRR PART
READ TAG'S BLOCK #0
FAIL?
Yes
No
READ TAG'S BLOCK #2
FAIL?
Yes
No
IS THIS TAG AN FRR ALREADY?
Yes
No
READ TAG'S BLOCK #'S 3, 4, 5
FAIL?
Yes
No
CALCULATE CORRECT CRC FOR FRR RESPONSE
STORE CRC IN BLOCK 0 RAM BUFFER
WRITE BLOCK #0
SEND END PROCESS CMD TO SLEEP THE TAG
WR_ALL_TAGS?
Yes
No
EXIT
TURN CARRIER OFF
A
Wait for command from PC

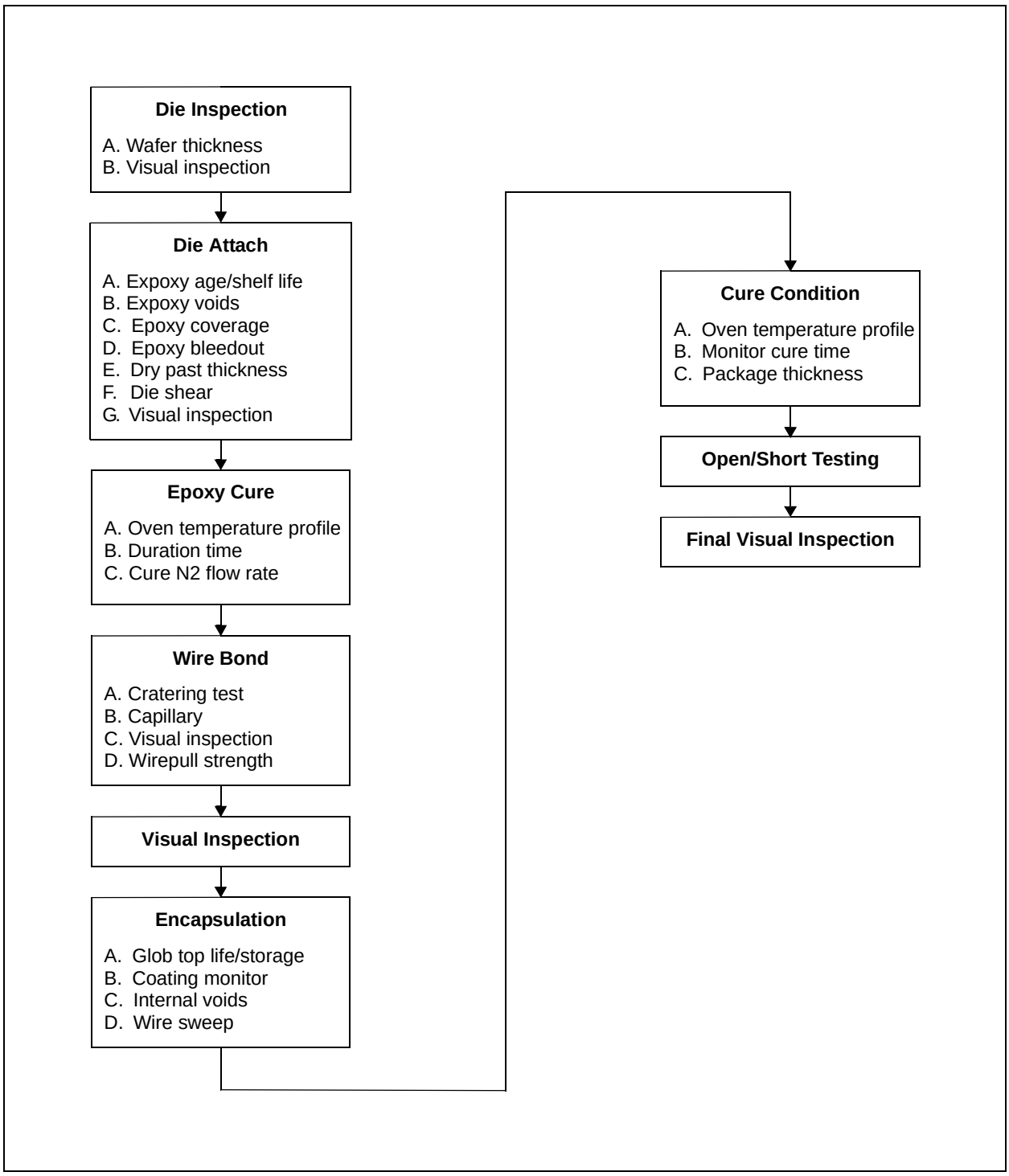



SLAVE PROCESSOR ISR
CAPTURE CURRENT STATE OF MANCHESTER DATA
CAPTURE TIME ELAPSED SINCE LAST EDGE ON MANCHESTER LINE
STATE = 0
STATE = 1
STATE = 2
IS THIS THE 4TH EDGE ?
Yes
STATE = 1
IS THIS A ZERO BIT ?
Yes
STATE = 3
SEND FIRST BYTE (ALWAYS 7F) OVER SPI BUS
ADD THE BIT TO BYTE-BUILDING BUFFER
8TH BIT?
HAS MASTER TAKEN PREVIOUS BYTE OFF SPID BUS?
Yes
FLAG: MASTER µP IS BUSY
SEND LATEST BYTE TO MASTER VIA SPI BUS
EXIT ISR

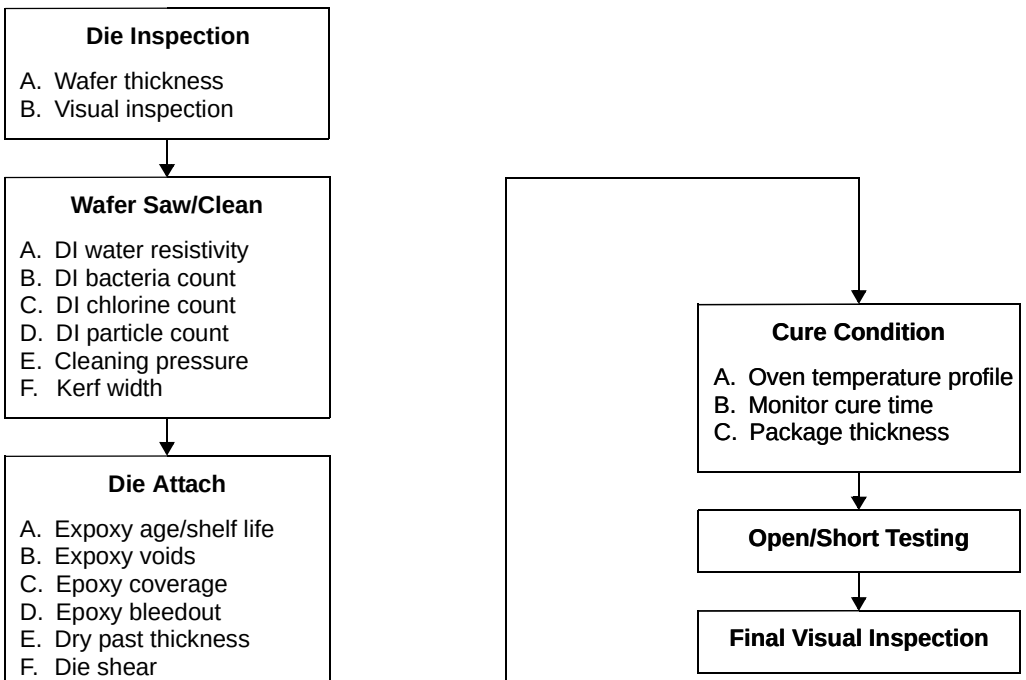
NOTES:

Recommended Assembly Flows

1.0 WAFER ON FRAME ASSEMBLY FLOW



2.0 WAFER ASSEMBLY FLOW



NOTES:

NOTES:

NOTES:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Austin - Analog
8303 MoPac Expressway North
Suite A-201
Austin, TX 78759
Tel: 512-345-2030 Fax: 512-345-6085

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Boston - Analog
Unit A-8-1 Millbrook Tarry Condominium
97 Lowell Road
Concord, MA 01742
Tel: 978-371-6400 Fax: 978-371-0050

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany - Analog
Lochhamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

06/01/01