Application Note AN-46
HiperPLC™ Family

Design Guide

Introduction

The PL810 is an integrated PFC + LLC power supply controller. It locks the frequency and phase of the PFC and the LLC so as to reduce bulk capacitor ripple current, and prevent edge collisions (coincidental switching edges between LLC and PFC stages) and associated noise related issues.

A PFC (Power Factor Corrector), is a non-isolated pre-regulator in front of the main LLC converter, which conditions and shapes the AC input current to follow the input voltage waveform in order to achieve the high power factor required to meet international standards.

The PLC810PG is designed for continuous-mode PFC boost conversion with a constant output voltage. The advantages of continuous conduction mode PFC compared to discontinuous conduction mode PFC are listed below.

- Smaller and lower cost choke
- Reduced choke high frequency ripple and peak currents
- Reduced MOSFET RMS current
- Reduced PFC input film capacitor ripple current
- Reduced Bulk Capacitor ripple current
- Reduced differential EMI, saving cost in the EMI filtering

An LLC is a type of a resonant converter with very low switching losses which yields high efficiency. LLC converters use a variable frequency switching approach to regulate output power. LLC converters do not require an output choke (in some cases a small post filter inductor may be required to attenuate high frequency spikes), and if an "integrated" transformer (with high leakage inductance) is used, have only one magnetic element. Integrated transformers have the additional advantage of low primary to secondary capacitance, reducing common mode EMI generation. The PLC810PG is designed to be used alongside a small standby PSU that provides VCC, to supply the IC.

Scope

This application note is positioned to provide information suitable for engineers with some experience in power supply design. The application note should be used with the PLC810PG data sheet, RD-189 Reference Design board, and PIXls PLC810PG Design Spreadsheet.

Step-by-Step Transformer and PFC Choke Design Procedure

This section describes the use of the PCL810PG design spreadsheet which is part of PIXls Designer v.7.1.4.4 spreadsheet design tool (part of PI Expert Suite 7.1). This software may be downloaded free from the PI website or requested as a CD from your local PI representative.

Run PIXls Designer 7.
Click File-New-HiperPLC810.

Note the column headings (Figure 1). The gray cells under the "INPUTS" column are where the user may enter values. If they are left blank, then the default values shown to the right in the "OUTPUTS" column are used. Cells in the "OUTPUTS" column which do not have corresponding gray cells to their left are calculated values.

Sometimes the user will want to change a value that is an output variable (calculated value) that does not have a grey entry cell. For example, bulk capacitance "CIN_MIN" and "Holdup time" are directly related, but "CIN_MIN" is an output while "Holdup time" is an input. If the user wants to know hold-up time for a given bulk capacitance, a "Goal Seek" function is provided in the Tools menu. Goal Seek will adjust and find the value of an input (in this Case Holdup time) that yields the desired output (bulk capacitance).

ACDC_PLC810_030509; Rev.1.3; Copyright Power Integrations 2008	INPUTS	INFO	OUTPUTS	UNITS	ACDC_PLC810_030509_Rev1-3.xls; PLC810 Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					Design Title
Vacmin			85	V	Minimum AC input voltage
Vacmax			265	V	Maximum AC input voltage
Iacinmax			3.84	A	Maximum input AC rms current at Vacmin
Vbulk			385.00	V	Nominal PFC output voltage
Vbulkmax			411.95	V	Peak PFC OVP voltage (typical is 7% above Vbulk)
Vbulkmin			250.25	V	Minimum bulk capacitor voltage at the specified holdup time. Typical value is between 250 - 320 VDC. Max holdup time is at 250 V
fL			50.00	Hz	AC Line input frequency
Holdup time			20.00	ms	Bulk capacitor hold up time
CIN_MIN			140.32	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbulkmin to change bulk cap value
bulk ripple			10.79	V	Bulk capacitor peak to peak voltage (low freq ripple)
Vrippeak			390.40	V	Bulk cap peak value of ripple voltage
IAC			3.84	A	AC input rms current at VACMIN
IAC_PEAK			5.43	A	Peak AC input current at full load and VACMIN

Figure 1. Input Parameters Section of HiperPLC Design Spreadsheet.

Step 1. Enter Input Parameters (Figure 1), Enter Values for VAC_{MIN}, VAC_{MAX}, V_{BULK}, $V_{BULK(MIN)}$, f_L, and Holdup Time

Typical input voltage ranges are given in the table below.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100 / 115	85	132
230	195	265
Universal	85	265

Table 1. Typical Worldwide Line Input Voltage Ranges.

V_{BULK} is the nominal output voltage of the PFC stage. A value of 385 V is commonly used to provide sufficient voltage margin for a 400 V rated output capacitor to be used. If a different voltage is required, enter the value in this cell.

f_L is the nominal line frequency (50 or 60 Hz), $V_{BULK(MIN)}$ is the voltage at the end of holdup time and must be greater than 65% of V_{BULK}. This is also the voltage below which the LLC will not regulate when fully loaded. Further information on choosing these values is presented in later sections.

Step 2. Enter LLC Secondary Outputs (Figure 2), Enter Values for Vo_1, Io_1, Vd_1, Vo_2, Io_2, Vd_2

The suffix '1' refers to the main output, and the suffix '2' refers to the secondary output. If the design only requires one LLC output, leave the latter blank. The transformer turns ratio refers to the main, higher power output, Vo_1. For a 2-output LLC, the lower power output, Vo_2, can be either higher or lower voltage than Vo_1. Vd_1 and Vd_2 describe the voltage drops of the output rectifiers for outputs 1 and 2 respectively.

Step 3. Enter Stand-by (Auxiliary) Outputs, Enter Values for Vo_3, Vo_4, Io_3, and Io_4 (Figure 3)

These parameters describe the outputs of the standby PSU and are used to calculate the additional load on the PFC. If there is only one output for the standby PSU, leave Vo_4 and Io_4 blank.

Step 4. Efficiency and Loss Allocation (Figure 4)

Enter the estimated efficiencies of the PFC (at low line, full load), LLC (at full load), and standby (at full load, while PFC is on) converters. Typical numbers are 92% for a wide-range PFC (85/90 VAC minimum), 95% for a PFC (180 VAC minimum), and 93% for an LLC with a main output >12 V.

Step 5. Enter PFC Design Parameters (Figure 5) Enter Values for $f_{(NOMINAL)DESIRED}$ and K_{RP}

$f_{(NOMINAL)DESIRED}$ is the LLC and PFC operating frequency at full load (dictated by the LLC). This will affect both the PFC choke and LLC transformer designs. K_{RP} is the PFC choke current ripple factor, which is the ratio of the peak-to-peak ripple current, to the peak current, at the peak of the AC sinusoid, at AC input voltage equal to VAC_{MIN}, at full load. A typical range is 0.25 to 0.5. (See later sections) Diode bridge V_F describes the forward voltage drop each diode in the input bridge, and is used to calculate the bridge rectifier losses.

Enter LLC (secondary) outputs					The spreadsheet assumes AC stacking of the secondaries
Vo1	24.00			V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
Io1	9.00			A	Main output maximum current
Vd1			0.70	V	Forward voltage of diode in main output
Po1			216.00	W	Output Power from first LLC output
Vo2	12.00			V	Second Output Voltage
Io2	4.00			A	Second output current
Vd2	0.40		0.40	V	Forward voltage of diode used in second output
Po2			48.00	W	Output Power from second LLC output

Figure 2. Secondary Parameters Section of HiperPLC Design Spreadsheet.

Enter stand-by (auxiliary) outputs					
Vo3	5.00			V	Auxiliary Output 1 Voltage
Io3	2.00			A	Auxiliary Output 1 maximum current
Vo4				V	Auxiliary Output 2 Voltage
Io4				A	Auxiliary Output 2 maximum current

Figure 3. Standby Parameters Section of HiperPLC Design Spreadsheet.

Efficiciency and Loss Allocation					
P_LLC			264.00	W	Specified LLC output power
P_AUX			10.00	W	Auxiliary output power
P_PFC			300.29	W	PFC output power
P_TOTAL			274.00	W	Total output power (Includes Output power from LLC stage and auxiliary stage)
LLC_n_estimated			0.92		Efficiency of LLC stage
AUX_n_estimated			0.75		Efficiency of auxiliary output
PFC_n_estimated			0.92		Minimum efficiency of PFC front end stage
PIN			326.40	W	AC input power
Overall efficiency			0.84		Minimum system efficiency
Ploss_PFC			26.11	W	PFC stage power loss
Ploss_LLC			22.96	W	LLC stage power loss
Ploss_AUX			3.33	W	Auxiliary power loss
Ploss_TOTAL			52.40	W	Total power loss

Figure 4. Efficiency and Losses Parameters Section of HiperPLC Design Spreadsheet.

Enter PFC Design Parameters					
f_nominal_desired			100.00	kHz	Desired full load switching frequency. Recommended value 66 kHz to 132 kHz
Krp			0.35		PFC choke ripple current factor. Actual Krp tends to increase at higher current when using iron powder/Sendust cores, due to drop in inductance at higher current
Diode bridge Vf			0.70	V	Forward voltage drop of diode bridge
Rdson			0.18	ohms	PFC MOSFET Rdson - use high temp value from datasheet
Coss			21.76	pF	PFC MOSFET high voltage Coss from datasheet
tON			20.00	ns	MOSFET turnon current rise time. Check actual value
Qrr			50.05	nC	Average Qrr of boost diode over AC sinusoid

Figure 5. PFC Design Section of HiperPLC Design Spreadsheet.

PFC CHOKE Parameters					
Lpfc			435.00	uH	PFC choke inductance
ILpk			7.33	A	PFC choke peak current at VACMIN
AL	380.00			nH/t^2	nH per turn^2 (from magnetics datasheet). Note - This value decreases by as much as 15% if a belly-band is added to reduce EMI
n			33.83	turns	PFC choke number of turns
MLT	5.00			cm	Mean length per turn
AWG_Choke	22				PFC choke wire gauge
Equivalent Choke Metric Wire gauge			0.70	mm	Equivalent diameter of wire in metric units
Wire length			1.69	m	Length of wire used on PFC choke
Strands	3				Number of wires
DCR			32.37	m-ohms	DC resistance of wire at 25 C
DCR at 85 C			40.79	m-ohms	DC resistance of wire at 85 C
Irms_CHOKE			3.84	A	PFC choke rms current
DCR Cu loss			0.60	W	PFC choke DC Copper loss for reference at 85 C
ACR_PFC_Choke			81.58	m-ohms	Measure or calculate; add 26% to measured value to get 85 C value
HF Irms			0.67	A	RMS current of switching component
HF Cu loss			0.04	W	Copper loss due to switching component at 85 C
tot Cu loss			0.64	W	Total copper loss at 85 C
LM	10.00			cm	Magnetic path length of core used
Hpk			31.17	Oe	Peak MMF in Oersteds, calculated at low line
Hpk_SI			2481	A/m	Peak MMF in A/m, calculated at low line

Figure 6. PFC CHOKE Section of HiperPLC Design Spreadsheet.

LLC TRANSFORMER CALCULATIONS					
Po			271.90	W	Output from LLC converter including diode loss
Vo			24.70	V	Output at transformer windings (includes diode drop)
Ae	2.10			cm^2	Transformer core cross-sectional area
Lpar			178.62	uH	Parallel inductance. (Lpar = Lopen - Lser for integrated transformer; Lpar = Lmag for non-integrated transformer)
Lser			59.54	uH	Leakage inductance of integrated transformer; Leakage + external inductor for non-integrated transformer
Lopen			238.16	uH	Primary open circuit inductance for integrated transformer
C			33.71	nF	Series resonant capacitor
fnominal_desired			100.00	kHz	Desired full load switching frequency. Recommended value 66 kHz to 132 kHz
fnominal_actual			99.2	kHz	Expected frequency at nominal input voltage (VBULK) and full load
IRMS_LLC_Primary			1.94	A	Primary winding RMS current at full load and nominal input voltage (VBULK)
IRMS_LLC_Q1			1.37	A	RMS current through upper MOSFET in LLC half bridge
VMIN			240.2	V	Minimum Voltage on Bulk Capacitor at minimum switching frequency
f_AT_VMIN			54.00	kHz	Frequency at minimum Bulk capacitor voltage
fpar			55	kHz	Parallel resonant frequency (defined by Lpar + Lser and C)
fser			95	kHz	Series resonant frequency (defined by series inductance Lser and C)
fmin			57	kHz	Min frequency, at VBULK _MIN and full load. Set PLC810 minimum frequency to this value. Operation below this frequency results in loss of ZVS
NP_1			30		Primary winding number of turns
NS_1	4.00		4		Secondary winding number of turns
n_RATIO			7.58		Transformer turns ratio. Adjust this value so that fnominal_actual is close to fnominal_desired
Bpkfmin			1287	Gauss	First Quadrant peak flux excursion at minimum frequency.
BAC			1483	Gauss	AC peak to peak flux density (calculated at fnominal_actual, VBULK at full load)
LLC sense resistor			0.10	ohms	LLC current sense resistor
Pdiss_LLC_senseR			0.37	W	Power dissipation in LLC sense resistor

Figure 7. LLC Transformer Section of HiperPLC Design Spreadsheet.

Step 6. PFC CHOKE Parameters (Figure 6)

This section aids design using ferrite, iron powder or Sendust/ Koolmu cores. Both EE or toroid cores can be used. The inductance L_{PFC} and its peak current $I_{L(PK)}$ are calculated values and are strongly influenced by K_{RP}. H_{PK} (mmf), which is proportional to $I_{L(PK)}$, is also calculated. A_L is the value of inductance per turn squared, expressed in nH per turn squared, and is obtained from the core data sheet. Ideally use the value with the given H_{PK}, because for iron powder and Sendust A_L drops with current/mmf. Because the A_L value and H_{PK} are inter-related, some iteration will be necessary.

MLT (mean length per turn) is the average distance the wire traverses in each turn, and is a function of the core dimensions. It goes up slightly with multi-layer designs. It is used to calculate total wire length and DC resistance (DCR). In order to reduce AC resistance (ACR) loss and to make winding the choke easier, bifilar or trifilar, magnet wire can be used. Actual AC resistance (ACR) can be measured and entered. ACR should be measured on an LCR bridge, with frequency set to $f_{(NOMINAL)DESIRED}$. This test must be done with the core removed and therefore can only be easily done with an EE core. With toroidal cores, set ACR to the same value as DCR. This is a reasonable assumption if the number of winding layers is less than 3. L_M is the magnetic path length and is dependent on the core dimensions. H_{PK} is inversely proportional to L_M.

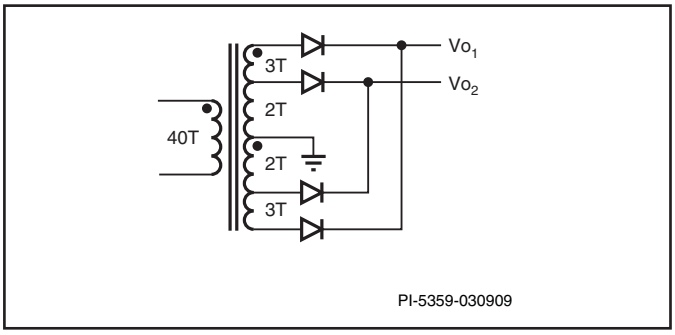


Figure 8. In This Example Transformer, NS_1 (which refers to Vo_1) is 5, and NS_2 (which refers to Vo_2) is 2.

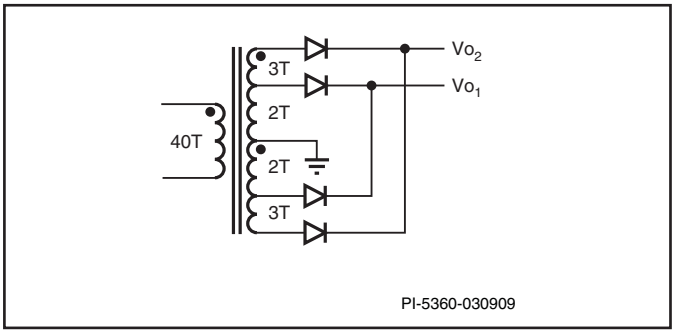


Figure 9. In This Example Transformer, NS_1 (which refers to Vo_1) is 2, and NS_2 (which refers to Vo_2) is 5.

If ferrite is the desired material for the PFC choke, the use of multifilar wire or Litz wire is recommended, because the large number of layers required by a typical ferrite choke will otherwise significantly raise the AC Resistance due to Proximity Losses despite the low AC ripple current inherent in continuous PFC designs.

When designing a ferrite PFC choke the following equations will apply:

$$B_P = \frac{100 \times L_{PFC} \times I_{L(PK)}}{N \times A_E}$$

Where B_P is the core peak flux density (T), which must be kept below 0.34 Tesla to prevent core saturation, L_{PFC} is the desired inductance (µH) from the PFC Design Section (Figure 6), N is the number of turns, A_E is the core effective cross sectional area (cm^2) from the core datasheet and $I_{L(PK)}$ is the peak PFC choke current (A) from the PFC Design Section (Figure 6).

For a given core and PFC design, N is adjusted to achieve the target peak flux density. In a typical application, the low ripple current of a continuous mode PFC design yields a correspondingly low AC flux density and core loss so that the highest efficiency is achieved by running the peak flux density as high as possible without saturation, which means setting B to 0.34 T. Once the turns are chosen, the air gap is adjusted until the desired inductance is achieved. An initial gap size, L_G (mm) can be estimated via the expression:

$$L_G = 40 \times \pi \times A_E \times \left(\frac{N^2}{1000 \times L_{PFC}} - \frac{1}{A_L}\right)$$

Where A_E is the core effective cross sectional area (cm^2) from the core datasheet, N is the number of turns, L_{PFC} is the desired inductance (µH) and A_L is the ungapped effective inductance (nH/N^2) from the core data sheet.

The gapped effective inductance, A_{LG} (nH/N^2), is useful when specifying the inductor design to a magnetics vendor and is given by:

$$A_{LG} = 1000 \times \frac{L_{PFC}}{N^2}$$

Where L_{PFC} is the desired inductance (µH) and N is the number of turns.

Step 7. LLC Transformer Calculations (Figure 7)

Core cross sectional area A_E is used to calculate flux density ($B_{PK(f_MIN)}$ and B_{AC}). Flux density and core area are inversely proportional.

After entering the parameters in steps 1 though 6, the PIXls spreadsheet will calculate suggested values for the 4 transformer/resonant tank variables: L_{PAR}, L_{SER}, C, and n_{RATIO} (turns ratio). These 4 variables will appear in the output column if the input column is left blank. Turns ratio is defined as the primary turns divided by secondary, where secondary turns is that of the main output turns (Vo_1) between the secondary ground pin, to the Vo_1 rectifier. (See Figures 8 and 9). These 4 variables can also set as inputs. The spreadsheet will perform a recalculation based on any new values entered.

The output of these calculations are f_{PAR} (parallel resonant frequency), f_{SER} (series resonant frequency), $f_{(NOMINAL)DESIRED}$ (actual frequency at full load and with nominal bulk voltage), V_{MIN}, $f_{(AT_VMIN)}$, and f_{MIN}. The spreadsheet will also create a graph of bulk voltage vs. frequency and primary MOSFET RMS current vs. frequency on a second spreadsheet page. Click the tab “PIXls Charts” at the bottom of the spreadsheet. Two load conditions are plotted for bulk voltage vs. frequency: full load, and minimum load.

V_{MIN} is the minimum bulk voltage at which the LLC can still deliver full load, and is slightly below the minimum frequency at which the LLC operates in ZVS. This is the minimum bulk voltage shown on the graph. The frequency that corresponds to V_{MIN} is $f_{(AT_VMIN)}$. f_{MIN} is a slightly higher frequency; which is the minimum frequency at which ZVS operation is maintained. It is acceptable to operate the LLC converter between f_{MIN} and $f_{(AT_VMIN)}$ V_{MIN} for short periods, such as during hold-up events, but it is preferable to operate above f_{MIN} in normal operation.

The initial values for the 4 input variables are calculated such that f_{SER} is slightly below $f_{(NOMINAL)DESIRED}$. However a different f_{SER} may be selected. (See appropriate sections for tradeoffs in setting f_{SER}). The initial 4 recommended values are also set such that:

$$L_{PAR} = 3 \times L_{SER}$$

The designer can change any of the 4 input variables and examine the results. In some cases the designer has limited choices for L_{SER} and/or C and so cannot use the spreadsheet recommended values, or the designer may want to use a different f_{SER} or L_{PAR} to L_{SER} ratio.

PRIMARY					
Primary gauge	40.00			AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.08	mm	Equivalent diameter of wire in metric units
Primary litz strands	125.00				Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Primary parallel wires	1.00				Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Primary			29.83	m-ohm/m	Resistivity in milli-ohms per meter
Transformer primary MLT	7.00			cm	Mean length per turn
Primary turns			30.31		Number of primary turns
Primary DCR 25 C			63.31	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			84.83	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current	1.50			A	Measured RMS current through the primary winding
ACR_Trf_Primary			135.73	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.31	W	Total primary winding copper loss at 85 C

Figure 10. LLC Transformer Primary Section of HiperPLC Design Spreadsheet.

Separate Series Inductor (For non-integrated transformer only)					Ignore this section if using integrated magnetics
Lsep			59.54	uH	Desired inductance from separate inductor
Ae_Ind	0.53			cm^2	Inductor core cross-sectional area
Inductor turns	15.00		15		Number of primary turns
BP_fnom			2202	Gauss	AC flux for core loss calculations (at fnom and full load)
BP_fmin			2913	Gauss	Peak flux density, calculated at minimum frequency fmin
Inductor gauge	40.00			AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.08	mm	Equivalent diameter of wire in metric units
Inductor litz strands	125.00				Number of strands used in Litz wire
Inductor parallel wires	1.00				Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			29.83	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT	7.00			cm	Mean length per turn
Inductor DCR 25 C			31.32	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			41.97	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			67.16	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.15	W	Total primary winding copper loss at 85 C

Figure 11. Separate Series Inductor Section of HiperPLC Design Spreadsheet.

The designer can fix L_{SER} or C to a different value, then re-optimize the 3 other variables. For a given value of f_{SER} and $f_{(NOMINAL)DESIRED}$ there is an optimal set of values for the 4 input variables. Optimal results are when V_{MIN} of the LLC is at or slightly below $V_{BULK(MIN)}$. When V_{MIN} is far below $V_{BULK(MIN)}$, the LLC will be running less efficiently due to higher circulating primary currents. The one other degree of freedom is the ratio of L_{PAR} to L_{SER}. A higher ratio yields lower currents, but it lowers f_{MIN}, thus raising flux density at f_{MIN} which may dictate a larger core cross-sectional area or more secondary turns.

Flux density is inversely proportional to frequency and secondary turns (NS_1), and directly proportional to output voltage. The gap, primary magnetizing inductance, and L_{PAR}, do not affect flux density. NS_1 must be adjusted to control flux density. NS_1 cannot be made arbitrarily high in order to reduce flux density, as this will reduce the diameter of the wire that can be used for both primary and secondary windings increasing resistive losses. Conversely, NS_1 cannot be made too low (irrespective of avoiding core saturation), because low secondary turns yield high B_{AC} resulting in excessive core losses. This is discussed in more detail below.

In order to re-optimize the 3 other variables after fixing L_{SER} or C, follow this procedure.

1. Decide on f_{SER}.
   a) If fixing L_{SER}, (letting it be the independent variable), use Goal Seek to adjust C in order that f_{SER} is at the desired value.
   b) If fixing C, (letting it be the independent variable), use Goal Seek to adjust L_{SER} in order that f_{SER} is at the desired value.
2. Next, decide on a ratio, k, of L_{PAR} to L_{SER}, A typical range is 2 to 4. Enter in the value for L_{PAR} where:

$$L_{PAR} = k \times L_{SER}$$

Where k is inductance ratio.

3. The previous 2 steps will set L_{PAR}, L_{SER}, and C. The final step is to set the turns ratio in order to achieve the desired $f_{NOMINAL(ACTUAL)}$. Use Goal Seek again, and let it adjust the value of N_{RATIO} (turns ratio) to achieve the desired value of $f_{NOMINAL(ACTUAL)}$. Examine the resulting value of V_{MIN}. If it is too low or too high, adjust the independent variable (L_{SER} or C), repeating with Goal Seek, until an acceptable value of V_{MIN} is achieved.

The designer may wish to save the results and try different values of k (inductance ratio), for a given f_{SER}. Different value of f_{SER} may also be tried. Examine $I_{RMS(LLC)PRIMARY}$ (primary current) or $I_{RMS(LLC)Q1}$ (MOSFET current). These are proportional to each other. Examine $B_{PK(f_MIN)}$ (flux density at f_{MIN}) and B_{AC} (pk-pk AC flux density at nominal bulk voltage). These are the figures of merit to consider. Lower primary currents tend to yield higher efficiency. Check that $B_{PK(fMIN)}$ does not reach saturation, and that AC flux is not excessive, which would lead to high core temperatures. Higher frequency ferrite core materials, such as PC44 or 3F3 may be used to reduce core losses.

Note that when using an integrated transformer (large built in leakage inductance), transformer leakage inductance (L_{SER}) changes when primary turns are changed. This leakage inductance is proportional to the square of the primary turns. If the optimal L_{SER} is greater than the actual leakage inductance, the designer can opt to add an external resonating inductor. For this inductor, gapped ferrite and Litz wire are recommended due to the high AC flux and resultant proximity losses.

Another input in the “LLC Transformer calculations” section is NS_1 (secondary turns), and from this, NP_1 (primary turns), is calculated, from N_{RATIO} (turns ratio).

“LLC sense resistor” is the recommended value based on the primary currents, and $P_{DISS(LLC)SENSER}$ is the power dissipation or the resistor at full load and nominal bulk voltage.

Step 8. PRIMARY (Figure 10), Enter the Primary Wire Parameters

Enter values for “Primary Gauge”, “Primary Litz Strands”, and “Primary Parallel Wires”. For example, if using 2 bundles of #40 Litz wire with 125 strands each, enter 40, 125, and 2. If using bifilar #27 magnet wire (not Litz), enter 27, 1, 2. The spreadsheet will calculate the losses accordingly.

The spreadsheet estimates ACR (AC resistance), displayed in the output column. You can override this number by entering actual ACR in the input column. The ACR can be measured on an LCR bridge by removing the core and setting the bridge measurement frequency to the LLC nominal frequency.

The spreadsheet also calculates DCR (DC resistance). Measure the actual resistance using a Kelvin connected resistance measurement setup, and compare. If the measured resistance is significantly higher than calculated, the Litz wire used may not have been terminated on the transformer pins properly. It requires careful attention to make solder penetrate all the way into the inner strands.

Step 9. Separate Series Inductor (For Non-Integrated Transformer Only) (Optional) (Figure 11)

This section is for designing a separate series inductor if the designer chooses this instead of integrated magnetics. The use of gapped ferrite inductors and Litz wire, in order to reduce losses associated with the high AC flux, is strongly recommended. Enter the desired inductance in L_{SEP} to override the default value which is taken from L_{SER}. Use a value of L_{SEP} where:

$$L_{SEP} = L_{SER} - L_{LK}$$

where L_{LK} is the measured leakage inductance of the main transformer.

The descriptions of the variables to be entered are similar to those described in the “Primary” section.

Step 10. Winding 1 (Vo_1) and Winding 2 (Vo_2) (Figure 12)

Enter the wire specifications and the number of turns for each output. The number of turns in this section is specified in the same manner as described in Figures 8 and 9. The spreadsheet assumes “AC Stacking” and will correctly calculate the winding currents and losses – i.e. the calculation of the current in the winding of the lower voltage output will include the current of the higher voltage winding.

The spreadsheet calculates DCR (DC resistance) at 25 °C and at 100 °C. Measure the actual resistance using a Kelvin-connected resistance measurement setup. If the measured resistance is significantly higher than the calculated 25 °C DCR, the Litz wire used may not have been terminated properly.

The spreadsheet estimates ACR (AC resistance), displayed in the output column. You can override this number by entering actual ACR in the input column. The ACR can be measured on an LCR bridge by removing the core and setting the bridge measurement frequency to the LLC nominal frequency. AC RMS and DC currents are calculated by the spreadsheet, which uses them to determine ACR and DCR losses.

Step 11. Total Copper Loss Calculation (Figure 13)

The total losses are calculated for all windings.

Step 12. Turns Calculator (Figure 14)

The turns calculator is not connected to any other part of the spreadsheet. It is used for multi-output designs, in order for the designer to experiment with different combinations of secondary

Winding 1 (Vo1)					Note - Power loss calculations are for each winding half of secondary
Sec 1 Wire gauge	40			AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.08	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	175				Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Parallel wires sec 1	2				Number of parallel individual wires to make up Litz wire
Resistivity_25 C_sec1			10.65	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT	7.00			cm	Mean length per turn
Sec 1 Turns			4.00		Secondary winding turns (each half)
DCR_25C_Sec1			1.49	m-ohm	Estimated resistance at 25 C (for reference)
DCR_100C_Sec1			2.00	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Sec 1 RMS current			14.15	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
DCR_Ploss_Sec1			0.32	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec1			3.20	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			1.28	W	Estimated AC copper loss (both secondary halves)
Total secondary winding Copper Losses			1.60	W	Total (AC + DC) winding copper loss for both secondary halves
Winding 2 (Vo2)					Note - Power loss calculations are for each winding half of secondary
Sec 2 Wire gauge	40			AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.08	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands	175				Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Parallel wires sec 2	1				Number of parallel individual wires to make up Litz wire
Resistivity_25 C_sec2			21.31	m-ohm/m	Resistivinty in milli-ohms per meter
Transformer Secondary 2 MLT	7.00			cm	Mean length per turn
Sec 2 Turns	2.00				Secondary winding turns (each half)
DCR_25C_Sec2			2.98	m-ohm	Estimated resistance at 25 C (for reference)
DCR_100C_Sec2			4.00	m-ohm	Estimated resistance at 100 C for half secondary (approximately 33% higher than at 25 C)
Sec 2 RMS current			20.44	Arms	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
DCR_Ploss_Sec1			1.35	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			6.40	m-ohm	Actual measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			5.34	W	Estimated AC copper loss (both secondary halves)
Total secondary winding Copper Losses			6.69	W	Total (AC + DC) winding copper loss for both secondary halves

Figure 12. LLC Transformer Secondary Section of HiperPLC Design Spreadsheet.

Total Copper loss calculation					Does not include fringing flux loss from gap
Primary copper loss (from Primary section)			0.31	W	Total primary winding copper loss at 85 C
Secondary copper Loss			8.30	W	Total copper loss in secondary winding
Transformer copper loss			8.60	W	Total copper loss in transformer (primary + secondary)

Figure 13. LLC Transformer Copper Loss Section of HiperPLC Design Spreadsheet.

TURNS CALCULATOR					This is to help you choose the secondary turns - not connected to any other part of spreadsheet
V1			24.00	V	Target Output Voltage Vo1
V1d1			0.70	V	Diode drop voltage for Vo1
N1	4.00				Total number of turns for Vo1
V2			11.95	V	Expected outputV
V2d2			0.40	V	Diode drop voltage for Vo2
N2	2.00				Total number of turns for Vo2

Figure 14. Transformer Turns Calculator Section of HiperPLC Design Spreadsheet.

turns and diode voltage drops to achieve the correct output voltages. After the number of turns for the main output has been determined, this number should be entered into NS_1 in the "LLC Transformer Calculations" section in order to properly calculate the flux density.

Layout, Decoupling, and EMI Recommendations

It is recommended that the designer refer to the HiperPLC data sheet for detailed layout and decoupling recommendations related to the PLC810PG. A small ferrite bead in the gate pin of the PFC MOSFET can help prevent parasitic self-oscillation. This will also slow down the drive so the PFC gate resistors may need to be adjusted.

A small ferrite bead on the MOSFET Drain lead can also greatly reduce radiated EMI. However, this can cause an increase in Drain voltage stress and which should be measured during startup. It may be necessary to slow down the turn-off drive to ensure acceptable Drain voltage stress. Be mindful that some ferrite bead material types are conductive, Ferrite type 43 works well for this purpose having high DC resistivity.

In laying out the secondary circuit, it is crucial that the output rectifiers be mounted close to the transformer secondary pins using short traces. If using a post filter, or multiple output capacitors, the last capacitor should be mounted close to the output connector. This will reduce output ripple from switching noise spikes.

Symmetry in the layout from the transformer secondary pins to each of the rectifiers is required for proper sharing of currents in the secondary halves. Poor sharing will result in increased secondary losses and increased output ripple voltage. The symmetry of the secondary winding halves inside the transformer is likewise important.

Like any other power supply, the EMI filter should be located away from the main switching magnetics (PFC choke and LLC magnetics). This is to prevent noise coupling and consequent high conducted EMI. The EMI filter components shown connected to AC next to the inlet in the schematic should be physically located close to the AC inlet.

LLC converters tend to generate low EMI, especially those with integrated magnetics (transformer has built-in leakage inductance). This is because integrated magnetics require the primary winding to be physically separated from the secondary windings, resulting in low primary-secondary coupling capacitance. This reduces common mode noise transmission across the transformer. Conversely, PFC converters generate a lot of noise. Techniques for reducing EMI include those mentioned in the data sheet. A grounded flux-suppression band on the PFC choke also assists in reducing EMI. A 'Z' winding technique on the choke can also help, especially with toroid cores, as can grounding heatsinks and the LLC transformer core. A flux-suppression (shorted) band on the LLC integrated transformer is not recommended as it can lower efficiency and the effects of this band should be carefully investigated prior to adoption.

Selection of Switching Frequency

The PLC810PG runs the LLC and PFC at the same frequency. The recommended frequency range for any PFC is 66 to 132 kHz. Higher frequencies yield smaller magnetics for both PFC and LLC, but due to PFC diode reverse recovery losses, the PFC efficiency reduces as frequency increases. 66 kHz operation benefits from a 2nd harmonic of 132 kHz, which is below 150 kHz (typically EMI standards do not require measurement below 150 kHz). 100 kHz switching is a good compromise for locked frequency designs, and 132 kHz has value in reducing magnetics size. Switching frequencies above 132 kHz tend to increase the cost and complexity of the EMI filter and provide progressively less benefit in reducing the size of magnetics. The LLC is frequency controlled and dictates the PFC switching frequency. Ideally the LLC converter should be designed to run close to its series resonant frequency (when at nominal input voltage) so that the operating frequency of the LLC changes very little as load varies. Slight changes in frequency will occur in order to reject the 100/120 Hz ripple present on the bulk capacitor. This produces a frequency jitter effect which can in some cases reduce EMI. During hold-up time, in order to maintain regulation, the LLC will lower its switching frequency towards a selected minimum (f_{MIN}) with decreasing input voltage.

PLC810PG PFC Basic Operation

The purpose of the PFC circuit is to draw a sinusoidal current in phase with the input voltage, reducing the current harmonics and raising power factor close to unity. The PLC810PG PFC boost controller also regulates the output (bulk capacitor) voltage. A typical set point is 385 V for a wide-input-range design. 385 V is slightly higher than the peak of an input

maximum voltage of 265 VAC and is low enough so that during a load dump (full load to light load transient), the typical OVP set point of 105% keeps the bulk voltage below 412 V. This is low enough to allow the use of a 420 V bulk capacitor which has cost advantages over higher voltage rated capacitors.

Most continuous-mode PFC controllers employ an inner current loop which tracks a sinusoidal reference derived from the input voltage. The PLC810PG draws sinusoidal current without using a sinusoidal reference (thus saving a pin and associated external components). This is accomplished through OFF-time control where the off-duty-cycle is kept proportional to the average inductor current (measured over several switching cycles). The PLC810PG PFC controller exploits the fact that the input voltage (V_{IN}) is effectively constant over several switching cycles, because the input AC line frequency is 50-60 Hz whereas the switching frequency is >1000 times higher.

The PLC810PG PFC section controls the PFC OFF-time. The Volt-Second balance equation for a continuous mode boost converter yields the OFF-time duty-cycle:

$$D_{OFF} = (1 - D) = \frac{V_{IN}}{V_{OUT}} \quad (1)$$

Where V_{IN} is the rectified version of the AC sinusoidal voltage. The input current wave shape follows the averaged inductor current (averaged over several switching cycles), and thus the PFC looks like a resistor, to the AC input mains.

$$I_{IN} = I_{SENSE} = \frac{V_{IN}}{R_E} \quad (2)$$

Where R_E is the equivalent load resistance that the AC input sees. The current I_{SENSE} is the current sensed by the PFC current-sense resistor, fed into the ISP pin.

Rearranging,

$$V_{IN} = I_{SENSE} \times R_E \quad (3)$$

Combining the equation (1) and (3) we get

$$D_{OFF} = I_{SENSE} \frac{R_E}{V_{OUT}} \quad (4)$$

$\frac{R_E}{V_{OUT}}$ is a slow changing proportionality constant.

Because R_E and V_{OUT} are held relatively constant, the above equation shows that D_{OFF} is proportional to I_{SENSE}. If the value R_E/V_{OUT} changes slowly with respect to the 60 Hz waveform, the average current will be in-phase with the input voltage.

Inside the PLC810PG, the proportionality constant between D_{OFF} and I_{SENSE} is represented by the voltage on the VCOMP pin, which has a nominal linear range of 0.5 V to 2.5 V. 0.5 V signifies maximum input AC current (low line, full load), and 2.5 V signifies minimum input AC current (high line, min load).

Internally,

$$D_{OFF} = - V_{ISP}(V_{COMP} - 0.5\,V) \times 7.5$$

0.5 V is an offset term, 7.5 is a scaling term, and V_{ISP} is the inductor current sense resistor voltage applied on the ISP pin (which is negative). The ISP pin also implements pulse by pulse current limiting which during operation is nominally at 0.43 V. At light load D_{OFF} diverges from this equation due to a proprietary scheme to allow proper operation. The inductor current sense signal is internally coupled via a low pass filter to remove the switching component. The external RC filter for the ISP pin is only required to filter out high frequency spikes.

The output voltage is regulated by changing the VCOMP pin voltage. A transconductance error amplifier is employed for this purpose. If the output voltage is too high, the VCOMP pin voltage will be adjusted upwards which will reduce the AC input current; if the output voltage is too low, the VCOMP pin voltage will be adjusted downwards which will increase the AC input current.

The VCOMP pin is internally connected to the output of an operational transconductance amplifier. The output of this amplifier is a current proportional to the error on the FBP pin:

$$I_{VCOMP} = (V_{FBP} - 2.2) \times 85\,\mu\text{A/V}$$

The FBP pin senses the PFC output voltage via a resistor divider. When the output is regulated, the voltage on the FBP pin will nominally be 2.2 V (parameter name FBP_{REF}). The current I_{VCOMP} charges or discharges the compensation network on the FBP pin. (See Figure 16). Because D_{OFF} is a function of the VCOMP pin voltage, the system gain is a function of this network. This network sets the loop-gain and shapes the frequency response. The loop-gain needs a cross-over frequency well below 50/60 Hz in order to achieve high power factor. The bulk capacitor will see a rectified version of the input AC current, which has a 100 or 120 Hz fundamental component (as well as the high frequency switching current). This 100/120 Hz AC current will produce voltage ripple. If the gain-crossover frequency is too high, the feedback loop will attempt to correct for this voltage ripple and the input AC current will be distorted.

Basic PFC Equations

Because a PFC has near unity power factor, the AC RMS voltage and RMS current are related by:

$$I_{AC} = \frac{P_{IN}}{V_{AC}}$$

Input power is related to converter efficiency and output power:

$$P_{IN} = \frac{P_{OUT}}{\eta}$$

Worst case efficiency (and worst case input current) occurs at minimum input voltage (85 VAC or 90 VAC for a typical design). The peak of the input AC current is $\sqrt{2}$ times the AC RMS current.

$$I_{ACPK} = \sqrt{2} \times \frac{P_{OUT}}{\eta \times V_{ACMINRMS}}$$

The choke current wave-shape will be a rectified version of the input sinusoid, with the switching frequency sawtooth superimposed on it. With a continuous mode design, this sawtooth peak-to-peak value will be smaller than the 100/120 Hz component.

The factor K_{RP} is defined as the ratio of peak-to-peak ripple current, to I_{ACPK}, at the peak of the AC sinusoid under low line and full load operating conditions.

$$K_{RP} = \frac{I_{RIPPLE}}{I_{ACPK}}$$

The smaller the K_{RP} factor, the smaller the high frequency current ripple, and the more deeply continuous the operation.

The maximum peak current required by the PFC will occur just after an AC dropout wherein the bulk voltage drops almost to $V_{BULKMIN}$, during a low line condition. It is during this condition that minimum switching frequency and maximum transient K_{RP} occurs. This transient K_{RP} will be higher than the K_{RP} during steady state operation at maximum load and low line. For this reason, check performance during an AC dropout at minimum AC voltage. Gradually increase the length of the dropout until the bulk voltage drops to near $V_{BULKMIN}$, and check that the PFC is capable of recovering.

PFC Component Selection

The PIXls Design Spreadsheet is designed to help the designer calculate various current stresses and component values for the PFC.

PFC Inductor Calculation

The inductor value determines K_{RP}. Higher inductance yields lower K_{RP}. The spreadsheet takes K_{RP} as an input and calculates inductance and current stresses. Lower K_{RP} means lower losses associated with the ripple and peak currents, but requires more turns (unless a larger core is used) and therefore increases choke copper losses. Typical K_{RP} values range from 0.2 to 0.5. Note that with iron-powder and Sendust™/KoolMu™ type cores, the inductance reduces at higher currents, so the inductance at high current will be less than the measured small-signal inductance. Therefore for a given small-signal inductance, the actual K_{RP} at high current will be greater than that predicted by the spreadsheet.

K_{RP} is defined at the nominal switching frequency. Higher switching frequency, yields a lower K_{RP} for a given inductance, or a lower inductance for a given K_{RP}. During light load operation (which is at higher frequency so the LLC can regulate its output), the current ripple will be small.

With the typical K_{RP} range of 0.2 to 0.5, using an EE core, the winding will typically have 3-5 layers. With this many layers, the AC resistance (due to skin-effect and proximity losses) increases and the I^2R_{AC} heating of the winding becomes significant. In this case, bifilar or trifilar windings can significantly reduce the copper losses. Continuous conduction mode PFC designs do not generally require Litz wire (unlike discontinuous conduction mode PFC designs).

The inductor core material (and turns) must be chosen so that the choke does not saturate at peak current values. A compromise between the core material cost, power dissipation, temperature and inductance roll-off at higher current levels is required.

To prevent saturation, calculate the magneto-motive force (mmf),

Where

$$H_{PK} = I_{PK} \times \frac{N}{l}$$

H_{PK} is in Ampere-turn (SI) or Oersteds (CGS),
N is number of turns
l is the magnetic path length of the core

Refer to the PIXls Design Spreadsheet for calculation of this parameter. Note that for iron powder cores such as Sendust or KoolMu, H (magnetic field strength) is a better parameter than B, flux density, to determine core saturation, because the core is highly nonlinear (permeability drops with H).

Sendust or KoolMu cores are well suited for PFC chokes because they have relatively high B_{SAT} (saturation flux density), compared to gapped ferrite, which results in a choke design with fewer turns, low copper losses, and acceptable core losses. A gapped ferrite core design would have to be much larger, resulting in much higher copper costs. The large number of layers required will also drive up AC resistance, further increasing losses and increasing copper size and cost, and possibly make Litz wire necessary even for continuous conduction mode designs.

Refer to the appropriate KoolMu application notes when starting an inductor design, given the inductance required, RMS current, and peak current requirements from the PIXls spreadsheet. Select the inductance at the peak current expected and use this value in the spreadsheet. Also use the AL value (inductance per turns squared) value at the expected H and enter this into the spreadsheet so that it will calculate the correct number of turns. The inductor design is a compromise between reducing the ripple current and reducing the inductor cost and size. A higher inductance value will reduce the ripple current at the switching frequency thus reducing bulk capacitor ripple current. A reduced inductor value will reduce the cost of the inductor but will increase ripple current and reduce overall efficiency.

For a small-sized core, there are tradeoffs between using more turns of thinner wire and fewer turns of thicker wire. A design with higher turns (if it reduces K_{RP} from the 0.5 to 0.3 range) can improve system efficiency, but will increase the temperature of the winding. Part of the inductor design involves thermal testing. Monitor the core and winding temperatures separately at minimum AC input voltage and maximum load. If the core is significantly hotter than the winding, increase the number of turns to balance the temperature, and vice versa. Balancing these temperatures tends to improve overall efficiency. Compare the DCR of the winding vs. the ACR (measured at the switching frequency on an LCR meter and with the core removed). Enter the ACR into the PIXls spreadsheet. The spreadsheet will calculate the losses due to the fundamental of the switching frequency. If the copper loss due to the ACR is excessive, increase the inductance (which requires more turns and raises DCR but reduces ACR copper losses due to reduced ripple current), or use multiple strands of finer wire such as using bifilar or trifilar windings.

Bulk Capacitor Value

There are 2 main factors that set the PFC output (bulk) capacitor size. First is the hold-up time, and second is the ripple current rating required. The PLC810PG has ripple-current cancellation, reducing the ripple current in the bulk capacitor compared to conventional solutions.

The hold-up time requirement will dictate the minimum capacitance, but a given bulk capacitor of this capacitance may have insufficient ripple current capability. In this case, select a bulk capacitor from a different family which has the required ripple current rating. Alternatively, a larger capacitance value, or two bulk capacitors may be used. Two capacitors of half the capacitance value will have more ripple current capability than a single capacitor (but will typically be higher cost).

During hold-up, the bulk capacitor voltage falls. The PLC810PG will shut off the LLC when the bulk voltage reaches $V_{SD(L)}$ which is nominally 65% of the set-point. For a 385 V design, 65% corresponds to approximately 250 V. In this case, in order to obtain maximum hold-up time for a given bulk capacitance, the LLC converter should be designed to be capable of operating with a bulk voltage down to 250 V (set parameter $V_{BULKMIN}$ in the spreadsheet to 250 V). However, the designer can choose to design the LLC to only operate down to a higher minimum voltage, (such as $V_{BULKMIN}$ = 275 V), in order to improve LLC efficiency. The compromise is that the increase in minimum operating voltage will increase the bulk capacitance required to provide a given hold-up time. If the bulk capacitance required to meet the ripple current is larger than needed to achieve the required hold-up time, then the designer can opt to increase $V_{BULKMIN}$ to increase LLC efficiency without incurring a cost penalty.

The spreadsheet calculates hold-up time and estimates ripple current.

Note that hold-up time is proportional to

$$C_{BULK} \times (V_{SETPOINT}^2 - V_{BULKMIN}^2)$$

Where $V_{BULKMIN}$ is the LLC input minimum voltage.

Therefore as $V_{BULKMIN}$ is increased, hold-up time rapidly reduces.

High Frequency Input Capacitor

The input capacitor which is positioned on the output of the input bridge rectifier, is a high frequency ripple filter. It can also be considered to be part of the EMI filtering. Typically this capacitor is a high quality film type such polypropylene in order to have the required current capability. The voltage rating needs to be at least the 107% of the PFC output voltage set point, plus any de-rating. For a 385 V output, a 500 V capacitor will typically be used. This capacitor will see a large ripple current, close to that of the PFC choke ripple current, and must be rated accordingly.

For a 100 kHz switching frequency, a value of between 0.1 μF and 0.33 μF per 100 W of output power is recommended. A large value will reduce the differential EMI and thus reduce the size of the differential EMI filter components (smaller X-capacitors, and less differential-mode leakage inductance required in the common mode chokes in the EMI filter). Because the input capacitor does not need to be a Safety-rated component, it is typically less costly to enlarge this capacitor than it is to increase the size of X-capacitors. However, making this capacitor too large will increase the zero-crossing distortion of the PFC input current waveform, which is worst at high input voltage and light load. Note that most PFC specifications do not require a very high power factor nor low distortion at very light load and maximum input AC voltage.

PFC Switching MOSFET and PFC Boost Diode

MOSFET and boost diode are chosen for a voltage rating of at least 500 V, to withstand a maximum transient PFC voltage of 107% of nominal PFC output voltage plus any parasitic inductive spikes. (107% is the maximum PFC OVP setpoint). The inductor peak-current is also the peak-current in the switching MOSFET and boost diode.

The choice of these two power component depends on the power output and heatsinking selected.

Generally a power budget is set for these power components to allow the PFC stage to meet its efficiency target at low line (typically 91%-93% at 90 VAC). The PFC efficiency rapidly improves as input voltage is increased. The spreadsheet section “PFC, FET, Diode and Output Parameters” provides power losses for the MOSFET, input bridge and current sense resistor.

The MOSFET RMS current increases as K_{RP} is increased. A larger MOSFET will improve efficiency, up to a point. A very large MOSFET will have a large C_{OSS} (Drain-Source capacitance), which will impact efficiency. A larger MOSFET will also require larger gate drive transistors.

The switching losses in a PFC are mainly the losses in the PFC MOSFET associated with the boost diode reverse recovery charge (Q_{RR}), plus the turn-on/turn-off crossover losses.

Q_{RR} varies widely with diode type. The best low/moderate cost ultrafast PFC boost diodes are capable of very good efficiency at 100-132 kHz switching frequency, in the range of 91-93% at 90 VAC. Every turn-on edge of the MOSFET in a continuous mode PFC will have an energy loss (E_{RR}) associated with Q_{RR} and PFC output voltage:

$$E_{RR} = Q_{RR} \times V_{SETPOINT}$$

Q_{RR} is a function of the diode current flowing just before reverse recovery. Peak diode current varies over the AC input phase angle, and thus Q_{RR} also varies. The average E_{RR} will be less than that at the peak of the sinusoid. The total loss in the MOSFET due to Q_{RR} is multiplied by the switching frequency.

The turn-on/turn-off crossover losses will be a function of MOSFET switching speed which are in turn a function of the gate-drive circuit (see the PLC810PG data sheet for gate-drive circuit recommendations). The gate drive resistors which determine switching speed have a significant effect on both efficiency and EMI. Because there are several low cost ways to

reduce EMI from the PFC, such as by adding a shorted belly band on the EMI choke, the use of these methods are recommended, so that efficiency by speeding up the PFC gate drive can be maximized. Note that MOSFETs with larger gate capacitance require larger gate drive currents and associated driver components.

Boost diode selection is critical. A diode with a fast recovery characteristic is important. Losses associated with the boost diode must be taken into account in the power-loss budget. Other parameters to consider when selecting the boost diode are the maximum reverse voltage, and forward current. 500 V or 600 V rated diodes are typically used for 385 V or 400 V output PFCs. 1 A to 3 A per 100 W of output power is a commonly used approximation for 90 VAC input, 385-400 V output PFC's.

Gate Drive Circuit

Refer to the PLC810PG data sheet for the recommended gate drive circuit.

Voltage Feedback Components

The FBP pin is used to sense the PFC output voltage (bulk capacitor voltage). The FBP pin is a high impedance voltage sensing pin and a simple resistor divider is used to sense bulk capacitor voltage. In this resistor divider the lower resistor should have a value of between 10 kΩ and 22 kΩ. Note that this resistor divider will dissipate power and increase power consumption in standby mode. A larger resistance than 22 kΩ can lead to errors due to leakage current in the FBP pin.

The resistor divider should be designed to provide 2.2 V (V_{FBPREF}) to the FBP pin when the PFC voltage is at the set-point. Because the voltage across the upper resistor is typically >380 V, care must be taken that the upper resistors are rated to withstand this voltage. A typical application will use several resistors in series. 1% resistors are recommended to ensure accurate OVP sensing. The OVP threshold of the PLC810PG ($V_{OV(H)}$) is 107% of the set-point (maximum). For a 385 V set-point, this corresponds to an OVP of 412 V. With 1% resistors, a 420 V bulk capacitor may be used subject to the designer's derating guidelines.

Detailed PFC Voltage Loop Compensation Analysis

A requirement in typical PFC converters is to keep the voltage loop bandwidth less than half the line frequency in order to avoid distortion of the AC line current. The distortion is a result of the voltage-loop attempting to regulate the 120 Hz ripple on the output of the PFC. The voltage loop bandwidth must be kept low to avoid this (8-12 Hz is typical). A compromise is necessary between the need for high gain that ensures good dynamic response in the error amplifier and low gain in order to avoid distortion.

Figure 15 shows the PFC small signal voltage loop blocks.

V_{FBREF} is the voltage on the FBP pin when the system is in regulation, nominally 2.2 V. The FBP pin is internally connected to the non-inverting input of the internal error amplifier and operational transconductance amplifier (OTA).

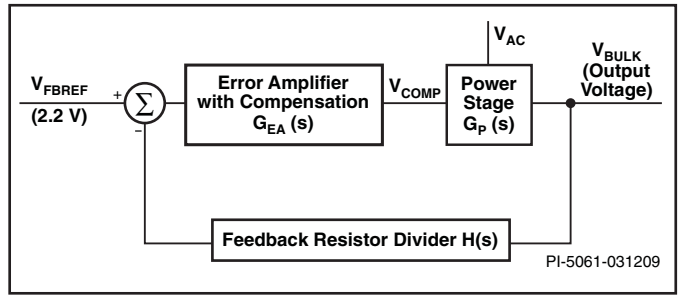


Figure 15. Simplified PFC Feedback Small-signal Loop Block Diagram.

The open loop gain of the voltage loop is:

$$T(s) = -G_P(s) \times G_{EA}(s) \times H(s)$$

Where (see Figure 16)

$$H(s) = \frac{R5}{R4 + R5}$$

H(s) is simply the ratio of FBP_{REF} to V_{BULK} (nominal bulk voltage in regulation). For a set point of 385 V:

$$H(s) = 2.2\,V/385\,V$$

The input of the power stage $G_{P(S)}$ is the VCOMP pin voltage, and the output is the bulk capacitor voltage. Given the PFC modulator characteristics, and the fact that the LLC DC-DC stage appears as a constant power load, the resulting small signal transfer function at low frequency is:

$$G_P(s) = 12 \times R_{SENSE}\left(\frac{P_{OUT}}{V_{IN(RMS)}}\right)^2 \times \frac{R_{LOAD}}{s(R_{LOAD} \times C_{BULK}) + 1}$$

Where R_{SENSE} = PFC current sense resistor value, C_{BULK} is the bulk capacitor value, P_{OUT} is the load power rating, and R_{LOAD} is the equivalent load resistance.

$$R_{LOAD} = \frac{P_{OUT}}{V_{BULK}}$$

The multiplier, 12, is a scaling factor built into the PLC810PG. Note that the bulk capacitance and load resistance form a pole at very low frequency. The gain at DC is proportional to the equivalent load resistance. The compensation network $G_{EA}(s)$ must have less than 45° of phase lag at the crossover frequency in order for the loop gain to have at least 45° of phase margin. The power stage gain is highest at maximum input current (full

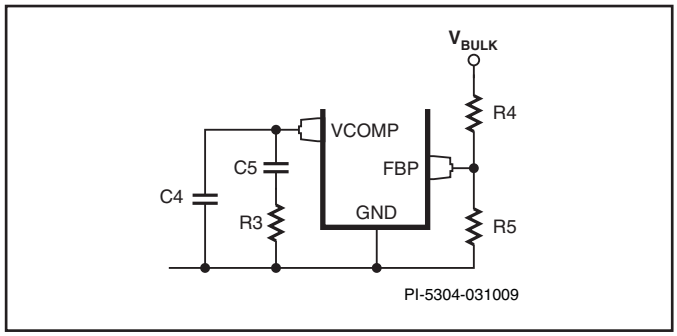


Figure 16. PFC Compensation Components.

load and minimum AC input voltage), and thus is the condition that needs to be designed for. This maximum gain point is where the potential for oscillation and AC current distortion occur. At lower AC input current (lighter load or higher input voltage), the gain is lower and thus of less concern.

Note that the VCOMP pin voltage has an offset of 0.5 V. The VCOMP pin linear operating range is nominally 0.5 V minimum, 2.5 V maximum. The VCOMP pin signal is also inverted – lower voltage yields higher output power. However the presence of this offset and inversion does not change the gain for the purpose of loop analysis.

The input of error amplifier $G_{EA}(s)$ is the voltage on the FBP pin. The output is the voltage on the VCOMP pin. The internal error amplifier is an operational transconductance amplifier (OTA) with gain G_M which is nominally 85 µA/V. The gain is G_M times the impedance of the compensation network

$$G_{EA}(s) = G_M \times \frac{(1 + sR3C5)}{s \times (C5 + C4 + sR3C4C5)}$$

R3 and C5 are the main compensation components. Capacitor C5 provides a pole at the origin (integration), in order to drive the output error to zero. Resistor R3 in conjunction with C5 form a zero. This zero frequency is placed at or slightly below the desired gain crossover frequency in order for the compensator to have less than 45° of phase lag at the gain crossover frequency. Capacitor C4 forms a high frequency pole; this must be kept several decades above the zero frequency (i.e. C4 must be much smaller than C5) so that the phase lag it introduces does not affect the loop operation at the gain crossover frequency.

The simplest way to compensate the PFC is to select some nominal starting values for the compensation components, and to iterate the design of the loop from there:

$$R3 = 2.2\ k\Omega$$
$$C5 = 10\ \mu F$$
$$C4 = 22\ nF$$

These values work well for C_{BULK} = 220 µF, V_{ACMIN} = 90 V, V_{BULK} = 385 V, and P_{OUT} = 300 W, and yield a gain crossover frequency of 9 Hz. (See Figure 17)

For different values of C_{BULK}, V_{ACMIN}, V_{BULK}, and P_{OUT}, adjust the values as described.

The time constant of R3 and C5 (zero frequency) should be maintained:

$$\frac{1}{2 \times \pi \times R3 \times C5} = 7\ Hz$$

This is the frequency of the zero in the transfer function inserted by R3. By keeping the zero frequency slightly below the gain crossover frequency, a phase margin of 45° is maintained. R3 should be kept inversely proportional to $G_{PS} \times H_S$ and is described by the following equation

$$R3 = 16\ k \times \left(\frac{1}{I_{ACMAX}}\right)^2 \times \frac{C_{BULK} \times V_{BULK}}{R_{SENSE}}$$

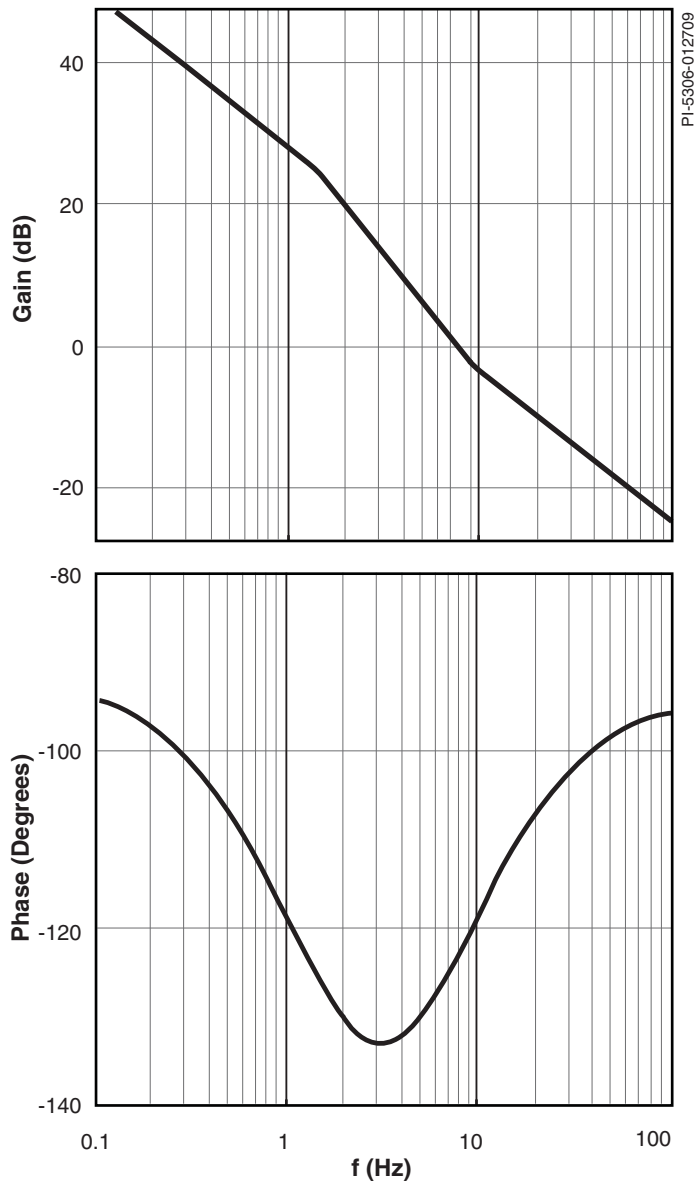


Figure 17. Gain and Phase Plot of the PFS Voltage Feedback Loop (R3 = 2.2 kΩ, C4 = 10 µF, V_{BULK} = 385 V, C_{BULK} = 220 µF).

where

$$I_{ACMAX} = \frac{P_{OUT}}{V_{ACMIN}}$$

Because the value of R_{SENSE} is inversely proportional to I_{ACMAX}, (in order to maintain the current limit just above the peak value of I_{ACMAX}) the equation can be simplified to:

$$R3 = 86\ k \times \frac{C_{BULK} \times V_{BULK}}{I_{ACMAX}}$$

Because C_{BULK} tends to be proportional to power and thus I_{ACMAX}, for 85~90 VAC input and V_{BULK} = 385 V, the correct starting value for R3 tends to remain fixed at 2.2 kΩ.

Selection of PFC Current Sense Resistor

The design spreadsheet should be used to calculate the value of the current sense resistor. Refer to the PLC810PG data sheet for

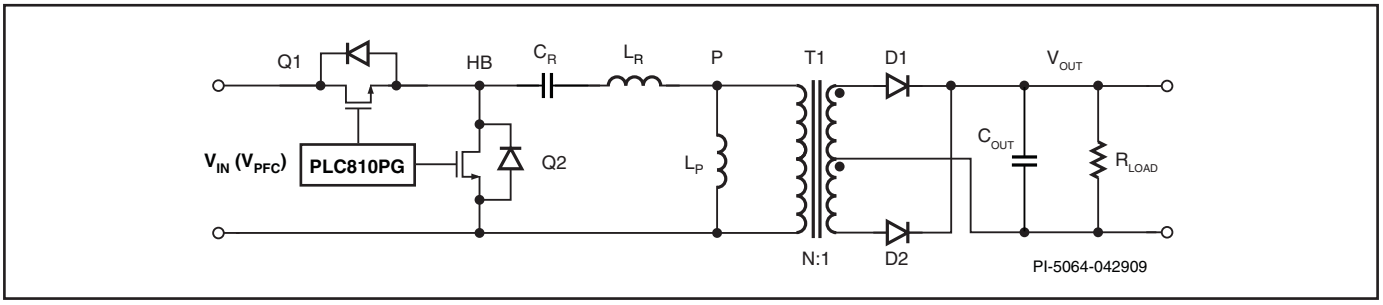


Figure 18. Simplified LLC Schematic Showing Key Power Components.

the PFC current-sense signal filtering recommendations. The voltage across the current-sense resistor determines the cycle-by-cycle current limit. The cycle-by-cycle current limit voltage is described by V_{OC} in the data sheet and is nominally 500 mV. In order to provide headroom for startup, overload, and AC dropout conditions, a good approximation is to use a sense resistor value 10-20% lower than the spreadsheet calculated value. This resistor will be subject to the bulk capacitor inrush current and therefore should have an appropriate I^2t rating. To limit the maximum voltage (and power) during bulk capacitor charging, place two 1N4007 diodes connected in series across this resistor with the cathode connected to the bridge rectifier.

LLC Basic Operation

An LLC converter is a resonant converter which uses frequency to regulate output voltage. LLC's are well suited for high efficiency applications, which require constant output voltage and fixed input voltage, such as with PFC pre-regulators. They can also be used for constant current output converters if the required output voltage range is limited to less than 1.5:1 and if they do not need significant hold-up time (for example LED drivers). LLC topologies are not suitable for applications which require an output voltage adjustable over a wide range (over 2:1), or for those requiring a wide voltage input voltage range. Fundamentally, an LLC controller needs to increase frequency to reduce output voltage or output power. A basic schematic is shown in Figure 18. Q1 and Q2 switch alternately, with a duty cycle of 50%, and at a frequency determined by the feedback loop. The voltage at HB is a square wave with a peak-to-peak value of V_{IN}. Transformer T1 is an ideal transformer. The parallel inductance, L_P, is typically 2 to 4 times the value of L_R the series inductance. If an integrated (with built-in high leakage inductance) transformer is used, L_R is the leakage inductance of the transformer. The measured primary inductance of an integrated transformer, is $L_R + L_P$. This is set by adjusting the gapping distance of the core. If separated magnetics are used, L_R is a separate inductor, and L_P is the primary inductance of a low-leakage-inductance transformer.

The equivalent turns ratio of an integrated transformer to be used in the equivalent circuit in Figure 18 is not equal to the physical turns ratio. Refer to the section "Integrated Transformer Turns Ratio Measurement and Calculation".

A simplification of the LLC resonant circuit elements is shown in Figure 19.

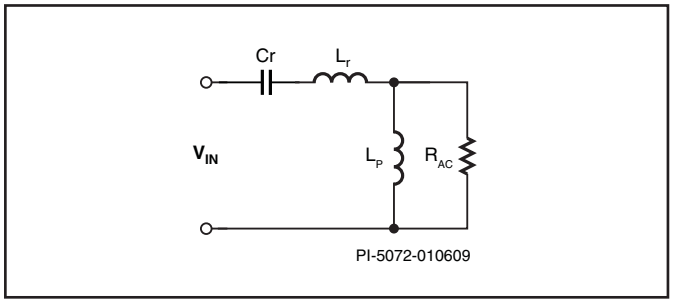


Figure 19. Linear Approximation of LLC Converter.

This linear approximation is used for first-harmonic analysis. The linear approximation is an important tool in understanding and analyzing the operation of the LLC without reference to time domain waveforms. It assumes that only the first harmonic, (fundamental component) of the square wave voltages produce currents (which are sinusoidal), in the circuit. This allows the analysis to be performed using linear frequency response techniques.

The model is comprised of the series or main resonating elements C_R and L_R, the parallel resonant inductance L_P, and R_{AC}. R_{AC} is related to the actual load resistance by the relationship

$$R_{AC} = R_{LOAD} \times \frac{8}{\pi^2} \times N^2$$

Where n is the turns ratio:

$$N = \frac{N_{PRI}}{N_{SEC}}$$

and N_{SEC} is the number of turns of one half of the secondary winding, and N_{PRI} is the number of primary winding turns.

The factor $\frac{8}{\pi^2}$ describes the relationship of power from a sinusoid into a resistor, to the power from a square wave.

The applied V_{IN} in Figure 19 is the fundamental component of the square wave applied to the input.

There are 2 resonant frequencies, parallel, and series. The parallel resonance is formed by the sum of the two inductors and C_R:

$$f_{PAR} = \frac{1}{2 \times \pi \times \sqrt{(L_R + L_P) \times C_R}}$$

The series resonance is

$$f_{SER} = \frac{1}{2\pi \times \sqrt{L_R \times C_R}}$$

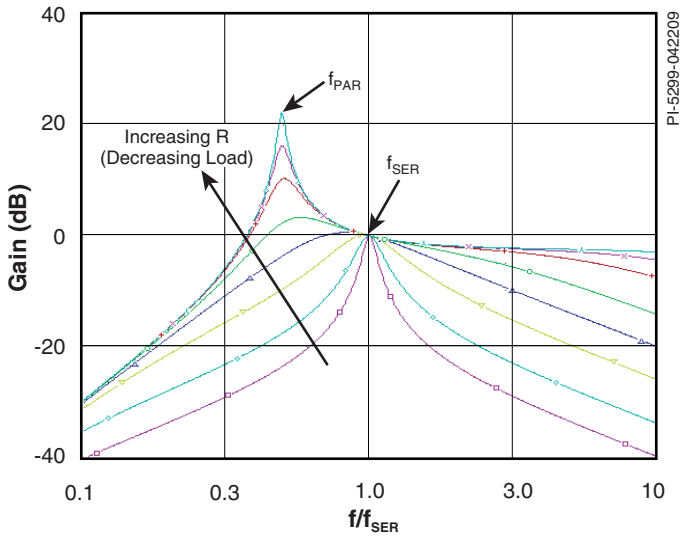


Figure 20. Transfer Function of LLC using Linear Approximation, With Varying R.

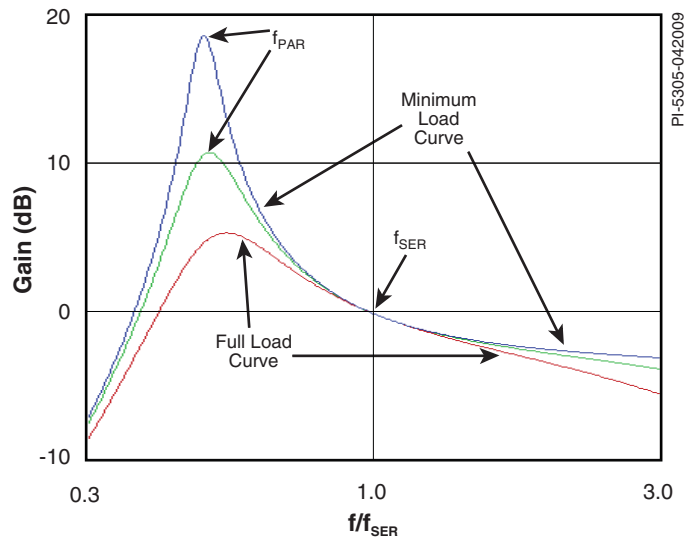


Figure 21. Transfer Function for Q Range of Typical LLC Converter.

The ratio of the 2 inductances is K:

$$K = \frac{L_P}{L_R}$$

Because in a typical LLC converter K is from 2 to 4, the ratio of f_{PAR} to f_{SER} is typically 1.73:1 to 2.24:1.

Q is defined as the Q of the series resonant tank

$$Q = \frac{2 \times \pi \times f_{SER} \times L_R}{R_{AC}}$$

A transfer function using K = 3 is shown in Figure 20.

This represents the steady state gain, V_{OUT} / V_{IN}. Note the 2 resonant peaks. Increasing R yields lower series resonant Q.

In a typical LLC design, the Q at full load is around 0.4 – 0.5. At lighter loads, Q decreases. Figure 21 is a set of curves that is a subset of the curves in Figure 20, showing only the Q range for a typical LLC converter.

The gain represents V_{OUT}/V_{IN}, and because the output voltage is regulated, higher gain represents the ability of the converter to regulate the output voltage at lower input voltage, such as during hold-up time.

An LLC converter must always operate to the right of f_{PAR} where higher frequency yields lower output voltage. If an LLC converter operates inadvertently to the left of the resonant peak, the gain will reverse sign and the feedback system's DC gain will become positive. This will "lock" the converter at the user specified f_{MIN}.

In addition, the area to the left of the resonant peak at any given Q, represents loss of ZVS (zero voltage switching) operation, and the MOSFETs will experience high switching losses. At heavier loads, the border of ZVS and non-ZVS operation occurs slightly to the right of the resonant peak. If the converter is allowed to operate briefly outside of ZVS, such as at the end of holdup time, the loss of efficiency may not be significant.

Note that at the series resonant frequency the gain of the converter does not change with load. This means the converter will have very low output impedance at this frequency. For this reason, at nominal input voltage, (385 V is a typical value for the PFC output), the resonant values should be chosen so that the desired nominal operating frequency is close to f_{SER}.

If full load operation is above f_{SER}, the output diodes will be operating in continuous conduction mode (the diodes are still conducting when the primary switches). This will increase output diode switching noise, output ripple and noise and increase reverse recovery loss (unless Schottky diodes are used), but reduces RMS current losses in the secondary. Note that as the gain close to f_{PAR} varies dramatically with R_{LOAD}, operating in this region should be avoided.

Reading the Spreadsheet Graphs of Frequency vs. Input Voltage

Figure 21 shows the ratio of output voltage to input voltage gain. In a power supply the output voltage is held constant. If we invert the graph, we can show input voltage vs. frequency, as the output voltage is held constant. The result is shown in Figure 22.

In the following example from the design spreadsheet, (Figure 22) nominal PFC output voltage (and LLC input voltage) is 385 V, nominal frequency is 100 kHz, and the ratio of parallel inductance to series inductance, K, is set at 2:1. The design minimum LLC input voltage is 250 V (Spreadsheet parameter $V_{BULKMIN}$). (250 V is the lowest allowable minimum LLC input voltage, which yields maximum hold-up time; it represents $V_{SD(L)}$, which is nominally 64% of the PFC set point. At the end of hold-up time, when the bulk capacitor discharges below this voltage, the PLC810PG will inhibit the LLC gate drive outputs.)

Figure 22 plots the frequency at which the converter needs to operate vs. input (bulk capacitor) voltage, for maximum load and minimum load. The frequency range of the PLC810PG must be limited according to this graph. The frequency range is

set with external resistors connected to the FBL pin and a resistor on the FMAX pin. Please refer to the PLC810PG data sheet for more details.

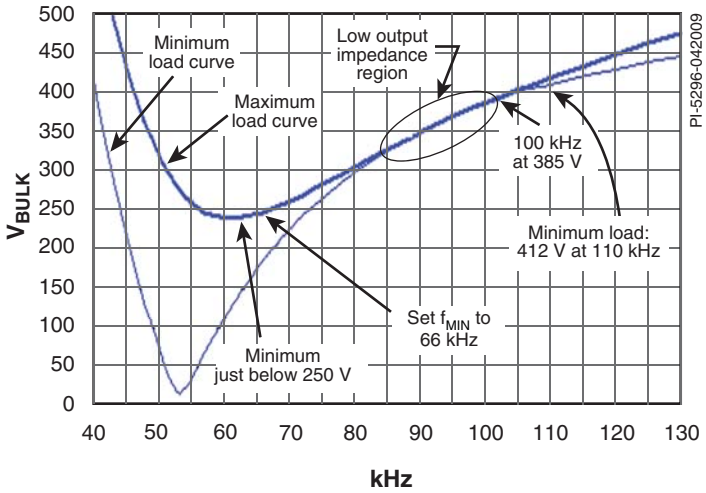


Figure 22. Frequency vs. Input Voltage for LLC, at Full Load and Minimum Load (Effectively Inverse of Figure 21).

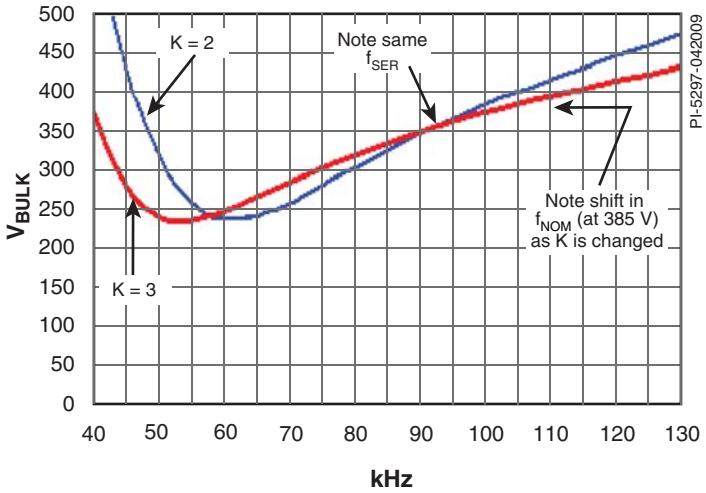


Figure 23. Effect of Changing Inductance Ratio K on Operating Frequency.

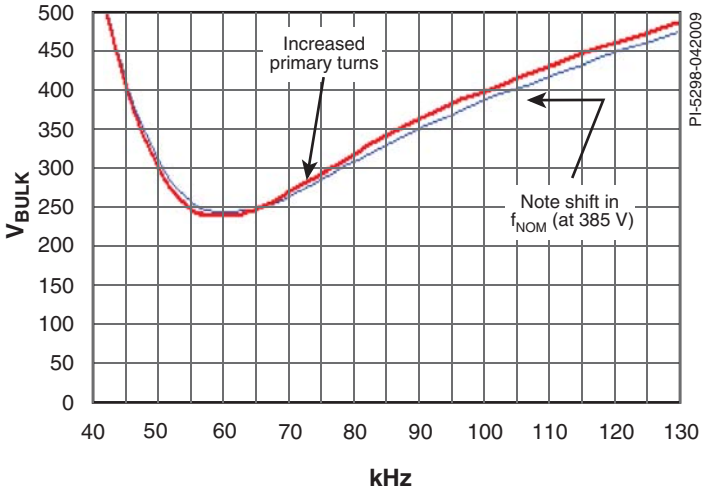


Figure 24. Effect of Primary Turns on Operating Frequency.

Note that in this example, the series resonant frequency is 92 kHz. The low output impedance region shown on the graph (Figure 21) is centred on 90 kHz (which corresponds to 350 V).

This has the advantage that during a large load step (which may Cause the bulk voltage to droop momentarily to 320 V from 385 V), the output impedance remains low and the output of the LLC will not show a significant drop. The downside of this arrangement Is that the output diodes in the LLC operate in continuous conduction mode when operating above the series resonant frequency. While this reduces RMS currents in the secondary thus improving efficiency, it increases output diode reverse recovery losses (unless Schottkys are used), and increases diode switching noise.

The maximum frequency at which an LLC operates occurs at minimum load and maximum input voltage. Maximum voltage output of the PFC stage is 107% (max $V_{OV(H)}$) of the nominal PFC set point, which can occur during a load dump. For a 385 V design, this will be 412 V. In Figure 22, the minimum load curve at 412 V indicates an operating frequency of 110 kHz is required. In practice, First Harmonic Analysis is accurate at heavy load, but becomes progressively less accurate as load decreases. The actual frequency needed is higher than predicted; the amount of variation from the model depends on parasitic elements in the transformer. Minimum load frequency more than 1.5× nominal is often required; if maximum frequency is insufficient to allow regulation at minimum load, an increase in primary turns provides an alternative solution. However increased primary turns will increase the $V_{BULKMIN}$ point and further adjustment of the resonant components will be required. Note that the FMAX pin resistor also affects the dead-time. Another option is to allow hysteretic burst mode at light load – see the PLC810PG data sheet for more details.

If the designer chooses to set the minimum input voltage higher than 64% of the PFC setpoint, the LLC will have higher efficiency, but will provide less hold-up time for a given size bulk capacitor. The PLC810PG will continue to switch until V_{BULK} reduces to 64% of the set point. f_{MIN} must still be set higher than the frequency at the bottom of the full load curve. When a higher $V_{BULKMIN}$ is higher than 65%, as the bulk capacitor voltage drops below the LLC minimum input voltage, the output will also begin to drop, however the PLC810PG will continue driving the LLC MOSFETs until the bulk voltage drops to 65% of the set-point.

Note that the slope of the line in Figure 22 represents the system loop gain contribution of the power train (change in output voltage divided by change in frequency) – this loop gain is not to be confused with “steady state gain” V_{OUT}/V_{IN} in the LLC Basic Analysis section.

In setting the resonant component values and the turns ratio, the designer has four variables: C, L_{SER}, L_{PAR}, and turns ratio N. The designer has 4 goals: desired f_{NOM}, f_{SER}, $V_{BULKMIN}$, and the frequency at $V_{BULKMIN}$ (f_{MIN}).

Because there are 4 variables and 4 goals, there will be a single solution set that will meet all 4 goals. However, there may be constraints in setting some of the variables and there may be extra flexibility in some of the other goals. For example, in an integrated transformer design, a designer may be constrained

with a fixed L_R (leakage inductance) for a given bobbin, and a given number of primary turns. The exact value for f_{SER} and f_{MIN} on the other hand, may be flexible. This may allow an acceptable solution set to be derived whilst still meeting circuit constraints.

If the leakage inductance is higher than what would yield an optimal solution, $V_{BULKMIN}$ will be lower than desired. The result is higher primary current than that achieved with a more optimal solution. However the results may still be acceptable. If L_{SER} still needs to be reduced, the bobbin will need to be changed, or primary and secondary turns both reduced.

Effects of the Resonant Component Values, and Transformer Turns Ratio

When the designer sets the series resonant frequency, the product of C and L_S is effectively fixed. There are two more degrees of freedom – the turns-ratio, and K (the ratio of L_P to L_R). The turns ratio is adjusted to achieve desired f_{NOM}. K is then adjusted to achieve the desired $V_{BULKMIN}$. So, for a given series resonant frequency, there are multiple combinations that achieve a given $V_{BULKMIN}$, with different values of K. The spreadsheet does not directly use K as an input; the user can adjust the 3 values by using the goal-seek function on the spreadsheet. By adjusting one of the resonant values, the spreadsheet can help the designer determine the combinations of the 3 parameters that will yield the required $V_{BULKMIN}$. There is some interdependence in these values so a short iterative process must be followed.

Changing K (Inductance Ratio)

Figure 23 shows what happens when a new solution is found that maintains a series resonant frequency of 92 kHz, and a $V_{BULKMIN}$ of 240 V, for a new value of K (3). In order to get the same $V_{BULKMIN}$ with K = 3, L_R has to be reduced and C increased (to maintain f_{SER}). Note that the nominal switching frequency, f_{NOM} is shifted higher, and f_{MIN} shifted lower. Higher K gives a larger change of frequency required to maintain regulation over a given change of input voltage. However, higher K produces higher parallel inductance, which reduces the magnetizing current, slightly improving efficiency. In this example, if the same f_{NOM} is desired, the resonant values can be re-adjusted to lower f_{NOM}, or primary turns can be increased slightly (see next section).

The slope of the curve from $V_{BULKMIN}$ to V_{NOM} is a factor in the overall system feedback loop-gain (the change in output voltage for a change in frequency). An increase in K reduces loop-gain. Loop-gain should not to be confused with the "steady state gain" described in the LLC Basic Analysis section.

Changing Primary Turns

It is often not possible to change the secondary turns in order to change the turns-ratio because of the low number of turns in the secondary. (e.g., going from 2 turns to 1 turn will double the flux density with a correspondingly huge increase in core losses). To change the turns-ratio usually only the primary turns can be adjusted. Changing the primary turns while keeping the series inductance constant (only possible with non-integrated magnetics) will change the gain around f_{SER}. Once the turns-ratio is correct, there is only limited room to change primary turns. If the designer decides to run f_{NOM} further or closer to f_{SER}, primary turns should be adjusted to get the desired f_{NOM}. Figure 24 shows the shift in f_{NOM} at full load due to a change in primary turns. If regulation at minimum load is a problem and hysteretic burst mode is undesirable, increasing primary turns should be considered.

Note that with integrated magnetics, the series (leakage) inductance is proportional to the square of the primary turns. The resonating capacitance will have to be adjusted to maintain the same series resonant frequency. K must also adjusted to maintain the same V_{IN} operating range.

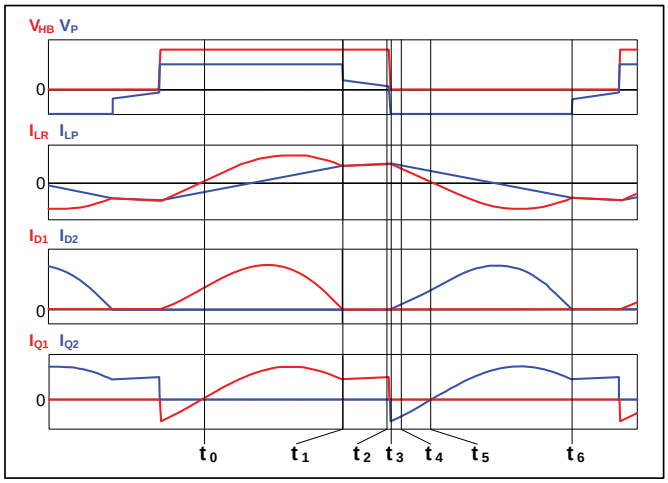


Figure 25. LLC Converter Timing Diagrams for Node Shown in Figure 18.

LLC Converter Time Domain Operation

As shown in Figure 18, the basic LLC converter circuit consists of two switches Q1 and Q2. The center point of the half-bridge (HB) is connected to the resonant tank (C_R, L_R and L_P) and the power transformer T1. The power switches are driven by 50% duty-cycle pulses. The output voltage of the converter is regulated by varying the switching frequency.

On the secondary side of the LLC, diodes D1 and D2 rectify the AC output of the transformer, while the output capacitor C_{OUT} filters the rectified voltage.

Depending on the state of the power switches Q1 and Q2, the operation of the LLC converter can be divided into six time intervals per cycle. Figure 25 shows the relationship of currents and voltages in the LLC converter during each interval, while Table 2 describes the circuit condition during each interval. Figure 25 shows operation below f_{SER}. Above f_{SER}, interval t, $\rightarrow t_2$ dissapears.

Zero Voltage Switching and Dead Time

The parasitic capacitance of the half bridge mid-point, operating in the zero-voltage switching (ZVS) region must be considered in order to insure zero-voltage-switching of the half-bridge MOSFETs. This capacitance must be charged and discharged during transitions. To enable ZVS, a dead-time is inserted between the ON states of the MOSFETs. During this dead-time neither MOSFETs is conducting. To ensure ZVS, the voltage at the mid-

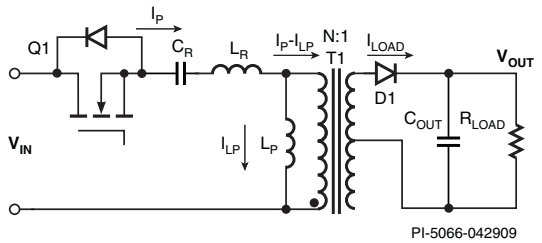
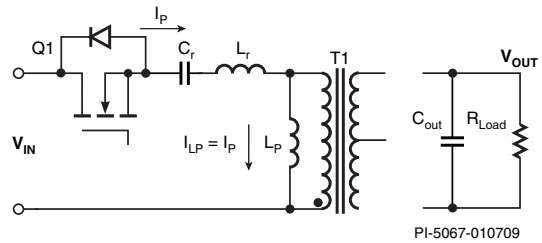
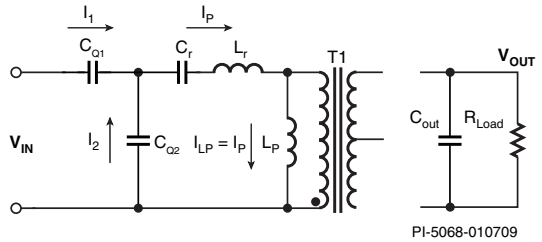
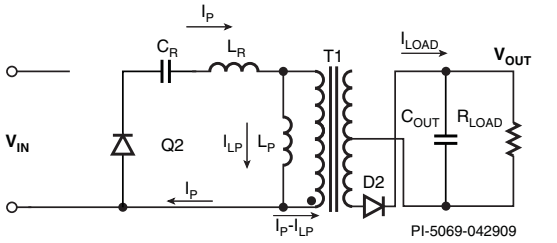
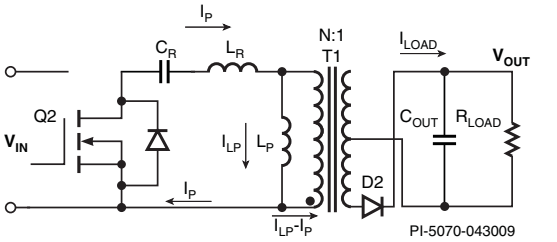
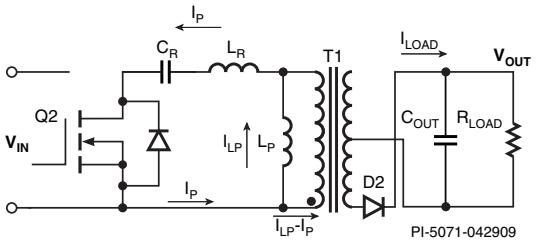
Interval	LLC Converter Equivalent Circuit	Description
$t_0 \rightarrow t_1$		During this period, switch Q1 is ON while switch Q2 of OFF. The primary current I_P resonates with the series resonant frequency: $$f_R = \frac{1}{2\pi\sqrt{L_R \times C_R}}$$ The primary current I_P is greater than the current that flows through the parallel resonant inductor (L_P). The difference current ($I_P - I_{LP}$) is the load current that flows through diode D1 when multiplied by turns ratio N. This interval ends at t_1 when the load current be comes null ($I_P = I_{LP}$).
$t_1 \rightarrow t_2$		During this period, switch Q1 in ON while switch Q2 is OFF. At instant t_1: $I_P = I_{LP}$, the secondary current is null. The voltage on the power transformer (T1) collapses (becomes lower than the output voltage). Neither of the output diodes on the secondary side (D1 and D2) is conducting. The load is supplied from the output capacitor C_{OUT}. The primary current I_P which is equal to the parallel current I_{LP} resonates with the parallel resonant frequency: $$f_{RP} = \frac{1}{2\pi\sqrt{(L_R + L_P) \times C_R}}$$ Instant t_2 corresponds to when Q1 turns off (no current through the channel).
$t_2 \rightarrow t_3$		This interval starts when Q1 turns off (no current through the channel). The primary current $I_P = I_{LP}$ is supported by the resonant inductor L_R. This current discharges the parasitic capacitance of switches Q1 and Q2 and drives the bridge voltage to 0 V. Instant t_3 corresponds to the bridge voltage reaching 0 V, the current starts to flow through the diode of switch Q2.
$t_3 \rightarrow t_4$		During this interval both switches Q1 and Q2 are OFF. At instant t_3, the bridge voltage reaches 0 V and the current starts to flow through diode of switch Q2. The voltage on the parallel inductor L_P is reversed and the secondary diode D2 starts to conduct. The primary current I_P resonates with the series resonant frequency: $$f_R = \frac{1}{2\pi\sqrt{L_R \times C_R}}$$ The primary current I_P is smaller than the I_{LP} current which flows through the parallel resonant inductor L_P. During this interval the voltage across switch Q2 is 0 V and can be turned on with zero voltage switching (ZVS), thus eliminating switching losses. Q2 is turned ON at instant t_4.
$t_4 \rightarrow t_5$		At instant t_4 Q2 is turned ON with zero voltage switching. The primary current I_P still flows in the opposite direction through switch Q2. The primary current I_P resonates with the series resonant frequency: $$f_R = \frac{1}{2\pi\sqrt{L_R \times C_R}}$$ During this interval, the primary current I_P is smaller than the current I_{LP} which flows through the parallel resonant inductor (L_P). The current difference $I_{LOAD} = I_{LP} - I_P$ is the load current which flows through the rectifier diode D2 when multiplied by the turns ratio N. At instant t_5 the primary current I_P changes polarity.
$t_5 \rightarrow t_6$		This interval is similar to interval [t_0, t_1]. In this case it is switch Q2 that is ON and switch Q1 that is OFF. The current flows in the opposite direction to interval [t_0, t_1]. The rectifier diode D2 is conducting and the load current is: $I_{LOAD} = I_{LP} - I_P$. At instant t_6, the primary current I_P becomes the same as the parallel inductor current I_{LP}. At this instant the load current (I_{LOAD}) is null. The output load starts to be supplied by the output capacitor. The set of the six intervals is then repeated.

Table 2. LLC Converter Operation and Basic Intervals.

point of the half bridge must drop from V_{IN} to 0 (or rise from 0 to V_{IN}) within the dead time (t_D). One of the key features of the PLC810PG is that the value of dead-time can be set externally by the FMAX resistor. This allows a further degree of flexibility in the design of the LLC converter. Being able to tightly control the dead-time ensures that ZVS is maintained in mass production.

The PLC810PG data sheet describes dead-time setup as a function of the FMAX pin pull-up resistor.

Power Losses and LLC Converter Efficiency

Efficiency under normal operating conditions is the key to the converter performance. The nominal operating condition corresponds to the resonant frequency f_R.

One of the major advantages of the LLC converter is the ZVS feature which virtually eliminates switching losses. The two main power losses in the LLC converter are therefore conduction losses in the switching MOSFETs Q1 and Q2, and the secondary-side diode conduction losses. These losses are proportional to the primary side RMS current and to the secondary side RMS current respectively.

A description of the RMS values of all the currents in the converter are given in the primary and secondary sections of the design spreadsheet. Other component losses that are due to the Equivalent Series Resistors (ESRs) can be easily calculated from these RMS current values.

Design of LLC Resonant Tank

The first step in designing the LLC is to choose the values for L_{SER}, L_{PAR}, C_{RES}, and turns ratio (n), by examining the transfer curves as the four values are manipulated. This process is described below.

Set the nominal switching frequency, which is at the PFC set point (typical 385 V), at full load, at the target switching frequency (66, 100, or 132 kHz).

Set V_{BULK}, the nominal PFC output voltage. 385 V is typical selected for a wide range input PSU.

Set $V_{BULKMIN}$, the minimum input voltage about 5 V below the actual target bulk minimum voltage to account for tolerances. A design that maximizes hold-up time will have a target bulk minimum voltage of 65% of the set point (250 V for a 385 V design). In this case set $V_{BULKMIN}$ to 245 V. A design that sacrifices hold-up time for improved LLC efficiency will have a higher $V_{BULKMIN}$. Note that the PLC810PG will shut down the LLC converter when the bulk capacitor voltage drops below 65% of set point, thus a lower $V_{BULKMIN}$ cannot be used.

Set the LLC series resonant frequency at 10% below the target operating frequency from step (1), this minimizes the converter output impedance at nominal input voltage minimizing output voltage variation with sudden load steps which could cause voltage dips on the bulk capacitor. Setting the series resonant frequency just below the target frequency will move the region of low output impedance into the range at/below the PFC output set point. It also results in slightly lower secondary RMS currents. However, diode currents will be in continuous conduction, resulting in higher switching noise, increased diode reverse recovery loss (if not using Schottky diodes), and more output noise and ripple.

If the series resonant frequency is set at or slightly above the target operating frequency, the diodes will be in discontinuous conduction and there will be less diode switching noise, no reverse recovery losses, and lower output ripple and noise but efficiency will be slightly reduced.

The spreadsheet will provide initial values of C, L_{PAR}, and L_{SER}. These values can then be optimized by an iterative process. The spreadsheet will calculate $V_{BULKMIN}$, frequency at $V_{BULKMIN}$, and frequency at V_{BULK} (nominal PFC output setpoint). Goal-Seek can be used to change any one of these variables in order to meet a target value for one of the output variables. Note that for integrated magnetics, the primary open-circuit inductance (L_{OPEN}), is equal to the sum of the series and parallel inductances.

Examine the operating frequency at minimum load and $V_{BULKMAX}$, which is at 107% of V_{BULK}. The curves generated by the spreadsheet are less accurate at light load, so the actual frequency at light load will be higher than the spreadsheet predicts.

For no load operation, the designer has 2 choices – allow hysteretic burst mode operation, or increase primary turns and reiterate the spreadsheet calculation. Minimum load regulation needs to be verified in a prototype unit.

LLC Feedback Circuit Design

The feedback loop system samples the output voltage, amplifies the error, and adjusts the FBL pin current accordingly, see Figure 26. In the case of a LM431 reference IC, the outputs are adjusted so that the LM431 feedback pin is at 2.5 V.

Note that if there are any LC post filters (small L and small C) in the output, R62 and R63 MUST be connected before the post filters. Connecting R62 and R63 after the post-filter creates an additional phase shift in the feedback loop which can cause oscillation. The output voltage sensing (R64 and R66) can remain connected to the outputs (after the post filters), in order for the feedback loop's DC gain to compensate for any voltage drop. Connecting R64 and R66 after any post filters will not cause oscillation because this is a low frequency feedback path, below the frequency of attenuation of the post filters. In this example, the value and therefore currents in these resistors can be weighted to achieve the desired relative regulation accuracy of the two outputs. The sum of the currents equals the current in R68. The LM431 amplifies the error voltage on the outputs and its output voltage appears on the bottom of the optocoupler's cathode. The optocoupler's photodiode is a current sensitive device. It has a low dynamic impedance compared to R62 and R63+C45, thus its voltage drop can be considered constant. The current in the photodiode is equal to the voltage on the 24 V rail minus the voltage on the optocoupler's anode, divided by impedance of the network formed by R62, R63, and C45. Resistor R65 merely sets the minimum current in the LM431

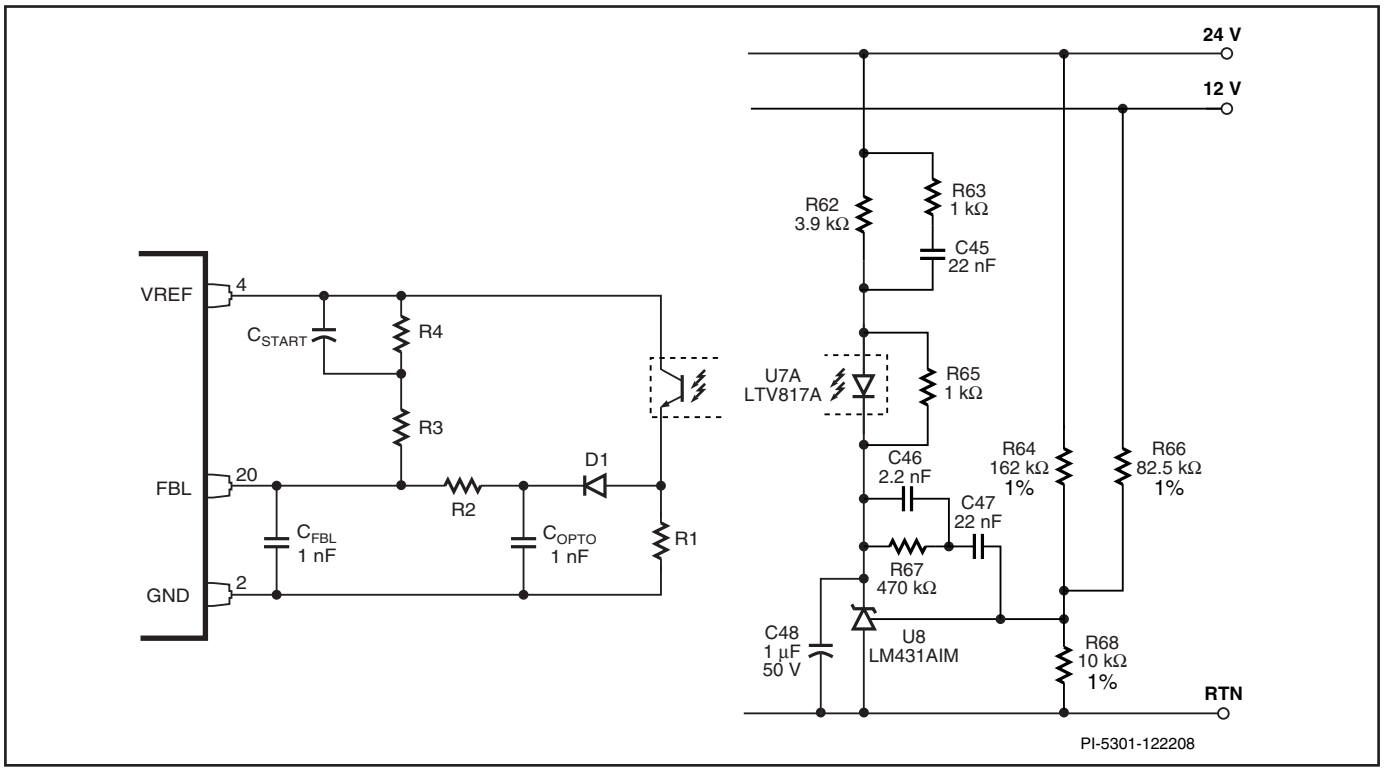


Figure 26. LLC Secondary Side Feedback Circuit.

when the feedback loop is closed; because the optocoupler voltage stays relatively constant at 1 V, the LM431 current, when the optocoupler is cut off, is

$$I = \frac{1V}{R65}$$

For a typical LM431 which needs a 1 mA cathode bias current, R65 is 1 kΩ.

The transfer function from LLC output voltage to LM431 cathode (V_{LM431}) is:

$$V_{LM431} = \frac{Z_{FEEDBACK}}{R68}$$

Where $Z_{FEEDBACK}$ is the impedance of C46, C47, and R67:

$$Z_{FEEDBACK} = \frac{1}{s \times C47} + \frac{R67\frac{1}{s \times C46}}{R67 + \frac{1}{s \times C46}}$$

The current in the optocoupler photodiode is

$$I_{OPTODIODE} = (V_{24Vo} - V_{LM431}) \times \left[\frac{R62 + \left(R63 + \frac{1}{s \times C45}\right)}{R62\left(R63 + \frac{1}{s \times C45}\right)}\right]$$

Some rules of thumb can be used.

The transfer function of V_{OUT} -> $I_{OPTODIODE}$ has a pole at the origin (integration). This main low frequency integrator gain is set by:

$$\frac{1}{R62 \times R68 \times C47}$$

R63 and C45 insert a pole-zero pair to perform a phase boost function, peaking its phase at the crossover frequency, which for an LLC, can be in the range of 1 kHz to 3 kHz. This is to improves the phase margin. As such, R63 needs to be 1/10th to 1/4th of R62, and the time constant of C45 and the geometric mean of R62 and R63 (root of their product):

$$\frac{1}{2 \times \pi\sqrt{R62 \times R63} \times C45}$$

needs to be close to the desired gain crossover frequency.

Resistor R67 and C46 form another pole-zero pair to reduce the gain at very low frequency and provide a phase boost to prevent low frequency (10-100 Hz) instability (wherein phase approaches or crosses 180° phase shift). This low frequency instability can manifest itself as low frequency “motorboating” that appears as a large low frequency output ripple, when the load is abruptly reduced. Without the phase-boost network, the low frequency (integrator gain) would need to be reduced and the 100/120 Hz bulk cap ripple rejection would be reduced. In Figure 26, the peak of the phase boost occurs at 51 Hz:

$$\frac{1}{2 \times \pi \times R67\sqrt{C46 \times C47}} = 51\ Hz$$

The presence of this low frequency phase boost network allows more gain above 51 Hz (set by C46) and yet keeps the phase margin high at low frequencies. Without the phase boost network, the LM431 feedback network would be a capacitor (with no RC), equal to 22 nF, and 100/120 Hz ripple rejection would be poor.

On the primary side, the current $I_{OPTODIODE}$ is multiplied by the optocoupler's CTR (in the Figure 26 example, CTR = 100% higher gain optocouplers are unnecessary). The optocoupler transistor current is multiplied by the resistor network ratio R1/R2. The gain from optodiode current to FBL pin current is:

$$CTR \times \frac{R1}{R2}$$

Note that the purpose of R1 is to act as a load on the optocoupler. For most optocouplers, 0.5 to 3 mA at full load is recommended. R2, R3, R4, and C_{START} set the minimum, maximum, and startup frequencies. Please see the PLC810PG data sheet for details. C_{OPTO} is a noise filter which tend to couple into the long traces to the optocoupler. This capacitor inserts a pole at:

$$\frac{1}{2 \times \pi \times R1 \times C_{OPTO}}$$

Likewise, C_{FBL}, the bypass capacitor for the FBL pin, forms a pole with the parallel combination of R2, R3, and the FBL pin nominal input resistance of 3.3 kΩ:

$$\frac{1}{2 \times \pi \times par(R2, R3, R_{FBL}) \times C_{FBL}}$$

For this reason, do not use capacitors greater than 1 nF for C_{OPTO} and C_{FBL}. Doing so will add excessive phase shift in the loop gain and make the LLC prone to oscillation.

The FBL pin current to frequency transfer function is given by the inverse of the slope of the curve in the data sheet (FBL Pin Current vs. Switching Frequency), which is 2 kHz / μA.

The LLC powertrain has a DC gain near the regulation point which is given by the slope of its curve, V_{OUT} / frequency, effectively the slope of the curve of Figure 21 near nominal input voltage. If referring to the curves in Figure 22, the slope needs to be recalculated in terms of V_{OUT} instead of V_{BULK}. The frequency characteristics of the LLC frequency to output voltage transfer function can be found in numerous technical papers.

LLC Transformer Design

An integrated LLC transformer is basically a half-bridge transformer with additional leakage inductance (which acts as the series resonant inductance) added. In addition the core is also gapped to set the magnetizing inductance. In order to increase leakage inductance, the primary and secondary windings are wound with a space between them (see Figure 27).

Because of the high leakage inductance, Litz wire is required in order to minimize the copper losses from the skin and proximity effects of the strong leakage flux.

An LLC converter can also be built with the series resonant inductance in a separate magnetic structure. In this case, the main transformer will look like a standard half-bridge transformer with low leakage and with a gapped core to achieve the required magnetizing inductance. Typically the series inductor would use Litz wire to minimize losses due to the large flux swing.

Note, the PIXls Spreadsheet has an LLC transformer calculator.

The transformer design needs to balance several requirements:

- The (ferrite) core should never be allowed to saturate, even at minimum frequency. The flux swing of the core is

$$\Delta B = \frac{V \times t}{N_{SEC} \times A_E}$$

Where V is the output voltage plus the diode drop
N_{SEC} is the number of turns of a half secondary
A_E is the core center leg area
t is a half period of the switching frequency.

- Ferrite typically begins saturating at 0.34 T at high temperature.
- Enough winding area so that magnet wire (Litz wire in the case of an integrated transformer) is thick enough to yield acceptable RMS current losses. Allocate enough secondary winding area such that copper losses in the secondary are acceptable.
- For the integrated transformer, the desired value of leakage inductance is obtained. Leakage inductance is proportional to the square of the primary turns.

If using an integrated transformer, the leakage inductance can be increased by increasing the spacing between the primary and secondary windings. However, the amount it can be increased by this method is limited to approximately 15%. Increasing the winding separation will reduce space available for copper, necessitating thinner gauge wire and increasing losses. Because leakage inductance is proportional to the square of the primary turns, increasing primary and secondary turns (to maintain the required turns ratio), has a much stronger effect on leakage inductance.

In some cases, especially with a multi output transformer, due to the low number of turns per volt, the designer has limited options with respect to secondary turns.

The turns-ratio is typically fixed by use of the transfer-curves in the spreadsheet.

Core Losses

For a given core material, core losses are a function of B_{AC} (peak-to-peak AC flux density), and frequency. Because core losses are a stronger function of B_{AC} than frequency, and because for a fixed number of turns, B_{AC} is inversely proportional to frequency, simply increasing the frequency and maintaining the number of turns reduces core losses. Another consequence is that if frequency is increased, and turns are reduced by the same percentage, core losses will go up. Therefore if a higher switching frequency is desired in order to reduce the number of turns, the turns will be reduced by a smaller percentage. Note also that proximity effect and skin loss effects become worse as frequency increases.

The symmetry of the half-windings in the secondary plays a major role in the secondary current sharing between the output halves. Tight coupling between the halves of the secondary winding will also help limit diode peak-voltage stress and ringing. If there are 2 or more outputs, tight coupling between the different outputs will improve cross-regulation. In general, LLC's have much better cross-regulation than forward type converters which require output chokes.

Figure 27. Photo of Integrated LLC Transformer with Separated Primary and Secondary Windings.

For a 100 kHz design, a typical target B_{AC} is less than 0.20 Tesla pk-pk for manageable core losses.

The design can be optimized by thermal testing. If the core is much hotter than the windings, the B_{AC} should be reduced – consider a core with a larger cross sectional area. If the winding is too hot, use finer Litz wire (in the case of an integrated transformer), or use more Litz wires in parallel. Check the termination resistance by comparing the measured pin-to-pin resistance to the calculated resistance in the spreadsheet.

Other LLC Components

Resonating Capacitor

This capacitor needs to be a high quality film capacitor. The current rating of the LLC resonating capacitor needs to be greater than the maximum RMS current at f_{MIN}. The spreadsheet will typically show the value of primary I_{RMS} at f_{MIN}. The maximum voltage can be calculated as

$$V_{PEAK} = V_{BULKMAX} + \frac{I_{OCP_LLC}}{2\pi \times f_{SER} \times C}$$

Where

$$I_{OCP_LLC} = \frac{0.5\,V}{R_{LLC_SENSE}}$$

R_{LLC_SENSE} is the LLC current sense resistor.

LLC MOSFETs

For a 385 V or 400 V PFC design, 500 V MOSFETs can be used. In the spreadsheet, the graphs for primary current are given. The MOSFETs will each see 29% lower RMS current. For a proper thermal design, the power dissipation in each MOSFET will be:

$$P = I_{RMS}^2 \times R_{DS(ON)}$$

Larger MOSFETs will improve efficiency, but the higher C_{OSS} will result in slower slew rates and will require a longer deadtime.

Output Rectifiers

The reverse voltage stress on the rectifiers will be:

$$V_{RRM} = 2 \times V_{OUT} + V_{SPIKE}$$

The voltage spike, V_{SPIKE}, can range from 5 – 20% of V_{OUT}. This should be verified by actual measurement. The coupling of the secondary halves within the transformer will determine the size of the spike. The tighter the coupling, the smaller the spike. Consider whether if a modest reduction in the spike voltage will enable lower voltage rectifiers, or Schottky diodes, which will improve efficiency.

Testing

PFC-Only Testing

When powering up the PLC810PG power supply, sometimes it is desirable to power only the PFC. If the LLC is not loaded, the LLC will run at high frequency (and force the PFC to follow accordingly), with correspondingly low efficiency. The solution is to position a potentiometer between VREF and FBL pins and use it to force operation at nominal frequency.

The LLC outputs may be disabled by connecting a 5 kΩ resistor from VREF to ISL. For troubleshooting purposes, it is useful to examine the voltages on the ISP, FBP, VCOMP, and VCC pins. The ISP pin will show an inverted analog of the choke current; it instigates current limit at approximately 500 mV. The FBP pin voltage is a scaled down version of the bulk voltage. When regulating, it will be close to 2.2 V. The VCOMP pin represents the RMS input AC current. At maximum input current, this should be close to 0.5 V; at minimum load, 2.5 V. The 120 Hz ripple should be small. The VCC pins should be above the startup threshold, and below the absolute maximum.

At full load, check the PFC MOSFET current at minimum AC voltage, it should not be entering current limit. Check the AC current wave shape, it should have clean wave shape and good crest factor. If the current wave shape is distorted, the first step should be to reduce the PFC gain, specifically by reducing the resistor value on the VCOMP pin. Lower the AC voltage below the minimum rated input. The voltage at which the PFC begins to current limit should be below the minimum input voltage.

LLC-Only Testing

To run the LLC, simply remove the AC source from the PFC input and connect a high voltage DC supply to the bulk capacitor. The LLC will run normally. Examine the pin voltages, ISL, and FBL. ISL should be an analog of the primary current and FBL should be approximately 1 V during normal operation. If the output is not regulating, check the operating frequency and examine the FBL pin and feedback circuits.

LLC Startup and Load Transients

ISP Signal Integrity

The ISP signal is a small, high bandwidth signal. Its integrity is

very important. Distortion can result in PFC misbehavior (e.g. current limit errors). Examine the signal using a probe with short prongs, connected to the GND pin and the ISP pin. Place an RC lowpass filter right across the PFC sense resistor, using the same values as the ISP pin RC filter. Examine the voltage across this capacitor, using a probe with short prongs, and compare it with the signal on the ISP pin. If there is significant distortion, check that:

A. There is only one connection from the GND pin to the primary return
B. The GND pin connected to the sense resistor via a dedicated PCB trace, and this trace connects directly to the sense resistor as closely as possible
C. There is no direct connection from the GNDL pin to the primary return; this connection must be through a ferrite bead and the connection is made directly to the LLC lower MOSFET Source
D. The ISP pin RC lowpass filter components are close to the ISP pin, connected with short traces
E. That the trace from this resistor to the PFC sense resistor runs alongside the trace from the GND pin to the sense resistor

Examine the LLC primary current as the output ramps up. The current dependant voltage should be well below the current limit thresholds. This is nominally +500 mV peak on the ISL pin for 8 consecutive cycles, or +1.4 V for 75 ns. If it is close, increase the soft start capacitor value. Examine the LLC primary current during a load-step. If the peak currents are too close to the ISL thresholds, consider reducing the LLC sense resistor value.

Checking LLC Secondary Symmetry

By examining the output voltage ripple on the first output capacitor (closest to the rectifiers), the level of current sharing in the secondary can be deduced, as at the switching frequency the capacitor impedance is mostly ESR.

Auto Restart and LLC Inhibit / Hysteretic Burst Mode

Auto restart will occur in the LLC when the ISL threshold is exceeded. The off-time of the auto-restart cycle is equal to 4096 clock cycles of F_{MAX}.

When the FBL current exceeds the current programmed in the FMAX pin by the FMAX resistor, the LLC outputs will be inhibited. This results in hysteretic burst mode, which can be adopted for light load or no-load operation.

Other Design Considerations

VCC

The V_{CC} range for the PLC810PG is 10-15 V. Depending on the standby supply used, the V_{CC} may need to be regulated. If the same standby supply is used as an output for the PSU, ensure that the V_{CC} supply does not dip below 9 V during a load dump on that output. A simple way to prevent this is to use a 470 µF or other suitable capacitor value on the standby output, before the regulator, to provide “ride through” capability for the V_{CC}.

The simplest regulation scheme uses a Zener and a BJT, as shown in Figure 28. The BJT needs to be a darlington configuration such as the BST22TA so that the required base current will be small. The bias supply needs to provide a minimum of 13 V in order for the regulator to provide at least 10.5 V. The regulator does not need to provide a perfectly constant output voltage, but it needs to limit the range of the voltage on V_{CC}. Note that the nodes “B-“ and “GND” refer to the PLC810PG GND pin and bulk capacitor negative terminal respectively. These nodes are connected together electrically. However, the primary bias return (bottom of C1), in Figure 28, is returned to the bulk capacitor, and GND is returned to the PLC810PG GND pin.

Figure 29 shows a simple remote ON/OFF circuit. Optocoupler PC817A will be powered when the supply is required to operate.

Optional Transistor to Improve PFC 0-100% Load Step Response

In some cases a 0-100% load step can cause the bulk capacitor voltage to drop to 65% (parameter $V_{SD(L)}$) of the output voltage set-point, shutting down the LLC. A transistor placed on the VCOMP pin (see Figure 30) will speed up the large signal response of the PFC to a large load step. It works by sensing when the VCOMP pin is sinking 400 µA, then rapidly discharging C5, immediately increasing the AC input current, arresting the bulk voltage drop. This circuit will only work with R3 ≥ 1.8 kΩ. The VCOMP pin output sink current increases to 400 µA when V_{FB} <2.1 V, signifying a 5% drop in the bulk voltage from the set-point.

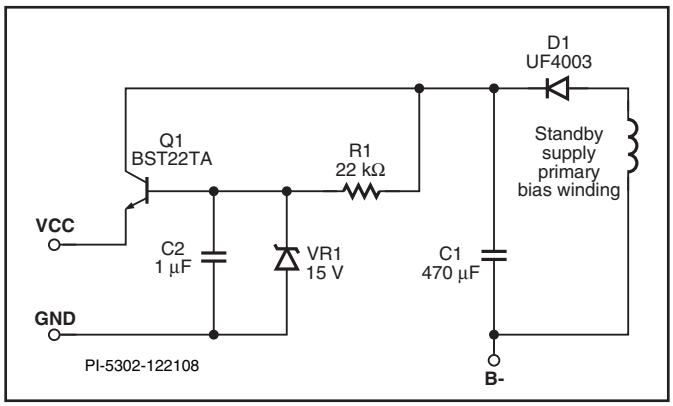


Figure 28. Simple Zener Regulation for VCC.

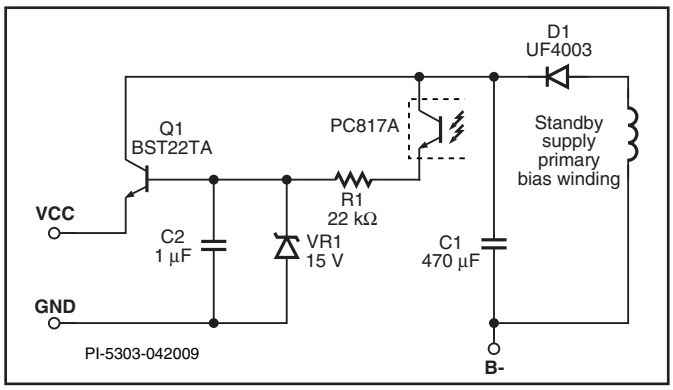


Figure 29. Remote ON/OFF on VCC Regulator.

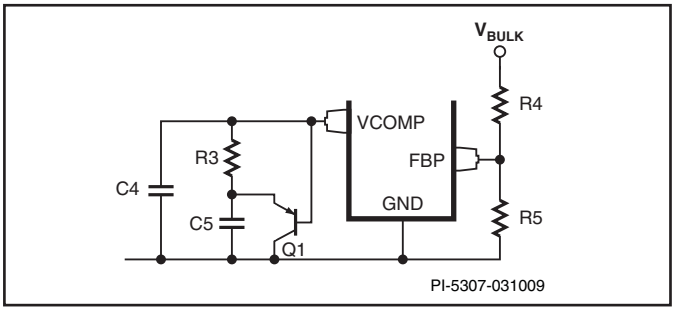


Figure 30. Optional BJT to Improve PFC Voltage Dip During Large Load Step.

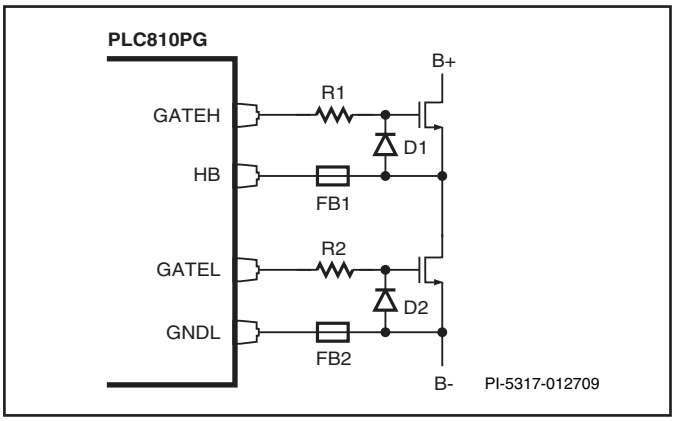


Figure 31. Reducing Negative Voltage Spike on GATEL and GATEH Pins (D1 and D2 are 1N4148).

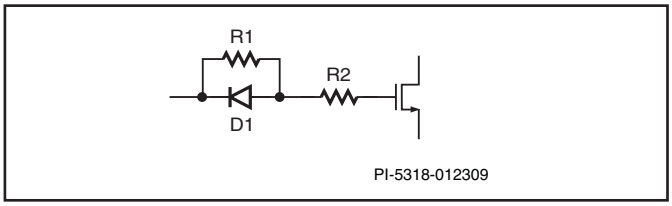


Figure 32. Additional Option for Reducing Negative Voltage Spike on GATEL and GATEH Pins.

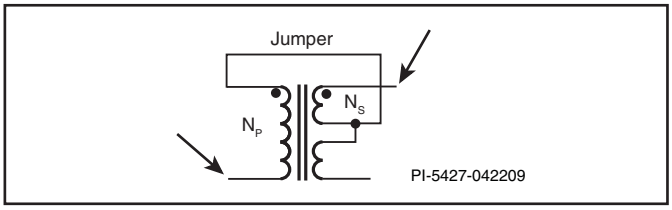


Figure 33. Measure Inductance L_{AID} at Arrows.

Limiting Negative Voltage on GATEL and GATEH Pins

The GATEL and GATEH pins have a maximum allowed negative voltage of -300 mV.

During voltage transitions in the half-bridge, a large dv/dt appears across both LLC MOSFETs (Drain to Source). During the negative going transition the induced low-side LLC MOSFET Drain-Source dv/dt is also negative. This negative dv/dt couples through the Drain-Gate capacitance and pulls current from the GATEL pin (while it is asserted low), pulling it negative with respect to the GNDL pin and producing a negative voltage spike. Similarly during the positive half-bridge transition, current flows out the GATEH pin which goes negative with respect to the HB pin. This current flows through the internal pull-down MOSFET for the gate output, which has a nominal $R_{DS(ON)}$ of approximately 4 Ω. If this current is large, it is possible that the gate voltage will fall below the specification limit of -300 mV

Figures 31 and 32 show two possible solutions to this problem. In Figure 31, the two diodes clamp the amplitude of the negative Gate-Source voltage. The remaining voltage will be reduced by the resistor divider formed by the gate resistor (R1 and R2) and the $R_{DS(ON)}$ of the internal pull-down MOSFETs for GATEL/GATEH.

In Figure 32, an alternative gate drive network is used in place of a simple series resistor. The negative voltage on V_{GS} will be reduced by the resistor divider formed by of R1, R2, and the $R_{DS(ON)}$ of the pull-down MOSFET. This drive scheme will slow down the turn-on, but this will have a negligible effect on performance.

Integrated Transformer Turns Ratio Measurement and Calculation

The equivalent turns ratio of an integrated transformer has to be calculated using the following procedure.

Measure the primary open circuit inductance, L_{OPEN}.

Short one phase of the secondary, then measure the inductance of the primary. This is L_{SER}. Calculate L_P:

$$L_P = L_{OPEN} - L_{SER}$$

Connect one phase of the secondary in series with the primary, to produce an autotransformer, in “series aiding” fashion (dotted end connected to undotted end) – see Figure 33. Measure the total inductance, L_{AID}, which should be greater than L_{OPEN}. If it is not, it has not been connected in “series aiding” fashion and has been connected dotted end to dotted end. Reverse the phase of the primary to correct this and re-measure.

The equivalent turns ratio of the transformer for the equivalent circuit in Figure 18 is given by:

$$N_{EQUIV} = \frac{1}{\left(\sqrt{\frac{L_{AID} - L_{SER}}{L_P}}\right) - 1}$$

Revision	Notes	Date
A	Initial Release	05/09
B	Updated text and equations on page 10, 14, 17 and 21.	07/09

For the latest updates, visit our website: www.powerint.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

Life Support Policy

POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

The PI logo, TOPSwitch, TinySwitch, LinkSwitch, DPA-Switch, PeakSwitch, EcoSmart, Clampless, E-Shield, Filterfuse, StakFET, PI Expert and PI FACTS are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies.
©2009, Power Integrations, Inc.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

China (Shanghai)
Room 1601/1610, Tower 1
Kerry Everbright City
No. 218 Tianmu Road West
Shanghai, P.R.C. 200070
Phone: +86-021-6354-6323
Fax: +86-021-6354-6325
e-mail: chinasales@powerint.com

China (Shenzhen)
Rm A, B & C 4th Floor, Block C,
Electronics Science and
Technology Bldg., 2070
Shennan Zhong Rd,
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

Germany
Rüeckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3910
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

Italy
Via De Amicis 2
20091 Bresso MI
Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

Japan
Kosei Dai-3 Bldg.
2-12-11, Shin-Yokomana,
Kohoku-ku
Yokohama-shi Kanagwan
222-0033 Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

Singapore
51 Newton Road
#15-08/10 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 114, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

Europe HQ
1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44-1252-730-141
Fax: +44-1252-727-689
e-mail: eurosales@powerint.com

Applications Hotline
World Wide +1-408-414-9660

Applications Fax
World Wide +1-408-414-9760