Application Note AN-1169

IRPLLED5
40V/1.4A Low Voltage LED Driver using IRS2548D

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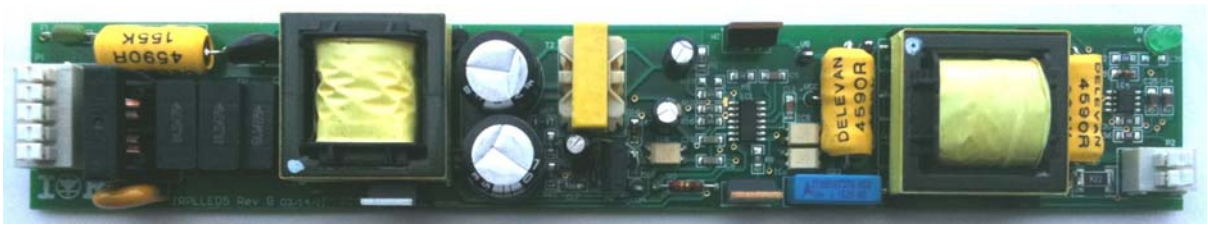
EVALUATION BOARD - IRPLLED5



1. Introduction

Solid state light sources are now available that offer viable alternatives to Fluorescent and HID lamps and far surpass incandescent lamps. Luminous efficacy expressed in Lumens per Watt has now reached levels enabling LEDs to be used for general illumination. High brightness LEDs also possess the added advantages of longer operating life span up to 50000 hours and greater robustness than other less efficient light sources making them suitable for outside applications such as street lighting.

High power LEDs are ideally driven with constant regulated DC current, requiring a "driver" or "converter" to provide the required current from an AC or DC power source. A two stage power converter based around the IRS2548D PFC plus half bridge LED driver IC provides a controlled current output over a wide AC line voltage input range with high power factor and low THD.

The IRPLLED5 evaluation board is an off line isolated low voltage / high output current LED driver designed to supply a 1.4A regulated DC output current over a voltage range of 30V to 60V operating from an AC line input voltage between 90 and 305VAC 50/60Hz. It also includes 1-10V dimming capability from 0 to 100% of light output. The outputs of this LED driver are fully protected against short circuit and limit the open circuit voltage to below 60VDC for safety compliance.

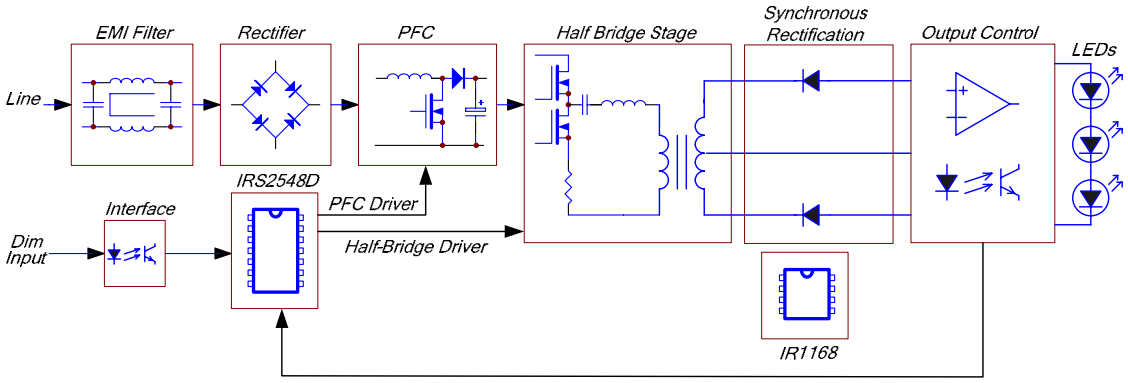


Figure 1: IRPLLED5 Block Diagram

2. PFC Section

The IRPLLED5 board uses a power factor correction Boost converter stage front end which operates in critical conduction mode. During each switching cycle of the PFC MOSFET the IRS2548D detects the point at which the inductor current discharges to zero when all stored energy has been transferred to the output before turning the PFC MOSFET on to start the next switching cycle.

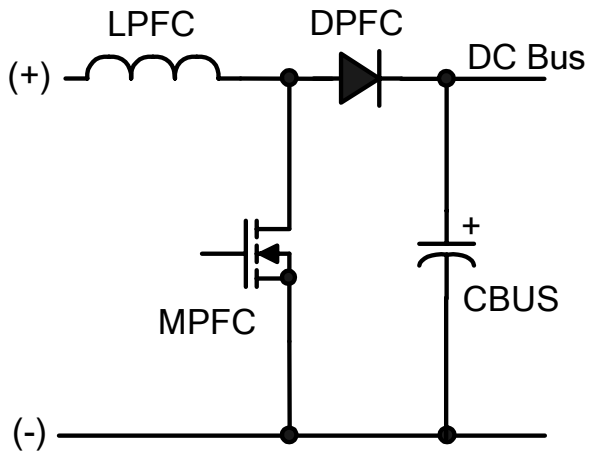


Figure 2: PFC Boost converter circuit.

When the switch MPFC is turned on, the inductor LPFC is connected between the rectified line input (+) and (-) return causing the current in LPFC to rise linearly. When MPFC is turned off LPFC is connected between the rectified line input (+) and the DC bus capacitor CBUS through diode DPFC and the stored energy in LPFC is transferred to CBUS. MPFC is turned on and off at a high frequency and the voltage on CBUS charges up to a specified voltage. The PFC feedback loop of the IRS2548D regulates this voltage to a fixed value by continuously monitoring the DC bus voltage and adjusting the on-time of MPFC accordingly. This negative feedback control is performed with a slow loop speed such that the average inductor current smoothly follows the low frequency line input voltage for high power factor and low THD. The on-time of MPFC therefore appears to be fixed (with an additional modulation to be discussed later) over several cycles of the line voltage. With a fixed on-time and an off-time determined by the inductor current discharging to zero the switching frequency constantly changes from a high frequency near the zero crossing of the AC input line voltage to a lower frequency at the peaks (Figure 3).

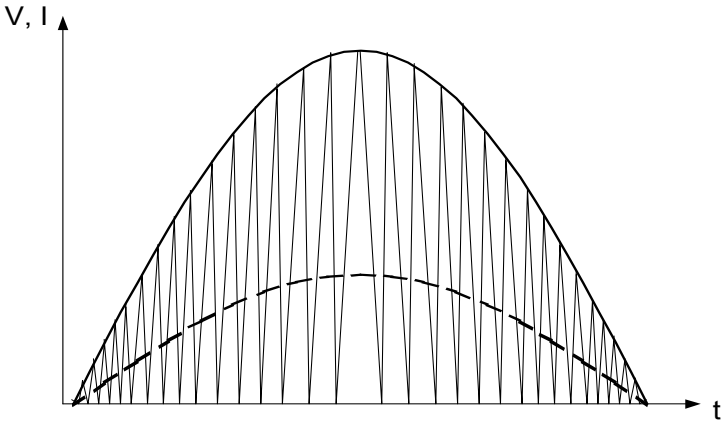


Figure 3: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line input voltage.

When the line input voltage is low near the zero crossing the inductor current rises to a relatively low level and the discharge time is therefore fast resulting in a high switching frequency. When the input line voltage is high near the peak the inductor current rises to a higher level and the discharge time is therefore longer giving a lower switching frequency. The PFC control circuit of the IRS2548D (Figure 4) includes five control pins: VBUS, COMP, ZX, PFC and OC. The VBUS pin measures the DC bus voltage via an external resistor voltage divider. The COMP pin at the error amplifier output sets the on-time of MPFC and the speed of the feedback loop with an external capacitor. The ZX (zero crossing) pin detects when the inductor current discharges to zero during the off time using a secondary winding from the PFC inductor. The PFC pin is the gate driver output for the external MOSFET, MPFC and the OC pin senses the current flowing through MPFC providing cycle-by-cycle over-current protection.

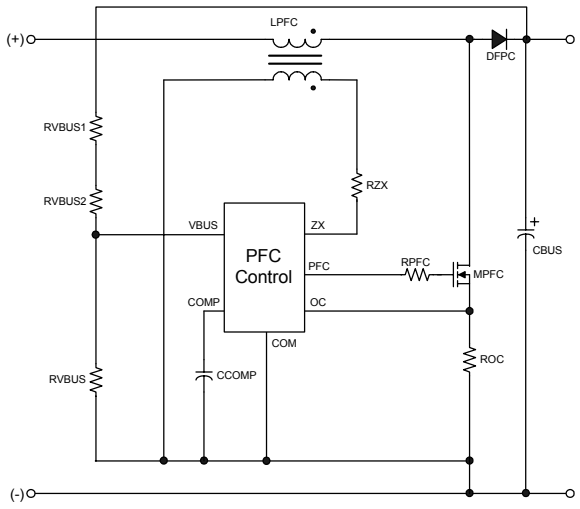


Figure 4: IRS2548D simplified PFC control circuit.

The VBUS pin is regulated against a fixed internal 4V reference voltage for regulation of the output DC bus voltage (Figure 5). The feedback loop error amplifier comprises an operational trans-conductance amplifier (OTA) that sinks or sources a current to the external capacitor at the COMP pin. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor (C1, Figure 5) and therefore programs the on-time of MPFC.

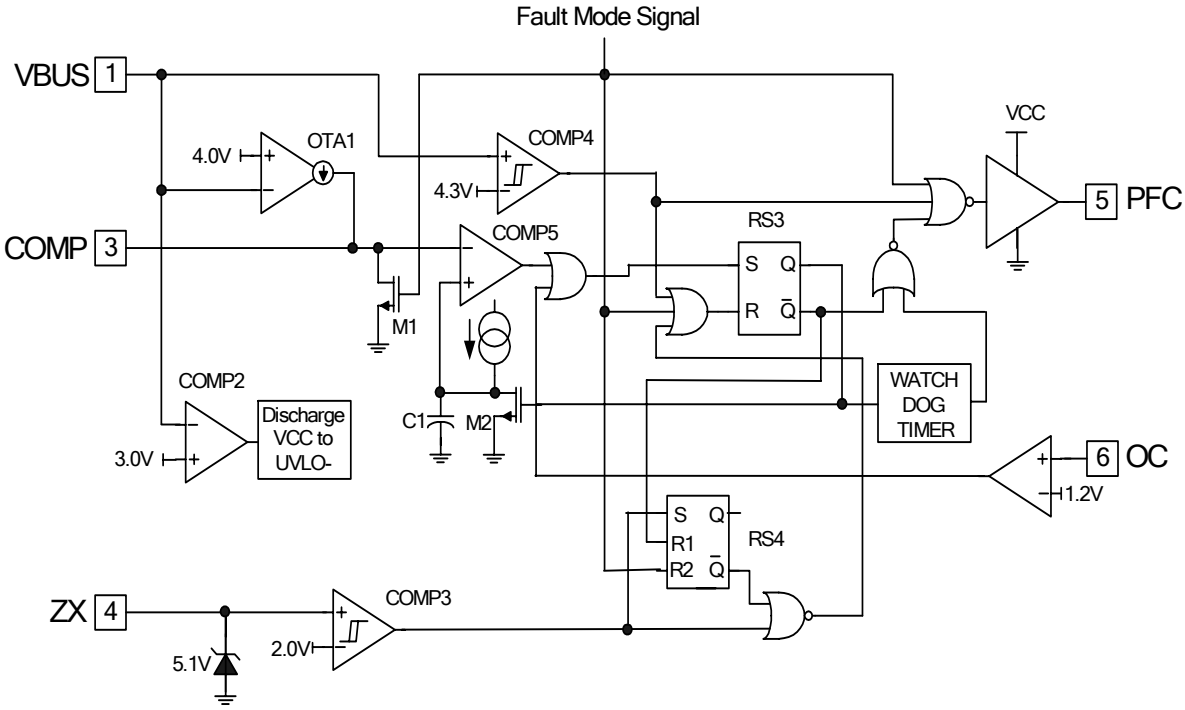


Figure 5: IRS2548D detailed PFC control circuit.

The zero current level is detected by a secondary winding on LPFC connected to the ZX pin through an external current limiting resistor RZX. A positive-going edge exceeding the internal 2V threshold (VZXTH+) signals the beginning of the off-time. A negative-going edge on the ZX pin falling below 1.7V (VZXTH+ - VZXHYS) will occur when the LPFC current discharges to zero which signals the end of the off-time and MPFC is turned on again (Figure 6). The cycle repeats itself indefinitely until the PFC section is disabled due to a fault detected by the system section (Fault Mode), an over-voltage or condition on the DC bus or the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin fail to be detected for any reason MPFC will remain off until the internal watch-dog timer forces a turn-on of MPFC. The watch-dog pulses occur every 400us (tW) indefinitely until a correct positive and negative-going signal is detected on the ZX pin and normal PFC operation is resumed. Should the OC pin exceed the 1.2V (VOCTH+) over-current threshold during the on-time, the PFC output will turn off. The circuit will then wait for a negative-going transition on the

ZX pin or a forced turn-on from the watch-dog timer to turn the PFC output on again.

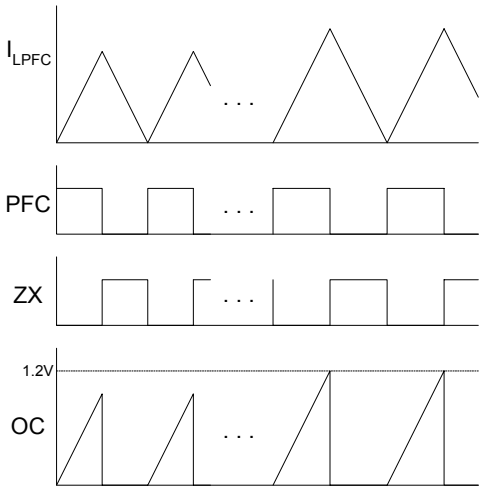


Figure 6: Inductor current, PFC pin, ZX pin and OC pin timing diagram.

A fixed on-time of MPFC over an entire cycle of the line input voltage produces a peak inductor current that naturally follows the sinusoidal shape of the line input voltage. The smoothed averaged line input current is in phase with the line input voltage to provide a high power factor. Some harmonic distortion of the line current still remains mostly due to cross-over distortion near the zero-crossings. To achieve low THD additional on-time modulation circuit is built into the IRS2548D PFC control. This function dynamically increases the on-time of MPFC as the line input voltage nears the zero-crossings (Figure 7). This causes the peak LPFC current, and therefore the smoothed line input current, to increase slightly higher near the zero-crossings of the line input voltage.

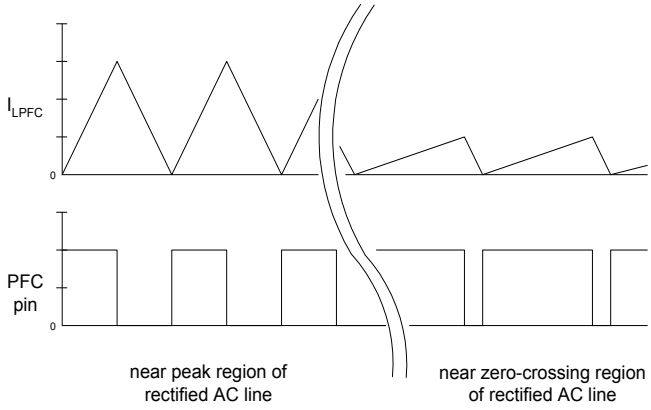


Figure 7: On-time modulation circuit timing diagram

Should over-voltage occur on the DC bus and the VBUS pin exceed the internal 4.3V threshold (VBUSOV+) the PFC output will transition to switch off MPFC. When the DC bus decreases again and the VBUS pin voltage decreases below the internal 4.15V threshold (VBUSOV-) PFC operation is resumed.

The PFC inductor value can be calculated from the following formula:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad \text{[Henries]}$$

where,

$VBUS$	=	DC bus voltage
VAC_{MIN}	=	Minimum rms AC input voltage
η	=	PFC efficiency (typically 0.95)
f_{MIN}	=	Minimum PFC switching frequency at minimum AC input voltage
P_{OUT}	=	System output power

The peak current in the PFC inductor is given by:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta} \quad \text{[Amps Peak]}$$

The PFC inductor should be designed such that it does not saturate at i_{PK} at maximum operating temperature. This involves adequate sizing of the core and air-gap.

The value of the PFC current sense resistor (ROC) is calculated from the following formula and rounded up to the nearest preferred value.

$$R_{OC} = \frac{1.25}{i_{PK}} \quad \text{where VCSTH+ = 1.25V} \quad \text{[Ohms]}$$

3. LLC Resonant Half Bridge Section

The run frequency is programmed with the timing resistor RFMIN at the FMIN pin.
The graph in Figure 6 (RFMIN vs. Frequency) can be used to select RFMIN value for desired run frequency.

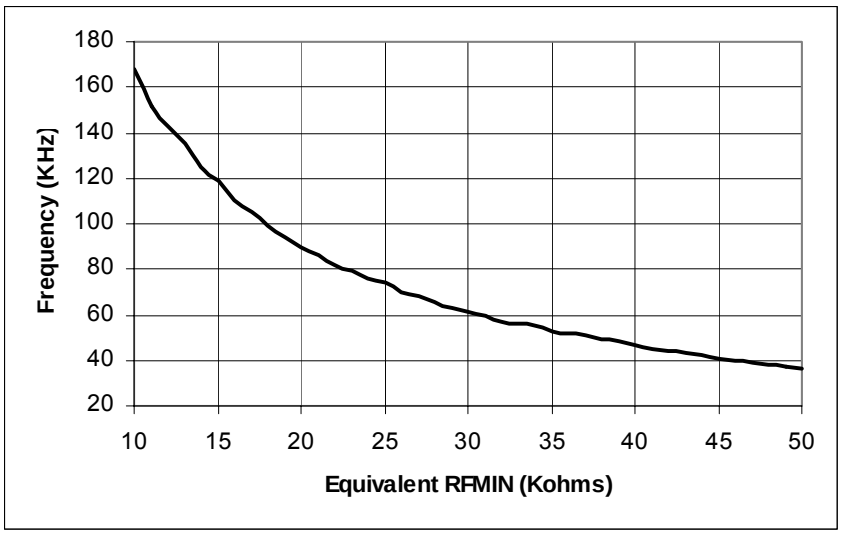


Figure 8: Graph of frequency against RFMIN

The maximum current is programmed with the external resistor RCS and an internal threshold of 1.25V (VCSTH+). This threshold determines the over-current limit of the system:

$$I_{MAX} = \frac{1.25}{R_{CS}}$$ [Amps Peak]

or

$$R_{CS} = \frac{1.25}{I_{MAX}}$$ [Ohms]

The half-bridge LLC resonant converter offers high efficiency due to zero voltage switching operation which also eliminates switching noise. Since the switching losses are negligible no heat sinking is required for the half-bridge MOSFETs. This topology can achieve high power density due to the efficient utilization of the transformer operating in two quadrants of the B-H curve. The resonant topology requires an additional series inductance to be added to the circuit in order to construct a complex resonant tank with Buck-Boost transfer characteristics in the

soft switching region. Although it is possible to incorporate this additional inductance into the transformer, for simplicity the IRPLLED5 design uses a standard transformer design with the additional inductance added externally. The typical power stage schematic for this topology is shown in figure 9.

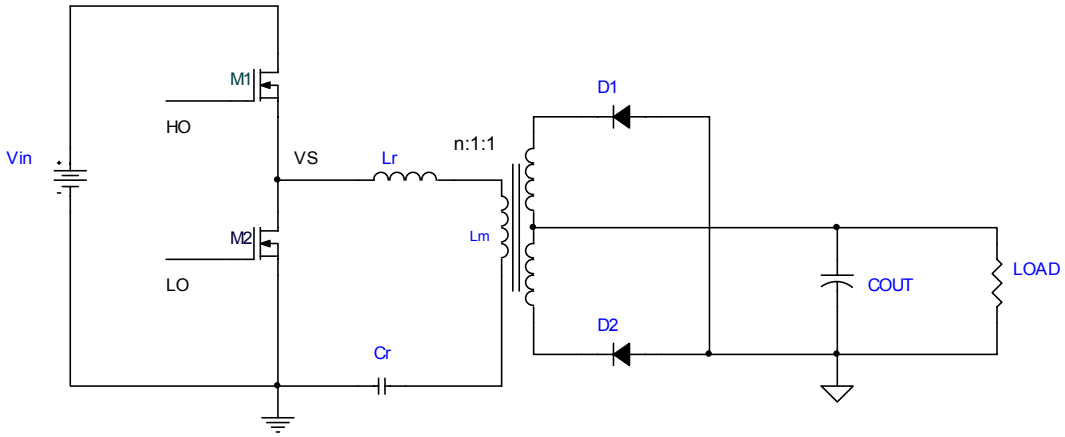


Figure 9: Typical schematic of a DC-DC half-bridge resonant converter

The half-bridge switches operate at 50% duty cycle where the output voltage is regulated by varying the switching frequency. Since the IRPLLED5 drives an LED load which can be represented by a voltage source with a series resistor, the current can also be regulated effectively by adjusting the frequency. The frequency will adjust to provide the required drive current for any number of LEDs connected to the output up to a maximum of 60V. The half-bridge resonant stage has two resonant frequencies the first determined by the series inductor (Lr) and resonant capacitor (Cr) and the second determined by the transformer magnetizing inductance (Lm) and the resonant capacitor. While the frequency remians in the inductive region the soft switching will occur.

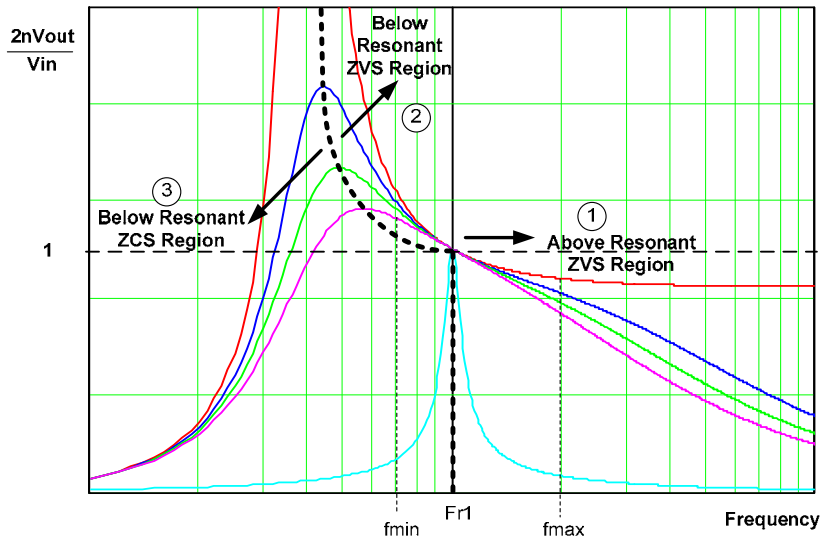


Figure 10: Typical frequency response of an LLC resonant converter

The characteristics of a LLC resonant converter can be divided into three regions based on the three different modes of operation. The first region is for switching frequency above the resonant frequency F_{r1}:

$$F_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}$$

In region 1 of figure 10 (the purple shaded area) the switching frequency is higher than resonant frequency F_{r1}. The converter operation is very similar to a series resonant converter. Here L_m never resonates with resonant capacitor (C_r) it is clamped by the output voltage and acts as the load of the series resonant tank. This is the inductive load region and the converter is always under ZVS operation regardless of the load condition.

In region 2 (the pink shaded area) the switching frequency is higher than the lower resonant frequency but lower than F_{r1}. The lower resonant frequency varies with load so the boundary of region 2 and region 3 traces the peak of the family load vs gain curves. In this complex region the LLC resonant operation can be divided into two time intervals; in the first time interval L_r resonates with C_r and L_m and is clamped by output voltage. When the current in the resonant inductor L_r resonates back to the same level as the magnetizing current L_r and C_r stop resonating. L_m now participates in the resonant operation and the second time interval begins. During this time interval the dominant resonant components become C_r and L_m in series with L_r. The ZVS operation in region 2 is guaranteed by operating the converter to the right side of the load gain curve. For a switching frequency below resonant F_{r1} it could fall in either region 2 or region 3 depending on the load condition.

In the ZCS range below f_{r1}, the LLC resonant converter operates in capacitive mode; M1 and M2 are hard switching with high switching losses. For this reason ZCS operation should always be avoided.

The waveforms in figures 11,12 and 13 show the behavior of the system in each of the operating regions. The typical voltage conversion ratio of a LLC resonant converter is shown in Figure 12.

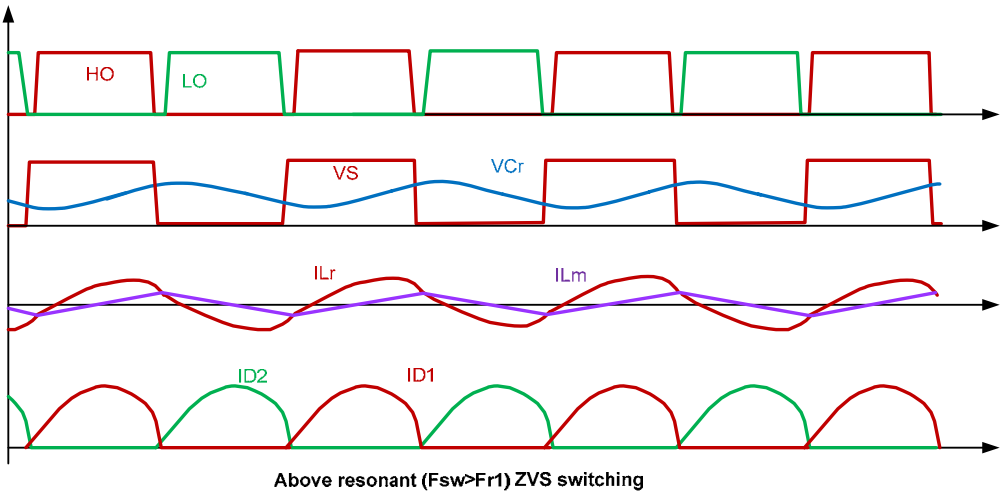


Figure 11: Typical waveform of above resonant ZVS switching

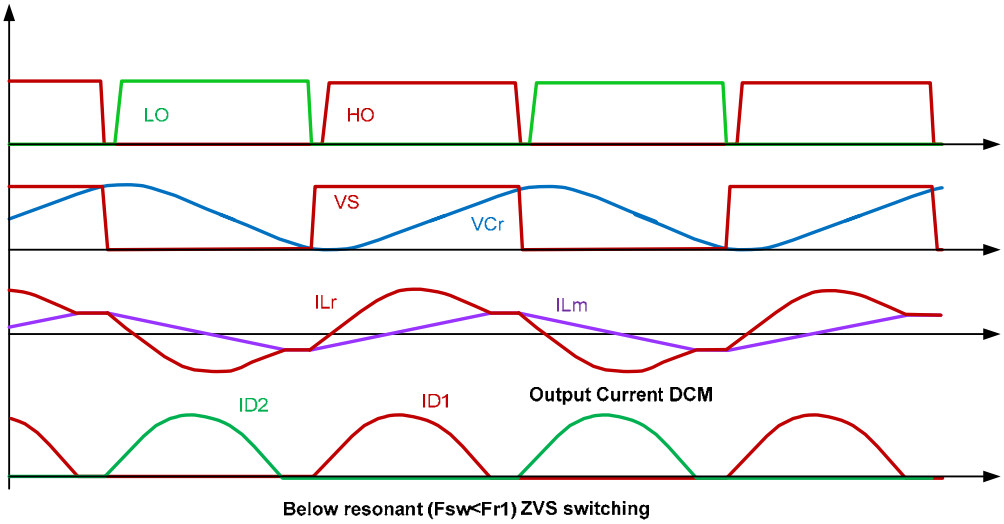


Figure 12: Typical waveform of below resonant ZVS switching

The waveforms in figure 12 indicate that the current in secondary rectifier diodes moves from continuous current mode (CCM) to discontinuous current mode (DCM) when the switching frequency varies from above resonant ZVS to below resonant ZVS due to load increasing. The ripple voltage on the resonant capacitor C_r also increases in the below resonant ZVS mode.

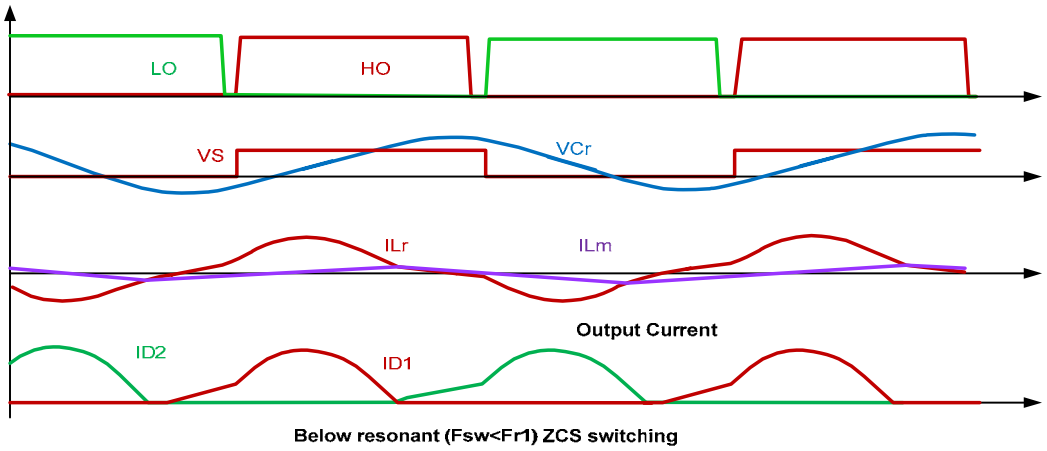


Figure 13: Typical waveform of below resonant ZCS switching

In ZCS mode, the two switching devices M1 and M2 are turned off under zero current condition. The turn-on of the two switches is hard switching (none ZVS). The turn-on switching loss is high especially under high voltage bus voltage. The resonant capacitor C_r also has high voltage stress. ZCS operation should always be avoided.

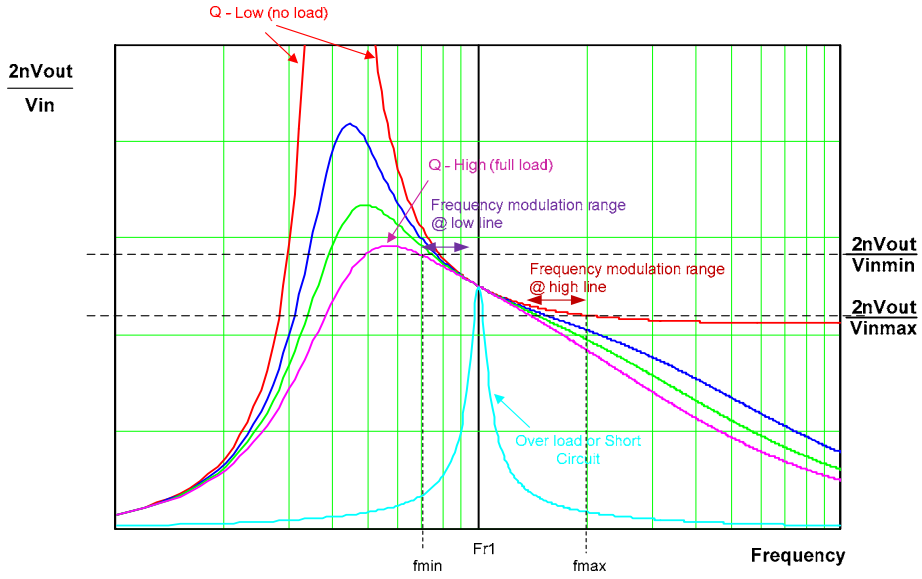


Figure 14: Typical voltage conversion ratio of a LLC resonant converter

With a regulated DC bus voltage supplied from the PFC stage the converter varies switching frequency to regulate the output voltage and current over load range keeping the same conversion ratio over the family of curves with different Q. Given a fixed load condition the converter adjusts the switching frequency along that load line to regulate the output over input voltage range.

The procedure used to design the LLC resonant half-bridge converter uses the First Harmonic Approximation (FHA) to obtain an equivalent circuit. All the components are moved to the primary side to simplify analysis. R_{ac} represents the equivalent load resistance in parallel with transformer primary inductance L_m.

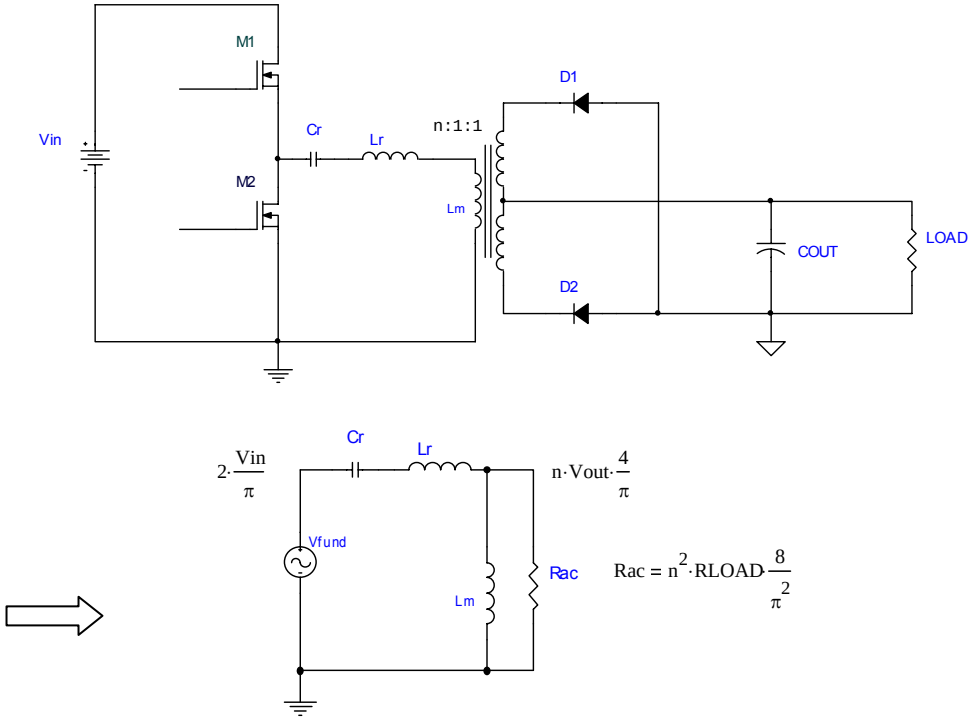


Figure 15: The FHA equivalent circuit

The input voltage of the resonant tank is a square wave with amplitude equal to the DC bus voltage Vbus. The fundamental component of the square waveform is:

$$\frac{2 \cdot Vbus}{\pi} \sin(\omega \cdot t)$$

The output voltage of the resonant tank is the voltage across L_m. It is very close to a square waveform with amplitude swinging from $-n \cdot Vout$ to $+n \cdot Vout$. So the fundamental component of the output square waveform is:

$$\frac{4 \cdot n \cdot Vout}{\pi} \sin(\omega \cdot t)$$

The power dissipation on the equivalent AC resistor is equal to the power dissipation of the load represented by a resistor R_{LOAD} which can be derived by dividing the maximum output voltage by the output current, written as:

$$\frac{Vout^2}{R_{LOAD}} = \frac{\left(\frac{4 \cdot n \cdot Vout}{\sqrt{2}\pi}\right)^2}{Rac}$$

Rearranging the formula gives the equivalent AC resistor:

$$Rac = \frac{8 \cdot n^2}{\pi^2} R_{LOAD}$$

The transfer ratio of the equivalent circuit can be obtained as following:

$$M = \left| \frac{\frac{j \cdot \omega \cdot Lm \cdot Rac}{j \cdot \omega \cdot Lm + Rac}}{j \cdot \omega \cdot Lr + \frac{1}{j \cdot \omega \cdot Cr} + \frac{j \cdot \omega \cdot Lm \cdot Rac}{j \cdot \omega \cdot Lm + Rac}} \right|$$

Simplifying to:

$$M = \left| \frac{1}{1 + \frac{Lr}{Lm} - \frac{1}{\omega^2 \cdot Lm \cdot Cr} + \frac{j\omega \cdot Lr}{Rac} - \frac{j}{\omega \cdot Cr \cdot Rac}} \right|$$

With the following definitions, calculation of M can be further simplified:

$$F_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}, \qquad x = \frac{Fsw}{F_{r1}}, \qquad \varpi = 2\pi Fsw = 2\pi \cdot x \cdot F_{r1} = \frac{x}{\sqrt{L_r \cdot C_r}},$$

$$k = \frac{L_m}{L_r}, \qquad Rac = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2}, \qquad Q = \frac{2\pi F_{r1} \cdot L_r}{Rac} = \frac{1}{2\pi F_{r1} \cdot C_r \cdot Rac}$$

$$M = \left| \frac{1}{1 + \frac{1}{k} \cdot \left(1 - \frac{1}{x^2}\right) + j \cdot Q \cdot \left(x - \frac{1}{x}\right)} \right|$$

Or,

$$M = \frac{1}{\sqrt{\left[1 + \frac{1}{k} \cdot \left(1 - \frac{1}{x^2}\right)\right]^2 + \left[Q \cdot \left(x - \frac{1}{x}\right)\right]^2}}$$

Per Figure 15, M is also equals to the output voltage to bus voltage ratio:

$$M = \frac{n \cdot Vout \cdot \frac{4}{\pi}}{2 \cdot \frac{Vbus}{\pi}} = \frac{Vout}{Vbus} \cdot 2 \cdot n$$

So the conversion ratio of output voltage Vout to bus voltage Vbus is:

$$\frac{Vout}{Vbus} = \frac{M}{2 \cdot n}$$

4. Transformer and Resonant Circuit Design

The system input data:

Parameter	Unit	Description	Value
$Vbus_{max}$	V	The maximum DC bus voltage	480
$Vbus_{min}$	V	The minimum DC bus voltage	440
$Vbus_{nom}$	V	The nominal DC bus voltage	460
Vout	V	The DC output voltage	48
Iout	A	The output load current	1.4
F_{r1}	kHz	The resonant frequency	60
Fmax	kHz	The maximum switching frequency	120
Dmax		The maximum duty-cycle	0.5
		Transformer core size	E32/16/9

Note: Typically set Fmax < 2 x F_{r1} as the parasitic capacitance in the system introduces a third resonant frequency that could cause the output voltage to increase with switching frequency at no load if the maximum switching frequency is higher than the limit.

Step 1: Calculate the transformer turns ratio

$$n = \frac{Vbus(\max)}{2 \cdot Vout},$$

$$n = \frac{480}{2 \cdot 48} = 5$$

The transformer turns ratio is calculated with the maximum input voltage to make sure the output is always under regulation, including the worst case - high-line voltage and no load condition.

Step 2: Choose k value

k is the ratio between the transformer magnetizing inductance and the resonant inductance. Smaller *k* value gives steeper gain curve, especially at the below resonant ZVS region as shown in figure 16. The output voltage is more sensitive to frequency variation with smaller *k* factor.

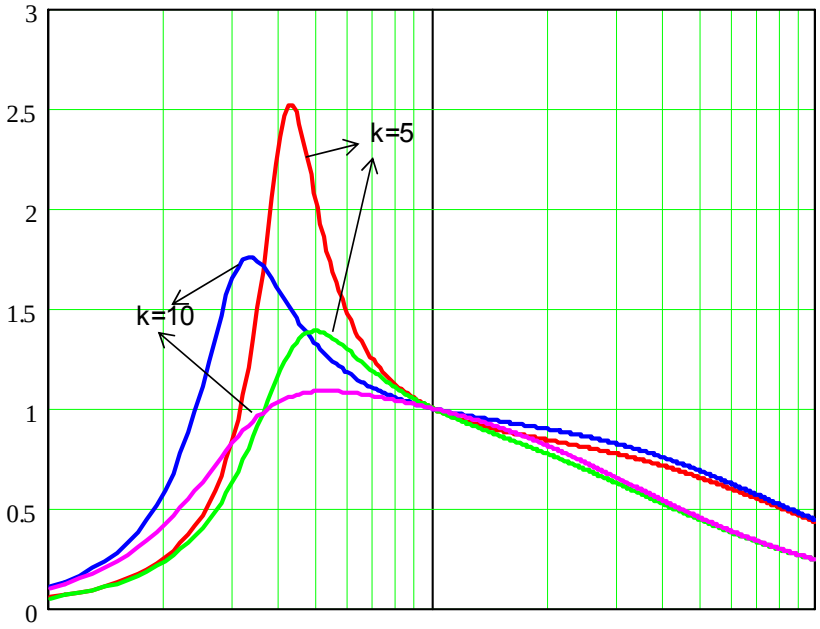


Figure16: k factor

A higher *k* value results in higher magnetic inductance and thus lower magnetizing current in the transformer primary winding – that means lower circulating power losses. However, higher magnetic inductance could also cause non-ZVS switching at high line and zero load condition where the circulating current is too small to fully charge / discharge the VS node during dead-time.

The recommend range of k is from 3 to 10. In this case $k = 7$ is chosen.

Step 3: Calculate Qmax to stay in ZVS operation at the maximum load under the minimum input voltage

The input impedance of the equivalent resonant circuit (Figure 15) is given by:

$$Zin = j\cdot\omega\cdot Lr + \frac{1}{j\cdot\omega\cdot Cr} + \frac{j\cdot\omega\cdot Lm\cdot Rac}{j\cdot\omega\cdot Lm + Rac}$$

$$Zin = Q\cdot Rac\left|\frac{k^2\cdot x^2\cdot Q}{1 + k^2\cdot x^2\cdot Q^2} + j\left(x - \frac{1}{x} + \frac{x\cdot k}{1 + k^2\cdot x^2\cdot Q^2}\right)\right|$$

To keep the converter working in soft switching mode, the operating point should always remain in the ZVS region as shown in figure 10. The ZVS-ZCS boundary line is defined by the phase angle of Zin Φ(Zin)= 0 (the boundary condition between capacitive and inductive load), i.e. the imaginary part of Zin is zero. With this condition we can calculate the maximum Q which allows the converter to stay in ZVS. The maximum Q happens at the minimum input voltage and the maximum load.

$$Qmax = \frac{1}{k}\cdot\sqrt{\frac{1+k\cdot\left(1-\frac{1}{Mmax^2}\right)}{Mmax^2-1}} = \frac{1}{k}\cdot\sqrt{\frac{1+k\cdot\left[1-\frac{1}{\left(2\cdot n\cdot\frac{Vout}{Vinmin}\right)^2}\right]}{\left(2\cdot n\cdot\frac{Vout}{Vinmin}\right)^2-1}}$$

Where *Mmax* is the maximum conversion ratio at the minimum input voltage,

$$Q\max = 0.523$$

Step 4: Calculate the minimum switching frequency

The minimum switching frequency happens at the maximum load and minimum input voltage with the previous calculated maximum Qmax. As Qmax is defined by Im(Zin)=0,

$$\left(x-\frac{1}{x}+\frac{x\cdot k}{1+k^2\cdot x^2\cdot Qmax^2}\right)=0$$

The Fmin can be calculated with:

$$xmin = \frac{1}{\sqrt{1+k\cdot\left(1-\frac{1}{Mmax^2}\right)}} = \frac{1}{\sqrt{1+k\cdot\left[1-\frac{1}{\left(\frac{2n\cdot Vout}{Vinmin}\right)^2}\right]}}$$

$$x\min = 0.736$$

$$F\min = x\min\cdot F_{r1} = 44.2KHz$$

Step 5: Calculate L_r, C_r and L_m

As Qmax happens at the maximum load, so the resonant components L_r, C_r and L_m can be calculated per the Qmax value that had obtained in step 3:

$$R_{LOAD} = \frac{Vout}{Iout} = \frac{48V}{1.4A} = 34.3\Omega$$

$$Rac = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2} = \frac{8 \times 5^2 \times 34.5}{\pi^2} = 699\Omega$$

$$L_r = \frac{Q\max \cdot Rac}{2 \cdot \pi \cdot F_{r1}} = \frac{0.523 \times 699}{2 \cdot \pi \cdot 44.2 \cdot 10^3} = 1.32mH$$

$$C_r = \frac{1}{2 \cdot \pi \cdot F_{r1} \cdot Q\max \cdot Rac} = \frac{1}{2 \cdot \pi \cdot 44.2 \cdot 10^3 \times 0.523 \times 699} = 9.85nF$$

Choose the nearest standard capacitor value for C_r, $C_r = 10nF$

Recalculate F_{r1} to keep the same Qmax with the selected C_r capacitor:

$$F_{r1} = \frac{1}{2 \cdot \pi \cdot C_r \cdot Q\max \cdot Rac} = 43.5kHz$$

Recalculate L_r with the selected C_r and F_{r1}:

$$L_r = \frac{Q\max \cdot Rac}{2 \cdot \pi \cdot F_{r1}} = 1.33mH$$

The actual L_r value should be lower than the calculated value to stay in ZVS region.
Now calculate L_m value based on L_r and the *k* factor that preset in step 2:

$$L_m = L_r \cdot k = 1.33 \times 7 = 9.31mH$$

Step 6: Calculate transformer primary and secondary turns

The standard half-bridge equation for the transformer turns number calculation is used here:

$$Np = \frac{Vin\min \cdot D\max}{2 \cdot \Delta B \cdot Ae \cdot F\min}$$

With $\Delta B = 0.2T$, $Ae = 0.83cm^2$ (ETD49), $F\min = 28kHz$, $Vin\min = 440V$, $D\max = 0.5$

$$Np = \frac{440 \times 0.5}{2 \times 0.2 \times 0.83 \times 28} \times 10 = 235$$

$$Ns = \frac{Np}{n} = \frac{235}{5} = 47$$

The transformer was designed to be capable of operating down to 28kHz to provide a safety margin although the minimum frequency is 43.5kHz in this design. Np was rounded to the nearest number divisible by n so that Ns would come out as a whole number.

Step 7: Calculate transformer primary and secondary current

In most LLC converter designs the minimum switching frequency is set below the resonant frequency Fr1 in order to maintain output voltage regulation at low line and full load. When the switching frequency is lower than the resonant frequency Fr1, the current waveform is shown as in figure 17.

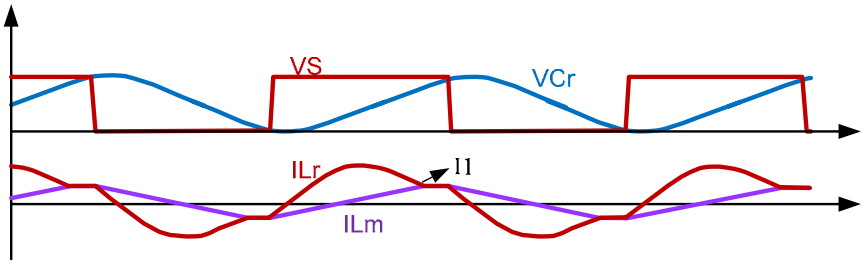


Figure17: Transformer primary current at full load and minimum input voltage

I1 is the current where the resonant current in L_r meets the magnetizing current in L_m. This is also the point where C_r and L_r finish resonance for the first half-period of F_{r1}. At this point, there is no more energy delivered to the load and the output diodes are off. The C_r starts to resonate with L_r + L_m until the switching MOSFETs change states. I1 can be calculated as:

$$I1 = \frac{n \cdot Vout}{2 \cdot Lm \cdot 2 \cdot Fr1} = 0.15A$$

The peak and RMS value of primary current can be estimated as:

$$Ipri(pk) = \sqrt{\left(\frac{Iout \cdot \pi}{2 \cdot n}\right)^2 + I1^2} = 0.47A$$

$$IpriRMS = \frac{Ipri(pk)}{\sqrt{2}} = 0.33A$$

The RMS current is calculated by assuming pure sinusoid current waveform. So the actual primary RMS current is higher than the calculated value.

The current in each secondary winding is very close to a half-sinusoid, thus the peak and RMS current can be estimated by:

$$Ispk = \frac{Iout \cdot \pi}{2} = 2.2A$$

$$Isrms = \frac{Iout \cdot \pi}{4} = 1.1A$$

The wire gauge of primary and secondary windings should be selected properly according to the calculated RMS current.

Step 8: Calculate resonant capacitor voltage

The C_r waveform is shown as in Figure 18:

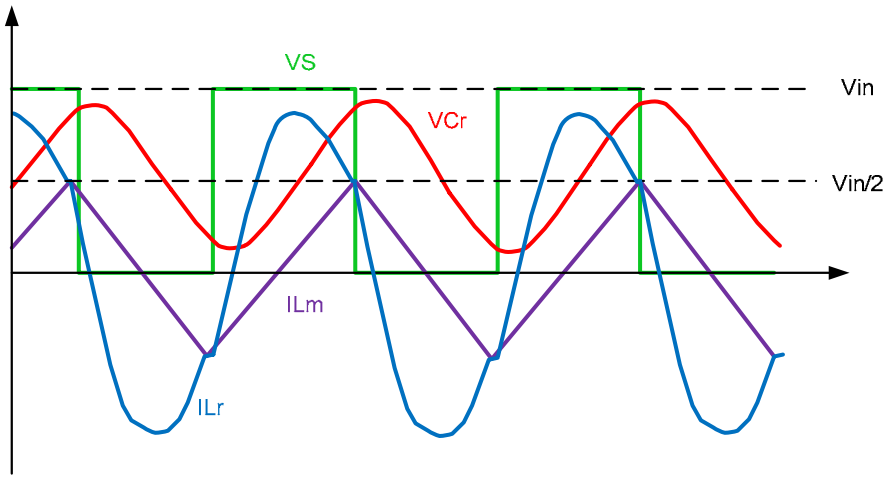


Figure 18: Typical resonant tank voltage and current waveforms

IL_m is the magnetizing current of transformer primary not including the current delivered to the secondary load through an ideal transformer in parallel with L_m. The difference between IL_r and IL_m is the output current.

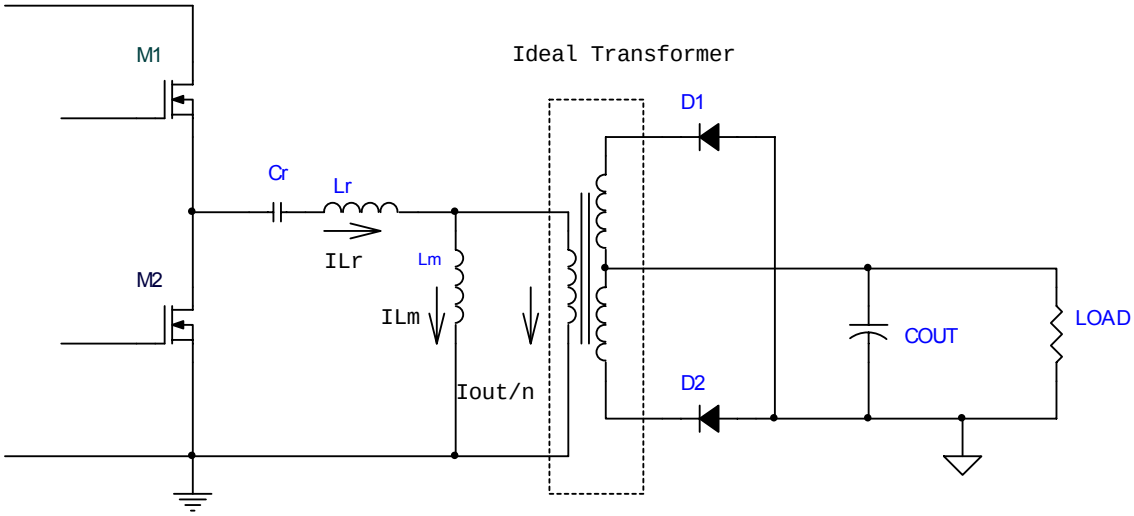


Figure 19: L_m and ideal transformer

The VC_r voltage reaches its peak when L_r current is crossing zero and it is at the mid of input voltage when L_r current reached its peak. The C_r voltage is at the maximum value when VS node is zero and it is at the minimum value when VS node is equals to Vin. So VC_{rmin} and VC_{rmax} can be calculated as:

$$VC_{r\max} = n \cdot Vout + Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}$$

$$VC_{r\min} = Vin - n \cdot Vout - Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}$$

The peak to peak voltage ripple of VC_r is VC_{rmax}-VC_{rmin}:

$$VC_{rpk\_pk} = 2n \cdot Vout + 2 \cdot Ipri(pk) \times \sqrt{\frac{L_r}{C_r}} - Vin$$

It can be seen that the maximum peak-to-peak voltage happens at the maximum load and the minimum DC input Vinmin, the switching frequency is at the minimum Fmin.

In this example:

$$Vcrpk\_pk = 2 \times 5 \times 48V + 2 \times 0.47A \times \sqrt{\frac{1.33mH}{10nF}} - 460V = 363V$$

The resonant capacitor C_r can be selected according to the capacitance value together with its voltage and current rating. Polypropylene film capacitor is preferred to use for lower power loss. Polypropylene film capacitors are rated at DC voltage or 50Hz AC voltage with voltage de-rating at high frequency. The ability of withstanding high frequency voltage is limited by thermal (power dissipation) and peak current capability. Even though the calculation result shows the maximum AC RMS voltage is 363V, a capacitor with higher voltage rating should be chosen per its frequency curve. Below is an example of EPCOS MKP capacitor B32612 (1000Vdc/250Vac).

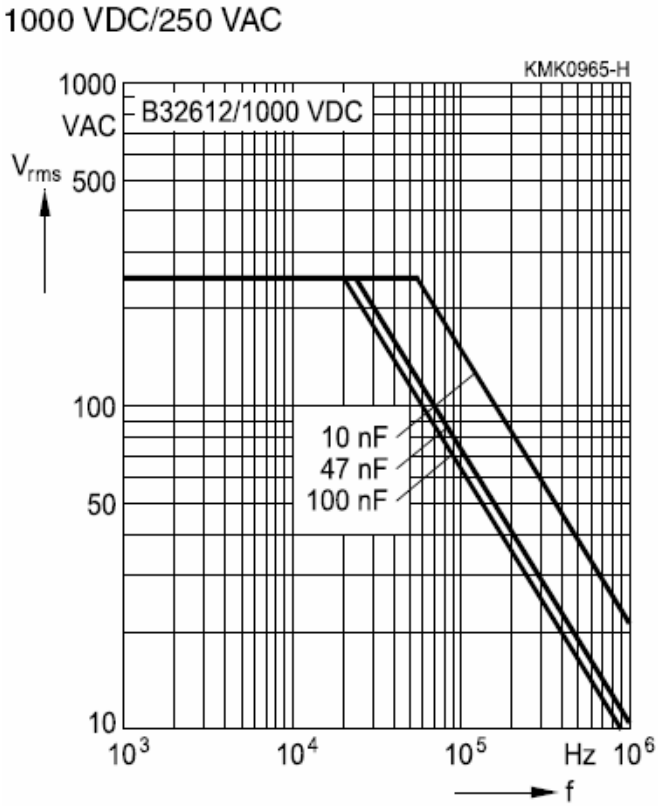
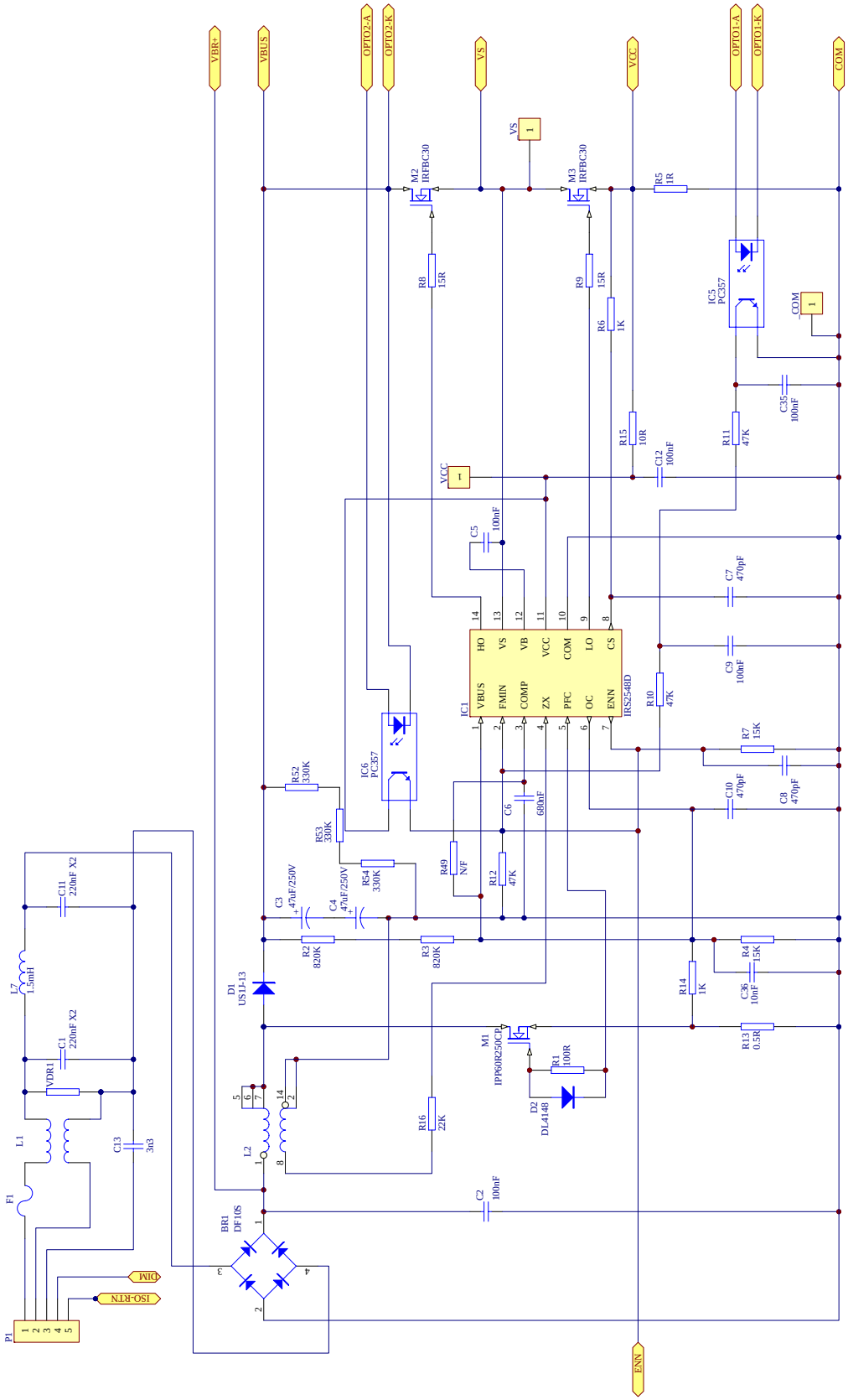
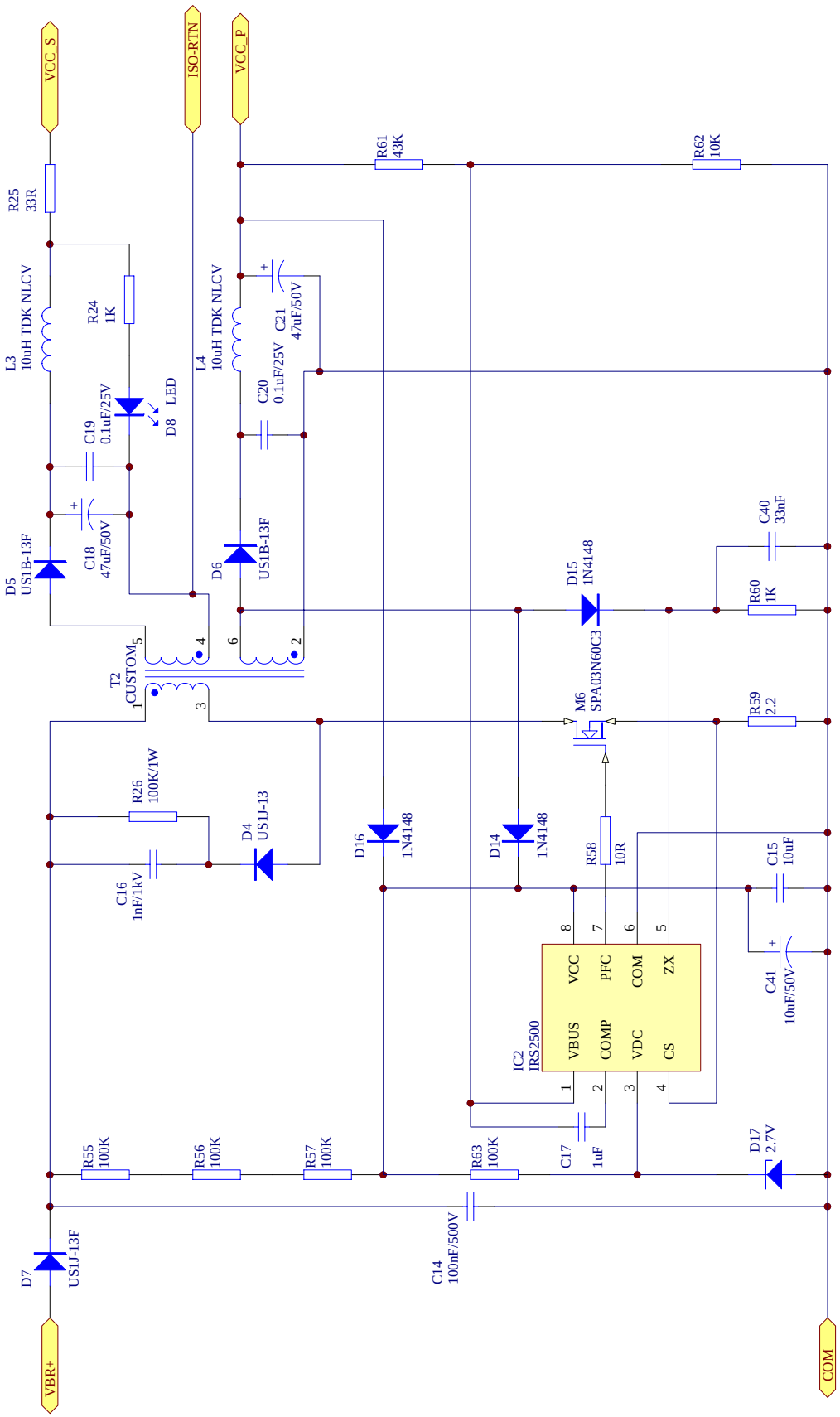


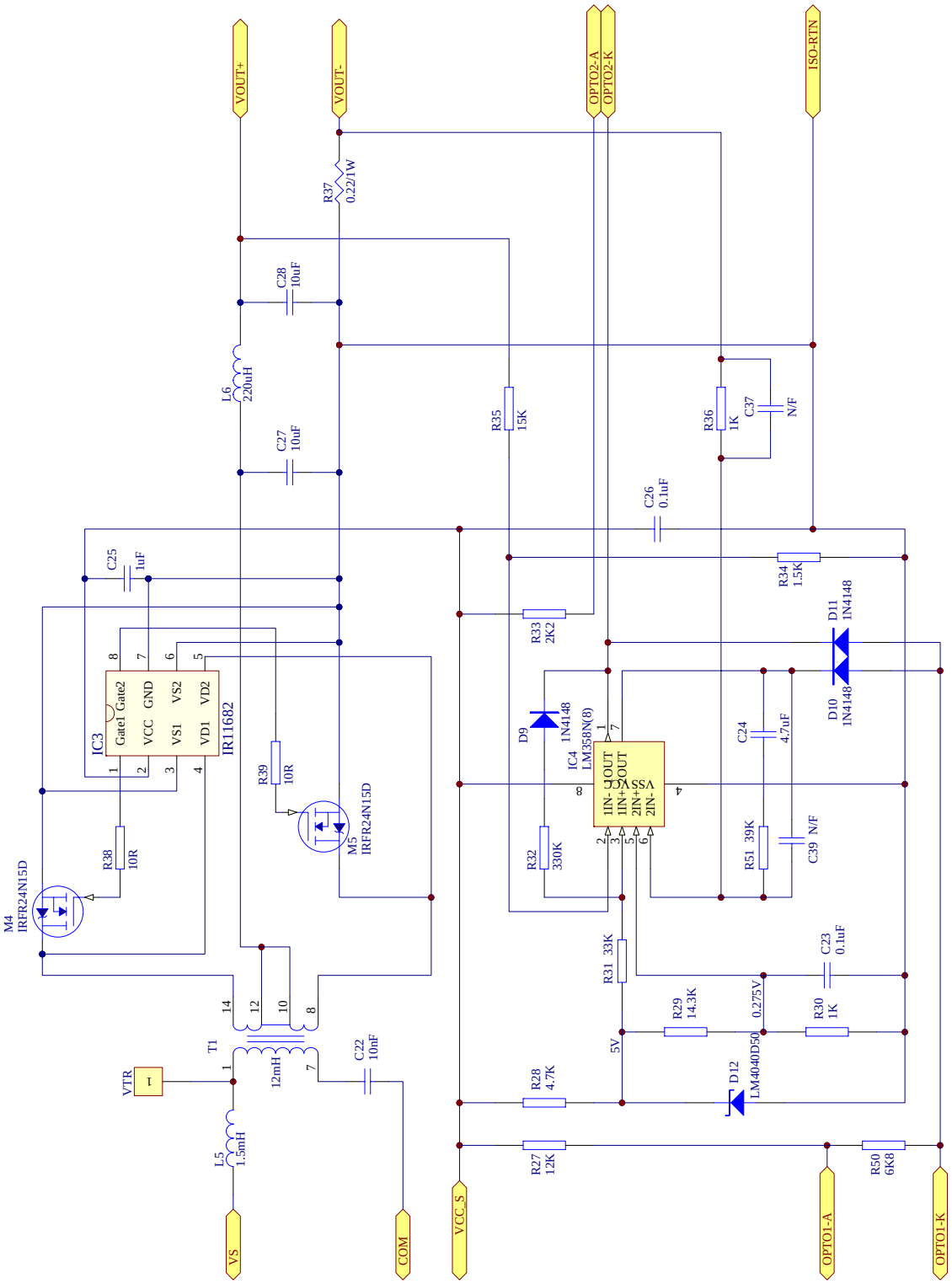
Figure 20: Vrms vs. frequency curve of MKP capacitor B32612 @ Ta<=90°C

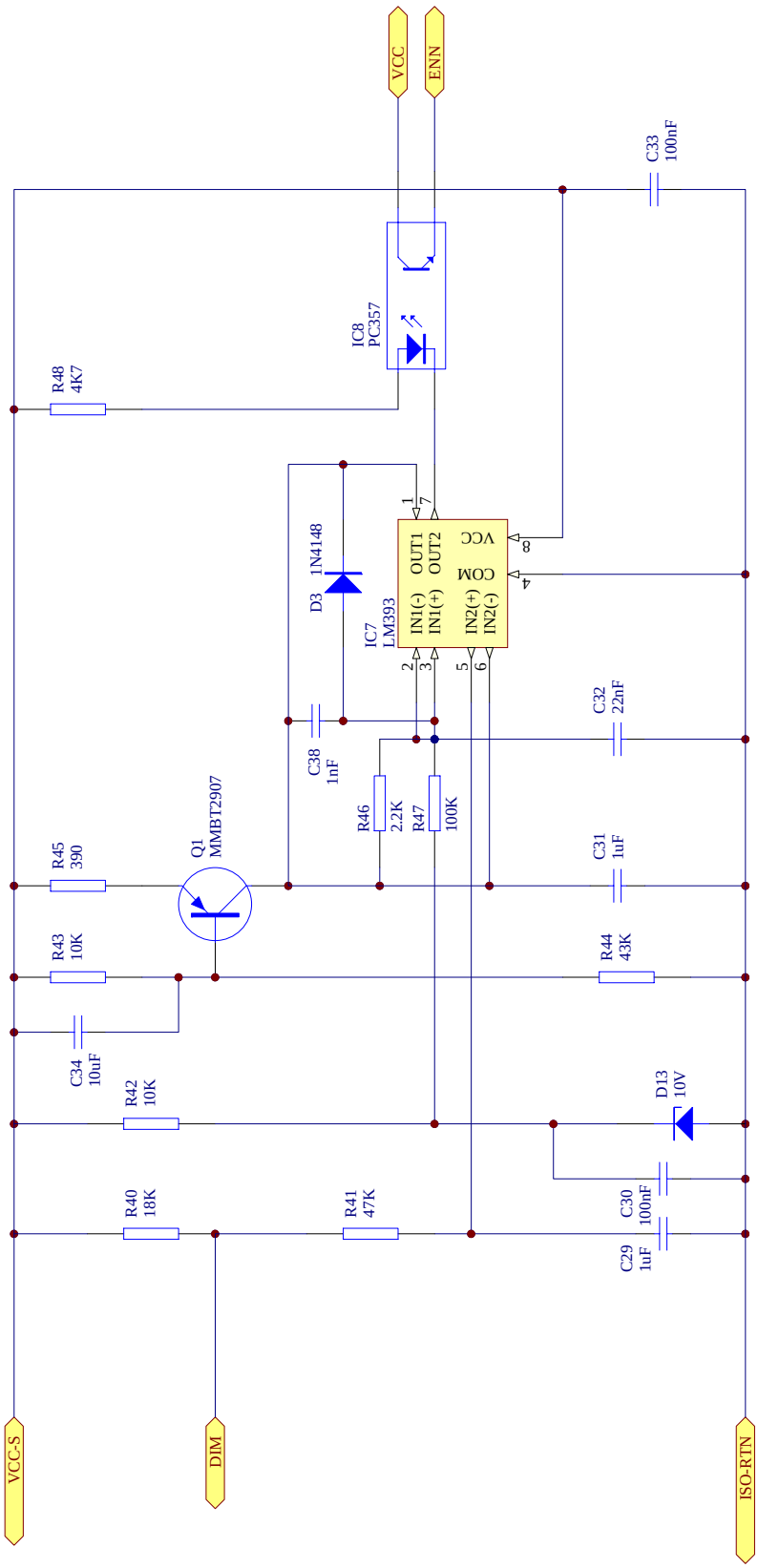
In practice the transformer (T1) used on the IRPLLED5 board has a magnetizing inductance of 12mH and the series resonant inductor (L5) has a value of 1.5mH. This allows a low cost off the shelf inductor to be used for L5 while maintaining a similar ratio between Lm and Lr.

5. IRPLLED5 Board Schematics




VCC_S
ISO-RTN
VCC_P
R25 33R
L3 10uH TDK NLCV
R24 1K
D8 LED
C19 0.1uF/25V
C18 47uF/50V
D5 US1B-13F
L4 10uH TDK NLCV
C20 0.1uF/25V
C21 47uF/50V
D6 US1B-13F
R61 43K
R62 10K
C40 33nF
R60 1K
D15 1N4148
M6 SPA03N60C3
R59 2.2
T2 CUSTOM
R26 100K/1W
C16 1nF/1kV
D4 US1J-13
D16 1N4148
D14 1N4148
R58 10R
C15 10uF
C41 10uF/50V
IC2 IRS2500
VCC
PFC
COM
ZX
VBUS
COMP
VDC
CS
R55 100K
R56 100K
R57 100K
R63 100K
C17 1uF
D17 2.7V
C14 100nF/500V
D7 US1J-13
VBR+
COM


VOUT+
VOUT-
OPTO2-A
OPTO2-K
ISO-RTN
R37
0.22/1W
C28
10uF
L6
220uH
C27
10uF
R35
15K
R36
1K
C37
N/F
C26
0.1uF
C25
1uF
R34
1.5K
D11
1N4148
D10
1N4148
R33
2K2
IC3
IR11682
Gate1
Gate2
VCC
GND
VS1
VS2
VD1
VD2
D9
1N4148
IC4
LM358N(8)
C24
4.7uF
R39
10R
M5
IRFR24N15D
R38
10R
M4
IRFR24N15D
R32
330K
R51
39K
C39
N/F
R31
33K
C23
0.1uF
R29
14.3K
0.275V
R30
1K
T1
12mH
C22
10nF
VTR
5V
D12
LM4040D50
R28
4.7K
L5
1.5mH
R27
12K
R50
6K8
VS
COM
VCC_S
OPTO1-A
OPTO1-K


VCC
ENN
C33
100nF
IC8
PC357
R48
4K7
D3
1N4148
IC7
LM393
OUT1
OUT2
VCC
COM
IN1(-)
IN1(+)
IN2(+)
IN2(-)
C32
22nF
C38
1nF
R46
2.2K
R47
100K
Q1
MMBT2907
R45
390
C31
1uF
R43
10K
R44
43K
C34
10uF
R42
10K
D13
10V
R40
18K
R41
47K
C30
100nF
C29
1uF
VCC-S
DIM
ISO-RTN

6. Auxiliary VCC Supply

The IRPLLED5 LED driver board required two low voltage power supplies that can provide VCC voltages for the primary and secondary circuitry. The primary circuitry including the IRS2548D (IC1) is supplied by VCC_P and the secondary circuitry including the IR11682 synchronous rectification controller (IC3) is supplied by VCC_S. The VCC_P supply does not require isolation but the VCC_S supply does since it is connected to the isolated output circuitry of the driver. As the system utilizes PWM dimming that pulses both the half-bridge drive and the PFC on and off to adjust the LED light level in burst mode, it is not possible to obtain VCC_P and VCC_S from the PFC or from the half-bridge by means of a charge pump. This is because at low dimming levels the system would be switching for insufficient time to supply these rails. In fact as the system can be dimmed to zero output it would not be possible to supply any low voltage circuitry under this condition with such a scheme. Because of this a small Flyback power supply has been used to produce VCC_P and VCC_S continuously, supplied by the rectified AC line voltage and independent of the PFC and half-bridge switching operation.

The Flyback converter is based on the IRS2500 (IC2) SMPS/PWM controller with a 600V switching MOSFET (M6) in conjunction with the Flyback inductor (T2). On startup C15 is charged from the rectified AC line through R55,R56 and R57 until the UVLO is reached and IC2 starts to provide gate drive to M6. C15 is required to be 10uF in order that the system can continue to switch long enough for VCC_P to come up and take over supplying VCC to IC2. An additional isolated winding on T2 provides VCC_S. An LED (D8) has been included on the board to indicate that this auxiliary power supply circuit is operating. The voltages provided at VCC_P and VCC_S are regulated by IC2 at approximately 14V. Voltage feedback is provided via R61 and R62 dividing 14V down to the 2.5V regulation voltage of the IRS2500. Primary peak current limiting is provided through R59 which prevents the primary current of T2 reaching a high enough level for saturation to occur. This primary side cycle by cycle peak current limit also prevents damage occurring if either VCC_P or VCC_S become short circuited.

In this design the Flyback converter is operating in discontinuous conduction mode using the zero crossing detection input of IC2 to produce an approximate fixed off time determined by the time constant of R60 and C40. During the period of the switching cycle when M6 turns off, the voltage at T2 pin 6 transitions from negative to positive and C40 is charged through D15. When all of the energy stored in T2 has been transferred the voltage at pin 6 of T2 drops to zero and C40 discharges through R60. When the voltage at the ZX input of IC2 drops below an internal threshold the start of the next cycle is triggered. Since the power requirement for this Flyback converter is less than one Watt, the off time can be very long compared to the on time and the conduction time in which energy is transferred to the VCC_P and VCC_S outputs. The end result is a power supply operating within a fairly narrow frequency range determined by R60 and C40.

7. Magnetics Specifications

International
IOR Rectifier

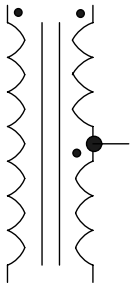
PFC INDUCTOR SPECIFICATION

Supplier: Murata Part Number: CD1488C

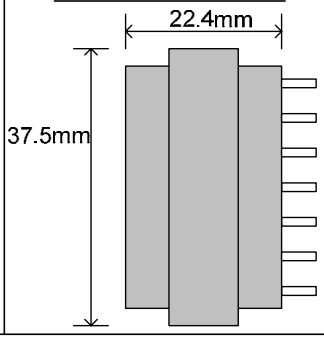
CORE SIZE	E32/16/9 (EF32)		
BOBBIN	HORIZONTAL	PINS	14
CORE MATERIAL	Philips 3C85, Epcos N27 or equivalent		
PRIMARY INDUCTANCE	0.95	mH	
AIR GAP LENGTH	1.0	mm	
PRIMARY PK TO PK VOLTAGE	500	Vpk	
MAXIMUM CORE TEMPERATURE	100	°C	
WINDING ISOLATION (Pri to Sec)	2000	V	

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
Primary	1	7	83	5 Strands of AWG 32
Secondary	14	8	8	1 Strand of AWG 32

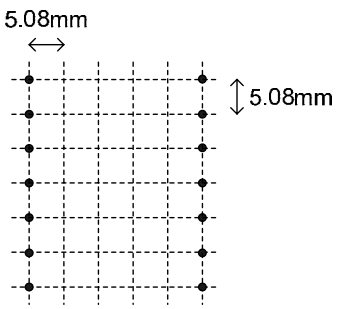
ELECTRICAL LAYOUT



PHYSICAL LAYOUT



TOP VIEW



TEST (TEST FREQUENCY = 50kHz)

PRIMARY WINDING INDUCTANCE	MIN 0.85	mH	MAX 1.05	mH
SECONDARY WINDING RESISTANCE	MAX 0.1	Ohms		

International
IOR Rectifier

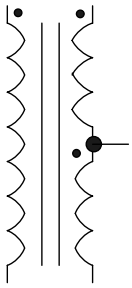
TRANSFORMER SPECIFICATION

Supplier: Murata Part Number: CD1490C

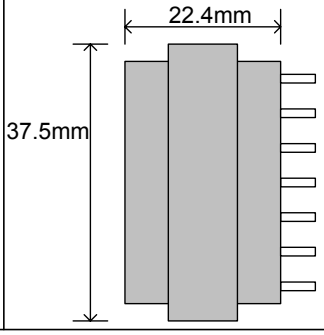
CORE SIZE	E32/16/9 (EF32)		
BOBBIN	HORIZONTAL	PINS	14
CORE MATERIAL	Philips 3C85, Epcos N27 or equivalent		
PRIMARY INDUCTANCE	12	mH	
AIR GAP LENGTH	0.4	mm	
PRIMARY PK TO PK VOLTAGE	500	Vpk	
MAXIMUM CORE TEMPERATURE	100	ºC	
WINDING ISOLATION (Pri to Sec)	2000	V	

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
Primary	1	7	235	1 Strand of AWG 32
Secondary (1)	14	12	47	5 Strands of AWG 32
Secondary (2)	10	8	47	5 Strands of AWG 32

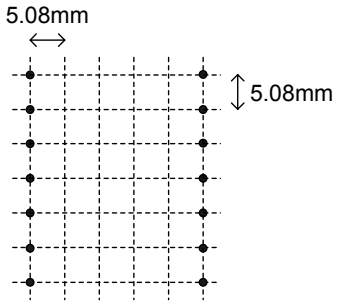
ELECTRICAL LAYOUT



PHYSICAL LAYOUT



TOP VIEW



TEST (TEST FREQUENCY = 50kHz)

PRIMARY WINDING INDUCTANCE	MIN 11	mH	MAX 13	mH
SECONDARY WINDING RESISTANCE	MAX 0.1	Ohms		

International
IOR Rectifier

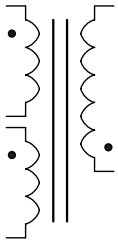
FLYBACK INDUCTOR SPECIFICATION

Supplier: Murata Part Number: CD1491C

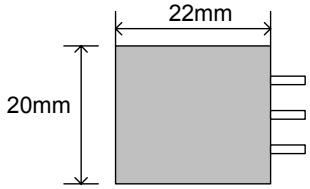
CORE SIZE	E20/10/6 (EF32)		
BOBBIN	VERTICAL	PINS	6
CORE MATERIAL	Philips 3C85, Epcos N27 or equivalent		
PRIMARY INDUCTANCE	1.4	mH	
AIR GAP LENGTH	~0.13	mm	
PRIMARY PK TO PK VOLTAGE	500	Vpk	
MAXIMUM CORE TEMPERATURE	100	ºC	
WINDING ISOLATION (Pri to Sec, Pri to Iso)	1000, 2000	V	

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
Primary	1	3	71	1 Strand of AWG 35
Secondary	2	6	11	1 Strand of AWG 30
Isolated	4	5	11	1 Strand of AWG 30

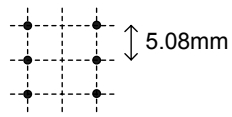
ELECTRICAL LAYOUT



PHYSICAL LAYOUT



TOP VIEW



TEST (TEST FREQUENCY = 50kHz)

PRIMARY WINDING INDUCTANCE	MIN 1.2	mH	MAX 1.6	mH
SECONDARY WINDING RESISTANCE	MAX 0.1	Ohms		

8. Output Current Regulation

The IRPLLED5 produces a regulated constant current output at a nominal 1.4A. The current is regulated by adjusting the frequency of the half-bridge LLC resonant power stage. The maximum available output is at minimum frequency, which is programmed by R12 (also referred to as RFMIN). Figure 8 shows the relationship between this value and the frequency. The IRS2548D has a fixed dead time of approximately 1.8uS, which is long enough to accommodate the half-bridge voltage transition without allowing additional ringing oscillations to occur. The frequency is increased by sinking additional current from IC1 pin 2 (FMIN) through R10 and R11 and opto-isolator IC5. The half-bridge oscillates at maximum frequency when the transistor in IC5 is fully switched on and this frequency is programmed by the values of R10 and R11. Capacitors C9 and C35 have been added to remove noise transients since the FMIN input of the IRS2548D is very sensitive and this can cause frequency jittering resulting in flicker. It is also necessary for R10 and C9 to be located very close to IC1 with very short traces and a direct connection to the signal ground at the COM pin.

IC5 is driven by the feedback circuitry at the isolated output. The output current is sensed through shunt resistor R37 and compared with a reference voltage of 0.275V (nominal) programmed by R29 and R30. D12 provides a temperature stable accurate 5V reference voltage from which the current reference is derived. IC4 is an LM358 dual operational amplifier where one half is used for the current feedback error amplifier and the other half is used for over voltage protection. The outputs are ORed together via diodes D10 and D11 to provide a current sink for the diode of IC5.

The current feedback loop has a very slow response time. This is in order not to interfere with the operation of the PFC front end stage whose error amplifier within IC1 has a response time covering several AC line half cycles. This is so that the on time remains constant during each cycle so that the input current waveform is able to follow the voltage waveform to be sinusoidal. The IRS2548D also contains circuitry that extends the on time close to the AC line zero crossings on a cycle by cycle basis in order to optimize THD, however this has negligible effect on the overall operation of the bus voltage regulation loop. As is typical in Boost PFC front end stages there exists some ripple on the DC bus at twice the line frequency. The back end stage current regulation loop must be slower than the PFC loop to prevent interference between the two loop that could introduce a sub-harmonic oscillation in the system and produce instability in the light output. If the current loop were to be made much faster than the PFC loop there would be distortion of the input current waveform since the effective load would be varying within the AC line cycle. The current loop speed is determined by R36, R51 and C24. R36 remains at 1K to provide a low input impedance to the current error amplifier, which greatly reduces error caused by noise pickup. Since the half-bridge produces high dV/dT during switching, the system is liable to pick up noise at sensitive

nodes and therefore each part of the circuit has been designed to minimize noise sensitivity.
The output voltage is sensed through R35 and R34. If the output exceeds 60V, which is the safety low voltage limit according to UL standards, IC4 pin 2 exceeds 5V and the output at pin 1 is driven low. This causes the half-bridge frequency to be forced to maximum and also switches on opto isolator IC6, which pulls up on the ENN pin and disables IC1. The PFC and half-bridge drives remain off until the output voltage drops to a low level because of the hysteresis provided by R32 and D9. This means that under an open circuit condition the output will continuously pulse to 60V and then decay. This burst mode of operation provides minimum power consumption during an open circuit condition.

9. 0 to 10V Dimming

Dimming is implemented using the PWM / burst mode controlled through the ENN input of IC1. A square wave signal is supplied to this input during dimming through opto isolator IC8. When this input exceeds the ENN input threshold the gate drive to the PFC and half-bridge MOSFETs are disabled. The compensation capacitor C6 at IC1 pin 3 is not discharged during this period and retains its voltage so that when switching starts up again the DC bus voltage can be regulated to the required level rapidly since C6 does not need to charge from zero to its previous level each time. This allows the DC bus voltage to remain quite stable even though the load is being pulsed on and off. This method of dimming allows stable control down to low levels. The output can be dimmed all the way to zero and back up again.
The dimming control circuitry is referenced to the output so that it is isolated from the AC line input and can be safely connected to any 0-10V dimming control source. It has an internal pull up so that if no dimming input is connected the system defaults to maximum output. This is compatible with most current sinking 0-10V dimmer controls that are often powered from the ballast itself.
A sawtooth waveform varying from 0 to 10V is generated using current source Q1 in conjunction with C31. The frequency is around 150Hz (above the flicker limit of 120Hz) and can be adjusted via R45, however at higher frequencies the delay in IC8 could become significant. The sawtooth waveform is compared with the 0-10V dimming control input to produce a rectangular waveform with a duty cycle that varies from 0 to 100% proportionally with the 0-10V dimming input. Dual comparator IC7 uses one comparator to create the sawtooth oscillator and the other to compare this with the control input and produce the PWM output to IC8.
It would be possible to replace this circuitry with a digital scheme such as a DALI interface based on a micro-controller to produce a similar PWM control input.

10. Test Results

Load: 2 x TT Electronics OPA731 connected in series

VACin (Vrms)	Pin (W)	PF	THDi (%)	Fs (kHz)	Vout (Vdc)	Iout (Adc)	Pout (W)	Eff (%)
100	51.1	0.998	3.2	49.5	32.1	1.32	42.4	82.9
120	49.8	0.997	7.2	49.5	32.0	1.32	42.2	84.8
220	49.3	0.973	15.3	49.3	31.9	1.32	42.1	85.4
240	48.9	0.965	16.5	49.7	31.8	1.32	42.0	85.8
277	48.9	0.94	20.0	49.6	31.8	1.32	42.0	85.8

Load: 2 x Eco Lumens EPAD connected in series

VACin (Vrms)	Pin (W)	PF	THDi (%)	Fs (kHz)	Vout (Vdc)	Iout (Adc)	Pout (W)	Eff (%)
100	55.1	0.999	2.3	42.8	39.2	1.22	47.8	86.8
120	55.4	0.998	6.4	42.8	39.1	1.23	48.1	86.8
220	55.0	0.979	13.1	42.8	39.1	1.24	48.5	88.2
240	55.1	0.972	15.6	42.8	39.1	1.24	48.5	88.0
277	55.5	0.952	18.3	42.8	39.1	1.25	48.9	88.1

Short circuit current = 1.5A (at frequency 60.2kHz)

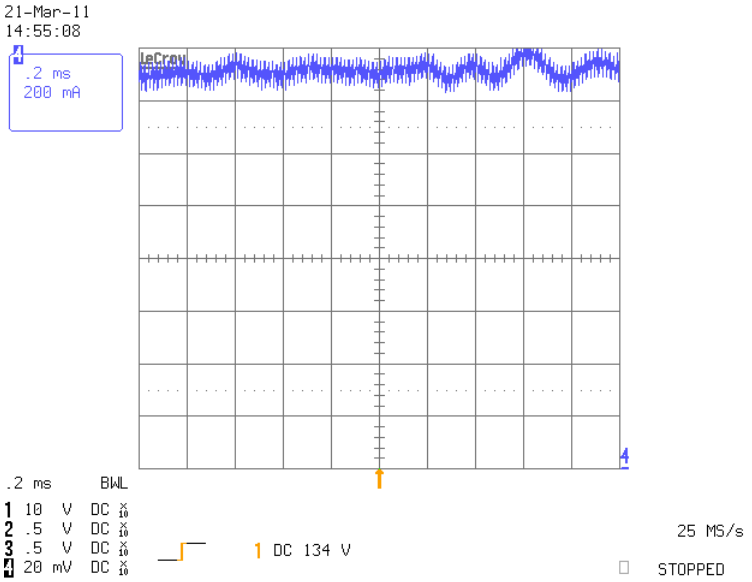


Figure 21: Short Circuit Current

Open circuit voltage = 54V

Open circuit power consumption = 1.4W @ 120VAC and 1.6W @ 230VAC

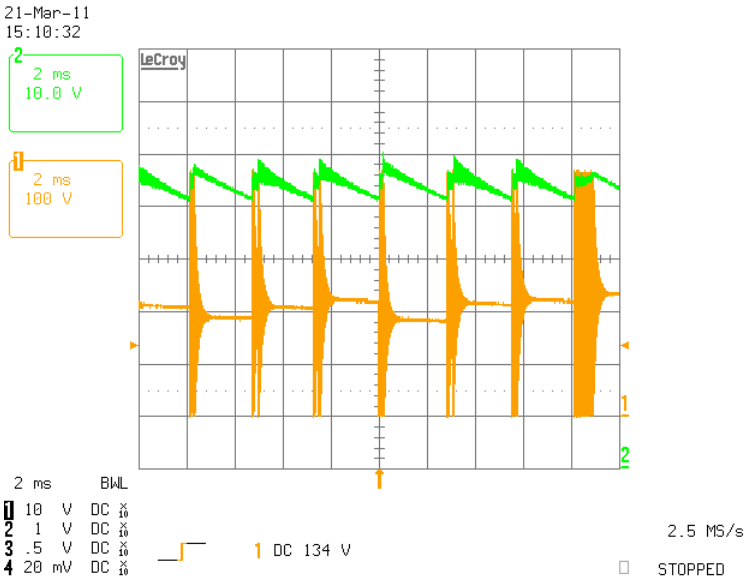


Figure 22: Open Circuit Operation

Channel 1 (orange) shows the half bridge operating in burst mode during an open circuit condition which limits the output to below 60V while minimizing power consumption.

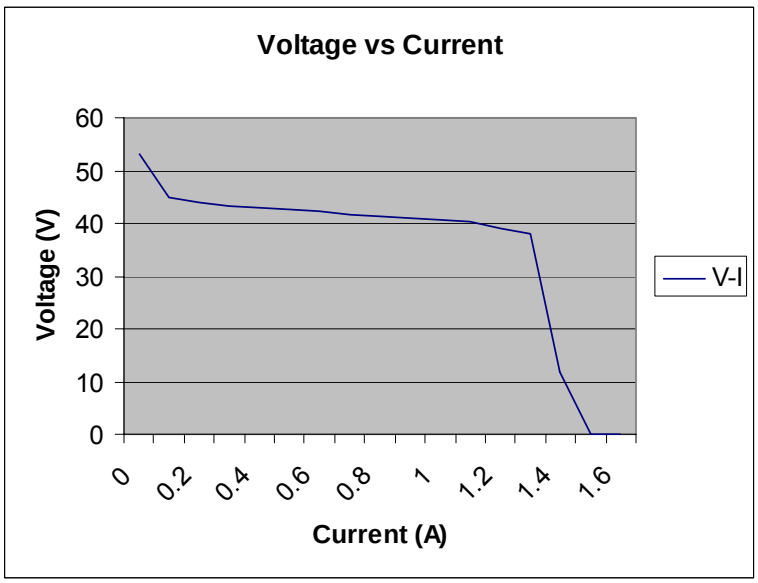


Figure 23: Output V-I Characteristic

Figure 23 shows the output voltage to current characteristic of the converter. This indicates the constant current limiting operation. When tested with a resistive

active load the voltage remains fairly flat over the range of current until the current reaches the regulation limit. For an LED load the voltage is clamped by the sum of the forward voltages of the series LEDs.

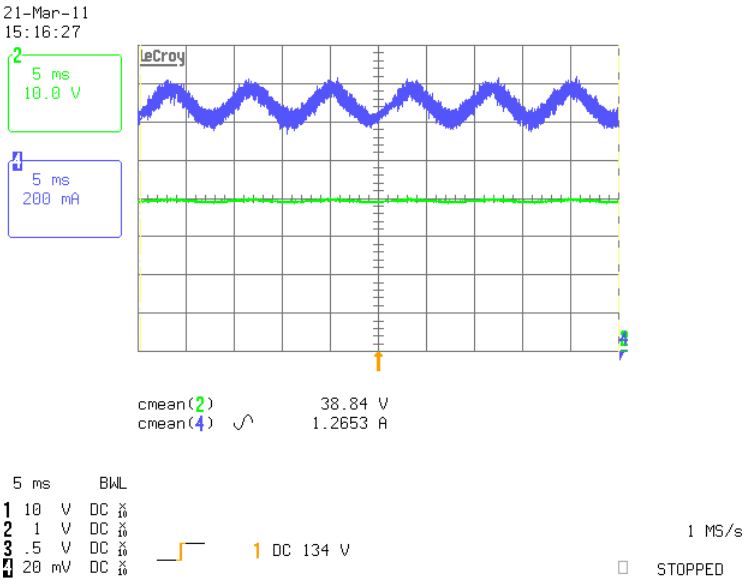


Figure 24: Output Voltage and Current

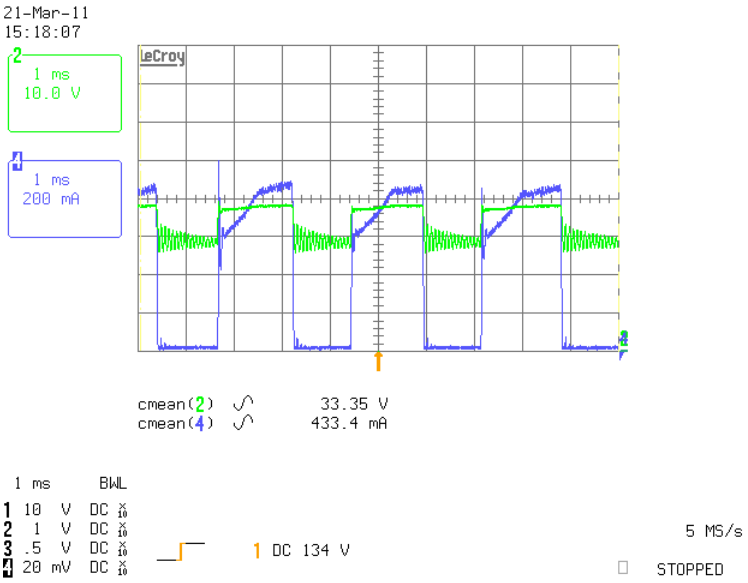


Figure 25: Output Voltage and Current Dimmed

In figure 24, channel 2 (green) shows the output voltage driving an LED load and channel 9 (blue) shows the output current at an average of 1.3A. The current

ripple is 200mApp which is approximately 15%. This has been accomplished without the addition of any electrolytic capacitors at the output.
Figure 25 shows the output current and voltage during dimming operation. During the off phase of PWM / burst mode dimming the LED voltage drops rapidly as the output capacitors discharge to the voltage level where no more current flows through the LEDs because of the forward voltage drop. The current drops to zero during this phase and takes a finite time to recover during the on phase since the output capacitors need to be replenished and the current control loop is slow for reasons described earlier. The peak current drops linearly as the PWM duty cycle is reduced the result of which is an effective combined PWM / linear dimming operation allowing dimming to very low levels.
Some audible noise can be heard during dimming operation since the power supply is being pulsed on and off at a frequency in the region of 150Hz. This could be greatly reduced by varnishing the inductors and placing the board inside an enclosure. It is also possible to increase the PWM dimming frequency although delays in the opto isolators would need to be considered.

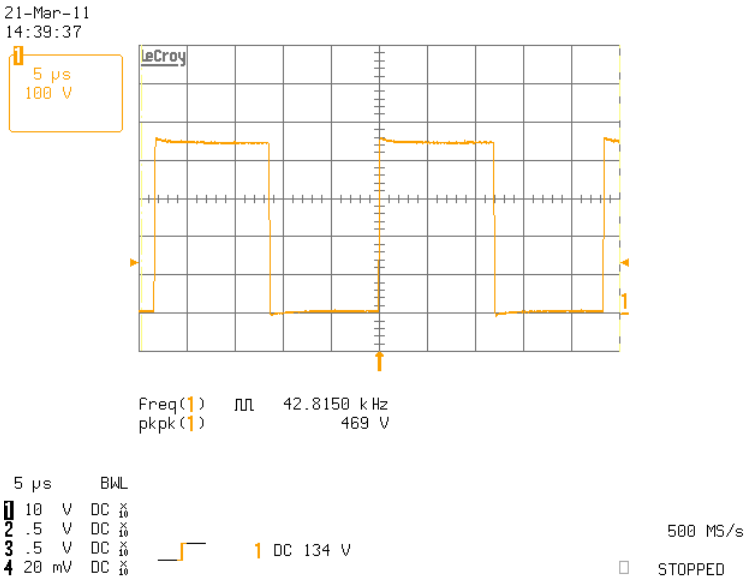


Figure 26: Half Bridge Switching Voltage

Figure 26 shows the half bridge switching waveform operating in the soft switching region with the bus voltage at 469V. The DC bus voltage contains a component of ripple at 120Hz of approximately 15Vpp.
The efficiency for the IRPLLED5 demo board measures between 85% and 90%. This will exceed 90% in higher power designs, however this demo board has been designed to operate at lower power in order to avoid the need for very large and expensive LED loads for test and evaluation.

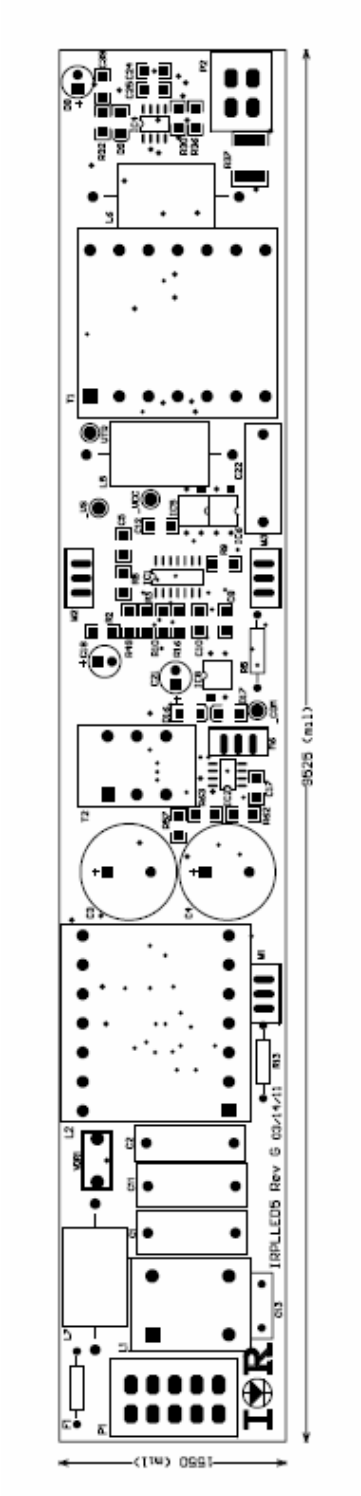
11. Bill of Materials

Item	Qty	Manufacturer	Part Number	Description	Reference
1	1	IR	IRS2548DS	LED Combo Controller, SO14	IC1
2	1	IR	IRS2500S	Flyback controller, SO8	IC2
3	1	IR	IR11682	Sync Rectifier Controller, SO8	IC3
4	1	STM	LM358DT	Dual Opamp, SO8	IC4
5	3	Toshiba	TLP621(BL,T,F)	Opto Isolator, DIP4	IC5,IC6,IC8
6	1	STM	LM393DT	Dual Comparator	IC7
7	1	Infineon	IPP60R250CP	MOSFET, 650V, TO220	M1
8	2	Vishay	IRFBC30A	MOSFET, 600V, TO220	M2,M3
9	2	IR	IRFR24N15DTRLP BF	MOSFET, 100V, DPAK	M4,M5
10	1	Infineon	SPA03N60C3	MOSFET, 650V, TO220	M6
11	1	Diodes Inc	MMBT2907	Transistor, PNP, 60V, SOT23	Q1
12	5	Diodes Inc	US1J-13	Diode, 600V, 1A, SMA	D1,D4,D5,D6,D7
13	8	Diodes Inc	LL4148	Diode, 100V, 200mA, SOD80	D2,D3,D9,D10, D11,D14,D15,D16
14	1	Dialight	521-9327F	LED, Green	D8
15	1	Diodes Zetex	LM4040D50FTA	Voltage Reference, 5V	D12
16	1	Diodes Inc	ZMM5240B-7	Diode, Zener 10V	D13
17	1	Diodes Inc	BZT52C2V7-7-F	Diode, Zener 2.7V	D17
18	1	Fairchild	DF10S	Bridge, 1000v, 1.5A, 4SDIP	BR1
19	1	Murata	CD1490C	Transformer, Resonant, 12mH	T1
20	1	Murata	CD1491C	Flyback Inductor, 1.4mH	T2
21	1	Panasonic	ELF-15N007A	EMI Common Mode Line Filter, 250V	L1
22	1	Murata	CD1488C	Inductor, PFC, 0.95mH	L2
23	2	TDK	NLCV25T-100K-PF	Inductor	L3,L4
24	2	Delevan	4590R-155K	Inductor, 1.5mH, 460mA,Axial	L5,L7
25	1	Delevan	4590R-224K	Inductor, 220uH, 2A, Axial	L6
26	10	Panasonic	ERJ-8GEYJ104V	Capacitor, 0.1µF, 50V, 1206	C5,C9,C12,C19,C20 ,C23,C26,C30,C33, C35
27	2	Panasonic	ECQ-U2A224ML	Capacitor, 220nF,275VAC,X2,TH,.6”	C1,C11
28	1	Panasonic	ECQ-U2A104BC1	Capacitor, 100nF, 275V, TH,O.6”	C2
29	2	Panasonic	EEU-EB2E470S	Capacitor, 47uF, 250V,TH.RAD,0.3”	C3,C4
30	1	TDK	C3216X7R1H684K	Capacitor, 680nF, 50V, 1206	C6
31	3	Yageo	CC1206KRX7R9BB 471	Capacitor, 470pF, 50V, 1206	C7,C8,C10
32	1	EPCOS	B32652A7103J	Capacitor, 10nF, 1.25KV, Polypro, 0.6”	C22
33	1	Vishay	VY1332M59Y5UQ6 3V0	Capacitor, 3.3nF, 500VAC, 0.3” disk	C13
34	2	TDK	C4532X7R1E106M	Capacitor, 10uF, 50V, 1812	C27,C28
35	4	Panasonic	ECJ-3YB1E105K	Capacitor, 1uF, 25V, X7R, 1206	C17,C25,C29,C31
36	1	AVX	12063C102MAT2A	Capacitor, 1nF, 25V, 1206	C38
37	1	TDK	C3216X7R1E475K	Capacitor, 4.7uF, 25V, 1206	C24
38	1	TDK	C3216C0G1E103J	Capacitor, 10nF, 25V, 1206	C36
39	1	TDK	C3216C0G1E223J	Capacitor, 22nF, 25V, 1206	C32
40	1	Vishay	VJ1812Y104KXEAT	Capacitor, 100nF, 500V, 1812	C14

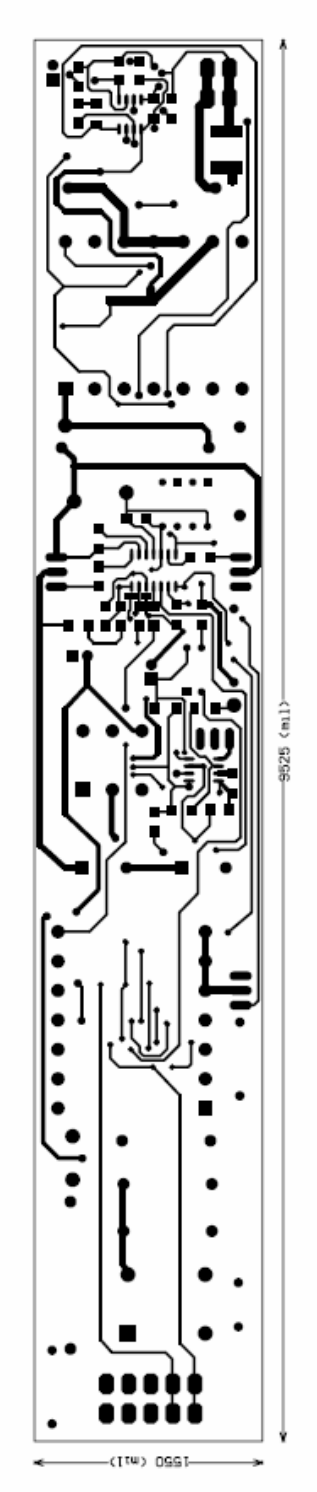
		Vitramon			
41	1	Murata	GRM31BR73A102K W01L	Capacitor, 1nF, 1kV, 1206	C16
42	2	Panasonic	EEU-FC1H470	Capacitor, 47uF, 50V, Radial	C18,C21
43	2	TDK	C1216X5R1E106M	Capacitor, 10uF, 25V, 1206	C15,C34
44	1	Panasonic	EEU-EB1H100S	Capacitor, 10uF, 50V, Radial	C41
45	1	TDK	C3216C0G1E333J	Capacitor, 33nF, 25V, 1206	C40
46	1	Rohm Semi	LTR18EZPJ101	Resistor, 100R, 5%, 1206	R1
47	2	Panasonic	ERJ-8GEYJ824V	Resistor, 820K, 5%, 1206	R2, R3
48	1	Panasonic	ERJ-8GEYJ153V	Resistor, 15K, 5%, 1206	R4
49	1	Vishay	PR01000101008JR 500	Resistor, 1R, 1W, TH 0.5”	R5
50	6	Panasonic	ERJ-P08J102V	Resistor, 1K, 5%, 1206	R6,R14,R24,R30,R36,R60
51	2	Panasonic	ERJ-8GEYJ153V	Resistor, 15K, 5%, 1206	R7,R35
52	2	Panasonic	ERJ-8GEYJ150V	Resistor, 15R, 5%, 1206	R8, R9
53	4	Panasonic	ERJ-8GEYJ473V	Resistor, 47K, 5%, 1206	R10,R11,R12,R41
54	2	Panasonic	ERJ-8GEYJ433V	Resistor, 43K, 5%, 1206	R44,R61
55	1	Vishay / BC	PAC100005007FA1 000	Resistor, 0.5R, 1W, TH 0.5”	R13
56	4	Panasonic	ERJ-8GEYJ100V	Resistor, 10R, 5%, 1206	R15,R38,R39,R58
57	1	Panasonic	ERJ-P08J223V	Resistor, 22K, 5%, 1206	R16
58	1	Panasonic	ERJ-P08J330V	Resistor, 33R, 5%, 1206	R25
59	1	Panasonic	ERJ-P08J123V	Resistor, 12K, 5%, 1206	R27
60	2	Panasonic	ERJ-P08J472V	Resistor, 4.7K, 5%, 1206	R28,R48
61	1	Panasonic	ERG-8ENF1432V	Resistor, 14.3K, 1%, 1206	R29
62	1	Panasonic	ERJ-8GEYJ333V	Resistor, 33K, 5%, 1206	R31
63	4	Panasonic	ERJ-8GEYJ334V	Resistor, 330K, 5%, 1206	R32,R52,R53,R54
64	1	Panasonic	ERJ-P08J222V	Resistor, 2.2K, 5%, 1206	R33
65	1	Panasonic	ERJ-8GEYJ152V	Resistor, 1.5K, 5%, 1206	R34
66	1	Panasonic	ERJ-1TRQJR22U	Resistor, 0.22Ohm, 1W, 2512	R37
67	1	Panasonic	ERJ-P08J183V	Resistor, 18K, 5%, 1206	R40
68	3	Panasonic	ERJ-8GEYJ103V	Resistor, 10K, 5%, 1206	R42,R43,R62
69	1	Panasonic	ERJ-P08J391V	Resistor, 390R, 5%, 1206	R45
70	1	Panasonic	ERJ-8GEYJ222V	Resistor, 2.2K, 5%, 1206	R46
71	5	Panasonic	ERJ-8GEYJ104V	Resistor, 100K, 5%, 1206	R47,R55,R56,R57,R63
72	1	Panasonic	ERJ-8GEYJ682V	Resistor, 6.8K, 5%, 1206	R50
73	1	Panasonic	ERJ-8GEYJ393V	Resistor, 39K, 5%, 1206	R51
74	1	Panasonic	ERJ-1TYJ104U	Resistor, 100K, 1W, 2512	R26
75		Vishay	CRCW2512100KJN EG	Resistor, 100K, 5%, 1W, 2512	R26 (alternate)
76	1	Panasonic	ERJ-8GEYJ2R2V	Resistor, 2.2Ohm, 5%, 1206	R59
77	1	Panasonic	ERZ-V10D511	Varistor, 320VAC, 10mm Diameter	VDR1
78	1	Littelfuse	0215002.MXEP	Fuse, 2A, Fast, 250V	F1
79	1	Wago	235-205	Connector, 5 Way, Light Gray	P1
80	1	Wago	235-202	Connector, 2 Way, Light Gray	P2
81	1			NF	R49
82	1			NF	C39
83	1			NF	C37

12. PCB Layout

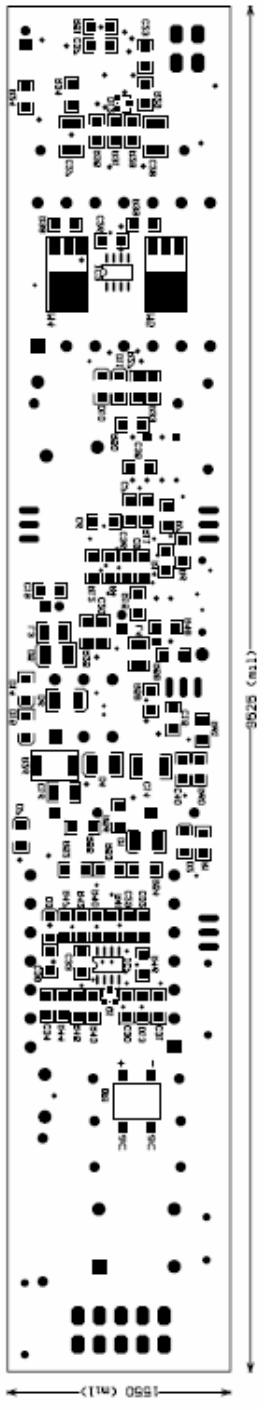
Top Overlay



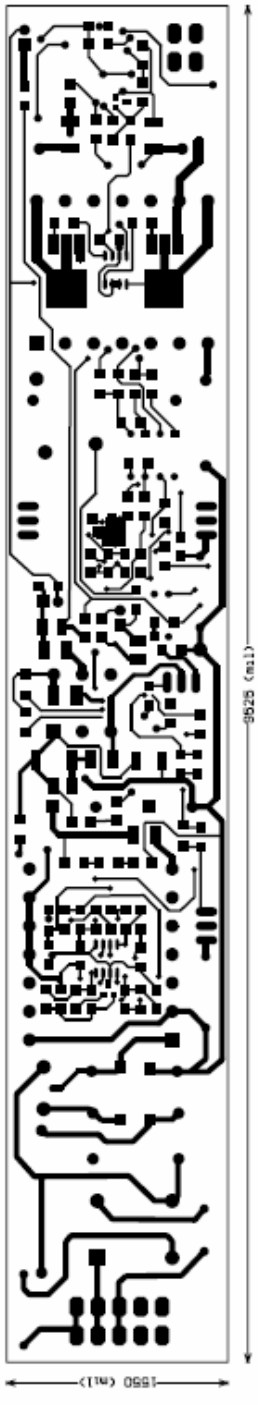
Top Metal



Bottom Overlay



Bottom Metal



References:

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AN-1160 Helen Ding (International Rectifier)