

晶采光電科技股份有限公司 AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AF-240160EFIQW
APPROVED BY	
DATE	

✓ Approved For Specifications

☐ Approved For Specifications & Sample

AMPIRE CO., LTD.

TOWER A, 4F, No.114, Sec. 1, HSIN-TAI 5th RD., HIS-CHIH, TAIPEI HSIEN, TAIWAN(R.O.C.)

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Date: 2005/9/5 AMPIRE CO., LTD.

RECORD OF REVISION

Revision Date	Contents	Editor
2005/1/21	New Release	Rosaline
2005/5/12	Modify White LED back-light characteristics	Tony
2005/9/5	Modify the module electronic characteristics	Lorry

1 FEATURES

(1) Display format: 240×160 dots, 1/160 duty, 1/13 bias.

(2) Construction: LCD panel, Edge LED White backlight and COF technology.

(3) Display type: FSTN, Transflective, Positive, 6 o' clock view.

(4) Controller: "ULTRACHIP" UC1611

(5) Interface for 8080 or 6800 series family MPU, select by BM0, BM1 setting.

2 MECHANICAL DATA

Parameter	Stand Value	Unit
Dot size	$0.23(W) \times 0.23(H)$	mm
Dot pitch	$0.24(W) \times 0.24(H)$	mm
Active area	$57.59(W) \times 38.39(H)$	mm
Viewing area	63.0(W) × 42.5(H)	mm
Module size	$81.0(W) \times 115.5(H) \times 6.5Max.(T)$	mm

3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Logic Circuit Supply Voltage	VDD-VSS	-0.3	+4.0	V
LCD Driving Voltage	VLCD	-4	+18.0	V
Input Voltage	VI	-0.3	VDD+0.3	V
Operating Temp.	Тор	0	50	°C
Storage Temp.	Tstg	-20	70	°C

4 ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Тур	Max	Unit	Note			
		Electro	nic Chara	cteristics						
Logic Circuit Supply Voltage	VDD-VSS		2.4	2.8	3.3	V				
LCD Driving	VLCD	-20 °C				V	* The LCD			
Voltage		0 °C					driving should be decided by real			
(FSTN)		25 °C		14.5*			design.			
		50 °C								
		70 °C								
Input Voltage	VIH		0.8VDD		Vdd	V				
	VIL		-0		0.2 VDD	V				
Logic Supply Current	IDD	VDD=2.8V		0.9	1.2	mA				
Optical Characteristics (FSTN)										
Contrast	CR	25°C		5			Note 1			
Rise Time	tr	25°C		200		ms	Note 2			
Fall Time	tf	25°C		200		ms				
Viewing Angle	θf	25°C &		40			Note 3			
Range	θЬ	CR≥2		35		Deg.				
	θ1			35						
	θr			35						
Frame Frequency	fF	25°C		70		Hz				
	W	hite LED B	ack-light	Characte	ristics	-				
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note			
Forward Voltage	VF	IF=60mA		3.2	3.5	V	Supply Voltage between A&K			
							Note 5			
Forward Current	IF	VF=3.3V		60	80	mA	Note 4			
LCM Luminous intensity		IF=60mA		20		cd/m ²	Note 4			
LED C.I.E	X	IF=60mA	0.28	0.31	0.34		Note 6			
	Y	IF=60mA	0.29	0.32	0.35					

(NOTE 4): Luminous intensity is decided by forward current of White LED.

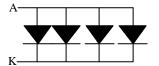
(NOTE 5): White LEDs are with voltage tolerance

(NOTE 6): White LEDs are with color tolerance

Date: 2005/9/5 AMPIRE CO., LTD.

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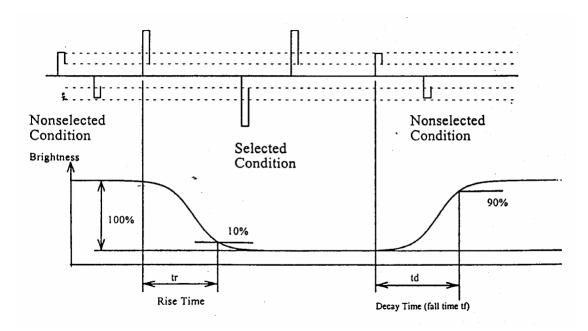
* LED Dice number = 4



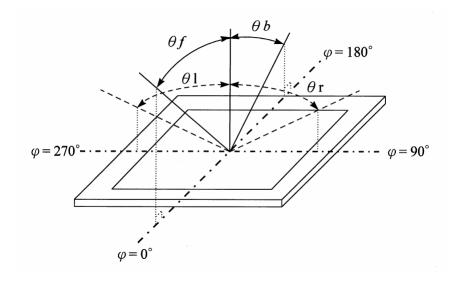
(NOTE 1) Contrast ratio:

CR = (Brightness in OFF state) / (Brightness in ON state)

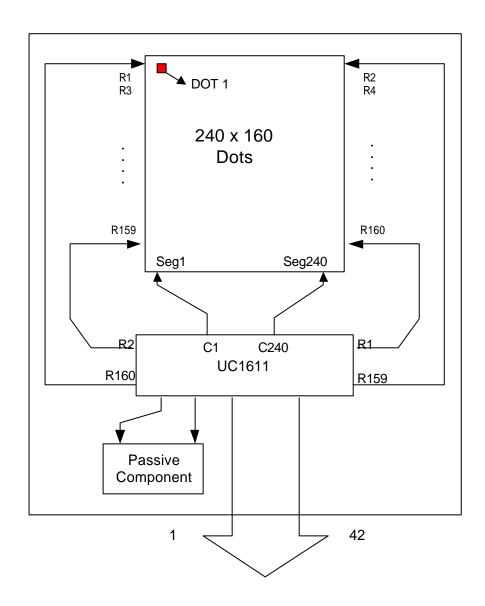
(NOTE 2) Response time:



(NOTE 3) Viewing angle



5 BLOCK DIAGRAM & POWER SUPPLY



Default Setting:

Symbol	H/L	Description
VCM	OPEN	
VS1	OPEN	
VS0	OPEN	Leave that pin "open" in single LCM situation.
PUMP_DN	OPEN	Leave that pin open in single Low situation.
DISP_ON	OPEN	
SCLK	OPEN	
SM	L	Master mode or default in other situation

6 INTERFACE

No.	Symbol	Function							
1	NC	No Connection							
2	VDD	Power supply for logic and other analog circuits.							
3	VSS	Ground (0V)							
4	BM0	Bus modes: "HL": 8 bit 8080 "HH": 8 bit 6800							
5	BM1	BM[1:0] "LL": 4 bit 8080 "LH": 4 bit 6800							
6	WR1	Bus Type: 8080 mode "/RD"; 68mode "E"							
7	WR0	Bus Type: 8080 mode "/WR"; 68 mode "R/W"							
8	CD	Select Control data or Display data for read/write operation.							
		("H": Display data, "L": control data)							
9	CS1	Chip Select. Chip is selected when CS1="H". When the chip is not selected, D[7:0] will be high impedance.							
10	RST	When RST="L", all control register are re-initialized by their default state and/or by their pin configurations if applicable.							
11	D0								
12	D1	4 bits Data Bus for 8080 or 6800							
13	D2	series							
14	D3	8 bits Data Bus for 8080 or							
15	D4	6800 series							
16	D5								
17	D6								
18	D7								
19	VSS	Ground (0V)							
20	NC	No Connection							

7 INSTRUCTION SET

The following is a list of host commands support by UC1611

C/D: 0: Control,

1: Data

W/R: 0: Write Cycle,

1: Read Cycle

Useful Data bitsDon't Care

Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action
Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte @ PA/CA
Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte @ PA/CA
Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status Summary
Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]=D[3:0]
Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4] =D[3:0]
Set Mux rate.	0	0	0	0	1	0	0	0	#	#	Set MR[1:0]=D[1:0]
Set Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]=D[1:0]
Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]=D[1:0]
Set Pump Control	0	0	0	0	1	0	1.	1	#	#	Set PC[3:2]=D[1:0]
Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0]=D[7:0],
(double byte command)	0	0	#	#	#	#	#	#	#	#	where R = 0, or 1
Set Max CA	0	0	0	0	1	1	0	0	1	0	Set MC = D[6:0]
(double byte command)	0	0	-	#	#	#	#	#	#	#	Oct Mo - D[0.0]
Set Start Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]=D[3:0]
Set Start Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]=D[3:0]
Set Page Address LSB	0	0	0	1	1	0	#	#	華	#	Set PA[3:0]=D[3:0]
Set Page Address MSB	0	0	0	1	.1	1	#	祥	#	#	Set PA[7:4]=D[3:0]
Set V _{REF} potential meter (double-byte command)	0	0	1 #	0 #	0 #	0 #	0	0 #	0 #	#	Set PM[5:0]=D[5:0] Set GN[1:0]=D[7:6]
Set RAM Address Control	0	0	1	0	0	0	1	#	#	*	Set AC[2:0]=D[2:0]
Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]=D[3:0]
Set Frame Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]=D[1:0]
Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]=D0
Set Inverse Display	0	0	1	0	1	Ō.	0	1	1	孝	Set DC[0]=D0
Set Display Enable	0	0	1	0	1	0	1	#	#	#	Sat DC[4:2]=D[2:0]
Set LCD Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]=D[2:0]
Set N-Line Inversion	0	0	1	1	0	1	1	#	#	禁	Set DC[7:5]=D[1:0]
Set Gray Scale Mode	0	0	1	1	0	1	0	0	存	排	Set LC[6:5] = D[1:0]
System Reset	0	0	- 1	1	1	0	0	D	1	0	System Reset sequence
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	排	Set BR[1:0]= D[1:0]
Reset Cursor Update Mode	0	0	1	1	4	0	1	1	1	0	Set AC[3]=0, CA=CR;
Set Cursor Update Mode	0	0	1	1	1	Ô	1	1	1	1	Set AC[3]=1, CR=CA;
Set Test Control	0	0	1	1	1	0	0	1.	Ţ		For testing only.
(double byte command)	0	0	养	#	#	#	#	#	#	#	De nat use.

^{*} Other than commands listed above, all other bit patterns result in NOP (No Operation).

DATA FORMAT:

Section Sect												244						- 16	/=n 1			′-1	
Description	MSF	Line Adderss										RAM								SL=0			SL=8
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D7/A D3/O D3/H D7/A D3/O D3/H D7/A D3/O				1	\dashv		7	┪	_	7	7	Page 1		┪	_	╗	\neg	R3	R147	R158	R94		
Page 2	D7/4 D3/0	03H										rayeı					\Box						
D7/A D8/O D8/H D7/A D8/O D7/A	D3/0 D7/4	04H	ĺ								\Box	Page 2											
Page 3														_	_	_	_						
D7/4 D8/0 D8/0 D7/4 D8/0			- 1				_		_	_	_	Page 3	Ш	_	_	_	_						
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D7/4 D3/0 13H D3/0 15H D3/0 D7/4 16H D3/0 D7/4 D3/0 D3/0 D3/0 D3/0 D3/0 D3/0 D3/0 D3/0 D3/0		12H										Page 9											
Page 10 Page 11 Page												r age s											
D7/4 D3/0 15H D3/0 17H D3/0 17H D3/0 17H D3/0 D7/4 18H D3/0 D7/4		1										Page 10					Ц		1				
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D7/4 D3/0 10H D3/0 D7/4 HH D3/0 D7/4 HH D3/0 D7/4 B3/0 R14 R147 R33 R15 R146 R82 R145 R81 R145				Н	\vdash	Н	\dashv	-	\vdash	\dashv	-					_	Н			\vdash			R84
D3/0 D7/4 18H D7/6 D3/0 18H D7/6 D3/0 D3			ı	Н	⊢	Н	\dashv	\neg	-	\dashv	\dashv	Page 14	\vdash	\vdash	_	_	Н	R30				R147	R83
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C774 C30 SICH						Н						Page 15						R32	R16			R145	R81
C7/A C3/O ABH C3/O ABH C3/O ABH C3/O C7/A C3/O ABH C3/O C7/O C3/O C3/O	C774 C376 C374 C374 C376 C376	30H 38H 3FH 40H 41H 42H 43H 44H 45H 46H 47H 40H										Page 71 Page 72 Page 73 Page 74 Page 75 Page 75						R142 R143 R144 R145 R146 R146 R146 R146 R150 R150 R152 R153		RID RIB RIT RIE RIS RIA RIS RI2 RII RIO RO RE RE			######################################
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		Z	4=	CZZI	CZS	CZD	CZ3	CESS	CZZ	C233	12		8	Š	8	S	ō						

CONTROL REGISTERS:

UC1611 contains registers which control the chip operation. These registers can be modified by commands. The commands supported by UC1611 are described in the next section.

Name: The Symbolic reference of the register byte.

Note that, some symbol names refers to collection of bits (flags) within one register byte.

Value after Power-up-Reset and System-Reset. Default:

"PIN" means default value depends on the connection of associated configuration pin(s).

Name	Bits	Default	Description					
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value are between 0 (for no scrolling) and (159 – 2xFL). Setting SL outside of this range cause undefined effect on the displayed image.					
FL	4	ОН	Fixed lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two region: one scrollable, one non-scrollable.					
CR	8	0H	Return Column Address.					
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)					
PA	7	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)					
BR	2	2H	Bias Ratio. The ratio between V _{LCD} and V _D .					
TC	2	1H	Temperature Compensation (per °C). 00: 0.0%					
GN	2	3H	Gain = Vp / VpM					
PM	6	10H	Electronic Potential Meter to generate V _{PM} from V _{REF}					
MR	2	3H	Multiplexing Rate: Number of pixel rows: 0: 64 1: 96 2: 128 3: 160					
OM	2	0	Operating Modes 10: Sleep 11: Normal 01: (Not used) 00: Reset					
BZ	1	_	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.					
RS	. 1		Reset in progress, Host Interface not ready					
PC	4,	ODH	Power Control.					
			PC[1:0]: 00: LCD: <20nF					
		,	PC[3:2]: 00: External V _{LCD} 01: 6x pump 10: 7x pump 11: 8x pump					
APC0	8	00H	Advanced Program Control. Default value should work fine.					

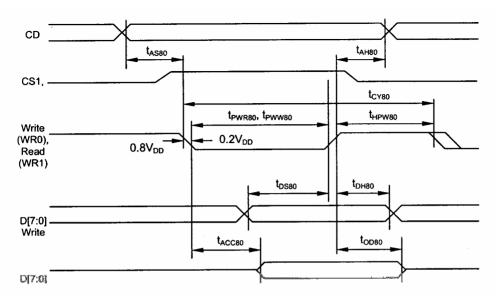
Name	Bits	Default	Description
DC	8	0H	Display Control:
			DC[0]: PXV: Pixels Inverse DC[1]: APO: All Pixels ON DC[4:2]: Display ON/OFF. Each bit controls a set of column drivers (80-80-80). When DC[4:2] is set to "HLH", the chip is turned into a 160x160 controller-driver and the programmers' view of CA becomes 0~159. DC[5]: N-Line inversion. 0: Invert every 17 lines. 1: Invert every 9 lines. DC[6:7]: Idle insertion control when N-Line inversion.
AC	4	1H	Address Control:
			AC[0]: WA: Automatic column/page Wrap Around AC[1]: Auto-Increment order 0: Column (CA) first 1: Page (PA) first AC[2]: PID: PA (page address) auto increment direction (L:+1 H:-1) AC[3]: CUM: Cursor update mode, when CUM=1, CA increment on write only, wrap around suspended
MC	8	EFH	CA max. CA wrapping boundary: when CA+1 = MC, CA will reset to 0. The proper value range for MC is 0-239 or 0~159, depends on the value of DC[4:2]. The chip's behavior is undefined when MC is out of these ranges.
LC	6	08H	LCD Control: LC[0]: MSF: MSB First mapping Option LC[1]: MX, Mirror X (Column sequence inversion) LC[2]: MY, Mirror Y (Row sequence inversion) LC[4:3]: Frame Rate 0: 135 fps 1: 150 fps 2: 165 fps 1: 185 fps LC[6:5]: Gray Scale selection 00: 16 gray scale 01: 8 gray scale

Date: 2005/9/5

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8 TIMING CHARACTERISTICS

8080-SYSTEM

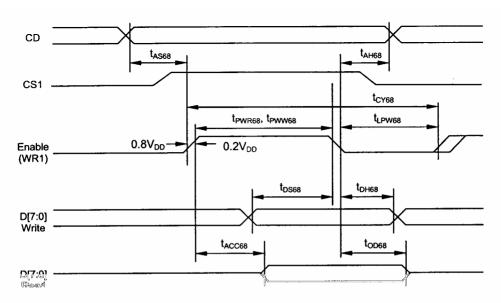


Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
tasso tahso	CD	Address setup time Address hold time		20 40	_	ns
toyeo		System cycle time		100	-	ns
teweso	WR1	Pulse width (read)		45		ns
tewwee	WRO	Pulse width (write)		45	-	กร
therweo	WR0, WR1	High pulse width		40		ns
tosao tohan	D0~D7	Data setup time Data hold time		30 10	_	ns
taccao tocac		Read access time Output disable time	C _L = 100pF	- 10	50 50	ns

6800-SYSTEM



Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	[Min.	Mæ.	Units
Carren Campa	CD	Address scup time Address hold time		20 40	هو.	ns
Tors		System cycle time		100		ns
(PARE)	WR1	Pulse width (read)		45	_	ns
(panaga	<u> </u>	Pulsa width (write)		45		ns
L-wes		Low pulse width	·	40	-	ns
10862 10862	D0-07	Data satup time Data held time		30 10		ns
Lycces loces		Read across time Output disable time	C _L = 100pF	10	50 50	ns .

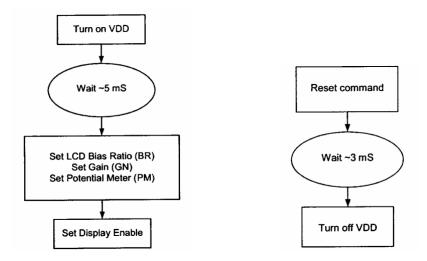
POWER ON/OFF SEQUENCE:

Power-ON Sequence:

UC1611 power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of System-Reset command after Power-ON-Reset. System programmer are only commands to UC1611. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands.

Power-OFF Sequence:

To prevent the charge stored in capacitors $C_{\text{BX+}}$, $C_{\text{BX-}}$, and C_{LCD} from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.



Reference Power-ON sequence

Reference Power-OFF sequence

9 QUALITY AND RELIABILITY

9.1 TEST CONDITIONS

Tests should be conducted under the following conditions:

Ambient temperature : $25 \pm 5^{\circ}$ C

Humidity : $60 \pm 25\%$ RH.

9.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

9.3 ACCEPTABLE QUALITY LEVEL

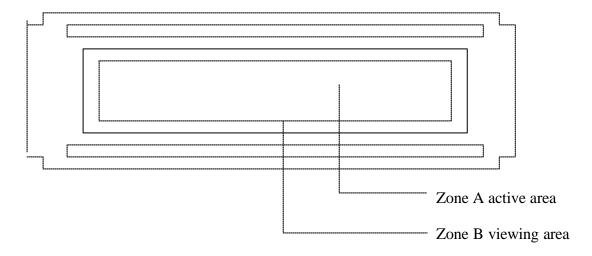
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

9.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under fluorescent light. The inspection area of LCD panel shall be within the range of following limits.

9.5 INSPECTION QUALITY CRITERIA

Item	Description	of de	fects		Class of	Acceptable level
					Defects	(%)
Function	Short circuit or Pattern cut				Major	0.65
Dimension	Deviation from	m drawi	ings		Major	1.5
Black spots	Ave . dia . D area A		A	area B	Minor	2.5
	D≤0.2	Γ	Disrega	ırd		
	0.2 <d≤0.3< td=""><td>3</td><td></td><td>4</td><td></td><td></td></d≤0.3<>	3		4		
	0.3 <d≤0.4< td=""><td>2</td><td></td><td>3</td><td></td><td></td></d≤0.4<>	2		3		
	0.4 <d< td=""><td>0</td><td></td><td>1</td><td></td><td></td></d<>	0		1		
Black lines	Width W, Length	L	A	В	Minor	2.5
	W≤0.03		disregard			
	0.03 <w≤0.05< td=""><td>3</td><td>4</td><td></td><td></td></w≤0.05<>		3	4		
	0.05 <w≤0.07 ,="" l≤3<="" td=""><td>1</td><td>1</td><td></td><td></td></w≤0.07>		1	1		
	See line criteria]	
Bubbles in	Average diameter D 0.2 < D < 0.5 mm			Minor	2.5	
polarizer	for $N = 4$, $D > 0.5$ for $N = 1$					
Color	Rainbow color or Newton ring.		•	Minor	2.5	
uniformity						
Glass	Obvious visible damage.				Minor	2.5
Scratches						
Contrast	See note 1			Minor	2.5	
ratio						
Response	See note 2			Minor	2.5	
time						
Viewing	See note 3			Minor	2.5	
angle						



9.6 RELIABILITY

	Test Conditions			
Test Item	Extended Temp. type			
High Temperature Operation	70±3°C, t=96 hrs			
Low Temperature Operation	-20±3°C , t=96 hrs			
High Temperature Storage	80±3°C, t=96 hrs	1,2		
Low Temperature Storage	-30±3°C, t=96 hrs	1,2		
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2		
Humidity Test	40 °C, Humidity 90%, 96 hrs	1,2		
Vibration Test (Packing)	Sweep frequency: 10 ~ 55 ~ 10 Hz/1min Amplitude: 0.75mm Test direction: X.Y.Z/3 axis Duration: 30min/each axis			

Note 1: Condensation of water is not permitted on the module.

Note 2: The module should be inspected after 1 hour storage in normal conditions (15-35°C, 45-65%RH).

Definitions of life end point:

Date: 2005/9/5

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

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10 HANDLING PRECAUTIONS

- (1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.
- (2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.
- (3) Under no circumstances should the position of the bezel tabs or their shape be modified.
- (4) Do not modify the display PCB in either shape or positioning of components.
- (5) Do not modify or move location of the zebra or heat seal connectors.
- (6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.
- (7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.
- (8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.
- (9) Prior to initial power up input signals should not be applied.
- (10) Protect the module against static electricity and observe appropriate anti-static precautions.

11 OUTLINE DIMENSION

