Freescale Semiconductor
Application Note

Document Number: AN3684
Rev. 1, 08/2012

i.MX25 Boot Options

by Multimedia and Applications Division
Freescale Semiconductor, Inc.
Austin, TX

This document describes the boot options for the i.MX25 device. For more in-depth details about how the boot mechanisms are implemented in the i.MX25 device, refer to the System Boot chapter of the *i.MX25 Multimedia Applications Processor Reference Manual* (MCIMX25RM).

Contents

1 Boot Options

Since the i.MX25 device is designed for a wide variety of applications, it is expected to operate in a large variety of configurations. In addition, the i.MX25 is a pin-reduced chip. Therefore I/O muxing is used aggressively and configuration restrictions are critical. To mitigate possible conflicts on bootable ports, the SD/MMC, CSPI, I^{2}C, or UART ports can all be chosen for boot. This adds great flexibility in system configuration.

1.1 Boot Type

The type of boot is chosen by the state of the Boot Mode pins (BOOT_MODE0 and BOOT_MODE1). These pins should be configured on the system board with pull-up or pull-down resistors to enter into the desired boot mode. The values of these pins are sampled during reset and after reset these pins can be configured to work as GPIOs. The value of the BOOT_MODE pins is stored in the CCM Status Register (RCSR) of the CCM. The possible boot type options are:

- Internal Boot (utilizing ROM code and HAB)
- FSL Test Mode (reserved for factory use)
- Eternal Boot (direct boot without much interaction from ROM and without HAB)
- USB/UART Bootloader (allows code to be downloaded via USB/UART ports)

Table 1 shows more details of the boot types.

Table 1. Boot Mode Summary

BMOD [1:0]	Boot Type	Boot Details
00	Internal Boot	Executes ROM code, which handles boot from following sources: • NOR Flash (via WEIM, 16-bit slow asynchronous mode for debugging purpose only) • OneNAND • CSPI (serial Flash, only on chip select #1) Or via I^{2}C • NAND Flash • SD/MMC (including high-capacity MoviNAND boot through MMC interface) • USB, UART boot (fallback option for all other modes when an error exception occurs)
01	FSL Test Mode	This mode is reserved for device testing and is intended for factory use only
10	External (Direct) Boot	Direct boot via the interface, independent of boot ROM code
11	USB/UART Boot Loader	Load and execute code via serial devices: • USB (Full-Speed, via integrated OTG PHY or external via the OTG interface[1]) • UART

[1] For typical application board usage, the internal PHY options is recommended. The use of external transceivers is not recommended, and would reduce availability of contacts.

1.2 Boot Pins and Fuses

Additional boot configuration is provided with either programmable e-fuses or by other pin values sampled during the reset sequence. The i.MX25 provides an option to sample the boot configuration with either the boot pins or the fuses. Selecting between the two options is controlled with the value of the GPIO_BT_SEL fuse (by default this fuse is left un-blown). In the case that GPIO_BT_SEL fuse is blown, all of the boot options are configured with the associated boot fuses as detailed in Table 2. When GPIO_BT_SEL is left un-blown (default), all of the boot options are determined by sampling the state of the dedicated boot pins during reset. For detailed information on the i.MX25 fuses refer to the *i.MX25 IC Identification Module (IIM) Fusebox Application Note Application Note (AN3682)*. Table 2 lists all of the associated boot pins along with their associated e-fuses.

Table 2. Fuses and Associated Contacts Used for Boot

BGA	Contact	Direction at Boot	eFuse Name	Details
W20	BMOD[1]	Input	N/A	Boot Mode Type selection (See Table 1)
V19	BMOD[0]			
U6	VSYNC	Input	BT_UART_SRC[2]	Selects which UART port is used as the bootable source
U7	HSYNC	Input	BT_UART_SRC[1]	
W3	LD15	Input	BT_UART_SRC[0]	
V4	LD14	Input	BT_EEPROM_CFG	Selects if EEPROM device uses DCD
W4, V5	LD[13:12]	Input	BT_SRC[1:0]	Chooses specific eSDHC, CSPI, or I^{2}C controller for booting
Y3	LD11	Input	BT_SPARE_SIZE	Specifies the size of spare bytes for 4 Kbyte page size NAND flash devices
Y4	LD10	Input	BT_MLC_SEL	Selects if NAND is SLC or MLC device
W5, V6	LD[9:8]	Input	BT_USB_SRC[1:0]	Selects if using internal/external OTG PHY
Y5, W6	LD[7:6]	Input	BT_BUS_WIDTH[1:0]	Selects bus width for selected interface
V7, Y6	LD[5:4]	Input	BT_PAGE_SIZE[1:0]	NAND Flash page size
U8, W7	LD[3:2]	Input	BT_MEM_TYPE[1:0]	Boot Memory Type
V8, Y7	LD[1:0]	Input	BT_MEM_CTL[1:0]	Boot Memory Control Type (memory device)
W2	PWM	Input	BT_LPB_FREQ[2]	Low Power Boot (LPB) ARM Core Frequency
V3	OE_ACD	Input	BT_LPB_FREQ[1]	
U5	LSCLK	Input	BT_LPB_FREQ[0]	
H20	CSI_PIXCLK	—	BT_RES3	Reserved
H19	CSI_HSYNC	—	BT_RES2	Reserved
G20	CSI_VSYNC	—	BT_RES1	Reserved
H18	CSI_MCLK	—	BT_RES0	Reserved
T20	VSTBY_ACK	Output	N/A	Pulse indication on finish of internal system reset, by visibility of hreset_b signal. After reset, this contact can be used for other purposes.

Table 3 contains a more detailed listing of all of the available boot options and configurations.

Table 3. Fuse Descriptions

Fuse/GPIO	Definition	Settings

BT_SRC[1:0]	Chooses boot port eSDHC, CSPI or I^{2}C.
	Has a corresponding GPIO pin.
		If BT_MEM_CTL[1:0] = 11 (Expansion card device) & BT_MEM_TYPE[1:0] = 00 (SD/MMC/MoviNAND/CE-ATA) then
		00 eSDHC1
		01 eSDHC2
		10 Reserved
		11 Reserved
		If BT_MEM_CTL[1:0] = 11 (Expansion card device) & BT_MEM_TYPE[1:0] = 10 (Serial ROM via I^{2}C) then
		00 I2C1
		01 I2C2
		10 I2C3
		11 Reserved
		If BT_MEM_CTL[1:0] = 11 (Expansion card device) & BT_MEM_TYPE[1:0] = 11 (Serial ROM via SPI) then
		00 CSPI1
		01 CSPI2
		10 CSPI3
		11 Reserved
		Other Reserved

BT_UART_SRC[2:0]	Choosing the specific UART controller for booting from.	000 UART1 001 UART2 010 UART3 011 UART4 100 UART5 Other Reserved
BT_MLC_SEL	SLC/MLC NAND device. Has a corresponding GPIO pin.	0 SLC NAND device 1 MLC NAND device
BT_SPARE_SIZE	Specifies the size of spare bytes for 4 Kbyte page size NAND Flash devices. Has a corresponding GPIO pin. **Note:** 512 byte page devices have 16 bytes spare area size, 2 Kbyte page devices have 64 bytes spare area size. **Note:** Assumes that the large spare area devices (218 byte) use 8-bit ECC. Otherwise, 4-bit ECC.	0 128 bytes spare (Samsung) (4-bit ECC) 1 218 bytes spare (Micron, Toshiba) (8-bit ECC)
BT_USB_SRC[1:0]	USB boot source selection. Has a corresponding GPIO pin.	00 USB OTG Internal PHY 01 USB OTG External ULPI PHY 10 Reserved 11 Reserved
BT_PAGE_SIZE[1:0]	NAND Flash Page Size. This field is used with conjunction with the BT_MEM_CTL[1:0] setting. Has a corresponding GPIO pin.	If BT_MEM_CTL = NAND Flash then 00 512 bytes 01 2 Kbytes 10 4 Kbytes 11 Reserved

Table 3. Fuse Descriptions (continued)

Fuse/GPIO	Definition	Settings
BT_EEPROM_CFG	Selects whether EEPROM device is used for load of configuration DCD data, prior to boot from other devices (not applicable when using EEPROM as boot device). Has a corresponding GPIO pin.	0 Use EEPROM DCD 1 Do not use EEPROM DCD
GPIO_BT_SEL	GPIO Boot Select. Determines if certain boot fuse values are controlled from GPIO pins or IIM	0 Boot mode configuration is taken from GPIOs 1 Boot mode configuration is taken from fuses
HAB_TYPE[2:0]	Security Type. This fuse comes pre-programmed to Engineering mode	001 Engineering (allows any code to be flashed and executed, even if it has no valid signature) 100 Security Disabled (For internal/testing use) Others Production (Security On)
BT_MEM_TYPE[1:0]	Boot Memory Type. Interpreted by boot ROM SW according to BT_MEM_CTL setting. Signals could also be interpreted by HW to alter delays and timing in support of direct boot. Has a corresponding GPIO pin.	If BT_MEM_CTL = WEIM then 00 NOR 01 Reserved 10 OneNand 11 Reserved If BT_MEM_CTL = NAND Flash 00 3 address cycles 01 4 address cycles 10 5 address cycles 11 Reserved If BT_MEM_CTL = Expansion Card Device 00 SD/MMC/MoviNAND/CE-ATA 01 Reserved 10 Serial ROM via I2C 11 Serial ROM via SPI
BT_BUS_WIDTH[1:0]	Bus width and muxed/unmuxed interface. Has a corresponding GPIO pin.	BT_MEM_CTL[1:0] = NAND Flash 00 8 bit bus 01 16 bit bus 10 Reserved 11 Reserved BT_MEM_CTL[1:0] = WEIM (NOR) 00 Reserved 01 16 bit address/data unmuxed interface 10 Reserved 11 Reserved BT_MEM_CTL[1:0] = Expansion Device (SPI) 00 2-Address word SPI device (16-bit) 01 3-Address word SPI device (24-bit) 10 Reserved 11 Reserved

Table 3. Fuse Descriptions (continued)

Fuse/GPIO	Definition	Settings
BT_MEM_CTL[1:0]	Boot Memory Control Type (memory device). Has a corresponding GPIO pin.	00 WEIM 01 NAND Flash 10 Reserved 11 Expansion Device (SD/MMC/MoviNAND/CE-ATA, I^2C, SPI) See BT_MEM_TYPE[1:0] settings for details
DIR_BT_DIS	Direct External Memory Boot Disable	0 Direct boot from external memory is allowed 1 Direct boot from external memory is not allowed

2 Interfacing with External Devices

In addition to setting the boot mode or configuring the boot fuses, users also need to be concerned about which IOMUX instance of each module is used for boot. Given that the i.MX25 uses an aggressive IOMUX scheme, some modules can be muxed out of more than one location to add flexibility. However, the boot ROM only utilizes a single location for each bootable module. The following sections provide more detail as to which pins are used for each module during boot.

2.1 Serial Flash or EEPROM Devices

The i.MX25 can be booted from a serial ROM device such as SPI Flash or an EEPROM device using CSPI or I^2C. When using the CSPI ports, only slave select 1 (SS1) of each port is bootable. Also if using I^2C, the interface is configured at speed of 389.6 Kbps. Table 4 lists the boot settings which must be set in order to boot from CSPI or I^2C ports.

Table 4. CSPI/I2C Boot Configuration

Fuse/GPIO	Setting	Comment
BMOD[1:0]	00	Must be set for internal boot for boot ROM to be used
BT_MEM_CTL[1:0]	11	Set to Expansion which includes I^2C and CSPI
BT_MEM_TYPE[1:0]	10 I^2C 11 CSPI	Boot with I^2C or CSPI
BT_SRC[1:0]	00 I2C1 01 I2C2 10 I2C3	If I^2C is selected with BT_MEM_TYPE
BT_SRC[1:0]	00 CSPI1 01 CSPI2 10 CSPI3	If CSPI is selected with BT_MEM_TYPE
BT_BUS_WIDTH[1:0]	Optional for SPI	00 2-Address word SPI device (16-bit) 01 3-Address word SPI device (24-bit)
BT_EEPROM_CFG	Optional for I^2C	0 Uses EEPROM DCD 1 Does not use EEPROM DCD

In addition to setting the boot mode pins, the pins to connect the external serial ROM device must be selected. Table 5 lists which IOMUX options and pins are used for each configuration when using CSPI or I^2C ports.

Table 5. CSPI/I2C Boot Device IOMUX

Interface	Function	Pad Name	BGA	ALT
CSPI1	SCLK	CSPI1_SCLK	U3	ALT0
	MOSI	CSPI1_MOSI	T4	ALT0
	MISO	CSPI1_MISO	W1	ALT0
	SS1	CSPI1_SS1	V2	ALT0
CSPI2	SCLK	SD1_DATA0	L20	ALT1
	MOSI	SD1_CMD	K20	ALT1
	MISO	SD1_CLK	M20	ALT1
	SS1	SD1_DATA3	J20	ALT1
CSPI3	SCLK	CS1_D4	F19	ALT7
	MOSI	CSI_D2	F18	ALT7
	MISO	CSI_D3	E19	ALT7
	SS1	CSI_D7	E18	ALT7
I2C1	SCL	I2C1_CLK	F17	ALT0
	SDA	I2C1_DAT	G17	ALT0
I2C2	SCL	FEC_RDATA1	M4	ALT1
	SDA	FEC_RX_DV	M3	ALT1
I2C3	SCL	GPIO_E	P18	ALT1
	SDA	CSPI1_SS1	V2	ALT1

2.2 SD/MMC Devices

The i.MX25 can be booted from SD/MMC cards through either of the two eSDHC interfaces. The eSDHC module supports high capacity SD, eSD (Embedded SD, version 2.1), MMC/eMMC (version 4.3), CE-ATA, and other managed NAND devices such as MoviNAND (which are all SD interfaces). Table 6 lists the boot settings which must be set in order to boot from eSDHC ports.

Table 6. SD/MMC Boot Configuration

Fuse/GPIO	Setting	Comment
BMOD[1:0]	00	Must be set for internal boot for boot ROM to be used
BT_MEM_CTL[1:0]	11	Set to Expansion which includes eSDHC
BT_MEM_TYPE[1:0]	00	Sets to eSDHC type device
BT_SRC[1:0]	00 eSDHC1 01 eSDHC2	Selects between eSDCH1 and eSDHC2 ports

In addition to setting the boot mode pins, the pins to connect the external SD/MMC device must be selected. Table 7 lists which IOMUX options and pins are used for each configuration when using the eSDHC1 or eSDCH2 ports. Although each eSDHC interface supports 8 bits of data, only a 1-bit interface is enabled. It is up to the users boot code to configure the interface to 4 or 8 bits.

Table 7. SD/MMC Boot Device IOMUX

Interface	Function	Pad Name	BGA	ALT
eSDHC1	CLK	SD1_CLK	M20	ALT0
	CMD	SD1_CMD	K20	ALT0
	DAT0	SD1_DATA0	L20	ALT0
	DAT1	SD1_DATA1	N20	ALT0
	DAT2	SD1_DATA2	M19	ALT0
	DAT3	SD1_DATA3	J20	ALT0
	DAT4	UART2_CTS	R2	ALT1
	DAT5	UART2_RTS	R3	ALT1
	DAT6	UART2_TXD	T1	ALT1
	DAT7	UART2_RXD	P4	ALT1
eSDCH2	CLK	CSI_D7	E18	ALT2
	CMD	CSI_D6	E20	ALT2
	DAT0	CSI_MCLK	H18	ALT2
	DAT1	CSI_VSYNC	G20	ALT2
	DAT2	CSI_HSYNC	H19	ALT2
	DAT3	CSI_PIXCLK	H20	ALT2
	DAT4	CSI_D2	F18	ALT2
	DAT5	CSI_D3	E19	ALT2
	DAT6	CSI_D4	F19	ALT2
	DAT7	CSI_D5	G18	ALT2

2.3 UART Interface

The i.MX25 can be booted from any of the five UART ports on the i.MX25. When in serial boot mode, the ROM polls both the UART and USB status registers for about 90 seconds. The port (USB or UART) which shows activity first is selected as the active interface. If there is no activity within the pre-defined loop time, the ROM resets the i.MX25 using the WDOG. In a valid boot session with USB or UART the WDOG is serviced periodically to prevent unwanted reset of the i.MX25. Additionally, if communication between the host and iMX25 hangs for more than 90 seconds or the i.MX25 goes into an endless loop, the WDOG expires and reset the device. When using UART, the interface is configured with baud rate of 115.2 Kbps, parity disabled, 1 stop bit, and 8-bit data length. Table 8 lists the boot settings which must be set in order to boot from the UART ports

Table 8. UART Boot Configuration

Fuse/GPIO	Setting	Comment
BMOD[1:0]	11	Must be set for serial boot via UART or USB
BT_UART_SRC[2:0]	000 UART1 001 UART2 010 UART3 011 UART4 100 UART5	Select which UART controller to boot from

In addition to setting the boot mode pins, the pins to connect the external UART device must be selected. Table 9 lists which IOMUX option and pins are used for each configuration when using the UART ports.

Table 9. UART Boot Device IOMUX

Interface	Function	Pad Name	BGA	ALT
UART1	CTS	UART1_CTS	T2	ALT0
	DCD	KPP_ROW2	P3	ALT4
	DSR	KPP_ROW1	R1	ALT4
	DTR	KPP_ROW0	N4	ALT4
	RI	KPP_ROW3	P2	ALT4
	RTS	UART1_RTS	T3	ALT0
	RXD	UART1_RXD	U2	ALT0
	TXD	UART1_TXD	U1	ALT0
UART2	CTS	UART2_CTS	R2	ALT0
	DCD	UART1_RTS	T3	ALT3
	DSR	UART1_TXD	U1	ALT3
	DTR	UART1_RXD	U2	ALT3
	RI	UART1_CTS	T2	ALT3
	RTS	UART2_RTS	R3	ALT0
	RXD	UART2_RXD	P4	ALT0
	TXD	UART2_TXD	T1	ALT0
UART3	CTS	KPP_ROW3	P2	ALT1
	RTS	KPP_ROW2	P3	ALT1
	RXD	KPP_ROW0	N4	ALT1
	TXD	KPP_ROW1	R1	ALT1
UART4	CTS	KPP_COL3	N1	ALT1
	RTS	KPP_COL2	N2	ALT1
	RXD	KPP_COL0	P1	ALT1
	TXD	KPP_COL1	N3	ALT1

Table 9. UART Boot Device IOMUX (continued)

Interface	Function	Pad Name	BGA	ALT
UART5	CTS	CSI_D5	G18	ALT1
	RTS	CSI_D4	F19	ALT1
	RXD	CSI_D2	F18	ALT1
	TXD	CSI_D3	E19	ALT1

2.4 USB Interface

The i.MX25 device can be booted from the OTG USB port. When in serial boot mode, the ROM polls both UART and USB status registers for about 90 seconds. The port (USB or UART) which shows activity first is selected as the active interface. If there is no activity within the pre-defined loop time, the ROM resets the i.MX25 using the WDOG. In a valid boot session with USB or UART the WDOG is serviced periodically to prevent unwanted reset of the i.MX25. Additionally, if communication between the host and i.MX25 hangs for more than 90 seconds or the i.MX25 goes into an endless loop, the WDOG expires and reset the device. When using the USB OTG interface, the internal HS OTG PHY or an external PHY using the OTG ULPI interface can be selected. Table 10 lists the boot settings which must be set in order to boot from the USB OTG port.

Table 10. USB Boot Configuration

Fuse/GPIO	Setting	Comment
BMOD[1:0]	11	Must be set for serial boot via UART or USB
BT_USB_SRC[1:0]	00 Internal PHY 01 External PHY	Select OTG Internal HS PHY or select to use an External ULPI PHY

In addition to setting the boot mode pins, the pins to connect the external USB device must be selected. Table 11 lists which IOMUX option and pins are used for each configuration when using the USB OTG port.

Table 11. USB Boot Device IOMUX

Interface	Function	Pad Name	BGA	ALT
USB OTG External ULPI PHY	USBOTG_OC	GPIO_B	N18	ALT2
	USBOTG_DATA0	CSI_D2	F18	ALT6
	USBOTG_DATA1	CSI_D3	E19	ALT6
	USBOTG_DATA2	CSI_D4	F19	ALT6
	USBOTG_DATA3	CSI_D5	G18	ALT6
	USBOTG_DATA4	CSI_D6	E20	ALT6
	USBOTG_DATA5	CSI_D7	E18	ALT6
	USBOTG_DATA6	CSI_D8	G19	ALT6
	USBOTG_DATA7	CSI_D9	F20	ALT6
	USBOTG_DIR	CSI_MCLK	H18	ALT6
	USBOTG_STP	CSI_VSYNC	G20	ALT6
	USBOTG_NXT	CSI_HSYNC	H19	ALT6
	USBOTG_CLK	CSI_PIXCLK	H20	ALT6
USB OTG Internal HS PHY	VBUS	USBPHY1_VBUS	K17	Dedicated
	DP	USBPHY1_DP	L18	Dedicated
	DM	USBPHY1_DM	K18	Dedicated
	UID	USBPHY1_UID	J18	Dedicated
	RREF	USBPHY1_RREF	L17	Dedicated

2.5 MLC/SLC NAND Devices

The i.MX25 can be booted from NAND Flash through the NFC interface. There is support for SLC and MLC (512 bytes 4-bit ECC, 2 Kbyte 4-bit ECC and 4 Kbyte page sizes 4/8-bit ECC). Table 12 lists the boot settings which must be set in order to boot from NAND ports.

Table 12. NAND Boot Configuration

Fuse/GPIO	Setting	Comment
BMOD[1:0]	00 Internal 10 External	Select internal boot which uses secure boot (requires an image header) or external for direct boot from NAND
BT_MEM_CTL[1:0]	01	Set to boot from NAND Flash
BT_MEM_TYPE[1:0]	00 3 address cycles 01 4 address cycles 10 5 address cycles	Sets the number of address cycles needed for the NAND
BT_MLC_SEL	0 SLC 1 MLC	Select SLC or MLC NAND

Table 12. NAND Boot Configuration (continued)

Fuse/GPIO	Setting	Comment
BT_SPARE_SIZE	0 128 bytes 1 218 bytes	0 128 bytes spare (Samsung) (4-bit ECC) 1 218 bytes spare (Micron, Toshiba) (8-bit ECC)
BT_PAGE_SIZE[1:0]	00 512 bytes 01 2 Kbytes 10 4 Kbytes	Set the NAND Flash page size
BT_BUS_WIDTH[1:0]	00 8-bit bus 01 16-bit bus	Set the NAND bus width

In addition to setting the boot mode pins, the pins to connect the external NAND device must be selected. Table 13 lists which IOMUX option and pins are used for the NFC interface.

Table 13. NAND Boot Device IOMUX

Interface	Function	Pad Name	BGA	ALT
NFC	NANDF_CE0	NF_CE0	D2	ALT0
	NANDF_CLE	NFCLE	E4	ALT0
	NANDF_ALE	NFALE	F4	ALT0
	NANDF_WE_B	NFWE_B	G4	ALT0
	NANDF_RE_B	NFRE_B	C1	ALT0
	NANDF_WP_B	NFWP_B	H4	ALT0
	NANDF_RB	NFRB	C2	ALT0
	EIM_D[15:0]	D[15:0]	—	ALT0

2.6 NOR Flash Devices

The i.MX25 can be booted from NOR Flash or OneNAND through the WEIM interface. Table 14 lists the boot settings which must be set in order to boot from the WEIM interface.

Table 14. NAND Boot Configuration

Fuse/GPIO	Setting	Comment
BMOD[1:0]	00 Internal 10 External	Select internal boot which uses secure boot or external for direct boot from WEIM
BT_MEM_CTL[1:0]	00	Set to boot from WEIM Interface
BT_MEM_TYPE[1:0]	00 NOR 10 OneNand	Set to boot with NOR or OneNand device
BT_BUS_WIDTH[1:0]	00 Reserved 01 16-bit unmuxed	00 Reserved 01 16 bit address/data unmuxed interface

In addition to setting the boot mode pins, the pins to connect the external NOR WEIM device must be selected. Since WEIM is the default option of the i.MX25, the ROM code does not need to modify any IOMUX settings and the boot is carried out on the EIM port.

3 Revision History

Table 15 provides a revision history for this application note.

Table 15. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	08/2012	• In Table 3, "Fuse Descriptions," on page 4, replaced “16 bit address/data muxed interface” with “Reserved.” • In Table 14, "NAND Boot Configuration," on page 12, replaced “16 bit address/data muxed interface” with “Reserved,” and “16-bit muxed” with “Reserved.”
0	06/2009	Initial release.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM is the registered trademark of ARM Limited.

© 2012 Freescale Semiconductor, Inc.

Document Number: AN3684
Rev. 1
08/2012