A Low-Jitter 1.8-kV 100-ps Rise-Time 50-kHz Repetition-Rate Pulsed-Power Generator

ARTICLE *in* IEEE TRANSACTIONS ON PLASMA SCIENCE · OCTOBER 2009

Impact Factor: 1.1 · DOI: 10.1109/TPS.2009.2025377 · Source: IEEE Xplore

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A Low-Jitter 1.8-kV 100-ps Rise-Time 50-kHz Repetition-Rate Pulsed-Power Generator

Lev M. Merensky, Alexei F. Kardo-Sysoev, Alexander N. Flerov, Alex Pokryvailo, Doron Shmilovitz, *Member, IEEE*, and Amit S. Kesar, *Member, IEEE*

***Abstract*—A 1.8-kV 100-ps rise-time pulsed-power generator operating at a repetition frequency of 50 kHz is presented. The generator consists of three compression stages. In the first stage, a power MOSFET produces high voltage by breaking an inductor current. In the second stage, a 3-kV drift-step-recovery diode cuts the reverse current rapidly to create a 1-ns rise-time pulse. In the last stage, a silicon-avalanche shaper is used as a fast 100-ps closing switch. Experimental investigation showed that, by optimizing the generator operating point, the shot-to-shot jitter can be reduced to less than 13 ps. The theoretical model of the pulse-forming circuit is presented.**

***Index Terms*—Drift-step-recovery diode (DSRD), pulse generation, pulse shaping circuits, silicon-avalanche shaper (SAS), subnanosecond, ultrawideband radiation.**

I. Introduction

NANOSECOND and subnanosecond pulsed-power generators are important for a variety of applications, such as ultrawideband radars [1], laser driving [2], material characterization [3], and immensely wide spectrum of plasma chemistry applications. The latter include, but are not limited to, material processing and surface modification, air and water purification, and medical treatment [4]–[7]. The deployment of all these technologies is heavily dependent on the availability of suitable pulse generators. The latter are typically characterized by output voltage, rise time, pulsewidth, repetition rate, jitter, and long-term drift of the aforementioned parameters. Efficiency, peak and average power, reliability, size, and cost are critical for wide use in most of the applications.

Several technologies exist for the generation of subnanosecond pulses. All of them rely on fast high-power switching. Either opening switches (OSs) or closing switches (CSs) and/or their combinations are used. Gas-discharge devices, nonlinear passive components, e.g., saturable inductors and nonlinear transmission lines, and solid-state switches depict the spectrum of available technologies [8]. High-pressure spark gap (SG) is a gas-discharge device of choice for the generation of very high power of nano- and subnanosecond pulses. An SG-based generator was reported by Baum *et al.* to produce a 1-MV output to an 85-Ω load at a repetition rate of 600 Hz. The rise time was 100 ps [9]. Radan generators [10] exemplify SG use as a mature technology. The shortcomings of SG-based pulsers are limited life and repetition rate, and high jitter. The first makes the specific cost of pulse generation, i.e., cost per pulse, prohibitively high for most applications except scientific research.

Magnetic compressors are widely used for the generation of nanosecond pulses in laser [11] and pollution control [6]; they become uneconomical at subnanosecond pulsewidths.

High-power pulses with subnanosecond rise time can be generated by compressing nanosecond-long pulses in a nonlinear transmission line. A 90-kV generator delivering 850-ps rise-time pulses to a 50-Ω load by a ferrite-loaded transmission line was reported by Brooker *et al.* [12]. This technology also is limited to relatively long pulse generation.

Semiconductors can be used as fast OS and CS. For cutting-edge applications, nanosecond-long pulses are generated by inductive storage systems employing OS with consecutive compression to subnanosecond width by CS. Probably, the most exhaustive treatment on subject, in English, is given in [13]. The experimental pulsers demonstrate very good performance and reliability, overcoming SG limitations, but have very high cost $\$/W$. The latter is expected to drop with wider deployment of the technology. Hereunder, we give several examples of the developed switches and systems.

The existence of nanosecond scale step-recovery effect in a commercial SRD rectifying diode is described in [14] and [15] and recently reported by Han *et al.* [16]. The output was a positive impulse with an amplitude of 2.3 V and a pulsewidth of 115 ps.

A 400-kV 8–10-ns pulsewidth 4-ns rise-time, at a repetition frequency of 300 Hz, generator having a semiconductor OS (SOS) was reported by Bushlyakov *et al.* [17]. The SOS was based on a stack of tens/hundreds of layers of silicon p^+-p-n-n^+ junctions. The opening of the switch is based on a step-recovery effect discovered by Grekhov and Mesyats [8], [18].

Drift-step-recovery diodes (DSRDs) can be used for nanosecond scale pulsing at high average power. A 2.7-kV

Manuscript received March 3, 2009; revised May 20, 2009. First published August 11, 2009; current version published September 10, 2009.

L. M. Merensky and A. S. Kesar are with the Propulsion Physics Laboratory, Soreq Nuclear Research Center, Yavne 81800, Israel (e-mail: levme@soreq.gov.il; kesar@soreq.gov.il).

A. F. Kardo-Sysoev is with the Power Semiconductor Devices Laboratory, Ioffe Physical Technical Institute, 194021 St. Petersburg, Russia (e-mail: alx@helen.ioffe.rssi.ru).

A. N. Flerov is with the Radioelectronic Systems Control Department, Baltic State Technical University "VOENMEKH" D. F. Ustinov, 198005 St. Petersburg, Russia (e-mail: t5709363@mail.wplus.net).

A. Pokryvailo is with the Propulsion Physics Laboratory, Soreq Nuclear Research Center, Yavne 81800, Israel, and also with Spellman High Voltage Electronics Corporation, Hauppauge, NY 11788 USA (e-mail: alex@soreq.gov.il).

D. Shmilovitz is with the School of Electrical Engineering, Faculty of Engineering, Tel Aviv University, Tel Aviv 69978, Israel (e-mail: shmilo@eng.tau.ac.il).

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Digital Object Identifier 10.1109/TPS.2009.2025377

TABLE I
TECHNOLOGY COMPARISON

Technology	V-peak [kV]	T-rise [ns]	PRF [kHz]	$\frac{V_P \cdot PRF}{T_R}$
SAS [current work]	1.8	0.1	50	900
DSRD [19]	2.7	0.7	600	2314
SOS [17]	400	10	0.3	12
Ferrites [12]	10	0.06	0.1	17
Spark-gaps [9]	770*	0.18	0.2	856

*Equivalent voltage to a 50 Ω load.

0.7-ns rise time at a repetition frequency of 600 kHz was reported by Kardo-Sysoev *et al.* [19]. The output jitter was less than 30 ps. A typical DSRD structure is made by layers of p^+-p-n-n^+ junctions [20]. The DSRD has an opening switching effect which is more efficient than that of the SOS. In space charge region of DSRD, there are no minority carriers during fast voltage restoration; thus, it differs by the faster rise time, far lower energy losses, and high repetition rate.

Subnanosecond pulses can be produced by fast-ionization breakdown effect [21]. This effect occurs when a reverse pulse is applied to an avalanche diode. Therefore, the diode behaves as a fast CS. These diodes are used as the last sharpening stage and therefore called silicon-avalanche shaper (SAS). The physics of the diode, including some design considerations, was presented by Kardo-Sysoev [13] and Focia *et al.* [22].

A pulse generator based on solid-state devices was reported by Efanov *et al.* [23]. An amplitude of 80 kV, a 0.9-ns rise time, a pulse repetition frequency (PRF) of 1 kHz, and jitter less than 100 ps were reported.

Another compact pulse generator was reported by Zazoulin *et al.* Applying both DSRD and silicon-avalanche diode produced 1-kV peak, 80-ps rise time, 50-kHz PRF, and less then 30-ps jitter [24].

Recent advances showed that SiC- and GaAs-based diodes [25] were implemented to produce subnanosecond pulses by the avalanche effect. These technologies have the potential advantage of higher peak power, compared to the regular silicon. However, the overall performance in terms of average power, energy efficiency, reliability, lifetime, and time position stability (e.g., jitter and drift), as well as simplicity and cost of pulsed-power generators based on such devices, has not yet proved to be better than that of silicon devices.

Various applications require a high product of voltage rate of rise dV/dt times the PRF; it can be used as a figure of merit. A comparison of this quantity for a few of the technologies described earlier is shown in Table I. As shown in the table, the DSRD and SG showed the highest $(dV/dt) \times PRF$ rates. However, solid-state devices, in general, have a lifetime of several years in continuous operation, whereas high-voltage SGs have a lifetime on the order of 10^7 shots and therefore may work continuously for several hours at a rate of hundreds of hertz [26].

High-stability generators, in terms of low drift and jitter, are important for ultrawideband applications, such as radars and communication. The drift is typically caused by warm-up over seconds to hours of operation. The shot-to-shot jitter in a semiconductor-based pulsed-power generator could be a function of the ripple of the input supply voltages, the characteristics of the circuit elements (such as diodes, transistors, transformers, etc.), and the circuit layout.

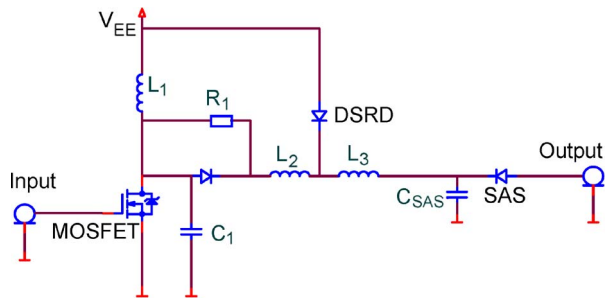

Fig. 1. PFC.

Although jitter as low as 30 ps in high-voltage (> 1 kV) semiconductor-based pulsed-power generators was reported previously, jitter analysis and optimization in terms of the overall circuit have not been reported yet.

In this paper, we analyze the jitter caused by the input supply voltage ripple. The jitter was correlated by averaging the shot-to-shot signal while sweeping the related supply voltage.

The objectives of this paper are to report the pulsed-power generator that was presented by Merensky *et al.* [27] and, with respect to this reference, demonstrate that circuit optimization can yield an increased output power by more than 40% and improved shot-to-shot stability by more than 30%.

II. PFC ANALYSIS

The pulse-forming circuit (PFC) is shown in Fig. 1. It uses three compression stages. The first stage uses a power MOSFET that produces high voltage by breaking the current through inductor L_1.

The second stage employs a DSRD that cuts the reverse current and creates a 1-ns rise-time pulse. The SAS and its peaking capacitor $C_{\rm SAS}$ are used in the last stage as a fast 100-ps CS.

Initially, the MOSFET switch is open, and no current (besides a negligible leakage current) flows through the circuit. The capacitors C_1 and $C_{\rm SAS}$ are charged to $V_{\rm EE}$.

Next, the MOSFET is closed, resulting in a current increase through L_1

$$I_1 = \frac{V_{\rm EE}}{R_{\rm DS}^{\rm on}} \left(1 - e^{-\frac{t}{\tau_1}}\right) \tag{1}$$

where $R_{\rm DS}^{\rm on}$ is the MOSFET ON-state resistance, the time constant $\tau_1 = L_1/R_{\rm DS}^{\rm on}$, and $V_{\rm EE}$ is the supply voltage.

Assuming that the DSRD forward resistance is negligible, we obtain the current through L_2 as

$$I_2 = \frac{V_{\rm EE}}{R_{\rm DS}^{\rm on} + R_1} \left(1 - e^{-\frac{t}{\tau_2}}\right) \tag{2}$$

where the time constant $\tau_2 = L_2/(R_{\rm DS}^{\rm on} + R_1)$.

The coil L_1 will be charged to a current determined by the duration the MOSFET is on. During this stage, the current that

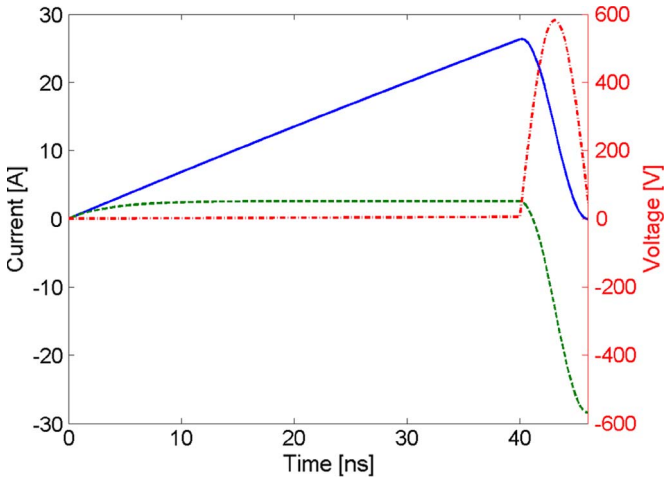

Fig. 2. Solution of (1)–(3), for (solid) I_1, (dashed) I_2, and dash–dotted V_C (with respect to the right axis).

flows through L_2 and R_1 is used as the DSRD forward pumping current.

In the next stage, the MOSFET is switched off, resulting in L_1 being discharged to C_1 and then through the diode and L_2 to reverse the DSRD current, therefore removing the charge that was accumulated previously in the DSRD. This stage can be described by

$$\begin{pmatrix} \dot{V_C} \\ I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} 0 & 1/C & 1/C \\ -1/L_1 & 0 & 0 \\ -1/L_2 & 0 & -R_{\text{tune}}/L_2 \end{pmatrix} \cdot \begin{pmatrix} V_C \\ I_1 \\ I_2 \end{pmatrix} + \begin{pmatrix} 0 \\ V_{\text{ee}}/L_1 \\ V_{\text{ee}}/L_2 \end{pmatrix} \tag{3}$$

where R_{tune} represents the equivalent of R_1 and the diode in the forward or reverse directions, I_1 and I_2 are the currents through the inductors L_1 and L_2, respectively, and V_c is the voltage over C_1.

When the accumulated charge is fully removed, the DSRD rapidly breaks the current, resulting in a pulse voltage charging C_{SAS}.

In the last stage, as the voltage of C_{SAS} exceeds the SAS avalanche voltage, the SAS closes, forming a fast rise-time pulse.

As an example for the first two stages, we take $L_1 = 75$ nH, $L_2 = 65$ nH, $R_1 = 20\ \Omega$, $C_1 = 100$ pF, and $V_{\text{EE}} = 52$ V. The MOSFET is switched on for 40 ns. Fig. 2 shows the solution of (1)–(3). As shown in the figure, during the "ON" state, L_1 is charged to 25 A, L_2 is charged to 2.5 A, and C_1 is discharged to zero.

The forward charge accumulated on the DSRD is assumed to be proportional to

$$Q_{\text{DSRD}} \propto \int I_2\, dt. \tag{4}$$

Due to high lifetime of carriers, the loss of charge due to recombination (< 1–2%) is negligible for efficiency, but may play a role in small thermal drift.

When the MOSFET is switched off, the voltage on C_1 reaches 600 V, and then, C_1 discharges through the diode and

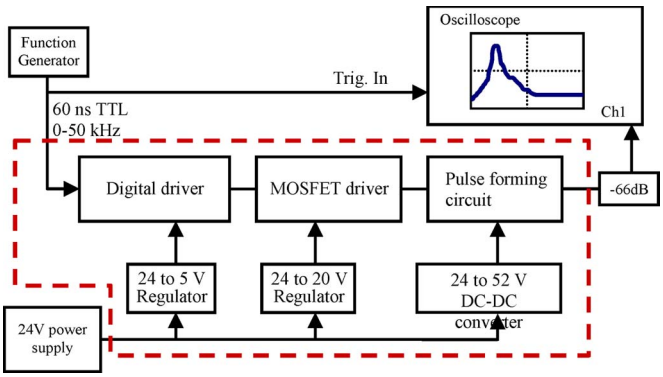

Fig. 3. Experimental setup.

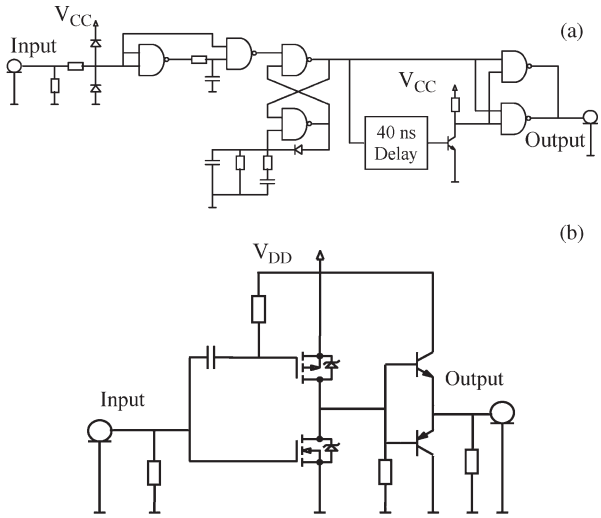

Fig. 4. Schematics of the (a) digital driver and (b) MOSFET driver.

L_2 to the DSRD in the reverse direction. The DSRD will break the reverse current when $Q_{\text{DSRD}} = 0$, i.e.,

$$\int I_F\, dt = \int I_R\, dt \tag{5}$$

where I_F and I_R are the DSRD currents in the forward and reverse directions, respectively.

III. Experimental Setup

The experimental setup is shown in Fig. 3. The generator is marked by the dashed line. The generator consisted of three parts: the digital driver, the MOSFET driver, and the PFC. The schematics of the digital and MOSFET drivers are shown in Fig. 4(a) and (b), respectively.

The digital and MOSFET drivers were fed by voltage regulators in which their nominal values were 5 and 20 V, respectively. The PFC was fed by a converter with a nominal value of 52 V. The 5-, 20-, and 52-V supplies are referred as V_{CC}, V_{DD}, and V_{EE}, respectively, through this paper. The generator was optimized by varying these supplies around their nominal values. All of these units were fed by an external 24-V power supply.

The digital driver was triggered by an external function generator. The PFC output was connected to a Textronix TDS820

TABLE II
GENERATOR NOMINAL PARAMETERS

Digital driver supply voltage, V_{CC}	5 V
MOSFET driver supply voltage, V_{DD}	20V
PFC supply voltage, V_{EE}	52 V
First compression stage inductor, L_1	75 nH
Second compression stage inductor, L_2	65 nH
Third compression stage inductor, L_3	45 nH
Tuning resistor, R_1	20 Ω
Capacitor, C_1	100 pF

oscilloscope via a 26-dB high-voltage attenuator (BARTH Electronics 2237-HFNFP) connected to an additional 40-dB low-voltage attenuator. Therefore, the generator load made by these attenuators is 50 Ω. In order to record the delay between the generator input and its output, the function generator output was split to trigger the scope externally. In order to preserve the fast rise time, the length of measurement cables was kept minimum, which is less than 1 m. We note that, in these measurements, only the relative delay, with respect to a constant time reference of about a few tens of nanoseconds, was recorded.

As shown in Fig. 1, the SAS is connected to the PFC output. However, in the cases we wanted to measure the DSRD output directly, the last compression stage, i.e., the SAS, was bypassed by a 1-μF capacitor.

A thermocouple, located 10-mm above the DSRD in the PFC block, was used to measure the ambient temperature. The ambient temperature was controlled externally.

Table II summarizes the generator nominal supply voltage levels and the PFC passive component values. Unless otherwise specified, these values are used throughout this paper.

IV. EXPERIMENTAL RESULTS

The pulse generator output is shown in Fig. 5, where Fig. 5(a) shows the DSRD output (when a 1-μF capacitor was used to bypass the SAS) and Fig. 5(b) shows the SAS output (without a bypass capacitor). As shown in these figures, the DSRD and SAS output voltages are 1.1 and 1.5 kV, respectively, and the corresponding pulse rise times (from 10% to 90%) were 1.0 and 0.07 ns, respectively, not counting the prepulse. The PRF was 50 kHz. The dc to pulse efficiency was 22.9%, whereas the output average power was 1.26 W.

The thin upper trace in Fig. 5(b) shows an average of 1000 pulses. The thick lower trace is the envelope of 1000 pulses. The envelope horizontal thickness is 20 ps, which indicates the measured peak-to-peak jitter.

In order to measure the SAS closing behavior, the voltage across the SAS capacitor C_{SAS} during the operation was measured by an ∼1:1700 attenuation probe. The probe was made of a 1-kΩ low-inductance resistor connected to C_{SAS}, and it was followed by a resistor network for further attenuation. This measurement is shown in Fig. 5(c). As can be seen in this figure, a signal of 1-ns rise time is rapidly cut with a fall time of about 150 ps.

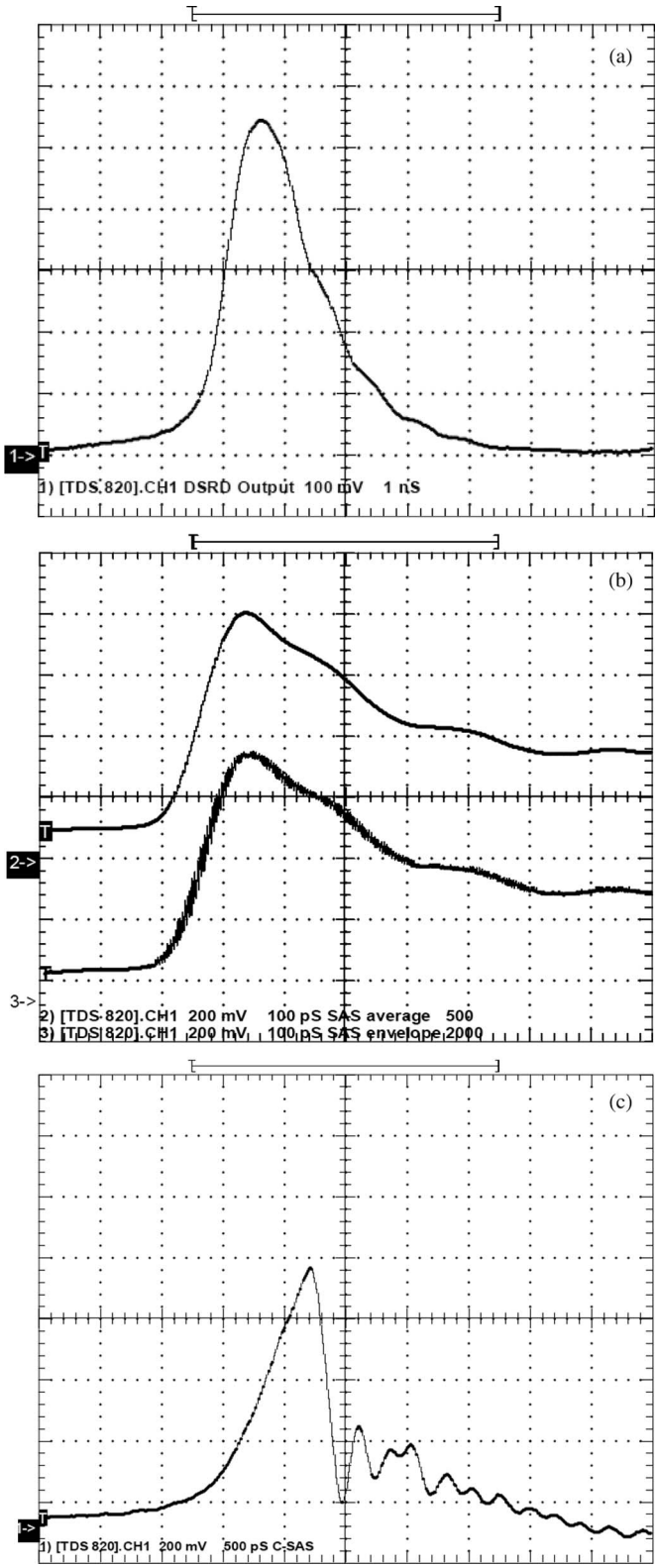

Fig. 5. (a) DSRD and (b) SAS output traces and (c) the voltage across C_{SAS}. The SAS output is displayed for two capturing modes of the oscilloscope: (Upper trace) Average and (lower trace) envelope modes. The vertical scale is 200 V/div in (a), 400 V/div in (b), and 340 V/div in (c).

A. Parametric Sweep

In order to optimize the charge through the DSRD, the tuning resistor R_1 was varied. Fig. 6 shows the DSRD output with respect to several R_1 values of 10, 16.5, 20, 25, 30, and 41 Ω. A maximum output voltage of 1.1 kV was reached for $R_1 = 16.5$ Ω. It is shown that a rise time of 1 ns was common to almost all cases of R_1.

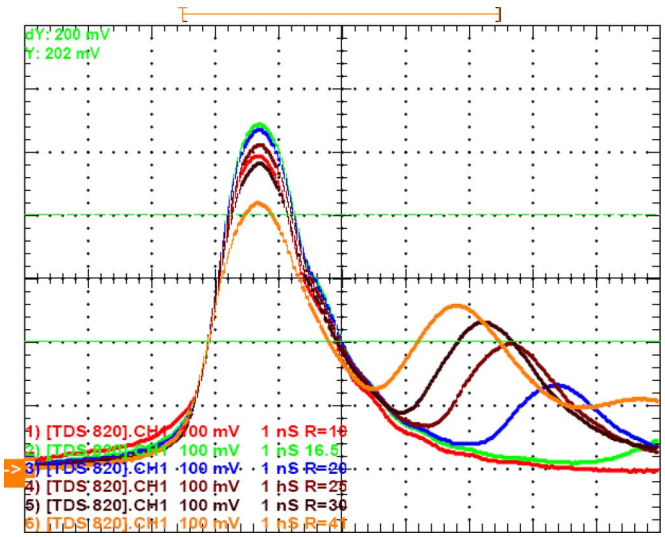

Fig. 6. DSRD output for various R_1 values. The vertical scale is 200 V/div.

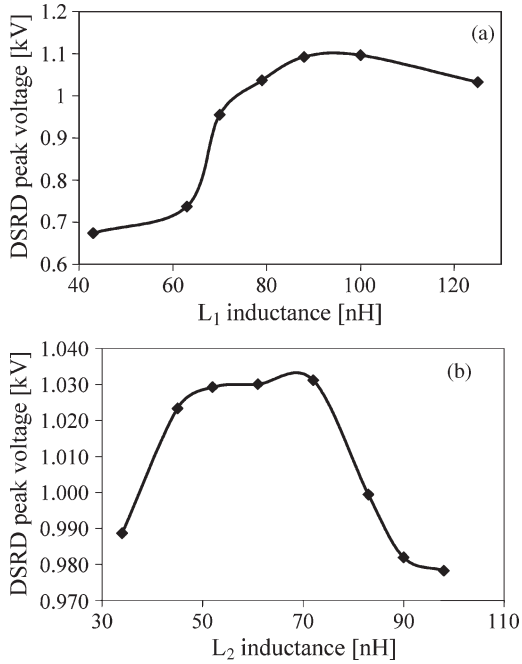

Fig. 7. DSRD output versus the inductance values of (a) L_1, where L_2 was constant (65 nH), and (b) L_2, where L_1 was constant (75 nH).

The optimization of the DSRD output voltage by varying L_1 and L_2 is shown in Fig. 7(a) and (b), respectively. The resistor R_1 was tuned for each inductor value. In Fig. 7(a), where L_2 was kept constant (65 nH), the optimal value for L_1 was 90 nH. In Fig. 7(b), where L_1 was kept constant (75 nH), the optimal value for L_2 was 70 nH. It is shown that the circuit was almost insensitive to L_2 between 50 and 75 nH.

B. Supply Voltage Sweep

Fig. 8(a) shows the (squares) DSRD and (diamonds) SAS peak output voltages with respect to the PFC supply $V_{\rm EE}$. It can be seen that the optimal values of 1.15 kV for the DSRD and 1.8 kV for the SAS were obtained when $V_{\rm EE}$ was 52 V.

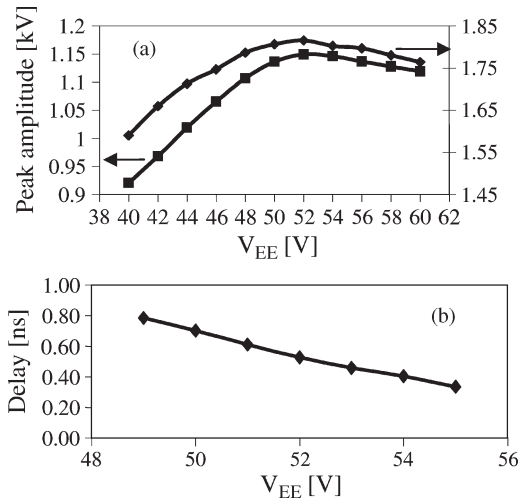

Fig. 8. (a) (Right axis) SAS and (left axis) DSRD peak outputs versus $V_{\rm EE}$. (b) Relative delay versus $V_{\rm EE}$.

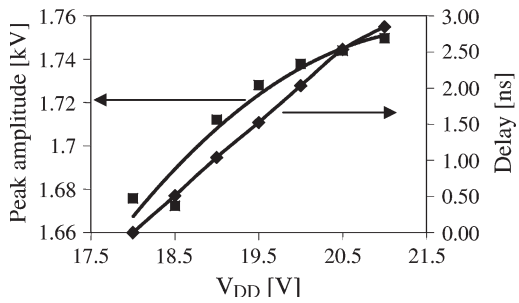

Fig. 9. SAS peak output and relative delay versus $V_{\rm DD}$.

It is also noted that the SAS output voltage correlated to the DSRD output voltage. The SAS rise time was 100 ps during the entire scan.

The relative delay between the generator input and its output versus $V_{\rm EE}$ is shown in Fig. 8(b). It is shown that a sensitivity of 75 ps/V was obtained for $V_{\rm EE}$ variation.

Fig. 9 shows the (squares) generator peak amplitude and (diamonds) relative delay versus the MOSFET driver supply voltage $V_{\rm DD}$. The solid lines between the points are their trend lines, respectively. A maximum output voltage of 1.75 kV was obtained when $V_{\rm DD}$ was 21 V. The SAS rise time was 100 ps during the entire scan. It is shown that a delay sensitivity of 1 ns/V was obtained for the variations in this supply voltage.

Fig. 10 shows the (squares) generator peak amplitude and (diamonds) relative delay, and their respective trend lines, versus the digital driver supply voltage $V_{\rm CC}$. A maximum output voltage of 1.8 kV was obtained when $V_{\rm CC}$ was 6 V. Also here, the SAS rise time was 100 ps during the entire scan.

The delay sensitivity ranged from -5.5 ns/V at 4 V and up to 30 ns/V when $V_{\rm CC}$ was 6 V. The sensitivity at the 5-V nominal supply voltage was 3 ns/V and was zero at 5.3 V.

The peak-to-peak ripple of $V_{\rm CC}$, $V_{\rm DD}$, and $V_{\rm EE}$ supplies was measured separately. The ripple values were 2.5, 2.8, and 5 mV, respectively.

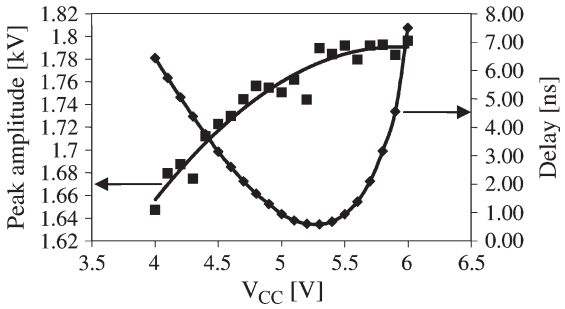

Fig. 10. SAS peak output and relative delay versus $V_{\rm CC}$.

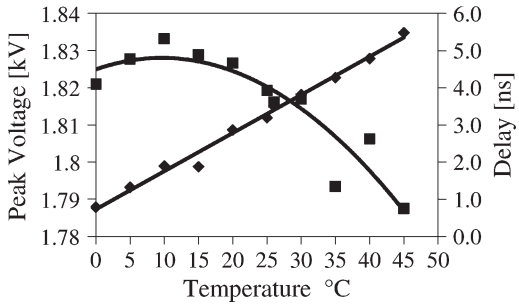

Fig. 11. SAS peak output and relative delay versus temperature.

C. Temperature Sweep

Fig. 11 shows the (squares) generator peak amplitude and (diamonds) relative delay, and their respective trend lines, versus the ambient temperature. The output peaked to 1.83 kV at 10 °C. The delay sensitivity was 0.1 ns/°C.

V. Discussion

A 1.8-kV 100-ps rise-time 50-kHz PRF pulse generator was presented. The analysis of the PFC first two stages was derived. The analysis assumed linear components and ideal switches, and therefore, it provides a basic understanding of the circuit behavior. However, this model is insufficient for optimization, since it does not take switching losses and performance limitations into account. These limitations relate to transient nonlinear voltage drops on power MOSFET, DSRD, and SAS in their "ON" states, as well as small residual charges of free carriers existing in the space charge region of DSRD during voltage restoration.

The parametric optimization of R_1, L_1, and L_2 was shown in Figs. 6 and 7. In Fig. 6, the DSRD rise time was almost insensitive to its output. The reason for that is related to the DSRD internal structure which determines its switching speed. Voltage restoration turnoff time $T_{\rm off}$ could be estimated as

$$T_{\rm off} \sim \frac{W_{\rm SCR}}{V_n} \tag{6}$$

where $W_{\rm SCR}$ is the space charge region width, and V_n is the velocity of majority carriers. The majority carriers are electrons in the n-type regions and holes in the p-type region. These carriers determine the velocity of the space charge region widening.

Voltage drop $V_{\rm SCR}$ in the space charge region is

$$V_{\rm SCR} \sim \frac{qN_dW_{\rm SCR}^2}{2\varepsilon} \tag{7}$$

where N_d is the doping level, q is the electron charge, and ε is the dielectric permittivity.

At low DSRD current density J_d

$$V_n \sim \frac{J_d}{qN_d}. \tag{8}$$

The current density reaches the maximum saturated value $J_{\rm ds}$, at $V_{\rm ns} = 10^7$ cm/s, as determined by

$$J_{\rm ds} = qN_dV_{\rm ns}. \tag{9}$$

Equation (9) determines the maximal current that the DSRD can break, which should correspond to the maximum DSRD breakdown voltage.

Between the linear (8) and saturated (9) cases, the dependence of the velocity on the current density could be approximated as

$$V_n \sim \sqrt{J_d}. \tag{10}$$

Equations (6), (7), and (10) show that, in this intermediate case, the practical turnoff time does not depend on the current and respectively on the voltage.

The time constant in the first compression stage $\tau_1 = L_1/R_{\rm DS}^{\rm on} = 375$ ns is much higher than the charging time $T_{\rm CH} = 40$ ns. Therefore, the inductor's accumulated energy would be $(V_{\rm EE} \cdot T_{\rm CH})^2/2L_1$. This implies that large inductors are undesirable. In Fig. 7, it is shown that inductors larger than the optimal value will result in amplitude reduction, as expected. However, decreasing the inductance resulted also in an output power decrease. This can be explained by the following: 1) relative increase of the MOSFET losses, which are related to transient and to its on-resistance value $(R_{\rm DS}^{\rm on})$ and 2) current limitations on the DSRD implied by (9).

The capacitance $C_{\rm SAS}$ of the sharpening capacitor is a compromise of two factors. First, it should be large enough to provide long discharge time determined pulsewidth $\tau_p \approx R_d \cdot C_{\rm SAS}$, where $R_d \approx R_l + R_{\rm SAS}$, and $R_{\rm SAS}$ is the internal resistance of the SAS in the "ON" state. In our case, $R_d \approx 50$ to 100 Ω. To get good energy efficiency, τ_p should be longer than the turn-on time of SAS, i.e., ∼100 ps. That gives estimation for $C_{\rm SAS} \geq 1$ pF. Second, the voltage rise time on the SAS and $C_{\rm SAS}$ is also determined by the DSRD turnoff time and a half period of L_3 and $C_{\rm SAS}$, which limits $C_{\rm SAS}$ to be ≤ 2 pF. The final value of $C_{\rm SAS}$ is determined experimentally to get the maximum of output voltage. The stray capacitance of mounting should be included in $C_{\rm SAS}$ as well.

The static breakdown voltage of SAS is around 1.2 kV. Due to fast applied voltage rise time, it is possible to overrun a static breakdown voltage of up to nearly two times before delayed overstressed ionization starts. It is the delayed ionization, which provides very fast switching of the SAS. To get good switching under delayed ionization, voltage rise time should be comparable or even shorter than the time of flight of carriers across the

TABLE III
DELAY NOISE ANALYSIS

DC supply	Nominal voltage [V]	Ripple [mV]	Delay sensitivity [ns/V]	Delay noise [ps]
V_{CC}	5	2.5	3	7.5
V_{DD}	20	2.8	1	2.8
V_{EE}	52	5	0.075	0.4

width of low doped region of the diode. The width is around 100 μm, and the time of flight is around 1 ns.

The voltage sweep resulted in an increased output of up to 1.8 kV. This corresponds to a peak power of 64.8 kW.

A 20-ps jitter was measured in Fig. 5(b). The jitter can be considered as a delay noise. In Table III, we analyze the contribution of the ripple from the three power supplies. Each power supply ripple was multiplied by the delay sensitivity (derived from Figs. 8–10) to produce the delay noise at the nominal operating voltage. We see that the total delay noise sums up to 10.7 ps. An additional measurement jitter of 4.3 ps can be attributed to the oscilloscope accuracy, as stated in its specifications. This explains 15 ps of jitter, with respect to the 20-ps measured value. We believe that the other 5 ps might be due to other measurement errors, noise jitter of the components, shot-to-shot memory effect (for example, in the capacitors), and interference induced into cables from external radio sources.

Jitter is usually calculated as sums of root mean squares of its components, because it is considered as a statistical behavior. However, in our case, the oscilloscope measured the envelope of the jitter. Therefore, the calculations were made by adding the contributing components in order to determine the limits of this envelope.

This analysis shows, however, that the major source of error was the V_{CC} ripple. As shown in Fig. 10, this ripple can be minimized by choosing 5.3 V as the operating voltage. Therefore, we conclude that the jitter could be reduced to less than 13 ps. This number is on the order of our current measurement capability since the other supply-related jitter plus the scope jitter and the 5-ps unidentified jitter sums up to 12.5 ps.

To conclude, a pulse generator with high peak (64.8 kW) and average (1.26 W) power has been introduced. The combination of high power and low jitter makes the technology attractive for a variety of UWB applications.

ACKNOWLEDGMENT

The authors would like to thank E. Shviro and M. Ogranovich for their technical support to this paper.

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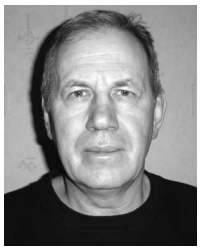
Lev M. Merensky was born in Kishinev, Moldova, in 1977. He received the B.Sc. degree in electrical engineering from Tel Aviv University, Tel Aviv, Israel, in 2004. The presented work is part of his thesis for the M.Sc. degree at Tel Aviv University.

Since 2004, he has been with the Propulsion Physics Laboratory, Soreq Nuclear Research Center, Yavne, Israel.

Alexei F. Kardo-Sysoev was born in Leningrad (now St. Petersburg), Russia, in 1941. He received the B.S. degree in semiconductor physics from Saint Petersburg Electrotechnical University, St. Petersburg, in 1964 and the Ph.D. degree from the Ioffe Physical Technical Institute (PTI) of Academy of Science, St. Petersburg, in 1973 on the basis of his work in the field of the physics of fast power semiconductor switches.

In 1967, he joined the Ioffe PTI of Academy of Science, where he started R&D work in the field of the physics of fast power semiconductor switches. In the late 1970s, he discovered two effects "superfast reversible breakdown" and "superfast voltage restoration" in high-voltage p-n junctions. These effects have been applied to other semiconductor structures, making possible the development of superfast power semiconductor devices. In 1987, he became a Professor. He was appointed to head the Physics Laboratory (in 1987). He is currently with the Power Semiconductor Devices Laboratory, Ioffe PTI. His main areas of interest shifted to ultrawideband electromagnetic, communication, radar, and electronic jamming. He has authored or coauthored more than 150 scientific and technical papers and inventions.

Prof. Kardo-Sysoev was the recipient of the State Prize in Physics in 1987.



Alexander N. Flerov was born in Leningrad (now St. Petersburg), Russia, in 1951. He received the B.S. degree in radio electronics design from the Baltic State Technical University "VOENMEKH" D. F. Ustinov, St. Petersburg, in 1974.

He is currently an Associate Professor with the Radioelectronic Systems Control Department, Baltic State Technical University "VOENMEKH" D. F. Ustinov. His main fields of interest are control systems of antennae arrays, design of fast power nano- and subnanosecond pulsers, research and design of synchronizing systems for such pulsers, and pulsed antennae arrays. In the late 1990s, he designed the first active-feedback loop-controlled pulsed array. He has authored or coauthored more than 50 scientific and technical papers and inventions.

Alex Pokryvailo was born in Vyborg, Russia. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Leningrad Polytechnic Institute, St. Petersburg, Russia, in 1975 and 1987, respectively.

He is currently with Spellman High Voltage Electronics Corporation, Hauppauge, NY, on sabbatical leave from the Propulsion Physics Laboratory, Soreq Nuclear Research Center, Yavne, Israel. His experience relates to pulsed power, with emphasis on high-current opening and closing switches and magnetic design, fast diagnostics, design of HV high-power switch-mode power supplies, corona discharges, study of switching arcs, design of SF_6-insulated switch gear, research in the area of interaction of flames with electromagnetic fields, etc. He published over 100 papers, two textbooks (in Hebrew), and more than 20 patents pertaining to HV technology.

Doron Shmilovitz (M'98) was born in Romania in 1963. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Tel Aviv University, Tel Aviv, Israel, in 1986, 1993, and 1997, respectively.

During 1986–1990, he worked in R&D for the IAF, where he developed programmable electronic loads. During 1997–1999, he was a Postdoctorate Fellow with the New York Polytechnic University, Brooklyn, where he worked on unity power factor bidirectional onboard chargers for electric vehicles. Since 2000, he has been with the School of Electrical Engineering, Faculty of Engineering, Tel Aviv University, where he established the state-of-the-art power electronics and power quality research laboratory. His research interests include switched-mode converters, topology, dynamics and control, power quality and power conversion for alternative energy sources, and general circuit theory.

Amit S. Kesar (M'06) received the B.Sc. and Ph.D. degrees in electrical engineering from Tel Aviv University, Tel Aviv, Israel, in 1997 and 2002, respectively.

From 2002 to 2005, he was first a Postdoctoral Associate and then a Research Scientist with the Plasma Science and Fusion Center, Massachusetts Institute of Technology (MIT), Cambridge. At MIT, he conducted experimental and theoretical research on high-intensity electron-beam sources and coherent radiation sources. Since 2005, he has been a Research Scientist with the Propulsion Physics Laboratory, Soreq Nuclear Research Center (Soreq NRC), Yavne, Israel. Since 2006, he has been the Head of the Pulsed Power Group, Soreq NRC, leading research projects on a variety of pulsed power sources and their applications. His research interests include fast opening and closing switches, diagnostics of highly relativistic bunches, high-gradient particle acceleration methods, and millimeter-wave sources.