Department of Electrical and Electronic Engineering
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EE 2.3: Semiconductor Modelling in SPICE
Course homepage:
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SPICE Diode and BJT models

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1. Summary of last lecture

We saw that:

- SPICE deals with current sources not voltage sources
- Gaussian elimination is used to solve the equations
- Newton-Raphson is used to solve circuits with non-linear elements
- There is a convergence aid, called GMIN, which aids convergence of the Newton-Raphson algorithm by eliminating divide by zero errors

2. Today’s lecture

We will look at:

- SPICE large signal diode model
- DC and large signal transient models
- SPICE large signal BJT model
- DC and large signal transient models
- The parameters of these models and how they relate to the device physics you know

3. The SPICE Diode Model

3.1. DC Model

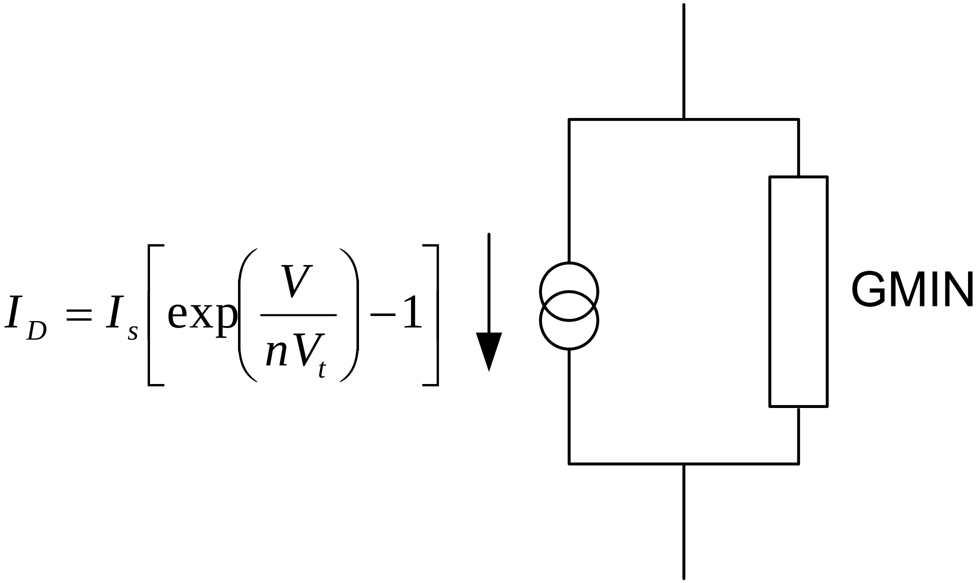
The simple DC equation you know is the well known Shockley equation, that is:

$$I_D = I_s \left[\exp\left(\frac{V}{V_t} \right) - 1 \right]$$

Where I_S is the diode's reverse saturation current, V is the applied voltage bias, V_t is the thermal voltage (equal to kT/q which is about 25mV at room temperature) and I_D is the current through the device.

The simple DC model used in SPICE is very similar to the Shockley equation, with the addition of a parameter *n*, and a convergence aid of a the GMIN parallel conductance (see **Error! Reference source not found.**). The basic static diode model equation is thus:

$$I_D = I_s\left[\exp\left(\frac{V}{nV_t}\right) - 1\right] + V_D GMIN$$



- The parameter *n* is an ideality factor for the diode, known as the emission coefficient.
- It has a SPICE parameter called N (all SPICE parameters are given in capitals).
- N=1 in a good diode.
- Rises above 1 if there is significant recombination of carriers in the depletion layer.
- n tends to be closer to 1 under high forward bias and more than 1 under small bias voltages because the depletion layer gets thinner as the forward bias is increased.
- The other SPICE parameter from this basic equation is IS.

- In order to allow faster simulations than this equation would provide, a simple approximation is made in moderate reverse bias.

- When V_D<-5nV_t, SPICE uses the assumption that the leakage current through the p-n junction is simply equal to $I_{S,}$ rather than actually calculating the exact exponential term.

- This means that under these conditions the total current through the complete static SPICE diode model is:

$$I_D = -I_s + V_D GMIN$$

What is a physical meaning of I_S?

It is the limit of the current in the diode under high reverse bias. If the diode did not exhibit breakdown, the maximum reverse current that you could get through the diode with an infinite reverse bias would be *Is*.

- You can now appreciate why the GMIN component is vital in achieving convergence in the region of V_D<-5nV_t, because the conductance would otherwise be zero in that region.

- SPICE includes breakdown in the model, and is modelled as an exponential breakdown past a certain voltage, the breakdown voltage, specified as SPICE parameter BV, with current at breakdown of IBV.

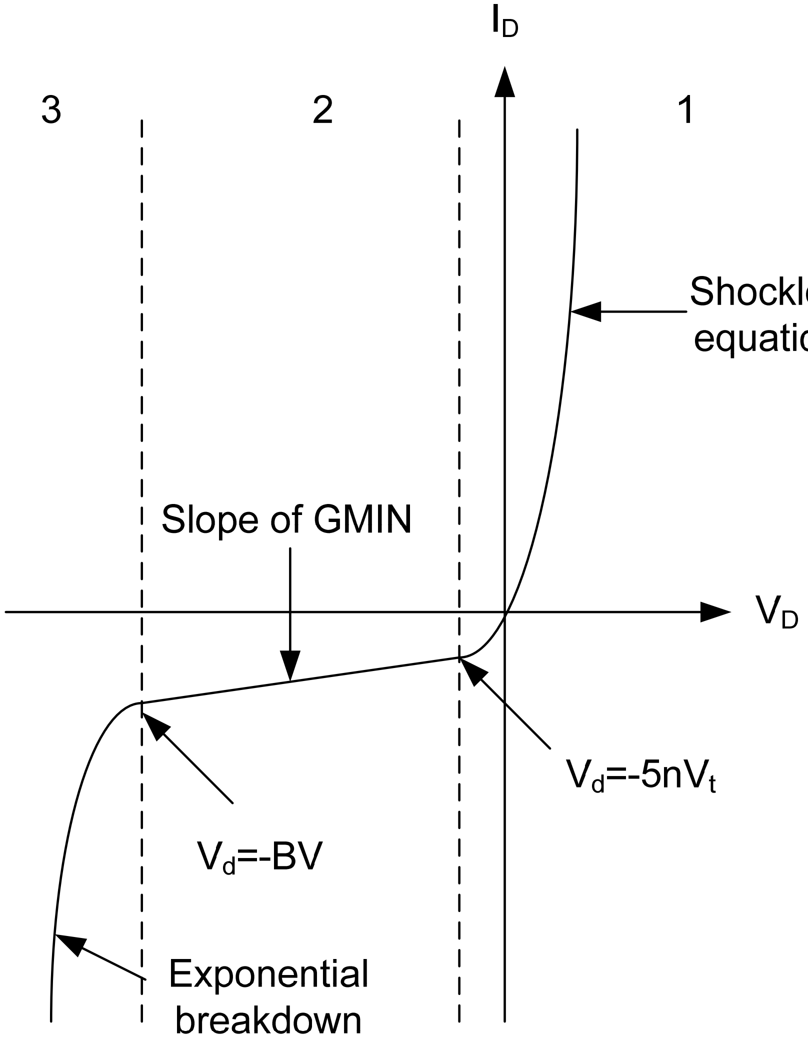
The current after breakdown is modelled with the following equation:

$$I_D = -I_S \left[\exp - \left(\frac{BV + V_D}{V_t} \right) - 1 + \frac{BV}{Vt} \right]$$

- When the diode voltage is equal to BV, the diode current as specified by this equation is $-I_s BV/V_t$.

- It is therefore important that the SPICE parameter IBV (current at breakdown) is somewhat near to $-I_s BV/V_t$ to allow continuity in the DC characteristic.

DC curve implemented by SPICE



SPICE model DC diode characteristic split into 3 regions

Finally, a series resistance is added to the diode model to simulate the resistances of the connecting wires and the ohmic contact resistances, giving us the following simple static model:

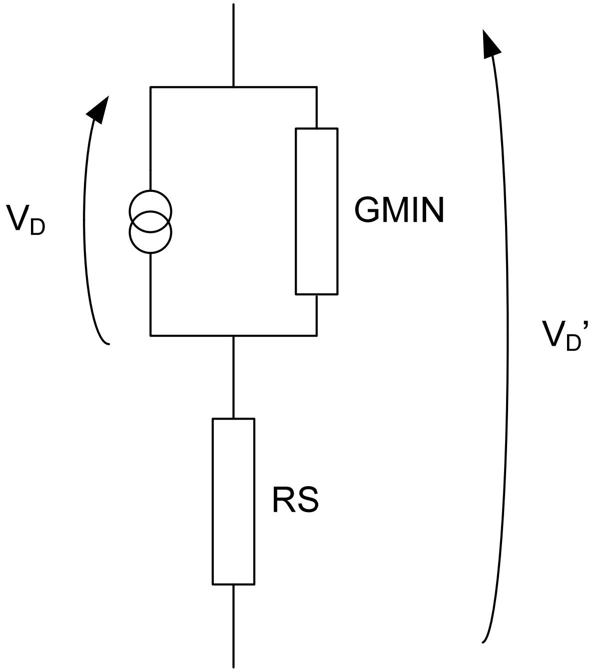


Figure 1 Static DC diode model

And so, $V_D' = V_D + I_D RS$

In summary, the important SPICE parameters (given in capitals and corresponding to the physical parameters in *italics*) for setting the DC characteristic are:

IS (I_s)	The reverse saturation current
RS (R_s)	The Ohmic resistance of the contacts and bond wires
N (n)	The emission (or ideality) coefficient
BV	The breakdown voltage (inputted to SPICE as a positive number)
IBV	The current at reverse breakdown (inputted to SPICE as a positive number)

With these parameters you can specify the complete static diode characteristic.

3.1.1. Limitation of the Diode Model

- The SPICE diode model does not include the effects of *high level injection*.
- When deriving the Shockley equation you previously made the assumption that the diode was operating in low-level injection.
- In power semiconductors, this is not necessarily the case because they operate in what is known as *high level injection*.
- The SPICE model does not include this effect (because it was originally designed to be used with low power signal devices).

3.2. Large Signal Transient Model

- We now need to add dynamic effects to the diode model
- Add capacitances to the model

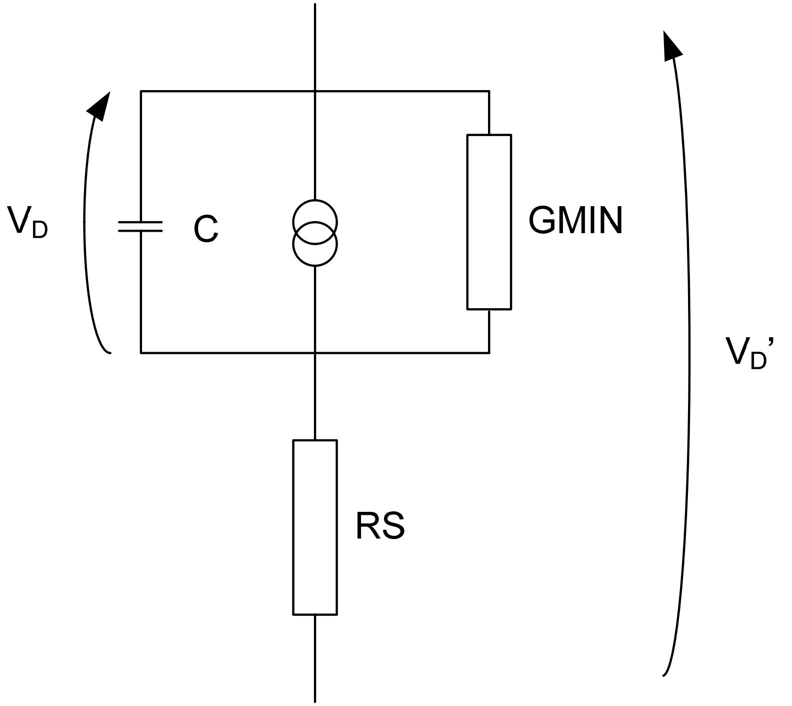


Figure 2 SPICE Large signal transient model

Capacitance Calculation

Two contributions to capacitance between the terminals of a diode.

- diffusion capacitance
- depletion (or junction) capacitance.

Depletion (junction) capacitance, dominant in reverse bias, is given by:

$$C_j = \varepsilon A \sqrt{\frac{e N_A N_D}{2\varepsilon (N_A + N_D)(V_0 - V)}}$$

How did we calculate this capacitance?

Why does it increase as V increases?

SPICE implements essentially the same equation, but written slightly differently…

Rewrite this:

$$C_j = A\sqrt{\frac{\varepsilon e N_A N_D V_0}{2(N_A + N_D)}}\sqrt{\frac{1}{1-\frac{V}{V_0}}}$$

Which can again be written as:

$$C_j = \frac{C_j(0)}{\sqrt{1-\frac{V}{V_0}}}$$

This is the equation SPICE uses to calculate the depletion capacitance, where C_j(o) is the junction capacitance at zero applied bias and is the SPICE parameter CJ0.

What is the physical meaning of CJ0?

- The diffusion capacitance, C_d, is dominant in forward bias.
- capacitance associated with the stored minority carriers in neutral regions.

$$C_d = \frac{e}{kT} I\tau$$

SPICE uses the same equation, but adds in the diode ideality coefficient:

$$C_d = \frac{e}{nkT} I\tau$$

What is the relation of C_d with device voltage?

Intuitively, why is this?

Dynamic SPICE diode model parameters

CJ0 ($C_j(0)$)	Zero bias junction capacitance
TT (τ)	The transit time
VJ (V_0)	Built in junction voltage

- You now know the most important parameters to allow you to specify a custom diode model in SPICE.

- There are a few more parameters which exist that we are not going to look at as we have covered the important ones.

3.3. A Note on the SPICE Area Parameter “A” and Device Scaling

SPICE has an area parameter called A, which can be used to scale any pn junction. The parameters IS, CJ0, RS and IBV are all proportional to device area.

Two choices when entering these parameters:

- Enter as parameters per unit cross sectional area and set the A parameter to the correct cross sectional area of the device

- Enter them as the values for a specific device and set the Area value to 1. Then if you want to have multiple devices in parallel, setting A=3 means your device will behave as if there were three devices in parallel.

4. The SPICE BJT model

4.1. DC model

We will use npn transistor for this analysis.

SPICE uses the **Ebers-Moll** transistor model

You know the following BJT equations:

$$I_c = I_s\left[\exp\left(\frac{V_{be}}{V_t}\right) - 1\right]$$

$$I_c = \beta I_b \qquad\qquad I_e = I_b + I_c$$

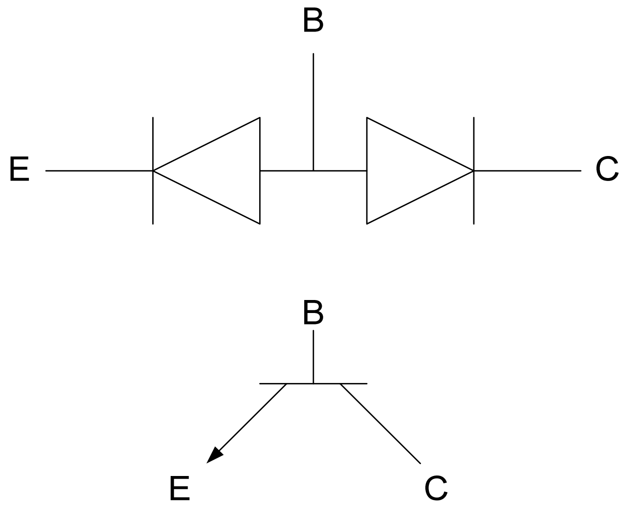
Why does SPICE not just use these equations?

There are 2 versions of the Ebers-Moll model:

- Injection model
- Transport model

SPICE uses transport model – but injection easier to understand

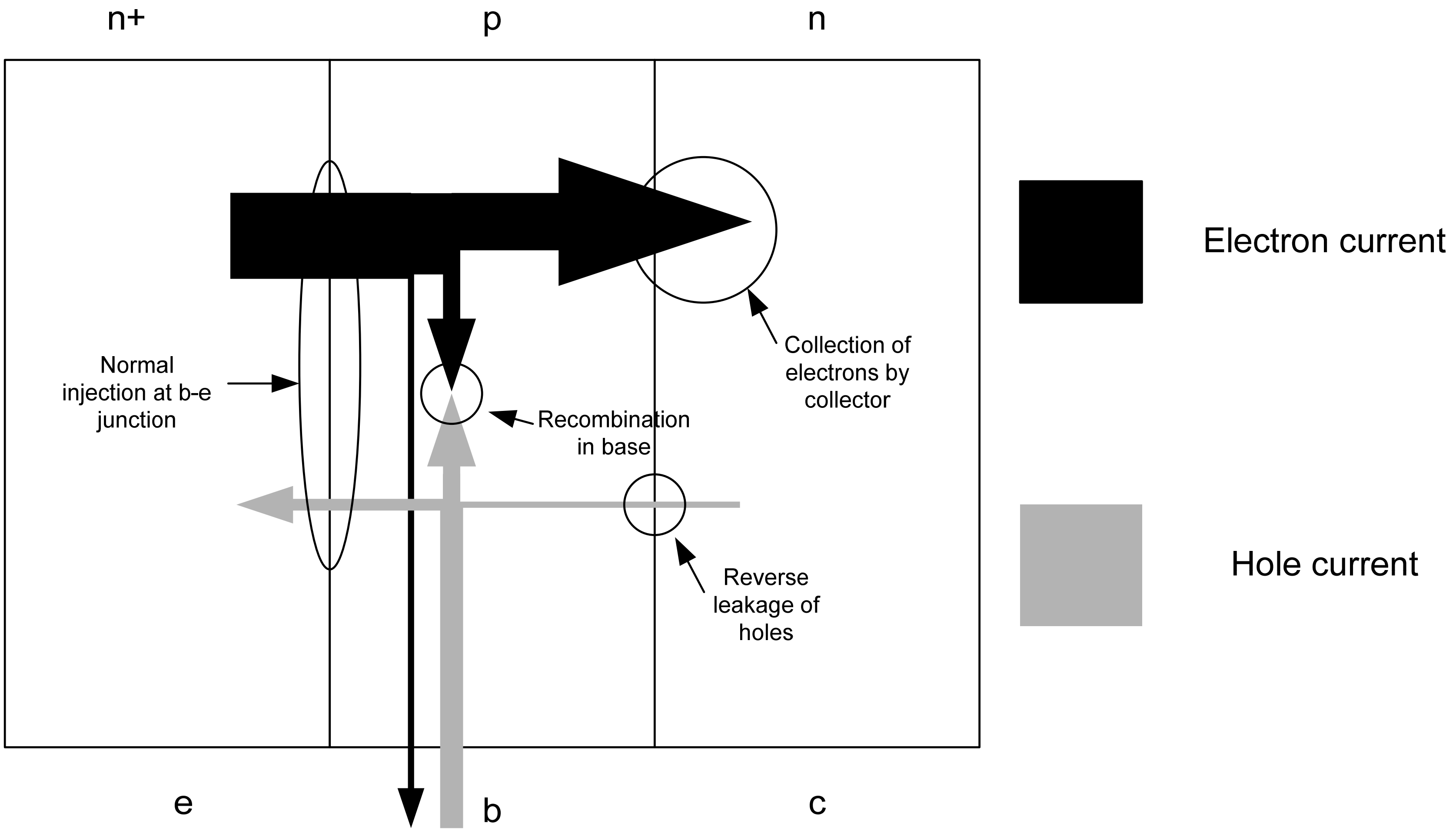
You are aware that a BJT is physically built as two back to back diodes, as shown below:



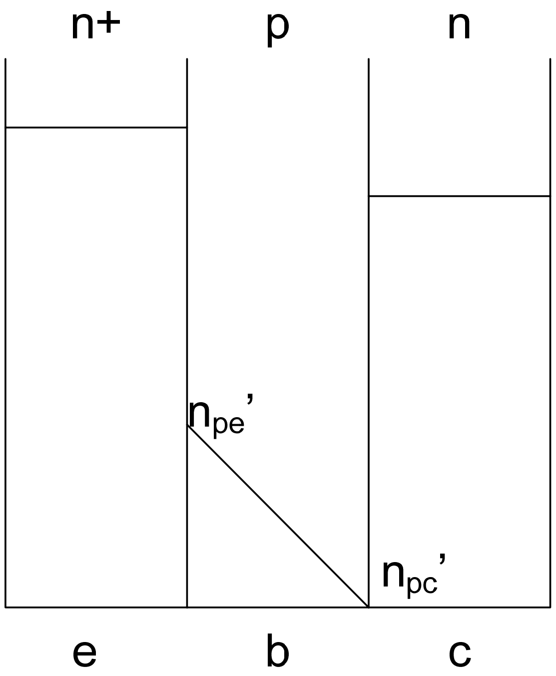
Why does it not behave like two back to back diodes?

The BJT in Active Mode

Refresh our memory of the carrier flows in an npn BJT in active mode….

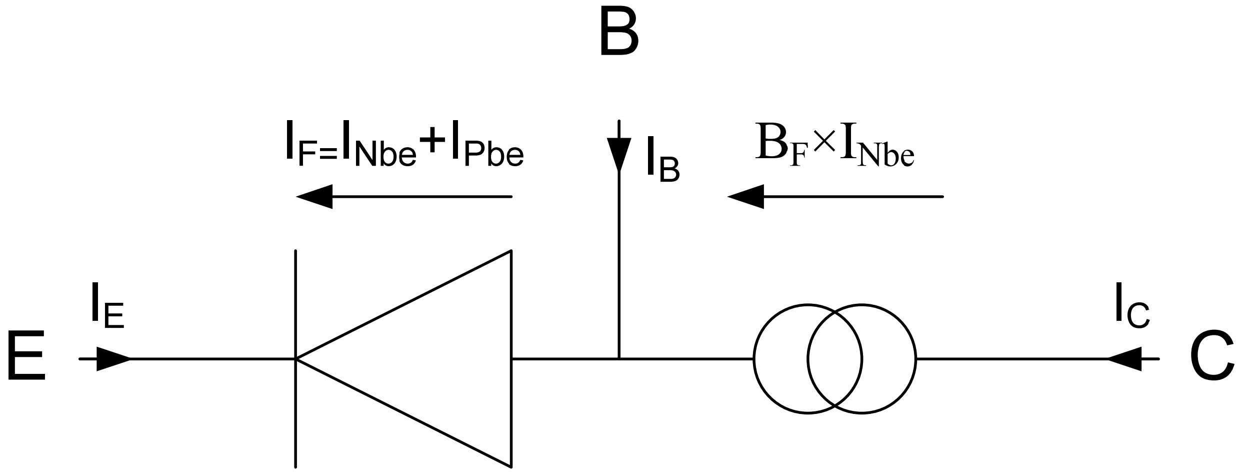


The collector current is proportional to the concentration gradient of minority carriers in the base….



- In active mode, n_{pc}' is approximately zero - the collector-base junction is reverse biased.
- emitter current is controlled completely by the base emitter voltage as this alters the concentration gradient by altering n_{pe}'.

Can think of the BJT operating in this way as the following large signal equivalent circuit.



Where:

I_{Nbe} – electron current through the base emitter junction
I_{Pbe} – hole current through the base emitter junction
I_F – the total current through the base-emitter junction ($I_{Nbe} + I_{Pbe}$)
B_F – fraction of electrons injected by the emitter which are collected by the collector

(Neglect hole contribution to collector current)

We will now define some terms which will allow us to simplify the diagram a little:

- **The forward emitter injection efficiency, γ_F:**

Fraction of emitter current which comes from emission of electrons (for npn) or holes (for pnp) from the emitter. For an npn transistor, it is therefore:

$$\gamma_F = \frac{I_{Nbe}}{I_e} = \frac{I_{Nbe}}{I_{Nbe} + I_{Pbe}}$$

- **The forward current transfer ratio, α_F:**

This is simply defined as:

$$\alpha_F = \frac{I_c}{I_e}$$

Assuming that the contribution of holes to the collector current is negligible:

$$I_c = B_F \times I_{Nbe}$$

And thus:

$$\frac{I_c}{I_e} = \alpha_F = \frac{B_F I_{Nbe}}{I_{Nbe} + I_{Pbe}} = B_F \gamma$$

Thus, $\alpha_F = B_F \gamma$

Therefore:

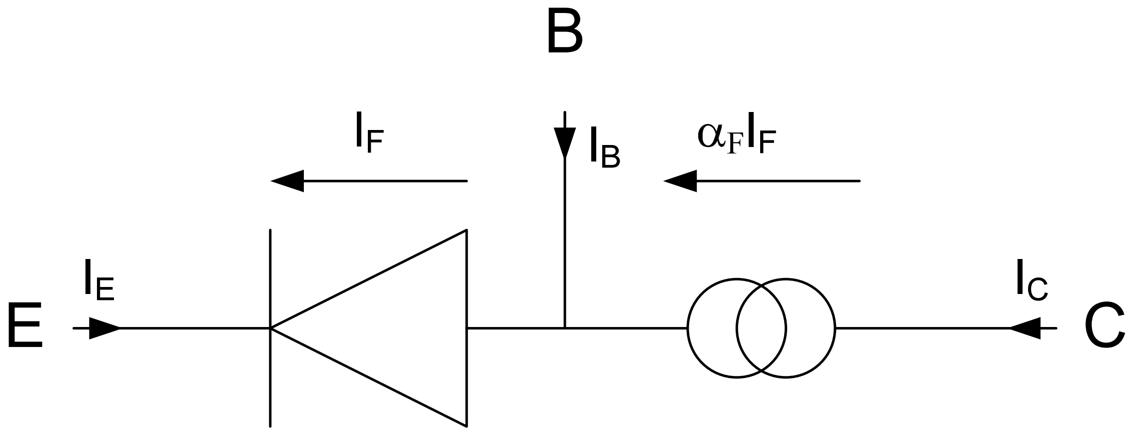
$$\alpha_F I_F = B_F \gamma (I_{Nbe} + I_{Pbe})$$

$$\therefore \alpha_F I_F = B_F \left(\frac{I_{Nbe}}{I_{Nbe} + I_{Pbe}} \right) (I_{Nbe} + I_{Pbe})$$

And thus:

$$\alpha_F I_F = B_F I_{Nbe}$$

We can therefore write our equivalent circuit in terms of currents only, and not worry about what type of carrier makes up which current.



Much neater!

The BJT in saturation

Now let's look at what happens to the device saturation. In saturation, both junctions are forward biased. If we look at the concentration of electrons in the device, we have:

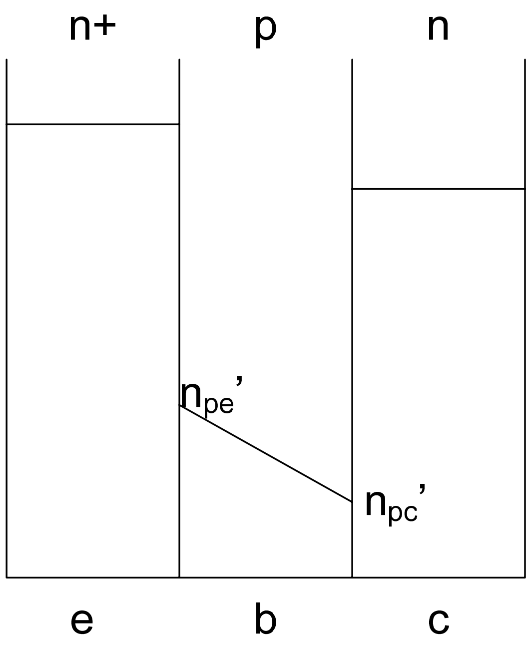
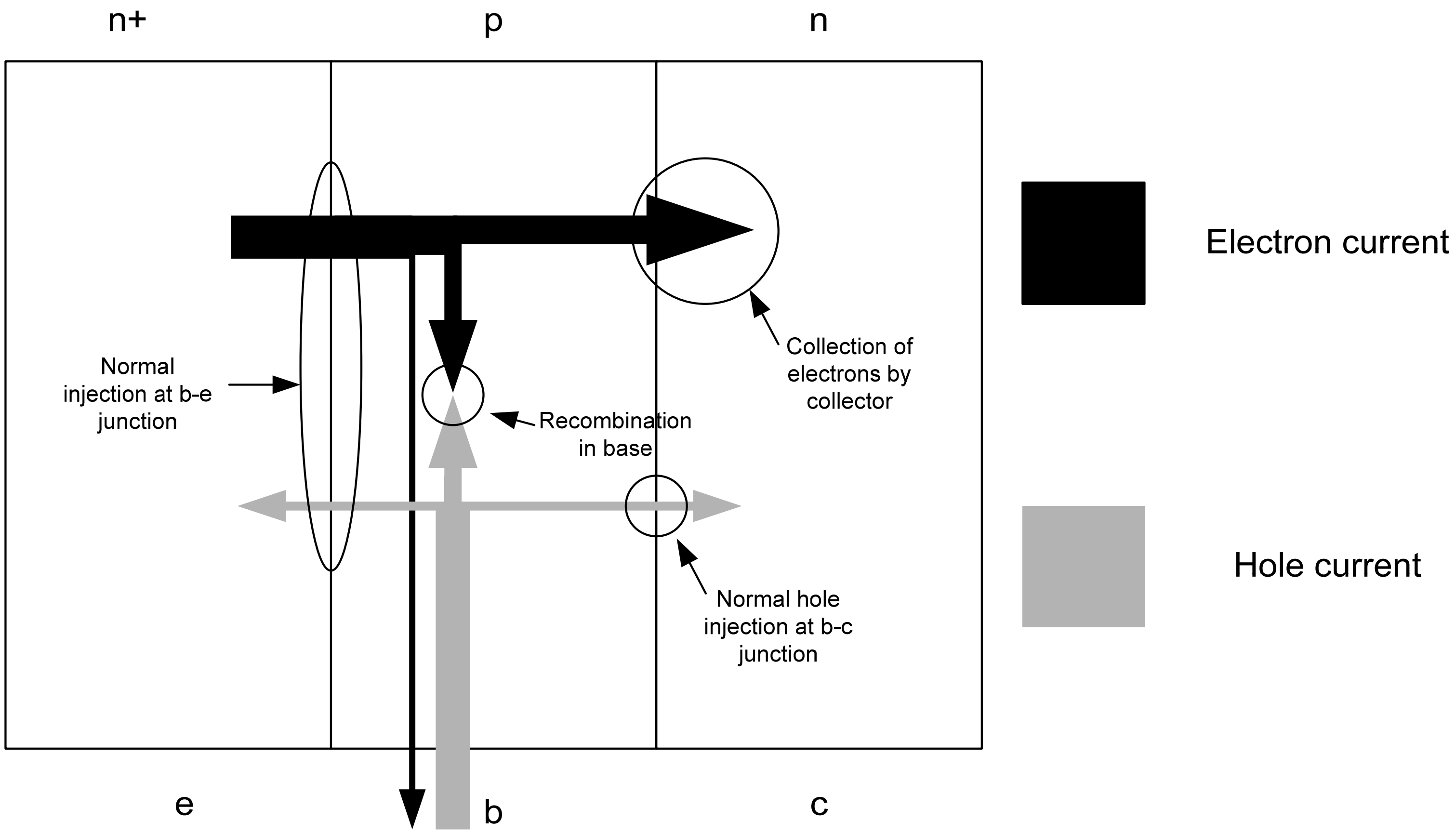


Figure 3 BJT electron concentration in saturation

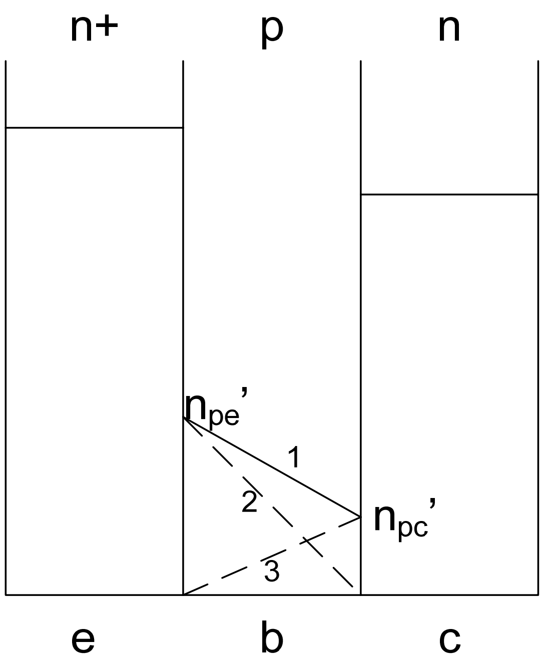
Carrier flows in Saturation…



- Electron current decreased
- Base current increased – holes injected into collector and emitter

Look at the electron current…

Can think of this as being made of a forward and a reverse flow of electrons (device in saturation in each case), due to the principle of linear superposition:



$$I_t = K\frac{n_{pe}' - n_{pc}'}{L_b}$$

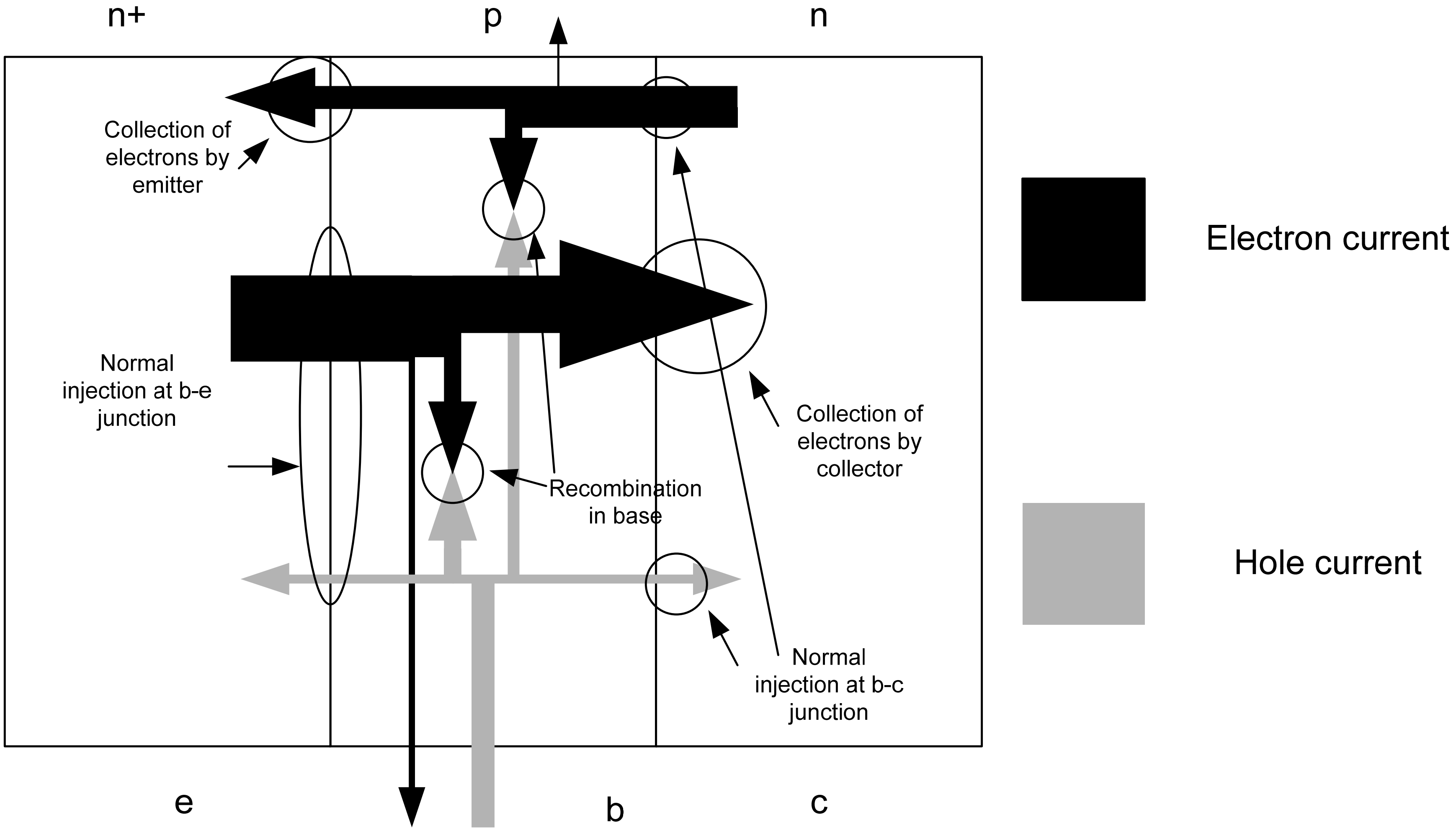
$$I_f = K\frac{n_{pe}'}{L_b}$$

$$I_r = K\frac{n_{pc}'}{L_b}$$

$$I_t = I_f - I_r = K\frac{n_{pe}' - n_{pc}'}{L_b}$$

Where K is just a constant of proportionality and L_b is the length of the base

Carrier flows with forward and reverse currents



Summary of this lecture

- The SPICE diode model is a piecewise non-linear function, which includes breakdown
- It is essential to have the GMIN convergence aid in that model because the conductance of the diode is set to zero for much of the characteristic in reverse bias
- The exponential equation you know for the behaviour of a BJT is not accurate in the saturation region and so not useful (on its own) for a SPICE model
- The started to look at the development of the Ebers Moll BJT model
- We can think of the currents in a saturated BJT as being a sum of forward and reverse carrier flows in the base for equivalent forward and reverse BJTs operating in active mode

Next time…

- We will finish the Ebers-Moll model and see how it relates to the SPICE model
- We will look briefly at the SPICE MOSFET models