A Global Maximum Power Point Tracking DC-DC Converter

by

Joseph Duncan

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

This thesis describes the design, and validation of a maximum power point tracking DC-DC converter capable of following the true global maximum power point in the presence of other local maxima. It does this without the use of costly components such as analog-to-digital converters and microprocessors. It substantially increases the efficiency of solar power conversion by allowing solar cells to operate at their ideal operating point regardless of changes in load, and illumination. The converter switches between a dithering algorithm which tracks the local maximum and a global search algorithm for ensuring that the converter is operating at the true global maximum.

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Title: Design Manager

MIT Thesis Supervisor: David J. Perreault
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Acknowledgments

This thesis would not have been possible without the assistance of the people below. I would like to thank Randy Flatness and Robert Dobkin for proposing the idea for the thesis. Talbott Houk and Eugene Cheung were invaluable in their roles as mentors and supervisors. I benefited greatly from their expertise in the fields of analog circuit design and power electronics. A working prototype of this thesis would not have been possible without Eugene Cheung's assistance and perseverance in the final stages of debugging. Thank you to Dave Bell and Linear Technology for their continued support of the VI-A program.

I would also like to thank my parents for their support of all aspects of my life, but especially of my education. They have been great role models but have also supported fully my desires to pursue a highly independent life.

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Chapter 1

Introduction

Worldwide interest in sustainable energy sources is increasing as both environmental awareness and oil prices continue to grow. The cost barriers to wider adoption of solar power are continuing to drop, with photo-voltaic (PV) cells reaching an average price of $2.12 per peak watt in 2002. Total shipments of PV panels and cells by US manufacturers increased 15% from 2001, continuing the trend of uninterrupted growth since 1993 [1].

Solar cells transform energy from an essentially unlimited source – the sun – into useable electricity. Because of the limitless nature of the source it is almost always desirable to draw as much power as possible from the solar cells. Unfortunately, direct connection of solar cells to batteries or inverters in grid-tie systems almost never allows optimum power transfer. A maximum power point tracker (MPPT) performs a load transformation to allow the solar cell to operate at this optimum point.

Partial shading creates multiple local maxima on the power-voltage or power-current curve of a typical solar panel, in which multiple solar cells are connected in series. This causes a problem for traditional MPPTs which simply assume a single maximum power point (MPP) and are prone to getting stuck on smaller local maxima.

This thesis develops algorithms and circuitry to perform true global MPP tracking without the use of costly components such as analog-to-digital converters and microprocessors. In addition to a dithering algorithm used to find the local power

maximum, the converter periodically runs a global search to ensure that it is tracking the true global maximum.

A prototype board has been built and the results of testing verified that the system behaves as expected under various lighting conditions including finding the correct peak in the presence of multiple local maxima.

1.1 Solar Panel Characteristics

A typical 120W solar panel consists of 48 PV cells connected in series and bypass diodes in parallel with each group of 24. Uniform insolation produces P-V curves similar to that shown in Figure 1-1.

Under partial shading conditions, multiple local maxima are created in the P-V curves. Without the bypass diodes, the current demands of the high insolation cells force shaded cells to reverse bias, wasting significant power. The bypass diodes allow sections of the panel to conduct the required current with a smaller voltage drop, reducing the amount of loss. Since all cells in the series chain must pass the same amount of current, P-V local maxima are created at each cell's optimum current level. As the current increases, shaded cells are bypassed, cutting their power output, while power from the remaining cells increases. Figures 1-2 and 1-3 are example P-V curves for weak and strong partial shading respectively.

1.2 Boost Converters

In a typical solar installation, many panels are connected in series to provide a high-voltage output into either a series stack of 12V batteries or a grid-tie inverter. However, with parallel connection of the solar panels and the addition of a simple MPPT, each solar panel can be individually controlled to provide its maximum power at all times. The optimum voltage output from each panel therefore must be stepped-up to match the expected levels at the load.

A generic boost converter, as shown in Figure 1-4, is a step-up DC-DC transformer.

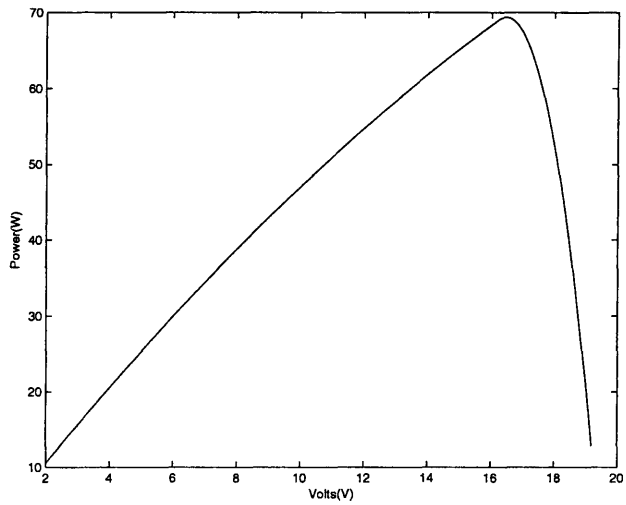

Figure 1-1: P-V Curve of a 48-cell solar panel under uniform insolation

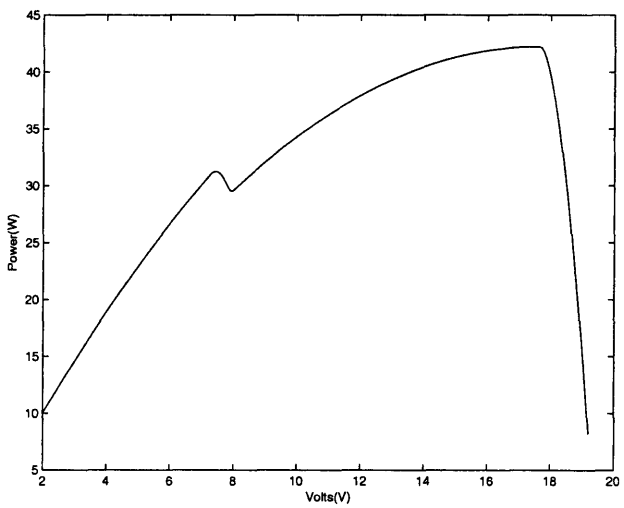

Figure 1-2: P-V Curve of a 48-cell solar panel under partial weak shading

It consists of a switch, diode, inductor, and capacitor. The conversion ratio for the boost converter can be determined by assuming that the inductors and capacitors are large enough that we can treat voltages and currents as DC values. The switch can be replaced by an equivalent voltage source with value $(1-D)V_{out}$. The complementary duty cycle, $D' = (1-D)$, represents the fraction of time when the diode conducts. Assuming an ideal diode, during this time period, the intermediate voltage, V_{SW}, is shorted to V_{out}. When the switch is on, the intermediate voltage shorts to ground. Thus, its average value is equal to $(1-D)V_{out}$ [2]. Since at DC the inductor can be replaced by a short,

$$V_{in} = (1-D)V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D}$$

The above equations express the conversion ratio of the boost converter in terms of duty cycle assuming constant-frequency operation. A boost converter can also be operated with constant on-time or constant off-time switching. In both of these cases, changes in duty cycle result in changes in frequency. This thesis will concentrate on a constant-frequency boost converter.

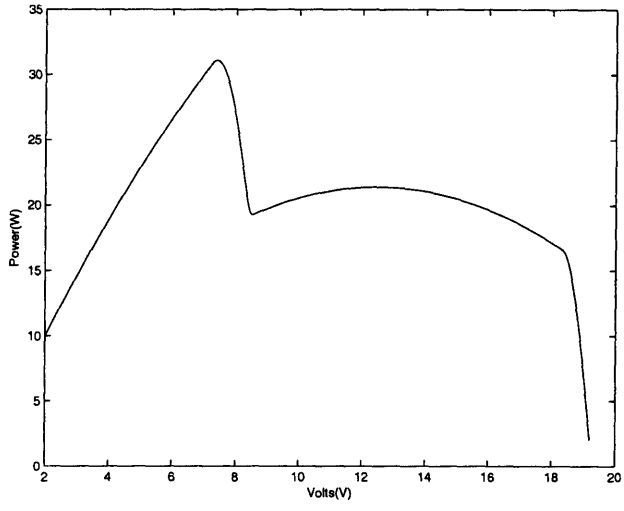

Figure 1-3: P-V Curve of a 48-cell solar panel under strong partial shading

Since we are looking for the peak in the P-I curve of the solar panel, it makes sense to directly control maximum inductor current instead of duty cycle. When the switch is on, the inductor current ramps up at a rate of $\frac{V_{in}}{L}$. When the switch is off, SW rises to V_{out} so that the diode turns on and the inductor current can flow into the output capacitor. During this phase, the inductor current ramps down at a rate of $\frac{V_{out}-V_{in}}{L}$. Peak inductor current is a valid replacement control variable because it increases monotonically with duty cycle.

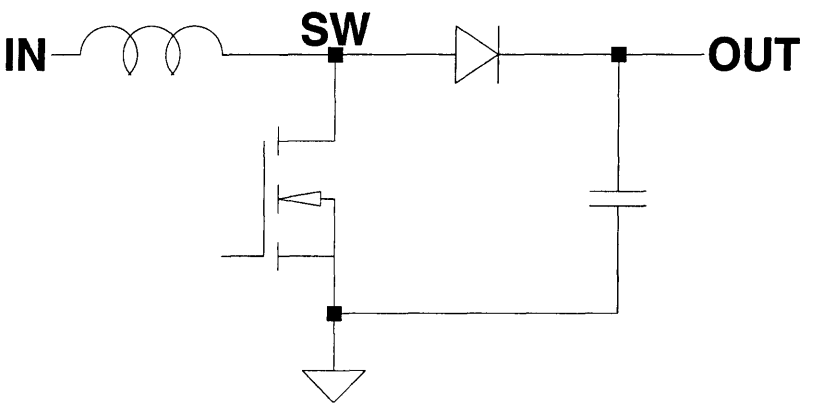

Figure 1-4: Generic Boost Converter

1.3 Maximum Power Point Trackers

Previous maximum power point trackers (MPPTs) have been flawed in one of two ways. All prior analog control implementations ignored the problem of multiple global maxima [3] [4], deeming it too difficult to solve without the use of analog to digital converters (ADCs) and a microprocessor. Others have done exactly what was suggested in the analog control papers and solved the problem with ADCs and a microprocessor. These solutions work; however, they require a large amount of hardware, necessitating more board space, raising the solution cost, and increasing the implementation complexity.

The solution described in this thesis finds the real maximum power point, even in

the presence of multiple local maxima. Figure 1-5 shows how an ideal MPP tracking boost converter can achieve maximum power out at any voltage above the real MPP. If voltages below this point were required, a buck converter could instead be used.

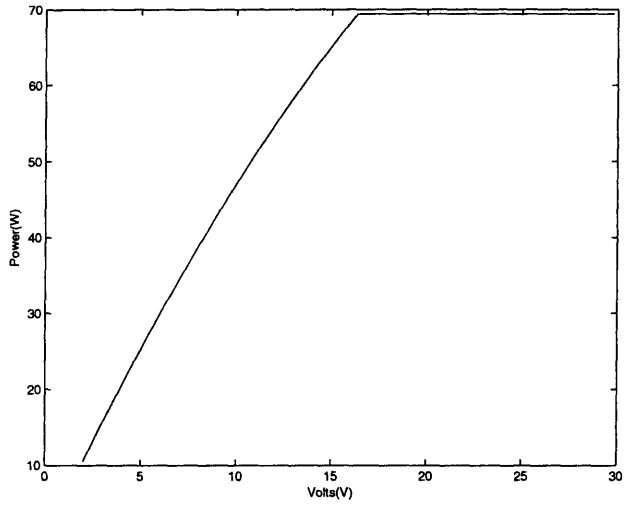

Figure 1-5: Solar panel attached to an ideal MPPT boost converter

This is accomplished entirely with analog and simple digital components. The system is suitable for integration into an integrated circuit requiring only a minimal number of external components. This level of simplicity and integration enables the system to be attached directly to solar panels, eliminating the need for a costly intermediate MPPT box between the panels and their battery or inverter load.

Other systems have been proposed as MPPTs that I do not believe meet the criteria for a "tracker". Some of these systems rely on the assumption that under perfect insolation conditions, a solar cell will produce its maximum power at approximately 70% of its open circuit voltage V_{oc}, or approximately 85% of its short circuit current I_{sc}. While this is indeed accurate under ideal conditions, if clouds, trees, or any other obstacles partially shade the solar panel, it will drastically change the P-I curve, as shown in Section 1.1 such that the panel is no longer operating anywhere near the maximum power point. The other category of MPPTs that do not qualify as "trackers" are those that use prior measurements of the particular solar

panel's characteristics under uniform insolation to determine the maximum power point. These are simply more accurate versions of the converters that operate at a fixed percentage of V_{oc} or I_{sc} and therefore do not actually track. They suffer from the same susceptibility to changing insolation conditions.

1.4 Organization

Chapter 1 has given motivation for this thesis, explaining why it is a topic of interest. It also provided background information on the characteristics of solar panels, basic boost converter operation, and prior maximum power point trackers. Chapter 2 details the design of both the local and global control algorithms, as well as the supervisory system on a purely conceptual level. Chapter 3 explains the operation of the algorithms at a more detailed level, as well as showing how each portion of the algorithms was implemented in real circuitry. In chapter 4 we will show basic simulation results that were used to validate the initial design described in Chapter 3. Chapter 5 will describe the layout and construction of a printed circuit board (PCB) prototype for testing of the circuit. Chapter 6 presents the results of the PCB prototype testing and Chapter 7 will recap key results and insights gained from this thesis.

Chapter 2

Algorithms

2.1 Local Dithering Algorithm

Given a starting operating point on a particular hill in the power-current curve of the solar panel, the local dithering algorithm must be capable of finding the peak of that hill and tracking it as it moves.

A logical flow-chart of the algorithm is shown in Figure 2-1. The controller begins by recording output power and then stepping duty cycle either up or down (the actual direction is irrelevant). It then measures the new output power to determine whether power increased or decreased with the step. If power increased, the converter will make another step in the same direction and again measure the difference to decide what to do from there. If power instead decreased with the original step, the next step will be in the opposite direction, and so on.

When the algorithm converges, it will limit cycle around the local maxima with at least two steps in each direction. When it is operating with a duty cycle just below the MPP, it will increase duty cycle once, register an increase in power as it hits the peak, and increase duty cycle a second time. This second increase will cause duty cycle to exceed the MPP, and the converter will step the operating point back down. The increased power will trigger another step down in duty cycle, thus lowering power. The above limit cycle will then repeat.

2.2 Global Search Algorithm

Under non-uniform insolation conditions, solar panel P-V and P-I curves can show multiple local maxima as shown in section 1.1. The local dithering algorithm described in section 2.1 uses a hill climbing technique that settles into a limit cycle around the high point of the P-I bump it begins on. A separate global search algorithm shown in Figure 2-2 is necessary to ensure that the local dithering operates around the true maximum power point, instead of a lower local maxima.

The algorithm sweeps the converter's operating range while recording the peak output power through a peak detector. The peak detector then switches to a second capacitor and the operating point sweep is restarted. The voltages on the capacitors are continuously compared using a comparator that trips when the second sweep comes within an acceptable delta of the maximum power point stored by the first capacitor. The second sweep then stops and the system returns to the local dithering algorithm. Since it is essential that the comparator always trips, it must be set to

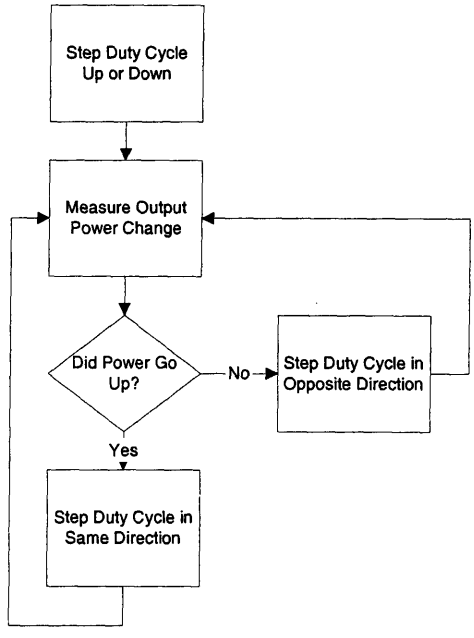

Figure 2-1: Local Dithering Algorithm

do so just below the maximum power point to allow for random offset and noise. As long as the trip point is close enough to ensure that the algorithm ends on the correct peak, the local dithering algorithm will zero in on the MPP. In the case of two peaks so close in power that the comparator trips on the wrong one, the error is by definition small enough to be unimportant.

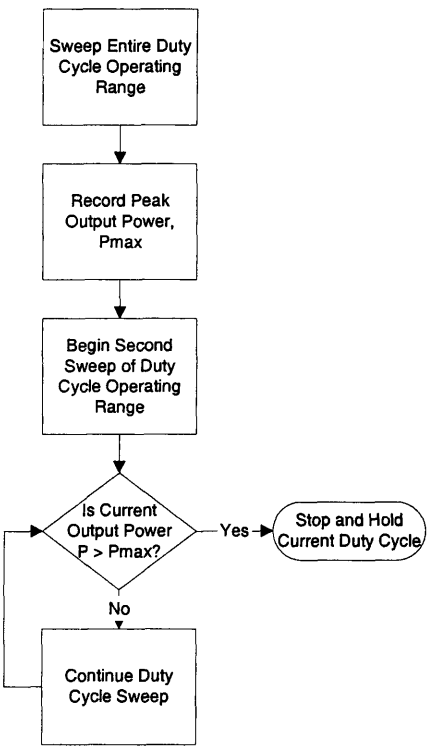

Figure 2-2: Global Search Algorithm

2.3 Supervisor System

A supervisor system is required to switch the converter between the local dithering and global search algorithms. For basic operation, the supervisor simply needs to periodically switch in the global search algorithm to ensure that the converter is operating in the vicinity of the true maximum power point. As soon as the maximum

power point is re-established, the supervisor will switch back to the local dithering algorithm. The above process should be repeated periodically with each timeout. This is shown in Figure 2-3. The duty cycle of the global algorithm in the prototype implementation is a negligibly small 0.1%. Therefore, even if power output was zero during the entire global sweep (which it clearly isn't as the sweep includes everything between zero and maximum power) the efficiency hit could not exceed 0.1%.

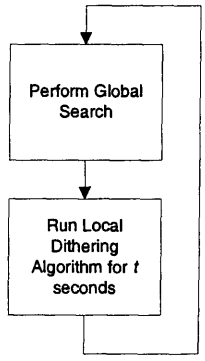

Figure 2-3: Supervisor Algorithm

Chapter 3

Implementation

Appendix A shows the entire schematic of the final prototype board. The following sections describe the individual parts of the system without necessarily describing the specifics of all components used.

3.1 General Circuitry

The LTC1871 wide input range, current mode, boost, flyback, and SEPIC controller [5] was used in boost mode as the basis for the MPPT converter in this thesis. It's ability to accept a high input voltage, and synchronize to an external clock were key features required for the design. Additionally, the on-chip 5.2V voltage regulator was able to power all of the other circuitry on the board. Figure 3-1 shows the basic circuitry required for the boost controller.

The *Mode* pin of the LTC1871 is driven by an on-board 300 kHz oscillator. This synchronizes the converter with the sampling circuitry of the local dithering algorithm as will be explained in Section 3.2.

When the LTC1871 is used as a regular boost converter, the I_{th} pin is connected to a compensation capacitor. This pin is the output of a transconductance amplifier in the feedback loop regulating output voltage inside the integrated circuit (IC). The voltage at this pin directly controls the maximum inductor current and is valid between approximately $300mV$ and $1.2V$. Since we want to maximize output power

instead of regulating an output voltage, this pin is directly driven by the control circuitry described in Sections 3.2 & 3.3.

Since off-chip circuitry overpowers the regular voltage regulating feedback loop, the resistive divider from the output to the FB pin is only used for over-voltage protection.

The on-chip frequency setting resistor, R_{freq}, simply needs to be set for a frequency sufficiently below 300 kHz to ensure the LTC1871 correctly synchronizes with the on-board oscillator [5].

The resistor, R_{sense}, in the load return path generates a voltage proportional to output current. This voltage monotonically increases with output power as all loads of interest in this thesis always have a positive incremental impedance.

3.2 Local Dithering Algorithm

The local dithering algorithm described in Section 2.1 and shown in Figure 2-1 requires the ability to measure output power and the ability to change the operating point (maximum inductor current) in a known (and remembered) direction. Remembering the direction in which the algorithm last moved the operating point also requires some form of state.

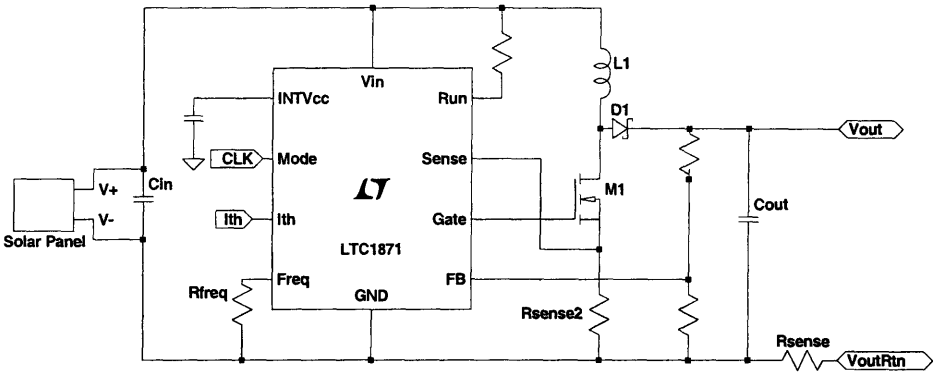

Figure 3-1: Basic Circuitry for LTC1871 Boost Converter

Unfortunately, the output current (proportional to output power) signal generated on R_{sense} as shown in Figure 3-1 has very large ripple at the switching frequency of the converter. For any continuous time derivative to work, this switching frequency ripple needs to be completely eliminated. By definition, the derivative of any signal containing ripple continually changes sign at the ripple frequency! Any continuous time derivative system would require heavy filtering that would be extremely difficult, if not impossible. Because it is desirable to run both the local dithering and global search algorithms as quickly as possible, the ripple-free output power signal should not be filtered at such a low cutoff frequency that its time constant dominates the response of the entire system. This makes the filtering requirements even more complex.

The use of a discrete time differentiator completely eliminates this problem. If the sampling frequency is equal to or a sub-harmonic of the switching frequency, a perfect notch filter is effectively created at the switching frequency. The local dithering algorithm uses a 16-phase clock as shown in Figure 3-2. Figure 3-3 shows the circuitry used to generate this clock. The outputs are inverted because the LTC201A transmission gate switch IC used for the sampling switches has active low control terminals [6]. The same on-board oscillator used to drive the converter is also used here as the input to the synchronous counter to ensure that both sub-circuits are operating at exactly the same frequency. This forces sampling to always occur at the same point in time relative to the switching cycle and performs the notch filtering described above. The divided-by-thirty-two 9kHz counter output forms the base period of the sampling clock. That signal is combined with the divide-by-sixteen, divide-by-eight, and divide-by-four counter outputs using NAND gates to form ϕ_2 and ϕ_{15}. The div-by-thirty-two signal is also used later in the signal chain as an equivalent to "ϕ_1" because the rising edges of the two signals are coincident and the falling edges are unused.

Figure 3-4 shows the circuitry used to perform the discrete differentiation. The algorithm only requires knowledge of whether output power increased or decreased, and not the magnitude of that change. Therefore, it is sufficient to simply connect two sampling capacitors (sampled at separate times) to the inputs of a comparator. The

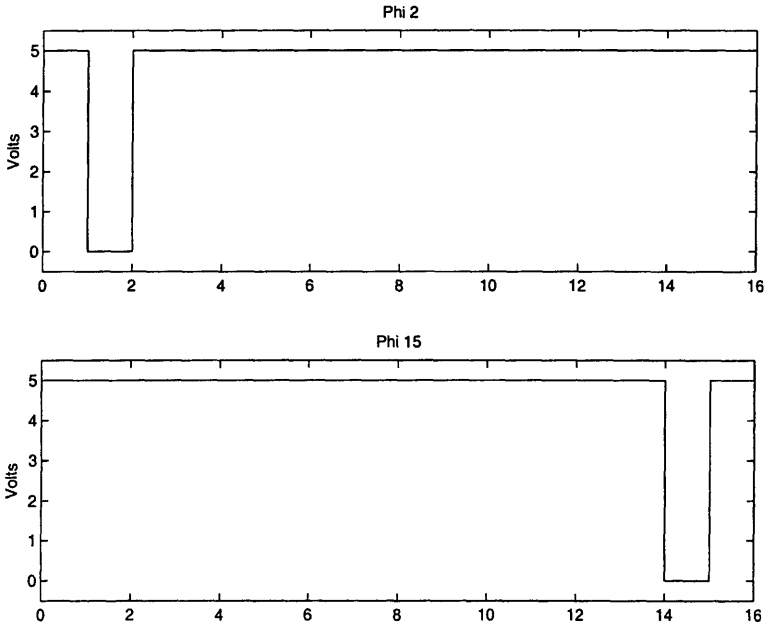

Figure 3-2: Outputs of 16-Phase Clock

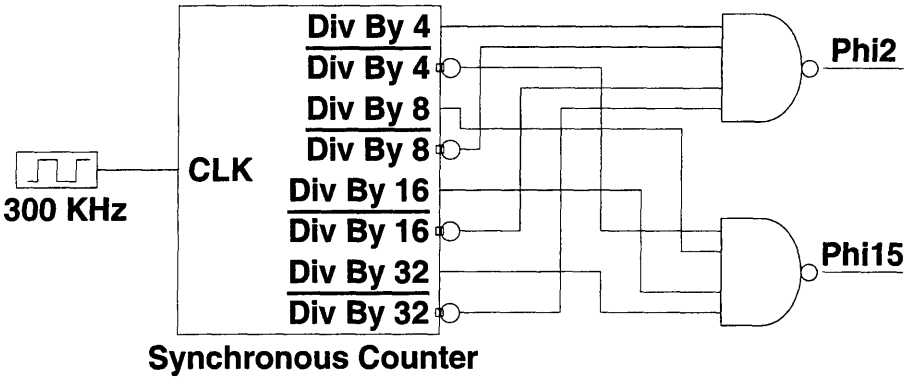

Figure 3-3: Generation Circuitry for 16-Phase Clock

first capacitor is sampled on the rising edge of ϕ_2 and the second capacitor is sampled on ϕ_{15}. If the voltage on the first capacitor is larger, power increased over the previous time period. If the voltage on the second capacitor is larger, power decreased. Non-inverting amplifiers with a gain of five are placed between the sampling capacitors and the comparator in order to increase the signal level and reduce the effect of any comparator offset. The output of the comparator will be valid some settling time after the rising edge of ϕ_{15}. The LT1671 comparator [10] used is fast enough to ensure that the output is valid long before time 0 (in Figure 3-2 when the result will be recorded on the rising edge of the div-by-four signal described above.

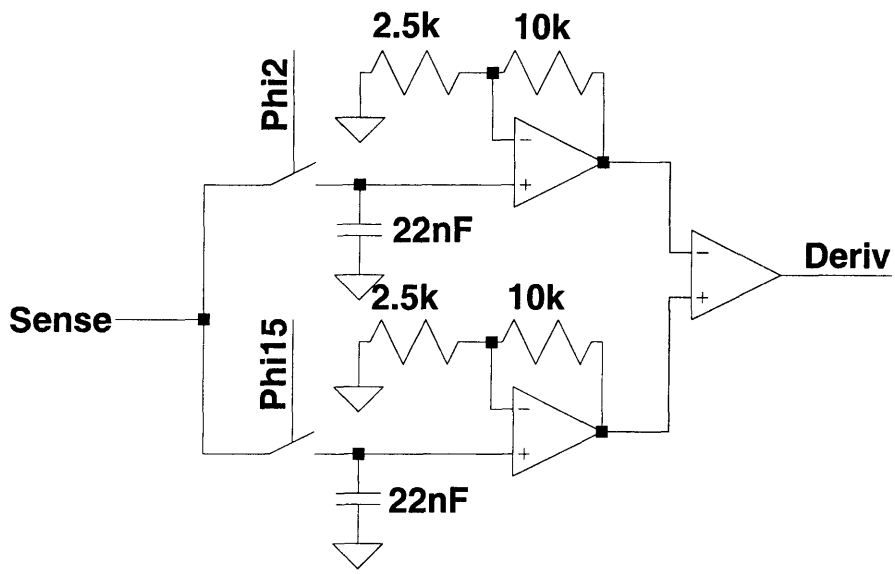

Figure 3-4: Discrete Time Differentiator

So far, the circuitry used to measure the output power "derivative" has been described. This must be combined with a memory of which direction the operating point was moved to decide which direction to move in next. Circuitry is also required to control the operating point based on this decision. Figure 3-5 is an equivalent description of the system showing how the signals can be combined to accomplish this goal. The output of the D Flip-Flop, $\frac{dI_{th}}{dt}$, is fed into an integrator whose output,

I_{th}, is connected directly to the I_{th} pin of the LTC1871 boost controller as described in Section 3.1. This integrator has other inputs from the Global Search Algorithm and Supervisor System that will be described in Section 3.3.

The input to the D Flip-Flop is generated by dividing the output of the differentiator, $\frac{dP_{out}}{dt}$ by the output of the D Flip-Flop, $\frac{dI_{th}}{dt}$. The resultant signal, $\frac{dP_{out}}{dI_{th}}$, represents the incremental slope of output power with respect to maximum inductor current (the control variable). Because we are actually operating with discrete time, quantized variables, the division would be performed by an XOR gate. However, to simplify the implementation, a JK Flip-Flop can replace both the D Flip-Flop and the feedback XOR gate.

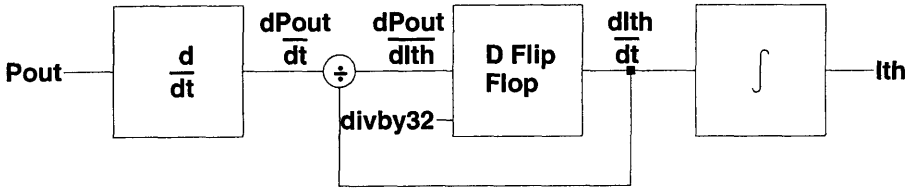

Figure 3-5: Local Dithering Algorithm using a D Flip-Flop

Figure 3-6 shows the circuitry taking advantage of this simplification. It is easiest to understand how these two circuits are equivalent by considering the behavior of a JK Flip-Flop and what happens under various input conditions. When both inputs of a JK Flip-Flop are tied together (as is the case), the output depends on the previous output. In the case of inverted inputs, when the inputs are both high the output remains the same as on the previous clock. When both inputs are low, the output toggles. Since the input is $\frac{dP_{out}}{dt}$, when output power is rising, the output of the JK Flip-Flop stays constant and the operating point continues moving in the same direction. When output power is decreasing, the output of the Flip-Flop toggles, and the operating point begins moving in the opposite direction. The Flip-Flop is clocked by the divide-by-thirty-two signal as in the timing diagram of Figure 3-2, its rising edge occurs at time 0, when the comparator output has become valid.

3.3 Global Search Algorithm

The Global Search Algorithm requires a means of taking control of and sweeping I_{th}, the operating point variable. It also needs to detect and record peak output power during sweeps and recognize when output power in the second sweep returns to the peak of the first sweep.

The integrator circuitry controlling I_{th} that was mentioned in Section 3.2 is shown in Figure 3-7. Since all of the control circuitry is operating on the 5.2V supply from the boost controller's low dropout regulator (LDO), the output of the integrator is put through a resistive divider to prevent the I_{th} pin from exceeding it's absolute maximum rating [5] if the integrator rails.

The inverting input of the opamp is nominally 2.5V. Thus, all inputs to the integrator drop 2.5V (from either 5V or GND) across their resistors. For the local

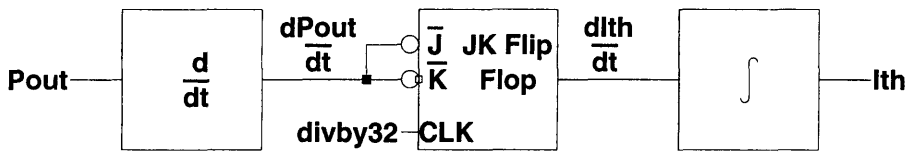

Figure 3-6: Local Dithering Algorithm using a JK Flip-Flop

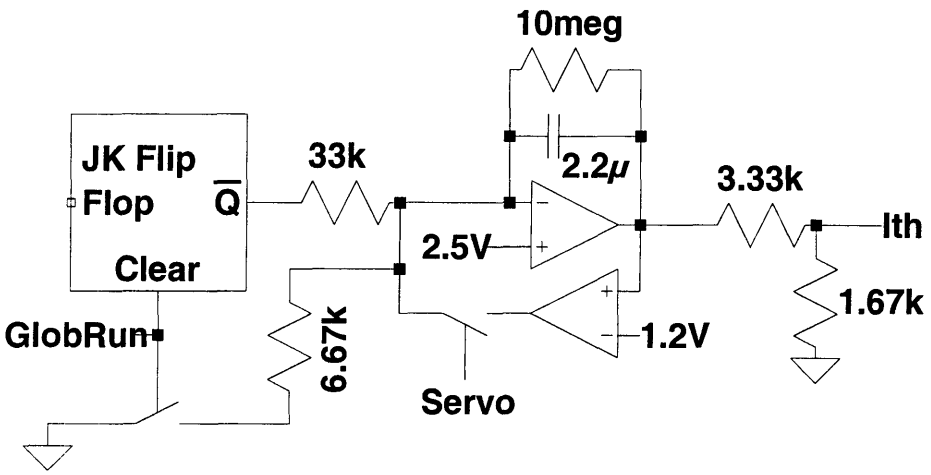

Figure 3-7: Ith Control Integrator

dithering algorithm's JK Flip-Flop input, this gives an input current of 757μA. The rate of voltage ramp for the integrator can be found by using the formula, $I = C \cdot \frac{dV}{dt}$. This can be rewritten as $\frac{dV}{dt} = \frac{I}{C}$ giving a ramp rate for the local dithering input of $344\frac{V}{S}$. Dithering decisions are made on a 9kHz clock, therefore I_{th} moves approximately 13mV during each dithering cycle. This value was chosen empirically during the simulation phase of design.

During global sweeps, the supervisor module asserts the *GlobRun* node, forcing the flip-flop output to ground and simultaneously connecting a second integrator input to ground through a 6.67kΩ resistor. The lowered resistance through this paralleled ground input increases the integrator ramp rate to almost $2000\frac{V}{S}$, sufficient to ensure a full sweep of I_{th}'s range in as little as 2mS.

Before each of the two I_{th} sweeps, the integrator output is reset to 1.2V. This forces I_{th} to 0.4V, about the minimum useful value. To accomplish this reset, a servo amplifier is placed in feedback around the integrator. The switch used has a typical on-resistance of 140Ω (2 LTC201A switches in parallel [6]) allowing a quick slew rate while being large enough to avoid any stability concerns.

The peak detect circuitry used for the global search algorithm is shown in Figure 3-8. The Sense signal from the sense resistor in the load return path is first level-shifted up through two cascaded PNP transistors. This ensures that even in situations where maximum output power is low, the NPN peak detect transistor can still turn on and charge the peak detect capacitors.

The output current peak-to-average ratio changes with the boost converters duty cycle. This means that once the operating point continues past the true maximum power point, *peak* output current (and power) can continue to increase. Because we record the peak output current, this causes the global search to terminate at a later point in the sweep. The simple RC filter inserted between the level shift PNP transistors and the peak detect NPN transistor reduces this effect to a tolerable level.

At the beginning of each global search, the supervisor system asserts the Reset node, shorting the peak detect capacitors to ground (while it simultaneously servo's I_{th} back to 0.4V). Then, when the sweep begins, PD1ON is asserted and the first

capacitor is connected to the peak detector. PD1ON is de-asserted when the first sweep finishes. After I_{th} is servo'd the second time, PD2ON is asserted and the second capacitor is connected to the peak detector. Both capacitors are always connected to a comparator whose output changes state during the second sweep when output power returns to the maximum recorded during the first sweep.

3.4 Supervisor System

The supervisor system generates the signals that enable and control the global search algorithm. The GlobRun, PD1ON, PD2ON, Reset, and Servo signals described in Section 3.3 are all generated by the supervisor system.

A timeout of approximately 14 seconds was chosen for the prototype design. This results in a duty cycle for the global search of less than 0.1%. Given that the system is still producing power through almost all of this time (including maximum power for some small percentage), this results in a negligible hit to overall system efficiency. The 14 second timeout was created by cascading the 8-bit counter used for the local dithering algorithm mentioned in Section 3.2 with an asynchronous 14-bit counter. The resultant 22-bit counter's most significant bit (MSB) output has a period of 14 seconds.

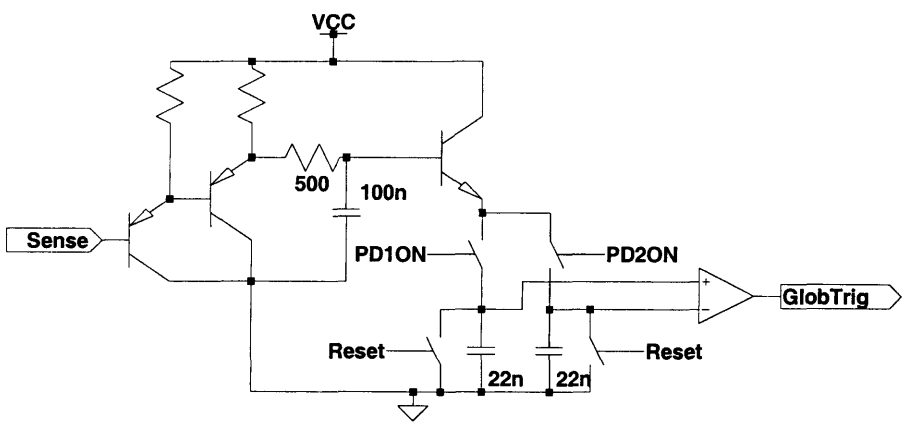

Figure 3-8: Peak Detect Circuitry

Two other counter outputs are combined with a cascade of D Flip-Flops to produce most of the control signals. This is shown in Figure 3-9. The simple logic functions used to generate GlobRun and Servo are shown in Figures 3-10&3-11 respectively.

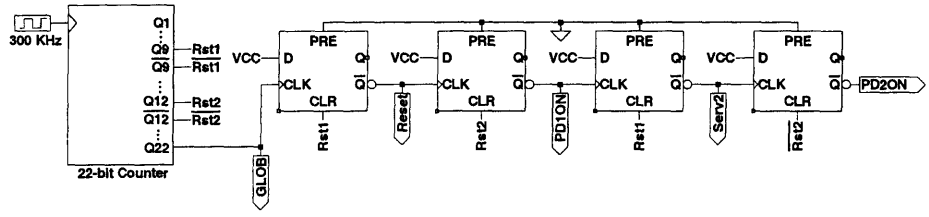

Figure 3-9: Main Supervisor System

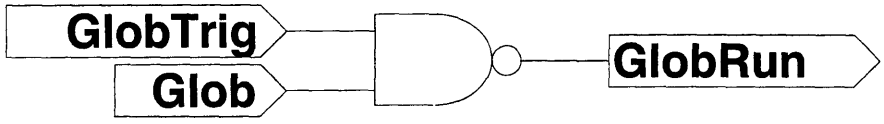

Figure 3-10: GlobRun Generation

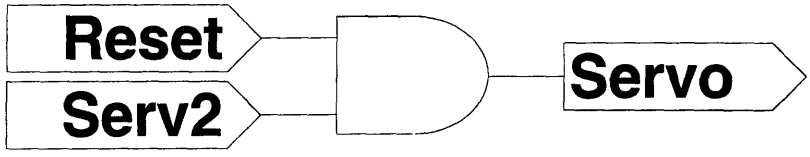

Figure 3-11: Servo Generation

Once every 14 seconds, on the rising edge of Glob, a high input is clocked into the first D Flip-Flop. Since Glob is the MSB output of the counter, all other counter outputs will be low. The Reset node (active low) will be asserted until the Rst1 counter output goes high. Since the second half of the counter is asynchronous, Rst1 will go high in one half period minus the time already spend rippling through to Glob. Since one half period is approximately $850\mu S$, this still gives plenty of time for the servo described in Section 3.3 to fully reset the integrator. This is also more than enough time for the peak detect capacitors to drain given that the time constant through the reset switches is $2.5\mu S$.

When Rst1 goes high it clears the output of the first Flip-Flop, forcing Reset ($\overline{Q}$ output of the flip-flop) high again and clocking the second flip-flop. This now asserts PD1ON and the first capacitor connects to the peak detector. This time we wait for Rst2 to go high and the same process repeats down the chain. Note that this method of generating these clock signals ensures that they are non-overlapping. Given that the clock signals have very small duty cycles (since they are only high for a short period of time once every 14 seconds) this is also one of the simplest methods for generating them.

The GlobRun signal is generated through the NAND (again, it is active low) shown in Figure 3-10. For it to be active both Glob and GlobTrig must be high. GlobTrig begins high and switches to a low state when the second peak detect capacitor exceeds the value stored on the first peak detect capacitor.

Since the servo needs to reset the integrator before both operating point sweeps, the Servo node must be active when either Reset or Serv2 are active. Because all signals involved are active low, an AND gate is used as shown in Figure 3-11.

Chapter 4

Simulation Results

The majority of the circuitry described in Section 3, Implementation, was verified in simulations using Linear Technology's SwitcherCAD [13] software before the prototype was built.

The full SwitcherCAD simulation schematic is shown in Figure 4-1. Most of the circuitry shown in Appendix A from the final prototype design was replicated for the simulations. The supervisor timing generation circuitry was omitted to simplify the simulations since its operation was relatively straightforward. The SwitcherCAD model for the LTC1871 boost converter did not support synchronizing to an external clock, therefore the local dithering algorithm clock signals were generated by dividing down the gate drive signal. This preserves synchronization between the converter and the sampling circuitry. Cascaded JK Flip-Flops were used in place of a counter again for ease of implementation in the simulations.

The solar cell was modeled in SwitcherCAD using an NMOS transistor, diode, resistor, and configurable voltage sources. The model is shown in Figure 4-2. A P-V curve for this model can be seen in Figure 1-1. The P-V curve is generated from an I-V curve which is essentially a NMOS I_{ds}-V_{ds} curve flipped about the x-axis and then shifted along the x-axis to end in the correct quadrant. This model approximates real solar cell curves reasonably well.

Figure 4-3 shows the simulation output with the solar panel model in full insolation. The top trace shows the two peak detect capacitor voltages. The center trace

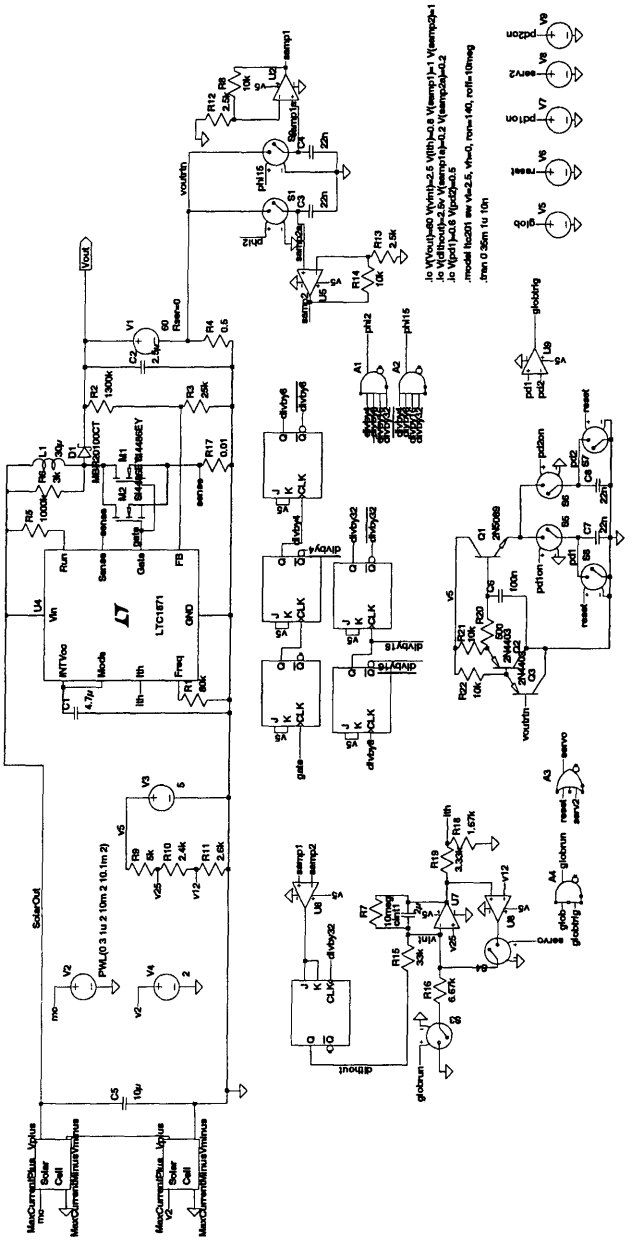

Figure 4-1: SwitcherCAD schematic used for simulations

is power out of the solar panel. The bottom trace shows I_{th}, the control variable for the system. This simulation shows a global search taking place shortly after startup followed by several milliseconds of local dithering. This local dithering would continue for the next 14 seconds before another global search took place. As I_{th} ramps in the first sweep, you can see power increase and decrease again as the maximum power point is passed. This value is recorded on the capacitor. Then, in the second sweep, as power returns to the value stored on the capacitor the system switches to dithering mode. Note that droop on the first capacitor across this time period is built in to ensure that the comparator will trip.

Figure 4-4 similarly shows I_{th}, solar panel output power, and the peak detect capacitor voltages for the case of partial shading. Partial shading generates the two peaks seen in the power curve. As can be seen in the simulation, the converter correctly identifies and tracks to the true maximum power point as expected.

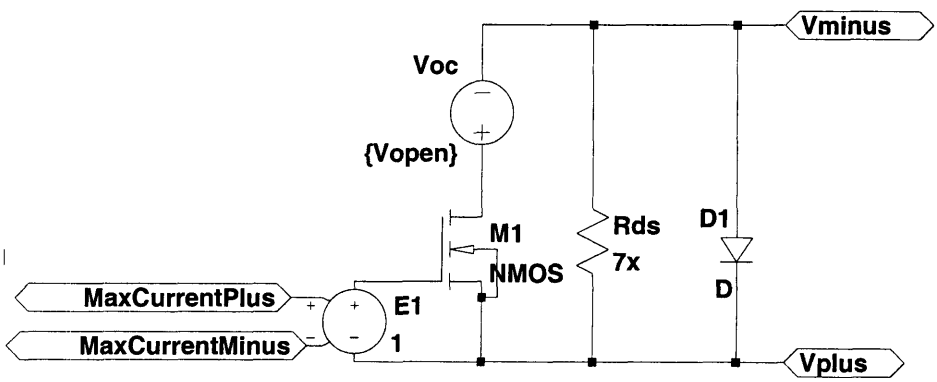

Figure 4-2: SwitcherCAD model for Solar Panel

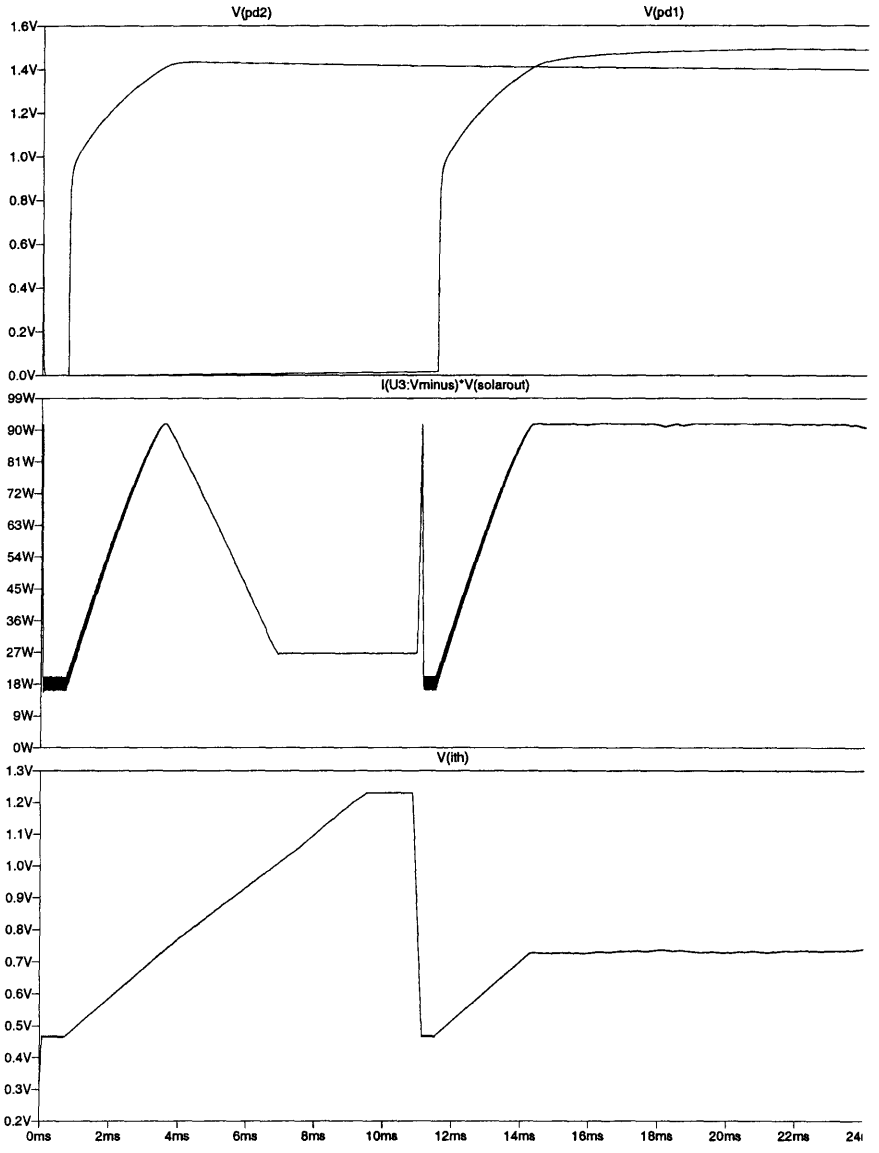

Figure 4-3: Simulation Output Showing Global Search and Local Dithering Algorithm Operation Under Uniform Insolation

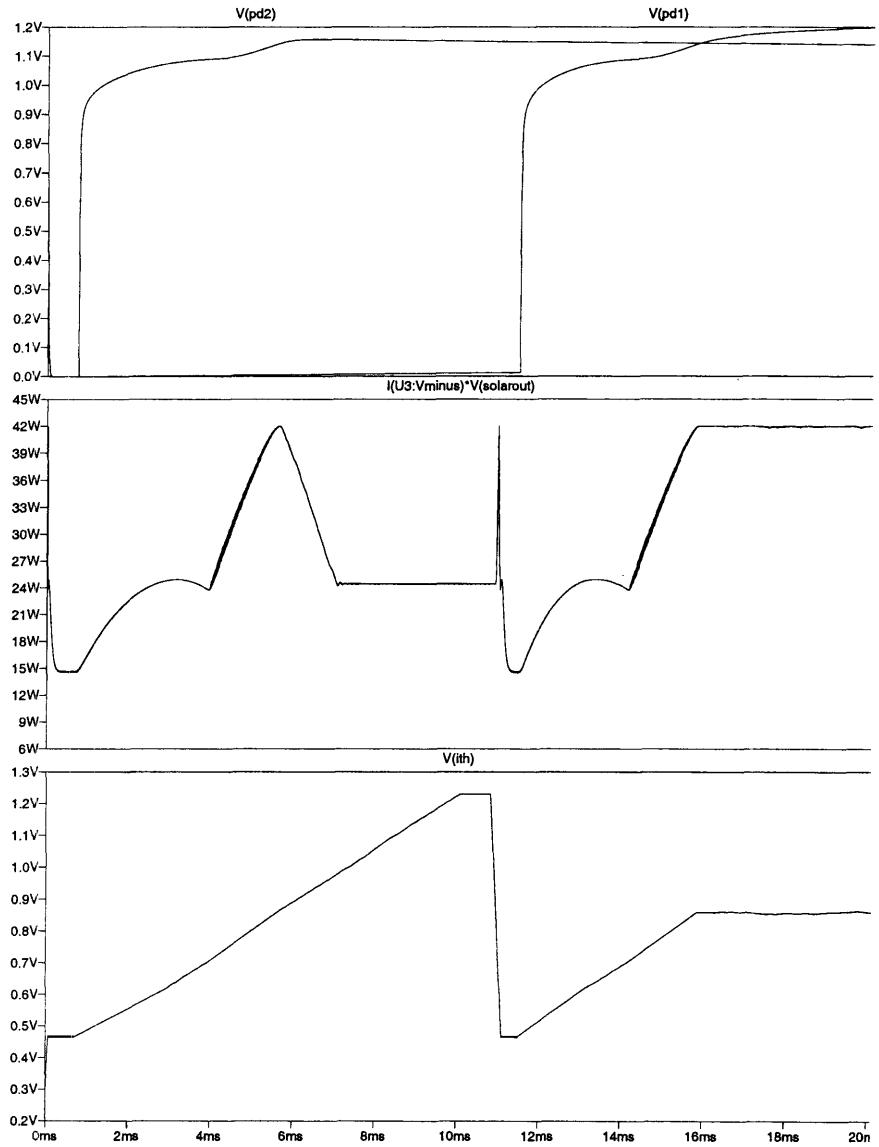

Figure 4-4: Simulation Output Showing Global Search and Local Dithering Algorithm Operation Under Partial Shading

Chapter 5

Prototype Design and Layout

5.1 Component Selection

Most components on the board were simply chosen according to hard design constraints. For example, referring to figures A-1 and A-2 in appendix A, the inductor L1 needs to handle a maximum current of approximately 7 amperes. Very few inductors are available with that current rating at $33\mu H$, therefore an inductor was designed in software and hand-rolled around an appropriate core. Two Siliconix Si4486 [8] power transistors are used in parallel. They were chosen for their combination of a high $V_{DS,MAX}$, low R_{on} and 5V gate drive capability. The diode was chosen to be the International Rectifier MBRB20100 [9] because of its high maximum reverse blocking voltage and low forward voltage (for such a high blocking voltage). The selection criteria for the boost controller itself, the LTC1871 [5] was explained in Section 3.1. Since it was necessary to have exact frequency lock between the LTC1871 boost controller and the sampling circuitry, the boost controller was driven by an external clock. The LTC6900 provided a simple means of generating an on-board clock with silicon in a small footprint [12]. Integrated transmission gates were used for all eight of the required switches. The LTC201A switch IC [6] had sufficiently low R_{on} and good off-state isolation. Most other components were non-critical and selection was restricted to finding the first component that would do the job.

The selection of U3 however was quite difficult. The dual opamp amplifies the

sampling capacitor voltages before presenting them to the comparator to reduce the effect of any comparator offset. Additionally, the LT1671 comparator [10] has a large input bias current relative to the size of the sampling capacitors which would create an unacceptable error in voltage over the time between the two samples. An opamp with very low input bias current can be used here to both reduce effective comparator offset and reduce the bias current seen by the capacitors. However, because of the small voltages generated on the sampling capacitors, any opamp used here must also have an input common mode range which includes ground. The LT1368 [11] is one of very few opamps that meet these goals.

5.2 Layout Considerations

The prototype was fabricated on a two-layer printed circuit board. The complete printed circuit board layout is shown in Figures 5-1 and 5-2. Figure 5-1 shows the top layer while Figure 5-2 shows the bottom layer. Note that these layout pictures do not reflect all the circuitry described in Chapter 3 as some small changes were made to the circuitry during debugging and testing.

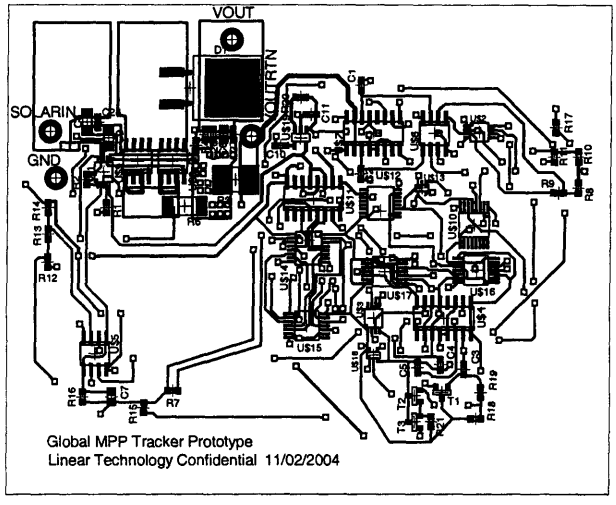

Figure 5-1: Top Layer of Prototype Printed Circuit Board

The ground plane that covers the vast majority of the bottom layer of the printed circuit board (PCB) can be seen in Figure 5-2. The top left corner of the ground plane is split off from the rest of the ground plane by a deliberate horizontal cut in the center left as well as a signal trace running vertically at the right hand end of the cut. This reduces the effect of switching noise on the rest of the control circuitry which may be very sensitive to any disturbances or potential differences in the ground plane. For instance, the sampling circuitry requires that ground be constant between the two sampling instants to ensure an accurate derivative.

The top left corner of the board containing the switching circuitry is particularly susceptible to poor layout. The loop from the positive input through the inductor and the diode to the output node, and back to ground was designed to be as short and low impedance as possible. The ground copper on the top of the PCB was connected to the bottom side ground plane (and therefore the negative input to the converter through a large number of vias to minimize any potential difference generated by the large current flow. The ground plane from these vias back to the negative input terminal was also kept completely clear of breaks.

The sensitive circuitry for the sampling and peak detect functions was restricted

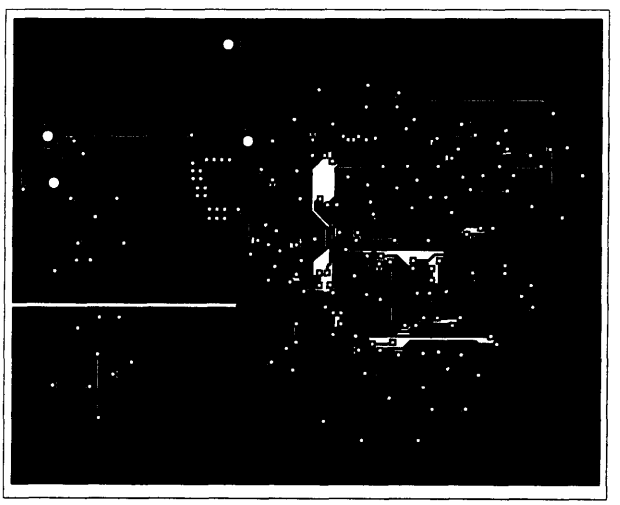

Figure 5-2: Bottom Layer of Prototype Printed Circuit Board

to the edge of the board well away from any ground current generated by the digital components. Trace lengths were minimized where possible.

The digital circuitry was initially laid out as closely as possible to try to fit the complete circuitry onto a 4" x 3" layout (the maximum allowed by the layout software used). Part way through layout it became clear that the circuitry would easily fit within this area regardless and the digital layout was finished in as straightforward a way as possible so that testing could begin.

Chapter 6

Prototype Testing Results

Testing of the prototype board consisted of general verification of operation, indoor testing using an artificial source, and outdoor testing with a solar panel under both full sun and partial shading.

Only key data is shown in this section. Appendix B presents complete measurement data.

6.1 General Operation

Verification of general circuit operation was performed using the artificial source described below in Section 6.2. Simple testing along the lines of that done in Section 6.2 was performed. This verified at first glance that the circuitry was operating as expected.

By observing I_{th}, the node controlling maximum inductor current (and therefore duty cycle), it is possible to verify basic functionality of both the global search and local dithering algorithms. Figure 6-1 is an oscilloscope capture showing the behavior of the algorithms on the I_{th} node. This matches the behavior shown in the simulation output Figure 4-3.

The lower trace in Figure 6-1 is simply used to trigger the capture when the global search begins. The upper trace is the I_{th} node. The "oscillations" at the left side of the capture are the global search algorithm. I_{th} initially slews down to its minimum

level. It them ramps back up to a maximum. Upon reaching this point, it slews back to the minimum again. The converter then switches to the second peak detect cap – as explained in Section 3.3 – and begins to ramp I_{th} a second time. When the ramp reaches the maximum power level recorded in the first sweep the global search terminates.

Since the two peak detect capacitors feed into a comparator, the voltage on the second capacitor must exceed the voltage on the first capacitor for the comparator output to trip. For printed circuit board prototyping such as that used here, this is a difficult thing to guarantee. It was accomplished by deliberately building in leakage on the first capacitor so that it drooped enough that the second capacitor would exceed it at the right time. Too much leakage causes the comparator to trip early, whereas too little leakage will cause it to trip too late or not at all. Looking at Figure 6-1, the overshoot on I_{th} from this phenomenon can be seen. There was slightly too little droop, causing the ramp to proceed for longer than was ideal. For

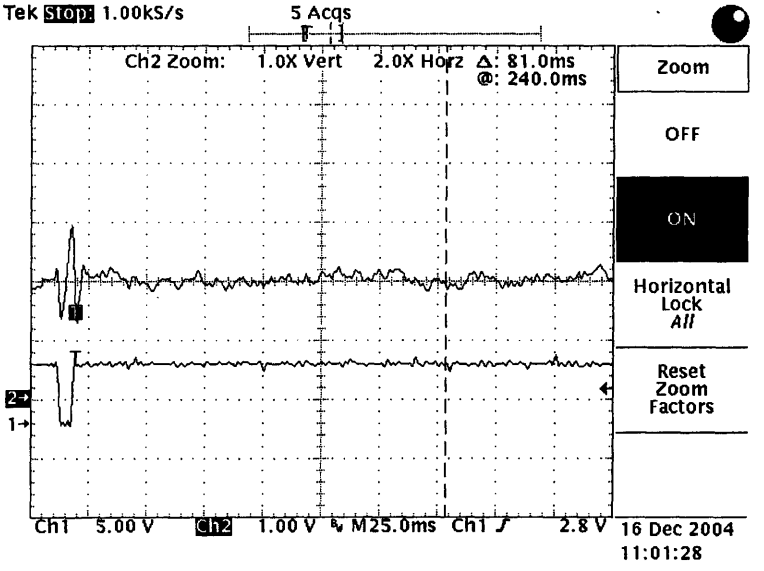

Figure 6-1: Oscilloscope capture photograph showing Ith behavior under the global and local search algorithms

an integrated circuit implementation, it is simple to build a specific amount of offset into the comparator, greatly simplifying this issue. As can be seen in Section 6.3.2, the overshoot was not significant enough to prevent the converter from finding the correct global MPP.

6.2 Indoor Testing

After general circuit operation was verified, full testing of the converter was performed using an artificial source indoors. This artificial source consisted simply of a variable DC voltage source in series with a variable resistance. Figure 6-2 shows the P-V curve of this source with $V_s = 30V$ and $R_s = 3\Omega$.

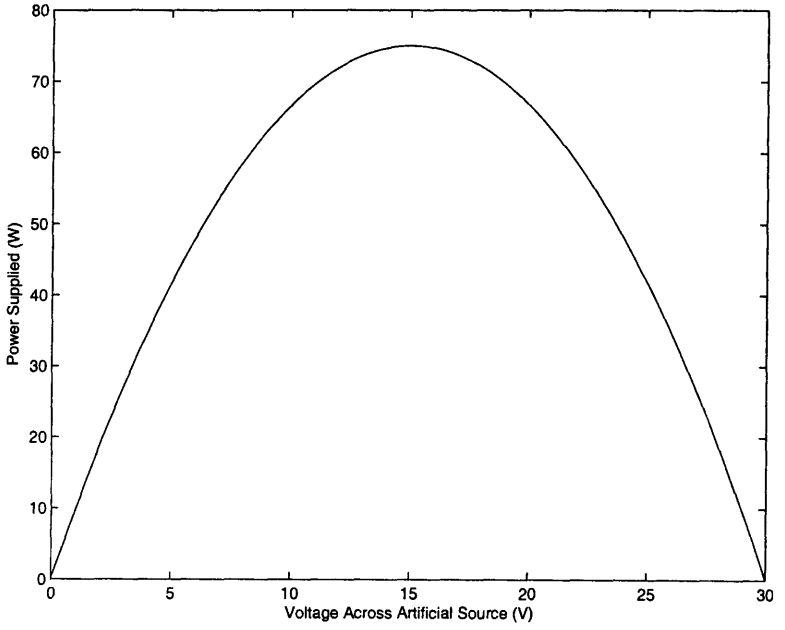

Figure 6-2: P-V curve of Typical Artificial Source

This curve can be generated from the following set of equations:

$$P_{out} = V_{out} \cdot I$$

$$I = \frac{V_s - V_{out}}{R_s}$$

$$P_{out} = V_{out} \cdot \frac{V_s - V_{out}}{R_s}$$

This is a parabolic function with a clear maximum at $\frac{V_s}{2}$. Adjusting R_s simply varies the maximum power available.

Figure 6-3 shows the P-V curve of the actual artificial source used at $V_s = 21.4V$ and $R_s = 3.16\Omega$.

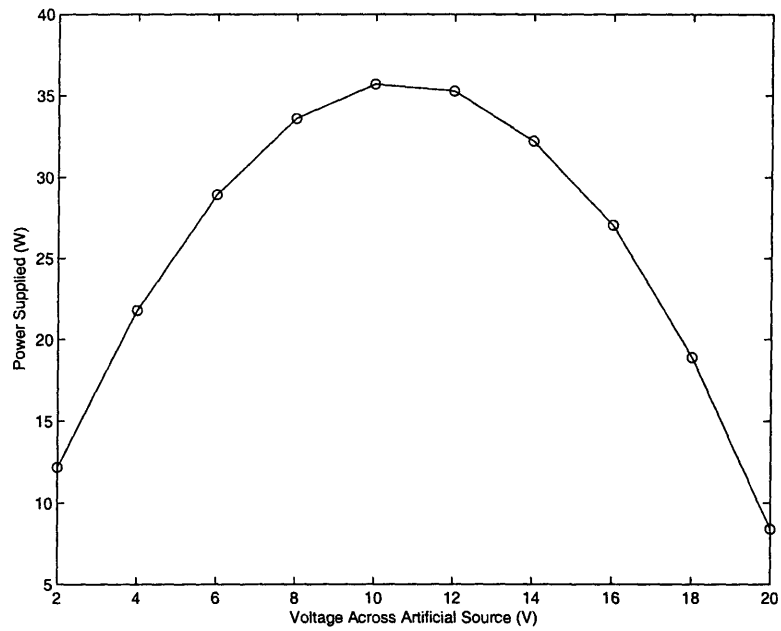

Figure 6-3: P-V curve of Actual Artificial Source

An active load capable of presenting a fixed voltage while sinking all output current was used for all testing. Figure 6-4 is a photograph of the indoor testing setup.

Ideally, the converter should provide the same output power (and close to the maximum power that the source is capable of supplying) into any voltage greater than the source voltage (a buck converter basis would be required to supply power into lower voltages). Practically however, the maximum output voltage is limited by

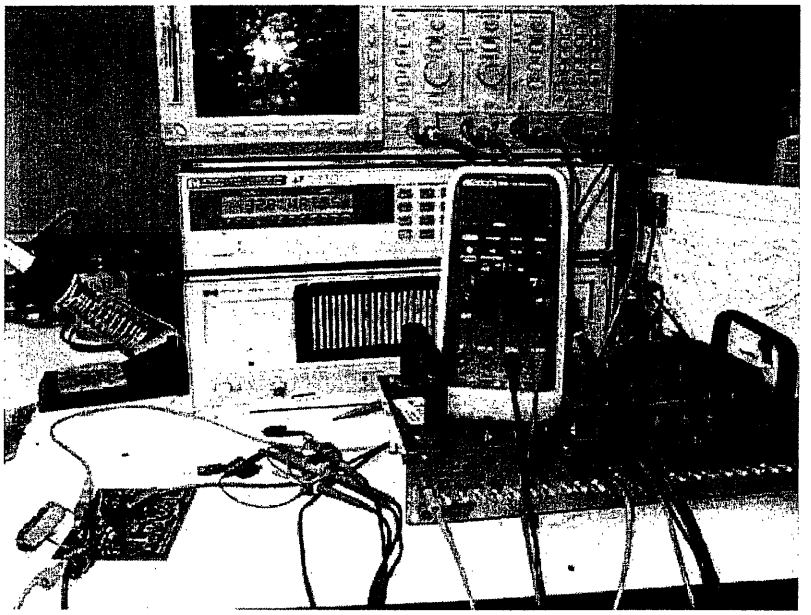

Figure 6-4: Indoor Testing Setup

both the LTC1871 controller [5] and the external control circuitry.

Figure 6-5 shows how power delivered to the load and power supplied by the source change as the output voltage is varied with $V_s = 21.4V$ and $R_s = 3.16\Omega$. The difference between the two curves represents the converter losses. The efficiency on this plot averages approximately 93.3%. When considering that the LTC1871 in its reference design achieves similar efficiencies [5], the control scheme appears to be very efficient. Given that this source configuration can supply a maximum of approximately 36.3W it is clear from Figure 6-5 that the converter is finding the maximum power point over most of the output range. Once V_{out} reaches approximately 48V, the converter loses its ability to track the maximum power point.

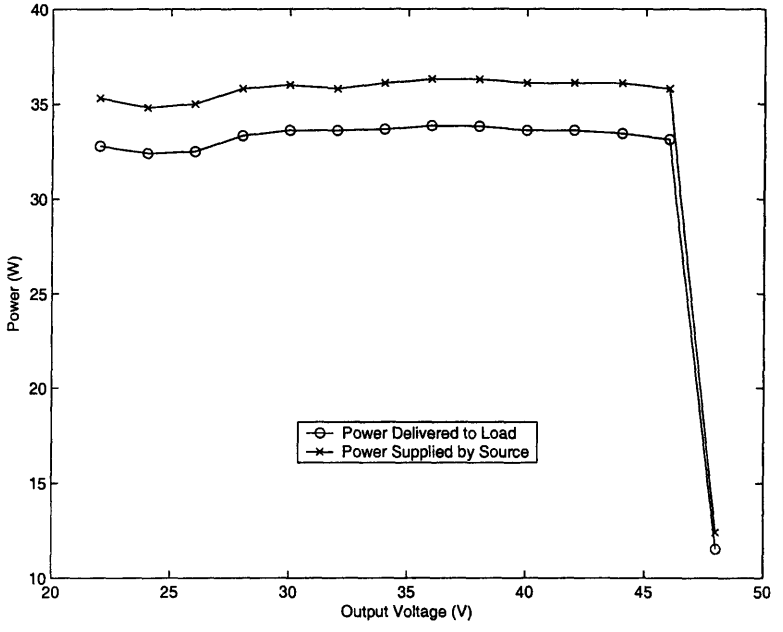

Figure 6-5: Input and Output Power over Vout for Vs = 21.4V, Rs = 3.16 ohms

Figure 6-6 similarly shows input and output power with $V_s = 30.9V$ and $R_s = 3.18\Omega$. Figure 6-7 has $V_s = 41.5V$ and $R_s = 6.16\Omega$. Finally, Figure 6-8 shows $V_s = 51.2V$ and $R_s = 6.16\Omega$.

The active load used was limited to a maximum voltage of 60V, therefore it was

impossible to determine the output voltage where the converter failed to track the MPP when V_s exceeded approximately 35V.

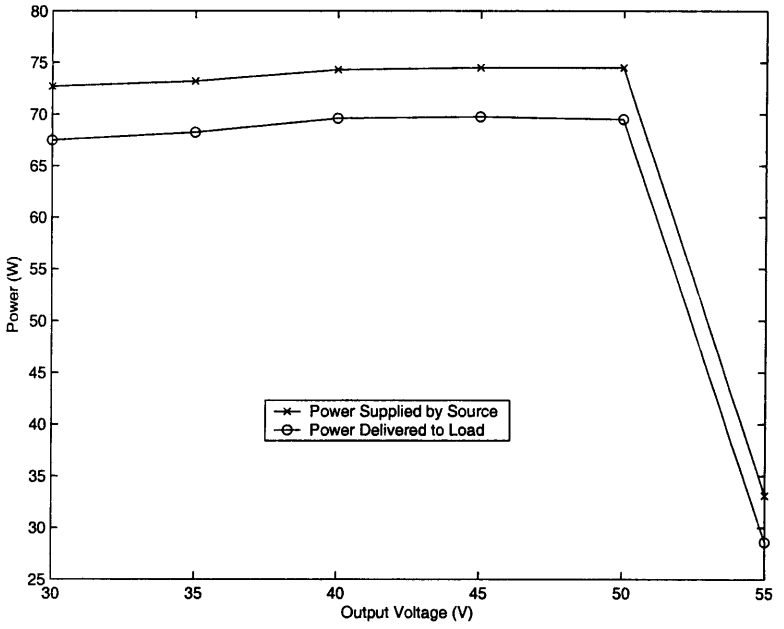

Figure 6-6: Input and Output Power over Vout for Vs = 30.9V, Rs = 3.18 ohms

Note that in the data used to generate Figures 6-5 through 6-8 overall system efficiency never falls below 93%, except when the converter can no longer track the maximum power point. At the higher power levels efficiency climbs as high as 94.7%.

As was shown in Figure 6-2 and its related equations, the artificial source has a maximum power point at half the source voltage. Therefore, the input voltage to the converter should always track such that its input voltage, $V_{in} = \frac{V_s}{2}$. Figure 6-9

At low source voltages the converter tracks to exactly the maximum power point. As the source voltage increases and the boost ratio is reduced, the converter tracks slightly to the high side of the ideal line. However, because of the parabolic nature of the source P-V curve, this represents only a small deviation from the maximum power point. For example, in Figure 6-9, the maximum deviation represents a power loss of approximately 1.5%. All other data points represent a power loss of well under

1%. Random offset in the local dithering algorithm circuitry causes this deviation from ideal behavior. Since the algorithm is trying to drive $\frac{dP_{out}}{dI_{th}}$ to zero (while also rejecting minimums) any offset effectively causes the converter to instead track to a non-zero derivative. As V_s increases, the P-V curve of the source broadens, and the voltage offset from the MPP required to reach the same non-zero derivative also increases. Therefore at low V_s, the converter tracks close to the ideal, whereas the error increases at high V_s.

Figure 6-10 shows the same behavior for $V_{out} = 40V, R_s = 6.18\Omega$.

6.3 Outdoor Testing

The converter was also tested outdoors with a solar panel as a source to verify its behavior under real operating conditions. It was tested with the solar panel under both full sunlight and partial shading. Partial shading testing showed that the panel was

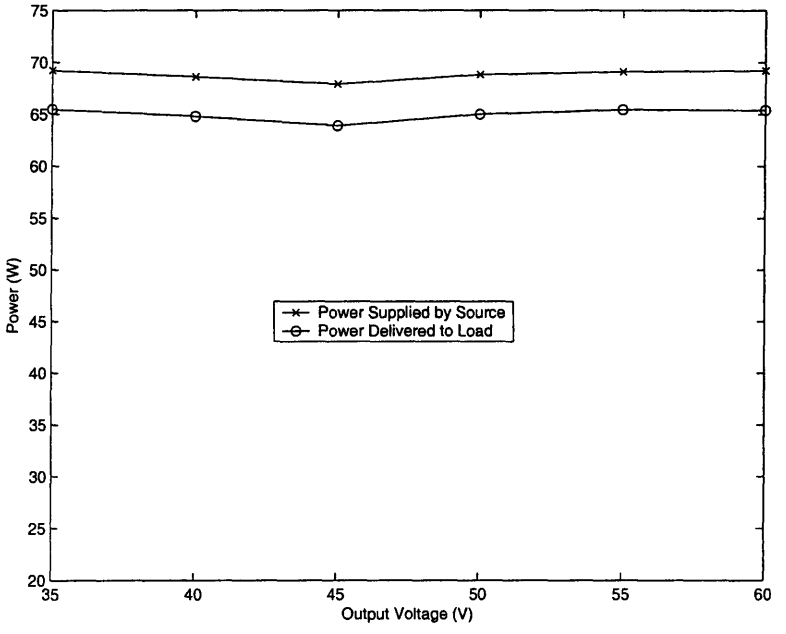

Figure 6-7: Input and Output Power over Vout for Vs = 41.5V, Rs = 6.16 ohms

capable of finding the true global maximum power point in the presence of multiple local maxima. Figure 6-11 shows the setup used for the outdoor testing.

As in the indoor testing, an active load was used that was capable of presenting a specific output voltage and sinking all available current. The 125 watt BP 3125 solar panel [7] was used as the source.

All measurements were performed in very late fall, so the power supplied by the panel reached a maximum of only approximately 60 watts.

6.3.1 Single Maximum

For testing the converter's ability to track the maximum power point when only a single maximum exists, the solar panel was placed in full sunlight.

Figure 6-12 shows the I-V and P-V curves of the solar panel that were recorded immediately prior to testing with the converter. These are similar to the theoretical curves described in Section 1.1. The panel was re-characterized immediately after

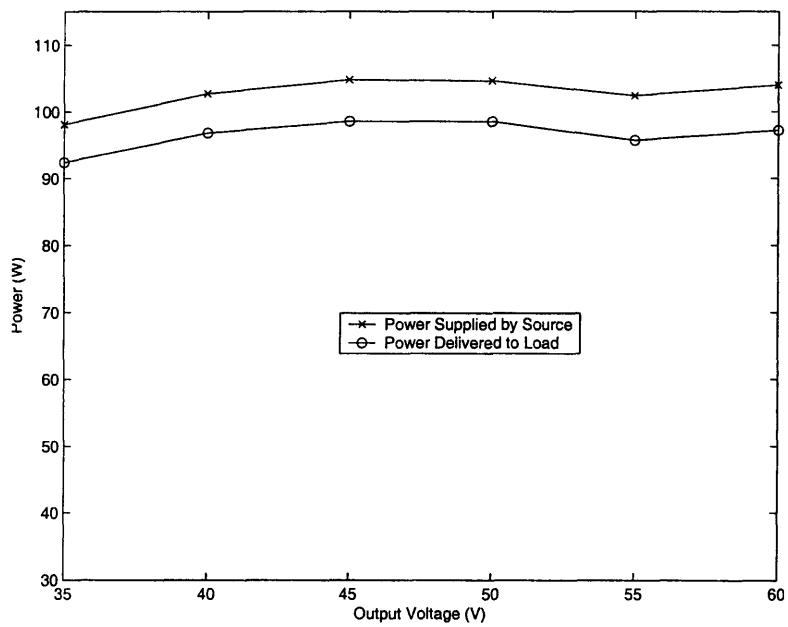

Figure 6-8: Input and Output Power over Vout for Vs = 51.2V, Rs = 6.16 ohms

testing to ensure that conditions had not changed significantly during the test time. The second set of curves was almost identical to the first.

With the converter in place between the solar panel and the active load, the load voltage was swept from 25 to 55 Volts. Figure 6-13 superimposes the solar panel characteristic curves before and after testing with the input and output power of the converter as V_{out} was varied.

The difference between the converter input and output power is the efficiency. For all output voltages tested, the converter operates almost exactly at the maximum power point. Therefore, for any battery load between 25 and 55 Volts connected to the converter, the panels would supply the maximum 60 Watts exactly as expected.

6.3.2 Multiple Local Maxima

Multiple local maxima were created in the solar panel P-V curve by partially shading a section of the panel. Figure 6-14 shows the resultant I-V and P-V characteristic

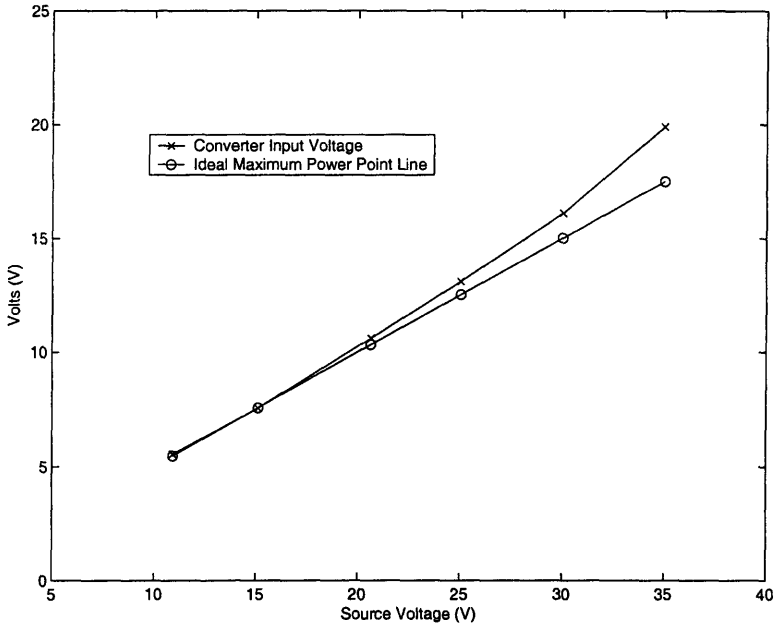

Figure 6-9: Converter Input Voltage, Vi over Vs for Vout = 40V, Rs = 3.18 ohms

curves.

The panel was characterized again after measurements had been taken with the converter. Unfortunately, unlike the full sun case, the characteristic curves shifted noticeably over the course of testing. When not in full sun, panel characteristics are very sensitive to the degree and area of shading. Movement of the sun – even during the few minutes required to take all of the measurements – noticeably changed the amount of shading and therefore the characteristic curves.

Once again with the converter in place between the solar panel and the active load, V_{out} was varied (from 25 to 45 Volts). Figure 6-15 superimposes the solar panel's characteristic curves before and after testing with the input and output power of the converter as V_{out} was varied. The change in the P-V curve between the two characterizations is clear in this figure. The true testing curve varied somewhere between the two boundary curves.

It is also clear that the converter tracked very close to the true global maximum

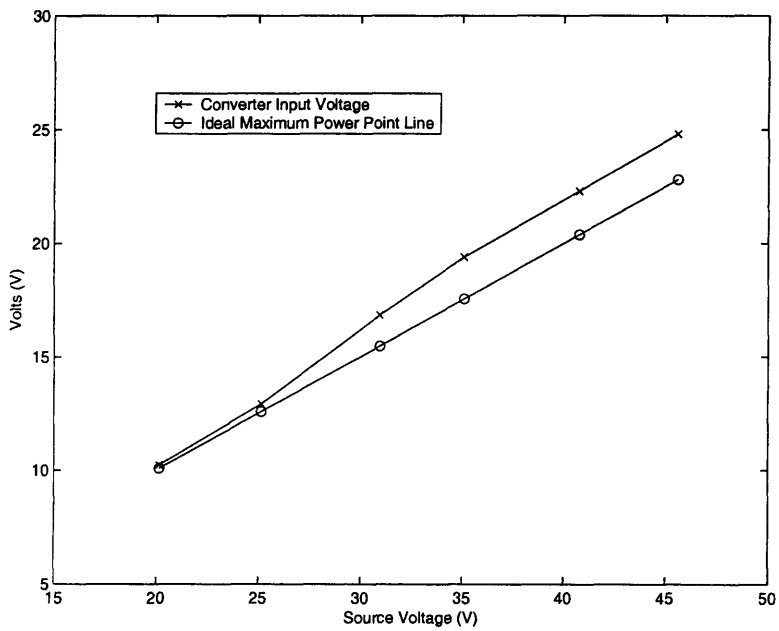

Figure 6-10: Converter Input Voltage, Vi over Vs for Vout = 40V, Rs = 6.18 ohms

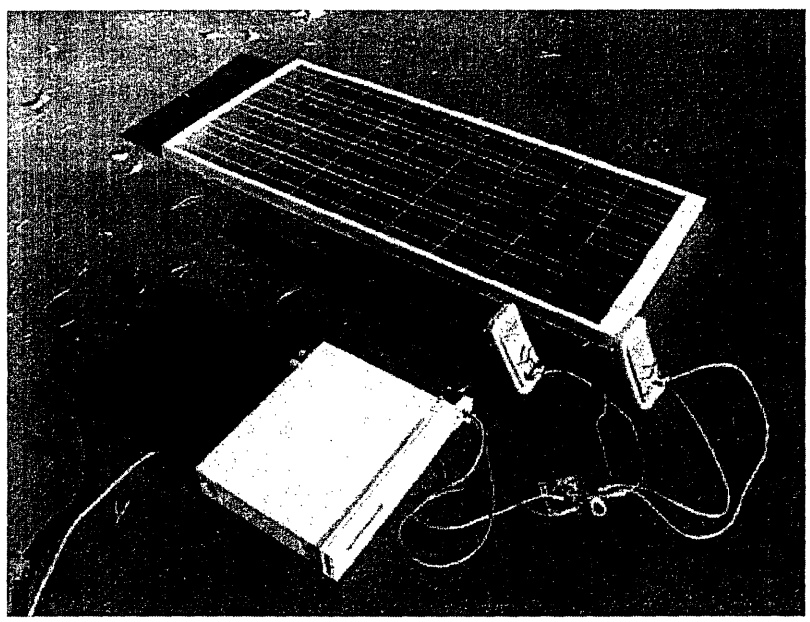

Figure 6-11: Outdoor Testing Setup

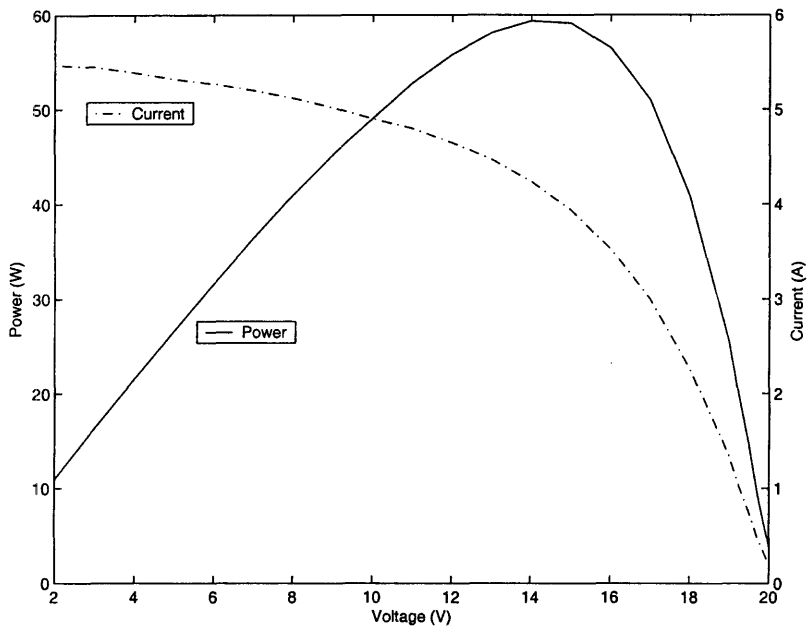

Figure 6-12: I-V and P-V characteristic curves of the BP 3125 solar panel under full sun test conditions

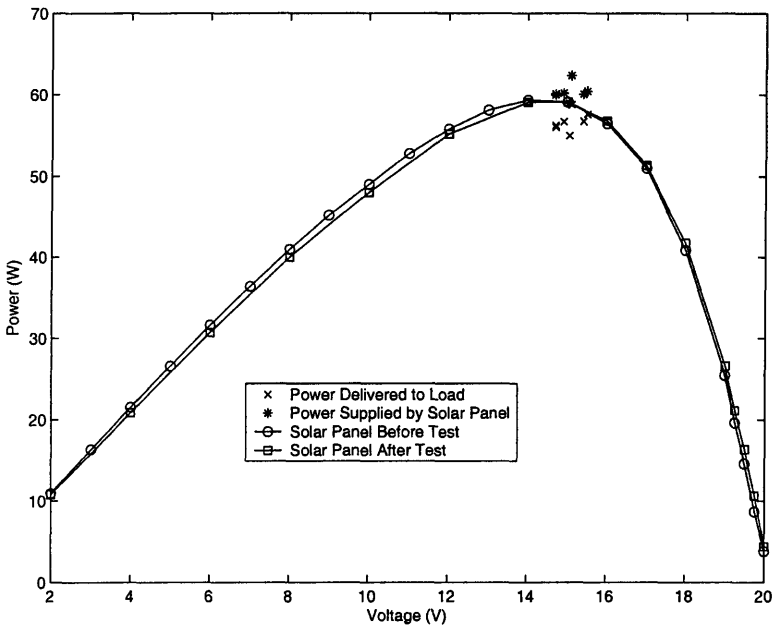

Figure 6-13: Converter input and output power vs. P-V curve of solar panel for different converter output voltages in full sun

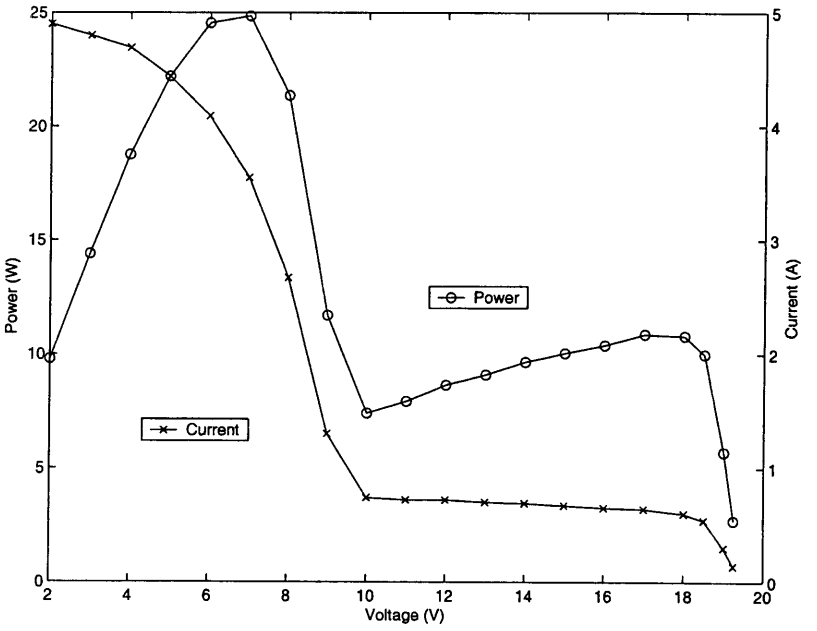

Figure 6-14: I-V and P-V characteristic curves of the BP 3125 solar panel under partial shading test conditions

power point over all tested V_{out} despite the presence of the second local maxima. The global search algorithm moved the operating point onto the larger of the two peaks then returned control to the local dithering algorithm which zeroed in on the actual MPP.

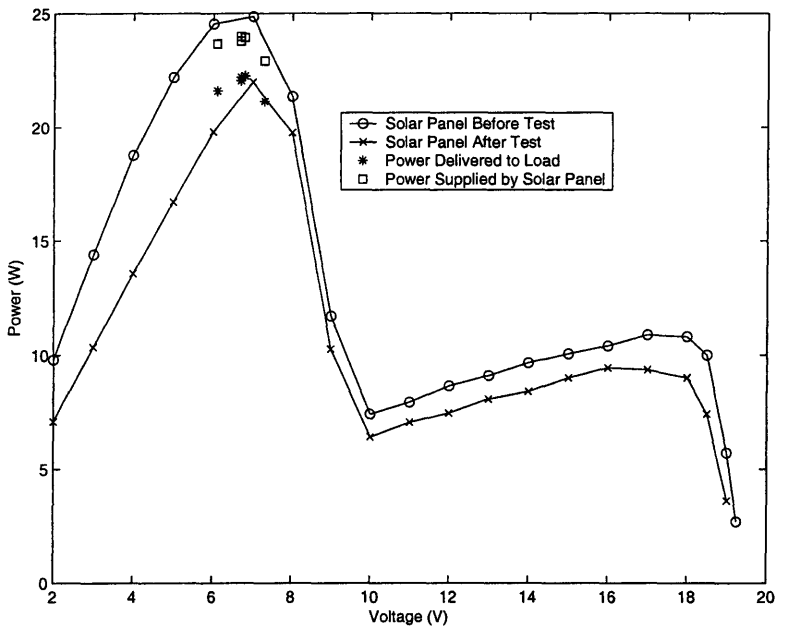

Figure 6-15: Converter input and output power vs. P-V curve of solar panel for different converter output voltages under partial shading

Chapter 7

Conclusions

7.1 Summary

A maximum power point tracking DC-DC converter has been described, implemented in circuitry, and tested. The converter is capable of finding the true global maximum power point, even in the presence of other local power maxima. It does this by utilizing two algorithms – a global search algorithm which moves the operating point close to the true global peak, and a local dithering algorithm which zeroes in on the actual maximum.

In contrast to previous work, this is all accomplished without the use of costly components such as analog-to-digital converters and microprocessors. The global search algorithm incorporates a unique method of finding the true maximum. The operating point is swept over its entire range while peak power is recorded. A second sweep of the operating point is then initiated, with the algorithm holding the operating point once power returns to the peak level recorded in the first sweep. The local dithering algorithm operates in discrete time with quantized values, eliminating the need for a very costly (if not impossible) continuous time filter. This also greatly simplifies the implementation circuitry.

The algorithms could easily be implemented in an integrated circuit with only minimal changes in the implementation. An integrated circuit would offer the increased benefit of more control over the specifications of individual components, greatly sim-

plifying some of the issues present in the printed circuit board prototype.

Testing was performed both with an artificial source and with a solar panel source. The artificial source was designed to be variable and have a maximum power point. The solar panel was used both in full sun for a single maximum power point, and in partial shading for multiple local maxima. In all cases, the converter tracked close to the maximum power point over a wide range of output voltages. In the case of partial shading, it accurately operated at the global maximum despite the presence of other local maxima.

Over all input and output operating points where the converter tracked correctly, system efficiency remained above 93%. In the best case, efficiency increased to 94.7%.

Given that the converter is tracking correctly to the true global maximum power point, delivering at least 93% of maximum power to the load is a very worthwhile improvement over direct connection schemes where power could drop to below 10% of maximum in the case of partial shading. Even under full sun with typical connection to battery stacks, power delivered may not exceed 70% of maximum.

7.2 Future Work

This thesis focused on validating one implementation of the algorithms described in Chapter 2. While Section 7.1 explained several ways in which this implementation uniquely solves key problems, specific component values and timing have not been optimized.

Furthermore, integration into an integrated circuit would allow full customization to raise efficiency levels beyond what was achieved here.

Adding a multiplier to measure true output power would extend the loads that the converter is capable of driving to include those with non-positive incremental impedance. Additionally, the sense resistor used to measure output current suffers from a tradeoff between efficiency and versatility. If the sense resistor is made small to maximize efficiency, it may work well when light levels are high and the solar panel is capable of supplying a large amount of power. However, if light levels drop and the

panel can only deliver 25% of what it can deliver in strong sunlight, the small sense resistor may not generate a large enough signal. If the sense resistor is made four times larger to accommodate these lower power levels, losses due to the sense resistor unnecessarily increase proportionally at higher light levels.

Appendix A

Full Schematic for Prototype Board

The full schematic for the circuitry is shown in Figures A-1 and A-2. Figure A-1 shows page 1 of the schematic. Figure A-2 shows page 2. These schematics are identical to the final prototype board except that the board has bypass capacitors locally connected to each package's power pin.

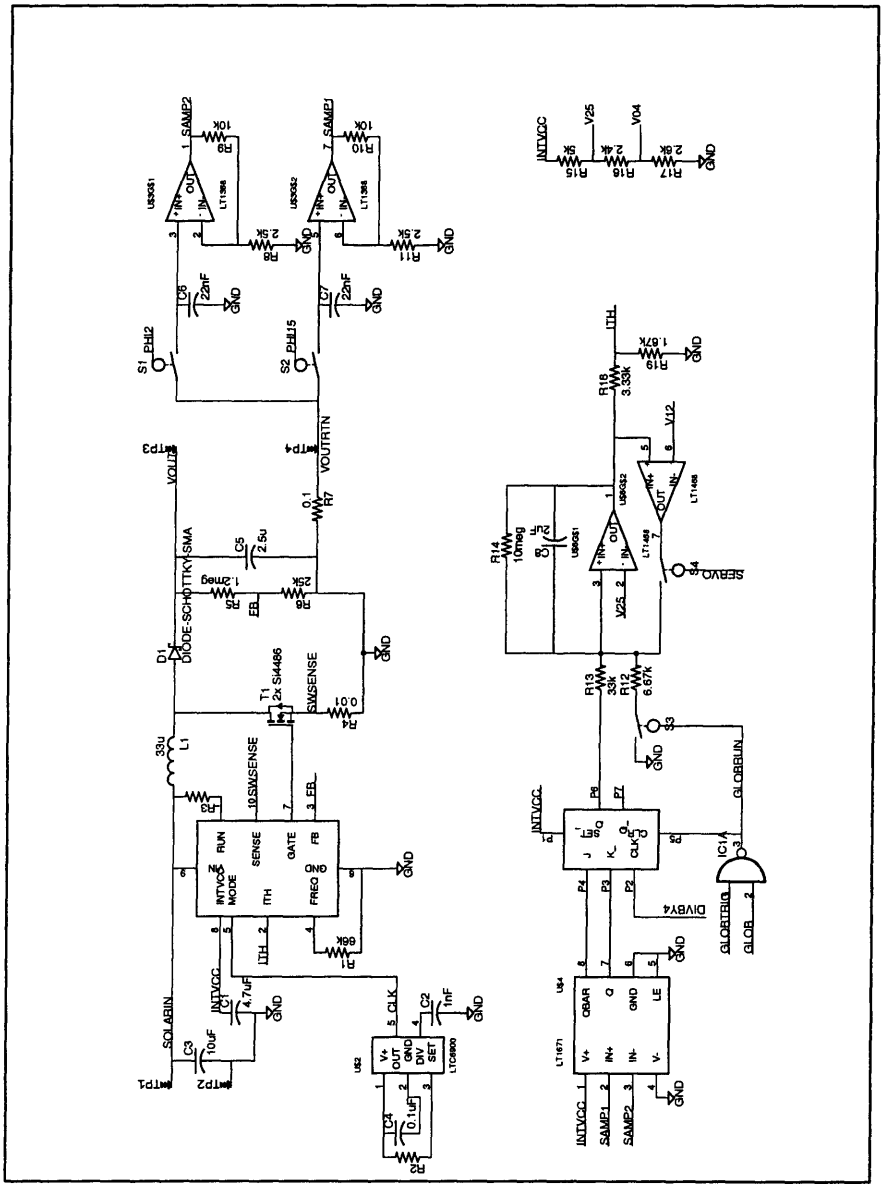

Figure A-1: Full Circuit Schematic Page 1

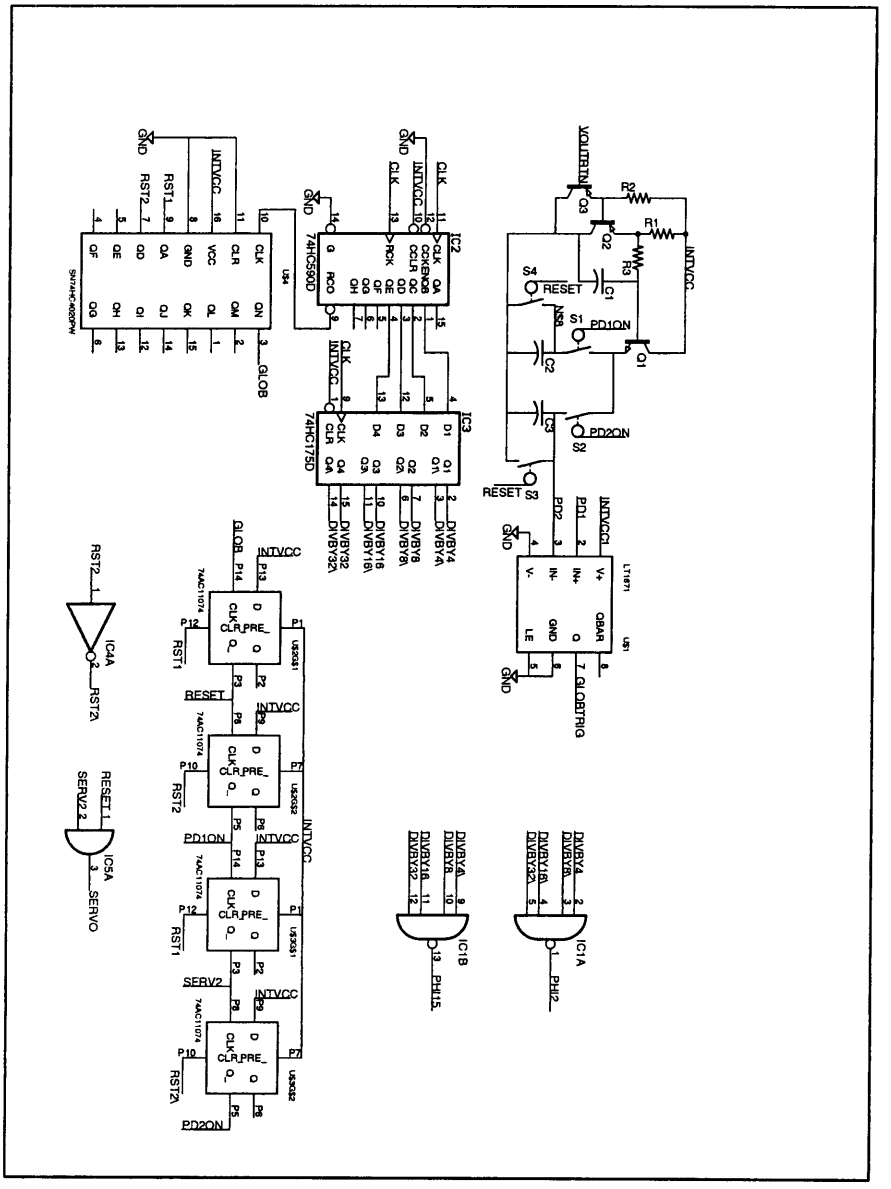

Figure A-2: Full Circuit Schematic Page 2

Appendix B

Complete Testing Data

B.1 Indoor Testing

V_{in}	I_{in}	P_{in}	V_{out}	I_{out}	P_{out}	*Efficiency*
14.9	2.05	30.5	16	1.74	27.8	91.1%
11.3	3.15	35.6	18	1.84	33.1	93.0%
11.9	2.98	35.5	20	1.65	33.0	93.1%
12.4	2.84	35.2	22	1.49	32.8	93.1%
12.7	2.74	34.8	24	1.35	32.4	93.1%
12.5	2.79	34.9	26	1.25	32.5	93.2%
11.8	3.03	35.8	28	1.19	33.3	93.2%
11.4	3.16	36.0	30	1.12	33.6	93.3%
11.2	3.2	35.8	32	1.05	33.6	93.8%
11.1	3.25	36.1	34	0.99	33.7	93.3%
11.1	3.27	36.3	36	0.94	33.8	93.2%
11.1	3.27	36.3	38	0.89	33.8	93.2%
11	3.28	36.1	40	0.84	33.6	93.1%
11	3.28	36.1	42	0.8	33.6	93.1%
10.9	3.3	36.0	44	0.76	33.4	93.0%
11.5	3.09	35.5	46	0.72	33.1	93.2%
19.3	0.64	12.4	48	0.24	11.5	93.3%

Table B.1: Input and Output Power vs. Vout for Vs = 21.4V and Rs = 3.16 ohms

V_{in}	I_{in}	P_{in}	V_{out}	I_{out}	P_{out}	*Efficiency*
18	4.04	72.7	30	2.26	67.8	93.2%
17.9	4.09	73.2	35	1.95	68.3	93.2%
16.7	4.45	74.3	40	1.74	69.6	93.7%
16.4	4.54	74.5	45	1.55	69.8	93.7%
16.4	4.54	74.5	50	1.39	69.5	93.3%
26.9	1.23	33.1	55	0.52	28.6	86.4%

Table B.2: Input and Output Power vs. Vout for Vs = 30.85V and Rs = 3.18 ohms

V_{in}	I_{in}	P_{in}	V_{out}	I_{out}	P_{out}	*Efficiency*
18	4.04	72.7	30	2.26	67.8	93.2%
17.9	4.09	73.2	35	1.95	68.3	93.2%
16.7	4.45	74.3	40	1.74	69.6	93.7%
16.4	4.54	74.5	45	1.55	69.8	93.7%
16.4	4.54	74.5	50	1.39	69.5	93.3%
26.9	1.23	33.1	55	0.52	28.6	86.4%

Table B.3: Input and Output Power vs. Vout for Vs = 31.1V and Rs = 6.16 ohms

V_{in}	I_{in}	P_{in}	V_{out}	I_{out}	P_{out}	*Efficiency*
21.7	3.19	69.2	35	1.87	65.5	94.5%
23.1	2.97	68.6	40	1.62	64.8	94.5%
23.9	2.84	67.9	45	1.42	63.9	94.1%
23.1	2.98	68.8	50	1.3	65.0	94.4%
22	3.14	69.1	55	1.19	65.5	94.7%
21.7	3.19	69.2	60	1.09	65.4	94.5%

Table B.4: Input and Output Power vs. Vout for Vs = 41.5V and Rs = 6.16 ohms

V_{in}	I_{in}	P_{in}	V_{out}	I_{out}	P_{out}	*Efficiency*
32.6	3.01	98.1	35	2.64	92.4	94.2%
29.6	3.47	102.7	40	2.42	96.8	94.2%
28.1	3.73	104.8	45	2.19	98.6	94.0%
28.9	3.62	104.6	50	1.97	98.5	94.2%
30.2	3.39	102.4	55	1.74	95.7	93.5%
28.9	3.6	104.0	60	1.62	97.2	93.4%

Table B.5: Input and Output Power vs. Vout for Vs = 51.2V and Rs = 6.16 ohms

V_s	V_{in}
10.94	5.55
15.12	7.55
20.65	10.6
25.04	13.1
30.02	16.1
35	19.9

Table B.6: Vin vs. Vs for Vout = 40V, Rs = 3.18 ohms

V_s	V_{in}
10.47	5
15.07	7.72
20.06	10.55
25.02	15.1
30.19	17.55
35.02	27.3

Table B.7: Vin vs. Vs for Vout = 30V, Rs = 3.18 ohms

V_s	V_{in}
20.16	10.23
25.16	12.92
30.95	16.83
35.1	19.4
40.77	22.3
45.6	24.8

Table B.8: Vin vs. Vs for Vout = 40V, Rs = 6.18 ohms

V_s	V_{in}
20.01	16.71
25	20.8
30.23	15.5
35.41	17.64
40.06	22.1
45.2	26.7

Table B.9: Vin vs. Vs for Vout = 50V, Rs = 6.18 ohms

B.2 Outdoor Testing

B.2.1 Full Sun

V_{load}	I	P
2	5.47	10.94
3	5.45	16.35
4	5.39	21.56
5	5.32	26.6
6	5.27	31.62
7	5.2	36.4
8	5.12	40.96
9	5.02	45.18
10	4.9	49
11	4.8	52.8
12	4.65	55.8
13	4.47	58.11
14	4.24	59.36
15	3.94	59.1
16	3.53	56.48
17	3	51
18	2.27	40.86
19	1.34	25.46
19.25	1.02	19.635
19.5	0.75	14.625
19.75	0.44	8.69
20	0.19	3.8

Table B.10: Solar Panel Characteristics Before Testing in Full Sun

V_{load}	I	P
2	5.4	10.8
4	5.22	20.88
6	5.12	30.72
8	5	40
10	4.8	48
12	4.6	55.2
14	4.22	59.08
15	3.94	59.1
16	3.55	56.8
17	3.02	51.34
18	2.32	41.76
19	1.4	26.6
19.25	1.1	21.175
19.5	0.84	16.38
19.75	0.54	10.665
20	0.22	4.4

Table B.11: Solar Panel Characteristics After Testing in Full Sun

V_{load}	I_{out}	P_{out}	V_{in}	I_{in}	P_{in}	*Efficiency*
25	2.27	56.75	15.4	3.9	60.06	94.5%
30	1.92	57.6	15.5	3.9	60.45	95.3%
35	1.62	56.7	14.9	4.04	60.196	94.2%
40	1.47	58.8	15.1	4.13	62.363	94.3%
45	1.25	56.25	14.7	4.08	59.976	93.8%
50	1.12	56	14.7	4.09	60.123	93.1%
55	1	55	15.04	3.92	58.9568	93.3%

Table B.12: Input and Output Power from Converter when Connected to Solar Panel in Full Sun

B.2.2 Partial Shading

V_{load}	I	P
2	4.9	9.8
3	4.8	14.4
4	4.69	18.76
5	4.44	22.2
6	4.09	24.54
7	3.55	24.85
8	2.67	21.36
9	1.3	11.7
10	0.74	7.4
11	0.72	7.92
12	0.72	8.64
13	0.7	9.1
14	0.69	9.66
15	0.67	10.05
16	0.65	10.4
17	0.64	10.88
18	0.6	10.8
18.5	0.54	9.99
19	0.3	5.7
19.25	0.14	2.695

Table B.13: Solar Panel Characteristics Before Testing in Partial Shade

V_{load}	I	P
2	3.54	7.08
3	3.45	10.35
4	3.39	13.56
5	3.34	16.7
6	3.3	19.8
7	3.14	21.98
8	2.47	19.76
9	1.14	10.26
10	0.64	6.4
11	0.64	7.04
12	0.62	7.44
13	0.62	8.06
14	0.6	8.4
15	0.6	9
16	0.59	9.44
17	0.55	9.35
18	0.5	9
18.5	0.4	7.4
19	0.19	3.61

Table B.14: Solar Panel Characteristics After Testing in Partial Shade

V_{load}	I_{out}	P_{out}	V_{in}	I_{in}	P_{in}	*Efficiency*
40	0.54	21.6	6.1	3.88	23.668	91.3%
30	0.74	22.2	6.7	3.58	23.986	92.6%
25	0.89	22.25	6.8	3.52	23.936	93.0%
35	0.63	22.05	6.7	3.55	23.785	92.7%
45	0.47	21.15	7.3	3.14	22.922	92.3%

Table B.15: Input and Output Power from Converter when Connected to Solar Panel in Partial Shading

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