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Hart Modem
HT2015
Application Note

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- Reference Connection Diagrams for Typical HT2015 Design
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- Medium Attachment Unit (MAU) Analog Interfacing
- Clock Interfacing
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General Description

The purpose of this document is to detail an example of a typical design using the HT2015. This reference design will provide greater understanding as to how the HT2015 interfaces and functions in a typical HART device. To fully understand the HT2015 this guide should be used in conjunction with the *HT2015 Datasheet* that can be found on the Smar Research website: http://www.SmarResearch.com.

The reference design explained in this application note was selected to showcase a typical design using the HT2015. While specific needs and medium requirements will vary between actual applications, the concepts and strategies described here cover the basic concepts necessary to implement a control system design based on the HT2015. In the pages to follow, specific interconnection, and circuit diagrams are included and explained.

The HT2015 is a single-chip mixed signal CMOS modem for use in Highway Addressable Remote Transducer (HART) field instruments and masters. Combined with a UART and a few external passive components, the HT2015 provides all of the functions needed to satisfy the HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect and transmit-signal shaping. The HT2015 is pin-compatible with the industry standard SYM20C15 and A5191.

The HT2015 HART Modem conforms to the HART Communication Foundation Physical Layer Specification. Thus, the internal analog and digital circuitry contained in the HT2015 is designed to integrate into a HART compliant design. A sample of the passive receive filter components and other external circuitry needed to complete the medium interface is provided in the following pages.

A generic HART application is shown in the block diagram below. It should be noted that much of the external analog circuitry will be highly dependent on the device power and isolation requirements, and thus is only generally described. This document does not discuss the control of the HART line current for slave devices, or driving the line with voltage, in the case of some master devices. These topics are left up to the developer. For in depth discussion on the input and output requirements of a HART compliant device, refer to the HART Foundation Physical Layer Specification. The HT2015 is designed to fall within all applicable HART physical layer specifications. Each section of Figure one will be discussed in detail in the following sections.

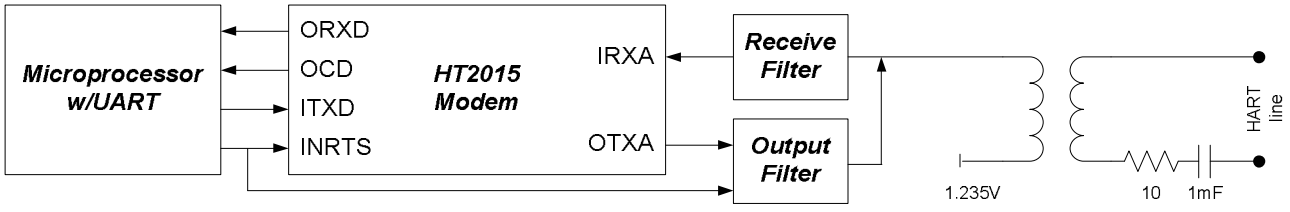

Figure 1 - Typical HT2015 HART Device Block Diagram

The design of a HART device using the HT2015 will be separated into three topics. The following topics will be discussed including reference examples whenever applicable:

- *Clocks*
- *Microcontroller Interfacing*
- *Medium Interfacing*

Clocks

In order for the HT2015 to function properly, the oscillator must be chosen and set up carefully. The HT2015 requires a 460.8 kHz clock signal on OXTL. This can be provided by an external clock or you may connect external components to the HT2015 internal oscillator.

Internal Oscillator Option
The oscillator cell will function with either a 460.8 kHz crystal or ceramic resonator. A parallel resonant ceramic resonator can be connected between OXTL and IXTL. Figure 2 illustrates the crystal option for clock generation using a 460.8 kHz parallel resonant crystal and two tuning capacitors. The actual values of the capacitors may depend on the recommendations of the manufacturer of the resonator. Typically, capacitors in the range of 100 pF to 470 pF are used.

Finding an oscillator at the frequency of 460.8KHz can be difficult. We recommend using the Toko BP11DCRK455 455KHx ceramic resonator. This oscillator has been proven to work successfully with many HT2015 designs.

External Clock Option
It may be desirable to use an external 460.8 kHz clock as shown in Figure 3 rather than the internal oscillator because of the high cost and low availability of ceramic resonators. It may be desirable to use the microprocessor clock or a division of it for this input. In addition, the HT2015 consumes less current when an external clock is used. Minimum current consumption occurs with the clock connected to OXTL and IXTL connected to V_{SS}.

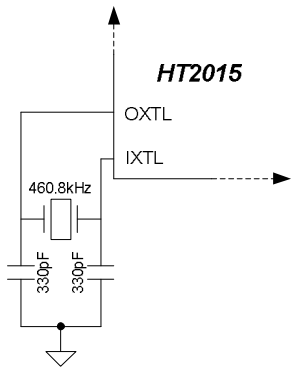

Figure 2 - Crystal Oscillator Clock Circuit

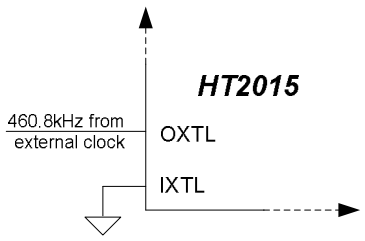

Figure 3 - External Clock Circuit

Microcontroller Interfacing

The HT2015 can interface to any microcontroller with a standard RS-232 UART or to any standalone UART. For the purposes of this document, we will discuss a microprocessor with an internal UART. The microcontroller interfacing consists of four connections: ORXD, ITXD, OCD and INRTS. Because the ITXD and ORXD pins accept and transmit standard RS-232 signals, interfacing to the UART is straightforward.

ORXD & ITXD
ORXD outputs the digital receive data from the demodulator and should be connected to the RX pin of the UART. ITXD is an input that accepts digital data in NRZ form to be modulated and sent to the HART line. ITXD should be connected to the TX pin of the UART. For both ORXD and ITXD a 1200Hz HART signal corresponds to logic level high and a 2200Hz HART signal corresponds to logic level low.

OCD
This signal outputs the carrier detect signal to the UART. OCD should be connected to the carrier detect (CD) input of the UART. OCD is high when a valid input is recognized on IRXA. This signal is used to notify the UART of a valid incoming message. The level at which OCD becomes active is determined by the DC voltage difference between ICDREF and IAREF. The selection of these values is discussed further in the Medium Interfacing section of this document. OCD is generally set to detect a nominal 100mV peak-to-peak signal. OCD is compliant with the HART Physical Layer Specification which requires the receiver to activate the carrier detect between the incoming signals levels of 80 and 120 mV peak-to-peak. The purpose of OCD is to indicate to the receiver that there is a sufficient signal to decode. OCD is not to be used to indicate the start or end of a particular frame. Start of frame detection is a HART specified Data Link Layer function and must occur by examination of the frame content.

INRTS
INRTS should be connected to the Request To Send (RTS) signal of the UART. INRTS is an active low signal that enables the internal modulator of the HT2015. When the microprocessor wishes to send a message, INRTS will become active-low, which in turn will enable the modulator and output the modulated signal to the OTXA pin.

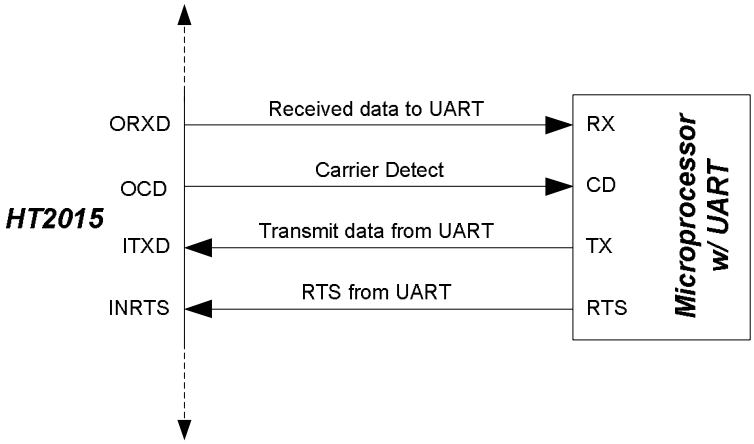

Figure 4 - Microprocessor Interface

Medium Interfacing - MAU

The HT2015 contains much of the medium attachment unit internally. However, due to the large size of the capacitors required and cost/value ratio of manufacturing, a few components must be added externally to complete the design. The medium attachment unit can be split into 2 sections, the receiver circuitry and the output circuitry. These are both discussed in detail below. As stated earlier, the coupling of the device to the HART network follows the HART Physical Layer Specification and is left as an exercise for the user. For more information on the medium interface and HART interconnections refer to the HART Communication Foundation Physical Layer Specification or visit the HART Foundation website at http://www.hartcomm.org.

Receiver Circuitry

Receive Bandpass Filter

The HT2015 contains an active filter which attenuates the frequencies outside the HART specified band pass. This internal active filter must be combined with an external passive filter to meet the HART specification filtering requirements. These external components are shown below in Figure 5 and can also be seen in Figure 8 of the HT2015 Datasheet. As stated in the datasheet, the circled resistor values should be noted, as they are different from those used with the LSI20C15 or AMI A5191HRT. These different values are attributed to differences in the internal designs of the receive filter and the manufacturing process.

Voltage References

In order for the HT2015 to function correctly, the voltage references IAREF and ICDREF must be set correctly. IAREF sets the DC operating point of the internal operational amplifiers and comparators. It should be set to split the DC potential between VDD and VSS and should be between 1.2 and 2.6 VDC. When using 3V for VDD, IAREF can use a 1.235 VDC reference such as the Texas Instrument LM335 or Analog Devices AD589.

The level at which the carrier detect (OCD) becomes active is determined by the DC voltage difference between ICDREF and IAREF. The goal is to select the correct voltage difference that will enable OCD when a HART compliant signal is input from the HART line. R9 in Figure 5 must be adjusted properly to work with the design of your particular circuit. In an ideal circuit, no attenuation would occur though the coupling circuit and the receiver circuit would receive the HART signal at 100mV p-p. However, in real world applications the incoming HART signal voltage to the external receiver circuit may be significantly lower due to attenuation by the coupling circuit. Because this attenuation will vary by design, it is recommended that R9 be adjusted specifically for your design. This can be accomplished by applying a HART compliant signal to your design at the HART line input. Any attenuation will occur through the coupling circuitry and R9 can be properly adjusted. The goal is to set R9 to a value where the minimum HART input signal desired enables OCD. This will ensure the circuit is properly tuned to your specific coupling circuitry and meets the desired level of signal detection.

The HT2015 requires a bias current resistor to be connected between OCBIAS and VSS to control the operating parameters of the internal op-amps and comparators. The recommended bias current resistor is 499 KOhm when IAREF is 1.235VDC. This value is determined by the reference voltage IAREF using the formula: $R_{BIAS} = \left(\frac{IAREF}{2.5\,\mu A}\right)$

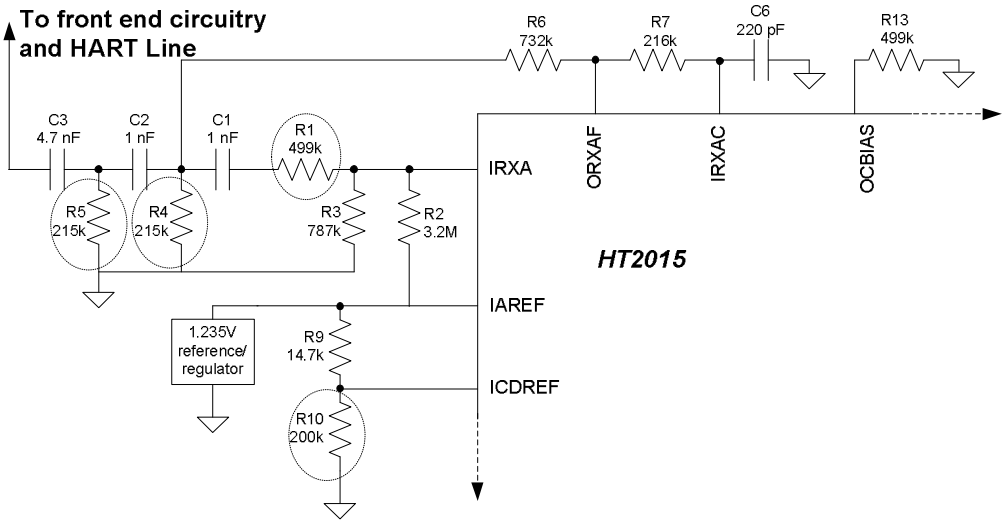

Figure 5 - Receiver Analog Circuitry

Output Circuitry

Output Wave Shaping Filter

The HT2015 contains an internal output wave shaping filter. This filter generates a HART compliant trapezoidal FSK modulated signal at the OTXA pin. The output wave shaping filter functions as a current to voltage modulator and smoothes transition edges to minimize spurious frequencies and harmonics over the transmission lines. This helps eliminate false triggers at the remote receiver due to noise centered on the transition threshold.

The HT2015 internal output wave shaper meets the HART specification requirements, however you may wish to add external components depending upon your application and design. For example, during a HART transmission from a Master Device, the output impedance of the voltage source is low. However, during reception of a HART message, the input impedance of the receive circuit must be high. Therefore the transmitter portion must be disabled when not active (INRTS = high). This can be seen in Figure 6.

The output amplitude of OTXA is nominally 500 mV peak-to-peak and meets the HART requirement. The additional output circuitry will vary largely dependant on the device type, Slave or Master.

For a slave device, the HART physical layer requires the device to modulate the loop with a 1mA peak-to-peak signal. The amplitude of modulation of the loop current must be adjusted before the amplifier in the current loop regulator or at the regulator itself. It is recommended to adjust the amplitude with voltage gain circuits in these Slave device applications.

For a Master device, the 500 mV peak-to-peak signal output at OTXA meets the HART requirements. However, the HT2015 cannot source enough current to drive a HART network. Because of this, it is recommended to add a low impedance voltage driver between the HT2015 OTXA pin and the HART network. An example of this can be seen on Figure 6 below. This external circuitry on OTXA is one of many solutions that will vary by the design requirements. Refer to the HART Specification for more details.

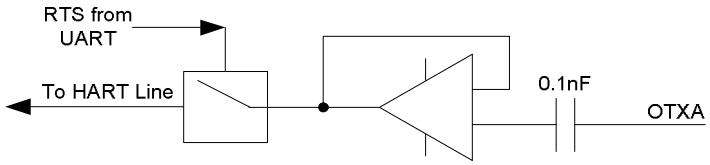

Figure 6 - Example External Output Circuitry

Summary

Combining the clock circuitry, receiver filter, output circuit and microprocessor connections discussed in the previous sections with simple power and ground connections yields a full example design. Figure 7 shows all these elements combined together into a functional example design. Following the guidelines of this application note combined with the HART specification, you will be well on your way to creating your specific design using the HT2015.

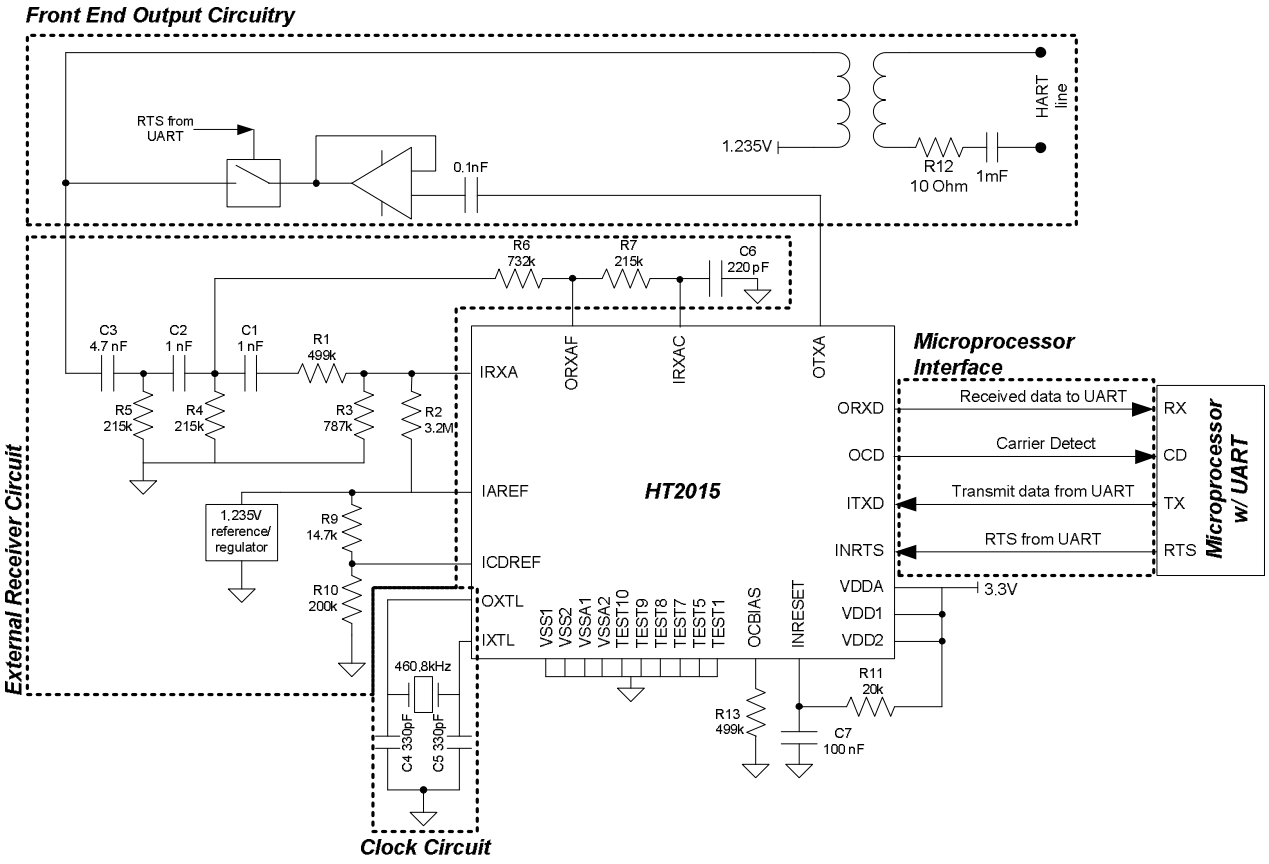

Figure 7 - Example HT2015 Application

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