DEVICE SPECIFICATION

TDA884X/5X-N2 series
I²C-bus controlled PAL/NTSC/SECAM TV processors

Tentative Device Specification

December 16, 1997

Previous version: April 24, 1997

PHILIPS

I²C-bus controlled PAL/NTSC/SECAM TV processors

TDA884X/5X-N2 series

FEATURES

The following features are available in all IC's:

- Multi-standard vision IF circuit with an alignment-free PLL demodulator without external components
- Alignment-free multi-standard FM sound demodulator (4.5 MHz to 6.5 MHz)
- Audio switch
- Flexible source selection with CVBS switch and Y(CVBS)/C input so that a comb filter can be applied
- Integrated chrominance trap circuit
- Integrated luminance delay line
- Asymmetrical peaking in the luminance channel with a (defeatable) noise coring function
- Black stretching of non-standard CVBS or luminance signals
- Integrated chroma band-pass filter with switchable centre frequency
- Dynamic skin tone control circuit
- Blue stretch circuit which offsets colours near white towards blue
- RGB control circuit with "Continuous Cathode Calibration" and white point adjustment
- Possibility to insert a "blue back" option when no video signal is available
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimised for DC-coupled vertical output stages
- I²C-bus control of various functions

The detailed differences between the various IC's are given in the table on page 3.

GENERAL DESCRIPTION

The various versions of the TDA 884X/5X series are I²C-bus controlled single chip TV processors which are intended to be applied in PAL, NTSC, PAL/NTSC and multi-standard television receivers. The N2 version is pin and application compatible with the N1 version, however, a new feature has been added which makes the N2 more attractive. The IF PLL demodulator has been replaced by an alignment-free IF PLL demodulator with internal VCO (no tuned circuit required). The setting of the various frequencies (33.4, 33.9, 38, 38.9, 45,75 and 58.75 MHz) can be made via the I²C-bus.

Because of this difference the N2 version is compatible with the N1, however, N1 devices cannot be used in an optimised N2 application.

Functionally the IC series is split up is 3 categories, viz:

- Versions intended to be used in economy TV receivers with all basic functions (envelope: S-DIP 56 and QFP 64)
- Versions with additional features like E-W geometry control, H-V zoom function and YUV interface which are intended for TV receivers with 110° picture tubes (envelope: S-DIP 56)
- Versions which have in addition a second RGB input with saturation control and a second CVBS output (envelope: QFP 64)

The various type numbers are given in the table below.

SURVEY OF IC TYPES

ENVELOPE	S-DIP 56		QFP 64	
TV receiver category	Economy	Mid/High end	Economy	Mid/High end
PAL only	TDA 8840		TDA 8840H	
PAL/NTSC	TDA 8841	TDA 8843	TDA 8841H	
PAL/SECAM/NTSC	TDA 8842	TDA 8844	TDA 8842H	TDA 8854H
NTSC only	TDA 8846/46A	TDA 8847		TDA 8857H

FUNCTIONAL DIFFERENCES BETWEEN THE VARIOUS IC VERSIONS

IC VERSION (TDA)	8840	8841	8842	8846	8846A	8843	8844	8847	8854H	8857H
Automatic Volume Limiting	X	X	X	X	X					
PAL decoder	X	X	X			X	X		X	
SECAM decoder			X				X		X	
NTSC decoder		X	X	X	X	X	X	X	X	X
Colour matrix PAL/NTSC(Japan)		X	X			X	X		X	
Colour matrix NTSC Japan/USA				X	X			X		X
YUV interface				X	X	X	X	X	X	X
Base-band delay line for PAL and SECAM or chroma comb filter for NTSC	X	X	X		X	X	X		X	
Adjustable luminance delay time						X	X	X	X	X
Horizontal geometry						X	X	X	X	X
Horizontal and vertical zoom						X	X	X	X	X
Vertical scroll						X	X	X	X	X
2nd CVBS output									X	X

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage	–	8.0	–	V
I_P	supply current	–	110	–	mA
Input voltages					
$V_{iVIFrms)}$	video IF amplifier sensitivity (RMS value)	–	35	–	μV
$Vi_{SIF(rms)}$	sound IF amplifier sensitivity (RMS value)	–	1.0	–	mV
$V_{iAUDIO(rms)}$	external audio input (RMS value)	–	350	–	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	–	1.0	–	V
$V_{iCHROMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
Output signals					
$V_{oCVBS(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.2	–	V
I_{oTUNER}	tuner AGC output current range	0	–	5	mA
$V_{oVIDSW(p-p)}$	CVBS1/CVBS2 output voltage of video switch (peak-to-peak value)	–	2.0/1.0	–	V
$V_{oB-Y(p-p)}$	–(R–Y) output/input voltage (peak-to-peak value)	–	1.05	–	V
$V_{oR-Y(p-p)}$	–(B–Y) output/input voltage (peak-to-peak value)	–	1.33	–	V
$V_{oY(p-p)}$	Y output/input voltage (peak-to-peak value)	–	1.4	–	V
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	2.0	–	V
I_{oHOR}	horizontal output current	10	–	–	mA
I_{oVERT}	vertical output current (peak-to-peak value)	–	1	–	mA
I_{oEW}	EW drive output current	1.2	–	–	mA

BLOCK DIAGRAMS

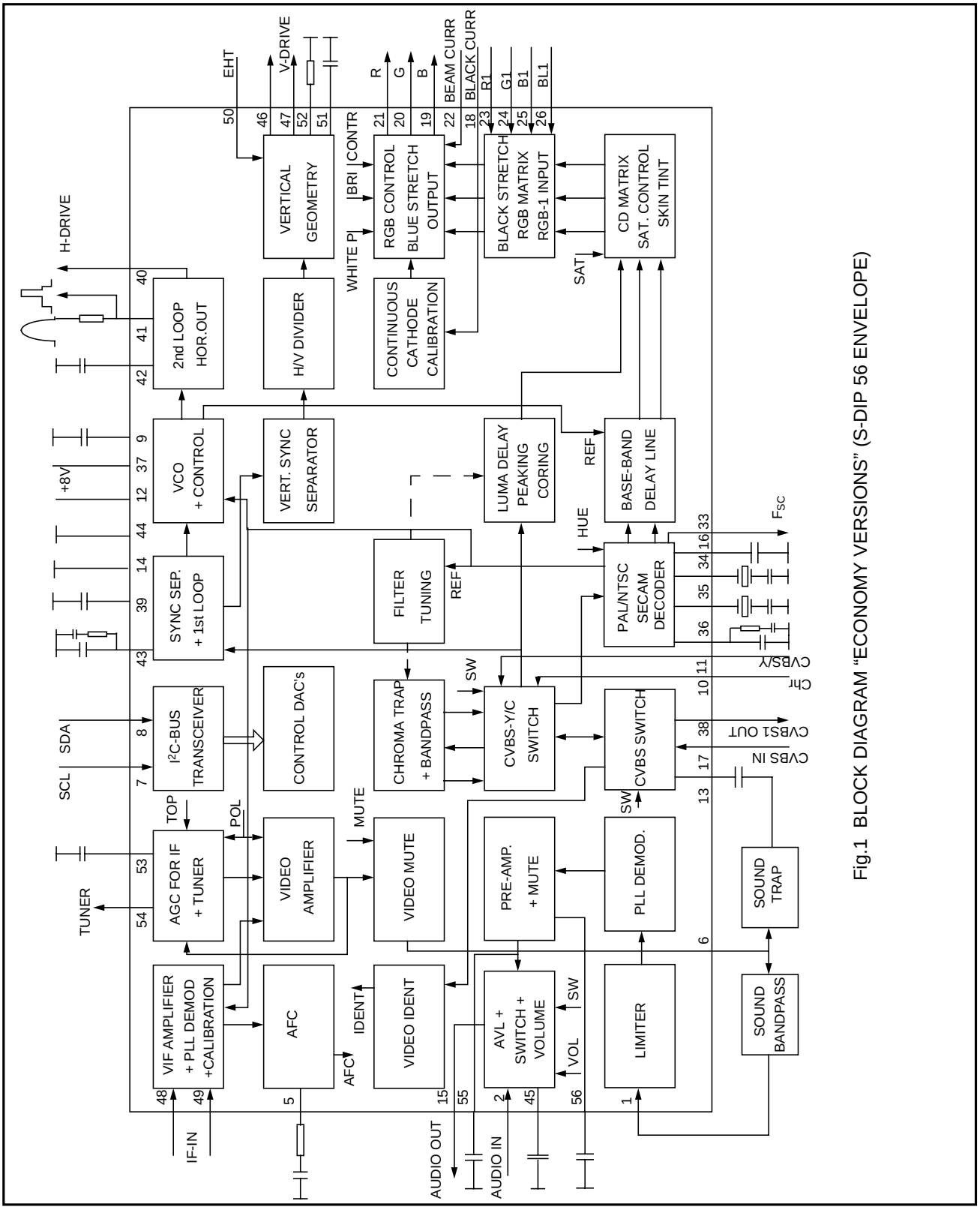


Fig.1 BLOCK DIAGRAM "ECONOMY VERSIONS" (S-DIP 56 ENVELOPE)

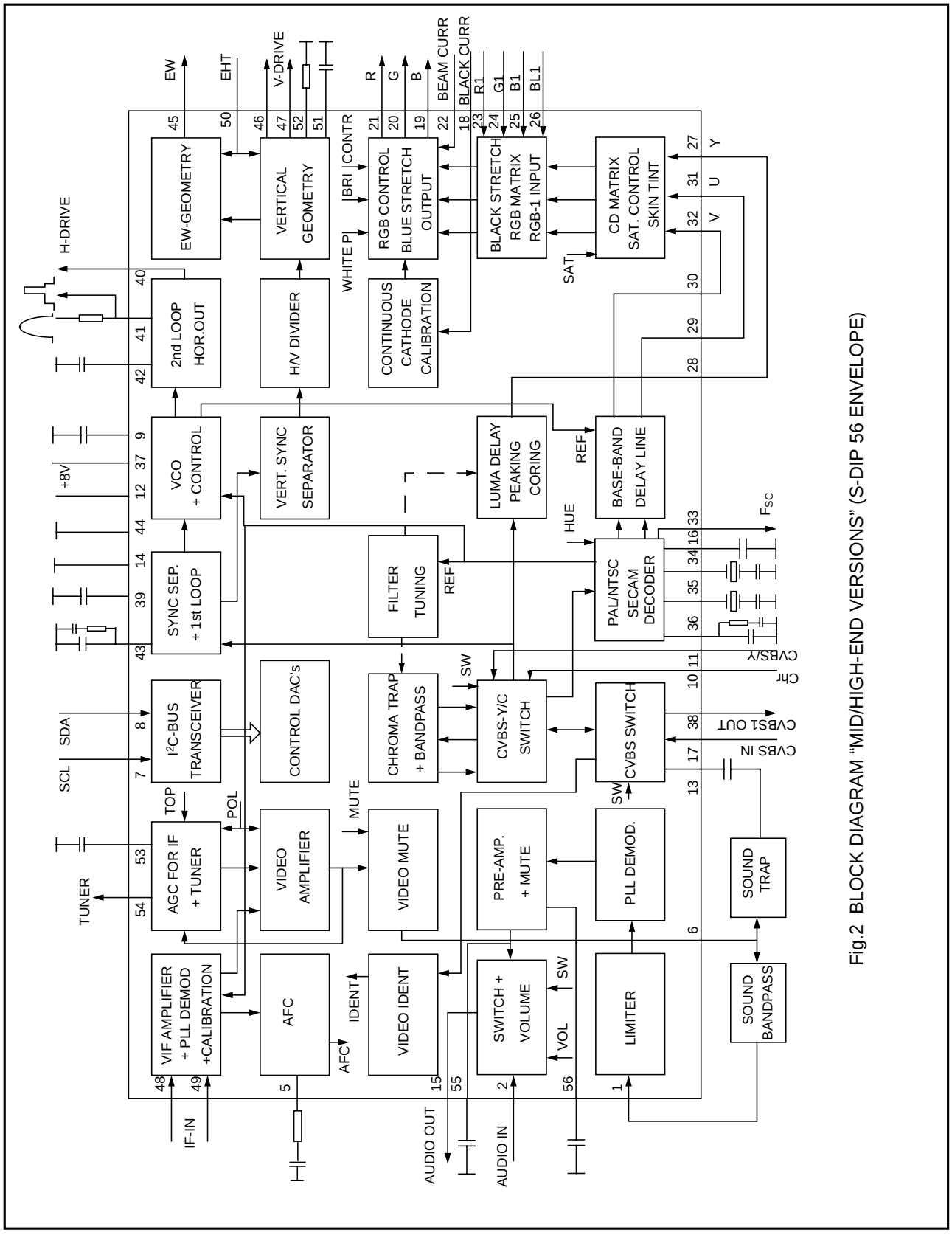


Fig.2 BLOCK DIAGRAM "MID/HIGH-END VERSIONS" (S-DIP 56 ENVELOPE)

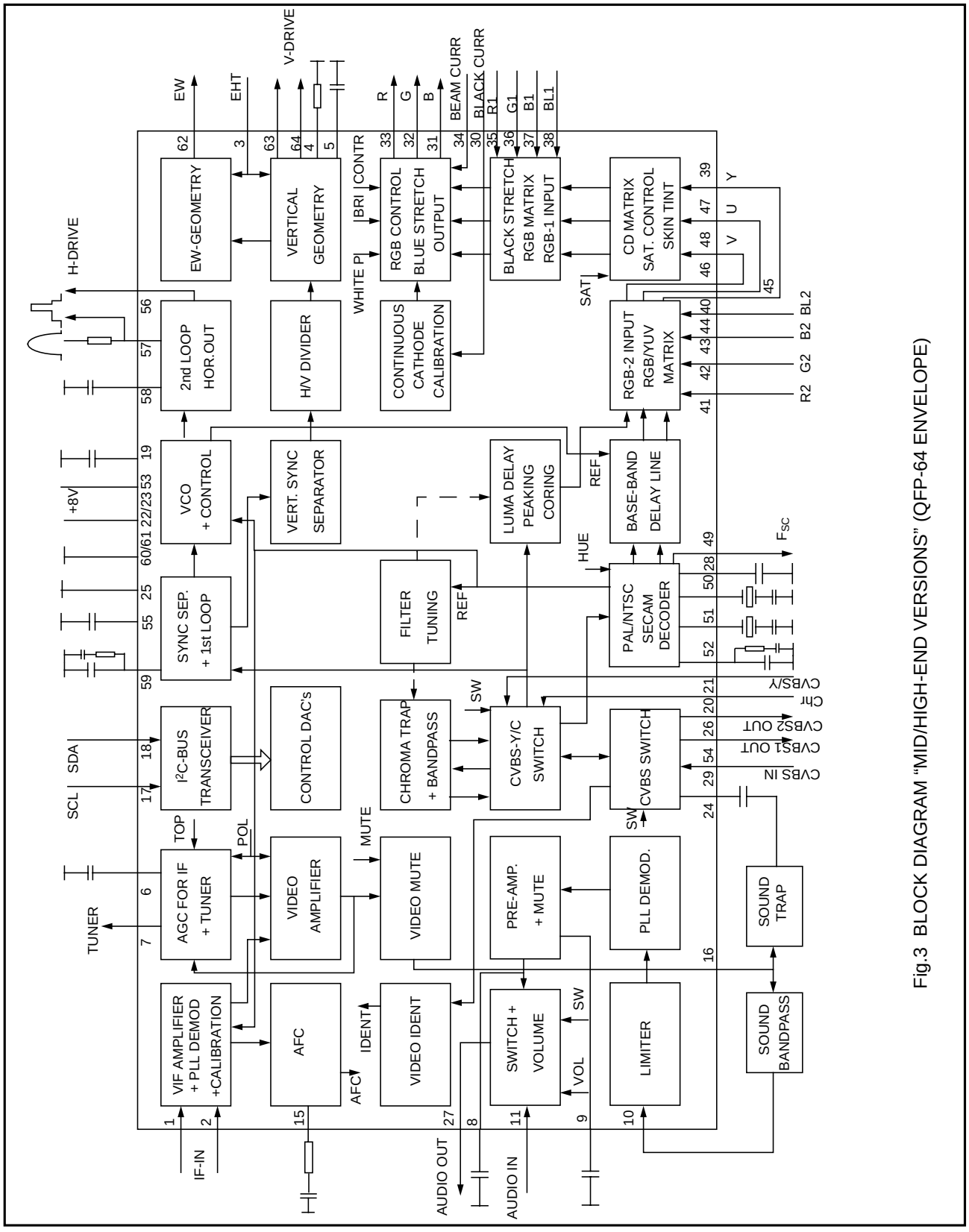


Fig.3 BLOCK DIAGRAM "MID/HIGH-END VERSIONS" (QFP-64 ENVELOPE)

PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP56	QFP64	
SNDIF	1	10	Sound IF input
AUDIOEXT	2	11	External audio input
NC	3	13	not connected
NC	4	14	not connected
PLLLF	5	15	IF-PLL loop filter
IFVO	6	16	IF video output
SCL	7	17	serial clock input
SDA	8	18	serial data input/output
DEC_{BG}	9	19	bandgap decoupling
CHROMA	10	20	chrominance input (S-VHS)
CVBS/Y	11	21	external CVBS/Y input
V_{P1}	12	22	main supply voltage 1 (+8 V)
$CVBS_{INT}$	13	24	internal CVBS input
GND1	14	25	ground 1
AUDIOOUT	15	27	audio output
SECPLL	16	28	SECAM PLL decoupling
$CVBS_{EXT}$	17	29	external CVBS input
BLKIN	18	30	black-current input
BO	19	31	blue output
GO	20	32	green output
RO	21	33	red output
BCLIN	22	34	beam current limiter input/V-guard input
RI	23	35	red input for insertion
GI	24	36	green input for insertion
BI	25	37	blue input for insertion
RGBIN	26	38	RGB insertion input
LUMIN	27	39	luminance input
LUMOUT	28	40	luminance output
BYO	29	45	(B–Y) signal output
RYO	30	46	(R–Y) signal output
BYI	31	47	(B–Y) signal input
RYI	32	48	(R–Y) signal input
REFO	33	49	subcarrier reference output
XTAL1	34	50	3.58 MHz crystal connection
XTAL2	35	51	4.43/3.58 MHz crystal connection
DET	36	52	loop filter phase detector
V_{P2}	37	53	2nd supply voltage 1(+8 V)
CVBS1O	38	54	CVBS-1 output

SYMBOL	PIN		DESCRIPTION
	SDIP56	QFP64	
DECDIG	39	55	Decoupling digital supply
HOUT	40	56	horizontal output
FBISO	41	57	flyback input/sandcastle output
PH2LF	42	58	phase-2 filter
PH1LF	43	59	phase-1 filter
GND2	44	60	ground 2
EWD	45	62	east-west drive output
VDRB	46	63	vertical drive B output
VDRA	47	64	vertical drive A output
IFIN1	48	1	IF input 1
IFIN2	49	2	IF input 2
EHTO	50	3	EHT/overvoltage protection input
VSC	51	4	vertical sawtooth capacitor
I_{ref}	52	5	reference current input
DEC_{AGC}	53	6	AGC decoupling capacitor
AGCOUT	54	7	tuner AGC output
AUDEEM	55	8	Audio deemphasis
DECSDEM	56	9	Decoupling sound demodulator
n.c.	–	12	not connected
VP3	–	23	Main supply voltage 2 (+8V)
CVBS2O	–	26	CVBS-2 output
RI2	–	41	2nd R input
GI2.	–	42	2nd G input
BI2	–	43	2nd B input
RGBIN2	–	44	2nd RGB insertion input
GND3	–	61	ground 3

The pin numbers mentioned in the rest of this document are referenced to the SDIP56 (SOT400) package.

In the TDA 8840/41/42/46/46A the following pins are different:

Pin 16 (SECAM PLL decoupling): Not connected in the TDA 8840/41/46/46A

Pin 27: Not connected in TDA 8840/41/42

Pin 28: Luminance output in TDA 8840/41/42

Pin 29-32 (U/V interface): Not available in TDA 8840/41/42

Pin 35 (4.43 MHz X-tal): Not connected in the TDA 8846/46A

Pin 45 (E-W drive output): AVL capacitor

In the TDA 8857H the pins 28 (SECAM PLL decoupling) and 51 (4.43 MHz X-tal) are not connected.

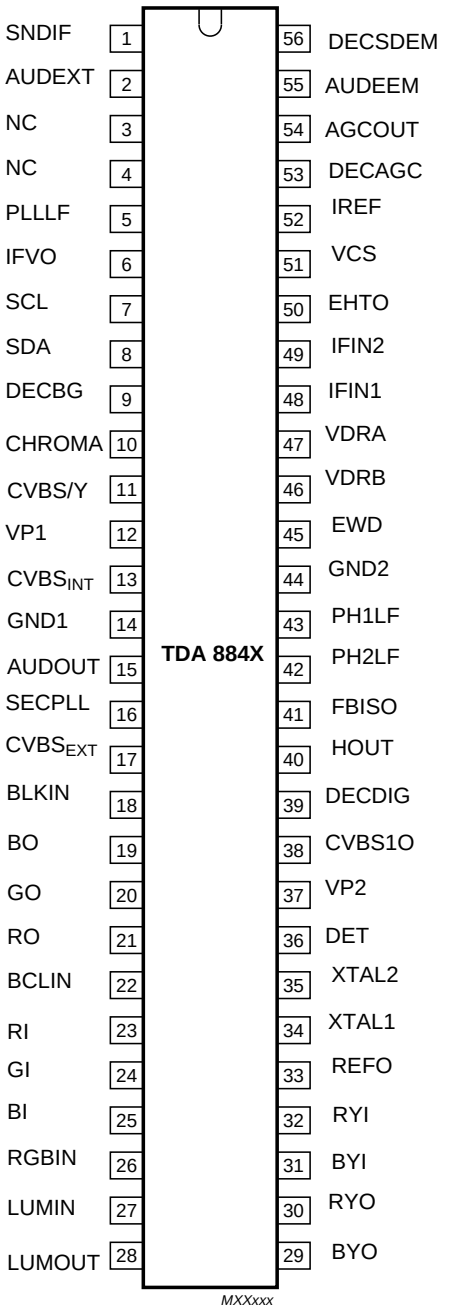


Fig.4 Pin configuration (SDIP56).

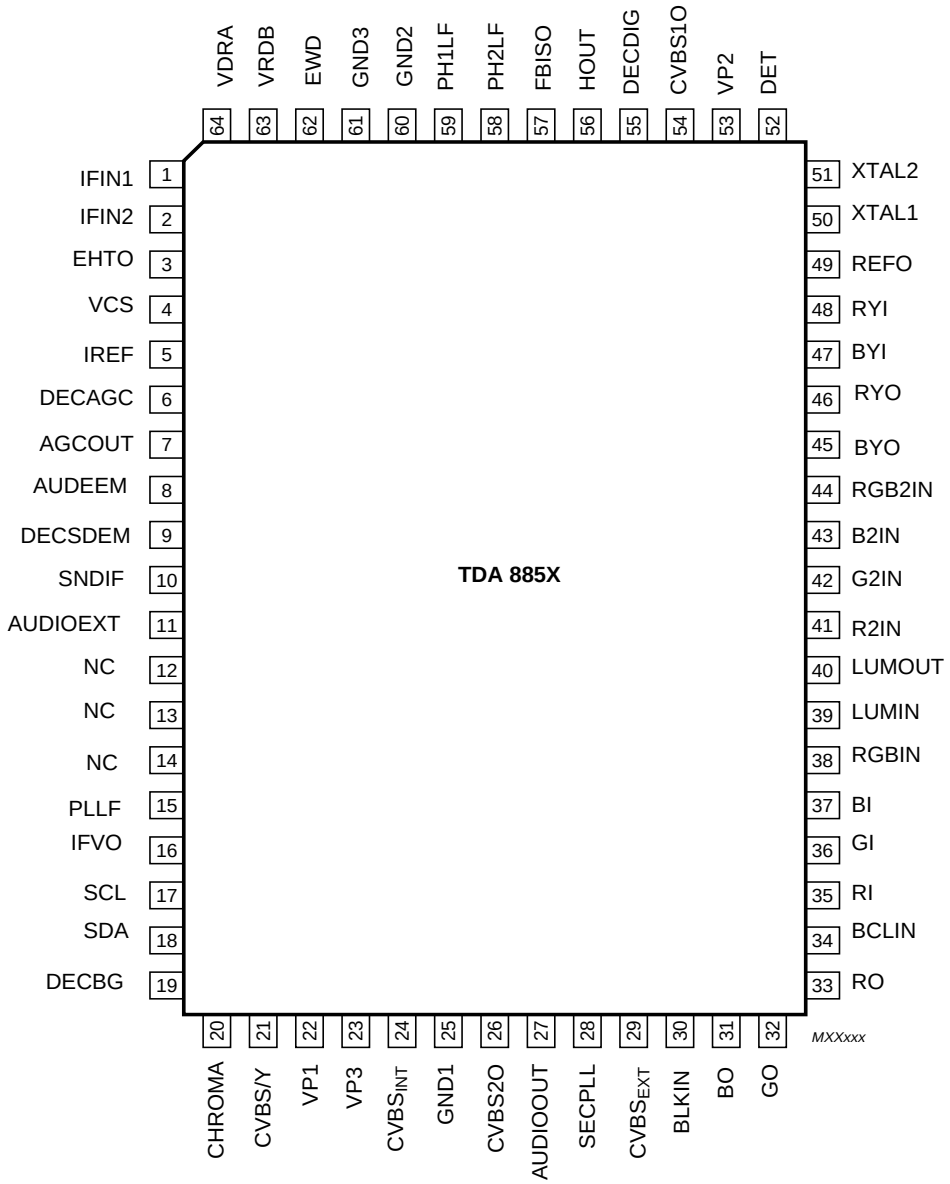


Fig.5 Pin configuration (QFP64).

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The IF-amplifier contains 3 ac-coupled control stages with a total gain control range which is higher then 66 dB. The sensitivity of the circuit is comparable with that of modern IF-IC's.

The video signal is demodulated by means of an alignment-free PLL carrier regenerator with an internal VCO. This VCO is calibrated by means of a digital control circuit which uses the X-tal frequency of the colour decoder as a reference. The frequency setting for the various standards (33.4, 33.9, 38, 38.9, 45.75 and 58.75 MHz) is realised via the I²C-bus. To get a good performance for phase modulated carrier signals the control speed of the PLL can be increased by means of the FFI bit.

The AFC output is generated by the digital control circuit of the IF-PLL demodulator and can be read via the I²C-bus. For fast search tuning systems the window of the AFC can be increased with a factor 3. The setting is realised with the AFW bit. The AFC data is valid only when the horizontal PLL is in lock (SL = 1)

Depending on the type the AGC-detector operates on top-sync level (single standard versions) or on top sync and top white- level (multi standard versions). The demodulation polarity is switched via the I²C-bus. The AGC detector time-constant capacitor is connected externally. This mainly because of the flexibility of the application. The time-constant of the AGC system during positive modulation is rather long to avoid visible variations of the signal amplitude. To improve the speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When during 3 field periods no action is detected the speed of the system is increased. For signals without peak white information the system switches automatically to a gated black level AGC. Because a black level clamp pulse is required for this way of operation the circuit will only switch to black level AGC in the internal mode.

The circuits contain a video identification circuit which is independent of the synchronisation circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. However, this ident circuit cannot be made as sensitive as the slower sync ident circuit (SL) and we recommend to use both ident outputs to obtain a reliable search system. The ident output is supplied to the tuning system via the I²C-bus.

The input of the identification circuit is connected to pin 13 (S-DIP 56 devices), the "internal" CVBS input (see Fig.6). This has the advantage that the ident circuit can also be made operative when a scrambled signal is received (descrambler connected between pin 6 (IF video output) and pin 13). A second advantage is that the ident circuit can be used when the IF amplifier is not used (e.g. with built-in satellite tuners).

The video ident circuit can also be used to identify the selected CBVS or Y/C signal. The switching between the 2 modes can be realised with the VIM bit.

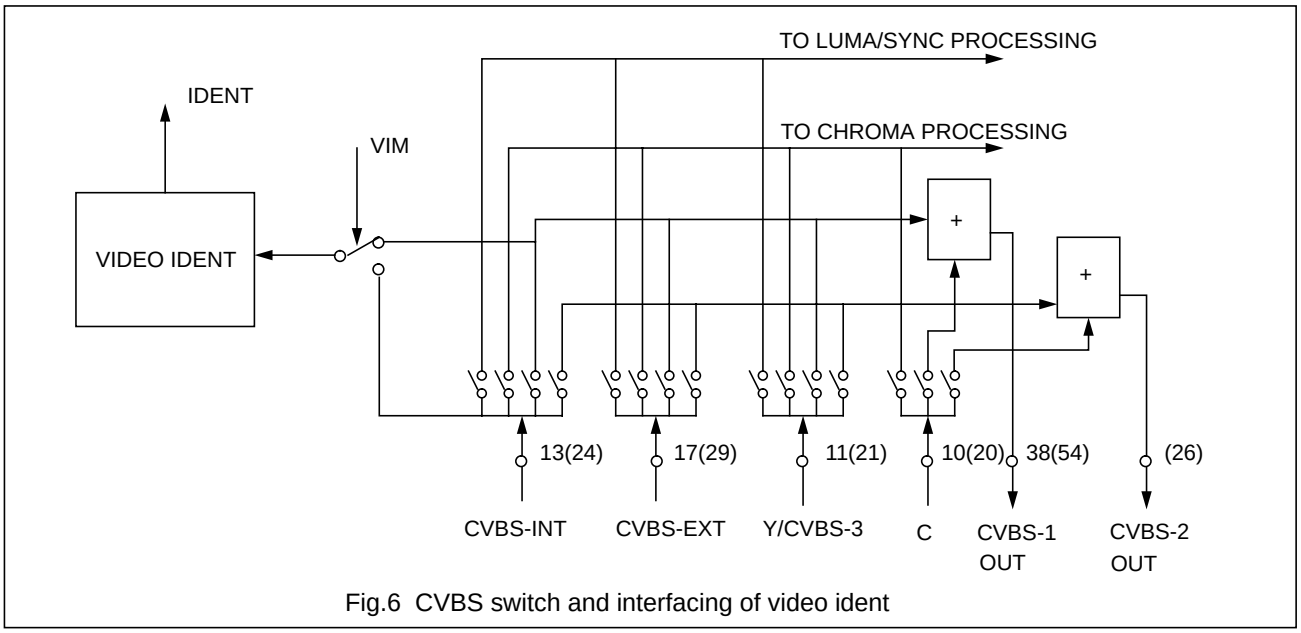


Fig.6 CVBS switch and interfacing of video ident

Video switches

The circuits have two CVBS inputs (internal and external CVBS) and a Y/C input. When the Y/C input is not required the Y input can be used as third CVBS input. The switch configuration is given in Fig.6. The selection of the various sources is made via the I²C-bus.

For the TDA 884X devices the video switch configuration is identical to the switch of the TDA 8374/75 series. So the circuit has one CVBS output (amplitude of 2 V_{P-P} for the TDA 884X series) and the I²C-bus control is similar to that of the TDA 8374/75. For the TDA 885X IC's the video switch circuit has a second output (amplitude of 1 V_{P-P}) which can be set independently of the position of the first output. The input signal for the decoder is also available on the CVBS1-output.

Therefore this signal can be used to drive the Teletext decoder. If S-VHS is selected for one of the outputs the luminance and chrominance signals are added so that a CVBS signal is obtained again.

Sound circuit

The sound bandpass and trap filters have to be connected externally. The filtered intercarrier signal is fed to a limiter circuit and is demodulated by means of a PLL demodulator. This PLL circuit tunes itself automatically to the incoming carrier signal so that no adjustment is required.

The volume is controlled via the I²C-bus. The deemphasis capacitor has to be connected externally. The non-controlled audio signal can be obtained from this pin (via a buffer stage).

The FM demodulator can be muted via the I²C-bus. This function can be used to switch-off the sound during a channel change so that high output peaks are prevented.

The TDA 8840/41/42/46 contain an Automatic Volume Levelling (AVL) circuit which automatically stabilises the audio output signal to a certain level which can be set by the viewer by means of the volume control. This function prevents big audio output fluctuations due to variations of the modulation depth of the transmitter. The AVL function can be activated via the I²C-bus.

Synchronisation circuit

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which is operating at 50% of the amplitude. The separated sync pulses are fed to the first phase detector and to the coincidence detector. This coincidence detector is used to detect whether the line oscillator is synchronised and can also be used for transmitter identification. This circuit can be made less sensitive by means of the STM bit. This mode can be used during search tuning to avoid that the tuning system will stop at very weak input signals. The first PLL has a very high statical steepness so that the phase of the picture is independent of the line frequency.

The horizontal output signal is generated by means of an oscillator which is running at twice the line frequency. Its frequency is divided by 2 to lock the first control loop to the incoming signal. The time-constant of the loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time-constant depending on the noise content of the incoming video signal.

The free-running frequency of the oscillator is determined by a digital control circuit which is locked to the reference signal of the colour decoder. When the IC is switched-on the horizontal output signal is suppressed and the oscillator is calibrated as soon as all sub-address bytes have been sent. When the frequency of the oscillator is correct the horizontal drive signal is switched-on. To obtain a smooth switching-on and switching-off behaviour of the horizontal output stage the horizontal output frequency is doubled during switch-on and switch-off (slow start/stop). During that time the duty cycle of the output pulse has such a value that maximum safety is obtained for the output stage.

To protect the horizontal output transistor the horizontal drive is immediately switched off when a power-on-reset is detected. The drive signal is switched-on again when the normal switch-on procedure is followed, i.e. all sub-address bytes must be sent and after calibration the horizontal drive signal will be released again via the slow start procedure. When the coincidence detector indicates an out-of-lock situation the calibration procedure is repeated. The circuit has a second control loop to generate the drive pulses for the horizontal driver stage. The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched-on during the flyback time.

Via the I²C-bus adjustments can be made of the horizontal and vertical geometry. The vertical sawtooth generator drives the vertical output drive circuit which has a differential output current. For the E-W drive a single ended current output is available. A special feature is the zoom function for both the horizontal and vertical deflection and the vertical scroll function which are available in some versions. When the horizontal scan is reduced to display 4:3 pictures on a 16:9 picture tube an accurate video blanking can be switched on to obtain well defined edges on the screen.

Overvoltage conditions (X-ray protection) can be detected via the EHT tracking pin. When an overvoltage condition is detected the horizontal output drive signal will be switched-off via the slow stop procedure but it is also possible that the drive is not switched-off and that just a protection indication is given in the I²C-bus output byte. The choice is made via the input bit PRD. The IC's have a second protection input on the φ_2 filter capacitor pin. When this input is activated the drive signal is switched-off immediately and switched-on again via the slow start procedure. For this reason this protection input can be used as "flash protection".

The drive pulses for the vertical sawtooth generator are obtained from a vertical countdown circuit. This countdown circuit has various windows depending on the incoming signal (50 Hz or 60 Hz and standard or non standard). The countdown circuit can be forced in various modes by means of the I²C-bus. During the insertion of RGB signals the maximum vertical frequency is increased to 72 Hz so that the circuit can also synchronise on signals with a higher vertical frequency like VGA. To obtain short switching times of the countdown circuit during a channel change the divider can be forced in the search window by means of the NCIN bit. The vertical deflection can be set in the de-interlace mode via the I²C bus.

To avoid damage of the picture tube when the vertical deflection fails the guard output current of the TDA 8350/51 can be supplied to the beam current limiting input. When a failure is detected the RGB-outputs are blanked and a bit is set (NDF) in the status byte of the I²C-bus. When no vertical deflection output stage is connected this guard circuit will also blank the output signals. This can be overruled by means of the EVG bit.

Chroma and luminance processing

The circuits contain a chroma bandpass and trap circuit. The filters are realised by means of gyrator circuits and they are automatically calibrated by comparing the tuning frequency with the X-tal frequency of the decoder. The luminance delay line and the delay for the peaking circuit are also realised by means of gyrator circuits. The centre frequency of the chroma bandpass filter is switchable via the I²C-bus so that the performance can be optimised for "front-end" signals and external CVBS signals. During SECAM reception the centre frequency of the chroma trap is reduced to get a better suppression of the SECAM carrier frequencies. All IC's have a black stretcher circuit which corrects the black level for incoming video signals which have a deviation between the black level and the blanking level (back porch). The timeconstant for the black stretcher is realised internally.

The resolution of the peaking control DAC has been increased to 6 bits. All IC's have a defeatable coring function in the peaking circuit. Some of these IC's have a YUV interface (see table on page 2) so that picture improvement IC's like the TDA 9170 (Contrast improvement), TDA 9177 (Sharpness improvement) and TDA 4556/66 (CTI) can be applied. When the CTI IC's are applied it is possible to increase the gain of the luminance channel by means of the GAI bit in subaddress 03 so that the resulting RGB output signals are not affected.

Colour decoder

Depending on the IC type the colour decoder can decode PAL, PAL/NTSC or PAL/NTSC/SECAM signals. The PAL/NTSC decoder contains an alignment-free X-tal oscillator, a killer circuit and two colour difference demodulators. The 90° phase shift for the reference signal is made internally.

The IC's contain an Automatic Colour Limiting (ACL) circuit which is switchable via the I²C-bus and which prevents that oversaturation occurs when signals with a high chroma-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chroma signal and not the burst signal. This has the advantage that the colour sensitivity is not affected by this function.

The SECAM decoder contains an auto-calibrating PLL demodulator which has two references, viz: the 4.4 MHz sub-carrier frequency which is obtained from the X-tal oscillator which is used to tune the PLL to the desired free-running frequency and the bandgap reference to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search or SECAM mode.

The frequency of the active X-tal is fed to the Fsc output (pin 33) and can be used to tune an external comb filter (e.g. the SAA 4961).

The base-band delay line (TDA 4665 function) is integrated in the PAL/SECAM IC's and in the NTSC IC TDA 8846A. In the latter IC it improves the cross colour performance (chroma comb filter). The demodulated colour difference signals are internally supplied to the delay line. The colour difference matrix switches automatically between PAL/SECAM and NTSC, however, it is also possible to fix the matrix in the PAL standard.

The "blue stretch" circuit is intended to shift colour near "white" with sufficient contrast values towards more blue to obtain a brighter impression of the picture.

Which colour standard the IC's can decode depends on the external X-tals. The X-tal to be connected to pin 34 must have a frequency of 3.5 MHz (NTSC-M, PAL-M or PAL-N) and pin 35 can handle X-tals with a frequency of 4.4 and 3.5 MHz. Because the X-tal frequency is used to tune the line oscillator the value of the X-tal frequency must be given to the IC via the I²C-bus. It is also possible to use the IC in the so called "Tri-norma" mode for South America. In that case one X-tal must be connected to pin 34 and the other 2 to pin 35. The switching between the 2 latter X-tals must be done externally. This has the consequence that the search loop of the decoder must be controlled by the µ-computer. To prevent calibration problems of the horizontal oscillator the external switching between the 2 X-tals should be carried out when the oscillator is forced to pin 34. For a reliable calibration of the horizontal oscillator it is very important that the X-tal indication bits (XA and XB) are not corrupted. For this reason the X-tal bits can be read in the output bytes so that the software can check the I²C-bus transmission.

Under bad-signal conditions (e.g. VCR-playback in feature mode), it may occur that the colour killer is activated although the colour PLL is still in lock. When this killing action is not wanted it is possible to overrule the colour killer by forcing the colour decoder to the required standard and to activate the FCO-bit (Forced Colour On) in the control-5 subaddress.

The IC's contain a so-called "Dynamic skin tone (flesh) control" feature. This function is realised in the YUV domain by detecting the colours near to the skin tone. The correction angle can be controlled via the I²C-bus.

RGB output circuit and black-current stabilisation

The colour-difference signals are matrixed with the luminance signal to obtain the RGB-signals. The TDA 884X devices have one (linear) RGB input. This RGB signal can be controlled on contrast and brightness (like TDA 8374/75). By means of the IE1 bit the insertion blanking can be switched on or off. Via the IN1 bit it can be read whether the insertion pin has a high level or not.

The TDA 885X IC's have an additional RGB input. This RGB signal can be controlled on contrast, saturation and brightness. The insertion blanking of this input can be switched-off by means of the IE2 bit. Via the IN2 bit it can be read whether the insertion pin has a high level or not.

The output signal has an amplitude of about 2 volts black-to-white at nominal input signals and nominal settings of the controls. To increase the flexibility of the IC it is possible to insert OSD and/or teletext signals directly at the RGB outputs. This insertion mode is controlled via the insertion input (pin 26 in the S-DIP 56- and pin 38 in the QFP-64 envelope). This blanking action at the RGB outputs has some delay which must be compensated externally.

To obtain an accurate biasing of the picture tube a "Continuous Cathode Calibration" circuit has been developed. This function is realised by means of a 2-point black level stabilisation circuit. By inserting 2 test levels for each gun and comparing the resulting cathode currents with 2 different reference currents the influence of the picture tube parameters like the spread in cut-off voltage can be eliminated. This 2-point stabilisation is based on the principle that the ratio between the cathode currents is coupled to the ratio between the drive voltages according to:

$$\frac{I_{k1}}{I_{k2}} = \left(\frac{V_{dr1}}{V_{dr2}}\right)^{\gamma}$$

The feedback loop makes the ratio between the cathode currents I_{k1} and I_{k2} equal to the ratio between the reference currents (which are internally fixed) by changing the (black) level and the amplitude of the RGB output signals via 2 converging loops. The system operates in such a way that the black level of the drive signal is controlled to the cut-off point of the gun so that a very good grey scale tracking is obtained. The accuracy of the adjustment of the black level is just dependent on the ratio of internal currents and these can be made very accurately in integrated circuits. An additional advantage of the 2-point measurement is that the control system makes the absolute value of I_{k1} and I_{k2} identical to the internal reference currents. Because this adjustment is obtained by means of an adaption of the gain of the RGB control stage this control stabilises the gain of the complete channel (RGB output stage and cathode characteristic). As a result variations in the gain figures during life will be compensated by this 2-point loop.

An important property of the 2-point stabilisation is that the off-set as well as the gain of the RGB path is adjusted by the feedback loop. Hence the maximum drive voltage for the cathode is fixed by the relation between the test pulses, the reference current and the relative gain setting of the 3 channels. This has the consequence that the drive level of the CRT cannot be adjusted by adapting the gain of the RGB output stage. Because different picture tubes may require different drive levels the typical “cathode drive level” amplitude can be adjusted by means of an I²C-bus setting. Dependent on the chosen cathode drive level the typical gain of the RGB output stages can be fixed taking into account the drive capability of the RGB outputs (pins 19 to 21). More details about the design will be given in the application report.

The measurement of the “high” and the “low” current of the 2- point stabilisation circuit is carried out in 2 consecutive fields. The leakage current is measured in each field. The maximum allowable leakage current is 100 μA

When the TV receiver is switched-on the RGB output signals are blanked and the black current loop will try to set the right picture tube bias levels. Via the AST bit a choice can be made between automatic start-up or a start-up via the μ-processor. In the automatic mode the RGB drive signals are switched-on as soon as the black current loop has been stabilised. In the other mode the BCF bit is set to 0 when the loop is stabilised. The RGB drive can than be switched-on by setting the AST bit to 0. In the latter mode some delay can be introduced between the setting of the BCF bit and the switching of the AST bit so that switch-on effects can be suppressed.

It is also possible to start-up the devices with a fixed internal delay (as with the TDA 837X and the TDA884X/5X N1). This mode is activated with the BCO bit.

The vertical blanking is adapted to the incoming CVBS signal (50 Hz or 60 Hz). When the flyback time of the vertical output stage is longer than the 60 Hz blanking time the blanking can be increased to the same value as that of the 50 Hz blanking. This can be set by means of the LBM bit.

For an easy (manual) adjustment of the V_{g2} control voltage the VSD bit is available. When this bit is activated the black current loop is switched-off, a fixed black level is inserted at the RGB outputs and the vertical scan is switched-off so that a horizontal line is displayed on the screen. This line can be used as indicator for the V_{g2} adjustment. Because of the different requirements for the optimum cut-off voltage of the picture tube the RGB output level is adjustable when the VSD bit is activated. The control range is 2.5 ± 0.7 V and can be controlled via the brightness control DAC.

It is possible to insert a so called “blue back” back-ground level when no video is available. This feature can be activated via the BB bit in the control2 subaddress.

I²C-BUS SPECIFICATION

The slave address of the IC’s is given in Fig.7. The circuit operates up to clock frequencies of 400 kHz.

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	0	1	1/0

MLA743

Fig.7 Slave address (8A).

Start-up procedure

Read the status bytes until POR = 0 and send all subaddress bytes. The horizontal output signal is switched-on when the oscillator is calibrated.

Each time before the data in the IC is refreshed, the status bytes must be read. If POR = 1, the procedure mentioned above must be carried out to restart the IC.

When this procedure is not followed the horizontal frequency may be incorrect after power-up or after a power dip.

TDA 8840/41/42/46/46A:

Valid subaddresses: 00 to 1A (subaddresses 04 to 07 and 17 are not used), subaddress FE is reserved for test purposes. Auto-increment mode available for subaddresses. The bit L'FA is only valid in the TDA 8842, the function of the colour mode bits (CM0-CM2 and CD0-CD2) is dependent on the functional content of the IC.

Table 1 Input status bits.

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Control 0	00	INA	INB	INC	BCO	FOA	FOB	XA	XB
Control 1	01	FORF	FORS	DL	STB	POC	CM2	CM1	CM0
Hue	02	AVL	AKB	A5	A4	A3	A2	A1	A0
Horizontal shift (HS)	03	VIM	GAI	A5	A4	A3	A2	A1	A0
Vertical slope (VS)	08	NCIN	STM	A5	A4	A3	A2	A1	A0
Vertical amplitude (VA)	09	VID	LBM	A5	A4	A3	A2	A1	A0
S-correction (SC)	0A	0	EVG	A5	A4	A3	A2	A1	A0
Vertical shift (VSH)	0B	SBL	PRD	A5	A4	A3	A2	A1	A0
White point R	0C	0	0	A5	A4	A3	A2	A1	A0
White point G	0D	0	0	A5	A4	A3	A2	A1	A0
White point B	0E	MAT	0	A5	A4	A3	A2	A1	A0
Peaking	0F	0	0	A5	A4	A3	A2	A1	A0
Brightness	10	RBL	COR	A5	A4	A3	A2	A1	A0
Saturation	11	IE1	0	A5	A4	A3	A2	A1	A0
Contrast	12	AFW	IFS	A5	A4	A3	A2	A1	A0
AGC take-over	13	MOD	VSW	A5	A4	A3	A2	A1	A0
Volume control	14	SM	FAV	A5	A4	A3	A2	A1	A0
Adjustment IF-PLL	15	IFA	IFB	IFC	0	0	0	0	0
Control 2	18	OSO	VSD	CB	BLS	BKS	0	0	BB
Control 3	19	HOB	BPS	ACL	CMB	AST	CL2	CL1	CL0
Control 4	1A	0	0	0	0	DS	DSA	FFI	EBS
Control 5	1B	0	0	0	0	0	0	0	FCO

Table 2 Output status bits.

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	X	SL	XPR	CD2	CD1	CD0
	01	NDF	IN1	X	IFI	AFA	AFB	SXA	SXB
	02	N2	X	BCF	IVW	ID3	ID2	ID1	ID0

TDA 8843/44/47:

Valid subaddresses: 00 to 1A, subaddress FE is reserved for test purposes. Auto-increment mode available for subaddresses. The bits L'FA, CM0-CM2 and CD0-CD2 are only available in the TDA 8843/44.

Table 3 Input status bits.

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Control 0	00	INA	INB	INC	BCO	FOA	FOB	XA	XB
Control 1	01	FORF	FORS	DL	STB	POC	CM2	CM1	CM0
Hue	02	HBL	AKB	A5	A4	A3	A2	A1	A0
Horizontal shift (HS)	03	VIM	GAI	A5	A4	A3	A2	A1	A0
EW width (EW)	04	0	0	A5	A4	A3	A2	A1	A0
EW parabola/width (PW)	05	0	0	A5	A4	A3	A2	A1	A0
EW corner parabola (CP)	06	0	0	A5	A4	A3	A2	A1	A0
EW trapezium (TC)	07	0	0	A5	A4	A3	A2	A1	A0
Vertical slope (VS)	08	NCIN	STM	A5	A4	A3	A2	A1	A0
Vertical amplitude (VA)	09	VID	LBM	A5	A4	A3	A2	A1	A0
S-correction (SC)	0A	HCO	EVG	A5	A4	A3	A2	A1	A0
Vertical shift (VSH)	0B	SBL	PRD	A5	A4	A3	A2	A1	A0
White point R	0C	0	0	A5	A4	A3	A2	A1	A0
White point G	0D	0	0	A5	A4	A3	A2	A1	A0
White point B	0E	MAT	0	A5	A4	A3	A2	A1	A0
Peaking	0F	0	0	A5	A4	A3	A2	A1	A0
Brightness	10	RBL	COR	A5	A4	A3	A2	A1	A0
Saturation	11	IE1	0	A5	A4	A3	A2	A1	A0
Contrast	12	AFW	IFS	A5	A4	A3	A2	A1	A0
AGC take-over	13	MOD	VSW	A5	A4	A3	A2	A1	A0
Volume control	14	SM	FAV	A5	A4	A3	A2	A1	A0
Adjustment IF-PLL	15	IFA	IFB	IFC	0	0	0	0	0
Vertical zoom (VX)	16	0	0	A5	A4	A3	A2	A1	A0
Vertical scroll	17	0	0	A5	A4	A3	A2	A1	A0
Control 2	18	OSO	VSD	CB	BLS	BKS	0	0	BB
Control 3	19	HOB	BPS	ACL	CMB	AST	CL2	CL1	CL0
Control 4	1A	YD3	YD2	YD1	YD0	DS	DSA	FFI	EBS
Control 5	1B	0	0	0	0	0	0	0	FCO

Table 4 Output status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	X	SL	XPR	CD2	CD1	CD0
	01	NDF	IN1	X	IFI	AFA	AFB	SXA	SXB
	02	N2	X	BCF	IVW	ID3	ID2	ID1	ID0

TDA 8854/57:

Valid subaddresses: 00 to 1A, subaddress FE is reserved for test purposes. Auto-increment mode available for subaddresses. The bits L'FA, CM0-CM2 and CD0-CD2 are only available in the TDA 8854.

Table 5 Input status bits.

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Control 0	00	INA	INB	INC	BCO	FOA	FOB	XA	XB
Control 1	01	FORF	FORS	DL	STB	POC	CM2	CM1	CM0
Hue	02	HBL	AKB	A5	A4	A3	A2	A1	A0
Horizontal shift (HS)	03	VIM	GAI	A5	A4	A3	A2	A1	A0
EW width (EW)	04	0	0	A5	A4	A3	A2	A1	A0
EW parabola/width (PW)	05	0	0	A5	A4	A3	A2	A1	A0
EW corner parabola (CP)	06	0	0	A5	A4	A3	A2	A1	A0
EW trapezium (TC)	07	0	0	A5	A4	A3	A2	A1	A0
Vertical slope (VS)	08	NCIN	STM	A5	A4	A3	A2	A1	A0
Vertical amplitude (VA)	09	VID	LBM	A5	A4	A3	A2	A1	A0
S-correction (SC)	0A	HCO	EVG	A5	A4	A3	A2	A1	A0
Vertical shift (VSH)	0B	SBL	PRD	A5	A4	A3	A2	A1	A0
White point R	0C	0	0	A5	A4	A3	A2	A1	A0
White point G	0D	0	0	A5	A4	A3	A2	A1	A0
White point B	0E	MAT	0	A5	A4	A3	A2	A1	A0
Peaking	0F	0	0	A5	A4	A3	A2	A1	A0
Brightness	10	RBL	COR	A5	A4	A3	A2	A1	A0
Saturation	11	IE1	IE2	A5	A4	A3	A2	A1	A0
Contrast	12	AFW	IFS	A5	A4	A3	A2	A1	A0
AGC take-over	13	MOD	VSW	A5	A4	A3	A2	A1	A0
Volume control	14	SM	FAV	A5	A4	A3	A2	A1	A0
Adjustment IF-PLL	15	IFA	IFB	IFC	0	0	0	0	0
Vertical zoom (VX)	16	0	0	A5	A4	A3	A2	A1	A0
Vertical scroll	17	0	0	A5	A4	A3	A2	A1	A0
Control 2	18	OSO	VSD	CB	BLS	BKS	CS1	CS0	BB
Control 3	19	HOB	BPS	ACL	CMB	AST	CL2	CL1	CL0
Control 4	1A	YD3	YD2	YD1	YD0	DS	DSA	FFI	EBS
Control 5	1B	0	0	0	0	0	0	0	FCO

Table 6 Output status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	X	SL	XPR	CD2	CD1	CD0
	01	NDF	IN1	IN2	IFI	AFA	AFB	SXA	SXB
	02	N2	X	BCF	IVW	ID3	ID2	ID1	ID0

INPUT CONTROL BITS

Table 7 Source select

INA	INB	INC	SELECTED SIGNALS	CVBS1 OUTPUT
0	0	0	Internal CVBS+ audio	Int. CVBS
0	0	1	External CVBS+ audio	Ext. CVBS
0	1	0	Y/C + ext. audio	Y/C(Y+C)
0	1	1	CVBS3 + ext. audio	CVBS3
1	0	0	Y/C + int audio, note 1	Int CVBS
1	1	0	Y/C + ext audio, note 1	Ext. CVBS

Note

1. These modes are intended for comb filter applications.

Table 8 Switch-on behaviour

BCO	STATUS
0	switch-on of picture without delay
1	switch-on of picture via internal delay

Table 9 Phase 1 (φ_1) time constant

FOA	FOB	MODE
0	0	normal
0	1	slow
1	0	slow/fast
1	1	fast

Table 10 Crystal indication

XA	XB	CRYSTAL
0	0	two 3.6 MHz
0	1	one 3.6 MHz (pin 34)
1	0	one 4.4 MHz (pin 35)
1	1	3.6 MHz (pin 34) and 4.4 MHz (pin 35)

Table 11 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto (60 Hz when line not in sync)
0	1	60 Hz
1	0	keep last detected field frequency
1	1	auto (50 Hz when line not in sync)

Table 12 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 13 Stand-by

STB	MODE
0	stand-by
1	normal

Table 14 Synchronization mode

POC	MODE
0	active
1	not active

Table 15 Colour decoder mode

CM2	CM1	CM0	DECODER MODE
0	0	0	not forced, own intelligence
0	0	1	forced X-tal pin 34 PAL/NTSC
0	1	0	forced X-tal pin 34 PAL
0	1	1	forced X-tal pin 34 NTSC
1	0	0	forced X-tal pin 35 PAL/NTSC
1	0	1	forced X-tal pin 35 PAL
1	1	0	forced X-tal pin 35 NTSC
1	1	1	Forced SECAM (X-tal pin 35)

Table 16 Auto. Volume Levelling (TDA 8840/1/2/6/6A)

AVL	MODE
0	not active
1	active

Table 17 RGB blanking mode (TDA 8843/44/47/54/57)

HBL	MODE
0	normal blanking (horizontal flyback)
1	wide blanking

Table 18 Black current stabilisation

AKB	MODE
0	active
1	not active

Table 19 Video ident mode

VIM	MODE
0	ident coupled to internal CVBS (pin 13)
1	ident coupled to selected CVBS

Table 20 Gain of luminance channel

GAI	MODE
0	normal gain (V27 = 1 VBL-WH)
1	high gain (V27 = 0.45 VP-P)

Table 21 Vertical divider mode

NCIN	VERTICAL DIVIDER MODE
0	normal operation
1	switched to search window

Table 22 Search tuning mode

STM	MODE
0	normal operation
1	reduced sensitivity of video indent circuit

Table 23 Video ident mode

VID	VIDEO IDENT MODE
0	φ1 loop switched on and off
1	not active

Table 24 Long blanking mode

LBM	BLANKING MODE
0	adapted to standard (50 or 60 Hz)
1	fixed in accordance with 50 Hz standard

Table 25 EHT tracking mode

HCO	TRACKING MODE
0	EHT tracking only on vertical
1	EHT tracking on vertical and EW

Table 26 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

Table 27 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 28 Overvoltage input mode

PRD	OVERVOLTAGE MODE
0	detection mode
1	protection mode

Table 29 PAL-SECAM/NTSC matrix (TDA8841/2/3/4/54)

MAT	MATRIX POSITION
0	adapted to standard
1	PAL matrix

Table 30 NTSC matrix (TDA 8846/46A/47/57)

MAT	MATRIX POSITION
0	Japanese matrix
1	USA matrix

Table 31 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 32 Noise coring (peaking)

COR	NOISE CORING
0	off
1	on

Table 33 Enable fast blanking RGB-1

IE1	FAST BLANKING
0	not active
1	active

Table 34 Enable fast blanking RGB-2 (TDA 885X)

IE2	FAST BLANKING
0	not active
1	active

Table 35 AFC window

AFW	AFC WINDOW
0	normal
1	enlarged

Table 36 IF sensitivity

IFS	IF SENSITIVITY
0	normal
1	reduced

Table 37 Modulation standard

MOD	MODULATION
0	negative
1	positive

Table 38 Video mute

VSW	STATE
0	normal operation
1	IF-video signal switched off

Table 39 Sound mute

SM	STATE
0	normal operation
1	sound mute active

Table 40 Fixed audio volume

FAV	MODE
0	normal volume control
1	audio output level fixed

Table 41 PLL demodulator frequency adjust

IFA	IFB	IFC	IF FREQUENCY
0	0	0	58.75 MHz
0	0	1	45.75 MHz
0	1	0	38.90 MHz
0	1	1	38.00 MHz
1	0	0	33.40 MHz
1	1	0	33.90 MHz

Table 42 Switch-off in vertical overscan

OSO	MODE
0	Switch-off undefined
1	Switch-off in vertical overscan

Table 43 Vertical scan disable

VSD	MODE
0	Vertical scan active
1	Vertical scan disabled

Table 44 Chroma bandpass centre frequency

CB	CENTRE FREQUENCY
0	F_{SC}
1	1.1 x F_{SC}

Table 45 Blue stretch

BLS	BLUE STRETCH MODE
0	off
1	on

Table 46 Black stretch

BKS	BLACK STRETCH MODE
0	off
1	on

Table 47 2nd CVBS output (TDA 885X)

CS1	CS0	CVBS-2 OUTPUT
0	0	internal CVBS
0	1	external CVBS
1	0	Y/C (Y + C)
1	1	CVBS-3

Table 48 Blue back when no video signal is identified

BB	BLUE BACK
0	off
1	on

Table 49 Helper output blanking (PAL^{PLUS})

HOB	OUTPUT BLANKING
0	not active
1	active

Table 50 Bypass of chroma base-band delay line

BPS	DELAY LINE MODE
0	active
1	bypassed

Table 51 Automatic colour limiting

ACL	COLOUR LIMITING
0	not active
1	active

Table 52 Enable external comb filter

CMB	COMB FILTER
0	disabled
1	enabled

Table 53 Start-up mode of black current loop; note 1

AST	MODE
0	automatic mode;
1	switch-on under control of μ-processor

Note

1. When the circuit is in the automatic mode the RGB drive is switched-on as soon as the black current loop has stabilised. Under control of the μ-processor the condition of the black current loop is indicated via the BCF bit. When this bit changes to 0 the RGB drive can be switched-on by setting the AST bit to 0.

Table 54 Cathode drive level

CL2	CL1	CL0	SETTING CATHODE DRIVE AMPLITUDE; NOTE 1
0	0	0	$57V_{BL-WH}$
0	0	1	63 V_{BL-WH}
0	1	0	70 V_{BL-WH}
0	1	1	77 V_{BL-WH}
1	0	0	84 V_{BL-WH}
1	0	1	91 V_{BL-WH}
1	1	0	99 V_{BL-WH}
1	1	1	107 V_{BL-WH}

Note

1. The given values are valid for the following conditions:
   - Nominal CVBS input signal
   - Settings for contrast, WPA and peaking nominal
   - Black- and blue-stretch switched-off
   - Gain of output stage such that no clipping occurs
   - Beam current limiting not active

   The tolerance on these values is about ± 3 V.

Table 55 Y-delay adjustment; note 1

YD0 to YD3	Y-DELAY
YD3	YD3 * 160 ns +
YD2	YD2 * 80 ns +
YD1	YD1 * 40 ns +
YD0	YD0 * 40 ns

Note

1. For an equal delay of the luminance and chrominance signal the delay must be set at a value of 160 ns. This is only valid for a CVBS signal without group delay distortions.

Table 56 Dynamic skin control on/off

DS	MODE
0	off
1	on

Table 57 Dynamic skin control angle

DSA	ANGLE OF CORRECTION
0	correction angle 123 degrees
1	correction angle 117 degrees

Table 58 Fast filter IF-PLL

FFI	CONDITION
0	normal time constant
1	increased time constant

Table 59 Extended Blue Stretch

EBS	CONDITION
0	off
1	on

Table 60 Forced Colour-On

FCO	CONDITION
0	normal colour killer function
1	no colour killer (in forced colour mode only)

OUTPUT CONTROL BITS

Table 61 Power-on-reset

POR	MODE
0	normal
1	power-down

Table 62 Field frequency indication

FSI	FREQUENCY
0	50 Hz
1	60 Hz

Table 63 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 64 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 65 Colour decoder mode

CD2	CD1	CD0	STANDARD
0	0	0	no colour standard identified
0	0	1	NTSC with X-tal pin 34
0	1	0	PAL with X-tal pin 35
0	1	1	SECAM
1	0	0	NTSC with X-tal pin 35
1	0	1	PAL with X-tal pin 34
1	1	0	spare

Table 66 Output vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 67 Indication RGB-1/2 (TDA 885X)insertion

INX	RGB INSERTION
0	no (pin 26/38 and/or 44 LOW)
1	yes (pin 26/38 and/or 44HIGH)

Table 68 Output video identification

IFI	VIDEO SIGNAL
0	no video signal identified
1	video signal identified

Table 69 AFC output

AFA	AFB	CONDITION
0	0	outside window; too low
0	1	outside window; too high
1	0	in window; below reference
1	1	in window; above reference

Table 70 X-tal indication

SXA	SXB	CONDITION
0	0	two 3.6 MHz X-tals
0	1	only 3.6 MHz X-tal
1	0	only 4.4 MHz X-tal
1	1	3.6 and 4.4 MHz X-tal

Table 71 Condition black current loop

BCF	CONDITION
0	black current loop is stabilised
1	black current loop is not stabilised

Table 72 Mask version indication

N2	MASK VERSION
0	N1 version
1	N2 version

Table 73 Condition vertical divider

IVW	STANDARD VIDEO SIGNAL
0	no standard video signal
1	standard video signal (525 or 625 lines)

Table 74 IC version indication

ID3	ID2	ID1	ID0	IC TYPE
0	0	0	1	TDA 8840/40H
0	0	1	0	TDA 8841/41H
0	0	1	1	TDA 8842/42H
0	0	0	0	TDA 8846
1	0	0	0	TDA 8846A
0	1	1	0	TDA 8843
0	1	1	1	TDA 8844
0	1	0	0	TDA 8847
1	1	1	1	TDA 8854H
1	1	0	0	TDA 8857H

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	operating junction temperature		–	150	°C
V_{es}	electrostatic handling	HBM; all pins; notes 1 and 2	–2000	+2000	V
		MM; all pins; notes 1 and 3	–200	+200	V

Notes

1. All pins are protected against ESD by means of internal clamping diodes.
2. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
3. Machine Model (MM): R = 0 Ω; C = 200 pF.

THERMAL CHARACTERISTICS (THERMAL RESISTANCE FROM JUNCTION TO AMBIENT IN FREE AIR)

SYMBOL	ENVELOPE	VALUE	UNIT
$R_{th\ j\text{-}a}$	SDIP 56	40	K/W
	QFP 64	50	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

Latch-up

At an ambient temperature of 70 °C nearly all pins meet the following specification:

- $I_{trigger} \geq 100$ mA or $\geq 1.5V_{DD(max)}$
- $I_{trigger} \leq -100$ mA or $\leq -0.5V_{DD(max)}$.

Some pins have a slightly lower trigger current. The pin numbers and and the allowable trigger current are given below.

Pin 50: $I_{trigger} \geq 70$ mA

Pin 51: $I_{trigger} \geq 60$ mA

Pin 52: $I_{trigger} \geq 60$ mA

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
POWER SUPPLY (PINS 12 AND 37)						
V.1.1	supply voltage		7.2	8.0	8.8	V
V.1.2	supply current pin 12		–	70	–	mA
V.1.3	supply current pin 37		–	60	–	mA
V.1.4	total power dissipation		–	1040	–	mW
IF circuit						
VISION IF AMPLIFIER INPUTS (PINS 48 AND 49)						
	input sensitivity (RMS value)	note 1				
M.1.1		f_i = 38.90 MHz	10	35	100	µV
M.1.2		f_i = 45.75 MHz	10	35	100	µV
M.1.3		f_i = 58.75 MHz	10	35	100	µV
M.1.4	input resistance (differential)	note 2	–	2	–	kΩ
M.1.5	input capacitance (differential)	note 2	–	3	–	pF
M.1.6	gain control range		64	75	–	dB
M.1.7	maximum input signal (RMS value)		150	–	–	mV
PLL DEMODULATOR (PLL FILTER ON PIN 5); NOTES 3 AND 4						
M.2.1	Free-running frequency of VCO	PLL not locked, deviation from nominal setting	–500	–	+500	kHz
M.2.2	Catching range PLL		–	2	–	MHz
M.2.3	Acquisition time PLL		–	–	20	ms

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO AMPLIFIER OUTPUT (PIN 6); NOTE 6						
M.3.1	zero signal output level	negative modulation; note 7	–	4.2	–	V
M.3.2		positive modulation; note 7	–	2.2	–	V
M.3.3	top sync level	negative modulation	1.8	1.9	2.0	V
M.3.4	white level	positive modulation	–	4.4	–	V
M.3.5	difference in amplitude between negative and positive modulation		–	0	15	%
M.3.6	video output impedance		–	50	–	Ω
M.3.7	internal bias current of NPN emitter follower output transistor		1.0	–	–	mA
M.3.8	maximum source current		–	–	5	mA
M.3.9	bandwidth of demodulated output signal	at –3 dB	6	9	–	MHz
M.3.10	differential gain	note 8	–	2	5	%
M.3.11	differential phase	notes 8 and 5	–	–	5	deg
M.3.12	video non-linearity	note 9	–	–	5	%
M.3.13	white spot clamp level		–	6.0	–	V
M.3.14	noise inverter clamping level	note 10	–	1.5	–	V
M.3.15	noise inverter insertion level (identical to black level)	note 10	–	2.7	–	V
	intermodulation	notes 5 and 11				
M.3.16	blue	V_o = 0.92 or 1.1 MHz	60	66	–	dB
M.3.17		V_o = 2.66 or 3.3 MHz	60	66	–	dB
M.3.18	yellow	V_o = 0.92 or 1.1 MHz	56	62	–	dB
M.3.19		V_o = 2.66 or 3.3 MHz	60	66	–	dB
	signal-to-noise ratio	notes 5 and 12				
M.3.20		weighted	56	60	–	dB
M.3.21		unweighted	49	53	–	dB
M.3.22	residual carrier signal	note 5	–	5.5	–	mV
M.3.23	residual 2nd harmonic of carrier signal	note 5	–	2.5	–	mV
IF AND TUNER AGC; NOTE 13						
Timing of IF-AGC with a 2.2 µF capacitor (pin 53)						
M.4.1	modulated video interference	30% AM for 1 mV to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
M.4.2	response time to IF input signal amplitude increase of 52 dB	positive and negative modulation	–	2	–	ms
M.4.3	response to an IF input signal amplitude decrease of 52 dB	negative modulation	–	50	–	ms
M.4.4		positive modulation	–	100	–	ms
M.4.5	allowed leakage current of the AGC capacitor	negative modulation	–	–	10	µA
M.4.6		positive modulation	–	–	200	nA

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner take-over adjustment (via I²C-bus)						
M.5.1	minimum starting level for tuner take-over (RMS value)		–	0.2	0.8	mV
M.5.2	maximum starting level for tuner take-over (RMS value)		40	60	–	mV
Tuner control output (pin 54)						
M.6.1	maximum tuner AGC output voltage	maximum tuner gain; note 2	–	–	9	V
M.6.2	output saturation voltage	minimum tuner gain; I_O = 2 mA	–	–	300	mV
M.6.3	maximum tuner AGC output swing		5	–	–	mA
M.6.4	leakage current RF AGC		–	–	1	µA
M.6.5	input signal variation for complete tuner control		0.5	2	4	dB
AFC OUTPUT (VIA I²C-BUS); NOTE 14						
M.7.1	AFC resolution		–	2	–	bits
M.7.2	window sensitivity		–	125	–	kHz
M.7.3	window sensitivity in large window mode		–	275	–	kHz
VIDEO IDENTIFICATION OUTPUT (VIA I²C-BUS)						
M.8.1	delay time of identification after the AGC has stabilized on a new transmitter		–	–	10	ms
Sound circuit						
DEMODULATOR INPUT; (PIN 1)						
G.1.1	input limiting for PLL catching range (RMS value)		–	1	2	mV
G.1.2	catching range PLL	note 15	4.2	–	6.8	MHz
G.1.3	input resistance	note 2	–	8.5	–	kΩ
G.1.4	input capacitance	note 2	–	–	5	pF
G.1.5	AM rejection	V_I = 50 mV RMS; note 16	60	66	–	dB
DE-EMPHASIS (PIN 55)						
G.2.1	output signal amplitude (RMS value)	note 15	–	500	–	mV
G.2.2	output resistance		–	15	–	kΩ
G.2.3	DC output voltage		–	3	–	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AUDIO OUTPUT (PIN 15)						
G.3.1	controlled output signal amplitude (RMS value)	−6 dB; note 15	500	700	900	mV
G.3.2	output resistance		–	500	–	Ω
G.3.3	DC output voltage		–	3.0	–	V
G.3.4	total harmonic distortion	note 17	–	0.15	0.5	%
G.3.5	total harmonic distortion	FAV = 1; note 18	–	0.15	0.5	%
G.3.6	power supply rejection	note 5	–	25	–	dB
G.3.7	internal signal-to-noise ratio	note 5 + 19	-	60	-	dB
G.3.8	external signal-to-noise ratio	note 5 + 19	-	80	-	dB
G.3.9	output level variation with temperature	note 5 + 20	-	-	tbf	dB
G.3.10	control range	see also Fig.8	–	80	–	dB
G.3.11	suppression of output signal when mute is active		–	80	–	dB
G.3.12	DC shift of the output when mute is active		–	50	100	mV
EXTERNAL AUDIO INPUT; (PIN 2)						
G.4.1	input signal amplitude (RMS value)		–	500	2000	mV
G.4.2	input resistance		–	25	–	kΩ
G.4.3	voltage gain difference between input and output	maximum volume	–	9	–	dB
G.4.4	crosstalk between internal and external audio signals		60	–	–	dB
AUTOMATIC VOLUME LEVELLING (ONLY IN TDA 8840/41/42/46/46A); CAPACITOR CONNECTED TO PIN 45; NOTE 21						
G.5.1	gain at maximum boost		–	6	–	dB
G.5.2	gain at minimum boost		–	-14	–	dB
G.5.3	charge (attack) current		–	1	–	mA
G.5.4	discharge (decay) current		–	200	–	nA
G.5.5	control voltage at maximum boost		–	1	–	V
G.5.6	control voltage at minimum boost		–	5	–	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS, Y/C, RGB, CD AND LUMINANCE OUT- AND INPUTS						
CVBS-Y/C SWITCH, PINS 10, 11, 13, 17 AND 38 (20, 21, 24, 26, 29 AND 54 FOR TDA 885X)						
S.1.1	CVBS or Y input voltage (peak-to-peak value)	note 22	–	1.0	1.4	V
S.1.2	CVBS or Y input current		–	4	–	µA
S.1.3	suppression of non-selected CVBS input signal	notes 5 and 23	50	–	–	dB
S.1.4	chrominance input voltage (burst amplitude)	note 2 and 24	–	0.3	1.0	V
S.1.5	chrominance input impedance		–	50	–	kΩ
S.1.6	output signal amplitude (CVBS1) (peak-to-peak value)		–	2.0	–	V
S.1.7	black level of CVBS1		–	2.1	–	V
S.1.8	output signal amplitude (CVBS2) (peak-to-peak value)		–	1.0	–	V
S.1.9	black level of CVBS2		–	3.3	–	V
S.1.10	output impedance		–	–	250	Ω
RGB INPUTS, PINS 23 TO 25 (35 TO 37 AND 41 TO 43 FOR TDA 885X)						
S.2.1	input signal amplitude for an output signal of 2 V (black-to-white) (peak-to-peak value)	note 25	–	0.7	0.8	V
S.2.2	input signal amplitude before clipping occurs (peak-to-peak value)	note 5	1.0	–	–	V
S.2.3	difference between black level of internal and external signals at the outputs		–	–	20	mV
S.2.4	input currents	no clamping; note 2	–	0.1	1	µA
S.2.5	delay difference for the three channels	note 5	–	0	20	ns
FAST BLANKING, PIN 26 (38 AND 44 FOR TDA 885X)						
S.3.1	input voltage	no data insertion	–	–	0.4	V
S.3.2		data insertion	0.9	0.6	–	V
S.3.3	maximum input pulse	insertion	–	–	3.0	V
S.3.4	delay time from RGB in to RGB out	data insertion; note 5	–	–	60	ns
S.3.5	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 5	–	–	20	ns
S.3.6	input current		–	–	0.2	mA
S.3.7	suppression of internal RGB signals	notes 5 and 23; insertion; f_i = 0 to 5 MHz	–	55	–	dB

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING INPUT (CONTINUED)						
S.3.8	suppression of external RGB signals	notes 5 and 23; no insertion; f_i = 0 to 5 MHz	–	55	–	dB
S.3.9	input voltage to blank the RGB outputs to facilitate 'On Screen Display' signals being applied to the outputs	only on pin 26 (pin 38 for the TDA 885X)	4	–	–	V
COLOUR DIFFERENCE OUTPUT AND INPUT SIGNALS (PINS 29, 30, 31 AND 32); NOTE 26						
S.4.1	signal amplitude (R–Y) (peak-to-peak value)	note 2	–	1.05	–	V
S.4.2	signal amplitude (B–Y) (peak-to-peak value)	note 2	–	1.33	–	V
LUMINANCE INPUTS AND OUTPUTS (PINS 27 AND 28); NOTE 26						
S.5.1	output signal amplitude (peak-to-peak value)	top sync-white	–	1.4	–	V
S.5.2	top sync level		–	2.0	–	V
S.5.3	output impedance		–	250	–	Ω
Chrominance filters						
CHROMINANCE TRAP CIRCUIT; NOTE 27						
F.1.1	trap frequency		–	f_{osc}	–	MHz
F.1.2	Bandwidth at fSC = 3.58 MHz	–3 dB	–	2.8	–	MHz
F.1.3	Bandwidth at fSC = 4.43 MHz	–3 dB	–	3.4	–	MHz
F.1.4	colour subcarrier rejection	at nominal peaking	20	30	–	dB
F.1.5	trap frequency during SECAM reception		–	4.3	–	MHz
CHROMINANCE BANDPASS CIRCUIT						
F.2.1	centre frequency (CB = 0)		–	f_{osc}	–	MHz
F.2.2	centre frequency (CB = 1)		–	$1.1xf_{osc}$	–	MHz
F.2.3	bandpass quality factor		–	3	–	
CLOCHE FILTER						
F.3.1	centre frequency		4.26	4.29	4.31	MHz
F.3.2	Bandwidth		241	268	295	kHz

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LUMINANCE PROCESSING						
Y DELAY LINE						
F.4.1	delay time	note 5	–	480	–	ns
F.4.2	tuning range delay time	8 steps	–160	–	+160	ns
F.4.3	bandwidth of internal delay line	note 5	8	–	–	MHz
PEAKING CONTROL; NOTE 28						
F.5.1	width of preshoot or overshoot	note 2	–	160	–	ns
F.5.2	peaking signal compression threshold		–	50	–	IRE
F.5.3	overshoot at maximum peaking	positive	–	45	–	%
F.5.4		negative	–	80	–	%
F.5.5	Ratio negative/positive overshoot		–	1.8	–	
F.5.6	peaking control curve	63 steps	see Fig.9			
CORING STAGE						
F.6.1	coring range		–	15	–	IRE
BLACK LEVEL STRETCHER; NOTE 29						
F.7.1	Maximum black level shift		15	21	27	IRE
F.7.2	level shift at 100% peak white		-1	0	1	IRE
F.7.3	level shift at 50% peak white		-1	–	3	IRE
F.7.4	level shift at 15% peak white		6	8	10	IRE

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal and vertical synchronization and drive circuits						
SYNC VIDEO INPUT (PINS 11, 13 AND 17)						
H.1.1	sync pulse amplitude	note 2	50	300	350	mV
H.1.2	slicing level for horizontal sync	note 30	–	50	–	%
H.1.3	slicing level for vertical sync	note 30	–	30	–	%
HORIZONTAL OSCILLATOR						
H.2.1	free running frequency		–	15625	–	Hz
H.2.2	spread on free running frequency		–	–	±2	%
H.2.3	frequency variation with respect to the supply voltage	V_P = 8.0 V ±10%; note 5	–	0.3	0.5	%
H.2.4	frequency variation with temperature	T_{amb} = 0 to 70 °C; note 5	–	–	100	Hz
FIRST CONTROL LOOP (FILTER CONNECTED TO PIN 43); NOTE 31						
H.3.1	holding range PLL		–	±0.9	±1.2	kHz
H.3.2	catching range PLL	note 5	±0.6	±0.9	–	kHz
H.3.3	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
H.3.4	hysteresis at the switching point		–	3	–	dB
SECOND CONTROL LOOP (CAPACITOR CONNECTED TO PIN 42)						
H.4.1	control sensitivity		–	120	–	µs/µs
H.4.2	control range from start of horizontal output to flyback at nominal shift position		–	19	–	µs
H.4.3	horizontal shift range	63 steps	±2	–	–	µs
H.4.4	control sensitivity for dynamic compensation		–	7.6	–	µs/V
H.4.5	Voltage to switch-on the “flash” protection	note 32	6	–	–	V
H.4.6	Input current during protection		–	–	1	mA
HORIZONTAL OUTPUT (PIN 40); NOTE 33						
H.5.1	LOW level output voltage	I_O = 10 mA	–	0.4	tbf	V
H.5.2	maximum allowed output current		10	–	–	mA
H.5.3	maximum allowed output voltage		–	–	V_P	V
H.5.4	duty factor	V_{OUT} = HIGH, note 5	–	45	–	%
H.5.5	frequency during switch-on and switch-off		–	2xfH	–	
H.5.6	duty factor during switch-on and switch-off		–	72	–	%

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL OUTPUT (CONTINUED)						
H.5.7	switch-on time		–	100	–	ms
H.5.8	switch-off time with RGB drive maximum	note 37	–	100/80	–	ms
H.5.9	switch-off time with RGB drive minimum	note 37	–	60	–	ms
FLYBACK PULSE INPUT AND SANDCASTLE OUTPUT (PIN 41)						
H.6.1	required input current during flyback pulse	note 2	100	–	300	µA
H.6.2	output voltage	during burst key	4.8	5.3	5.8	V
		during blanking	1.9	2.1	2.3	V
H.6.3	clamped input voltage during flyback		2.6	3.0	3.4	V
H.6.4	pulse width	burst key pulse	3.3	3.5	3.7	µs
H.6.5		vertical blanking, note 34	–	14	–	lines
H.6.6	delay of start of burst key to start of sync		5.2	5.4	5.6	µs
VERTICAL OSCILLATOR; NOTE 35						
H.7.1	free running frequency		–	50/60	–	Hz
H.7.2	locking range		45	–	64.5/72	Hz
H.7.3	divider value not locked		–	625/525	–	lines
H.7.4	locking range		434/488	–	722	lines/ frame
VERTICAL RAMP GENERATOR (PIN 51 AND 52)						
H.8.1	sawtooth amplitude (peak-to-peak value)	VS = 1FH; C = 100 nF; R = 39 kΩ	–	3.0	–	V
H.8.2	discharge current		–	0.9	–	mA
H.8.3	charge current set by external resistor	note 36	–	16	–	µA
H.8.4	vertical slope	control range (63 steps)	–20	–	+20	%
H.8.5	charge current increase	f = 60 Hz	–	19	–	%
H.8.6	LOW level of ramp		–	2.3	–	V
VERTICAL DRIVE OUTPUTS (PINS 46 AND 47)						
H.9.1	differential output current (peak-to-peak value)	VA = 1FH	–	0.95	–	mA
H.9.2	common mode current		–	400	–	µA
H.9.3	output voltage range		0	–	4.0	V
EHT TRACKING/OVERVOLTAGE PROTECTION (PIN 50)						
H.10.1	input voltage		1.2	–	2.8	V
H.10.2	scan modulation range		–5	–	+5	%
H.10.3	vertical sensitivity		–	6.3	–	%/V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EHT TRACKING/OVERVOLTAGE PROTECTION (CONTINUED)						
H.10.4	EW sensitivity	when switched-on	–	–6.3	–	%/V
H.10.5	EW equivalent output current		+100	–	–100	µA
H.10.6	overvoltage detection level	note 32	–	3.9	–	V
DE-INTERLACE						
H.11.1	first field delay		–	0.5H	–	
EW WIDTH; NOTE 38						
H.12.1	control range	63 steps	100	–	65	%
H.12.2	equivalent output current		0	–	700	µA
H.12.3	EW output voltage range		1.0	–	8.0	V
H.12.4	EW output current range		0	–	1200	µA
EW PARABOLA/WIDTH						
H.13.1	control range	63 steps	0	–	22	%
H.13.2	equivalent output current	EW = 3FH	0	–	440	µA
EW CORNER/PARABOLA						
H.14.1	control range	63 steps	–43	–	0	%
H.14.2	equivalent output current	PW = 3FH; EW = 3FH	–190	–	0	µA
EW TRAPEZIUM						
H.15.1	control range	63 steps	–5	–	+5	%
H.15.2	equivalent output current		–100	–	+100	µA
VERTICAL AMPLITUDE						
H.16.1	control range	63 steps; SC = 00H	80	–	120	%
H.16.2	equivalent differential vertical drive output current (peak-to-peak value)	SC = 00H	760	–	1140	µA
VERTICAL SHIFT						
H.17.1	control range	63 steps	–5	–	+5	%
H.17.2	equivalent differential vertical drive output current (peak-to-peak value)		–50	–	+50	µA
S-CORRECTION						
H.18.1	control range	63 steps	0	–	30	%
VERTICAL ZOOM MODE (OUTPUT CURRENT VARIATION WITH RESPECT TO NOMINAL SCAN); NOTE 39						
H.19.1	vertical expand factor		0.75	–	1.38	
H.19.2	output current limiting and RGB blanking		–	1.05	–	
VERTICAL SCROLL						
H.20.1	Control range (percentage of nominal picture amplitude)		-18	–	19	%

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour demodulation part						
CHROMINANCE AMPLIFIER						
D.1.1	ACC control range	note 40	26	–	–	dB
D.1.2	change in amplitude of the output signals over the ACC range		–	–	2	dB
D.1.3	threshold colour killer ON		–30	–	–	dB
D.1.4	hysteresis colour killer OFF	strong signal conditions; S/N ≥ 40 dB; note 5	–	+3	–	dB
D.1.5		noisy input signals; note 5	–	+1	–	dB
ACL CIRCUIT; NOTE 41						
D.2.1	chrominance burst ratio at which the ACL starts to operate		–	3.0	–	
REFERENCE PART						
Phase-locked loop; note 42						
D.3.1	catching range		±360	±600	–	Hz
D.3.2	phase shift for a ±400 Hz deviation of the oscillator frequency	note 5	–	–	2	deg
Oscillator						
D.4.1	temperature coefficient of the oscillator frequency	note 5	–	–	1	Hz/K
D.4.2	oscillator frequency deviation with respect to the supply	note 5; V_P = 8 V ±10%	–	–	25	Hz
D.4.3	minimum negative resistance		–	–	1.0	kΩ
D.4.4	maximum load capacitance		–	–	15	pF
HUE CONTROL						
D.5.1	hue control range	63 steps; see Fig.10	±35	±40	–	deg
D.5.2	hue variation for ±10% V_P	note 5	–	0	–	deg
D.5.3	hue variation with temperature	T_{amb} = 0 to 70 °C; note 5	–	0	–	deg
DEMODULATORS (PINS 29 AND 30)						
General						
D.6.1	(R–Y) output signal amplitude (peak-to-peak value)	note 43	–	1.05	–	V
D.6.2	(B–Y) output signal amplitude (peak-to-peak value)	note 43	–	1.33	–	V
D.6.3	spread of signal amplitude ratio between standards	note 5	–1.5	–	+1.5	dB
D.6.4	output impedance (R–Y)/(B–Y) output	note 5	–	500	–	Ω
D.6.5	bandwidth of demodulators	–3 dB; note 44	–	650	–	kHz

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/NTSC demodulator						
D.6.6	gain between both demodulators G(B–Y) and G(R–Y)		1.60	1.78	1.96	
D.6.7	residual carrier output (peak-to-peak value); only valid for PAL and NTSC signals	f = f_{osc}; (R–Y) output	–	–	10	mV
D.6.8		f = f_{osc}; (B–Y) output	–	–	10	mV
D.6.9		f = $2f_{osc}$; (R–Y) output	–	–	10	mV
D.6.10		f = $2f_{osc}$; (B–Y) output	–	–	10	mV
D.6.11	H/2 ripple at (R–Y) output (peak-to-peak value)		–	–	25	mV
D.6.12	change of output signal amplitude with temperature	note 5	–	0.1	–	%/K
D.6.13	change of output signal amplitude with supply voltage	note 5	–	–	±0.2	dB
D.6.14	phase error in the demodulated signals	note 5	–	–	±8	deg
SECAM demodulator						
D.7.1	black level off-set		–	–	7	kHz
D.7.2	pole frequency of deemphasis		77	85	93	kHz
D.7.3	ratio pole and zero frequency		–	3	–	
D.7.4	non linearity		–	–	3	%
D.7.5	calibration voltage pin 16		3	4	5	V
Base-band delay line						
D.8.1	variation of output signal for adjacent time samples at constant input signals		-0.1	–	0.1	dB
D.8.2	residual clock signal (peak-to-peak value)		–	–	5	mV
D.8.3	delay of delayed signal		63.94	64.0	64.06	µs
D.8.4	delay of non-delayed signal		40	60	80	ns
D.8.5	difference in output amplitude with delay on or off		–	–	5	%

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COLOUR DIFFERENCE MATRICES (IN CONTROL CIRCUIT)						
TDA 8840/41/42/43/44/54: PAL/SECAM mode; (R–Y) and (B–Y) not affected						
D.9.1	ratio of demodulated signals		–	–0.51 ±10%	–	
D.9.2	ratio of demodulated signals		–	–0.19 ±25%	–	
TDA 8840/41/42/43/44/54: NTSC mode; the matrix results in the following signals (nominal hue setting)						
D.9.3	(B–Y) signal: 2.03/0°			$2.03U_R$		
D.9.4	(R–Y) signal: 1.59/95°			$-0.14U_R + 1.58V_R$		
D.9.5	(G–Y) signal: 0.61/240°			$-0.31U_R - 0.53V_R$		
TDA 8846/46A/47/57; the matrix results in the following signals (nominal hue setting)						
MAT-bit = 0						
D.9.6	(B–Y) signal: 2.03/0°			$2.03U_R$		
D.9.7	(R–Y) signal: 1.59/95°			$-0.14U_R + 1.58V_R$		
D.9.8	(G–Y) signal: 0.61/240°			$-0.31U_R - 0.53V_R$		
MAT-bit = 1						
D.9.9	(B–Y) signal: 2.20/-1°			$2.20U_R - 0.04V_R$		
D.9.10	(R–Y) signal: 1.53/99°			$-0.24U_R + 1.51V_R$		
D.9.11	(G–Y) signal: 0.70/223°			$-0.51U_R - 0.48V_R$		
REFERENCE SIGNAL OUTPUT PIN 33; NOTE 45						
D.10.1	reference frequency			3.58/4.43		MHz
D.10.2	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
D.10.3	output level to enable the comb filter		4.0	4.2	5.0	V
D.10.4	output level to disable the comb filter		–	0.1	1.4	V
DYNAMIC SKIN TONE (FLESH) CONTROL; NOTE 46						
D.11.1	control angle	DSA=0	–	123	–	deg
D.11.2	control angle	DSA=1	–	117	–	deg
D.11.3	correction range (angle)		–	45	–	deg

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Control part						
SATURATION CONTROL; NOTE 25						
C.1.1	saturation control range	63 steps; see Fig.11	52	–	–	dB
CONTRAST CONTROL; NOTE 25						
C.2.1	contrast control range	63 steps	–	18	–	dB
C.2.2	tracking between the three channels over a control range of 10 dB	see Fig.12	–	–	0.5	dB
BRIGHTNESS CONTROL						
C.3.1	brightness control range	63 steps; see Fig.13	–	±0.7	–	V
RGB AMPLIFIERS (PINS 19, 20 AND 21)						
C.4.1	output signal amplitude (peak-to-peak value)	at nominal luminance input signal, nominal contrast and white-point adjustment;	tbf	2.0	tbf	V
C.4.2	maximum signal amplitude (black-to-white)	note 47	–	tbf	–	V
C.4.3	input signal amplitude (Y-input, pin 27) at which the soft clipping is activated	note 47	–	tbf	–	V
C.4.4	output signal amplitude for the ‘red’ channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL)	tbf	2.1	tbf	V
C.4.5	nominal black level voltage		–	2.4	–	V
C.4.6	black level voltage	when black level stabilisation is switched-off (via AKB bit)	–	2.5	–	V
C.4.61	black level voltage control range	VSD bit active; note 48	1.8	2.5	3.2	V
C.4.7	width of video blanking with HBL bit active	note 49	14.4	14.7	15.0	µs
C.4.8	control range of the black-current stabilisation		–	±1	–	V
C.4.9	blanking level	difference with black level, note 47	–	-0.5	–	V
C.4.10	level during leakage measurement		–	-0.1	–	V
C.4.11	level during “low” measuring pulse		–	0.25	–	V
C.4.12	level during “high” measuring pulse		–	0.38	–	V
C.4.13	adjustment range of the ratio between the amplitudes of the RGB drive voltage and the measuring pulses	note 47	–	±3	–	dB
C.4.14	variation of black level with temperature	note 5	–	1.0	–	mV/K

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB AMPLIFIERS (CONTINUED)						
C.4.15	relative variation in black level between the three channels during variations of	note 5				
C.4.16	supply voltage (±10%)	nominal controls	–	–	tbf	mV
C.4.17	saturation (50 dB)	nominal contrast	–	–	tbf	mV
C.4.18	contrast (20 dB)	nominal saturation	–	–	tbf	mV
C.4.19	brightness (±0.5 V)	nominal controls	–	–	tbf	mV
C.4.20	temperature (range 40 °C)		–	–	tbf	mV
C.4.21	signal-to-noise ratio of the output signals	RGB input; note 50	60	–	–	dB
C.4.22		CVBS input; note 50	50	–	–	dB
C.4.23	residual voltage at the RGB outputs (peak-to-peak value)	at f_{osc}	–	–	15	mV
C.4.24		at $2f_{osc}$ plus higher harmonics	–	–	15	mV
C.4.25	bandwidth of output signals	RGB input; at –3 dB	9	–	–	MHz
C.4.26		CVBS input; at –3 dB; f_{osc} = 3.58 MHz	–	2.8	–	MHz
C.4.27		CVBS input; at –3 dB; f_{osc} = 4.43 MHz	–	3.5	–	MHz
C.4.28		S-VHS input; at –3 dB	6	–	–	MHz
WHITE-POINT ADJUSTMENT						
C.5.1	I²C-bus setting for nominal gain	HEX code	–	20H	–	
C.5.2	adjustment range of RGB drive levels		–	±3	–	dB
C.5.3	gain control range to compensate spreads in picture tube characteristics		–	±6	–	dB
2-POINT BLACK-CURRENT STABILISATION (PIN 18); NOTE 51						
C.6.1	amplitude of “low” reference current		–	8	–	µA
C.6.2	amplitude of “high” reference current		–	20	–	µA
C.6.3	acceptable leakage current		–	±100	–	µA
C.6.4	maximum current during scan		–	tbf	–	mA
C.6.5	input impedance		–	tbf	–	Ω
BEAM CURRENT LIMITING (PIN 22); NOTE 52						
C.7.1	contrast reduction starting voltage		–	3.0	–	V
C.7.2	voltage difference for full contrast reduction		–	1.8	–	V
C.7.3	brightness reduction starting voltage		–	1.9	–	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BEAM CURRENT LIMITING (CONTINUED)						
C.7.4	voltage difference for full brightness reduction		–	1	–	V
C.7.5	internal bias voltage		–	3.3	–	V
C.7.6	detection level vertical guard		–	3.65	–	V
C.7.7	minimum input current to activate the guard circuit		–	100	–	µA
C.7.8	maximum allowable current		–	1	–	mA
BLUE STRETCH; NOTE 53						
C.8.1	decrease of small signal gain for the red and green channel	BLS = 1	–	14	–	%
C.8.2	decrease of small signal gain for the red channel	EBS = 1	–	22	–	%
C.8.3	decrease of small signal gain for the green channel	EBS = 1	–	8	–	%
I²C-BUS CONTROL INPUT/OUTPUT (SDA/SCL)						
B.1.1	input voltage level		0	–	5.5	V
B.1.2	low-level input voltage		–	–	1.5	V
B.1.3	high-level input voltage		3.5	–	–	V
B.1.4	low-level input current	V_i = 0 V	–	–	-10	µA
B.1.5	high-level input current	V_i = 5.5 V	–	–	10	µA
B.1.6	low-level output voltage	SDA, I_L = 3 mA	–	–	0.4	V

Notes

1. On set AGC.
2. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
3. Loop bandwidth BL = 60 kHz (natural frequency fN = 15 kHz; damping factor d = 2; calculated with top sync level as FPLL input signal level).
4. The IF-PLL demodulator uses an internal VCO (no external LC-circuit required) which is calibrated by means of a digital control circuit which uses the X-tal frequency of the colour decoder as a reference. The required IF frequency for the various standards is set via the I²C-bus (IFA-IFC bits in sub-address 15H). When the system is locked the resulting IF frequency is very accurate with a deviation from the nominal value of less than 25 kHz.
5. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
6. Measured at 10 mV (RMS) top sync input signal.
7. So called projected zero point, i.e. with switched demodulator.
8. Measured in accordance with the test line given in Fig.14. For the differential phase test the peak white setting is reduced to 87%.

   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.

   The phase difference is defined as the difference in degrees between the largest and smallest phase angle.

9. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.15.
10. The noise inverter is only active in the “strong signal mode” (no noise detected in the incoming signal)
11. The test set-up and input conditions are given in Fig.16. The figures are measured with an input signal of 10 mV RMS. The indicated parameter values are obtained when a capacitor with a value of 1 nF is connected in parallel with the PLL loop filter on pin 5.
12. Measured at an input signal of 10 mV_{RMS}. The S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value). B = 5 MHz. Weighted in accordance with CCIR 567.
13. The AGC response time is also dependent on the acquisition time of the PLL demodulator. The values given are valid when the PLL is in lock.
14. The AFC control voltage is generated by the digital tuning system of the PLL demodulator. This system uses the X-tal frequency of the colour decoder as a reference and is therefore very accurate. For this reason no maximum and minimum values are given for the window sensitivity figures (parameters M.7.2 and M.7.3). The tuning information is supplied to the tuning system via the I²C-bus. 2 bits are reserved for this function. The AFC value is valid only when the SL-bit is 1.
15. The ratio of the output signal amplitudes of the deemphasis pin (pin 55) and the audio output (pin 15) is dependent on the type and/or the frequency of the X-tals connected to the IC (indicated via the XA/XB bits). The indicated values are valid for the PAL, PAL/NTSC and multi-standard versions when a 4.43 MHz X-tal is connected to pin 35 (pin 51 in the QFP-64 envelope). For the NTSC types and the other IC’s (when only 3.5 MHz X-tals are used) the gain between the deemphasis output and the audio output is a factor 2 higher so that the audio output signal is not effected by the lower frequency deviation of the M/N standard.

    The test conditions are: Vi = 100 mV_{RMS}, FM: 1 kHz, $\Delta f = \pm$ 25/50 kHz.
16. Vi = 50 mV_{RMS}, f = 4.5/5.5 MHz; FM: 70 Hz, +/- 50 kHz deviation; AM: 1.0 kHz, 30% modulation.
17. Vi = 100 mV_{RMS}, f = 5.5 MHz; FM: 1 kHz, +/- 17.5 kHz deviation. Measured with a bandwidth of 15 kHz and the audio attenuator at -6 dB.
18. Vi = 100 mV_{RMS}, f = 4.5 MHz, FM: 1 kHz, +/- 100 kHz deviation.
19. Unweighted RMS value, Vi = 100 mV_{RMS}, FM: 1 kHz, +/- 50 kHz deviation, audio attenuator at -6 dB.
20. Audio attenuator at -20 dB; temperature range 10 to 50 °C.
21. The Automatic Volume Levelling (AVL) circuit stabilises automatically the audio output signal to a certain level which can be set by means of the volume control. This AVL function prevents big audio output fluctuations due to variation of the modulation depth of the transmitter. The AVL can be switched on and off via the I²C-bus.

    For the TDA 8846/46A the AVL is active over an input voltage range (measured at the deemphasis output) between 75 and 750 mV_{RMS}. For the TDA 8840/41/42 this input level is dependent on the X-tals which are connected to the colour decoder. When only 3.5 MHz X-tals are connected (indicated via the XA/XB bits) the active input level is identical to that of the TDA 8846/46A. When a 4.4 MHz X-tal is connected the input range is increased to 150 to 1500 mV_{RMS}, this to cope with the larger FM swing of European transmitters.

    The AVL control curve for the 2 standards is given in Fig.17 and Fig.18. The control range of +6 dB to –14 dB is valid for input signals with 50% of the maximum frequency deviation.
22. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
23. This parameter is measured at nominal settings of the various controls.
24. Indicated is a signal for a colour bar with 75% saturation (chroma : burst ratio = 2.2 : 1).
25. The saturation control is active on the internal signal (YUV) and on the second RGB input. The contrast control is active on YUV and the 2 RGB inputs. Nominal contrast is specified with the DAC in position 20 HEX. Nominal saturation as maximum -10 dB.

26. Several versions have a YUV interface. The luminance and colour difference out- and inputs can directly be connected. When additional picture improvement IC's (like the TDA 9170) are applied the inputs of these IC's must be ac coupled because of the black level clamp requirement. The output signal of the picture improvement IC can directly be coupled to the luminance and colour difference inputs as long as the dc level of these signals have a value between 1 and 7 Volts (for the luminance signal) or between 1 and 4 Volts (for the UV signals). When the dc level of the input signals exceed these levels the signals must be ac coupled and biased to a voltage level within these limits.

    To be able to apply CTI IC's like the TDA 4565/66 the gain of the luminance channel can be increased via the setting of the GAI bit in the I²C subaddress 03.

27. When the decoder is forced to a fixed subcarrier frequency (via XA/XB or the CM-bits) the chroma trap is always switched-on, also when no colour signal is identified. When 2 X-tals are active the chroma trap is switched-off when no colour signal is identified.

28. Valid for a signal amplitude on the Y-input of 0.7 V black-to-white (100 IRE) with a rise time (10% to 90%) of 70 ns and the video switch in the Y/C mode. During production the peaking function is not tested by measuring the overshoots but by measuring the frequency response of the Y output.

29. For video signals with a black level which deviates from the back-porch blanking level the signal is "stretched" to the blanking level. The amount of correction depends on the IRE value of the signal (see Fig.19). The black level is detected by means of an internal capacitor. The black level stretcher can be switched on and off via the BKS bit in the I²C-bus. The values given in the specification are valid only when the luminance input signal has an amplitude of 1 V_{p-p}.

30. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch). When the amplitude of the sync pulse exceeds the value of 350 mV the sync separator will slice the sync pulse at a level of 175 mV above top sync. The maximum sync pulse amplitude is 4 V_{p-p}.

31. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the I²C-bus. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when too much noise is present in the signal. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching between the two modes can be automatically or overruled by the I²C-bus.

    The circuit contains a video identification circuit which is independent of first loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input. The coupling of the video identification circuit with the first loop can be defeated via the I²C-bus.

    To prevent that the horizontal synchronisation is disturbed by anti copy signals like Macrovision the phase detector is gated during the vertical retrace period so that pulses during scan have no effect on the output voltage. The width of the gate pulse is about 22 μs. During weak signal conditions (noise detector active) the gating is active during the complete scan period and the width of the gate pulse is reduced to 5.7 μs so that the effect of noise is reduced to a minimum.

    The output current of the phase detector in the various conditions are shown in Table 75.

32. The IC's have 2 protection inputs. The protection on pin 42 is intended to be used as "flash" protection. When this protection is activated the horizontal drive is switched-off immediately and then switched-on again via the slow start procedure.

    The protection on pin 50 is intended for overvoltage (X-ray) protection. When this protection is activated the horizontal drive can directly be switched-off (via the slow stop procedure). It is also possible to continue the horizontal drive and to set the protection bit (XPR) in the output bytes of the I²C-bus. The choice between the 2 modes of operation is made via the PRD bit.

33. During switch-on the horizontal output starts with the double frequency and with a duty cycle of 75% (VOUT = high). After about 50 ms the frequency is changed to the normal value. Because of the high frequency the peak currents in the horizontal output transistor are limited. Also during switch-off the frequency is switched to the double value and the RGB drive is set to maximum so that the EHT capacitor is discharged. The switching to maximum drive occurs only when RBL=0, for RBL=1 the drive voltage remains minimum during switch-off. After about 100 ms the RGB drive is set to minimum and 50 ms later the horizontal drive is switched-off.

    It is possible to discharge the EHT capacitor in the vertical overscan so that the screen stays black during switch-off. This feature is activated by the OSO bit. In this condition the vertical scan is stopped and the current is set to the maximum scan value. It should be checked with the picture tube supplier whether this mode of switch-off is allowed for the given picture tube.

    The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched-on during the flyback time.

34. The vertical blanking pulse in the RGB outputs has a width of 26 or 21 lines (50 or 60 Hz system). The vertical pulse in the sandcastle pulse has a width of 14 lines. This to prevent a phase distortion on top of the picture due to a timing modulation of the incoming flyback pulse.

35. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. During TV reception this divider circuit has 3 modes of operation:

    a) Search mode ‘large window’.

        This mode is switched on when the circuit is not synchronized or when a non-standard signal (number of lines per frame outside the range between 311 and 314(50 Hz mode) or between 261 and 264 (60 Hz mode) is received). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).

    b) Standard mode ‘narrow window’.

        This mode is switched on when more than 15 succeeding vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

    c) Standard TV-norm (divider ratio 525 (60 Hz) or 625 (50 Hz).

        When the system is switched to the narrow window it is checked whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

        When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

    The vertical divider needs some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of the NCIN bit in subaddress 08.

    When RGB signals are inserted the maximum vertical frequency is increased to 72 Hz. This has the consequence that the circuit can also be synchronised by signals with a higher vertical frequency like VGA.

36. Conditions: frequency is 50 Hz; normal mode; VS = 1F.

37. During switch-off the RGB drive outputs are shortly set to maximum so that the EHT capacitor of the picture tube can be discharged. The switch-off behaviour depends on the switch-off mode. When the vertical scan is set in the overscan during switch-off the RGB outputs are first set to minimum during 20 ms, then the drive is set to maximum during 80 ms followed by a period of 60 ms with the drive on minimum. When the vertical scan is active during switch-off the RGB drive voltages are directly set to maximum when the switch-off command is given. The output remain high during a period of 100 ms followed by a period of 60 ms with the drive on minimum.

38. The output range percentages mentioned for E-W control parameters are based on the assumption that 400 μA variation in E-W output current is equivalent to 20% variation in picture width.

39. The IC's have a zoom adjustment possibility for the horizontal and vertical deflection. For this reason an extra DAC has been added in the vertical amplitude control which controls the vertical scan amplitude between 0.75 and 1.38 of the nominal scan. At an amplitude of 1.05 of the nominal scan the output current is limited and the blanking of the RGB outputs is activated. This is illustrated in Fig.21. In addition to the variation of the vertical amplitude a vertical scroll function is introduced so that it is always possible to display the most important part of the picture.

    The nominal scan height must be adjusted at a position of 19 HEX of the vertical "zoom" DAC and 1F HEX of the vertical scroll DAC.

40. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and −20 dB.

41. The ACL function can be activated by via the ACL bit in the I²C subaddress 19. The ACL circuit reduces the gain of the chroma amplifier for input signals with a chroma-to-burst ratio which exceeds a value of 3.0.

42. All frequency variations are referenced to 3.58 or 4.43 MHz carrier frequency.
    All oscillator specifications are measured with the Philips crystal series 9922 520 with a series capacitance of 18 pF. The oscillator circuit is rather insensitive to the spurious responses of the X-tal. As long as the resonance resistance of the third overtone is higher than that of the fundamental frequency the oscillator will operate at the right frequency.

    The typical crystal parameters for the X-tals mentioned above are:

    a) Load resonance frequency f_0 = 4.433619 or 3.579545 MHz; C_L = 20 pF.

    b) Motional capacitance C_M = 20.5 fF (4.43 MHz crystal) or 14.5 fF (3.58 MHz crystal).

    c) Parallel capacitance C_0 = 5.0 pf for both X-tals.

    The minimum detuning range can only be specified if both the IC and the X-tal tolerances are known and therefore the figures regarding catching range are only valid for the specified X-tal series. In this figure tolerances of the X-tal with respect to the nominal frequency, motional capacitance and ageing have been taken into account and have been counted for by gaussic addition.

    Whenever different typical X-tal parameters are used the following equation might be helpful for calculating the impact on the tuning capabilities:

    Detuning range = $C_M / (1 + C_0/C_L)^2$

    The resulting detuning range should be corrected for temperature shift and supply voltage deviation of both the IC and the X-tal. To guarantee a catching range of ±300 Hz on 4.43 MHz the minimum motional cpacitance of the X-tal must have a value 13.2 fF or higher. For a catching range of 250 Hz with the 3.58 MHz X-tal the minimum motional cpacitance must have a value of 9 fF.

    The actual series capacitance in the application should be CL = 18 pF to account for parasitic capacitances on and off chip.

    For 3-norma applications with 2 X-tals connected to one pin the maximum parasitic capacitance of the X-tal pin should not exceed 15 pF.

43. Because the base-band delay line is integrated the demodulated colour difference signals are matrixed before they are supplied to the outputs. The colour difference out- and inputs must be dc coupled.

44. This parameter indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the low-pass filter of the demodulator is approximately 1 MHz.

45. The subcarrier output signal can be used as reference signal for external comb filter IC's (e.g. SAA 4961). When the CMB bit is low the subcarrier signal is suppressed and the dc level is low. With the CMB bit high the output level is high and the subcarrier signal is present.

46. The Dynamic Skin Tone Correction circuit is designed such that it corrects (instantaneously and locally) the hue of those colours which are located in the area in the UV plane that matches to skin tones. The correction is dependent on the luminance, saturation and distance to the preferred axis and can be realised for 2 different angles. This angle can be set by means of the DSA bit. Because the amount of correction is dependent on the parameters of the incoming YUV signal it is not possible to give exact figures for the correction angle. The correction angle of 45 (+/-22.5) degrees is just given as an indication and is valid for an input signal with a luminance signal amplitude of 75% and a colour saturation of 50%. A graphical representation of the control behaviour is given in Fig.20.

47. Because of the 2-point black current stabilisation circuit both the black level and the amplitude of the RGB output signals depend on the drive characteristic of the picture tube. The system checks whether the returning measuring currents meet the requirement and adapts the output level and gain of the circuit when necessary. Therefore the typical value of the black level and amplitude at the output are just given as an indication for the design of the RGB output stage.

    The 2-point black level system adapts the drive voltage for each cathode in such a way that the 2 measuring currents have the right value. This has the consequence that a change in the gain of the output stage will be compensated by a gain change of the RGB control circuit. Because different picture tubes may require different drive voltage amplitudes the ratio between the output signal amplitude and the inserted measuring pulses can be adapted via the I²C-bus. This is indicated in the parameter “Adjustment range of the ratio between the amplitudes of the RGB drive voltage and the measuring pulses”.

    Because of the dependence of the output signal amplitude on the application the soft clipping limiting has been related to the input signal amplitude.

48. For the alignment of the picture tube the vertical scan can be stopped by means of the VSD bit. In that condition a certain black level is inserted at the RGB outputs. The value of this level can be adjusted by means of the brightness control DAC.
49. When the reproduction of 4:3 pictures on a 16:9 picture tube is realised by means of a reduction of the horizontal scan amplitude the edges of the picture may slightly be disturbed. This effect can be prevented by adding an additional blanking to the RGB signals. The blanking pulse is derived form the horizontal oscillator and is directly related to the incoming video signal (independent of the flyback pulse). The additional blanking overlaps the normal blanking signal with about 1 µs on both sides. This blanking is activated with the HBL bit (only in the TDA8843/44/47/54/57).
50. Signal-to-noise ratio (S/N) is specified as peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
51. This is a current input.
52. The beam current limiting and the vertical guard function have been combined on this pin. The beam current limiting function is active during the vertical scan period.
53. Via the “blue stretch” (BLS bit) or “extended blue stretch” (EBS bit) function the colour temperature of the bright scenes (amplitudes which exceed a value of 80% of the nominal amplitude) can be increased. This effect is obtained by decreasing the small signal gain of the red and green channel signals which exceed the 80% level. The effect is illustrated in Fig.22.

Table 75 Output current of the phase detector in the various conditions

I²C-BUS COMMANDS				IC CONDITIONS			φ-1 CURRENT/MODE			
VID	**POC**	**FOA**	**FOB**	**IDENT**	**COIN**	**NOISE**	**SCAN**	**V-RETR**	**GATING**	**MODE**
–	0	0	0	yes	yes	no	180	270	yes 1)	auto
–	0	0	0	yes	yes	yes	30	30	yes	auto
–	0	0	0	yes	no	–	180	270	no	auto
–	0	0	1	yes	yes	–	30	30	yes	slow
–	0	0	1	yes	no	–	180	270	no	slow
–	0	1	0	yes	yes	no	180	270	yes	fast
–	0	1	0	yes	yes	yes	30	30	yes	slow
–	–	1	1	–	–	–	180	270	no	fast
0	0	–	–	no	–	–	6	6	no	OSD
–	1	–	–	–	–	–	–	–	–	off

Note

1. Only during vertical retrace, width 22 μs. In the other conditions the width is 5.7 μs and the gating is continuous.

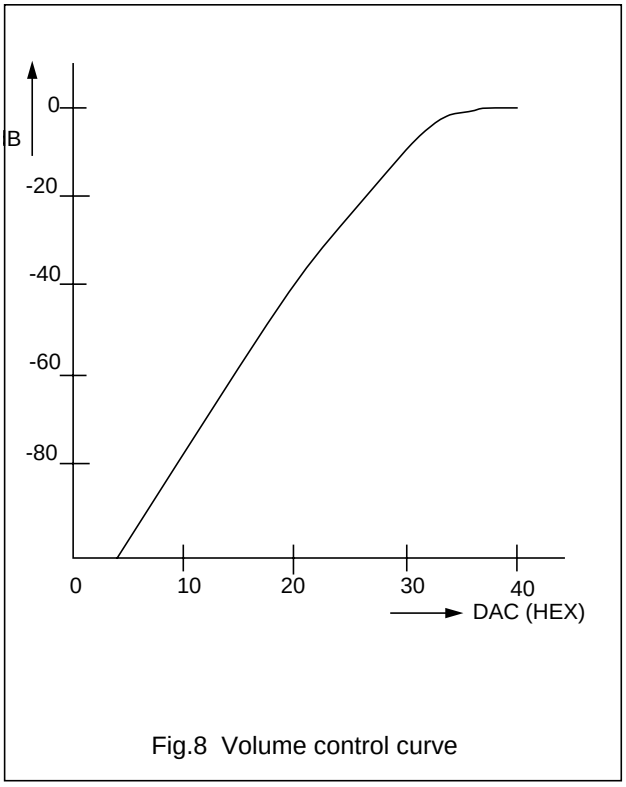
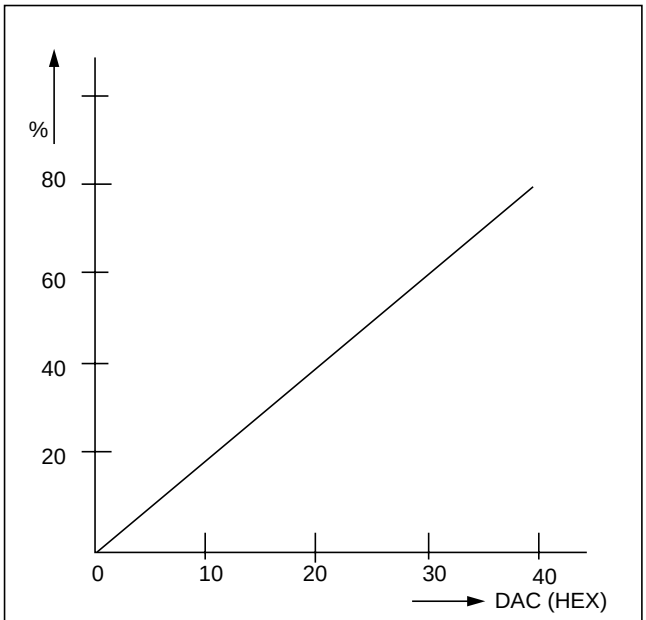


Fig.8 Volume control curve



Overshoot in direction 'black'.

Fig.9 Peaking control curve.

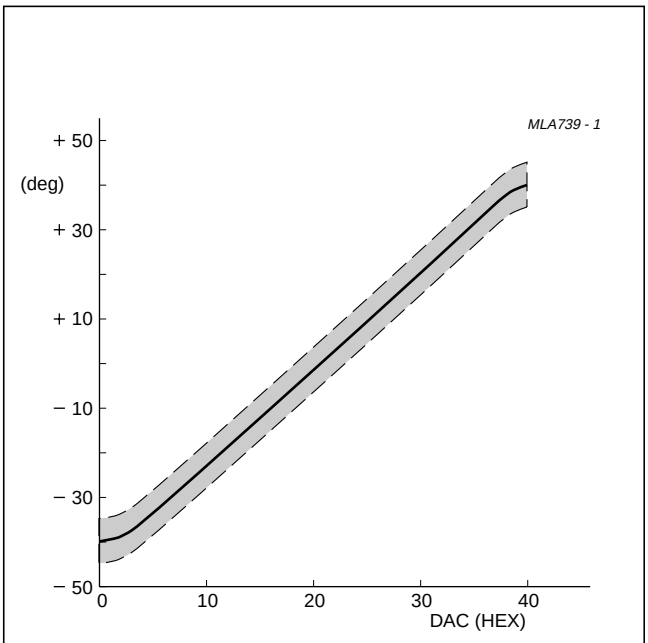


Fig.10 Hue control curve.

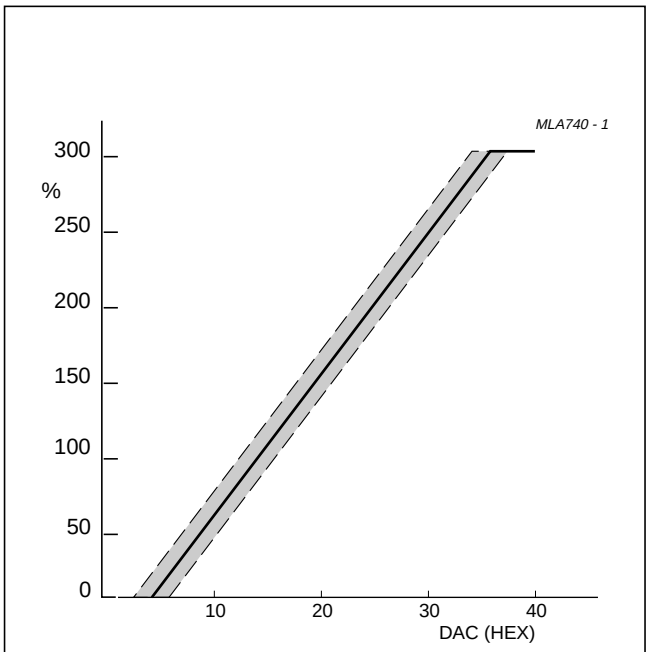


Fig.11 Saturation control curve.

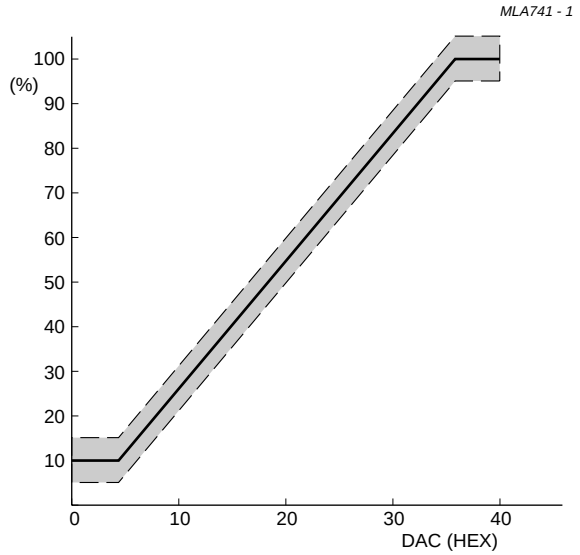


Fig.12 Contrast control curve.

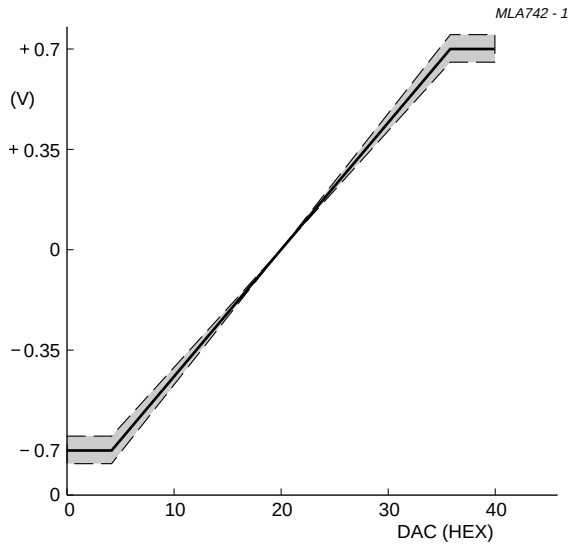


Fig.13 Brightness control curve.

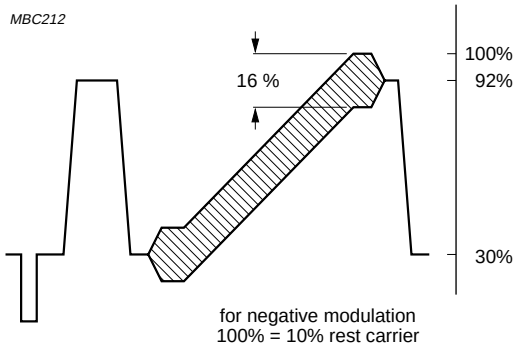


Fig.14 Video output signal.

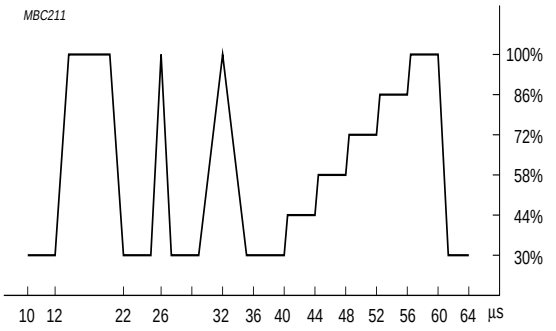
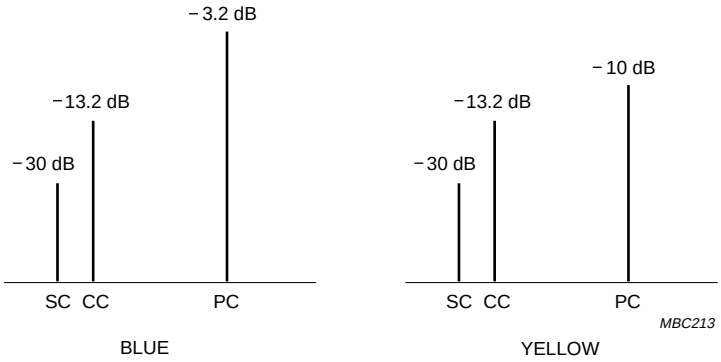
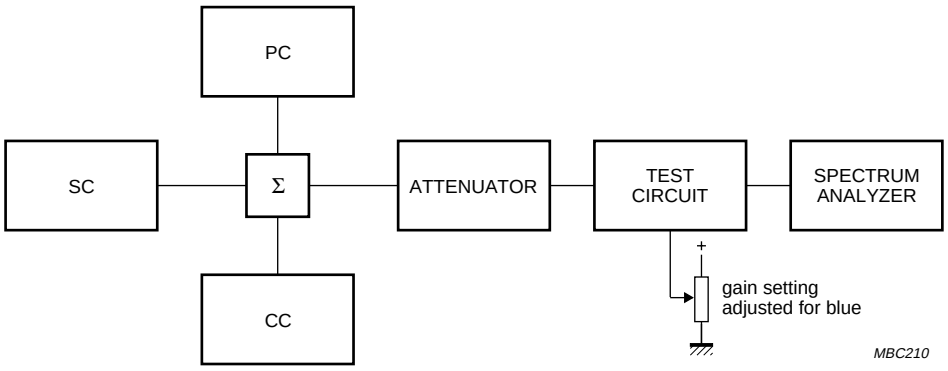


Fig.15 Test signal waveform.





Input signal conditions: SC = sound carrier; CC = colour carrier; PC = picture carrier.
All amplitudes with respect to top sync level.

$$\text{Value at 0.92 or 1.1 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 0.92 or 1.1 MHz}} + 3.6 \text{ dB}$$

$$\text{Value at 2.66 or 3.3 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 2.66 or 3.3 MHz}}$$

Fig.16 Test set-up intermodulation.

CHARACTERISTIC POINTS AVL	A	B	C	D	UNIT
Deemphasis voltage	75	150	250	750	mV_{RMS}
FM swing	7.5	15	25	75	kHz

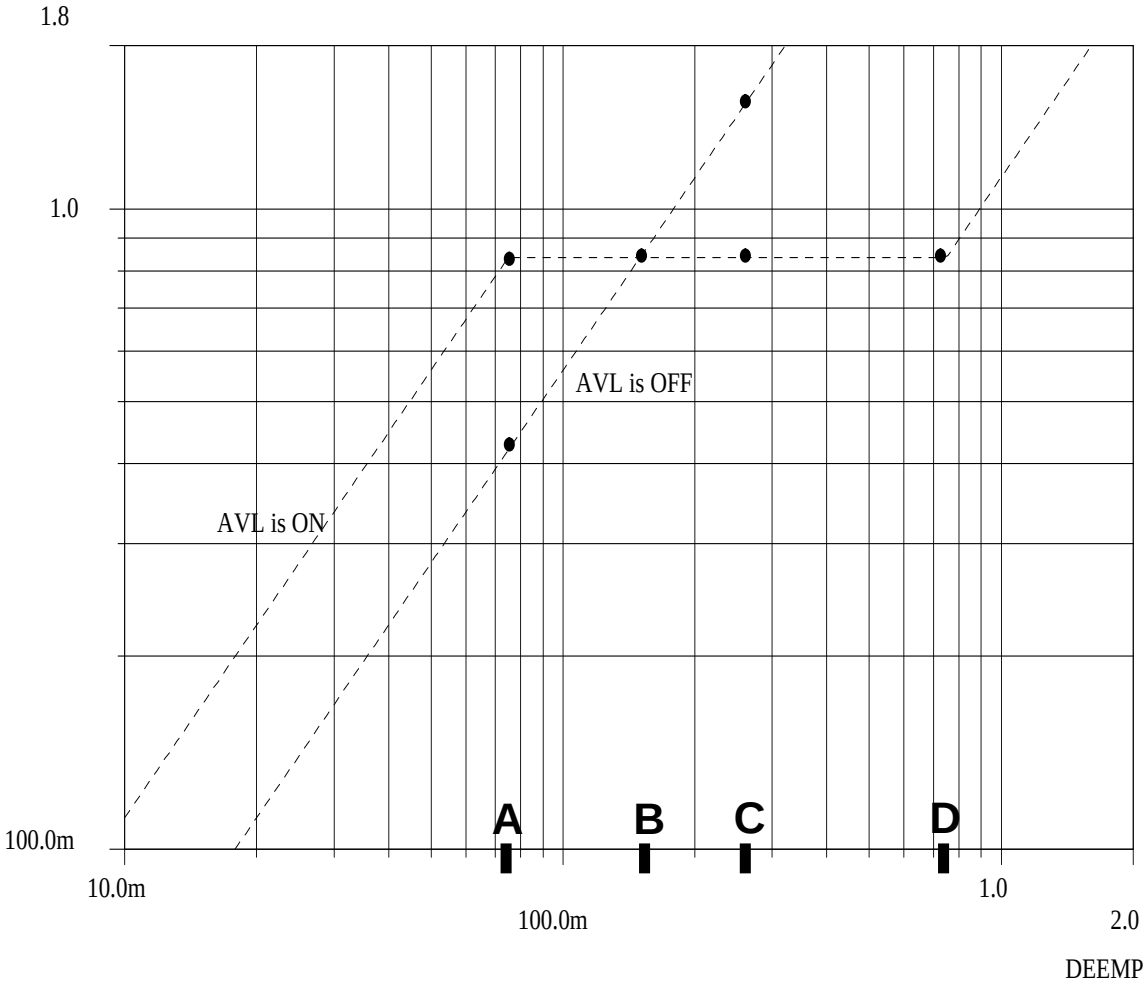


Fig.17 AVL characteristic for TDA 8840/41/42/46/46A for 3.5 MHz standard

CHARACTERISTIC POINTS AVL	A	B	C	D	UNIT
Deemphasis voltage	150	300	500	1500	mV_{RMS}
FM swing	15	30	50	150	kHz

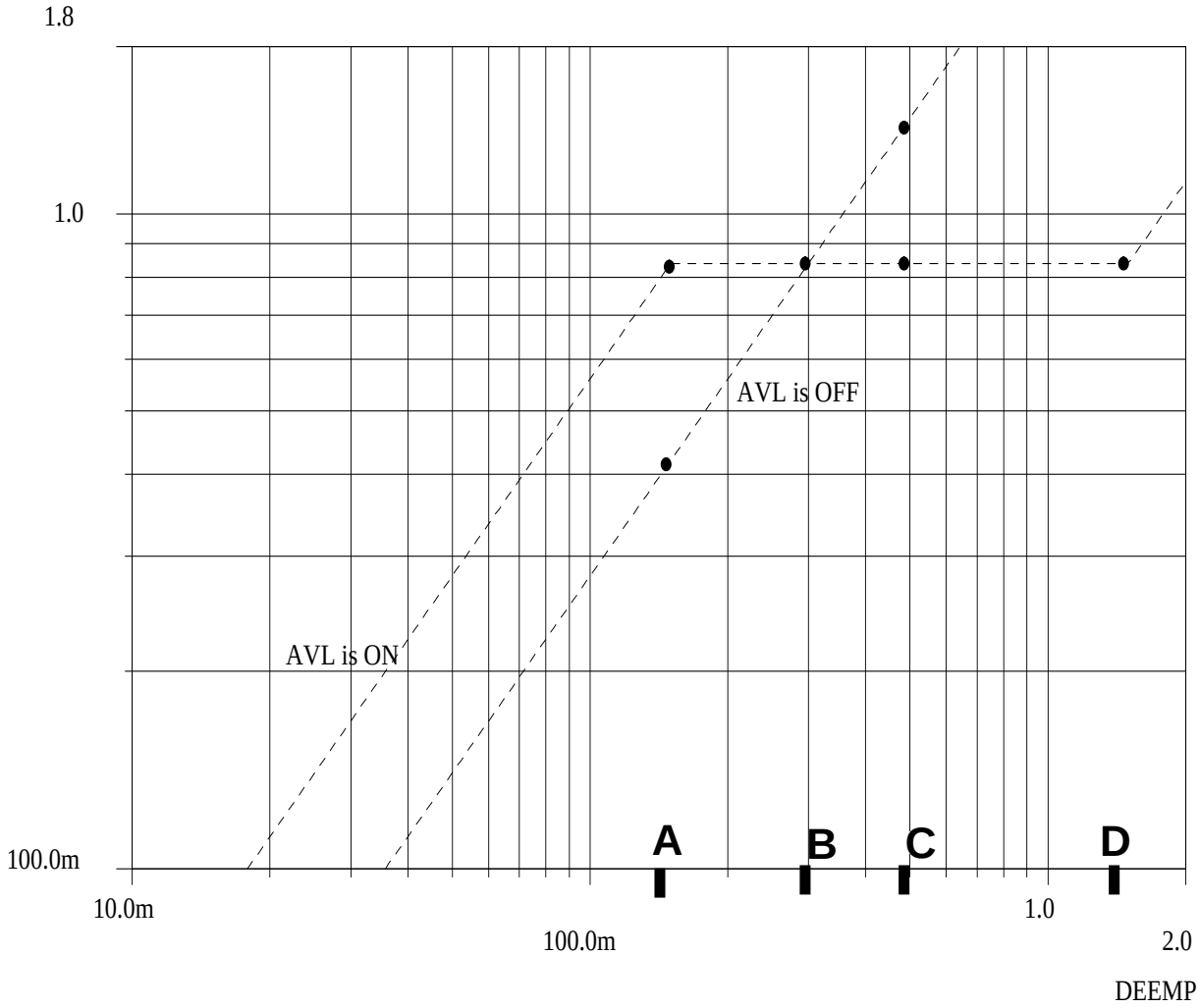
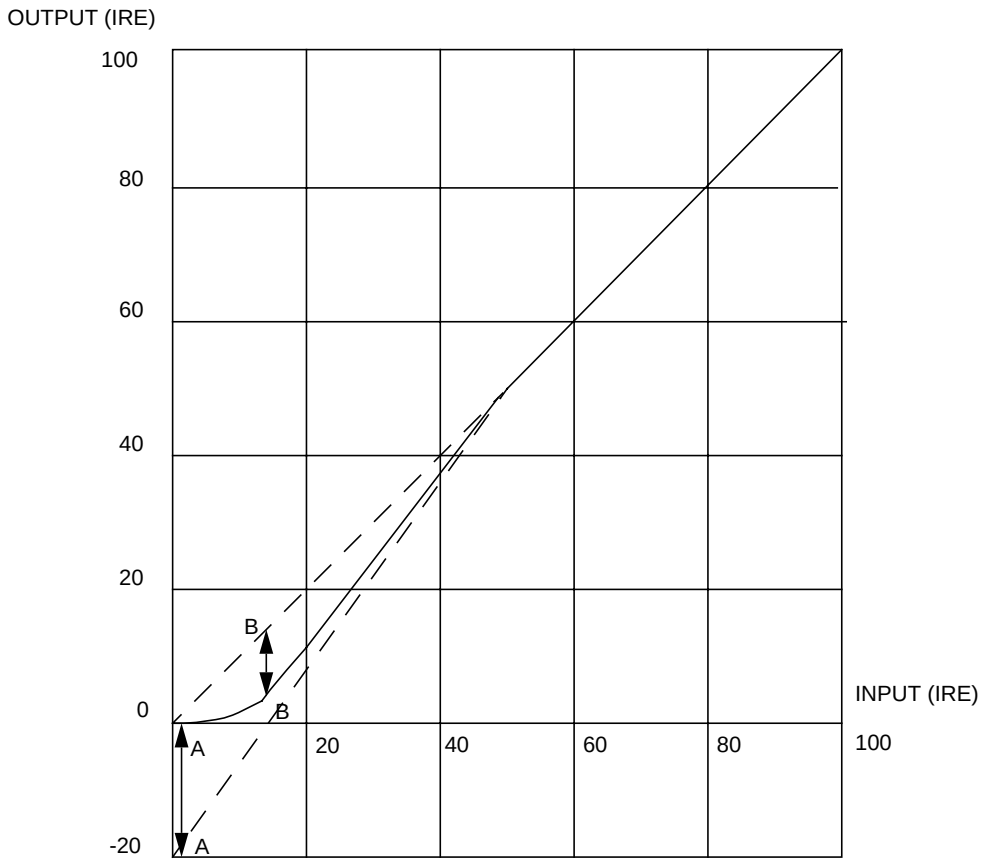


Fig.18 AVL characteristic for TDA 8840/41/42/46/46A for 4.4 MHz standard



A-A: MAXIMUM BLACK LEVEL SHIFT

B-B: LEVEL SHIFT AT 15% OF PEAK WHITE

Fig.19 I/O relation of the black level stretch circuit

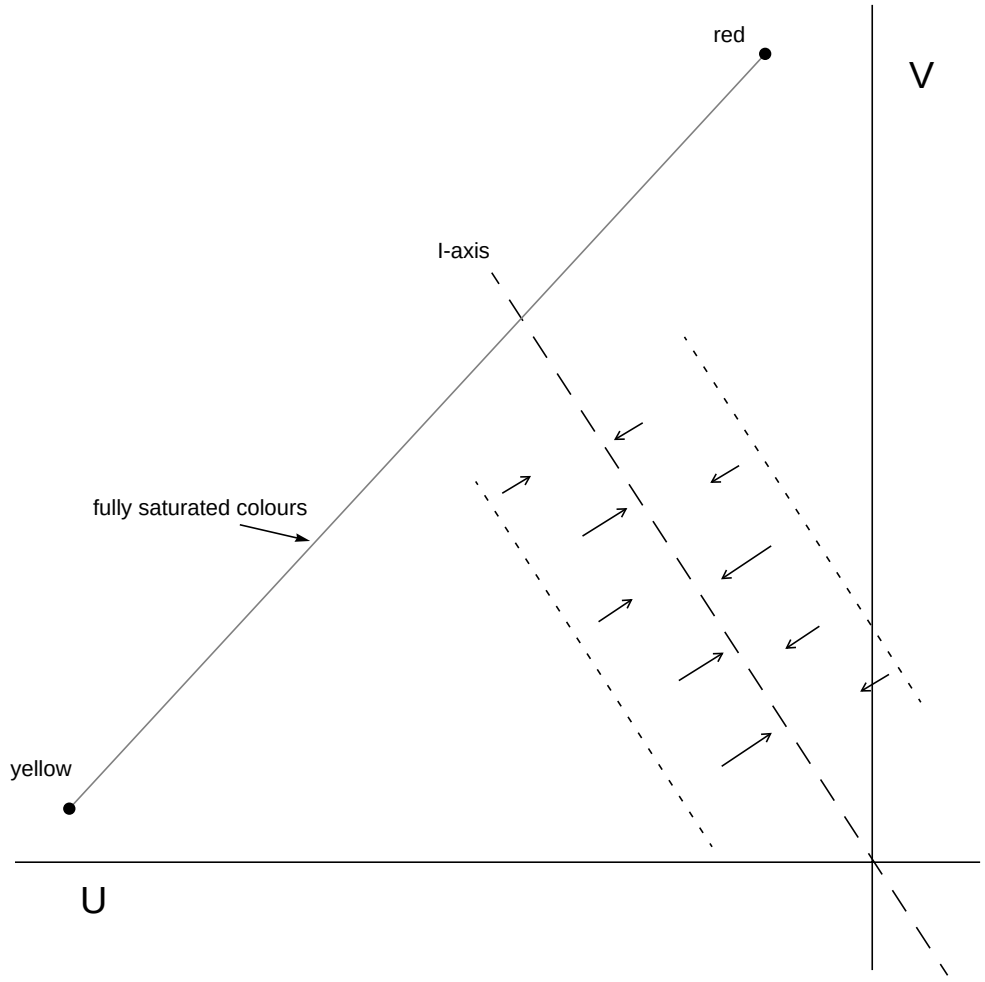


Fig.20 Skin tone correction range for a correction angle of 123 deg.

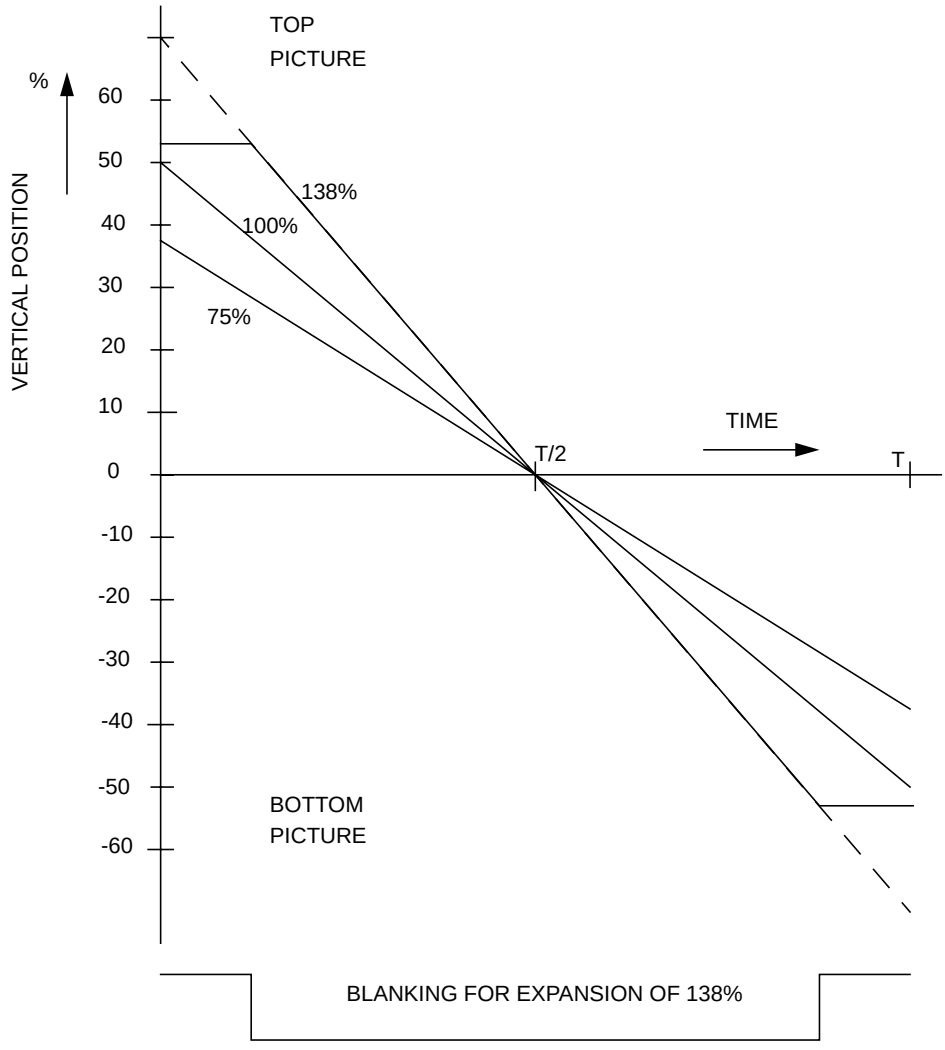


Fig.21 Sawtooth waveform and blanking pulse of the TDA 884X/5X

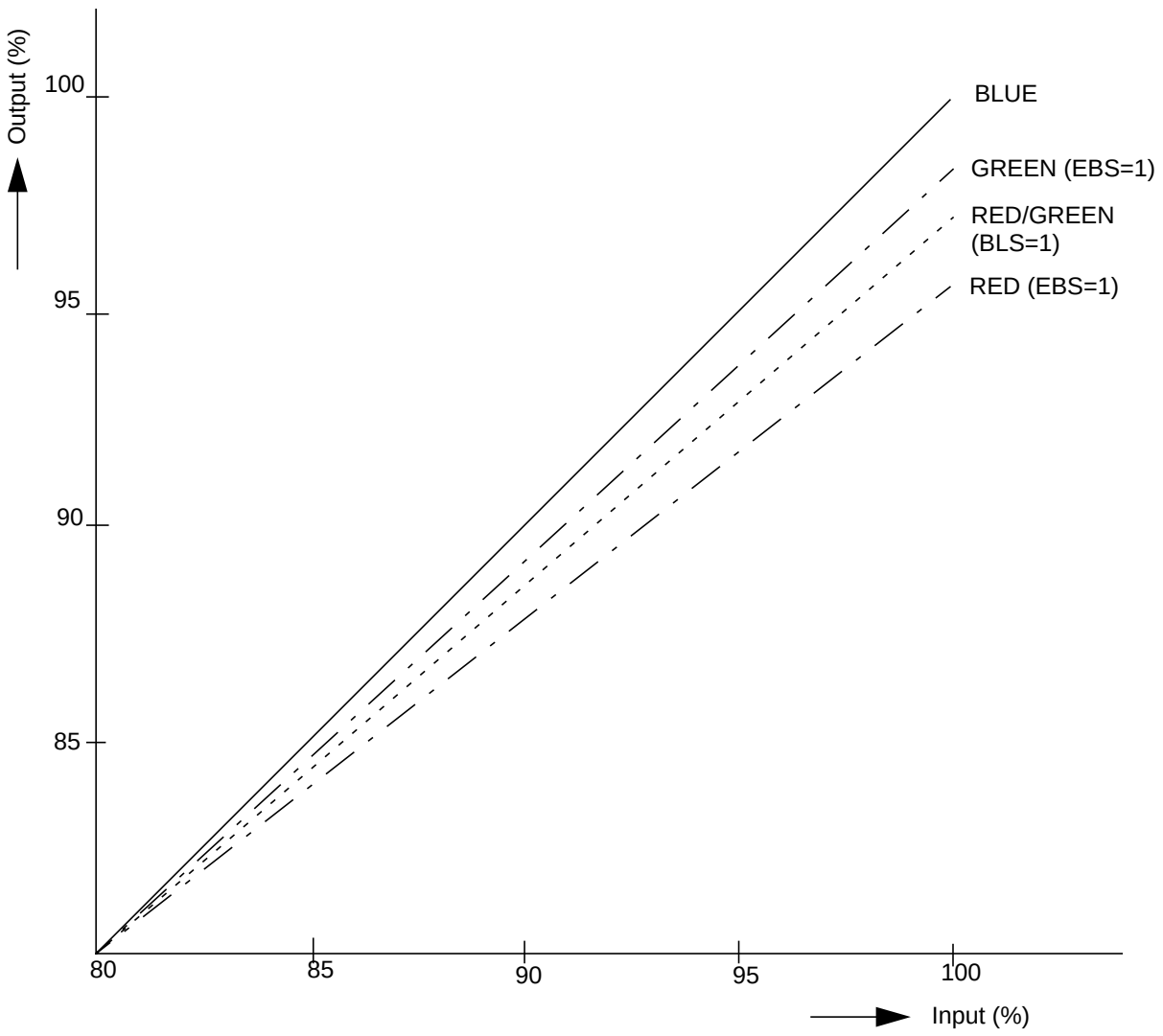


Fig.22 Blue stretch characteristics

TEST AND APPLICATION INFORMATION

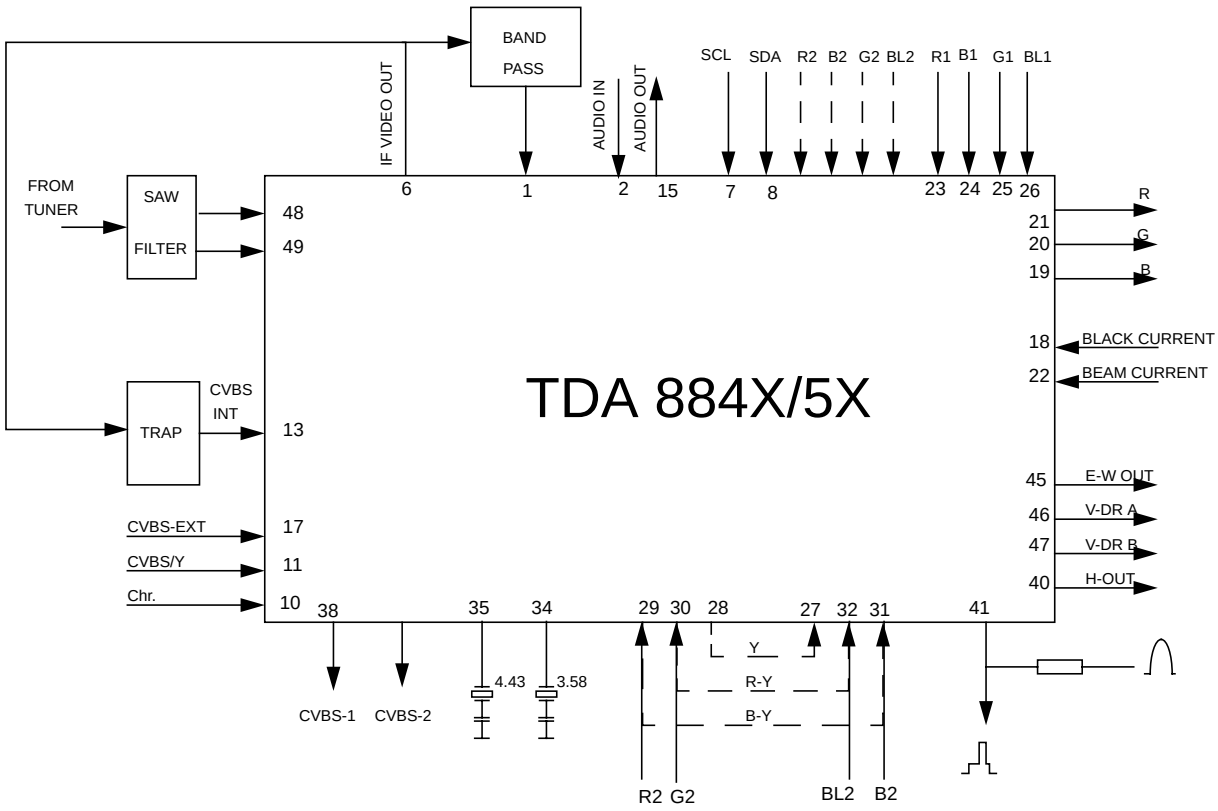


Fig.23 Application diagram.

East-West output stage

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the EW output stage should be dimensioned as illustrated in Fig.24.

Resistor R_{EW} determines the gain of the EW output stage. Resistor R_c determines the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of R_c is 39 kΩ which results in a reference current of 100 μA (V_{ref} = 3.9 V).

The value of R_{EW} must be:

$$R_{EW} = R_c \times \frac{V_{scan}}{18 \times V_{ref}}$$

Example: With V_{ref} = 3.9 V; R_c = 39 kΩ and V_{scan} = 120 V then R_{EW} = 68 kΩ.

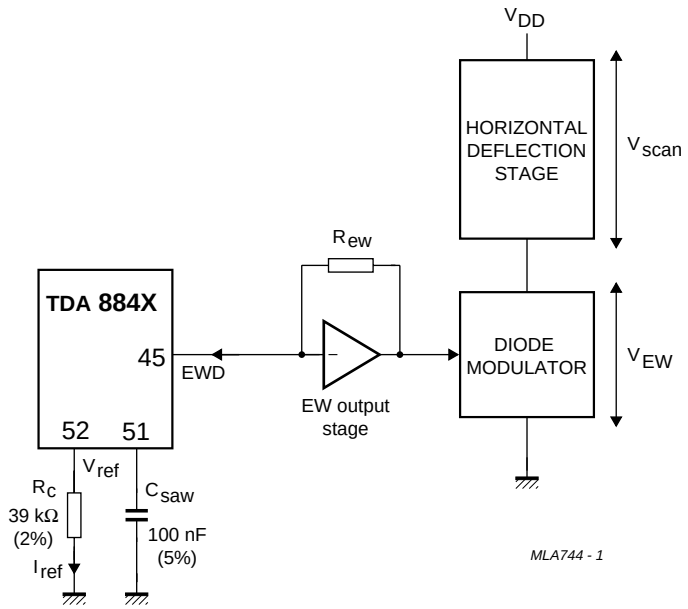
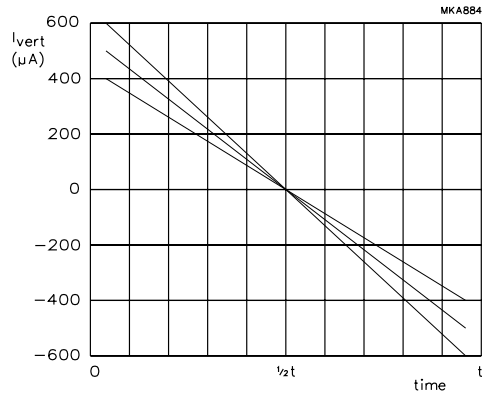
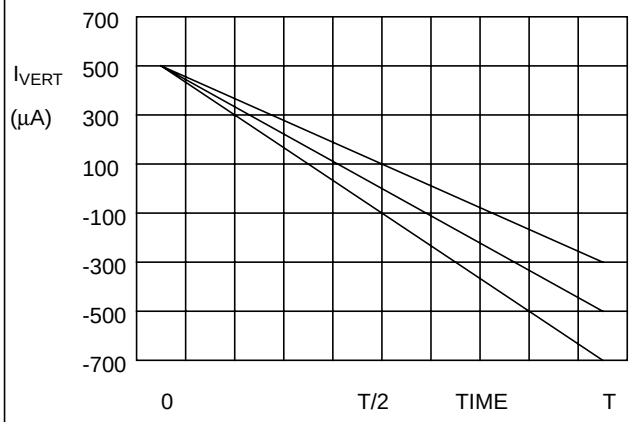


Fig.24 East-West output stage.



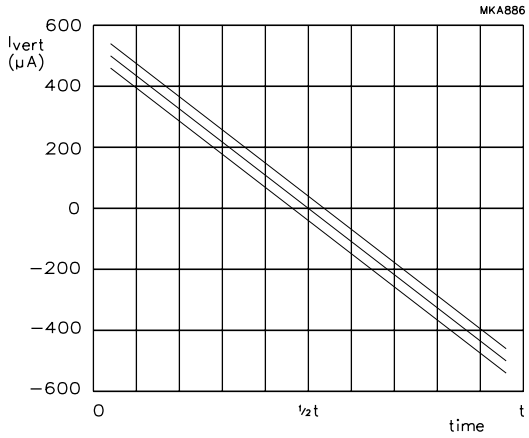
VA = 0, 31H and 63H; VSH = 31H; SC = 0.

Fig.25 Control range of vertical amplitude.



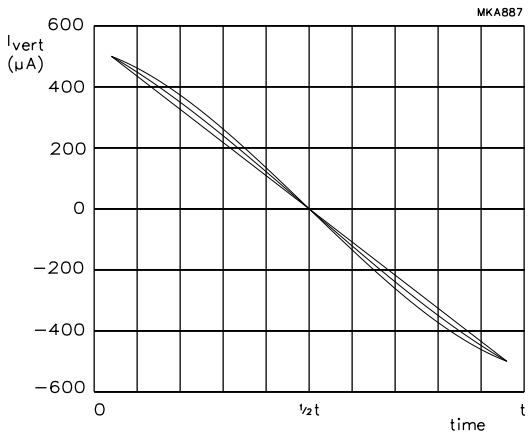
VS = 0, 31H and 63H; VA = 31H; VHS = 31H; SC = 0.

Fig.26 Control range of vertical slope.



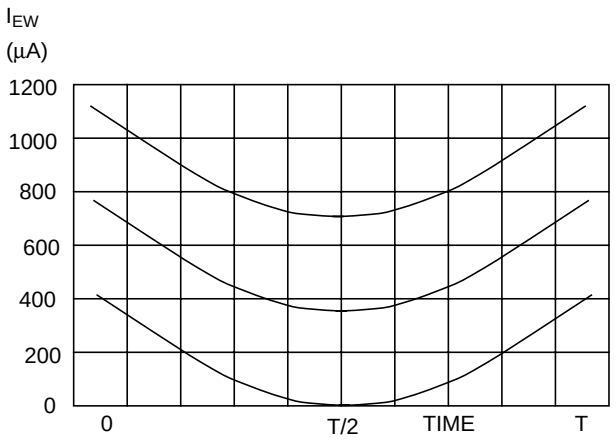
VSH = 0, 31H and 63H; VA = 31H; SC = 0.

Fig.27 Control range of vertical shift.



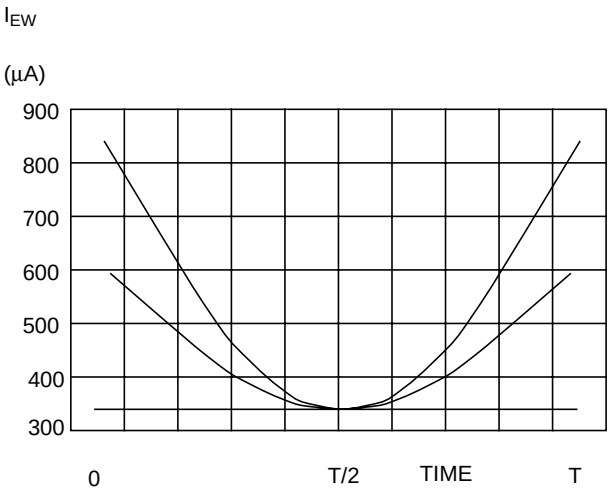
SC = 0, 31H and 63H; VA = 31H; VHS = 31H.

Fig.28 Control range of S-correction.



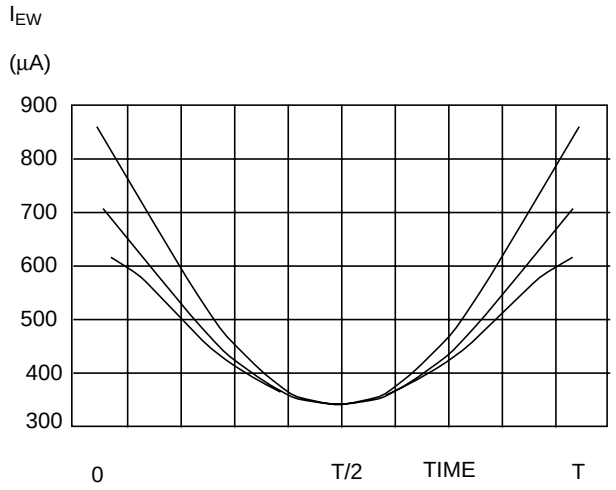
EW = 0, 31H and 63H; PW = 31H; CP = 31H.

Fig.29 Control range of EW width.



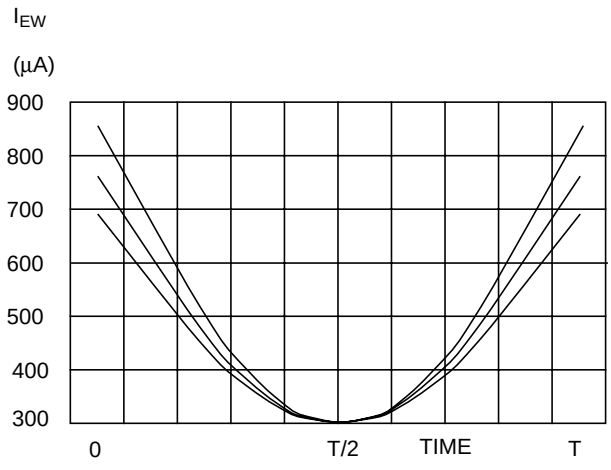
PW = 0, 31H and 63H; EW = 31H; CP = 31H.

Fig.30 Control range of EW parabola/width ratio.



CP = 0, 31H and 63H; EW = 31H; PW = 63H.

Fig.31 Control range of EW corner/parabola ratio.



TC = 0, 31H and 63H; EW = 31H; PW = 31H.

Fig.32 Control range of EW trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA8840/41/42/46/46A offers 5 control parameters for picture alignment, viz:

- S-correction
- vertical amplitude
- vertical slope
- vertical shift
- horizontal shift.

The TDA 8843/44/47/54H/57H offer in addition:

- EW width
- EW parabola width
- EW corner parabola
- EW trapezium correction.
- vertical zoom
- vertical scroll

It is important to notice that the IC's are designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type, vertical output stage and EW output stage it is determined which are the required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio. These parameters can be preset via the I²C-bus, and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range (i.e. 1FH), or with the values obtained by previous TV-set adjustments.

The vertical shift control is meant for compensation of off-sets in the external vertical output stage or in the picture tube. It can be shown that without compensation these off-sets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the value of the off-set, and to the square of the S-correction needed. The necessity to use the vertical shift alignment depends on the expected off-sets in vertical output stage and picture tube, on the required value of the S-correction, and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope independent of each other, a special service blanking mode can be entered by setting the SBL bit HIGH. In this mode the RGB-outputs are blanked during the second half of the picture. There are 2 different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

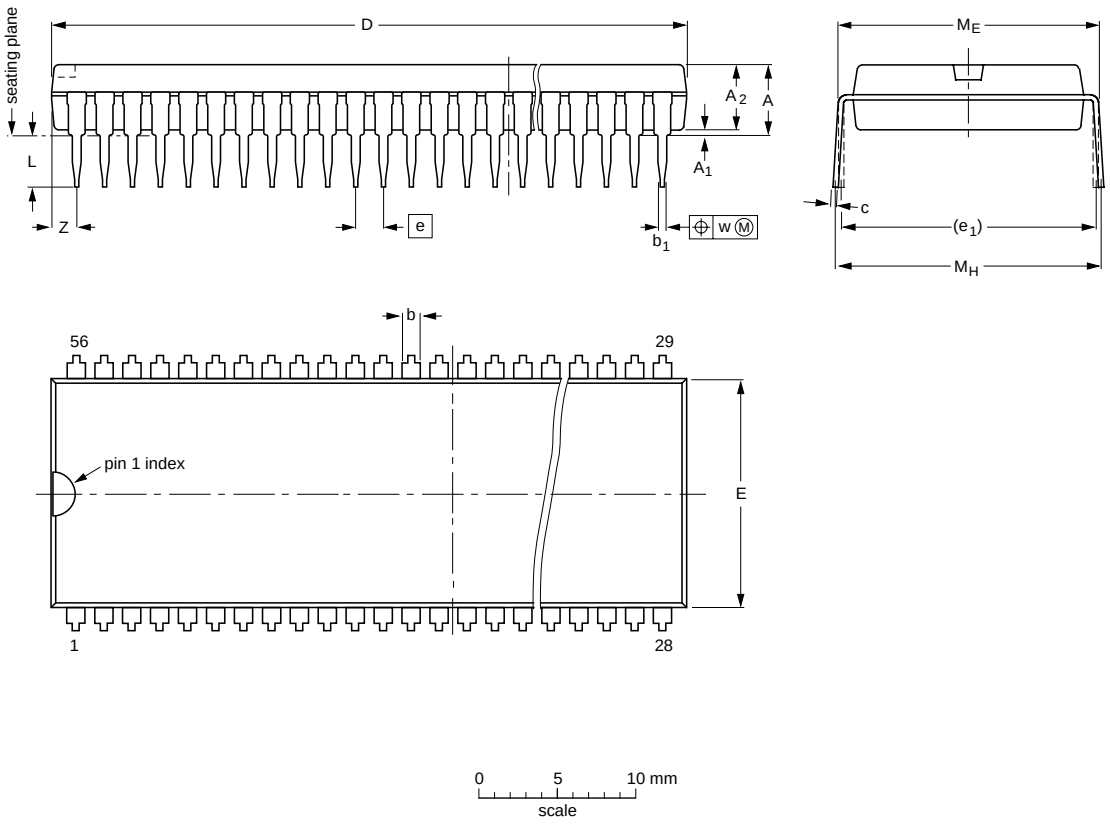
The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). With the vertical slope control the beginning of the blanking is positioned exactly on the middle of the picture. Then the top and bottom of the picture are placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the right setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1F). Then the top of the picture is placed by adjustment of the vertical amplitude and the bottom by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the EW width and the horizontal shift. Finally (if necessary) the left- and right-hand sides of the picture are aligned in parallel by adjusting the EW trapezium control.

To obtain the full range of the vertical zoom function with the TDA 8844/47/54H/57H the adjustment of the vertical geometry should be carried out at a nominal setting of the zoom DAC at position 19 HEX and the vertical scroll DAC at position 1F HEX.

PACKAGE OUTLINES

SDIP56: plastic shrink dual in-line package; 56 leads (600 mil) **SOT400-1**



DIMENSIONS (mm are the original dimensions)

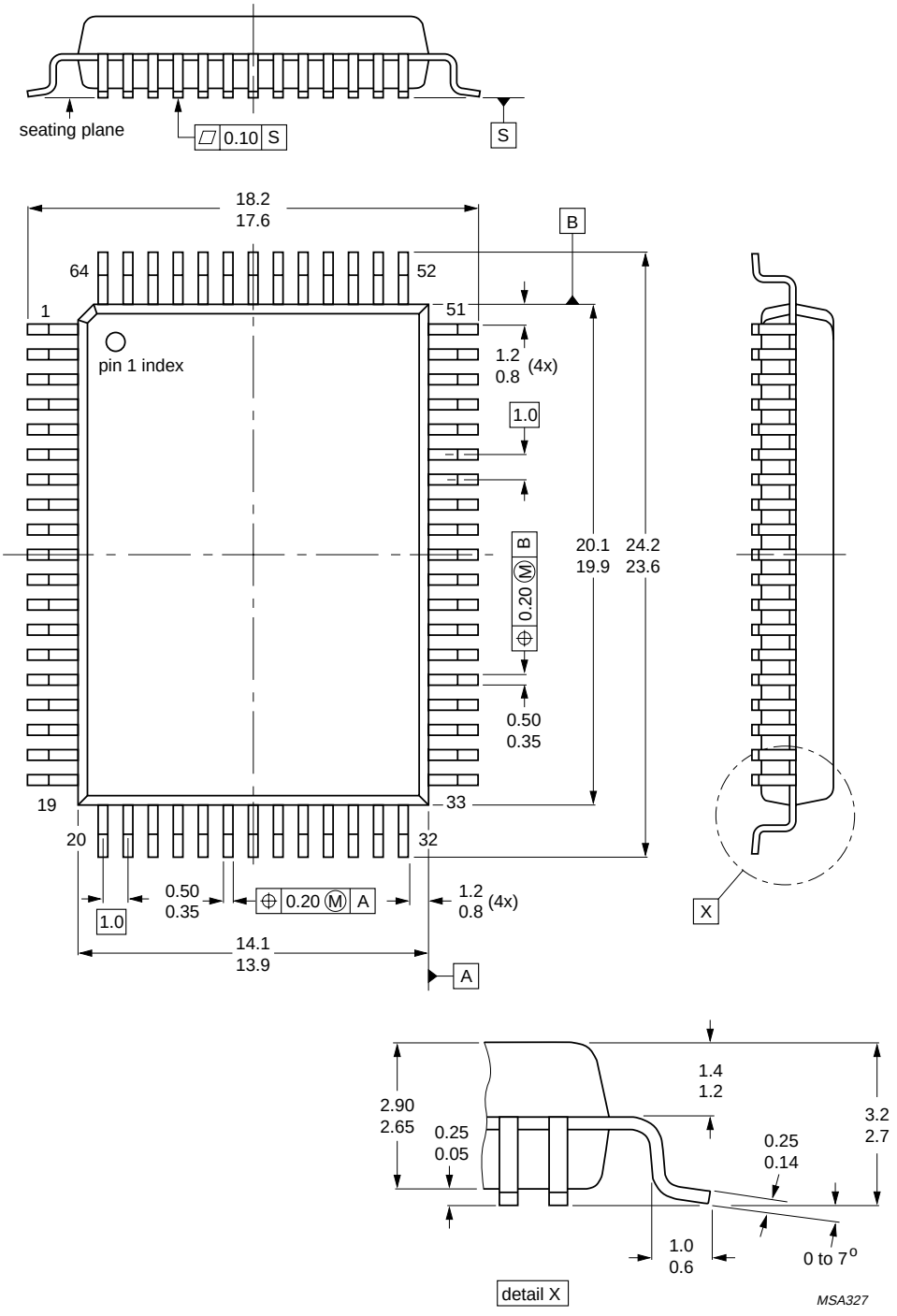
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	52.4 51.6	14.0 13.6	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	2.3

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT400-1						95-12-06

Fig.33 Plastic shrink dual in-line package; 56 leads (600 mil) SDIP56; SOT400AA1.



Dimensions in mm.

Fig.34 Plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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