Application Note AN-43
TOPSwitch®-HX Family

Design Guide

Introduction

The TOPSwitch-HX is a highly integrated monolithic off-line switcher IC designed for off-line power supplies. TOPSwitch-HX integrated circuits enable design of power supplies up to 195 W, while providing high efficiency under all load conditions. TOPSwitch-HX also provides very good performance at low load and during standby (no load) operation. The TOPSwitch-HX family allows the designer to meet the efficiency requirements for the new energy-efficiency standards. Innovative and proprietary features enable design of compact and cost effective switching power supplies while reducing overall design cycle time and system cost. The TOPSwitch-HX family also enables the design of power supplies with robust functionality and provides enhanced safety features such as output overvoltage protection, overload power limiting and hysteretic thermal protection.

Each member of the family has a high-voltage power MOSFET and its controller combined monolithically. Internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up circuitry. The internal oscillator is frequency modulated (jitter) to reduce EMI. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits power dissipation in the MOSFET, the transformer and the output diode during overload, output short-circuit or open-loop conditions. The auto-recovering hysteretic thermal shutdown function also disables MOSFET switching if temperature exceeds safe limits. A programmable UV/OV detection feature allows glitch free start-up and shutdown of the power supply during line sag or line surge conditions. Power Integrations' EcoSmart® technology enables supplies designed around the TOPSwitch-HX family to consume less than 200 mW at no load and maintain constant efficiency over the full line and load range. TOPSwitch-HX family of solutions easily meets energy efficiency standards such as the California Energy Commission (CEC), European Code of Conduct and ENERGY STAR.

Basic Circuit Configuration

The discussion of the function of application-specific requirements, such as constant current, constant power outputs, etc., is beyond the scope of this design guide. However, such requirements may be satisfied by adding additional circuitry to the basic converter descriptions shown here. For more information on additional circuit capabilities, design examples and other information, visit the Power Integrations web site or contact your PI sales representative.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the TOPSwitch-HX family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To help simplify the task, the application note refers directly to the PI Xls design spreadsheet that is part of the PI Expert™ design software suite available at no charge from

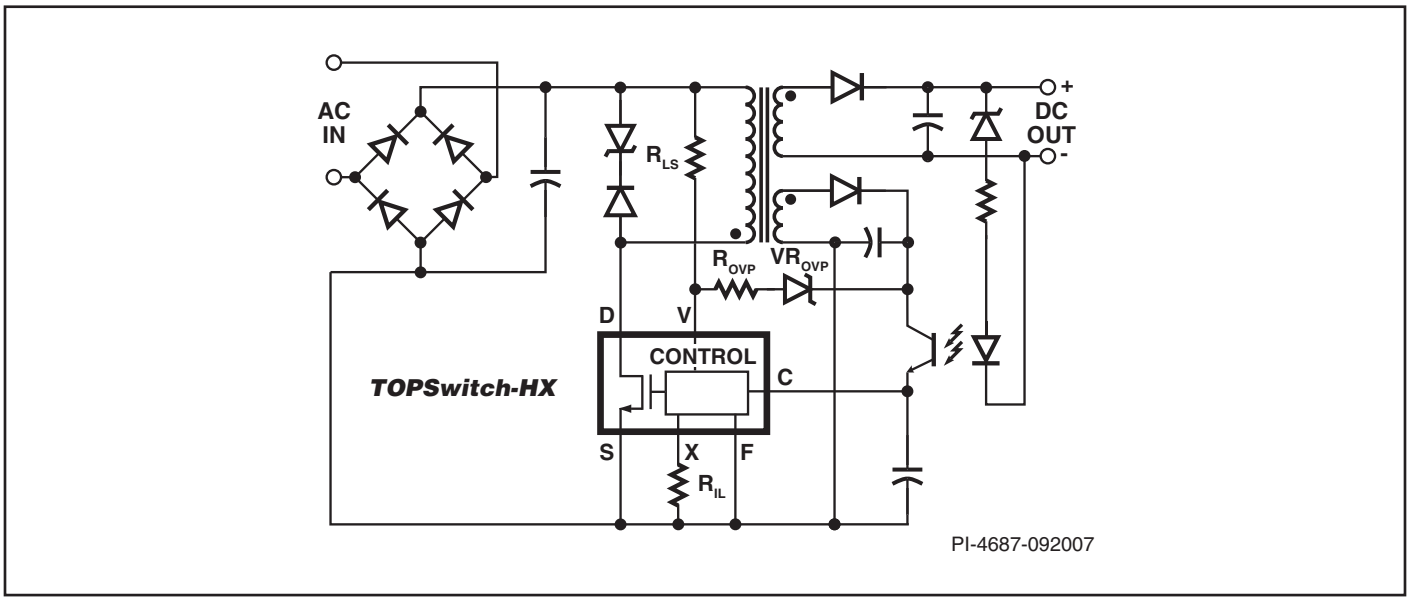

Figure 1. Typical TOPSwitch-HX Flyback Power Supply with Primary Sensed Overvoltage Protection.

www.powerint.com. The basic configuration used in TOPSwitch-HX flyback power supplies is shown in Figure 1, which also serves as the reference circuit for component identifications used in descriptions throughout this application note.

In addition to this application note, the reader may also find the TOPSwitch-HX Reference Design Kits (RDKs) useful. Each contains a fully functional engineering prototype board, engineering report and device samples. Further details on downloading PI Expert, and obtaining an RDK and updates to this document can be found at www.powerint.com.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach described later, and can use the following information to quickly design the transformer and select the components necessary for a first prototype. For this approach, only the information described below needs to be entered into the PI Xls spreadsheet, other parameters will be automatically selected based on typical design requirements. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX} and minimum line frequency f_L [B3, B4, B5]
- Enter Nominal Output Voltage V_O [B6]
- For designs with a peak load condition, enter average output power, else enter continuous output power [B7]
- For designs with a peak load current, enter peak load current else leave blank [B8]
- Enter efficiency estimate [B9]
  0.8 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC) and 0.85 for a single 230 VAC (185-265 VAC) design. Adjust the number accordingly based on measurement at peak load and VACMIN.
- Enter loss allocation factor Z [B10]
  0.5 for typical application (adjust the number accordingly after first prototype-board evaluation)
- Enter C_{IN} input capacitance [B13]
  3 µF/W for universal (85-265 VAC) or single (100/115 VAC)
  Use 1 µF/W single 230 VAC for single (185-265 VAC).
- Select the TOPSwitch-HX part from the drop down list or enter directly [B17]
- Select the device in the table below according to output power and line input voltage
- Enter Operating Frequency – [B22]
  "H" for 66 kHz operation
  "F" for 132 kHz operation
  If P, G and M packages are chosen, selecting "H" or "F" in cell B22 does not change the design as these parts only operate at 66 kHz (nominal) frequency.
- Enter core type (if desired) from drop down menu [B52]
  A suggested core size will be selected automatically if none is entered
  If any warnings are generated, make changes to the design by following instructions in spreadsheet column F
- Build transformer
- Select key components
  See Steps 7 through 12.
- Build prototype and iterate design as necessary, replacing estimates in the spreadsheets with measured values as appropriate (e.g. efficiency, V_{MIN}).

Output Power Table

Product[5]	230 VAC ±15%[4]			85-265 VAC		
	Adapter[1]	Open Frame[2]	Peak[3]	Adapter[1]	Open Frame[2]	Peak[3]
TOP252PN/GN	9 W	15 W	21 W	6 W	10 W	13 W
TOP252MN			21 W			13 W
TOP253PN/GN	15 W	25 W	38 W	9 W	15 W	25 W
TOP253MN			43 W			29 W
TOP254PN/GN	16 W	28 W	47 W	11 W	20 W	30 W
TOP254MN			62 W			40 W
TOP255PN/GN	19 W	30 W	54 W	13 W	22 W	35 W
TOP255MN			81 W			52 W
TOP256PN/GN	21 W	34 W	63 W	15 W	26 W	40 W
TOP256MN			98 W			64 W
TOP257PN/GN	25 W	41 W	70 W	19 W	30 W	45 W
TOP257MN			119 W			78 W
TOP258PN/GN	29 W	48 W	77 W	22 W	35 W	50 W
TOP258MN			140 W			92 W

Product[5]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
TOP252EN	10 W	21 W	6 W	13 W
TOP253EN	21 W	43 W	13 W	29 W
TOP254EN/YN	30 W	62 W	20 W	43 W
TOP255EN/YN	40 W	81 W	26 W	57 W
TOP256EN/YN	60 W	119 W	40 W	86 W
TOP257EN/YN	85 W	157 W	55 W	119 W
TOP258EN/YN	105 W	195 W	70 W	148 W
TOP259EN/YN	128 W	238 W	80 W	171 W
TOP260EN/YN	147 W	275 W	93 W	200 W
TOP261EN/YN	177 W	333 W	118 W	254 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient. Use of an external heat sink will increase power capability.
2. Minimum continuous power in an open frame design at +50 °C ambient.
3. Peak power capability in any design at +50 °C ambient.
4. 230 VAC or 110/115 VAC with doubler.
5. Packages: P: DIP-8C, G: SMD-8C, M: SDIP-10C, Y: TO-220-7C, E: eSIP-7C. See part ordering information.

- Power Integrations offers a transformer prototyping service and links to other vendors: for details see www.powerint.com/componentsuppliers.htm

Step-by-Step Transformer Design Procedure

Introduction

The design flow allows for design of power supplies both with or without a peak output power requirement. This is of particular relevance when using the P, G or M packages. Here the current limit enables design of power supplies capable of delivering peak power for a short duration limited only by thermal characteristics of the TOPSwitch-HX package and ratings of other components in the circuit.

As average power increases, based on the measured transformer and device temperature, it may be necessary to select a larger transformer to allow increased copper area for the windings and/or to increase the amount of device heat sinking

The power table (Table 1) provides guidance for peak and continuous (average) power levels obtainable in both sealed adapter and open frame applications. For the P, G and M packages, the power values for Adapter and Open Frame are thermally limited. The peak values represent the electrically limited output power, assuming operation at current limit ($I_{LIM(MIN)}$). For the Y package, the Adapter power values are also thermally limited, however, the Open Frame values are electrically limited and therefore also represent the peak output power. As the continuous power values are thermally limited, they indicate the upper limit of continuous power for worst case conditions but may vary depending on the specific application. For example, if the peak power condition has a very low duty cycle, such as the 1-second peak required to close the drawer in a DVD player, then the thermal rise of the device (and transformer) is only a function of the continuous average power. However, if the peak power is repetitive with a significant duty cycle, then it would need to be considered as a limiting factor in the design.

Figure 2 shows how to calculate the average power requirements for a design with two different peak load conditions.

$$P_{AVE} = P_1 + (P_3 - P_1) \times \delta_1 + (P_2 - P_1) \times \delta_2$$

$$\delta_1 = \frac{\Delta t_1}{T}, \delta_2 = \frac{\Delta t_2}{T}$$

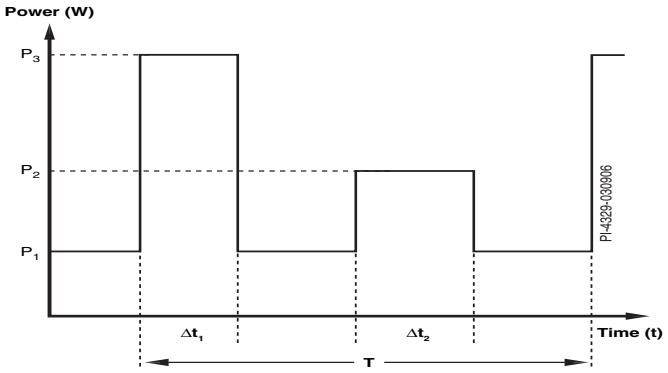

Figure 2. Continuous (average) output power calculation example.

Where P_X are the different output power conditions, Δt_X are the durations of each peak power condition and T is the period of one cycle of the pulsed load condition

The design procedure requires both peak and continuous (average) powers to be specified. If there is no peak power requirement for the design, the same value should be used for continuous as well as peak power.

The peak power is used to select the TOPSwitch-HX device and design the transformer for power delivery at minimum input line voltage while continuous (or average power if the peak load is periodic) is used for thermal design and may affect the size of the transformer and the heat sink.

Step 1. Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, $P_{O(AVE)}$, $P_{O(PEAK)}$, η, Z, V_B, t_C, C_{IN}

Determine the input voltage range from Table 2.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100 / 115	85	132
230	195	265
Universal	85	265

Table 2. Standard Worldwide Input Line Voltage Ranges.

Line Frequency, f_L

50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimums. For most applications this gives adequate overall design margin. For

ACDC_TOPSwitchHX_091007; Rev.1.3; Copyright Power Integrations 2007	INPUT	INFO	OUTPUT	UNIT	TOP_HX_091007: TOPSwitch-HX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					Customer
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage (main)
PO_AVG	35.00			Watts	Average Output Power
PO_PEAK	50.00		50.00	Watts	Peak Output Power
n	0.81			%/100	Efficiency Estimate
Z	0.48				Loss Allocation Factor
VB	15			Volts	Bias Voltage
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	120.0		120	uFarads	Input Filter Capacitor

Figure 3. Application Variable Section of TOPSwitch-HX *Design Spreadsheet.*

DC INPUT VOLTAGE PARAMETERS					
VMIN			85	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

Figure 4. DC Input Voltage Parameters Showing Grey Override Cells for DC Input Designs.

absolute worst case or based on the product specification, reduce these numbers by 6% (47 Hz or 56 Hz). For half-wave rectification, use FL/2. For DC input, enter the voltage directly into Cells B65 and B66.

Nominal Output Voltage, V_O (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally the main output is the output from which feedback is derived.

Continuous / Average Output Power $P_{O(AVE)}$ (W)
Enter the average output power of the power supply. If the power supply is a multiple output power supply, enter the sum total power of all the outputs.

Peak Output Power $P_{O(PEAK)}$ (W)
Enter the peak output power under peak load conditions. If the design does not have a peak load condition, then leave this entry blank and a value equal to $P_{O(AVE)}$ is assumed. $P_{O(PEAK)}$ is used to calculate the primary inductance value.

In multiple output designs, the output power of the main output (typically the output from which feedback is taken) should be increased such that the peak power (or maximum continuous output power as applicable) matches the sum of the output power from all the outputs in the design. The individual output voltages and currents should then be entered at the bottom of the spreadsheet (cells [B120 to B166]).

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply measured at the output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 80% for VAC_{MIN} of 85 VAC and 85% for 195 VAC. These are typical for a design where the majority of the output power is drawn from an output voltage of 12 V and no current sensing is present on the secondary. Once a prototype has been constructed, then measured efficiency can be entered and a further transformer iteration performed, as appropriate.

Power Supply Loss Allocation Factor, Z
This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc) are not processed by the power stage (transferred through the transformer) and therefore, although they reduce efficiency, the transformer design is not effected by their effect on efficiency.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

For designs that do not have a peak power requirement, a value of 0.48 is recommended. For designs with a peak power requirement, enter 0.65.

Bias Winding Output Voltage (V_B)
Enter the voltage at the output of the bias winding output. A value of 15 V is recommended. The voltage may be set to different values, for example, when the bias winding output is also used as a primary side (non-isolated) auxiliary output. Higher voltages increase no-load input power. Values below 10 V are not recommended as at light load there may be insufficient voltage to correctly bias the optocoupler, causing loss of output regulation. A 10 µF, 50 V electrolytic capacitor is recommended for the bias winding output filter.

Bridge Diode Conduction Time, t_C (ms)
Enter a bridge diode conduction time of 3.00 ms if there is no better data available.

Total Input Capacitance, C_{IN} (µF)
Table 3 suggests suitable multiplication factors to be used for calculating input capacitance for different AC input formats.

	Total Input Capacitance per Watt Output Power (µF/W)
AC Input Voltage (VAC)	Full Wave Rectification
100/115	3
230	1
85-265	3

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} >70 V.

Step 2 – Enter TOPSwitch-HX Variables: TOPSwitch-HX Device, Current Limit, V_{OR}, V_{DS}, V_D,

Select the correct TOPSwitch-HX device
First, refer to the TOPSwitch-HX power table and select a device based on the peak output power design. Then compare the continuous power to adapter column numbers in the power table, if the power supply is of fully enclosed type, or compare to the open-frame column if the power supply is an open-frame design. If the continuous power exceeds the value given in the power table (Table 1), then the next largest device should be selected. Similarly, if the continuous power is close to the adapter power levels given in the power table, then it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

Peak power values are only given for P, G and M packages. For Y packages, high peak and continuous ratings are the same. This is due to the power dissipation capability of the Y package. For the P, G and M, the maximum device dissipation is limited by both the junction to case and case to ambient

thermal impedance. However, for Y package the junction to case impedance is low, and the device can be connected to a heat sink sized to maintain an acceptable device temperature.

External Current Limit Reduction Factor KI
The factor KI sets the value of the current limit threshold. This allows the current limit level to be adjusted slightly above the minimum peak current (I_P) required for power delivery. This optimizes the transformer design by limiting the peak flux density during overload and start-up.

For higher efficiency and improved thermal performance, KI, also allows the selection of a larger TOPSwitch-HX device to be used than required for power delivery by reducing KI, such that the current limit of the larger device is equal to the original smaller part selected.

High Line Operating Mode
This parameter confirms the mode of operation of the TOPSwitch-HX at high line. It is desirable to operate in full-frequency mode at high line as the switching frequency jitter feature will be enabled. (See TOPSwitch-HX datasheet for an explanation of operating modes). This provides improved EMI performance.

Reflected Output Voltage, V_{OR} (V)
This parameter is the secondary winding voltage during diode conduction, reflected back to the primary through the turns ratio of the transformer. The default value is 135 V; however the acceptable range for V_{OR} is between 80 V and 135 V, providing no warnings in the spreadsheet are triggered. For design optimization purposes, the following should be kept in mind:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given TOPSwitch-HX device.
2. Higher V_{OR} reduces the voltage stress on the output diodes, which in some cases may allow the use of a lower forward drop Schottky diode for higher efficiency.
3. Higher V_{OR} increases leakage inductance that reduces efficiency of the power supply.
4. Higher V_{OR} increases peak and RMS current on the secondary side, which may increase secondary side copper and diode losses.

Optimal selection of the V_{OR} value depends on the specific application and is based on a compromise between the factors mentioned above.

Values below 80 V are not usually recommended. Low V_{OR} may cause excessive triggering of the MOSFET self-protection feature during startup, especially in designs where all outputs are >5 V.

TOPSwitch-HX ON State Drain to Source Voltage, V_{DS} (V)
This parameter is the average ON state voltage developed across the DRAIN and SOURCE pins of TOPSwitch-HX. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

Output Diode Forward Voltage Drop, V_D (V)
Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN diode if no better data is available. By default, a value of 0.5 V is assumed.

Performance Goal	VOR Value Suggestion	Comment
Maximum output power / smallest TOPSwitch-HX Device	135 V	Maximizes power from given device
Highest Efficiency	100 V - 120 V	Gives lowest overall losses between, conduction, output diode and leakage inductance
Multiple Output Design	90 V - 110 V	Improves cross regulation by reducing transformer leakage inductance and peak secondary currents

Table 4. Suggested Values for VOR.

Bias Winding Diode Forward Voltage Drop, V_{DB} (V)
Enter the average forward voltage drop of the bias winding output diode. Use 0.7 V for an ultra-fast recovery diode.

Ripple to Peak Current Ratio, K_P
Figure 6 shows K_p < 1, indicating continuous conduction mode, K_P is the ratio of ripple to peak primary current.

ENTER TOPSWITCH-HX VARIABLES					
TOPSwitch-HX	TOP258PN/GN			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP258PN/GN*	Power Out	35 W / 50 W	48W
KI	1.00				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			1.534	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			1.766	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	H		H		Only half frequency option available for P, G and M package devices. For full frequency operation choose Y package.
fS			66000	Hertz	TOPSwitch-HX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			59400	Hertz	TOPSwitch-HX Minimum Switching Frequency
fSmax			72600	Hertz	TOPSwitch-HX Maximum Switching Frequency
High Line Operating Mode			FF		
VOR	135.00			Volts	Reflected Output Voltage
VDS	5.63		5.63	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.40				Ripple to Peak Current Ratio (0.3 < KRP < 1.0 : 1.0< KDP<6.0)

Figure 5. TOPSwitch-HX *Section of Design Spreadsheet.*

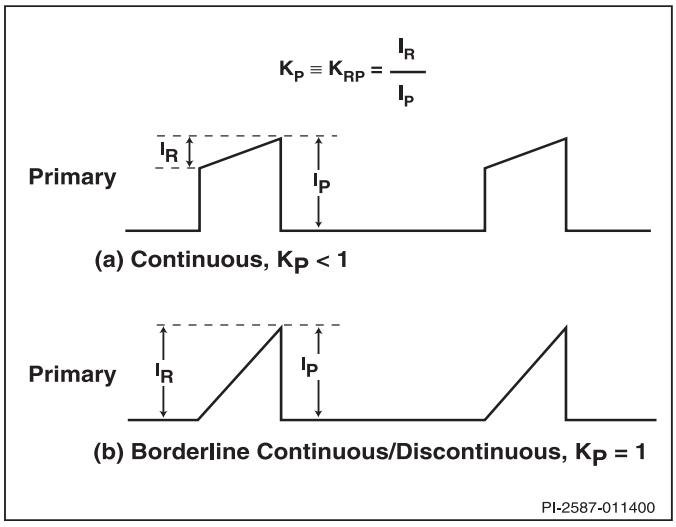

Figure 6. Continuous Mode Current Waveform, Kp≤1.

$$K_P \equiv K_R = \frac{I_R}{I_P}$$

Figure 7 shows $K_p > 1$, indicating discontinuous conduction mode, K_P is the ratio of primary MOSFET off time to the secondary diode conduction time.

The value of K_P should be in the range of $0.3 < K_P < 6$, and guidance is given in the comments cell if the value is outside this range.

A K_P value of < 1 will result in higher efficiency by lowering the primary RMS current. Typically the highest efficiency for a given core size will be obtained with a K_P range of 0.65 to 0.55, but values outside this range are acceptable.

The spreadsheet will calculate the values of peak primary current, the RMS ripple current, average primary current and the maximum duty cycle for the design.

$$K_P \equiv K_{DP} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

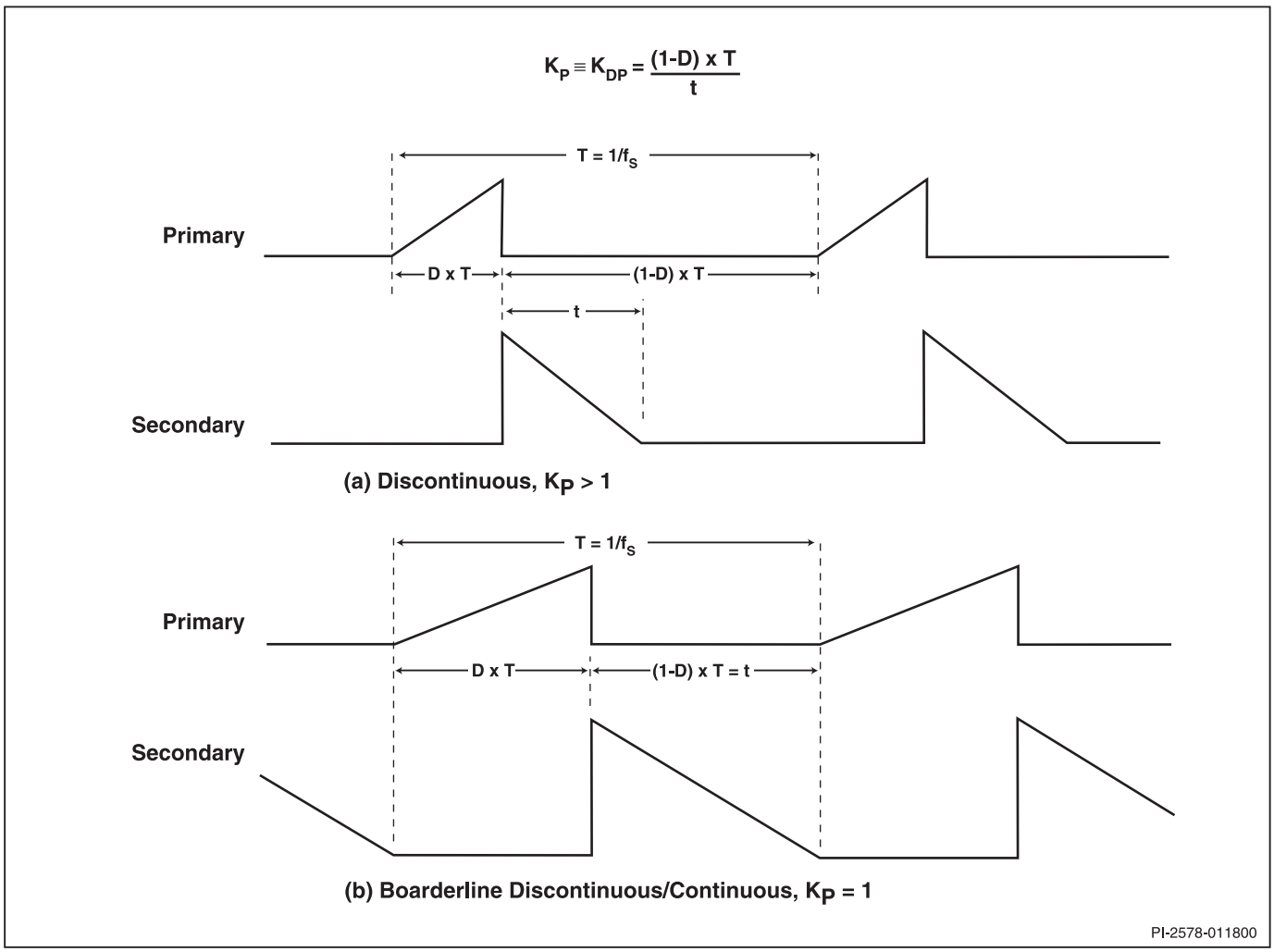

Figure 7. Discontinuous Mode Current Waveform, Kp≥1.

PROTECTION FEATURES					
LINE SENSING					Note - For P/G package devices only one of either Line sensing or Overload power limiting protection featues can be used. For all other packages both these functions can be simultaneously used.
VUV_STARTUP			95	Volts	DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			445	Volts	DC Bus Voltage at which power supply will shut-down
RLS			4.0	M-ohms	Use two standard, 2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			27	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.02		Margin to current limit at low line.
ILIMIT_EXT_VMIN			1.50	A	External Current limit at VMIN
ILIMIT_EXT_VMAX			1.29	A	External Current limit at VMAX
RIL			6.65	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only

CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.63		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.51	Amps	Average Primary Current (calculated at average output power)
IP			1.44	Amps	Peak Primary Current (calculated at Peak output power)
IR			1.27	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.65	Amps	Primary RMS Current (calculated at average output power)

Figure 8. Circuit Protection Component Section of Design Spreadsheet.

Step 3 – Choose Protection Features, Line Under / Overvoltage, Output Overvoltage and Overload Power Limiting - Optional

The optional line undervoltage lockout feature of TOPSwitch-HX, defines the startup voltage of the supply and prevents the power supply output from gliching when the input voltage is below the normal operating range. Connecting a resistor from the input capacitor to the V pin enables this feature. Enter the desired DC voltage across the input capacitor, at which the power supply should operate in the cell adjacent to VUV_STARTUP. The spreadsheet calculates the ideal resistor value R_{LS}.

The value of R_{LS} also defines the line OV threshold. The calculated voltage ($V_{OV(SHUTDOWN)}$) at which the power supply will stop operating due to an input overvoltage condition is displayed.

Output Overvoltage Shutdown - Optional

The output voltage of the bias winding can be used for primary sensed output overvoltage. This is an inexpensive way of protecting the power supply should a component in the feedback circuit fail.

This feature can be enabled by connecting a series combination of a resistor and Zener diode from the bias winding output to the V pin (as shown in Figure 1). The spreadsheet estimates a value of the Zener diode required to initiate shutdown in case of loss of feedback but without false triggering during transient conditions such as during dynamic load changes.

During a fault, the bias winding voltage rises causing the Zener diode to conduct and current to flow into the V (or M) pin. If this current exceeds 112 µA (I_{OV}) for longer than 100 µs, then switching is disabled and the supply enters auto-restart. This prevents further increase in output voltage but does not latch off the power supply. Switching is enabled again when the current reduces by greater than the 4 µA V pin hysteresis requirement. If the current through the Zener and into the V (or M pin) exceeds 336 µA, the latching shutdown feature of TOPSwitch-HX is triggered, and the power supply latches off. To reset the latched condition, either the input AC supply has to be removed for long enough for the control pin capacitor to discharge below $V_{C(RESET)}$ (~3 V) or the V (or M pin) can be externally pulled below 1 V.

In a typical circuit, a high series resistance R_{OVP} in the order of 5.1 kΩ will result in a non-latching shutdown. A low resistance in the range of 4.7 Ω to 22 Ω will result in a latching shutdown.

It is recommended that the resistor should be connected to the V pin and the Zener diode cathode should be connected to the bias winding output.

Output Power Limiting vs Input Voltage (Optional)

The X-pin on the TOPSwitch-HX can be used to program a current limit value lower than the maximum internal current limit for the part selected. A resistor connected from the X-pin to the source pin (R_{IL} in Figure 1) allows selection of a fixed externally programmed current limit. See datasheet for current limit resistor selection curves.

The addition of a second resistor connected from the X-pin to the DC-Bus (R_{PL}), as shown in Figure 12, allows reduction of the programmed current limit as a function of the line voltage. This is desirable as typical Flyback power supplies that operate in continuous conduction mode at low line (K_P < 1) will have a higher overload power capability at high line by 200-300%. In certain applications this may require over design of the output diode, transformer and output capacitors to handle the increased dissipation.

The PIXIs spreadsheet calculates the values of the two resistors required for power limiting vs line based on the choice of the TOPSwitch-HX part and the value of Kp selected. At V_{MIN} the target current limit value is equal to $I_{LIMIT(MIN\_EXT)}$. At high line the

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EF25		EF25		Core Type
Core		*EF25*		*P/N:*	PC40EF25-Z
Bobbin		*EF25_BOBBIN*		*P/N:*	*
AE			0.518	cm^2	Core Effective Cross Sectional Area
LE			5.78	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			15.6	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00				Number of Primary Layers
NS			5		Number of Secondary Turns

Figure 9. Transformer Core and Construction Variables Section of Spreadsheet.

target current limit value is calculated based on the value required for specified $P_{O(PEAK)}$ multiplied by the margin factor, Overload Current Limit Ratio at V_{MAX}. The recommended value of 120% ensures that the MOSFET protection mode is not triggered during startup, especially with high output voltage designs. Lower values are acceptable, but startup into maximum (peak) load at high input line voltage must be verified.

Resistor values are calculated using the worst case current limit reduction curves provided in the TOPSwitch-HX datasheet.

Step 4 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, BW, M, L, N_S

Core effective cross-sectional area, A_E: (cm^2)
Core effective path length, L_E: (cm).
Core ungapped effective inductance, A_L: ($nH/turn^2$).
Bobbin width, BW: (mm)
Tape margin width equal to half the total margin, M (mm)
Primary Layers, L
Secondary Turns, N_S

Core Type

If the core type cell is left empty, the spreadsheet will default to the smallest commonly available core suitable for the continuous (average) output power specified. The entire list of cores available can be selected from the drop down list in the tool bar of the PIXIs design software.

The grey override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list, or the specific core or bobbin information differs from that referenced by the spreadsheet.

Table 5 provides a list of commonly available cores and power levels at which these cores can be used for typical designs.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary but do not use triple-insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. For universal input designs, a total windings margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin were only on one side of the bobbin.

For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety Table creepage distances. Typically, many bobbins exist for any core size and, each will have different mechanical spacing. Refer to the bobbin datasheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required.

Output Power	66 kHz		132 kHz	
	Triple Insulated Wire	Margin Wound	Triple Insulated Wire	Margin Wound
0 - 10 W	EF12.6 EE13 EF16 EE16 EE19 EI22 EI22/19/6	EI22 EE19 EI22/19/6 EEL16 EF20 EI25 EEL19	EF12.6 EE13 EF16 EE16	EI22 EE19 EI22/19/6 EEL16
10 W - 20 W	EF20	EI28 EEL22 EF25	EE19 EI22 EI22/19/6 EF20	EF20 EI25 EEL19
20 W - 30 W	EF25	EI30 EPC30 EEL25		EI28
30 W - 50 W	EI28 EI30 E30/15/7 EER28	E30/15/7 EER28 ETD29 EI35 EI33/29/ 13-Z EER28L	EF25	EEL22
50 W - 70 W	ETD29 EI35 EF32	EF32 ETD34	EI28	EEL25 E30/15/7 EER28
70 W - 100 W	ETD34 E36/18/11 EI40	EI40 E36/18/11 EER35	EI30 E30/15/7 EER28 ETD29	ETD29 EI35 EI33/29/ 13-Z EER28L EF32
100 W - 150 W	ETD39 EER40	ETD39 EER40 E42/21/15	EI35 EF32 ETD34	ETD34 EI40 E36/18/11 EER35
>150 W	E42/21/15 E42/21/20 E55/28/21	E42/21/20 E55/28/21	E36/18/11 EI40 ETD39 EER40 E42/21/15 E42/21/20 E55/28/21	ETD39 EER40 E42/21/15 E42/21/20 E55/28/21

Table 5. Transformer Core Table.

As the margin reduces the available area for the windings, the margin format described above may not be suitable for small core sizes. If after entering the margin, more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design approach using triple-insulated wire.

Primary Layers, L
Primary layers should be in the range of 1 < L < 3, and in general it should be the lowest number that meets the primary current density limit (CMA). Values of 100 Cmils/Amp for designs <5 W scaling linearly to 500 Cmils/Amp at 200 W are typical in designs without forced air cooling. Designs with more than 3 layers are possible, but the increased leakage inductance and issues associated with the physical fit of the windings should be considered. A split primary construction may be helpful for designs where leakage inductance clamp dissipation is too high. Here half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement.

Secondary Turns, N_S
If the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density BM is kept below the recommended maximum of 3000 Gauss (300 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired (see the explanation of BM limits).

Step 5 – Iterate Transformer Design / Generate Prototype

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to wind a prototype transformer or sent to a vendor for samples. (See note on transformer prototying services in Quick Start section.)

The key transformer electrical parameters are:

Primary Inductance, L_P (µH)
This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $LP_{TOLERANCE}$(%)
This is the assumed primary inductance tolerance. A value of 10% is used by default; however if specific information is known from the transformer vendor, then this may be entered in the grey override cell.

Number of Primary Turns, N_P
For low leakage inductance applications, a split primary construction may be used, and is recommended for designs above 20 W.

Gapped Core Effective Inductance, A_{LG}: (nH/N²)
Used by the transformer vendor to specify the core center leg air gap.

Maximum Operating Flux Density, B_M (Gauss)
A maximum value of 3000 Gauss during normal operation is recommended. This limits transformer core loss and audible noise generated at light load levels. Under these conditions the output voltage is low, and little reset of the transformer occurs during the MOSFET off time. This allows the transformer flux density to staircase above the normal operating level. A value of 3000 Gauss at the peak current limit of the selected device, together with the built in protection features of TOPSwitch-HX, provides sufficient margin to prevent core saturation under startup or output short circuit conditions.

The MCM mode of operation used in TOPSwitch-HX can generate audio frequency components in the transformer, especially if a long core is used. This audible noise generation is minimized when a value of 3000 Gauss is used for BM. This results in an operating flux density of 750 Gauss in MCM mode. Following this guideline and using the standard transformer production technique of dip varnishing practically eliminate audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, a cure may be to replace them with capacitors having a different dielectric, for example a polyester film type.

Peak Flux Density, B_P (Gauss)
A maximum value of 4200 Gauss is recommended to limit the maximum flux density under start up and output short circuit conditions. This calculation assumes worst-case current limit and inductance values. In high ambient temperature applications, such as sealed adapters, this value may need to be reduced to 3600 Gauss due to the higher operating ambient temperature. It is important to verify that core saturation does not occur at maximum ambient temperature under overload conditions just prior to loss of regulation.

Maximum Primary Wire Diameter, OD (mm)
By default, if the override cell is empty, double insulated wire is assumed and the standard wire diameter is chosen. The grey override cells can be used to enter the wire diameter directly by the user.

The other factors automatically calculated by the spreadsheet include:

Estimated Total Insulation Thickness, INS (mm)
Primary wire size, DIA: (mm)
Primary wire gauge, AWG
Number of primary layers, L
Estimated core center leg gap length: L_g: (mm)
Number of secondary turns, N_s
Secondary wire size, DIAs: (mm)
Secondary wire gauge, AWG

In multiple output design NSx, CMSx, AWGSx (where x is the output number) should also be used.

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1281	uHenries	Primary Inductance
LP Tolerance	5		5		Tolerance of Primary Inductance
NP			123		Primary Winding Number of Turns
NB			14		Bias Winding Number of Turns
ALG			85	nH/T^2	Gapped Core Effective Inductance
BM			2901	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			3736	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			580	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1776		Relative Permeability of Ungapped Core
LG			0.73	mm	Gap Length (Lg > 0.1 mm)
BWE			46.8	mm	Effective Bobbin Width
OD			0.38	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.32	mm	Bare conductor diameter
AWG			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			128	Cmils	Bare conductor effective area in circular mils
CMA		Warning	198	Cmils/Amp	!!! INCREASE CMA>200 (increase L(primary layers),decrease NS,larger Core)
Primary Current Density (J)			9.99	Amps/mm^2	!!! Decrease current density Use larger wire diameter, increase L or increase core size.

Figure 10. Transformer Primary Design Parameters Section of Spreadsheet.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5	Volts	Output Voltage
IO1_AVG			7	Amps	Average DC Output Current
PO1_AVG			35.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			5.00		Output Winding Number of Turns
ISRMS1			12.176	Amps	Output Winding RMS Current
IRIPPLE1			9.96	Amps	Output Capacitor RMS Ripple Current
PIVS1			20	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			2435	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			16	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			1.29	mm	Minimum Bare Conductor Diameter
ODS1			3.12	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.64		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.64		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			35	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Figure 11. Transformer Secondary Design Parameters Section of Spreadsheet – Multiple Outputs.

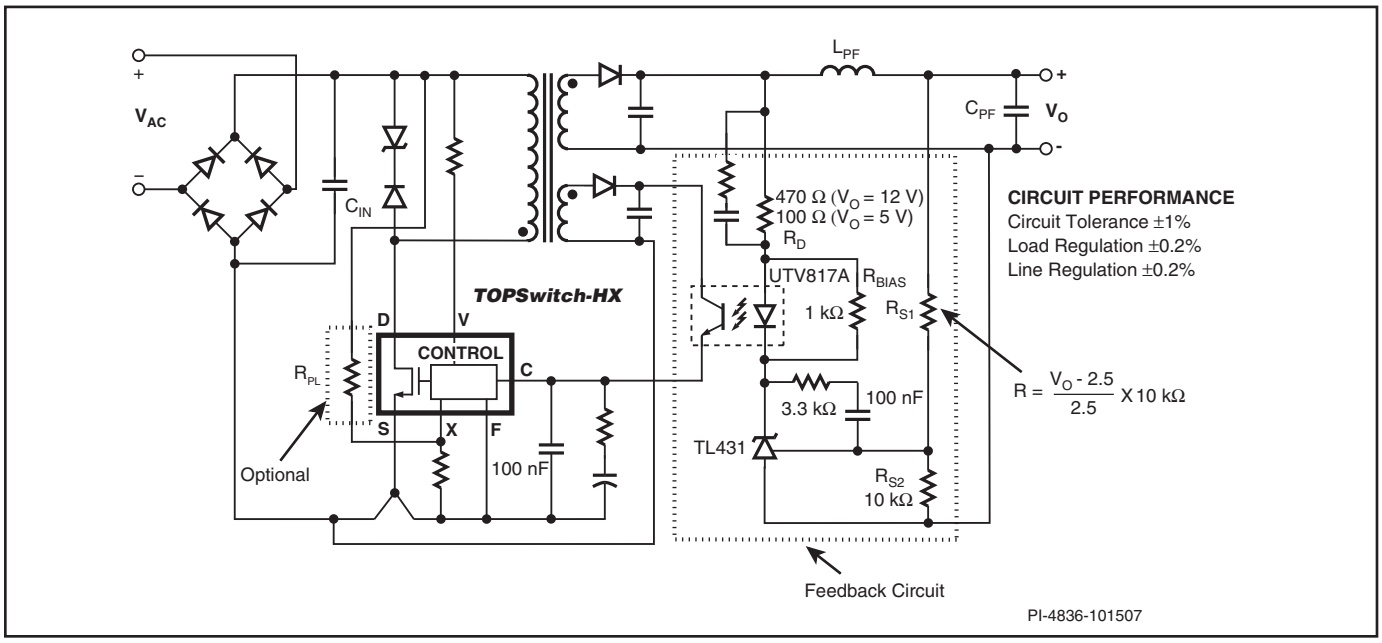

Figure 12. Typical TOPSwitch-HX *Flyback Power Supply Using Optocoupler-TL431 Feedback Circuit.*

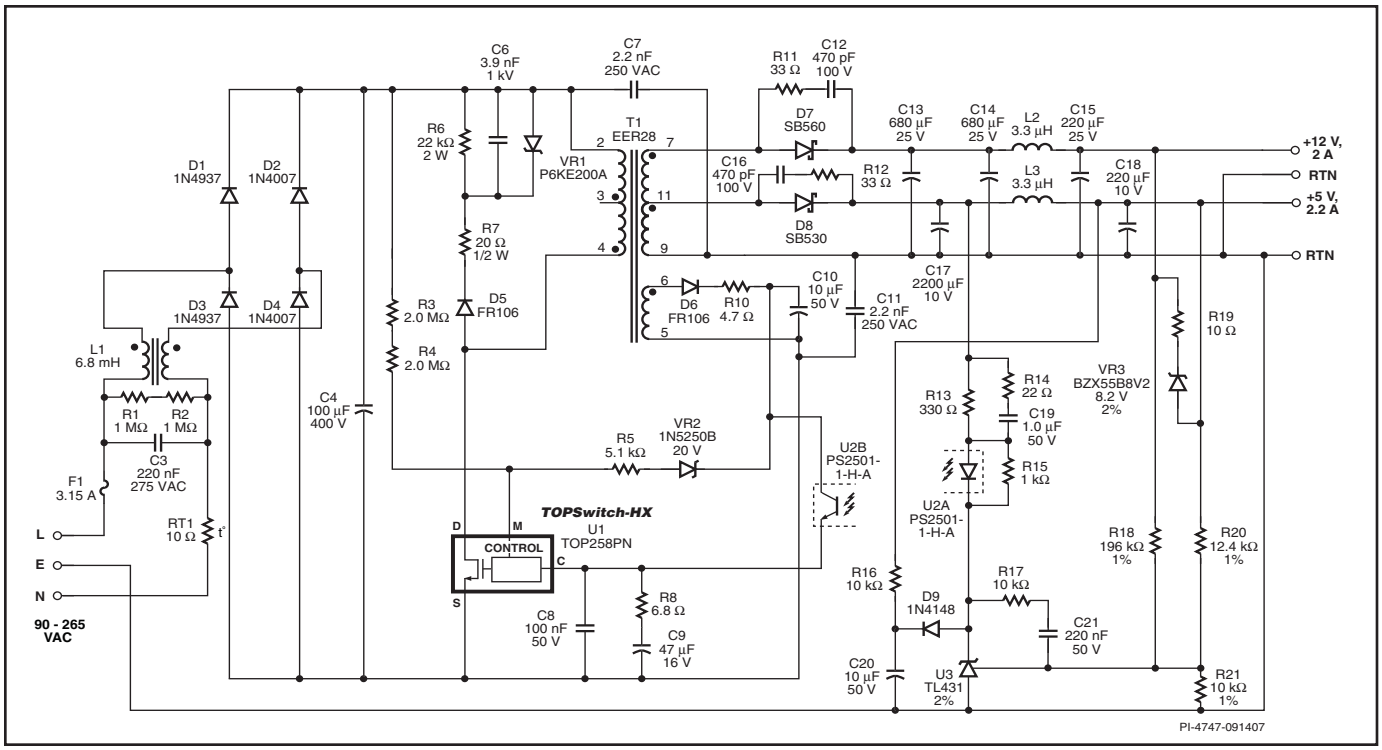

Figure 13. Universal Input, 35 W Power Supply Using TOP258PN.

Step 6 – Selection of TOPSwitch-HX External Components

Control Pin – External Components

The schematic in Figure 12 shows the external components required for a typical TOPSwitch-HX power supply design. It is strongly recommended that a 100 nF capacitor be connected between the CONTROL pin and the SOURCE pin of the TOPSwitch-HX. This capacitor should be located adjacent to the TOPSwitch-HX with short traces. In designs using surface mount components, this capacitor should be located directly at the pins of the TOPSwitch-HX.

In addition to the 100 nF capacitor connected to the CONTROL pin, a series combination of a 6.8 Ω resistor and a 47 µF electrolytic capacitor is required to be connected between the CONTROL pin and the SOURCE terminal of the TOPSwitch-HX. The capacitor provides both timing for auto-restart and, together with the dynamic impedance Z_C of the CONTROL pin, sets the dominant pole for the control loop. The combination of the capacitor and series resistor adds a zero to the transfer function of the control loop, The resulting phase boost at approximately 200 Hz improves the bandwidth of the power supply.

Step 7 – Selection of Line - Undervoltage / Overvoltage Components

The line undervoltage detection feature prevents the power supply from starting until the input voltage is above a defined level. During power-up or when the switching of the power MOSFET is disabled during auto-restart, the current into the EN/UV pin must exceed 25 µA to initiate switching (I_{UV} in data sheet). As a resistor from the DC rail to the V pin is used to sense the input voltage, the supply voltage that causes the current into the V pin to exceed 25 µA defines the undervoltage threshold. The resistor connected to the V pin also sets the voltage at which a line input overvoltage condition will be detected.

The sense resistor should be rated above 400 V, generally requiring either a single 0.5 W or two 0.25 W devices connected in series. A typical value of 4 MΩ is suggested for use as line sense resistor for Universal input applications. Additional guidance is provided by the design spreadsheet.

If the undervoltage (UV) or the overvoltage (OV) functions are to be used selectively, a number of circuits are provided in the TOPSwitch-HX family datasheet to ease the selection of external components. If the V pin function is not used, the V pin should be connected to the source pin. The V pin should not be left unconnected.

Step 8 – Selection of Primary Clamp Components

It is recommended that either a Zener clamp or an RCD combined with a Zener clamp be used in TOPSwitch-HX designs. This is to ensure that the peak drain voltage is limited to below the BV_{DSS} of the internal MOSFET while still maximizing efficiency and minimizing no-load consumption.

A standard RCD clamp designed to limit the peak drain voltage under peak load conditions represents a significant load as the output power is reduced, resulting in lower light-load efficiency and higher no-load consumption.

Figure 13 shows an example of an optimized clamp arrangement. The clamp ensures that peak drain voltage is limited to an acceptable level under worst-case conditions of maximum input voltage, the overload power or output short circuit and maximum ambient temperature.

Rec. Diode	V_R(V)	I_D(A)	Package	Manufacturer
Schottky				
1N5819	40	1	Axial	General Semi
SB140	40	1	Axial	General Semi
SB160	60	1	Axial	General Semi
MBR160	60	1	Axial	IR
11DQ06	60	1.1	Axial	IR
1N5822	40	3	Axial	General Semi
SB340	40	3	Axial	General Semi
MBR340	40	3	Axial	IR
SB360	60	3	Axial	General Semi
MBR360	60	3	Axial	IR
SB540	40	5	Axial	General Semi
SB560	60	5	Axial	General Semi
MBR745	45	7.5	TO-220	General Semi / IR
MBR760	60	7.5	TO-220	General Semi
MBR1045	45	10	TO-220	General Semi / IR
MBR1060	60	10	TO-220	General Semi
MBR10100	100	10	TO-220	General Semi
MBR1645	45	16	TO-220	General Semi / IR
MBR1660	60	16	TO-220	General Semi
MBR2045CT	45	20(2×10)	TO-220	General Semi / IR
MBR2060CT	60	20(2×10)	TO-220	Genreal Semi
MBR20100	100	20(2×10)	TO-220	General Semi / IR
UFR				
UF4002	100	1	Axial	General Semi
UF4003	200	1	Axial	General Semi
MUR120	200	1	Axial	General Semi
EGP20D	200	2	Axial	General Semi
BYV27-200	200	2	Axial	General Semi / Philips
UF5401	100	3	Axial	General Semi
UF5402	200	3	Axial	General Semi
EGP30D	200	3	Axial	General Semi
BYV28-200	200	3.5	Axial	General Semi / Philips
MUR420	200	4	TO-220	General Semi
BYW29-200	200	8	TO-220	General Semi Philips
BYV32-200	200	18	TO-220	General Semi / Philips

Table 6. List of Diodes Suitable for use as the output rectifier.

The peak drain voltage should be limited to a maximum of 650 V under these conditions to provide a margin for component variation. In the design shown in Figure 13, the peak drain voltage was limited to 600 V. The clamp diode (D5) must be a fast or an ultra-fast recovery type with a reverse recovery time <500 ns. Under no circumstances should a standard recovery rectifier diode be used. The high dissipation that may result during startup or an output short circuit can cause failure of the diode. Resistor R7 damps ringing for reduced EMI.

Power supplies using different members of the TOPSwitch-HX family will have different peak primary currents and leakage inductances, and therefore different leakage energy. Capacitor C6 and R6 must be optimized for each design. As a general rule, minimize the value of capacitor C6 and maximize the value of resistor R6 while still meeting the recommended 650 V peak drain voltage limit.

Step 9 – Select Output Rectifier Diode

For each output use the values of peak inverse voltage (V_R) and output current (I_O) provided in the design spreadsheet to select the output diodes. Table 6 shows some commonly available types.

$V_R \geq 1.25 \times PIV_S$: where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

$I_D \geq 2 \times I_O$: where ID is the diode rated DC current, and I_O is the average output current. Depending on the temperature rise and the duration of the peak load condition, it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heatsinking required.

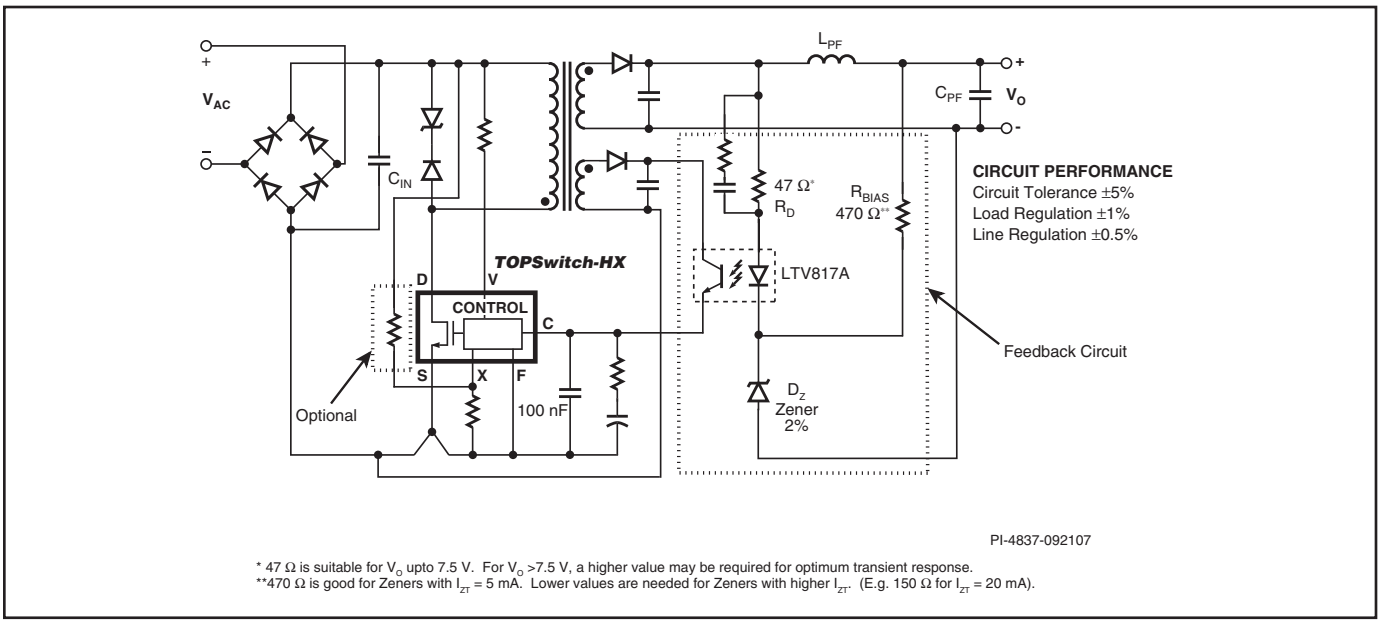

Figure 14. Typical Zener Feedback Circuit.

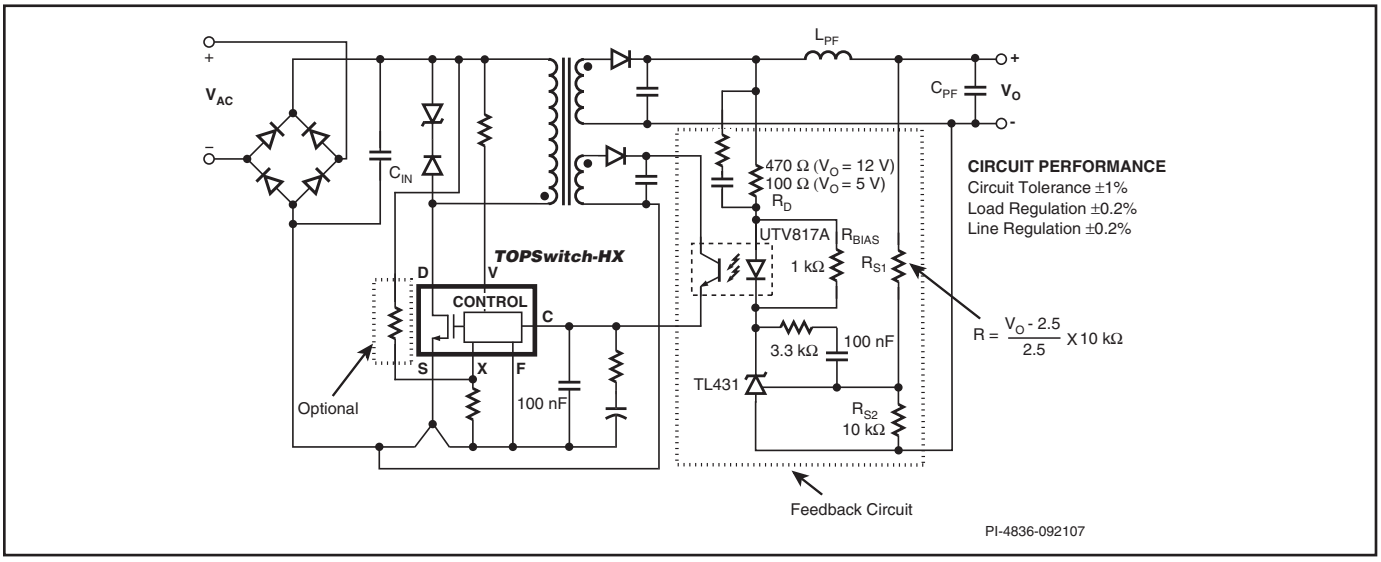

Figure 15. Optocoupler-TL431 Feedback Circuit.

Step 10 – Select Output Capacitor

Ripple Current Rating

The spreadsheet calculates output capacitor ripple current using the average output power. Therefore the actual rating of the capacitor will depend on the peak to average power ratio of the design. In most cases this assumption will be valid as capacitor ripple rating is a thermal limitation, and most peak load durations are shorter than the thermal time constant of the capacitor (< 1 s). For such designs, select the output capacitor(s) such that the ripple rating is greater than the calculated value of I_{RIPPLE} from the spreadsheet. However, in designs with high peak to continuous (average) power and long duration peak load conditions, the capacitor rating may need to be increased based on the measured capacitor temperature rise under worst-case load and ambient conditions.

In either case, if a suitable individual capacitor cannot be found, then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should also be considered to ensure that the capacitor is not oversized.

ESR Specification

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a capacitor rated for the output ripple, will result in an acceptable value of ESR.

Voltage Rating

Select a voltage rating such that $V_{RATED} \geq 1.25 \times V_O$

Step 11 – Select Feedback Circuit Components

The choice of the feedback circuit for a power supply is governed by the desired output regulation. A simple feedback circuit can be configured using a Zener diode in series with the optocoupler diode. Though this method is inexpensive, it relies on the Zener diode to control the output voltage, which limits performance due to the device's typically poor tolerance and temperature coefficient.

Figure 14 shows a typical implementation of Zener feedback. The drop across the Zener diode D_Z, optocoupler series resistor R_{FB1} and the optocoupler LED determine the output voltage. Resistor R_{BIAS} provides a 1 mA bias current so that the Zener diode is operating close to its knee voltage. Resistor R_D sets the DC gain of the feedback. Both these can be 0.125 W or 0.25 W, 5% types. Selecting a Zener with a low test current ($I_{ZT} \leq 5$ mA) is recommended to minimize the current needed to bias the feedback network, reducing no-load input power consumption.

P/N	CTR(%)	BVCEO	Manufacturer
4 Pin DIP			
PC123Y6	80-160	70 V	Sharp
PC817X1	80-160	70 V	Sharp
SFH615A-2	63-125	70 V	Vishay, Isocom
SFH617A-2	63-125	70 V	Vishay, Isocom
SFH618A-2	63-125	55 V	Vishay, Isocom
ISP817A	80-160	35 V	Vishay, Isocom
LTV817A	80-160	35 V	Liteon
LTV816A	80-160	80 V	Liteon
LTV123A	80-160	70 V	Liteon
K1010A	60-160	60 V	Cosmo
6 Pin DIP			
LTV702FB	63-125	70 V	Liteon
LTV703FB	63-125	70 V	Liteon
LTV713FA	80-160	35 V	Liteon
K2010	60-160	60 V	Cosmo
PC702V2NSZX	63-125	70 V	Sharp
PC703V2NSZX	63-125	70 V	Sharp
PC713V1NSZX	80-160	35 V	Sharp
PC714V1NSZX	80-160	35 V	Sharp
MOC8102	73-117	30 V	Vishay, Isocom
MOC8103	108-173	30 V	Vishay, Isocom
MOC8105	63-133	30 V	Vishay, Isocom
CNY17F-2	63-125	70 V	Vishay, Isocom, Liteon

Table 7. Optocouplers.

For improved accuracy, Figure 15 shows a typical implementation using a reference IC. A TL431 is used to set the output voltage and is programmed via a resistor divider R_{S1} and R_{S2}. Resistor R_{BIAS} provides the minimum operating current for the TL431 while R_D sets the DC gain. The 100 nF capacitor and series resistor roll off the gain of TL431 so that it does not respond to cycle-by-cycle output ripple voltage. AC feedback is provided directly through the optocoupler. An RC circuit placed across the resistor R_D can provide additional phase boost to improve control loop bandwidth.

A post filter (L_{PF} and C_{PF}) is typically added to reduce high frequency switching noise and ripple. Inductor L_{PF} should be in the range of 1 µH – 3.3 µH with a current rating above the peak output current. Capacitor C_{PF} should be in the range of 100 µF to 330 µF with a voltage rating ≥1.25 x V_{OUT}. If a post filter is used then the optocoupler should be connected as shown, before the post filter inductor and the sense resistors, after the post filter inductor (when applicable).

Table 7 is a list of commonly used optocouplers for feedback control of isolated switching power supplies. Use of an optocoupler with a CTR of 0.8 to 2 is recommended.

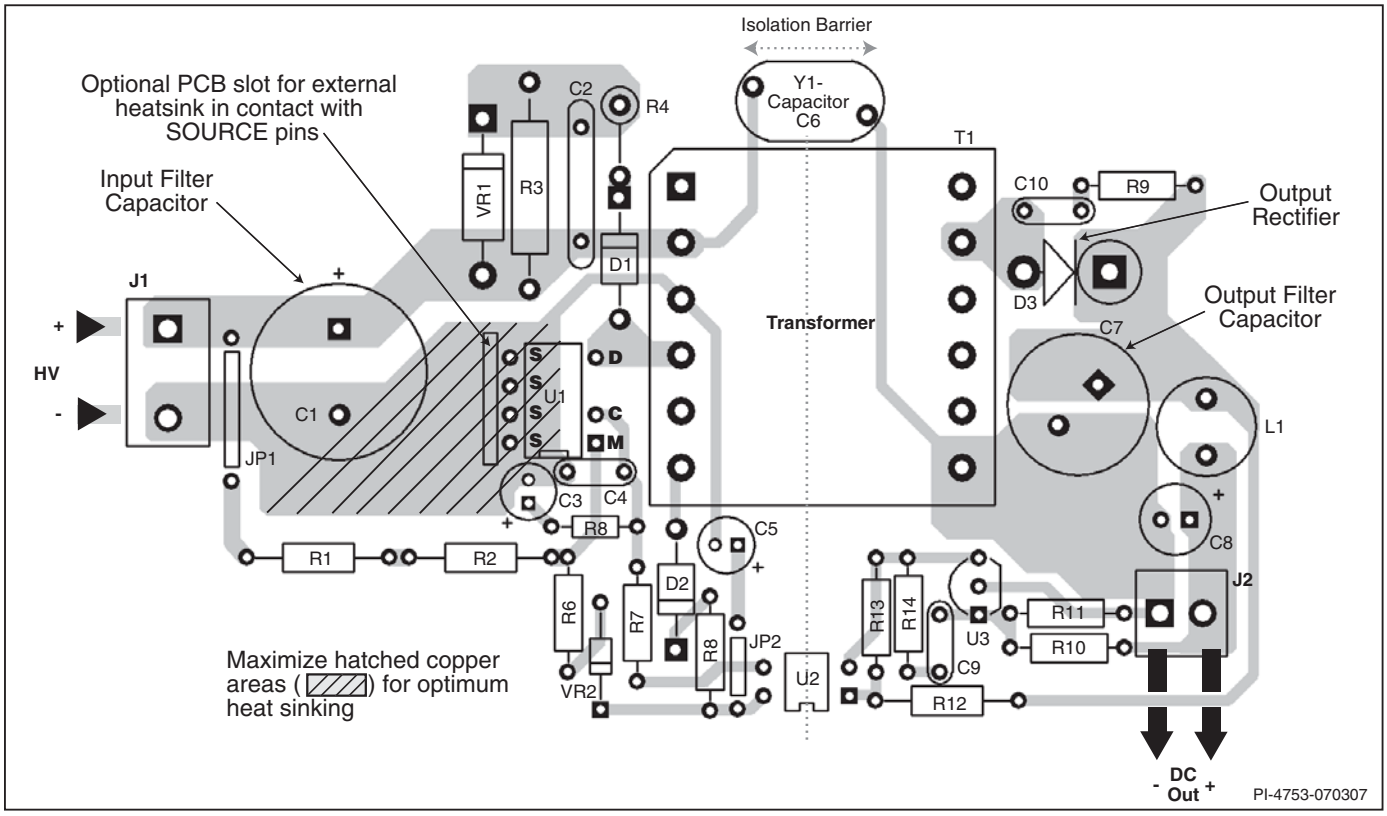

Figure 16. PCB Layout Example Using P-Package.

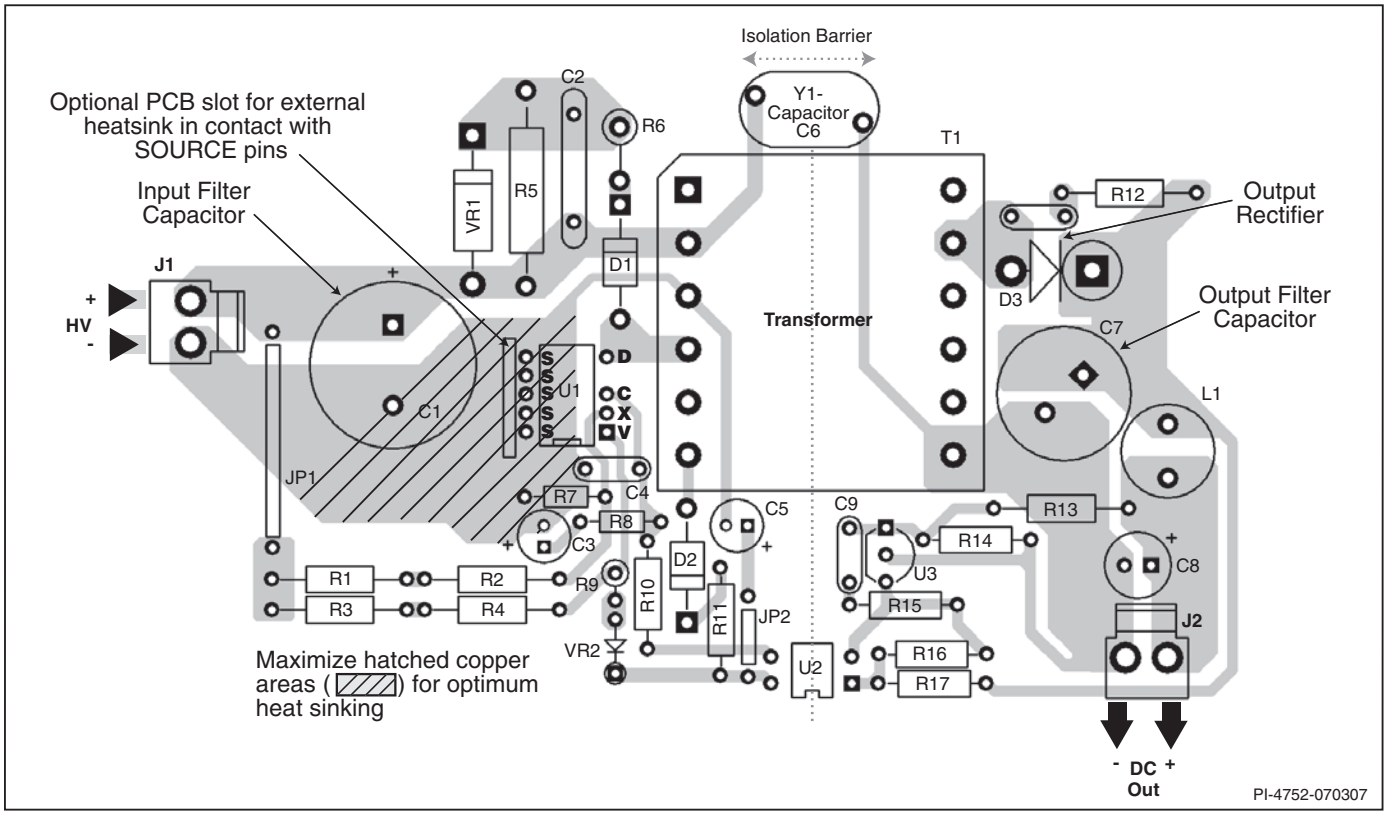

Figure 17. PCB Layout Example Using M-package.

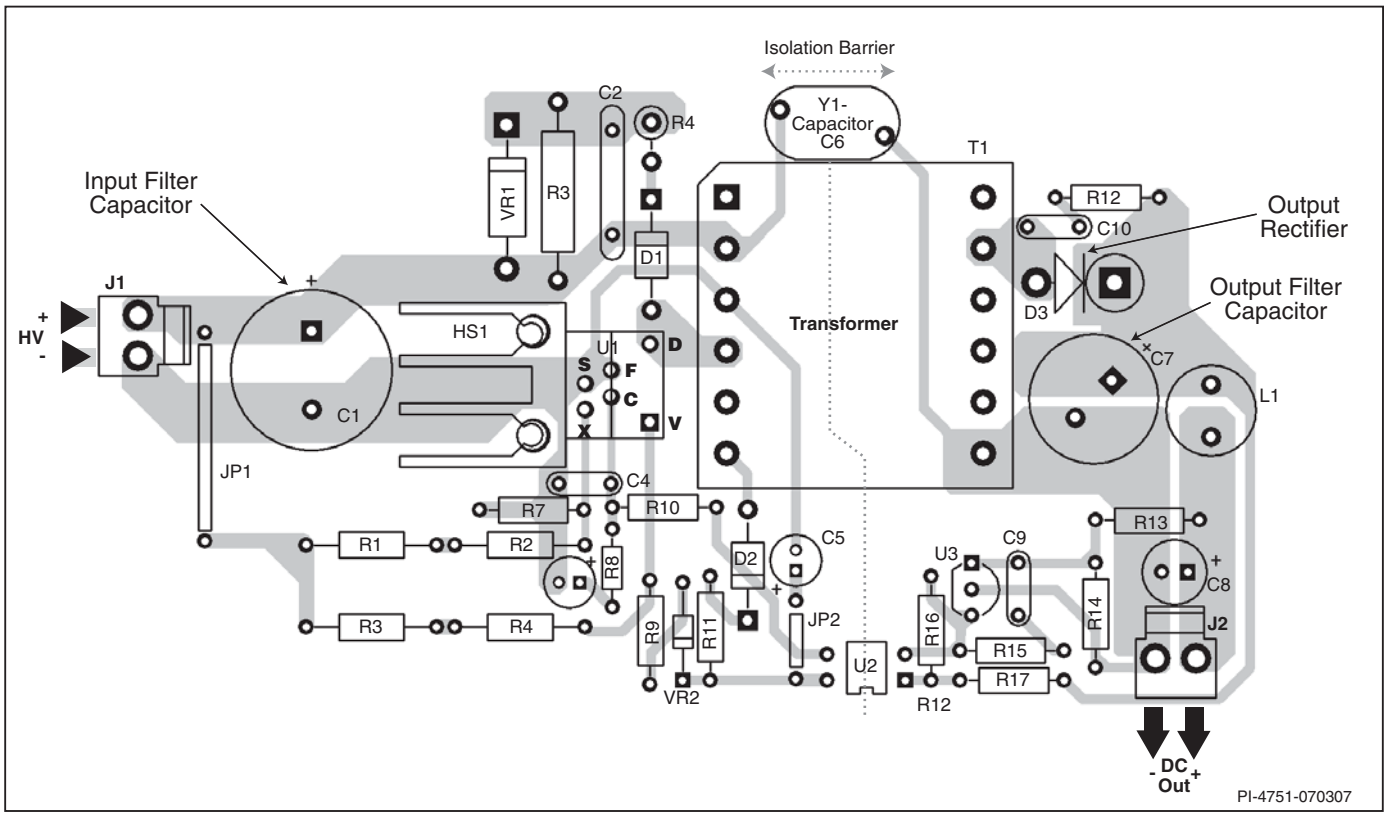

Figure 18a. PCB Layout Example Using Y-package.

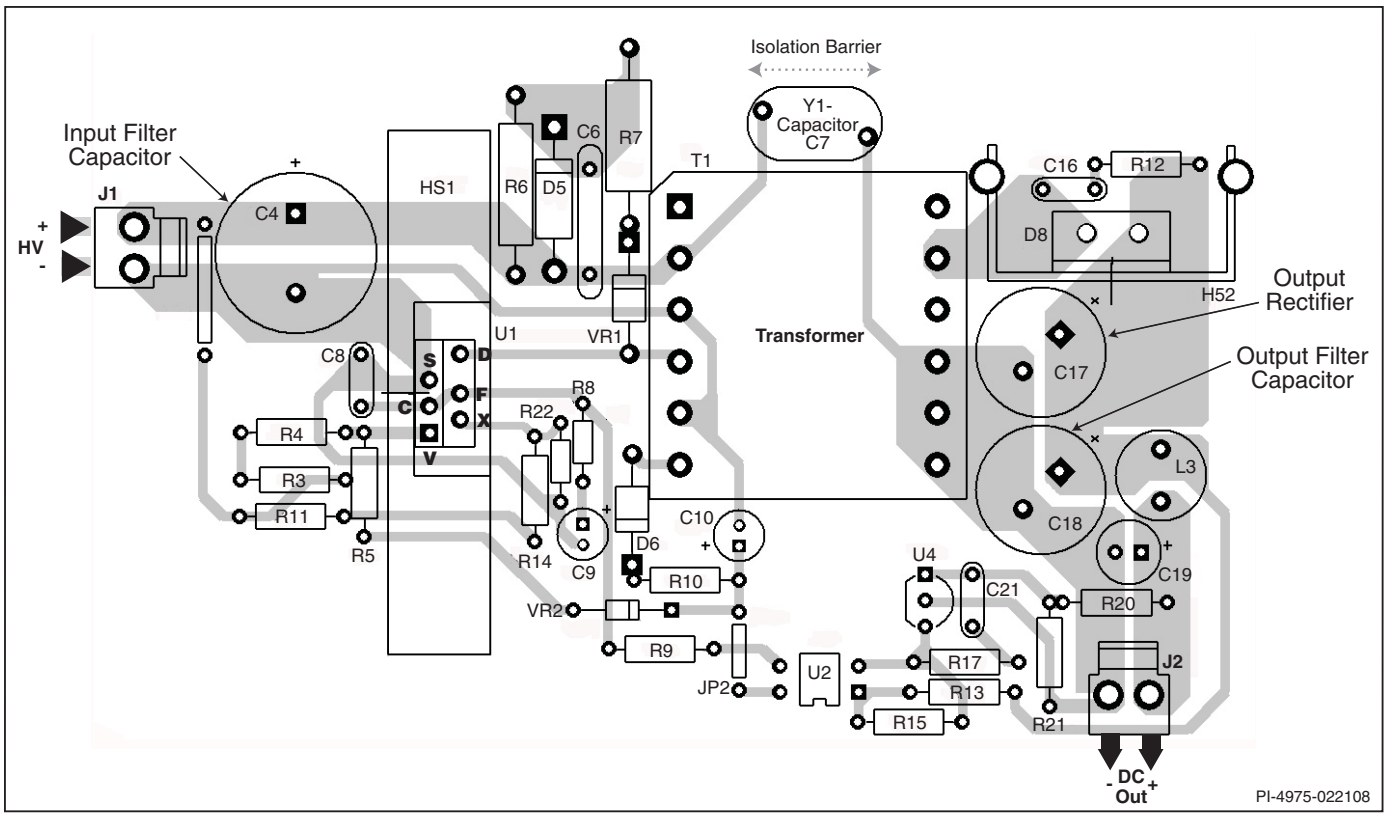

Figure 18b. Layout Considerations for TOPSwitch-HX Using E-Package and Operating at 66 KHz.

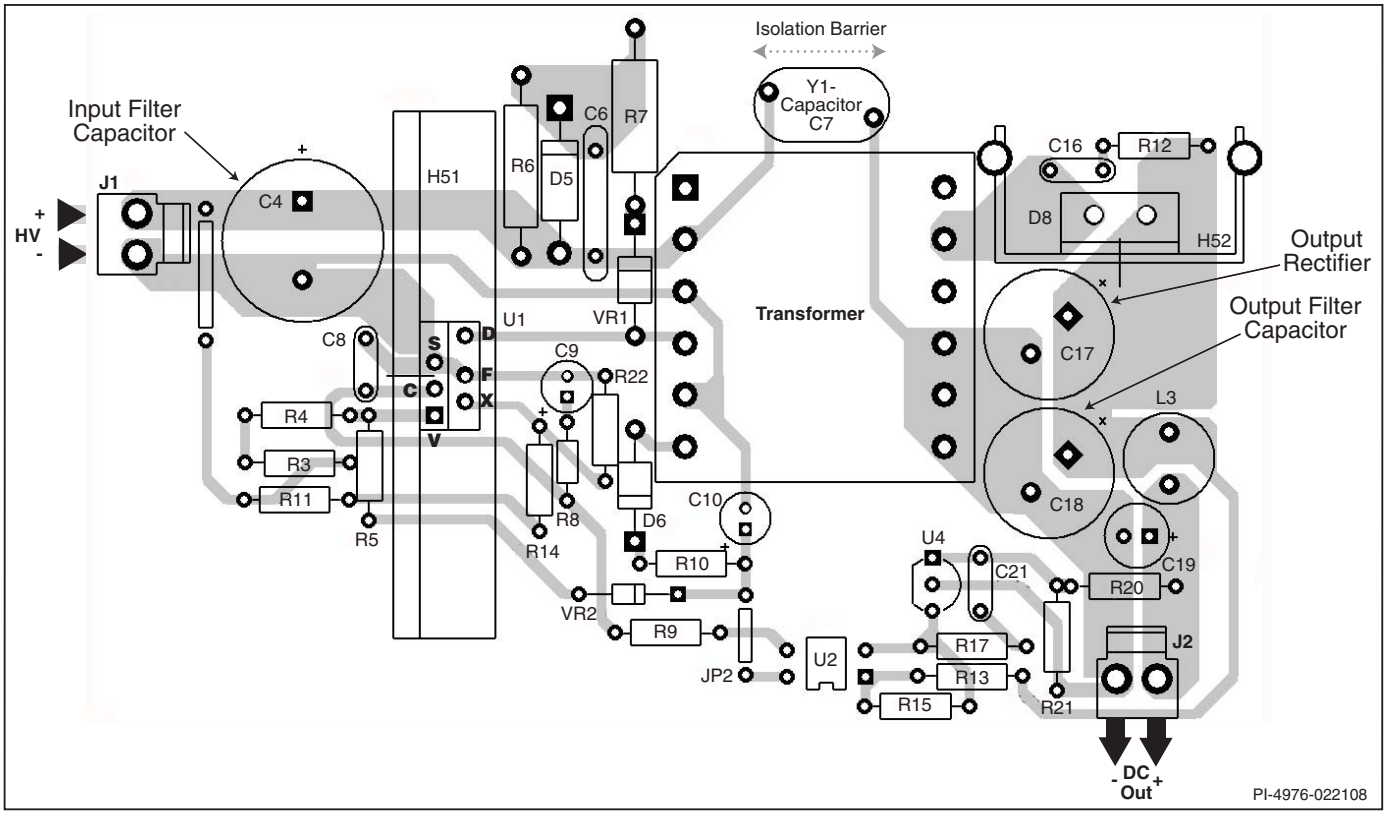

Figure 18c. Layout Considerations for TOPSwitch-HX Using E-Package and Operating at 132 KHz.

Tips for Designs

Design Recommendations:

- A soft finish circuit is recommended for high output voltage designs (>12 V). This ensures startup with full load at low line. In Figure 22, R23, D6 and C19 show one implementation of the soft finish circuit.
- A 10 µF, 50 V electrolytic capacitor is recommended for the bias winding output filter to ensure appropriate bias voltage for the optocoupler when the power supply is unloaded. The bias winding output voltage should be a minimum of 10 V or higher.

Circuit Board Layout

TOPSwitch-HX is a highly integrated power supply solution that integrates on a single die both the controller and the high voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply.

When designing a PCB for the TOPSwitch-HX based power supply, it is important to follow the following guidelines:

Primary Side Connections

- Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the TOPSwitch-HX SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.
- The CONTROL pin bypass capacitor should be located as close as possible to the SOURCE and CONTROL pins and its SOURCE connection trace should not be shared by the main MOSFET switching currents or bias winding return connection.
- All SOURCE pin referenced components connected to the MULTI-FUNCTION (M), VOLTAGE MONITOR (V) or EXTERNAL CURRENT LIMIT (X) pins should also be located closely between that pin and the SOURCE pin. The SOURCE connection trace of these components should not be shared by the main MOSFET switching or bias winding return currents. It is very critical that the SOURCE pin switching current is returned to the input capacitor negative terminal through a separate trace that is not shared by the components connected to CONTROL, MULTI-FUNCTION, VOLTAGE-MONITOR or EXTERNAL CURRENT LIMIT pins. This is because the SOURCE pin is also the controller ground reference pin. Any traces to the M, V or X pins should be kept as short as possible and physically away from the DRAIN node, clamp components or any node with high di/dt or dv/dt, to prevent noise coupling.
- The LINE-SENSE resistor should be located close to the M or V pin to minimize the trace length on the high impedance M or V pin side. The DC bus side of the V pin resistor should be connected as close to the bulk capacitor as possible.
- In addition to the 47 µF CONTROL pin capacitor, a high frequency 0.1 µF bypass capacitor in parallel should be used for local decoupling (C4 in Figures 16, 17 and 18).
- The feedback optocoupler output should be routed away from any high voltage or high current traces to prevent noise coupling.

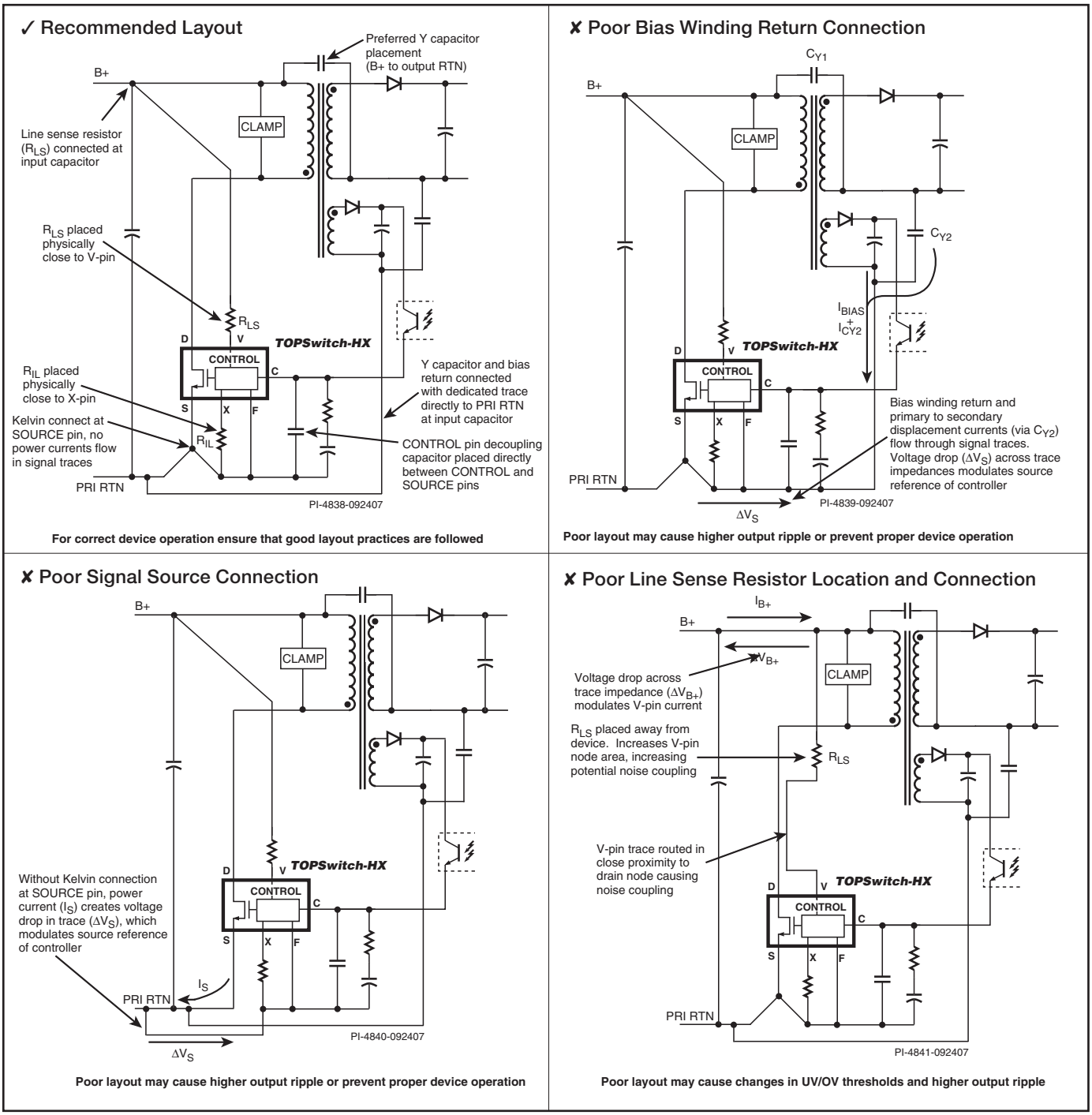

Figure 19. Layout Considerations (Shown Schematically) and Common Mistakes.

Y-Capacitor

The preferred Y-capacitor connection is close to the transformer secondary output return pin(s) and the positive primary DC input pin of the transformer. If the Y capacitor is connected between primary and secondary RTN, then the primary connection should be made via a dedicated trace from the Y-capacitor to the negative input capacitor terminal. This ensures that surge currents across the isolation barrier are routed away from traces connected to the TOPSwitch-HX.

Secondary

To minimize leakage inductance and EMI, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heatsinking. A larger area is preferred at the quiet cathode terminal as a large anode area can increase high frequency radiated EMI.

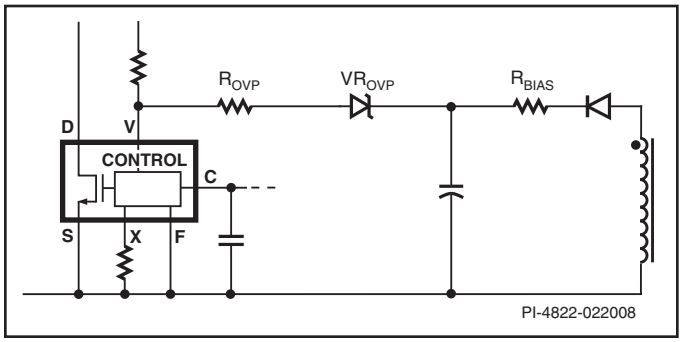

Figure 20. Primary Sensed OVP circuit for TOPSwitch-HX *based Flyback Power Supply.*

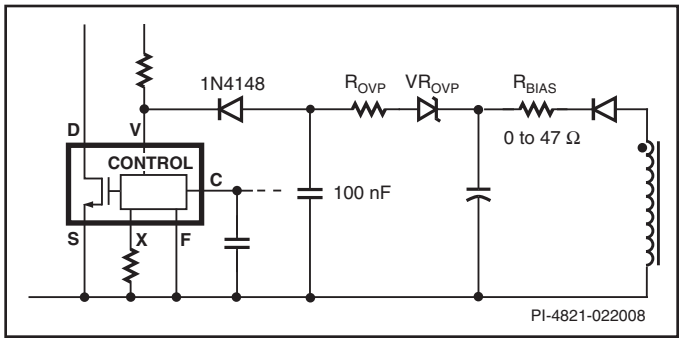

Figure 21. Primary Sensed Overvoltage Protection Circuit for a Flyback Power Supply Using TOPSwitch-HX *with Additional V-pin Noise Decoupling.*

Common Layout Problems to Avoid

A poor layout will often result in performance issues that may be time consuming to analyze, and they may occur at the end of development, when PCB design changes are difficult. Figure 19 will help quickly identify the root cause of a problem and correct the layout. The figure schematically shows common layout mistakes and the reasons they should be avoided

Implementing Overvoltage Protection Feature Using the TOPSwitch-HX

The bias winding output tracks the changes in the output voltage for the flyback topology. If the feedback loop fails and results in an increase in output voltage, the output voltage of the bias winding will also increase. This can be used to detect an output overvoltage condition.

A suitable Zener diode with a series resistor connected between the bias winding output and the V pin can be selected such that the Zener diode conducts once the bias winding voltage rises significantly (typically 20% to 30%) above the highest voltage at the output of the bias winding during normal operation (or under a transient loading condition during normal operation). A current injected in the V-pin in excess of 112 µA will result in the switching cycle being terminated instantaneously. If the injected current remains higher than 112 µA for over 100 µS, the part will enter hysteretic OV shutdown. In such a situation, switching will resume as soon as the injected current reduces below the hysteresis point after completing an auto-restart cycle.

If the injected current exceeds 112 µA, the V-pin responds by dropping the V-pin voltage by 0.5 V. If the drop in V-pin voltage causes the V-pin current to jump to a value higher than 336 uA, the part enters a state of latched shutdown. In this state the operation will not resume unless input is cycled and the C-pin capacitor is allowed to discharge, thereby resetting the part. In addition the latched state may be reset by pulling the V-pin below 1 V with an external transistor. Care must be taken when designing external circuits connected to the V-pin. The V-pin operates at very low currents to reduce no-load power consumption. This results in the V pin node having a relatively high impedance, and it is therefore susceptible to noise. See the layout guidline section for more detailed information. If the value of the series resistor R_{OVP} is very small (in the range of 5 Ω to 22 Ω), the change of V-pin voltage in response to the injected current reaching 112 µA is often adequate to cause a current in excess of 336 µA to flow which results in latched overvoltage condition, requiring a reset.

In some designs the Zener diode connected from the bias winding may become a source of noise injected into the V-pin. This happens when the bias winding output ripple is high, or the circuit board layout allows noise from adjacent circuits to be coupled in the trace connecting the Zener diode to the V-pin. In such a situation, the solution shown in Figure 21 should be used.

The circuit shown in Figure 21 is also useful in situations where it is difficult to achieve a latched shutdown due to slow rise in power supply and bias winding output voltages after the feedback loop opens. Power supplies with large output capacitance and/or high output load may have this issue during an open loop fault. If necessary, R_{BIAS} can be added to provide additional filtering of the bias output to prevent false triggering of the OVP function.

Designing With the Y-Package (TOP259-TOP261)

The Y-Package option is offered for devices capable of delivering high power. Operation at high power involves high drain switching currents, which can lead to a considerable amount of switching noise that can affect device operation. The use of a dedicated pin for signal return (G pin) on the Y-Package reduces noise coupling and ensures stable operation.

The circuit on page 20 shows the standard configuration with the Y-Package parts (TOP259-TOP261).

Note: The shorter pin length of the E package reduces noise coupling. For this reason, TOPSwitch-HX devices using the E packages do not require a dedicated G pin.

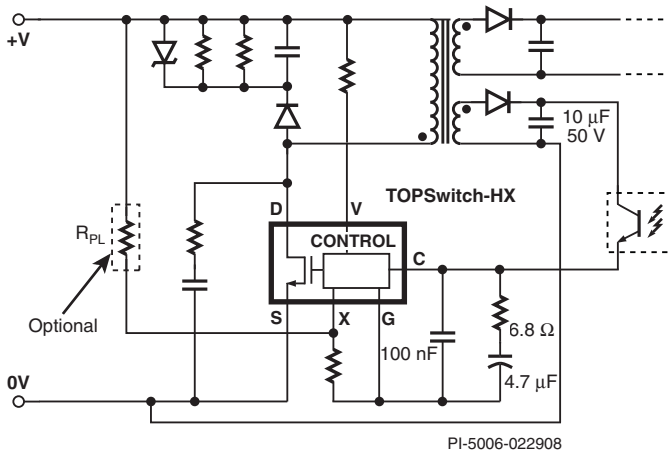

Figure 22. Recommended Circuit Configuration for TOP259YN - TOP261YN with G Pin.

Designing High-Power Power Supplies Using TOPSwitch – HX

At high power levels, design of power supplies using a flyback topology presents the following challenges.

1. Proximity losses in the transformer can be significant and make design of flyback transformers at high power levels very sensitive to the construction method with respect to winding configuration and the choice of the number of strands in multi wire configuration. The choice of wire size in a high frequency transformer is dependent on switching frequency. Skin depth is proportional to switching frequency and limits the usable cross sectional area of each conductor. Multi strand (filar) windings and litz wires are commonly used to reduce conduction losses in high frequency transformers. To further reduce skin effects, the use of foil windings is recommended for low voltage high current outputs.
2. Slight increases in leakage inductance of the transformer and PCB traces can lead to a large increase in dissipation in the snubber circuit. To reduce leakage inductance, it is important to use sandwich winding construction in the transformer and minimize PCB trace lengths, especially the loop formed by the secondary winding, output diode and output capacitors. Design of the snubber circuit is critical in achieving high efficiency; typically, at high power levels a correctly sized RCD clamp will ensure that the drain source voltage does not exceed 650 V.
3. At high output currents, the secondary ripple current increases and may be above the rating of a single very low ESR output capacitor. It is therefore common to use multiple capacitors in parallel. In this case, special attention must be paid to equalize the trace length to all capacitors to give even distribution of the ripple current. This ensures equal dissipation and temperature rise, critical to ensure an acceptable operating life. Even with multiple capacitors, a second-stage LC filter is required to reduce switching frequency ripple.
4. Minimize the length and loop area of PCB traces that carry large switching currents and voltages as these can be a source of radiated EMI.

For high power designs using any TOPSwitch-HX, and especially for designs that use TOP259 – TOP261, it is recommended that provision is made on the PCB board for a small RC network positioned between the DRAIN and SOURCE terminals. This reduces switching noise from affecting power supply operation and also helps in reduction of EMI. A 22 Ω to 150 Ω network resistor and a 1 kV rated ceramic capacitor in the range of 10 pF to 33 pF will be suitable for most applications. See Figure 27.

Quick Design Checklist

As with any power supply, all TOPSwitch-HX designs should be verified with actual hardware to ensure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 675 V at highest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just before the power supply goes into auto-restart (loss of regulation).
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. TOPSwitch-HX has a minimum leading edge blanking time of 180 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope for the drain current waveform at the end of the 180 ns minimum blanking period.
3. Thermal check – At maximum output power, minimum and maximum input voltage and maximum ambient temperature;

verify that temperature limits are not exceeded for the TOPSwitch-HX, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation in the $R_{DS(ON)}$ of TOPSwitch-HX, as specified in the data sheet. A maximum source pin temperature for the P/G and M packages or tab temperature for Y/E packages of 110 °C is recommended to allow for these variations. Alternatively, the design margin can be verified by connecting an external resistance that is in series with the DRAIN pin and is attached to the same heat sink. The resistance selected would be equal to the difference between the measured $R_{DS(ON)}$ of the device under test and the worst case maximum specification.

Appendix A

Application Examples

A High Efficiency, 150 W, 250 – 380 VDC Input Power Supply

The circuit shown in Figure 23 delivers 150 W (19 V at 7.7 A) at 84% efficiency using a TOP258YN from a 250 VDC to 380 VDC input. A DC input is shown, as typically at this power level a power factor correction stage would precede the power supply. Capacitor C1 provides local decoupling, necessary when the supply is remote from the main PFC output capacitor.

Flyback topology is still usable at this power level due to the high output voltage, keeping the secondary peak currents low enough to ensure that the output diode and capacitors are reasonably sized. In this example, the TOP258YN is close to the upper limit of its power capability.

Resistors R3, R6 and R7 provide power limiting, maintaining relatively constant overload power with input voltage. Line sensing is implemented by connecting a 4 MΩ resistor from the V pin to the DC rail. Resistors R4 and R5 together form the 4 MΩ line sense resistor. If the DC input rail rises above 450 VDC, then TOPSwitch-HX will stop switching until the voltage returns to normal, preventing device damage.

Due to the high primary current, a low leakage inductance transformer is essential. Therefore, a sandwich winding with a copper foil secondary is used. Even with this technique, the leakage inductance energy is beyond the power capability of a simple Zener clamp. Therefore, R1, R2 and C3 are added in parallel to VR1 and VR3, two series Zener diodes being used to share dissipation. During normal operation, very little power is dissipated by VR1 and VR3, the leakage energy instead being dissipated by R1 and R2. However, VR1 and VR3 are essential to limit the peak drain voltage during start-up and/or overload conditions to below the 700 V rating of the TOPSwitch-HX MOSFET. The schematic shows an additional snubber circuit, consisting of R20, R21, R22, D5 and C18. This reduces turn-off losses in the TOPSwitch-HX.

The secondary is rectified and smoothed by D2, D3 and C5, C6, C7 and C8. Two windings are used and rectified with

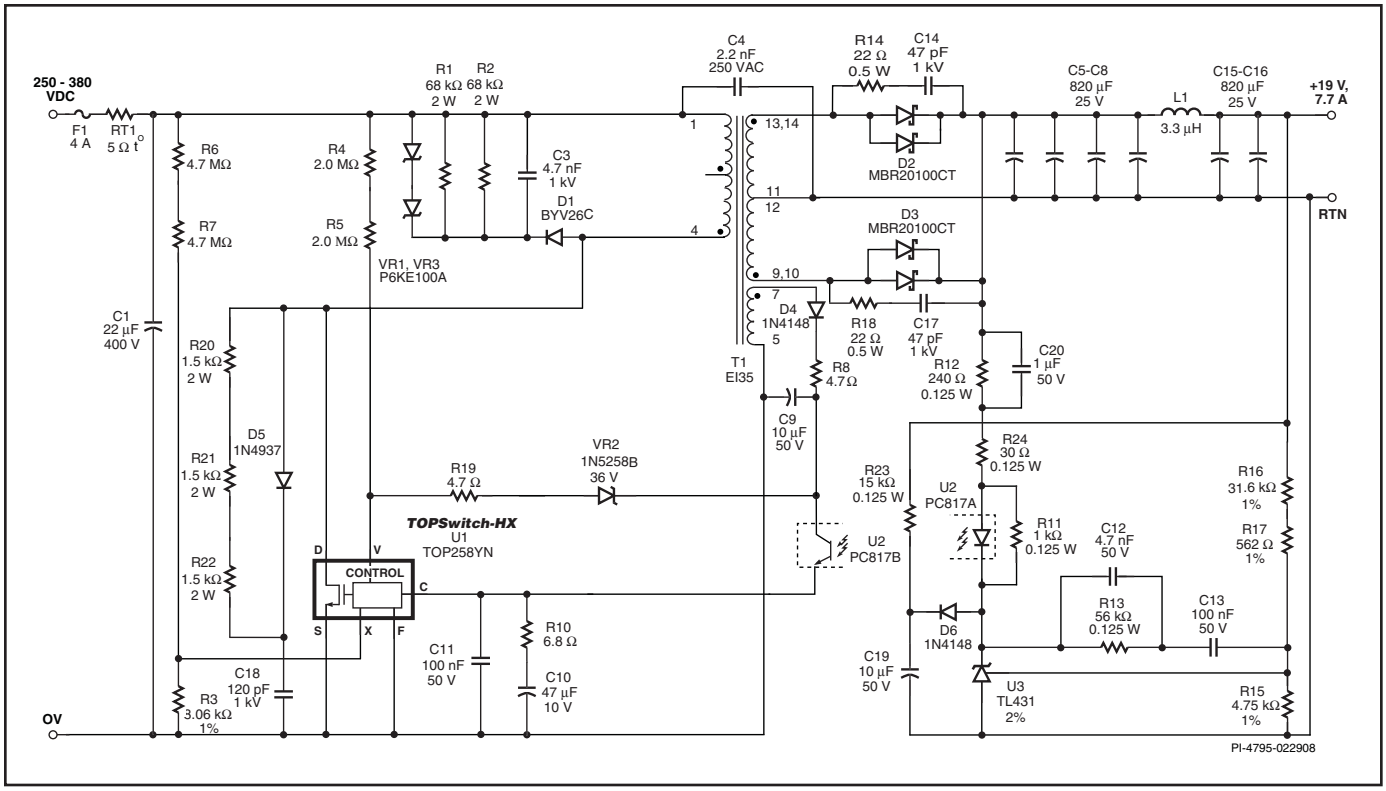

Figure 23. 150 W, 19.5 V Power Supply using TOP258YN.

separate diodes D2 and D3 to limit diode dissipation. Four capacitors are used to ensure their individual maximum ripple current limits are not exceeded. Inductor L1 and capacitors C15 and C16 provide switching noise filtering.

Output voltage is controlled using a TL431 reference IC. Resistor R15, R16 and R17 form a potential divider to sense the output voltage. Resistor R12 and R24 together limit the optocoupler LED current and set overall control loop DC gain. Control loop compensation is achieved using additional components, C12, C13, C20 and R13. Diode D6 and capacitor C19 form a soft finish network. This feeds current into the control pin prior to output regulation, preventing output overshoot and ensuring startup under low line, full load conditions.

Sufficient heat sinking is required to keep the TOPSwitch-HX device below 110 °C when operating under full load, low line and maximum ambient temperature. Airflow may also be required if a large heat sink area is not acceptable.

A High Efficiency, 20 W Continuous – 80 W Peak, Universal Input Power Supply

The circuit shown in Figure 24 takes advantage of several of TOPSwitch-HX features to reduce system cost, power supply size and improve power supply efficiency while delivering significant peak power. This design delivers 20 W continuous and 80 W peak at 32 V from an 85 VAC to 265 VAC input. A nominal efficiency of 82% at full load is achieved using TOP258MN.

The M-package part has an optimized current limit to enable design of power supplies capable of delivering high power for a short duration.

Resistor R12 programs the current limit of the TOPSwitch-HX. Resistors R11 and R14 provide a signal that reduces the current limit with increasing DC bus voltage, thereby maintaining a constant overload power level with increasing line voltage. Resistors R1 and R2 implement the line undervoltage and overvoltage function and also provide feed forward compensation for reducing line frequency ripple in output. The overvoltage feature stops TOPSwitch-HX switching during a line surge, extending the high voltage withstand voltage to 700 V without device damage.

The snubber circuit comprising VR7, R17, R25, C5 and D2 limits the maximum drain voltage and dissipates energy stored in the leakage inductance of transformer T1. This clamp configuration maximizes energy efficiency by preventing C5 from discharging below the value of VR7 during the lower frequency operating modes of TOPSwitch-HX. Resistor R25 damps high frequency ringing for reduced EMI.

A combined output overvoltage and over power protection circuit is provided via the latching shutdown feature of TOPSwitch-HX and R20, C9, R22 and VR5. Should the bias winding output voltage across C13 rise due to output overload or an open loop fault (optocoupler failure), then VR5 conducts, triggering the latching shutdown. To prevent false triggering due to short duration overload, a delay is provided by R20, R22 and C9.

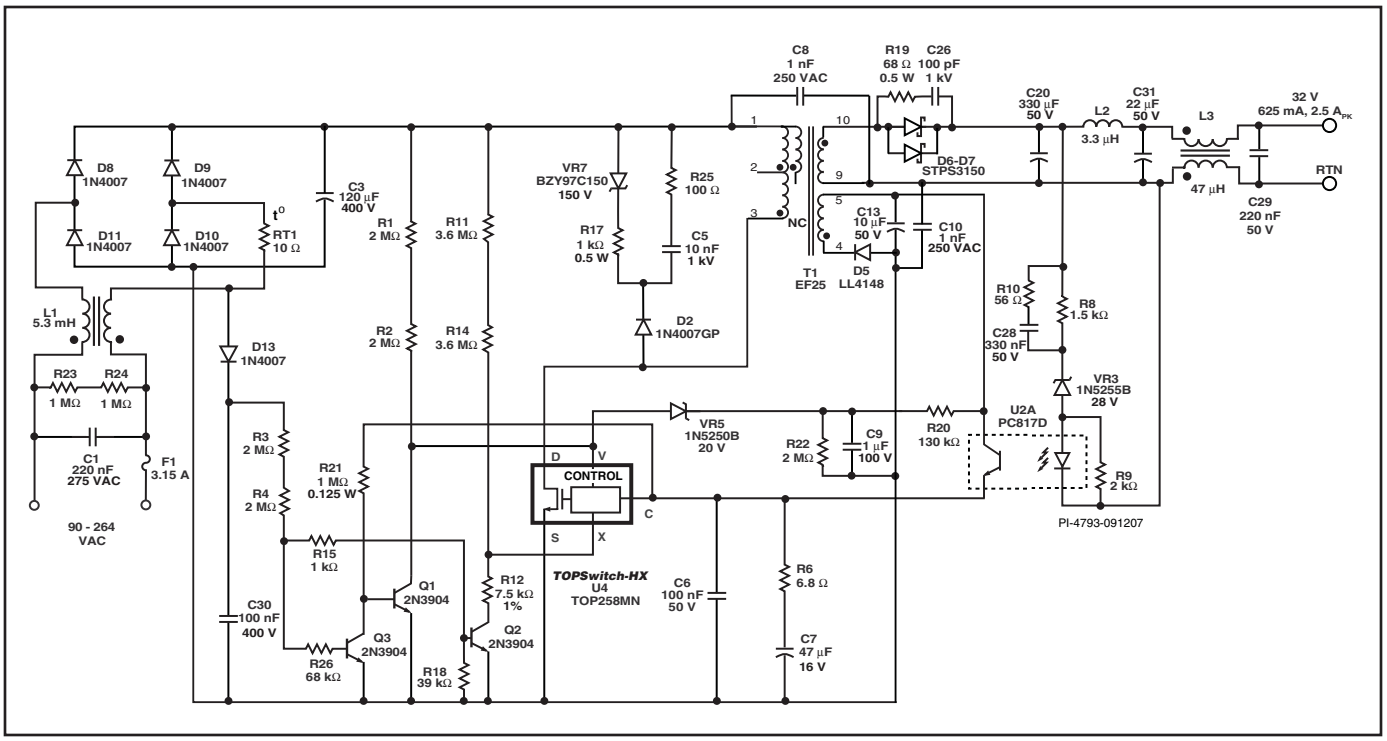

Figure 24. 20 W Continuous, 80 W Peak, Universal Input Power Supply.

To reset the supply following a latching shutdown, the V pin must fall below the reset threshold. To prevent the long reset delay associated with the input capacitor discharging, a fast AC reset circuit is used. The AC input is rectified and filtered by D13 and C30. While the AC supply is present, Q3 is on and Q1 is off, allowing normal device operation. However when AC is removed, Q1 pulls down the V pin and resets the latch. The supply will then return to normal operation when AC is again applied.

Transistor Q2 provides an additional lower UV threshold to the level programmed via R1, R2 and the V pin. At low input AC voltage, Q2 turns off, allowing the X pin to float, and thereby disables switching.

A simple feedback circuit automatically regulates the output voltage. Zener VR3 sets the output voltage together with the voltage drop across series resistor R8, which sets the DC gain of the circuit. Resistors R10 and C28 provide a phase boost to improve loop bandwidth.

Diode D6 is a low loss Schottky rectifier, and capacitor C20 is the output filter capacitor. Inductor L3 is a common mode inductor to limit radiated EMI when long output cables are used and the output return is connected to safety earth ground. Examples of this include PC peripherals such as inkjet printers.

A High Efficiency, 35 W, Dual Output - Universal Input Power Supply

The circuit in Figure 25 takes advantage of several of the TOP Switch-HX features to reduce system cost and power supply size and to improve efficiency. This design delivers 35 W total output power from a 90 VAC to 265 VAC input at an ambient of 50º C in an open frame configuration. A nominal efficiency of 84 % at full load is achieved using TOP258PN. With a DIP-8 package, this design provides 35 W continuous output power using only the copper area on the circuit board underneath the part as heat sink. The different operating modes of the TOPSwitch-HX provide significant improvement in the no-load, standby, and light load performance of the power supply as compared to previous generations of TOPSwitch.

Resistors R1 and R2 provide line sensing, setting UV at 95 VDC and OV at 445 VDC.

Diode D5, together with resistors R7, R6, capacitor C6 and Zener VR1, forms a clamp network that limits the drain voltage after the MOSFET inside the TOPSwitch turns OFF. Zener VR1 provides a defined maximum clamp voltage and typically only conducts during fault conditions such as overload. This allows the RCD clamp (R6, R7, C6 and D5) to be sized for normal operation, thereby maximizing efficiency at light load.

Should the feedback circuit fail, output of the power supply will exceed regulation limits. This increased voltage at output will also result in an increased voltage at the output of the bias winding. Zener VR2 will break down, and current will flow into the “M” pin of the TOPSwitch, initiating hysteretic overvoltage protection. Resistor R5 will limit the current into the M pin; if latching OVP is desired, the value of R5 can be reduced to 20 Ω.

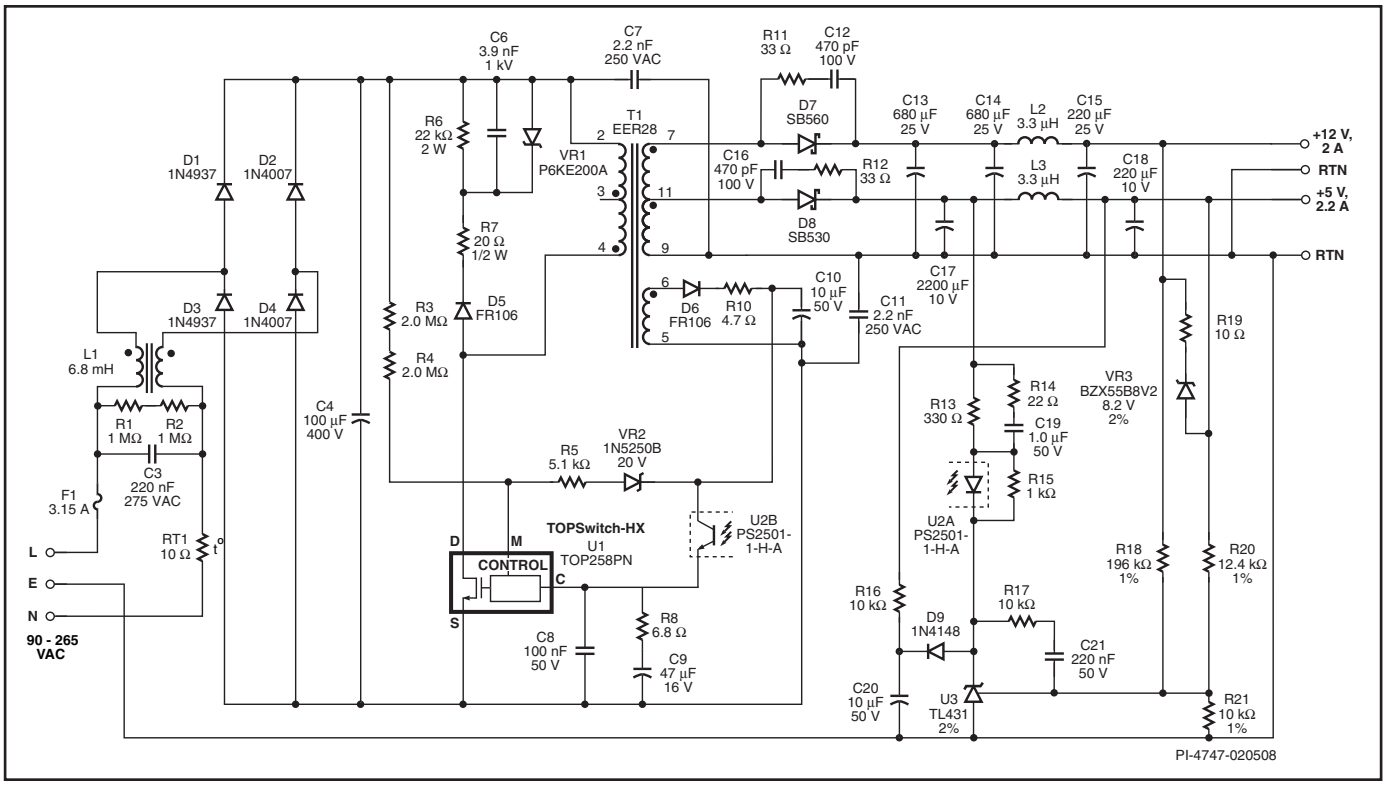

Figure 25. Universal Input, 35W Power Supply Using TOP258PN.

Output voltage is controlled using the amplifier TL431. Diode D9, capacitor C20 and resistor R16 form the soft finish circuit. At start, capacitor C20 is discharged. As the output voltage starts rising, current flows through the optocoupler diode inside U2A, resistor R13 and diode D9 to charge capacitor C20. This provides feedback to the primary circuit. The current in the optocoupler diode U2A gradually decreases as the capacitor C20 becomes charged and the control amplifier IC U3 becomes operational. This ensures that the output voltage increases gradually and settles to the final value without any overshoot. Diode D9 ensures that the capacitor C23 is maintained charged at all times after startup, which effectively isolates C20 from the feedback circuit after start-up. Capacitor C23 discharges via R16 when the power supply shuts down. Resistor R18, R20 and R21 form a voltage divider network. The output of this divider network is primarily dependent on the divider circuit formed using R20 and R21 but modified by changes in voltage at the 12 V output due to the connection of resistor R18 to the output of the divider network.

Resistor R19 and VR3 improve cross regulation in case only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification.

A High Efficiency, 65 W, Universal Input Power Supply

The circuit shown in Figure 26 delivers 65 W (19 V @ 3.42 A) at 88% efficiency using a TOP260EN operating over an input voltage range of 90 VAC to 265 VAC.

Capacitors C1 and C6 and inductors L1 and L2 provide common mode and differential mode EMI filtering. Capacitor C2 is the bulk filter capacitor that ensures low ripple DC input to the flyback converter stage. Capacitor C4 provides decoupling for switching currents, reducing differential mode EMI.

In this example, the TOP260EN is used at reduced current limit to improve efficiency.

Resistors R5, R6 and R7 provide power limiting, maintaining relatively constant overload power with input voltage. Line sensing is implemented by connecting a 4 MΩ impedance from the V pin to the DC rail. Resistors R3 and R4 together form the 4 MΩ line sense resistor. If the DC input rail rises above 450 VDC, then TOP Switch-HX will stop switching until the voltage returns to normal, preventing device damage.

This circuit features a high efficiency clamp network, consisting of diode D1, zener VR1 and capacitor C5, together with resistors R8 and R9. The snubber clamp is used to dissipate the energy into the leakage reactance of the transformer. At light load levels, very little power is dissipated by VR1, improving efficiency as compared to a conventional RCD clamp network. The secondary output from the transformer is rectified by diode D2 and filtered by capacitors C13 and C14. Ferrite Bead L3 and capacitor C15 form a second stage filter and effectively reduce the switching noise to the output.

Output voltage is controlled using a LM431 reference IC. Resistors R19 and R20 form a potential divider to sense the output voltage. Resistor R16 limits the optocoupler LED current and sets the overall control loop DC gain. Control loop compensation is achieved using C18 and R21. The components connected to the control pin on the primary side, C8, C9 and R15, set the low frequency pole and zero to further shape the control loop response. Capacitor C17 provides a soft finish during startup. Optocoupler U2 is used for isolation of the feedback signal.

Diode D4 and capacitor C10 form the bias winding rectifier and filter. Should the feedback loop break due to a defective component, a rising bias winding voltage will cause the Zener VR2 to break down and trigger the over voltage protection, which will inhibit switching.

An optional secondary side over voltage protection feature that offers higher precision (as compared to sensing via the bias winding) is implemented using VR2, R14 and U2. Excess voltage at the output will cause current to flow through the optocoupler U3 LED, which in turn will inject current in the V-pin through resistor R13, thereby triggering the over voltage protection feature.

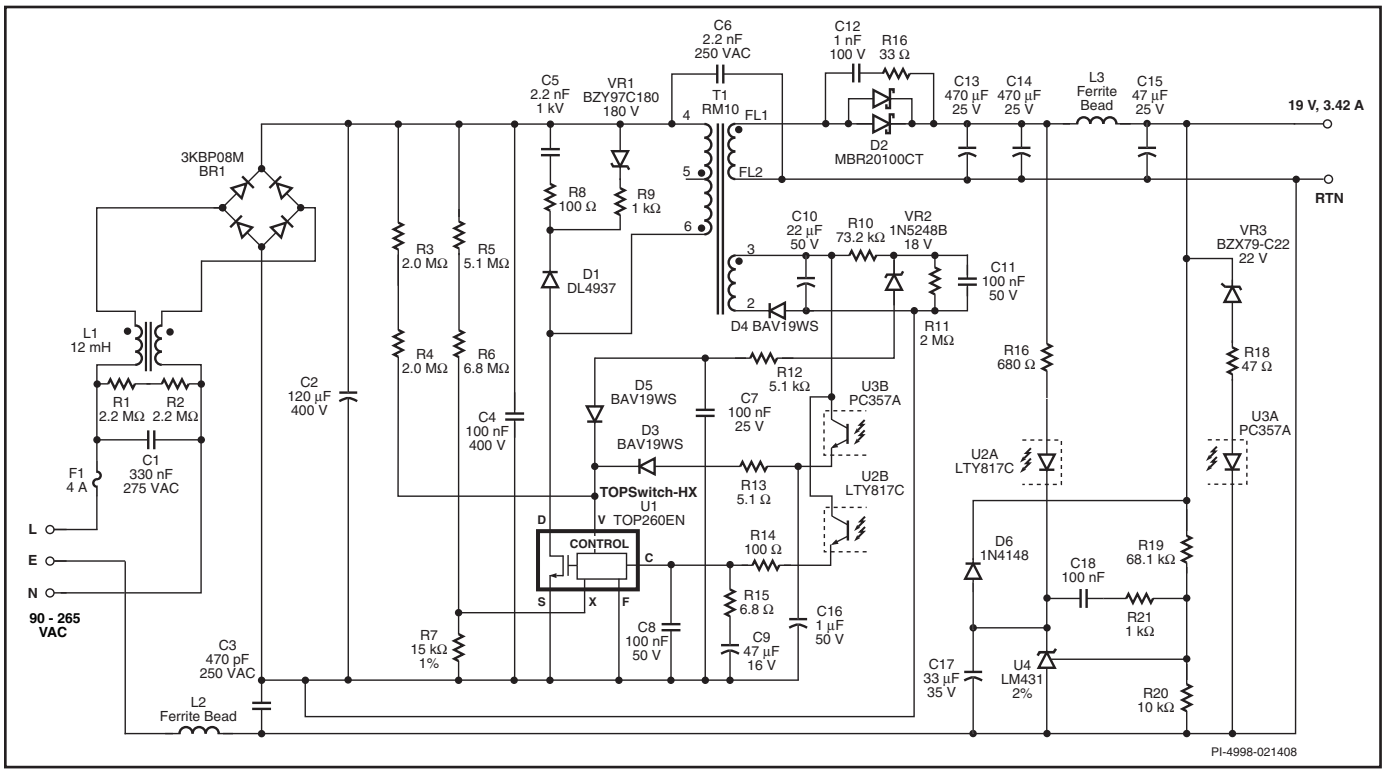

Figure 26. 65 W, 19 V Power Supply Using TOP260EN.

Appendix B

Multiple Output Flyback Power Supply Design

The only difference between a multiple output flyback power supply and a single output flyback power supply of the same total output power is on the secondary side design.

Design with Lumped Output Power

A simple multiple output flyback design is described in detail in AN-22, "Designing Multiple Output Flyback Power Supplies with TOPSwitch." The design method starts with a single output equivalent by lumping output power of all outputs to one main output. Secondary peak current ISP and RMS current I_{SRMS} are derived. Output average current I_O, corresponding to the lumped power, is also calculated.

Assumption for Simplification

The current waveforms in the individual output windings are determined by the impedance in each circuit, which is a function of leakage inductance, rectifier characteristics, capacitor value and output load. Although this current waveform may not be exactly the same from output to output, it is reasonable to assume that, to the first order, all output currents have the same shape as for the single output equivalent of combined circuit.

Output RMS Current vs. Average Current

The output average current is always equal to the DC load current, while the RMS value is determined by current wave shape. Since the current wave shapes are assumed to be the same for all outputs, their ratio of RMS to average currents must also be identical. Therefore, with the output average current known, the RMS current for each output winding can be calculated as

$$I_{SRMS}(n) = I_O(n) \times \frac{I_{SRMS}}{I_O}$$

where $I_{SRMS(n)}$ and $I_{O(n)}$ are the secondary RMS current and output average current of the nth output, and I_{SRMS} and I_O are the secondary RMS current and output average current for the lumped single output equivalent design.

Customization of Secondary Designs for Each Output

The turns for each secondary winding are calculated based on the respective output voltage $V_{O(n)}$:

$$N_S(n) = N_S \times \frac{V_O(n) + V_D(n)}{V + V_D}$$

Output rectifier maximum inverse voltage is

$$PIV_S(n) = V_{MAX} \times \frac{N_S(n)}{N_P} + V_O(n)$$

With output RMS current $I_{SRMS(n)}$, secondary number of turns $N_{S(n)}$ and output rectifier maximum inverse voltage $PIV_{S(n)}$ known, the secondary side design for each output can now be carried out exactly the same way as for the single output design.

Secondary Winding Wire Size

The TOPSwitch-HX design spreadsheet assumes a CMA of 200 when calculating secondary winding wire diameters. This gives the minimum wire sizes required for the RMS currents of each output using separate windings. Designers may wish to use larger size wire for better thermal performance. Other considerations, such as skin effect and bobbin coverage, may suggest the use of a smaller wire by using multiple strands wound in parallel. In addition, practical considerations in transformer manufacturing may also dictate the wire size.

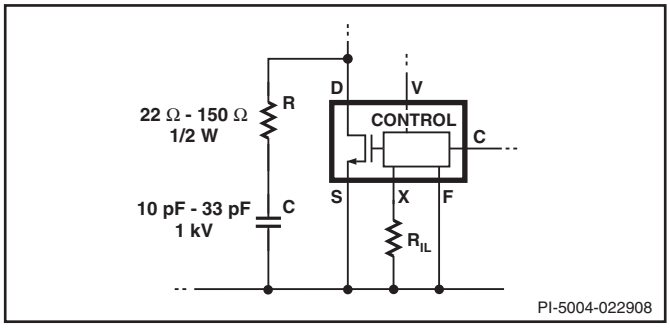

Figure 27. Recommended Snubber for Larger (TOP259-TOP261) TOPSwitch-HX Devices.

Notes

Revision	Notes	Date
A	Initial Release	9/07
B	Text changes	9/07
C	Style, formatting and renumbering	10/07
D	Added high-power TOPSwitch-HX information	03/08

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