STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Device Operation

GENERAL DESCRIPTION

All ISD single-chip voice record/playback devices are analog sampled data systems. Current product offerings include the ISD1000A series, the ISD1100 series, the ISD1200 series, the ISD1400 series, and the ISD2500 series. Each series member has an on-chip microphone preamplifier, AGC, antialiasing and smoothing filters, high-density multilevel storage array, speaker driver, control interface and internal precision reference clock. The difference between the ISD technology and other competing voice storage technologies is that no A-D or D-A converters are required. As each sample is taken, it is temporarily stored in a sample and hold circuit and eventually "recorded" into a single EEPROM cell. Since we are recording with the equivalent of 8 bits of accuracy, it would require 3.8 million bits of digital memory (as well as the A-D and D-A converters) to equal the 480,000 cells contained in the ISD2500 series device's storage array.

The sample rates versus storage time and filter upper pass band for each device in the above series are shown in Table 1. Filter specification applies to the antialiasing filter and the smoothing filter.

How the frequency response is determined will be covered later in this document.

NOTE *All pin numbers quoted assume a DIP package and an ISD1000A, ISD1100, ISD1200, ISD1400 or ISD2500 device.*

Table 1: Sample Rate, Storage Time, and Frequency Response

Device Part Number	Sample Rate (KHz)	Storage Time (seconds)	Filter Pass Band (Hz)
ISD1016A	8.0	16	3400
ISD1020A	6.4	20	2700
ISD1110	6.4	10	2600
ISD1112	5.3	12	2200
ISD1210	6.4	10	2600
ISD1212	5.3	12	2200
ISD1416	8.0	16	3300
ISD1420	6.4	20	2600
ISD2532/60	8.0	32/60	3400
ISD2540/75	6.4	40/75	2700
ISD2548/90	5.3	48/90	2300
ISD2564/120	4.0	64/120	1700

All analog circuits in the ISD device series are referenced to an internally generated analog ground bias of approximately 1.5 volts. A designer can measure this bias level externally at the MIC INPUT (pin 17), MIC REF (pin 18), and ANA IN input (pin 20). This measurement will be within ±20 mV of the internal value. All connections to these pins should be capacitively coupled so that this bias is not disturbed.

MIC (PIN 17)

The on-chip microphone amplifier is designed to amplify signals in the 1 to 20 millivolt range. This gain controlled transconductance amplifier has an input impedance of ≈10 KΩ and a maximum gain of 24 dB. A typical electret microphone supplies a level adequate to drive this amplifier. Since the input impedance is known, the low end frequency response is determined by the audio source and the input coupling capacitor. In the ISD1000A data sheet example, an electret microphone is used with a 0.1 μF coupling capacitor. This becomes a high pass filter with an approximate low end cutoff frequency response of 160 Hz. This is determined by first assuming that the input signal will be attenuated 3 dB at frequencies below where the reactance of the input capacitor equals the internal impedance of the microphone input. The equation for this is:

$$F_{3dB} = \frac{1}{2\pi RC}$$

Since R nominally equals 10 KΩ, this equation may be further simplified to:

$$F_{3dB} = \frac{1}{62832 \times C}$$

where C is in Farads

An on-chip AGC circuit controls the gain of the microphone preamplifier. Its gain will vary from 0 to 20 dB as required to maintain an appropriate input level.

MIC REF (PIN 18)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise canceling or common mode rejection input to the device. The preferred circuit for connecting the microphone is the differential circuit illustrated in the "Microphone and Speaker Selection" section of Application Information. This configuration gives even better noise rejection than the next method. Alternatively, a capacitor is connected from this pin to analog ground. This capacitor should have exactly the same value as the Microphone preamplifier input coupling capacitor. The ground for the microphone should be physically close to the ground connection for the MIC REF capacitor. The addition of this "noise-canceling" input gives approximately 10 dB of improvement in the background noise level over not using it. If this input is not used, it must be left unconnected.

AGC (PIN 19)

The applications schematic in the data sheet shows R2 and C2 connected from pin 19 to ground. These two components set up the attack and release time constants for the internal Automatic Gain Control circuit in the microphone preamplifier. The attack time is determined by a network consisting of an internal R and external C while the release time is determined by the two external components in parallel. Nominal values of 470 KΩ (R2) and 4.7 μF (C2) give satisfactory results in most cases.

ANA OUT (PIN 21)

ANA OUT is the direct output of the microphone preamplifier. In a typical application, this output is capacitively coupled to the ANA IN pin.

ANA IN (PIN 20)

The ANA IN pin feeds an input amplifier with an input impedance of ≈2.7 KΩ. As with the microphone input, the coupling capacitor that connects ANA IN to ANA OUT sets the low end frequency response of this section of the circuit. With the ISD1000A data sheet circuit example value of 0.1 μF for C1 and C3, the system low end frequency response is the series combination of these two single pole high pass filters. Since the MIC circuit has a pole at approximately 160 Hz, the result will be a system high pass with a 3 dB point at a slightly higher frequency than either pole or approximately 600 Hz. With the 4.5 to 6.5 VDC operating voltage range of a 5.1 KΩ resistor is normally used in series with the coupling capacitor to slightly drop the voltage fed to the array to prevent distortion; this changes the frequencies slightly.

ANTIALIASING AND SMOOTHING FILTERS

The antialiasing and smoothing filters are actually a single filter that is multiplexed into each circuit function as needed for Record and Playback. This filter is constructed using conventional (non-switched capacitor) circuit techniques with no external components. It is a 5-pole Chebychev filter with <2 dB of ripple. The 3 dB point of this filter is set for each of the devices in the ISD series. The response is in Table 1 at the beginning of this section.

SAMPLE AND HOLD REGISTERS

Some of the complexity of the internal design of the ISD devices can be grasped once the user understands the internal workings of the device. Looking only at the ISD1016A device during Record, samples are taken of the incoming waveform every 125 μs (8 KHz sample rate). It takes about 10 ms to "record" an incoming sample into the storage array. Therefore two banks of at least 80 sample and hold registers are required to buffer the incoming samples. It is the hold time of these capacitors that determine the minimum sample frequency. One bank will be receiving incoming samples serially in real-time while the other bank is connected in parallel to program multiple cells simultaneously.

STORAGE ARRAY

The EEPROM storage array of the ISD1000A series is organized as 160 rows. Other ISD device series may have a different organization. In a later chapter you will find out how to control where a message can be started for record or playback. In the ISD1000A series there are 160 possible starting addresses; you start record or playback from the beginning of one of the 160 rows. Whenever a message is recorded or played back, you proceed through a row until the end, at which time the internal row address counter advances by one and you continue at the beginning of the next row. The address counter is internal to the ISD devices. The address pins of the device are inputs only. The "current" address is not directly available.

$\overline{\text{EOM}}$ (PIN 25) AND EOM BITS (ISD1000A AND ISD2500 SERIES)

An inherent requirement for addressing multiple words or "messages" in the ISD1000A and ISD2500 devices is knowing where the message ends. Anytime a Record cycle is stopped by a rising $\overline{\text{CE}}$ signal, an EOM bit is set in a separate digital EEPROM memory inside the ISD device. When a message playback is begun with a pulsed $\overline{\text{CE}}$ signal, that playback will continue until an EOM bit is found.

Each of the rows of the storage array in an ISD1000A or ISD2500 device is addressed individually. There are four evenly spaced EOM locations that point into each row. In the ISD1000A device, this equates to 4 x 160 or 640 EOM locations. The ISD2500 series devices have 4 X 600 or 2400 possible EOM locations. The 8 KHz sample rate products available from ISD are addressable on 100 millisecond boundaries and the EOM resolution is 25 ms. Thus the maximum delay from the end of a message to the output of an $\overline{\text{EOM}}$ signal is 25 ms. The $\overline{\text{EOM}}$ signal is low going and lasts for 12.5 ms. The rising edge of $\overline{\text{EOM}}$ actually marks the end of the message. So, audio will continue to be output from a ISD device during the time $\overline{\text{EOM}}$ is low and will stop at its rising edge. These times will vary with other sample rate devices available from ISD. See the appropriate ISD data sheet for these timings.

In the ISD1000A series, the $\overline{EOM}$ pin also carries the Overflow indication. At Overflow in playback, the $\overline{EOM}$ pin will go LOW and stay LOW until Overflow is cleared. At Overflow in record, the $\overline{CE}$ input signal will transfer to the $\overline{EOM}$ output.

$\overline{RECLED}$ (PIN 25) AND EOM BITS (ISD1100, ISD1200 AND ISD1400 SERIES)

This pin on the ISD1100, ISD1200, and ISD1400 series carries two signals. The identified signal, $\overline{RECLED}$, pulls LOW at the start of a Record operation initiated by taking the $\overline{REC}$ pin LOW. It has adequate drive capability to control an LED through a 1 KΩ resistor to V_{CC}. This signal will go back HIGH at the end of a Record operation when the $\overline{REC}$ pin is taken back HIGH or the end of the device memory is reached.

The ISD1100, ISD1200, and ISD1400 series also contain an EOM structure similar to that in the ISD1000A series. There are half as many possible EOM bits per row, however, giving a 50 ms. End of Message resolution, for instance, in the ISD1416 device. To maintain the ability to determine when a Playback cycle is finished, the $\overline{RECLED}$ pin also carries an $\overline{EOM}$ signal. It pulses LOW at the end of a message during a Playback cycle. If this pin is connected to an LED as indicated in the previous paragraph, it may be seen to "blink" on momentarily at the end of each message during playback.

There is no Overflow signal in the ISD1100, ISD1200, and ISD1400 series. If a message ends at the end of the device memory, an EOM bit is set at memory end. When this message is played back, a normal LOW going EOM pulse is generated to the $\overline{RECLED}$ pin.

$\overline{OVF}$ (PIN 22, ISD2500 SERIES ONLY)

One of the major features added in the ISD2500 was the separation of the Overflow ($\overline{OVF}$) and end-of-message ($\overline{EOM}$) output signals into two separate pins, $\overline{OVF}$ and $\overline{EOM}$. This more efficiently enables multi-device cascade. In the ISD2500 series, the $\overline{EOM}$ pin only pulses LOW during playback when a set EOM bit is encountered. It **does not** pulse LOW at Overflow. Instead, the $\overline{OVF}$ pin pulses LOW for approximately 6 ms when an Overflow condition is reached.

After Overflow is reached, the $\overline{CE}$ signal is coupled through the device to the $\overline{OVF}$ output. This means that the input $\overline{CE}$ signal "appears" at the $\overline{OVF}$ output of any device in overflow.

To understand why this operates this way, consider several ISD2500 devices connected in cascade. To cascade properly, each $\overline{OVF}$ is connected to the $\overline{CE}$ of the following device. The $\overline{OVF}$ of the final device will be discussed later. The $\overline{CE}$ now "daisy chains" through devices that are in overflow. Changing the state or pulsing $\overline{CE}$ LOW at the input of the first device in cascade will directly control the first device down the line that is not in overflow.

Operation of $\overline{OVF}$ in Record

Since the $\overline{CE}$ signal is held LOW during recording, $\overline{OVF}$ goes LOW and stays LOW at Overflow. It does not pulse LOW. When the $\overline{CE}$ input goes LOW, $\overline{OVF}$ follows it LOW.

Operation of $\overline{OVF}$ in Playback

Normal Playback operations begin by pulsing $\overline{CE}$ LOW and then back HIGH. In this case, the $\overline{OVF}$ pin will pulse LOW at Overflow to cause playback to begin in the next device in the cascade. If the system uses a continuous LOW $\overline{CE}$ during Playback, the $\overline{OVF}$ pin will go LOW and stay LOW at Overflow. The LOW pulse will not be output.

NOTE *The $\overline{EOM}$ output of the ISD2500 series device does not pulse LOW when the Overflow condition is reached. A message being played back can end with a set EOM bit, or, because it runs into overflow. If the designer needs a single logic output to indicate that a message has ended, it is necessary to or the $\overline{EOM}$ and $\overline{OVF}$ outputs together. Since these are active LOW signals, a two-input and gate may be used to generate an active LOW combined signal. Alternatively, two diodes and a pull up resistor may be used. (Note that the $\overline{OVF}$ signal is a 6 µs long pulse.)*

SPEAKER OUTPUT, SP+ (PIN 14) & SP– (PIN 15)

The ISD devices include a differential speaker driver. It has the capability to drive 50 milliwatts into 16 Ω from the AUX IN pin. From the memory array, with a properly recorded signal, it will provide 12.6 mW output power. The signals are exactly 180 degrees out of phase. A lower impedance speaker may be used but distortion and peak I_{CC} current will increase as the speaker impedance decreases. Do not use an impedance less than 8 Ω. These outputs may be used single ended with the signal taken from either pin but should never be shorted together or tied to ground. When driving a single ended connection, capacitive coupling is recommended because of the possible large DC bias current that could result (100 mA). If the outputs are used single ended, the unused pin must be left unconnected. **Do not ground the unused output.**

When the power-down pin is low (device powered up) and the Playback/Record pin is high (Playback Mode) both speaker pins will be at an average value of about 1.5 volts. When the device is in Record or is Powered Down, the two speaker outputs will be pulled hard to ground. **Do not parallel the speaker outputs with other signals without taking this into consideration. The speaker outputs can sink and source large amounts of current!**

The speaker outputs are internally pulled to ground to protect the output transistors on the ISD devices. Remember, these outputs are normally connected to a speaker. A speaker is an electromechanical device with the ability to inductively generate a large voltage spike if abruptly struck or dropped.

AUX INPUT (PIN 11, ISD1000A AND ISD2500 SERIES)

When an ISD device is in the Playback Mode (Playback/Record Pin 27 HIGH), not powered down (power-down Pin 24 LOW) and not actively playing back a message, the AUX IN is an input to the speaker output. This analog path to the differential speaker driver has a voltage gain of a little less than 0 dB. The input impedance is ≈10 KΩ to analog ground. Other signal sources can therefore use the speaker output drivers. This input is also used in Cascading applications. This pin is not connected on the ISD1100, ISD1200, and ISD1400 devices.

$\overline{\text{PLAYL}}$ (PIN 23, ISD1100, ISD1200, AND ISD1400)

The $\overline{\text{PLAYL}}$ pin starts a Playback cycle when taken LOW. The Playback cycle will continue until an EOM is reached as long as $\overline{\text{PLAYL}}$ is held LOW. If the $\overline{\text{PLAYL}}$ pin is taken back HIGH during playback, playback will immediately stop. When playback stops (because of $\overline{\text{PLAYL}}$ going LOW or an EOM being reached) the device will automatically go into a power-down state.

The $\overline{\text{PLAYL}}$ pin may also be used to interrupt a Playback cycle initiated by the $\overline{\text{PLAYE}}$ pin by cycling $\overline{\text{PLAYL}}$ LOW then back HIGH. A Playback cycle may also be interrupted by the $\overline{\text{REC}}$ pin. See the heading entitled "$\overline{\text{REC}}$ (Pin 27, ISD1100, ISD1200, and ISD1400)" below.

The ISD1100 device has a pull-up resistor to V_{CC} on the $\overline{\text{PLAYL}}$ pin. This pull-up resistor is approximately 100 KΩ.

$\overline{\text{PLAYE}}$ (PIN 24, ISD1100, ISD1200, AND ISD1400)

The $\overline{\text{PLAYE}}$ pin starts a Playback cycle when taken LOW. This is an edge triggered event and playback will continue, even if $\overline{\text{PLAYE}}$ is taken back HIGH. Playback will stop when a set EOM bit is reached or interrupted by the $\overline{\text{PLAYL}}$ pin as explained above. When playback stops, the device will automatically power-down. A Playback cycle may also be interrupted by the $\overline{\text{REC}}$ pin. See the heading entitled "$\overline{\text{REC}}$ (Pin 27, ISD1100, ISD1200, and ISD1400)" below.

The ISD1100 device has a pull-up resistor to V_{CC} on the $\overline{PLAYE}$ pin. This pull-up resistor is approximately 100 KΩ.

$\overline{REC}$ (PIN 27, ISD1100, ISD1200, AND ISD1400)

The $\overline{REC}$ pin initiates a Record cycle when taken LOW. This is a level activated signal and Record will end when $\overline{REC}$ is taken back HIGH. The device will automatically power down when $\overline{REC}$ goes HIGH.

NOTE *If $\overline{REC}$ is held LOW after the end of device memory is reached, the device will not power down until this pin is allowed to go back HIGH.*

The $\overline{REC}$ control pin takes priority over both $\overline{PLAYL}$ and $\overline{PLAYE}$ pins. Taking $\overline{REC}$ LOW during a Playback cycle will immediately interrupt playback and begin a Record cycle.

The ISD1100 device includes a pull-up resistor to V_{CC} on the $\overline{REC}$ pin. This pull-up resistor is approximately 100 KΩ.

MICROCONTROLLER INTERFACE (PINS 23, 24, 27, ISD1000A AND ISD2500 SERIES)

The $\overline{CE}$, PD and P/$\overline{R}$ pins on the ISD devices are internally debounced. They can be driven by toggle switches. There will be a number of circuit examples given later to demonstrate their ease of use in various applications. These same inputs are flexible enough, however, to be driven from a microcontroller. The above named pins along with $\overline{EOM}$ are all TTL compatible and can be driven from a microcontroller system.

NOTE *The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible. If a device is to be used on a bus oriented system, the address lines must be buffered and latched.*

OVERFLOW (ISD1000A, ISD2500)

The internal logic of ISD devices is designed to allow easy cascading of chips. This will extend the total storage time available to the user. To accomplish this, the device changes Operation Modes when completely full. This change in mode is called Overflow. Once a device is in Overflow, it will not respond to a new $\overline{CE}$ cycle until cleared from this state. In both the ISD1000A and ISD2500 device series, a PD cycle is required to clear the Overflow state. The length of power-down cycle required to reset an Overflow condition is T_{SET}. The device will now respond to a $\overline{CE}$ pulse.

The ISD1100, ISD1200, and ISD1400 series do not have a comparable Overflow state.

PRECISION CLOCK WITH EXTERNAL DRIVE (PIN 26)

The ISD devices include an on-chip temperature compensated reference oscillator that controls the sample rate of the device. This oscillator requires no external parts. The sample rate is derived from a set of dividers following the internal oscillator circuitry.

An external clock may be used to drive the ISD devices through the XCLK pin (Pin 26). Driving from an external clock can be useful for system synchronization. Otherwise, this pin is normally tied LOW to ensure that the internal oscillator drives the device. If a TTL level clock is fed into this pin, the internal oscillator switches off and the external clock runs the device. The XCLK pin feeds a ÷2 flip-flop. Thus, the external clock must be twice the desired internal clock. It also means that the duty cycle of the external clock drive is not important.

NOTE *Care should be taken to ensure that the 1 and 0 logic level requirements are met when driving any ISD device input. Over or under shoot outside the data sheet limits may cause an increase in device noise. This is especially important when externally driving the XCLK pin.*

It is important to remember that the antialiasing and smoothing filters are fixed and do not change with the external clock rate. As a result, it is possible to have problems with aliasing into the passband if the clock is driven slower than the designed speed. When the clock is driven faster than the designed speed, the filters will still control the passband upper limit to the original value and there may be no advantage in doing this. Table 2 shows the external clock speed requirement for each of the standard ISD devices.

NOTE *The frequency range is limited by factors that may change from device to device and are not tested. The ISD devices are only guaranteed to operate at their design frequency. Customers may vary this clock frequency only at their own risk. You should know that the primary factors involved in the upper and lower clock frequency limits are sample-and-hold "droop" on the low end of the range and EEPROM programming speed on the high end.*

The information under the previous heading Sample and Hold Registers, described how internal sample-and-hold registers temporarily store the analog sample until the EEPROM programming step. At some low end speed (which varies from device to device) the analog voltage stored in the sample-and-hold registers will droop unacceptably.

As you speed up the device, at some frequency there will no longer be enough time to successfully program the EEPROM storage locations. Significant reduction in signal quality will occur.

EXTERNAL CLOCK DRIVE USING THE ISD1100, ISD1200 OR ISD1400

In the ISD1000A or ISD2500 device series, some customers experienced difficulties in switching from internal to external clock and back again. Particularly, any noise or spikes at the wrong time could convince the part it was in the external mode when there was no clock present. Then the device would cease to function, ignoring all inputs until the power was removed and reapplied.

Table 2: External Clock Drive Frequencies

Device Part Number	Int. Osc. Freq. (KHz)	Ext. Drive Freq. (KHz)	Sample Rate (KHz)	Filter Pass Band (Hz)
ISD1016A	512.0	1,024.0	8.0	3400
ISD1020A	409.6	819.2	6.4	2700
ISD1110	409.6	819.2	6.4	2600
ISD1112	341.3	682.7	5.3	2200
ISD1210	409.6	819.2	6.4	2600
ISD1212	341.3	682.7	5.3	2200
ISD1416	512.0	1,024.0	8.0	3300
ISD1420	409.6	819.2	6.4	2600
ISD2532/60	512.0	1,024.0	8.0	3400
ISD2540/75	409.6	819.2	6.4	2700
ISD2548/90	341.3	682.7	5.3	2300
ISD2564/120	256.0	512.0	4.0	1700

The ISD1100, ISD1200, and ISD1400 series is designed so the device will not end up in a locked up state. This is accomplished by logic that automatically switches the device back to internal clock whenever the three pins, $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$, are all HIGH. In this way, the device is always looking for command inputs with the internal clock if the external clock is off.

Expressing this a different way, to use the external clock, one of the three inputs must be LOW. A recording is made by having an external clock present at the XCLK pin when $\overline{REC}$ goes LOW. The $\overline{PLAYL}$ input should be brought LOW simultaneously (or shortly after) with $\overline{REC}$. At the end of the recording $\overline{REC}$ is brought HIGH. This begins the "finish recording" process. Because the device continues to sample and record for the remaining portion of the row until it reaches an EOM location, $\overline{PLAYL}$ must be kept LOW for another 50 to 75 msec (see Figure 1). This keeps the device in the external clock mode until everything is written to memory. If only $\overline{REC}$ is used there will be a short "chirp" or change in pitch at the very end of the recording.

Playback with the external clock requires that the $\overline{PLAYL}$ pin be used, not the $\overline{PLAYE}$. This is because the device will switch to external clock when $\overline{PLAYE}$ goes LOW but will immediately revert to the internal clock when $\overline{PLAYE}$ goes HIGH again.

For applications where one wants to vary the pitch of playback the $\overline{PLAYL}$ pin must be used for playback. Another alternative is to record with the external clock and then use the internal clock and $\overline{PLAYE}$ for playing back the messages. This eliminates the need for external timing of the $\overline{PLAYL}$ signal in playback.

NOTE *The ISD1100, ISD1200 and ISD1400 devices include a pull-down resistor to V_{SS} on the XCLK pin. This pull-down resistor is approximately 100 KΩ.*

MESSAGE ADDRESSING

The ISD devices allow the designer to select individual messages using eight or ten address input lines. From 80 to 600 individual message start locations can be addressed. Each message has an internal End Of Message (EOM) bit that is saved with a recording to indicate when the message is complete. This capability is discussed in detail in the Basic Addressing section page 8.

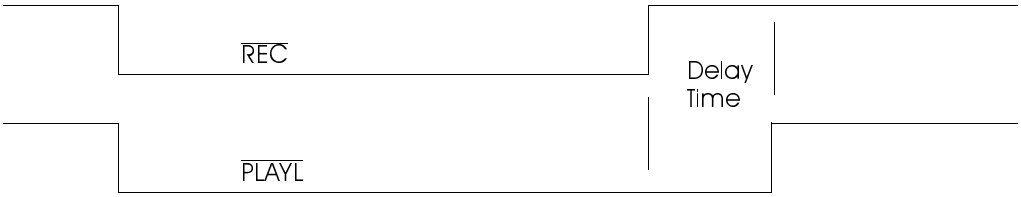
The ISD1100 device includes pull-up resistors to V_{CC} on address lines A6 and A7 and pull-down resistors to A0 through A5. These pull-up or pull-down resistors are approximately 100 KΩ.

NOTE *The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible. If a device is to be used on a bus oriented system, the address lines must be buffered and latched.*

Table 3: Delay Time from $\overline{\text{REC}}$ to $\overline{\text{PLAYL}}$ Rising Edges

Device Type	Duration (seconds)	Internal Sample Rate (KHz)	Delay Time to Finish Recording (msec)
ISD1110/ISD1210	10	6.4	62.50
ISD1112/ISD1212	12	5.3	75.00
ISD1416	16	8.0	50.00
ISD1420	20	6.4	62.50

Figure 1: Delay Time from $\overline{\text{REC}}$ to $\overline{\text{PLAYL}}$ Rising Edges



OPERATIONAL MODES

The address maps of the ISD devices have unique address locations set aside for special operating modes. This part of the address map is unique in that all Operational Modes use addresses with the two most significant address bits HIGH simultaneously. These do not latch. An Operational Mode function is only in effect for the operational cycle initiated by the falling edge $\overline{\text{CE}}$ (ISD1000A or ISD2500) or on the falling edge of $\overline{\text{PLAYL}}$, $\overline{\text{PLAYE}}$, or $\overline{\text{REC}}$ (ISD1100, ISD1200, and ISD1400). If an Operational Mode is not selected in the next operational cycle, a plain address cycle will be performed.

Because the Operational Modes do not latch, the user cannot simultaneously address individual messages and execute an Operational Mode. All Operational Modes start at address <00000000> unless they themselves modify or control chip addressing. The Operational Modes are discussed in detail under the Application "Operational Modes."